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Fan Control with Reduced Control Signals

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Fan Control with Reduced Control Signals

Server fan control is currently achieved by transmitting PWM pulses directly to each individual system fan through a controller IC (Integrated Circuit). Each signal is directed serially from a controller port in a 1:1 fashion to each fan. This can lead to the following problems and limitations:

- (a) As the complexity of server design increases, there is a limit to the number of fans that can be directly controlled and routed on each system. Some server chassis house multiple individual server nodes cooled by a shared mass array of fans. The maximum number of fans that can be supported by the system is then limited by the number of PWM output ports available on the controller. To support more fans in the system, the designer may have to select a different controller with more PWM output ports, or add an additional controller cascaded to support more PWM output ports, resulting in a higher cost burden on the system design.
- (b) When a higher total number of fans supported goes up, the increased number of control signals that needs to be routed in PCB design goes up proportionally. This adds to increased physical size of the PCB design as fan PWM signals are noisy signals that require them to be spaced apart an appropriate distance from each other, as well as routed a “keep way” distance apart from more sensitive signals that may be affected by the noise generated. (For implementation in systems with integrated fans)
- (c) When a higher number of total fans supported goes up, the increased number of fan cables (housing control signals) that needs to be routed in the system goes up proportionally. This adds to increased cable routing complexity as the total number of cables that need to be routed through the system goes up proportionally to the number of fans required (For implementation in systems employing the use of a separate fan board)

Proposed is a mechanism for Fan Control with Reduced Control Signals (FCRCS) that utilizes readily available shift registers to control fans with a reduced number of control signals to resolve the existing problems and limitations of today’s current designs.

Current designs have each system fan directly routed to an output port on a controller, which multiplies the number of signals proportionally as the required number of total fans goes up. Figure 1 below highlights how fan control is achieved in current designs. A controller’s output port is routed directly to a fan connector or cabled to a separate fan board in a 1:1 fashion. The total number of fans that can be supported is limited by the number of available PWM output ports on the controller. Figure 2 below shows the implementation of the FCRCS mechanism, where a total of 3 serial control signals (Clock, Data, Load) can be routed to shift register(s), which will shift and output latched signals to control any number of system fans required. Figure 3 shows the current implementation

required in a server system with 16 system fans. Figure 4 employs the use of the FCRCs mechanism to reduce the control signals to 3 (down from 16 in Figure 3) while still controlling 16 system fans. Figure 5 provides an example of an existing shift register that can be used in the FCRCs design to limit the number of control signals used. Figure 6 shows the relation of the signals feeding into the shift register and being outputted. The highlighted pulses represent the separate pulses routed to each fan. In today's design, each Fan pulse shown needs to be routed individually from a controller output port to each fan. FCRCs uses three signals (clock, data, load) to input to a shift register which decodes the signals to the same individual pulses that are highlighted.

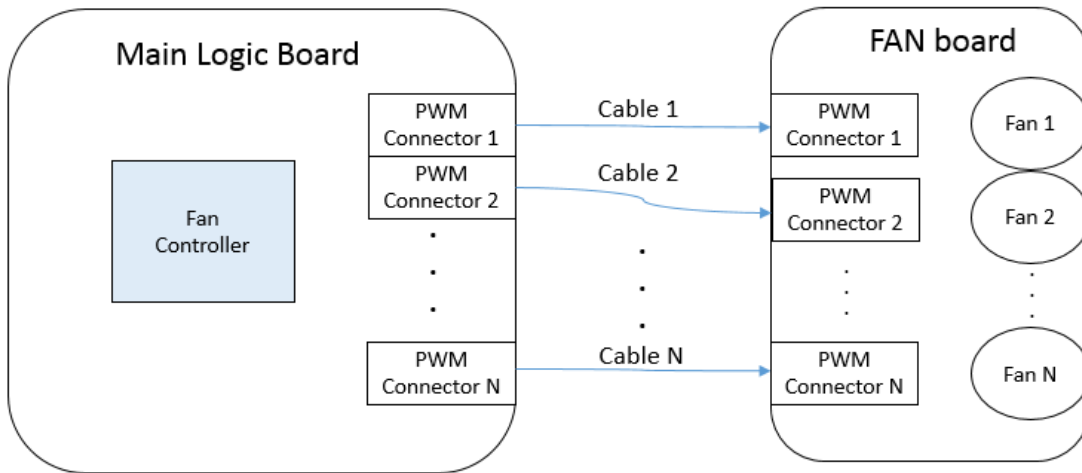


FIG. 1 Current Fan Control Implementation

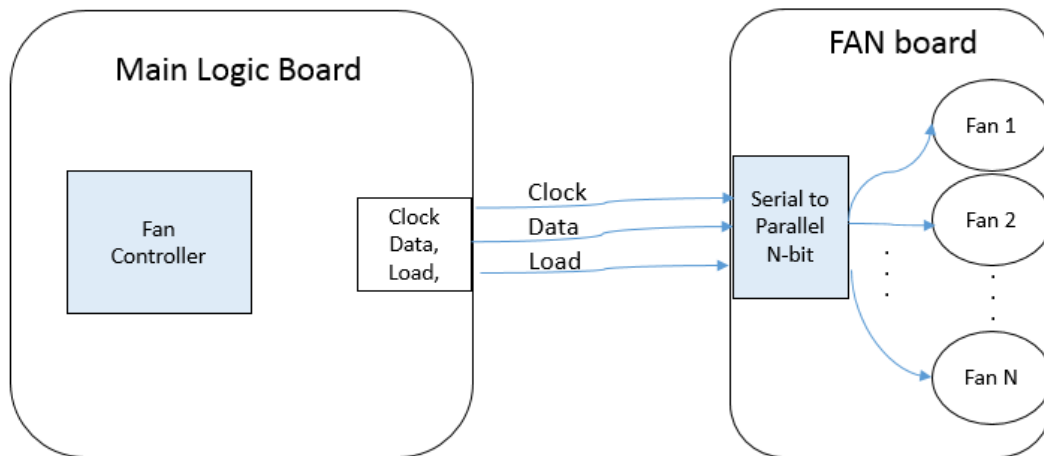


FIG. 2 Fan Control with Reduced Control Signals

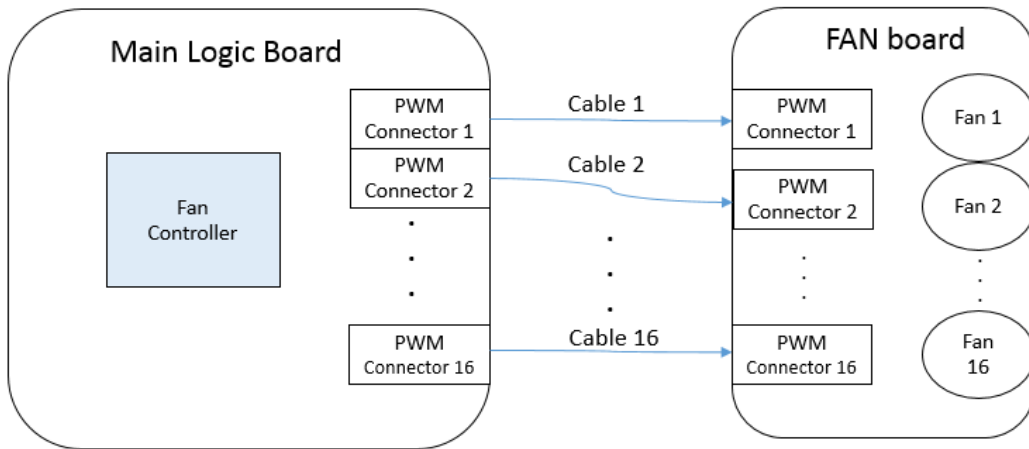


FIG. 3 Current Fan Control Design for a System with 16 System Fans

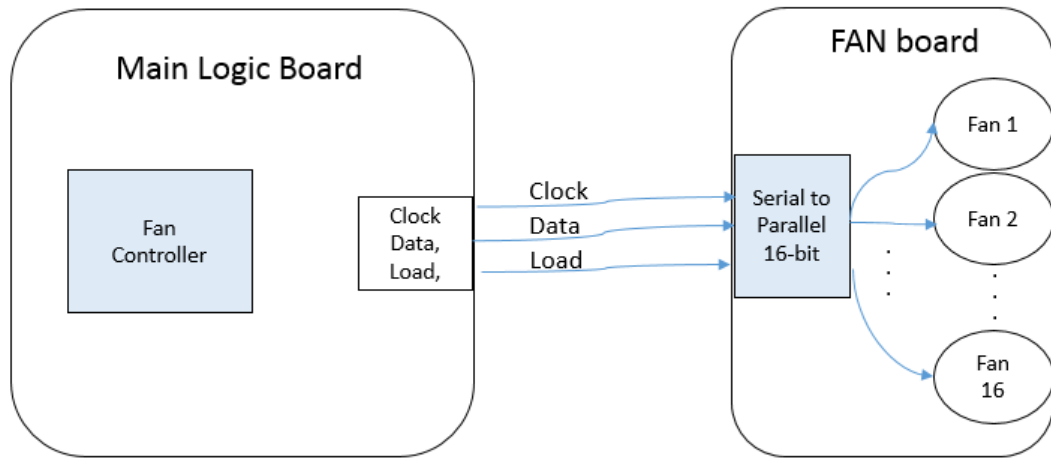


FIG. 4 FCRCS Design for a System with 16 System Fans

MC74HC595A

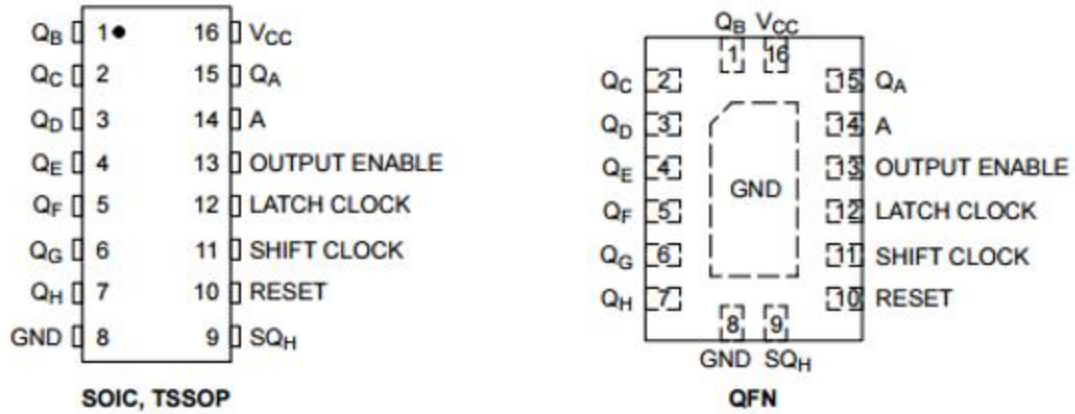


Figure 1. Pin Assignments

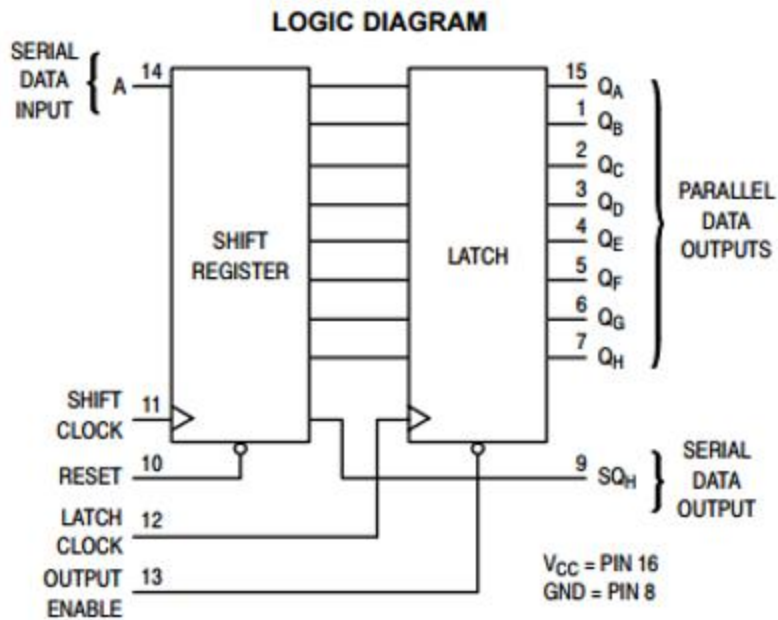


FIG. 5 Existing Shift Register Available on Market

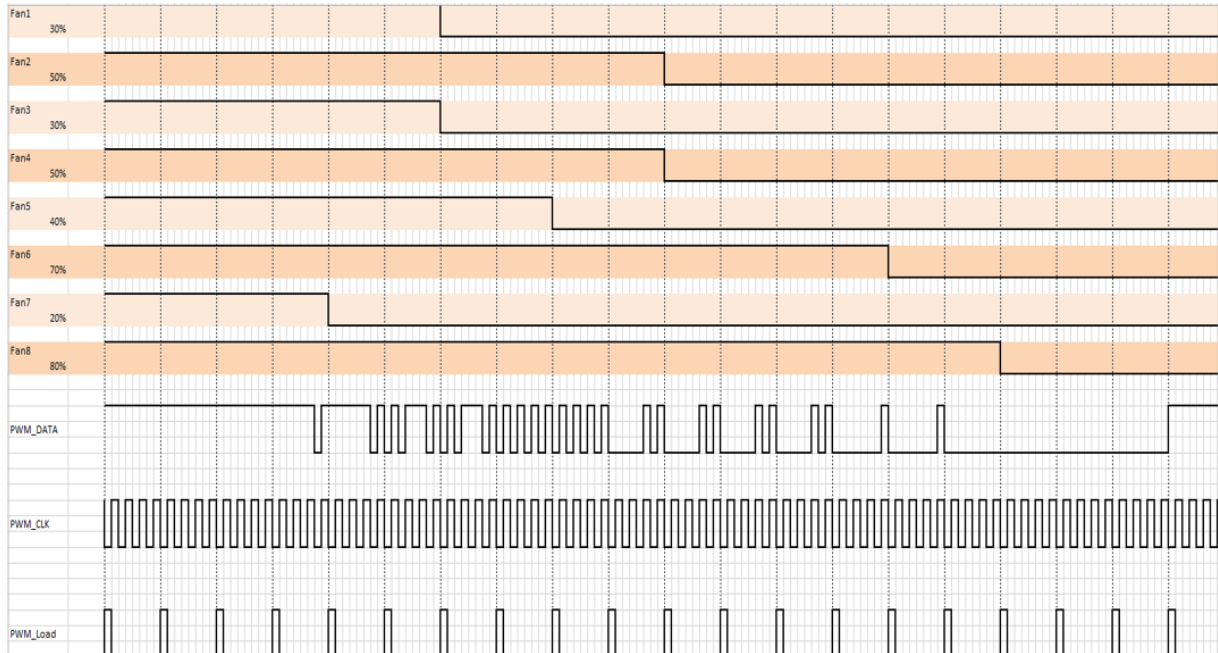


Figure 6

Reducing the number of control signals can yield these advantages over current designs:

- (a) On server system PCBs with integrated fan control design, FCRCs reduces the number of total control signals from N (based on number of total system fans) to 3. This can help reduce the size of the PCB due to “noisy” control signals requiring a “keep out” area when being routed close to areas with other noise sensitive signals.
- (b) Reducing the number of control signals reduces the noise generated where the control signals are routed, leading to better signal integrity in those areas (less noise effect on neighboring signals)
- (c) On server systems using a separate fan board, the FCRCs reduces the total number of cables being used to connect the system board to the fan board, which reduces the complexity of system cable routing.
- (d) Saves cable material cost by reducing the number of fan control cables (in a design using a separate fan).
- (e) Saves design cost by reducing the physical PCB dimensions (in a design using integrated fan control)
- (f) Saves cost in selecting a different controller when more system fans are required. Shift registers are cheaper than selecting an active controller chip with more PWM output ports.

- (g) Total number of fans that can be supported become limitless, as the shift registers can be cascaded to support any number of fans. The previous design requires a 1:1 connection and is limited by a controller's output ports.

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