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Different SRAM Cells Using Low Power Reduction Techniques

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Abstract
With increasing technology, usage of SRAM Cells has been increased to large extent while designing the system on-chips in CMOS technology. Power consumption and the speed are the major factors of concern for designing a chip along with the leakage power. The consumption of power and speed of SRAMs are some important issues among a number of factors that provides a solution which describes multiple designs that minimize the consumption of power and this article is also based on that. This article presents the simulation of 6T, 8T and 9T SRAM cells using low power reduction techniques and develops a modified model that provides the consumer with a product that costs less and having reduced power delay product. All the simulations have been carried out on 90nm at Tanner EDA tool. The entire circuit verification is done using the Tanner tool.
Keywords: CMOS Logic, SRAM and VLSI.

1. Introduction

Figure 1 shows the write mode. Word line is used for enabling the access transistors M1 and M2 for write operation [13].

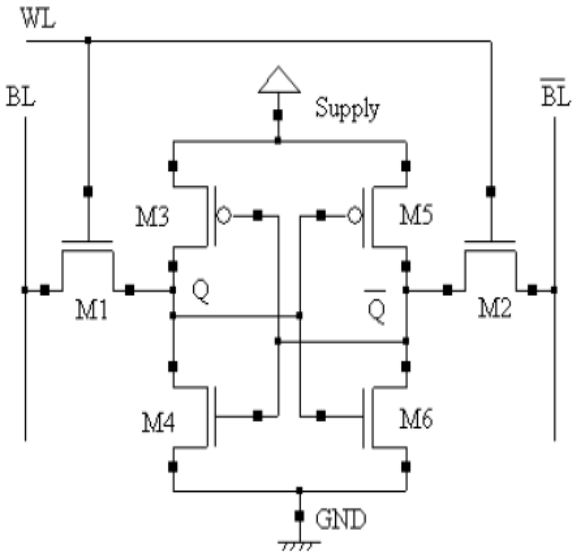

Figure.1 6T SRAM Conventional [1]

Memory Architecture is Random-access architecture which is an Asynchronous design. The SRAM IC is R/W memory circuit that permits the modification (writing) as well as their retrieval (reading). The SRAM IC was developed using the CDS IC446 [8], cadence IC design environment. The design was based on the AMI 0.6-micron process. The popular, full CMOS 6-transistor cell configuration was used to design the SRAM memory array [2]. Some of the advantages of using full CMOS SRAM configuration include high switching speeds [3].

In order to design a 64 bit SRAM, 64 full CMOS 6-T cells were used. Each full CMOS 6-T [9] cell has a capability of storing 1 bit [5]. Based on the literature survey, it has been concluded that SRAM [12] memory cell dissipate large amount of power [4] during rise time and fall time of input data because at that time the direct path exist between the V_{dd} and ground.

2. Low Power SRAM

Figure 2 shows the write mode SRAM. SRAM [13] cell introduced one Control signal transistor for controlling these transistors in this figure. But due to one more transistors area is increased in comparison to Conventional approach. This control transistor uses control select signals which can properly control the dissipation [3] [10] in power.

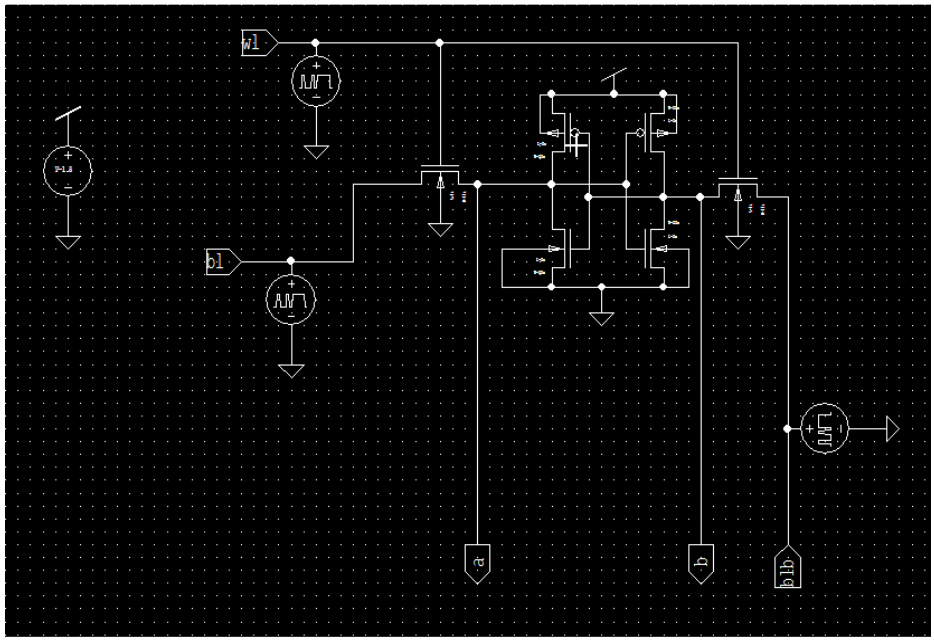

Figure.2 6-T

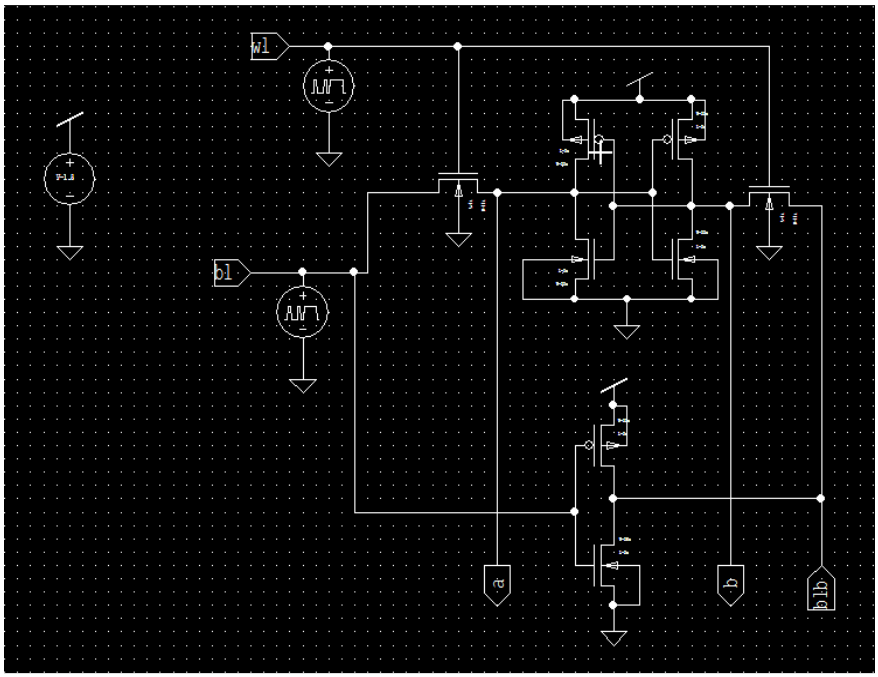

Figure.3 8-T

Figure 3 shows the dual-port cell (8T-cell) created by adding two transistors; the read [11] can be entirely decoupled from the write operation in an 8T [1] cell by sensing the data through a separate read stack controlled by a separate read word lines (RWL).

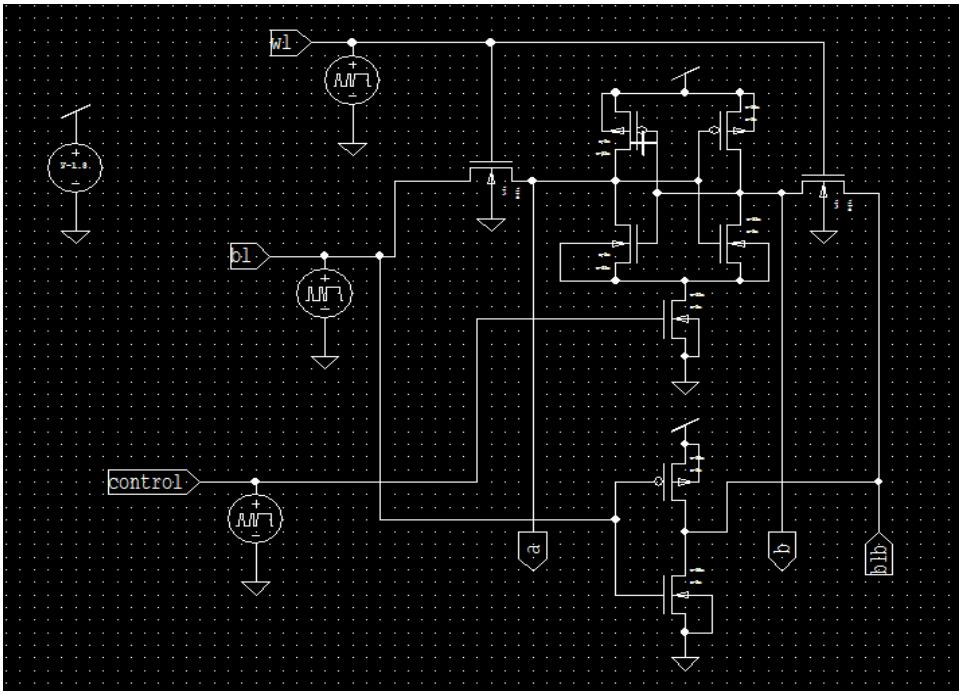

Figure.4 9-T

The schematic of the 9T SRAM cell, for CMOS technology, is shown in Figure 4. The upper sub circuit of the 9T [15] memory circuit is essentially a 6-T with minimum sized devices (composed of M3, M4, M5, M6, M1 and M2). Write signal (WL) control M5 and M6. The data is stored within this upper memory sub-circuit [7]. The lower sub circuit of the new cell is composed of the bit-line access transistors (M7 and M8) and the read access transistor (M9).

3. Simulation Analysis

All the circuits have been simulated using 90 nm technology on Tanner EDA tool. To make the impartial testing environment all the circuits has been simulated on the same input patterns.

4. Simulation Results

Figures 5 to 7 shows output waveforms of different SRAM cells at 90nm technology.

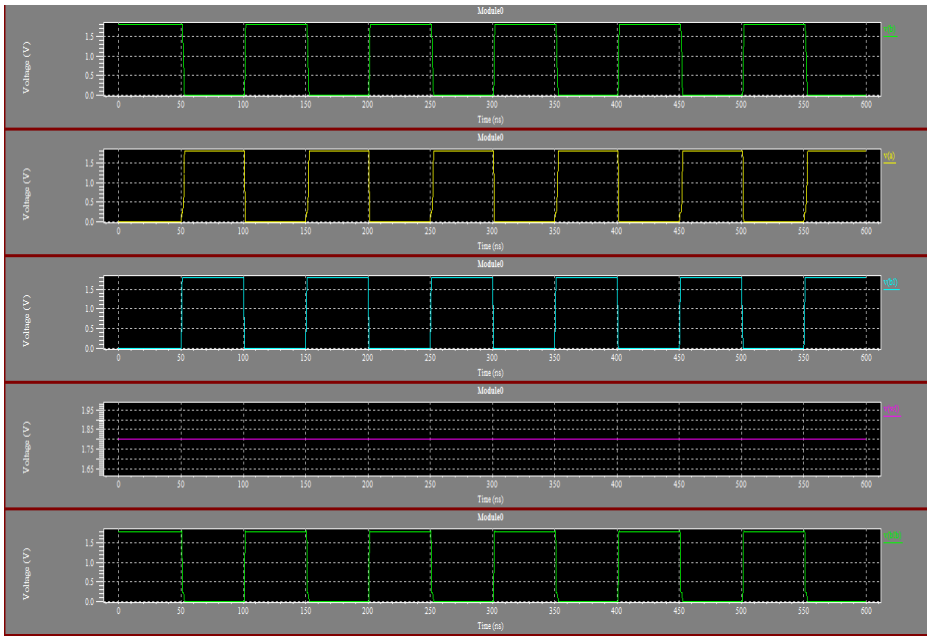

Figure.5 Output Waveform of 6T

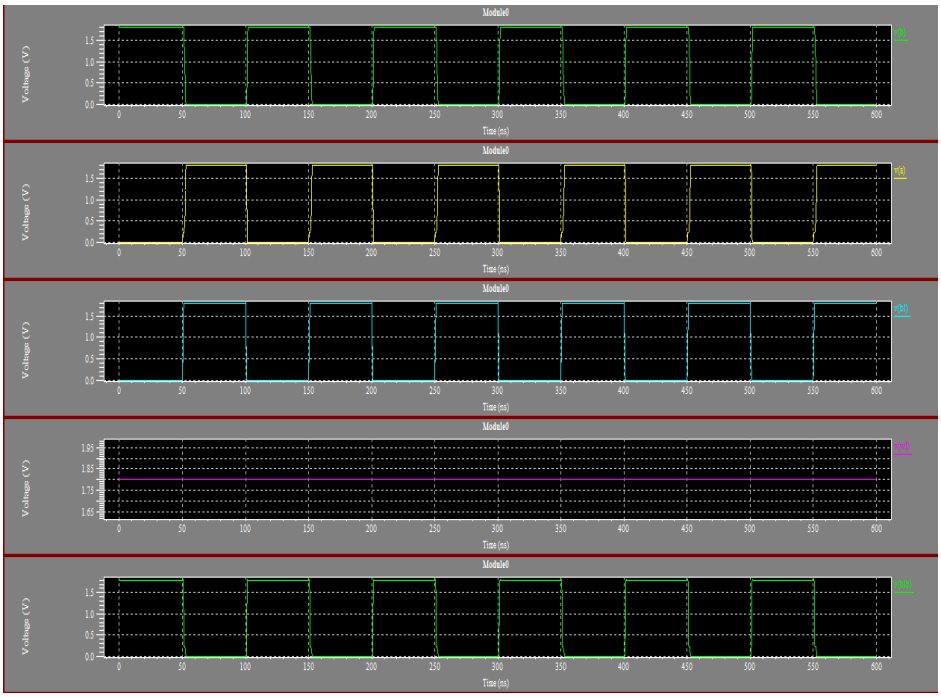

Figure.6 Output Waveform of 8T

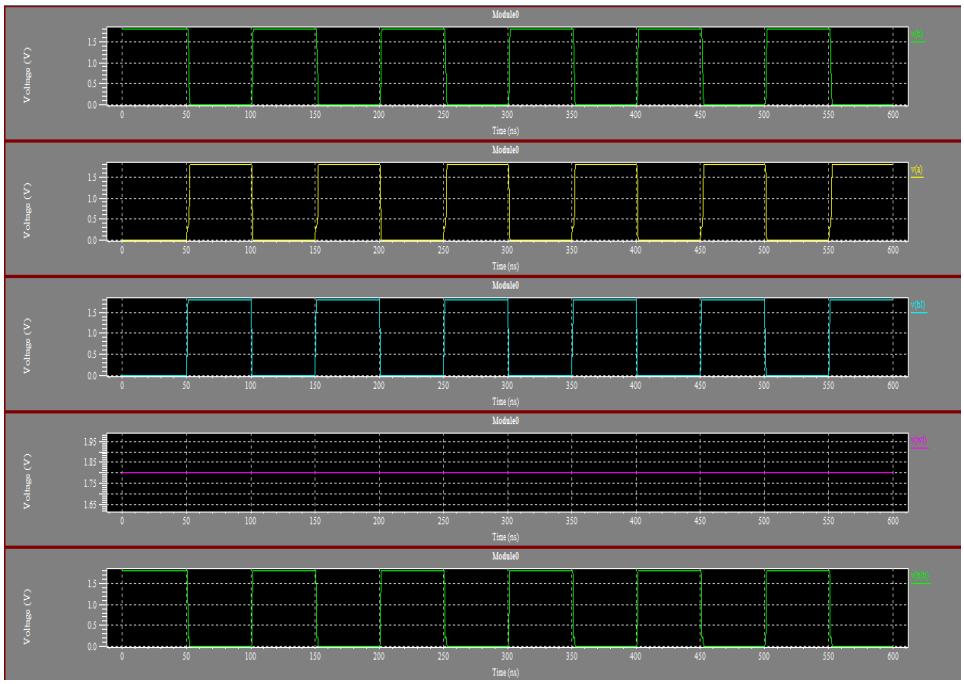

Figure.7 Output Waveform of 9T

5. Final Results

The observations of power and delay of different SRAM cells are shown in table 1.

Table I. POWER AND DELAY COMPARISON OF DIFFERENT SRAM CELLS AT 90 NM TECHNOLOGIES

Design Style	No. of transistors	Minimum Length (µm)	Avg. Power Consumption (watts)	Prop. Delay (nsec)
6T	6	.09	$2.2x10^{-4}$	$1.9x10^{-10}$
8T	8	.09	$3.2x10^{-4}$	$2.6x10^{-10}$
9T	9	.09	$1.9x10^{-3}$	$1.2x10^{-9}$

6. Conclusions

The most efficient technique to reduce the power dissipation is the reduction of the supply voltage. The power dissipation reduction in SRAMs is not only due to power supply voltage reduction, but also due to operating frequency and temperature. Technology scaling demands a decrease in both V_{dd} and V_t to sustain delay reduction, while restraining active power dissipation. To increase their reliability, the lifetime of battery is a prime concerned at the cost of speed. Reduction in the power consumption reduces the problems associated with high temperature and also provides an additional benefit in terms of the extended life of the battery.

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Biography

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