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Design of Low Offset and High Speed CMOS Comparator for Analog to Digital Converter

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Abstract

In today's world everything is digitized but nature is analog, so it is necessary to have such a device which converts analog signal into digital and for this analog to digital converter is required. Now a day's ADC's require lesser power, better slew rate, high speed and less offset. Performance limiting component for ADC's are amplifiers and comparators in which comparator is the most important.This paper presents the design of low offset low power dissipation and high speed comparator. The proposed comparator consists of a preamplifier stage, decision stage and self biased output buffer stage. The proposed design uses a low power current mirror circuitry for providing a highly biased current. The circuit is designed using 90nm CMOS process for a supply voltage of 1V and reference voltage of 0.5V and power consumption is approximately 300μW.

Keywords: CMOS Comparator, Current Mirror, Pre Amplifier, Output Buffer

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1. Introduction

The recent advancements in technology prove that we are working in the digital world, but we know that all the signals are analog in nature. So, it is necessary to have a device, which converts all the analog signals into digital. For this purpose, we use an Analog-to-Digital Converter (ADC) [Paul R Gray, Paul J Hurst, Stephen H Lewis and Robert G Meyer (1984), Hao Gao, Baltus,p ,Qiao- meng, (2010)]. The basic component in ADC device is a comparator. Figure1 shows comparator symbol. Many comparators have been proposed earlier. Among the circuits proposed, some are concerned with speed, some emphasizing on low power and high resolution, and some on offset cancellation [Jia-chen, Kurachi,S, Shimin Shen (2005)]. Bang-Sup Song proposed a comparator circuit with only preamplifier and decision stage, but did not provide any experimental results to analyze the circuit performance [Bang-Sup Song, Seung-Hoon Lee and Michael F. Tempsett (1990)]. Amalan Nag proposed a comparator with 200 MHz speed and with offset cancellation [Amalan Nag, K. L. Baishnab F. A. Talukdar, (2010)]. Allstot also thought of and simulated a novel comparator circuit which has cascading stages and ended up with a minimum power supply requirement of 3.5 V. The resolution may be higher but achieved at the expense of bulky cascading stages [David J. Allstot (1982)]. The comparator basically can be decomposed into three stages shown in Figure 2. The stages are input stage, decision stage, output stage. Designing a comparator can begin with considering input common-mode range, power dissipation, propagation delay, and comparator gain.

The rest of the paper is organized in nine different sections:

Circuit description of comparator and proposed Current mirror in section 2 and 3. Design of pre-amplifier using proposed current mirror and comparator circuit is described in section 4 and 5. Simulation results are discussed in section 6 and finally, section 7 provides conclusion.

2. Circuit Description

This design consists of three stages; the first stage is the preamplifier, followed by a positive feedback or decision stage, and an output buffer. The preamplifier stage amplifies the input signal to improve the comparator sensitivity. Output of pre-amplifier goes into decision block where comparator makes decision that which of the input signals is large. The decision stage is non-linear cross-coupled circuit which switches from one state to another. The output stage buffer the decision stage and convert the signal level to digital signal level [Wen-Rong Yang, Jia-dong Wang (2007)].

2.1. Pre-Amplifier

A preamplifier is an amplifier that prepares a small electrical signal for further amplification or processing. A preamplifier is often placed close to the sensor to reduce the effects of noise and interference. It is used to boost the signal strength to drive the cable to the main instrument without significantly degrading the signal-to-noise ratio (SNR).When the gain of the preamplifier is high, the SNR of the final signal is determined by the SNR of the input signal and the noise of the pre-amplifier. The main criteria for designing a pre-amplifier are its gain

and bandwidth. Figure 3 shows a preamplifier circuit which is first stage of comparator circuit. We also called this circuit a differential amplifier with pull up which can be a resistor load or active load. Generally we prefer active load because it is very difficult to fabricate resistor with controlled values in CMOS technology. So it is desirable to fabricate resistor with MOS. If gate and drain terminal of NMOS are shorted then it works as a resistive load.

2.2 Decision Making Block

The decision circuit is called as a heart of comparator and should be capable of discriminating mill volt signals. It is also called as a latch. Simplest form of latch is shown in Figure 4(a) which consists of two cross coupled NMOS transistor. Current sources are use in order to identify the dc current in transistors. The circuit uses positive feedback from the cross-gate connection of M1 and M2 to increase the gain of the decision element.

The decision circuit is a bi stable cross coupled circuit. It is in one state or another. The state is determined by the magnitude of the input currents.

If $i_{o-} >> i_{o+}$ M2 and M4 are on and M1 and M3 are off. Figure 4(b) shows the following conditions to hold:

$i_{o-}= i_2+i_4 = i_2$; since $i_4 = 0$, M4 is cut off

$i_{o+}= i_1+i_3= i_1$; since $i_3= 0$, M3 is cut off

$i_{o+}+i_{o-}=I_B$; I_B= constant bias current

Under these conditions, $V_{o+} = V_{DS1} \approx 0$ (M1 is on) and V_{o-} is determined by the value of V_{GS4} when $i_4=i_{o-}$

That is,

$$i_{o-} = i_4 = \frac{\beta_4}{2}(V_{GS4} - V_t)^2 = \frac{\beta_A}{2}(V_{o\_} - V_t)^2 \qquad (1)$$

where, $\beta_A= \beta_4= \beta_3$= Trans-conductance, V_{GS} is gate to source voltage and V_t is threshold voltage of MOS transistors.

To change state, increase i_{o+} hence decrease i_{o-} ($=I_B - i_{o+}$) shown in Figure 4(c). The decrease in i_{o-} will cause V_{o-} to decrease by eq (1). The $V_{o-} = V_{GS2}$, hence the decrease V_{o-} will eventually shut off M2. The value of V_{o-} just before the M2 shut off is given by:

$$i_{o+} = i_1 = \frac{\beta_1}{2}(V_{GS4} - V_t)^2 = \frac{\beta_B}{2}(V_{o\_} - V_t)^2 \qquad (2)$$

Where, $\beta_A= \beta_1= \beta_2$

On dividing eq(1) and eq(2), obtains

$$i_{o+} = \frac{\beta_B}{\beta_A} i_{o-} \qquad (3)$$

2.3 Output Buffer

The final component in conventional comparator design is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or 1). The output buffer should accept a differential input signal and not have slew-rate limitations. For simplicity here we use a self-biasing differential amplifier which works as a output buffer in comparator. This circuit is derived from two well-known conventional CMOS amplifiers. The current mirror loads from both amplifiers are deleted and connecting the corresponding gates and drains. This circuit has a PMOS and NMOS current source which must be biased to achieve identical current. Any differences would results in amplifier output shifts. To solve this, the two bias-voltage inputs are disconnected from their voltage sources and instead connected together to an internal amplifier node V_{BIAS}. Figure 5 shows the complementary self-biased CMOS differential amplifier which differs from CMOS differential amplifier in two ways first one is that the amplifiers are complementary, i.e. each n type device operates in push pull fashion with corresponding p- type devices and second one is that the amplifiers are self biased using negative feedback. Self biasing of amplifier creates a negative feedback loop that stabilizes the bias voltage. Any variation in processing parameter or operating condition that shifts the bias voltage away from nominal value result in shifting of V_{bias}, that corrects the bias voltages through negative feedback [R. Jacob Baker,

Harry W. Li, David E. Boyce (2002), P Philip E. Allen (2002) and Douglas R. Holberg 2010].

3. Current Mirror

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The current mirror is used to provide bias currents and active loads to circuit. Motivation behind a current mirror circuit is to generate a current from current source and reflect this current to the multiple locations. Earlier basic current mirror circuit and cascode current mirror circuit was used but this current mirror circuit have certain disadvantages therefore a new current mirror circuit was proposed. This new current mirror circuit then used in pre-amplifier circuit to generate more accurate biased current [Sedra & Smith (2005) H.P. Le, A. Zayegh, and J. Singh (2003)].

3.1 Proposed Current Mirror

In order to provide suitable biasing amplifiers of gain A_1 and A_2 are inserted in the proposed design which provides suitable biasing voltage to turn on transistor M3 and M4 respectively and provides high gain when working in saturation. Once transistor M4 is turned on, same output resistance as in cascode current mirror is observed. Figure 6 shows the proposed current mirror. To obtain low input impedance, we incorporate transistor M3 in series with the input terminal of the basic circuit of the current mirror and use an amplifier of gain '$-A_1$' to control the gate voltage of transistor M3, amplifier of gain A_2. Any increment in source voltage of transistor M3 (because of injected input current) causes its gate voltage to decrease '$-A_1$' times this works as stronger sink of input current which results in input impedance decrement by 'A_1'. The amplifier can be implemented by only two transistors which act as a simple inverter for which input voltage is obtained as:

$$V_{in} = V_{sg3} + V_{ds5} \tag{4}$$

For the amplifier to have the significant gain required for perfect operation of the circuit, transistors M5 and M6 should operate in saturation region. If either of M5 or M6 leaves saturation condition, amplifier gain reduces leading to increase in input impedance [Nidhi Tarun, Shruti Suman, P.K Ghosh (2014)].

3.2 Input Resistance Analysis

Figure 7 shows the small signal equivalent circuit for the proposed circuit in which the direction of p-type current mirrors are drawn opposite to the direction of n-type. From Figure 7 we get,

$$V_{gs5} = V_{sg6} = V_{in} \tag{6}$$

$$V_{s4} = V_{s5} = 0 \tag{7}$$

$$V_{gs3} = -(g_{m5}V_{gs5} + g_{m6}V_{gs6})(r_{ds5} \| r_{ds6}) \tag{8}$$

$$V_{gs3} = (g_{m5} + g_{m6})(r_{ds5} \| r_{ds6})V_{in} \tag{9}$$

With reference to the basic proposed circuit of Figure 6, the voltage gain A_1 is defined as

$$A1 = -\frac{V_{gs3}}{V_{in}} \tag{10}$$

Using equation (6) to (9), this simplifies to

$$A_1 = (g_{m5} + g_{m6})(r_{ds5} \| r_{ds1}) = (g_{m5} + g_{m6}) / (g_{ds5} + g_{ds6}) \tag{11}$$

$$V_{in} = I_{in}\left[\frac{1}{g_{m1}} \| r_{ds1}\right] + (g_{m3}V_{gs3} + I_{in})r_{ds3} \tag{12}$$

$$\cong I_{in}\left[\frac{1}{g_{m1}}\right] + (g_{m3}V_{gs3} + I_{in})r_{ds3} \tag{13}$$

$$V_{gs3} = V_{g3} - V_{S3} = -(A_1 + 1)V_{in} \tag{14}$$

$$V_{in} = I_{in}\left[\frac{1}{g_{m1}}\right] - g_{m3}r_{ds3}(A_1 + 1)V_{in} + I_{in}r_{ds3} \tag{15}$$

$$V_{in} g_{m3} r_{ds3} (A_1 + 1) = I_{in} \left[\frac{1}{g_{m1}} + r_{ds3} \right] \quad (16)$$

The input impedance R_{in} then obtained as

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{\left[\frac{1}{g_{m1}} + r_{ds3} \right]}{1 + g_{m3} r_{ds3} (A_1 + 1)} \cong \frac{r_{ds3}}{1 + g_{m3} r_{ds3} (A_1 + 1)} \quad (17)$$

From analysis it is clearly observed that the input resistance of proposed current mirror circuit depends on the amplification gain A_1. Higher the amplification gain, the lower will be the input resistance and in order to achieve higher gain, it is necessary that both transistor M7 and M8 (PMOS and NMOS) should work in saturation region.

3.3 Output Resistance Analysis

The small signal circuit for calculating the output resistance of proposed current mirror is given in Figure.8 Applying KCL at the output node in Figure .8 we get,

$$I_{out} = g_{m4} V_{gs4} + r_{ds4} (V_o - V_{s4}) \quad (18)$$

$$I_{out} = g_{m4} (V_{g4} - V_{s4}) + r_{ds4} V_o - r_{ds4} V_{s4} \quad (19)$$

$$A_2 = V_{g4} / V_{s4} \quad (20)$$

$$V_{gs} = A_2 V_{S4} \quad (21)$$

$$I_{out} = g_{m4} V_{gs4} (A_2 - 1) + r_{ds4} V_o - r_{ds4} V_{s4} \quad (22)$$

$$V_{s4} = I_{out} r_{ds2} \quad (23)$$

Putting all the values, the output impedance R_o is then,

$$I_{out} (1 + g_{m4} r_{ds4} (A_2 - 1) + r_{ds2} r_{ds4}) = V_o r_{ds4} \quad (24)$$

$$R_o = V_o / I_{out} = (1 + g_{m4} r_{ds2} A_2 + r_{ds2} r_{ds4}) \quad (25)$$

$$R_o = g_{m4} r_{ds2} r_{ds4} A_2 \quad (26)$$

Output resistance of proposed mirror circuit is equivalent to cascode current mirror and also it depends on amplification gain A_2. Higher the amplification gain of amplifier, more will be its output resistance.

4. Design of Proposed Pre-Amplifier using Proposed Current Mirror

For the preamplifier stage, the circuit is as shown in Figure 9. The circuit is a differential amplifier with active loads. The size of M1 and M2 are set by considering the differential amplifier's trans-conductance and the input capacitance. The trans-conductance sets the gain of the stages, while the input capacitance of the comparator is determined by the size M1 and M2. We have concentrated on speed in this design, and hence no high impedance nodes are used in the circuit, other than the input and output nodes. The input stage is a differential amplifier with diode connected active loads. The input voltages V_{+}, V_{-} are converted to output currents i_{o+}, i_{o-} used to drive the decision circuit. By symmetry the bias current I_{SS} is split evenly between the two sections. Transistor M1 converts the V_{GS1} to current. To determine the total current i_{o+} the equivalent includes the biasing current of $I_{SS}/2$.

$$i_{o+} = g_{m1} V_{gs1} + \frac{I_{SS}}{2} = g_m \left(\frac{V_+ - V_-}{2} \right) + \frac{I_{SS}}{2} = I_{SS} - i_{o-} \quad (26)$$

Where $g_{m1}=g_{m2}=g_m$

5 Proposed CMOS comparator

In the comparator circuit shown in Figure 10, proposed current mirror circuitry is used to provide bias current to pre-amplifier or input stage of comparator and decision stage of comparator. Input voltages V_{in1+} and V_{in2-} are converted into output currents i_{o+} and i_{o-}which is then drive the decision circuit. Bias current which is

generated by a proposed current mirror circuit is split in two sections and drives transistor M3 and M4. M5 and M6 works as a constant current source provides constant current to transistor M7 and M10.

6 Simulation Results

In this section the proposed comparator circuit and conventional comparator circuit is simulated for the propagation time delay, offset voltage, gain and power dissipation in TSPICE EDA tool version 13.0 on 90nm level 49 parameters.

6.1 Input Characteristic of Proposed Current Mirror

It is desirable for low voltage operation that M1 and M2 operate either in sub-threshold or in saturation region. By applying proper biasing voltage, the turn on condition of PMOS transistor will ensure NMOS transistor to work in saturation region. Also when M7 and M8 enter into saturation region, this in turn, lowers the input resistance. The minimum input voltage of proposed current mirror is obtained as 0.3V. Figure 11 shows the input characteristic of proposed current mirror.

6.2 Output Characteristic of Proposed Current Mirror

The minimum output voltage of the proposed current mirror is reduced to 0.1V as observed from Figure 12. Also high swing at output is obtained. Reduction in $Vmin_{(Out)}$ is because of cascoding of transistors.

6.3 Frequency Response of Proposed Current Mirror

The current through M4 should be small enough to keep M4 in sub-threshold region. Correspondingly W/L ratio should also be large. This will increase the device capacitance and bandwidth. Figure 13 shows a frequency response of proposed current mirror. From this Figure 13 a bandwidth of 98.45 MHz is obtained.

6.4 Transient Response of Proposed Pre-Amplifier

In transient response of proposed pre-amplifier circuit V_{in+} is the ac voltage source and V_{in-} is the dc or reference voltage source. This pre-amplifier amplifies the difference of two input voltages. The input voltages V_{+}, V_{-} are converted to output currents i_{o+} , i_{o-} are then used to drive the decision circuit. Transient response of proposed pre-amplifier for CMOS comparator shown in Figure 14

6.5 AC Response of Proposed Pre-Amplifier

For calculating AC response, the input V_{in+} is a ac voltage source and V_{in-} is taken as DC voltage source. Using AC analysis we find pre-amplifier gain and bandwidth. Coupling capacitance and stray capacitance affects the performance on ac characteristics of proposed pre-amplifier circuit. AC response of proposed pre-amplifier for CMOS comparator shown in Figure 15.

6.6 DC Response of Proposed CMOS Comparator

For calculating DC response both input V_{in+} and V_{in-} are taken as the DC voltage source. An important parameter of a comparator is offset voltage. Offset voltage of the comparator was measured by taking the values of input. $V_{in-,}$ at 1.0V and V_{in+} of the comparator swept from -1.0V to 2V. From the Figure 16 we can see the systematic offset voltage is approximately 15mV.

6.7 Transient Response of Proposed CMOS Comparator

For observing the transient response of Comparator a ac voltage source of 1.0V and 500 MHz is applied to the input V_{in+} and V_{in-} was set to 500 mv. We are driving V_{in+} input of comparator over the V_{in-}. When V_{in+} is greater than V_{in-} output is at logic 1 i.e. 1.8V and when V_{in+} is less than V_{in-} output is at logic 0 i.e. 0V. The transient response of proposed comparator is shown in Figure 17.

6.8 Transient Response of Self Biased Differential Buffer Amplifier

From transient response, gain will be nearly unity as shown in Figure18

7. Conclusion

This paper has presented a low offset and low power dissipation comparator implemented in 90nm CMOS technology. This proposed comparator is then used in analog to digital convertor. The key design objectives are power consumption, and offset voltage. The entire circuit consuming approximately 350µW of power, and provides gain of 30dB. The proposed low power, low offset comparator has great potential in analog integrated design.

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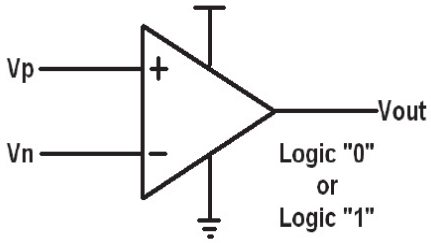

Figure 1. Basic Comparator Symbol

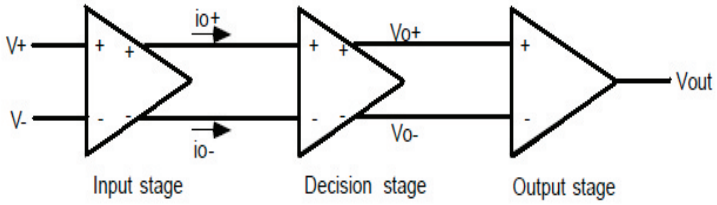

Figure 2. Block Diagram of Voltage Comparator

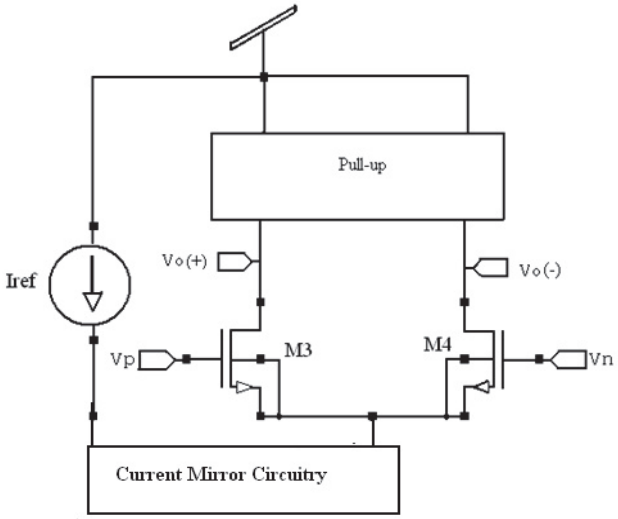

Figure 3. Pre-amplifier circuit

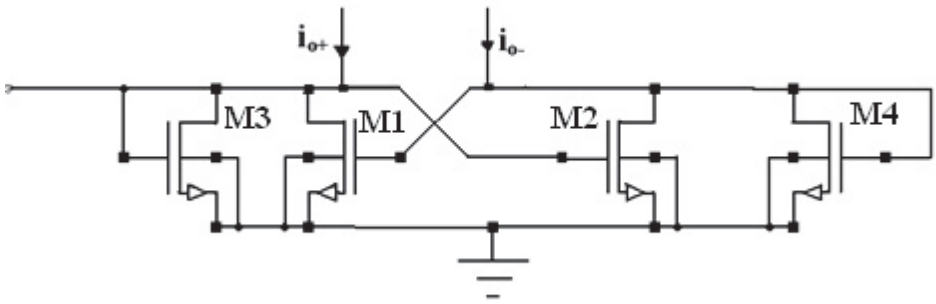

Figure 4(a). Decision Circuit

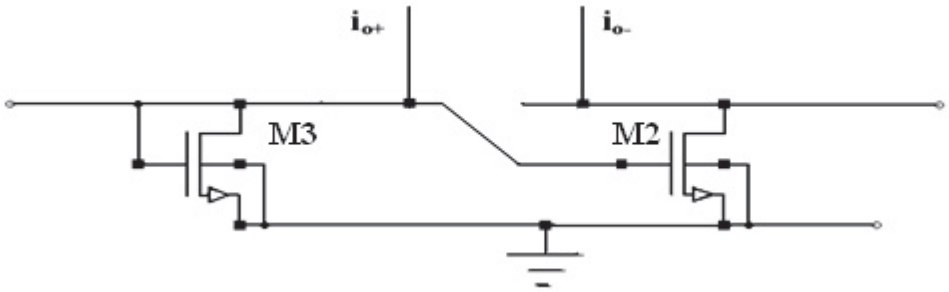

Figure 4(b). Equivalent Circuit when $v_{o+} > v_{o-}$

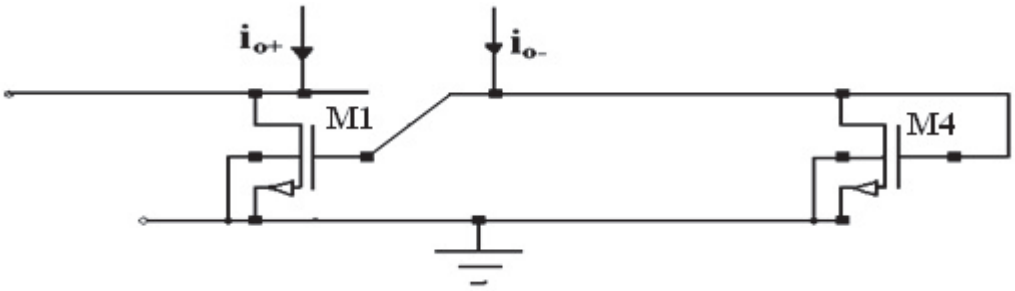

Figure. 4(c). Equivalent Circuit when $v_{o+} < v_o$

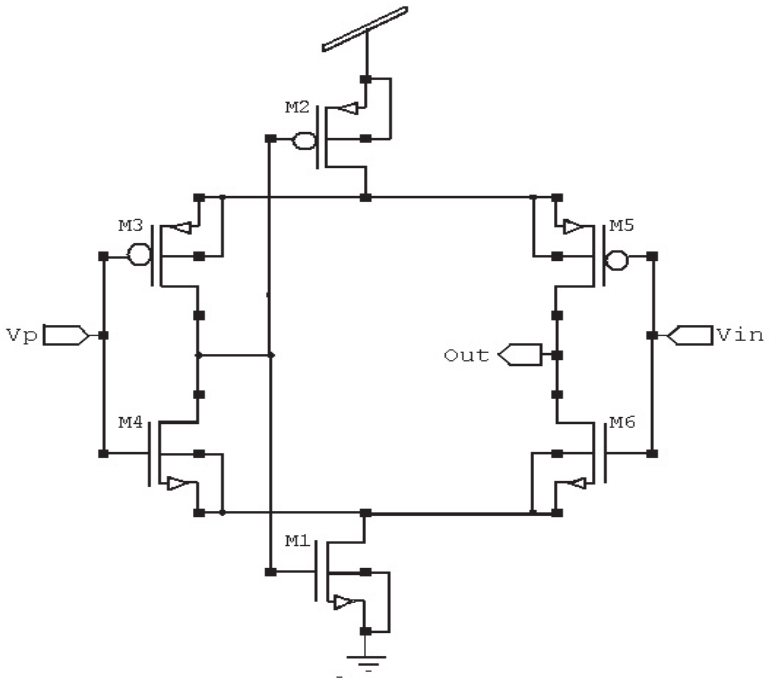

Figure 5. Self Biased Differential Amplifier Circuit

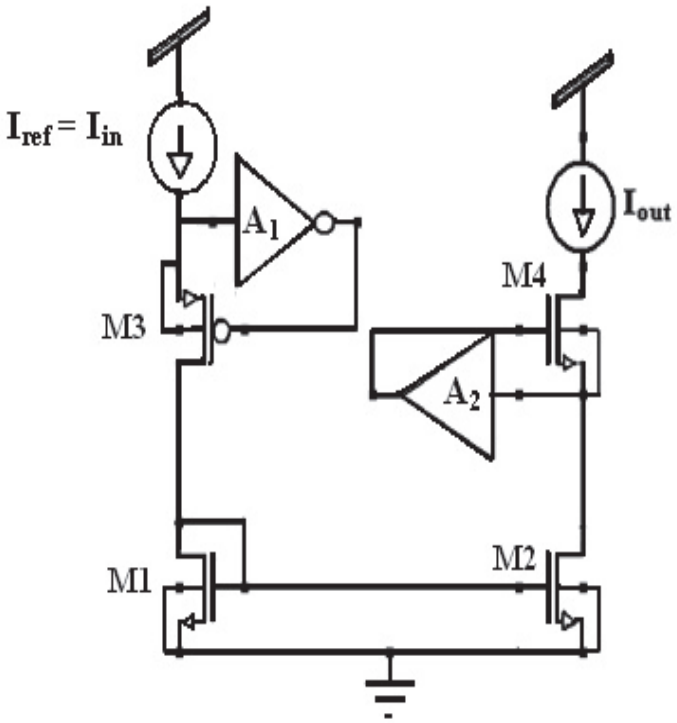

Figure 6. Proposed Current Mirror

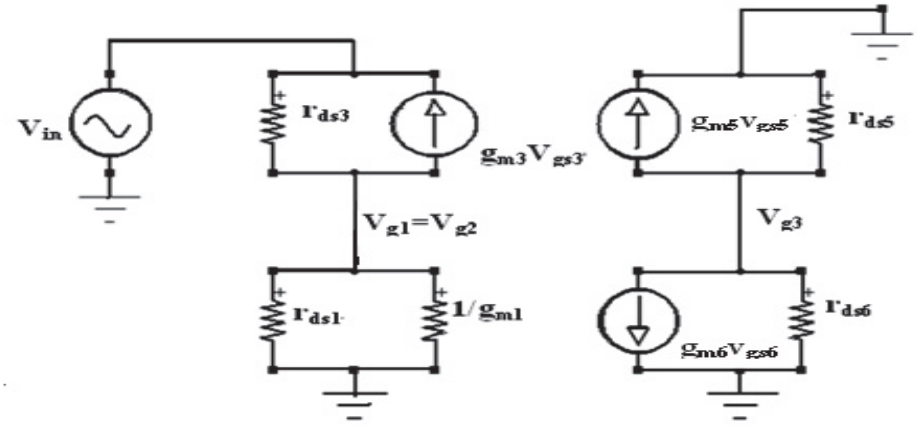

Figure 7. Small Signal Analysis for calculating Input Resistance

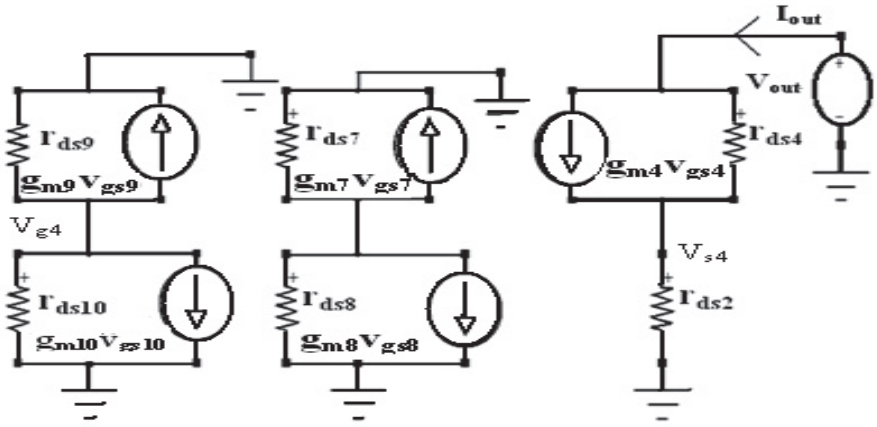

Figure 8. Small Signal Analysis for calculating Output Resistance

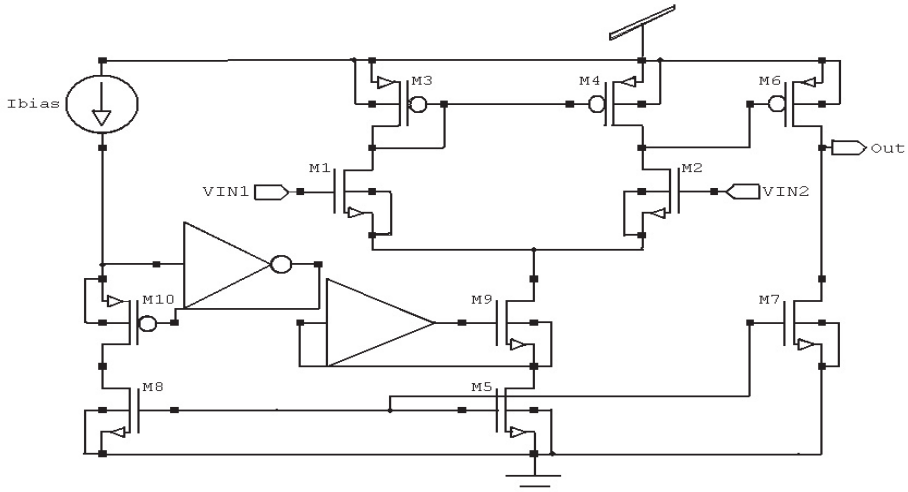

Figure 9. Proposed Design of Pre-amplifier using Current Mirror

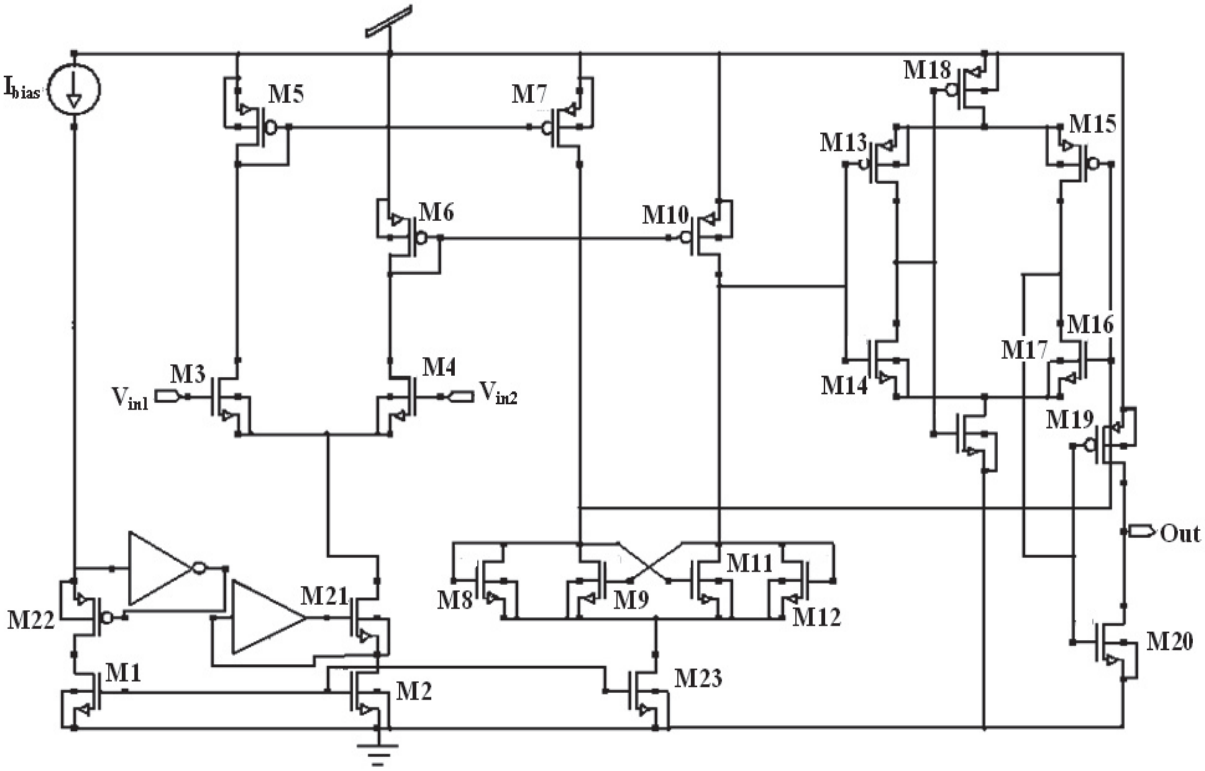

Figure10. Proposed Design of Comparator using Current Mirror

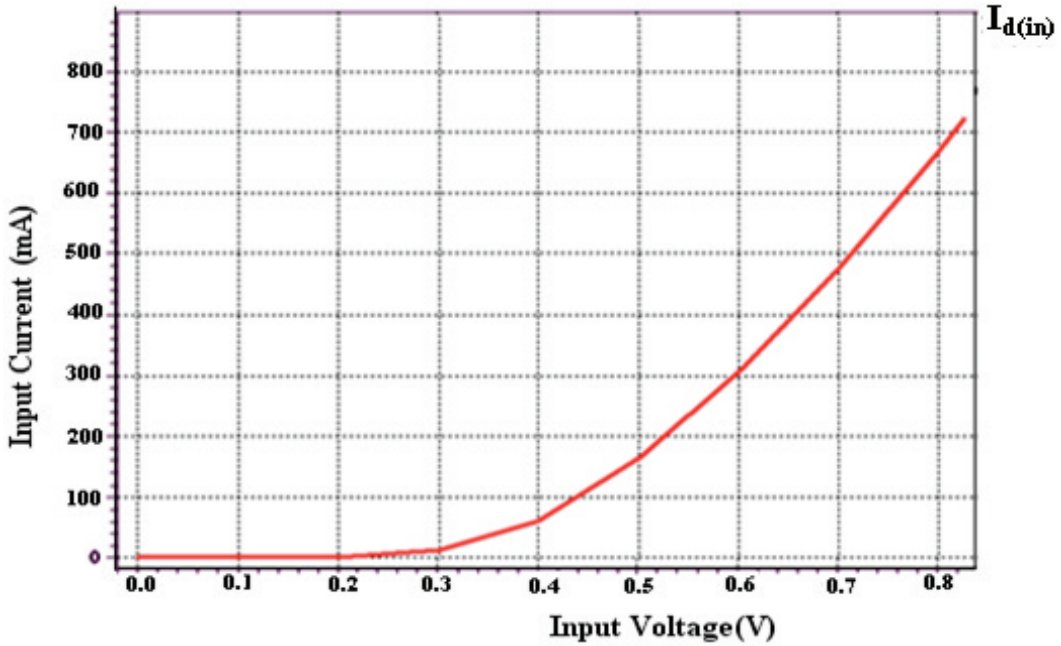

Figure 11. Input Characteristic of Proposed Current Mirror circuit

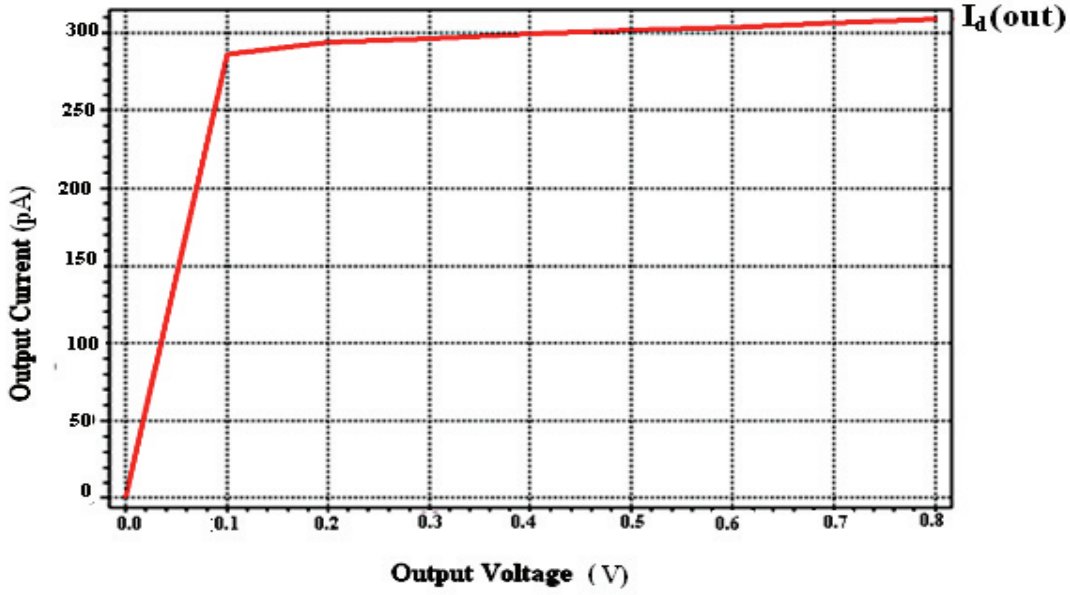

Figure 12. Output Characteristic of Proposed Current Mirror circuit

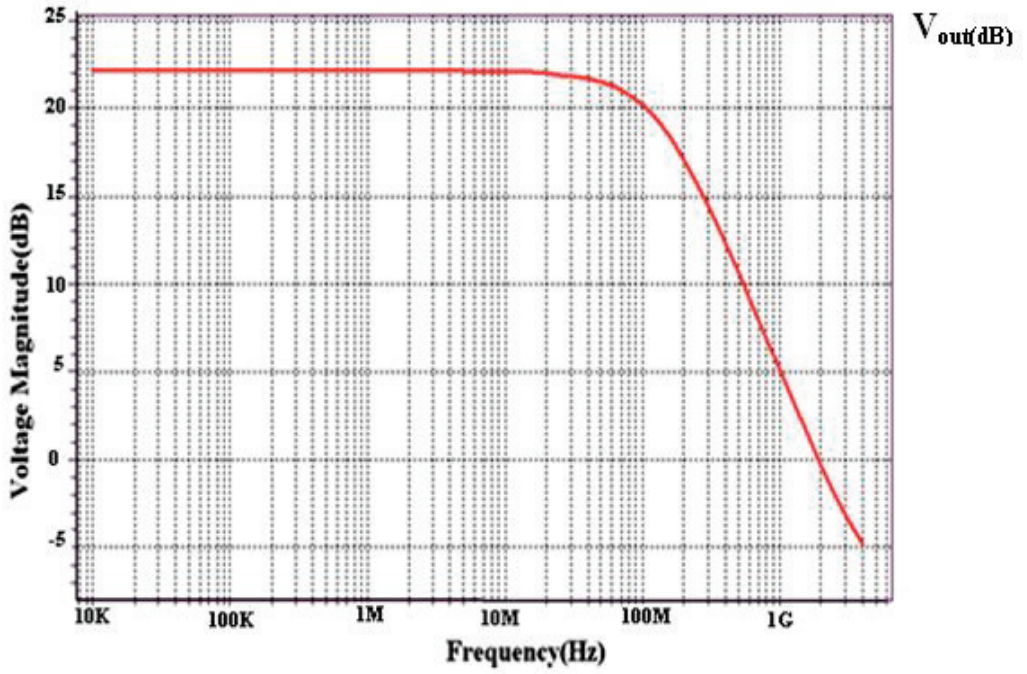

Figure 13. Frequency Response of Proposed Current Mirror circuit

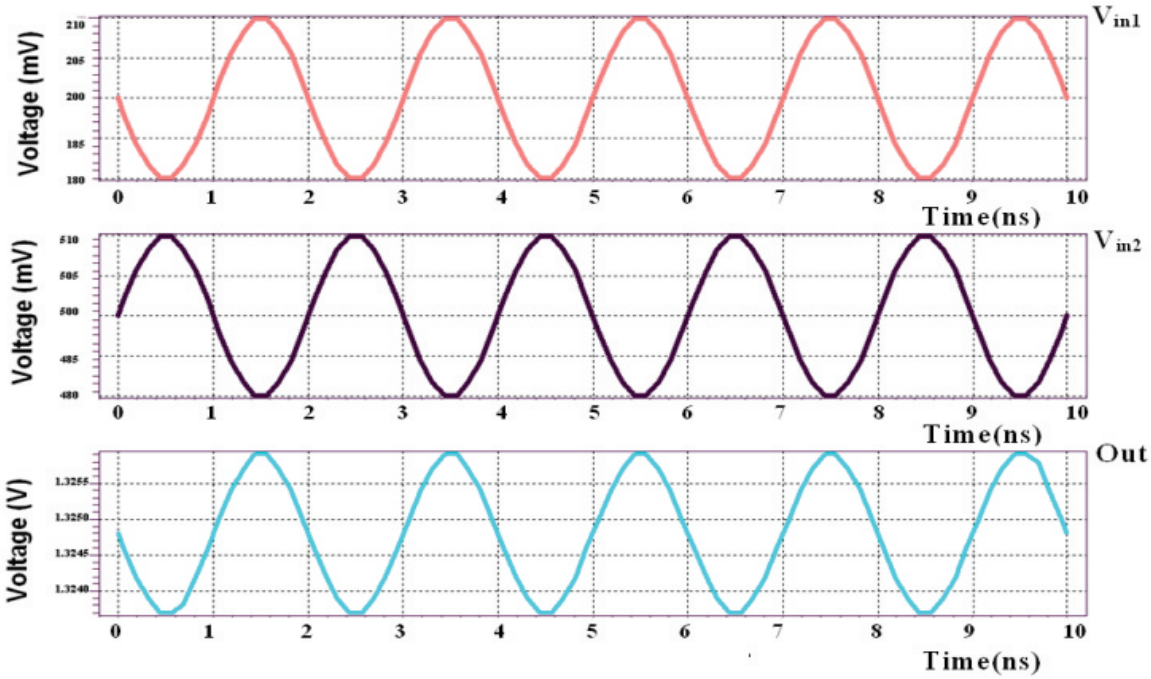

Figure 14. Transient Analysis of Pre-Amplifier

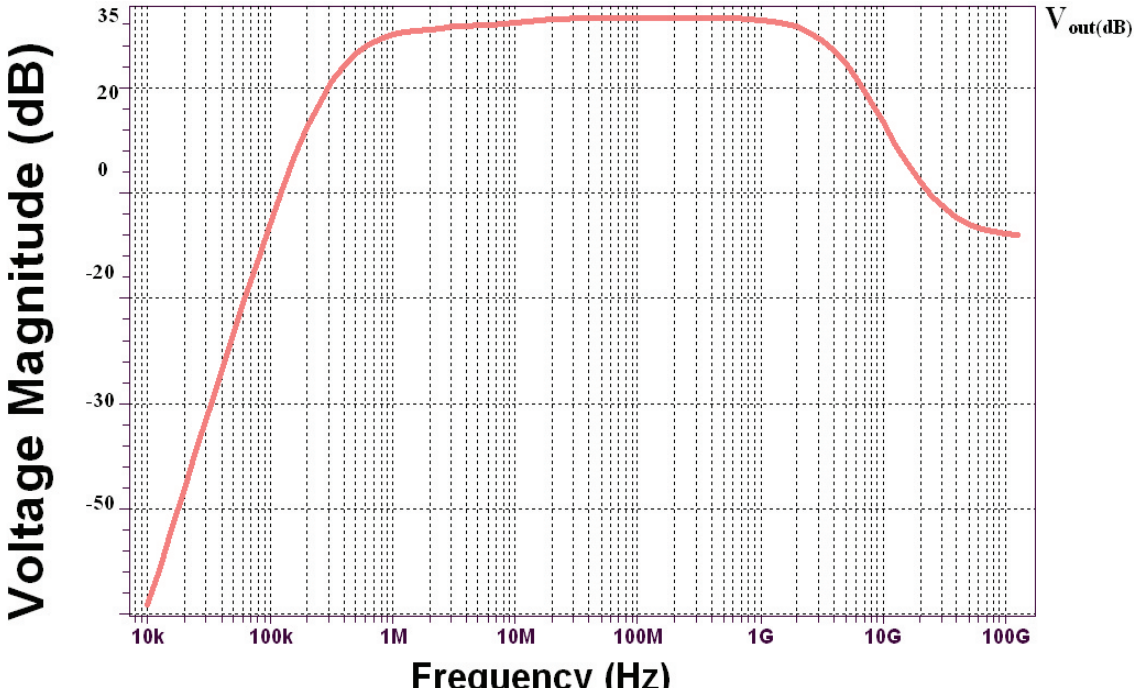

Figure 15. Transient Analysis of Proposed Comparator

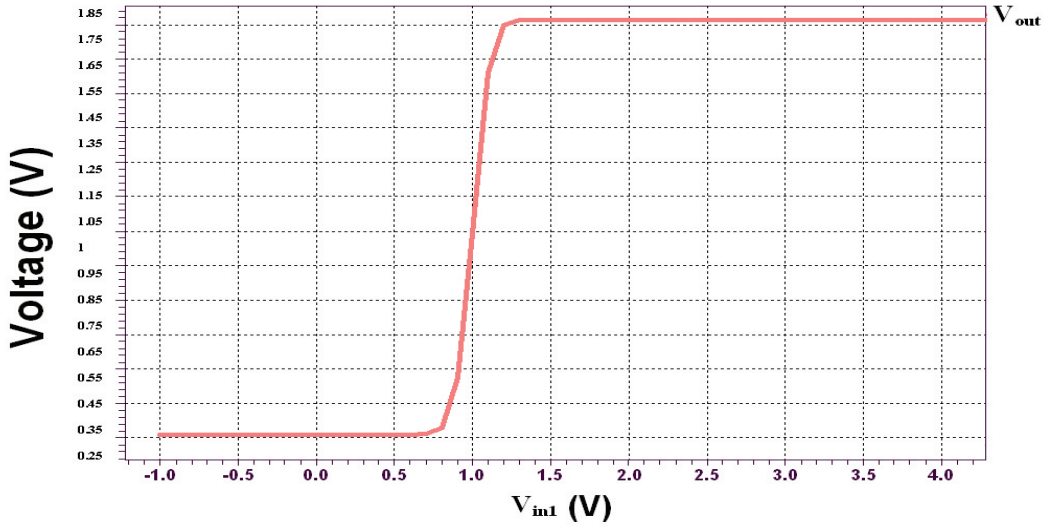

Figure 16. DC Analysis of Proposed Comparator

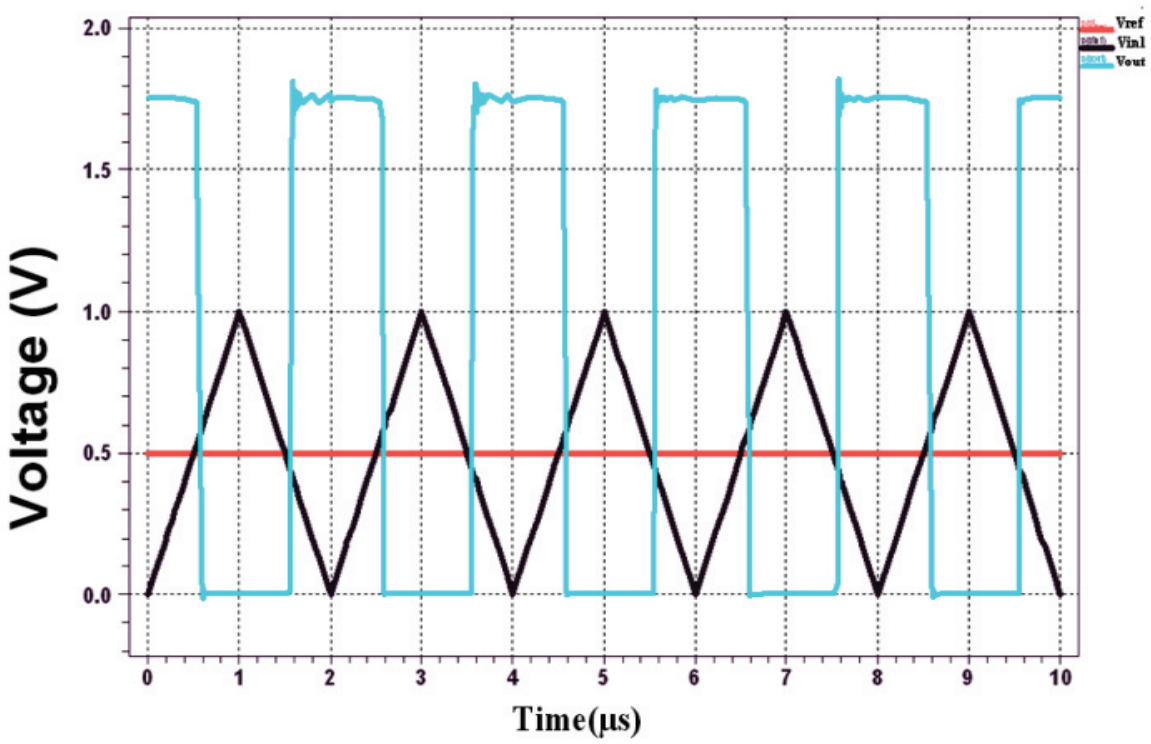

Figure 17. Transient Analysis of Proposed Comparator

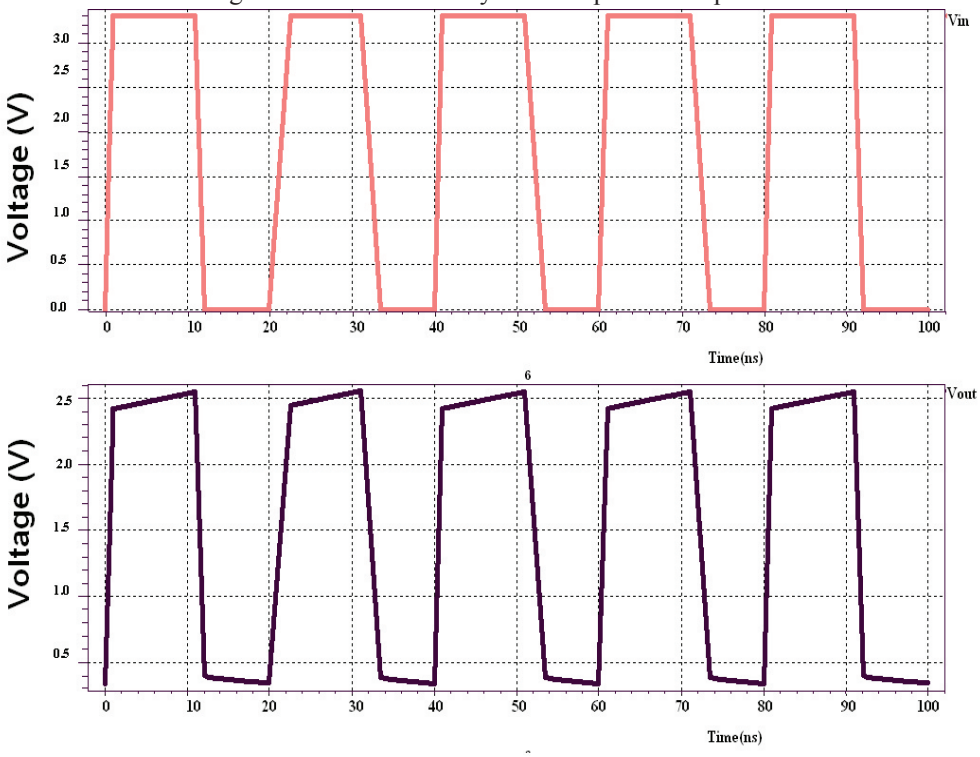

Figure 18. Transient Analysis of Output Buffer

Table I. Comparison between Conventional, Cascode and proposed Current Mirror

Properties	Conventional Current Mirror	Cascode Current Mirror	Proposed Current Mirror
Technology	90nm	90nm	90nm
Supply Voltage	1.0V	1.0V	0.8V
Minimum Input Voltage	0.4	0.6	0.3
Minimum Output Voltage	0.2	0.1	0.1
Input Resistance	0.2020KΩ	59.460KΩ	0.1790KΩ
Output Resistance	125.16 KΩ	2.756MΩ	6.247MΩ
Bandwidth	876MHz	95.8 KHz	98.45MHz
Power Consumption	52.8 µW	74.186 µW	46 µW

Table 2 Comparison between Existing Comparator and Proposed Comparator

Properties	Existing Comparator	Proposed Comparator
Transistor count	21	24
Technology used	0.18µm	90nm
Power Supply	1.8V	1.0V
Power Consumption	430µW	350µW
f_{-3dB}	600MHz	710MHz
A_{V-3dB}	9.5dB	30dB

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