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Low Power 6-Transistor Latch Design for Portable Devices

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Abstract

The latest advances in mobile battery-powered devices such as the Personal Digital Assistant (PDA) and mobile phones have set new goals in digital VLSI design. The portable devices require high speed and low power consumption. Even low power consumption is the dominant requirement and to do so speed can be compromised. In this paper a novel area efficient latch design is proposed. The simulation results show that the proposed design with less transistor count is better choice for low power and high speed portable applications.

Keywords: Latch, Low power, Portable, 8T, 6T, Power consumption, Delay.

1. Introduction

Advances in CMOS technology have led to a renewed interest in the design of basic functional units for low power, high speed, small area, longer battery life and more reliable systems. This tremendous demand is due to popularity of battery-operated portable equipments such as personal computing devices, wireless communication, medical applications and other portable devices.

The design of high-speed and low-power VLSI architectures needs efficient arithmetic processing units, which are optimized for the performance parameters, namely, speed and power consumption [1][2].

Device design in VLSI is being motivated by three basic goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed. Using less number of transistors is beneficial in reducing the number of components, interconnect parasitic capacitances, chip area, propagation delay and potentially lower power consumption.

Sub-threshold digital circuits are suitable for the specific applications, which need high performance clubbed with low power consumption. This type of application includes medical equipments such as hearing aids and pace maker, wearable wrist-watch computation and self powered devices. It can also be applied to applications in which the circuit remains idle for an extended period or to portable applications which cannot carry heavy batteries. Sub-threshold current of MOSFET transistor occurs when the gate-to-source voltage (VGS) of a transistor is lower than its threshold voltage (VTH). When VGS is lower than VTH, there are less minority carriers in the channel, but their presence comprises a current and the state is known as weak-inversion. In standard CMOS design, this current is a sub-threshold parasitic leakage, but if the supply voltage (VDD) is lowered below VTH, the circuit can be operated using the sub-threshold current with ultra-low power consumption [3][4]. In sub-threshold region, the drain current IDS is exponentially related to the gate voltage VGS as shown in equation 1.

$$I_{DS} = I_0 exp\left(\frac{V_{GS}-V_{TH}}{V_{TH}}\right)\left[1 - exp\left(\frac{V_{DS}}{V_{TH}}\right)\right] \qquad (1)$$

Where, $I_0 = \frac{W}{L}\mu C_{ox} V_{TH}^2$, and VTH is the thermal voltage. For VDS > 3VTH, IDS becomes independent of VDS for all practical purposes. In digital design, the near-ideal current source characteristic improves the noise margin of the circuits.

The total energy dissipation ET of static CMOS circuits operating in sub-VT regime is modeled as

$$E_T = E_{dyn} + E_{leak} + E_{sc} \tag{2}$$

$$E_T = \alpha C_{tot} V_{DD}^2 + I_{leak} V_{DD} T_{clk} + I_{peak} t_{sc} V_{DD} \tag{3}$$

Where, Edyn, Eleak, and Esc are the average energy dissipation due to switching activity, the energy dissipation resulting from integrating the leakage power over one clock cycle Tclk, and the energy dissipation due to short circuit currents, respectively. The energy dissipation Esc has been shown to be negligible in the sub-VT regime [5]. The dynamic and leakage power dissipation is only results from sub-threshold currents [6]. The dynamic power dissipation, since the input and the supply voltages are less than the threshold voltage of the transistor, is also very less as compared with the super-threshold operation of the device.

The critical path delay in CMOS devices is given by [7]

$$T_{clk} = k_{crit} \frac{C_{inv} V_{DD}}{I_o exp\left(\frac{V_{DD}}{nV_T}\right)} \tag{4}$$

Where, kcrit is the critical path delay, n denote the slope factor and VT the thermal voltage. Thus from equation 3 and 4, the total energy dissipation ET assuming operation at the maximum frequency is

$$E_T = C_{inv} V_{DD}^2 [\mu_e k_{cap} + k_{crit} I_{leak} e^{-\frac{V_{DD}}{nV_T}}] \tag{5}$$

It is found that the sub-VT model predicts the energy dissipation with less than 3.8% error [8].

Flip flop and Latch are the most commonly used sequential elements whose purpose is synchronizing data signals. A latch is a three-terminal element, having two inputs, data (D) and clock (clk) and one output (Q). For timing requirements, level sensitive latches are widely used in high performance ICs where timing analysis is more critical and challenging. The conventional edge-triggered flip-flop (FF) design methods using clock synchronization are very practical, since only the timing constraints defined by a given clock frequency are optimized. However, clock skew that has a strong influence on clock frequency design prevents the FF design because of the variations. Thus, level-triggered latch design method has been proposed as alternatives to FF-based design methods.

There are three main sources of power dissipation [9] in the latch:

- Internal power dissipation of the latch, including the power dissipated for switching the output loads
- Local clock power dissipation, presents the portion of power dissipated in local clock buffer driving the clock input of the latch
- Local data power dissipation, presents the portion of power dissipated in the logic stage driving the data input of the latch

Total power parameter is the sum of all three measured kinds of power.

This paper is organized as follows: Section 2 describes the existing eight transistor (8T) latch reported in the literature. Section 3 describes the design and functionality of proposed six transistor (6T) latch. Simulation results, comparisons and layouts are presented in Section 4 and finally Section 5 draws the conclusion.

2. Latch Design

2.1. Conventional 8T design

The conventional 8-transistor latch design [5] uses transmission gate logic (Figure 1). The output Q assumes the value of the input D, when the clock is active, i.e. for CLK=1. When the clock signal goes to zero, the output will simply preserve its state [10]. Thus the clock acts as an enable signal which allows data to be accepted into the D-latch.

This circuit basically contains two inverter loop and two transmission gate (TG) switches. The TG at the feedback loop is activated when CLK signal low. Thus the input is accepted (latched) into the circuit when the CLK is high, and the information is preserved as the state of the inverter loop when the CLK is low. The 8T latch is positive level triggered.

2.2. Proposed 6T design

The basic idea behind the proposed design is to replace transmission gate logic by pass transistor logic in conventional 8T design. The proposed 6-transistor design implements pass transistor logic for the transmission of data through it. The drain of first transistor PMOS_1 are connected to the data input and this data will be available at the drain terminal only when the clock will be low (Figure 2.)

Since PMOS transistors are weak zero transistors, so small threshold loss is observed when data is zero. The output of this transistor is connected to the input of the first inverter. This inverter then inverts this data and also compensates the threshold loss, but not completely and thus less than the desired output loss is observed at the output. The next inverter again inverts the data and produces the output ‘Q’. This output is feedback to the transistor NMOS_1.But overall performance of the device is almost unaffected because of the presence of the inverters.

The transistor NMOS_1 passes the output according to the delayed version of the clock. Thus whenever clock is high, data is not passing through the transistor PMOS_1 but output is again feedback through the circuit and output remains same. Thus this proposed clocked latch acts as a negative level triggered flip flop. Whenever, clock is negative, the output changes with respect to data but remains constant as clock goes positive.

2.3. Layout designs of the conventional and proposed latches

Integrated circuit (IC) layout is the representation of an IC in terms of planar geometric shapes, which correspond to the patterns of metal, oxide and semiconductor layers that make up the components of an IC. Layout is the process by which a circuit specification is converted to a physical implementation with enough information to deduce all the relevant physical parameters of the circuit. The layout step is the last major step in the design process before testing and fabrication.

The layout design for the conventional 8T latch is shown in Figure 3. In the layout design of the conventional 8T latch, number of poly contacts is two and number of poly and metal overlap is only one.

The layout design for the proposed 6T latch is indicated in Figure 4. The substrate terminals of all the circuits are connected to their respective source terminals in order to nullify the substrate-bias effect. In the layout design of the proposed 6T latch, number of poly contacts is two but there is no poly and metal overlapping, the reduction in poly contacts and poly and metal overlap leads to reduce power consumption and delay to some extent and hence significant reduction in PDP take place.

The designed layouts of conventional and proposed latches are used to extract the parasitic capacitances. The Total numbers of parasitic capacitance are six in both the designs, which are having value more than 1fF. DRC is performed to validate a high overall yield and reliability of the design. LVS check confirms that shorts, opens, component mismatches, and missing components are not found.

3. SIMULATION AND COMPARISON

All schematic simulations are performed on Tanner EDA tool version 13.0 at 65nm and 45nm technology. The aspect ratio for all the transistors is 1 for both the designs (W/L = 1). The power supply VDD and the input voltages are kept below the threshold voltage of the MOS transistors to ensure that all the transistors are indeed operating in the sub-threshold region.

After the physical layout designing post-layout simulations are carried out with extraction of parasitic capacitances. Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. The reduction in any one of power consumption and delay provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heat sinks. An additional benefit of the reduced power consumption is the extended life of the battery in battery powered systems. Table 1 shows significant reduction in total capacitance as well as output parasitic capacitances. The capacitance values are obtained after layout simulation.

From this comparison, it is clear that both output capacitance and total parasitic capacitance for proposed design is lower than conventional design which is desirable for low power consumption and less delay, as power consumption is directly proportional to capacitance, therefore proposed design is having reduction in power consumption, i.e., useful for low power applications.

The input-output waveforms are shown in (Figure 5). Whenever, clock is negative, the output changes with respect to data but remains constant as clock goes positive. The output remains unaffected and preserve its previous state even if clock is absent, thus the proposed latch is static in nature. The input and supply voltage range is taken as 0mv to 350 mV in steps of 50 mV.

The proposed latch is analyzed in terms of average power consumption (APC), delay and power delay product (PDP) at varying supply voltages, frequencies and temperatures in sub-threshold region. PDP is the function of power consumption as well as delay, so any reduction in average power consumption or delay will lead to overall reduction in PDP. To establish an impartial testing environment both circuits were simulated on same input patterns which covers each and every combination of the input stream. All these figures are plotted on logarithmic scale to show better view of comparison. All simulation work is carried out at 65nm technology as well as 45nm technology to show technology independency of the proposed circuit.

3.1. Simulation results in 65nm technology

It can be deduced from Figure 6 that with the increase in temperature power consumption also increases and power consumption for both the designs are almost comparable. Power consumption is a dependent parameter of supply voltage and as the supply voltage increases, power consumption also increases. Figure 7 presents the same but APC of the proposed latch is slightly more than the conventional latch. Average power consumption is also directly proportional to the input signal frequency. Figure 8 presents the comparison of the APCs of both designs and APC of the 6T design is comparable upto 1 MHz but remarkably less at 5 MHz. Since the circuit shows degraded performance above 5MHz and thus not simulated beyond 5 MHz.

As temperature increases, the characteristics of the semiconductor device are affected due to increase in thermal generation and recombination rate of the carriers. Thus, average power consumption and delay of the device are affected with temperature as the collision rate of the carrier increases and some of the power is consumed in the form of thermal energy. It is clear from Figure 9 that the delay introduced by the proposed design is lower than the 8T design.

Circuits operating in sub-threshold region are very sensitive to the supply voltage. The sensitivity of the circuit delay increases with decreasing power supply value. Figure 10 indicates that delay in the proposed 6T design is significantly less than the conventional 8T design at various supply voltages.

The dynamic power component of the power consumption, i.e., P = α.C.V2.f, where α is the switching activity, is dominant at higher frequencies and becomes negligible at lower frequencies as the static power component takes over, i.e., $P = V_{DD} \times I_{Sub-threshold}$. Power consumption in sub-threshold region is much lower than super-threshold region. Figure 11 shows the behavior of the proposed circuit with the variation in frequency. As in sub-threshold region, circuits work better up to medium frequencies, hence range of frequency is taken from 50 kHz to 5 MHz, and here also the 6T design shows better results than 8T.

The PDP is the amount of energy per switching activity of the signal. Thus, having a lower PDP means the sub-threshold circuit is consuming less energy, when all the contending circuits are operating with the same amount of switching activity. The product of Average power consumption and delay is calculated and mentioned in the table 2- table 4. The analysis of the presented data reveals that the 6T design is better than the 8T design.

3.2. Simulation results in 45nm technology

Similar results are obtained when simulations are carried out at 45nm technology. It shows technology independent behavior of the proposed circuit.

The average power consumption at various temperature, supply voltage and frequencies is plotted (Figure 12-14). In 45 nm technology, the average power consumption of the proposed design is found less than the earlier design at all the values of the temperatures, voltages and frequencies. The produced results indicate that the design is better suitable for low power designs.

Delay in the proposed design is always remarkably lesser than the previous 8T latch design (Figure 15-17) and thus the PDP of the 6T latch is considerably reduced as indicated in the table 5- table 7.

4. Conclusion

In this paper, the design and the simulation results of the conventional and proposed design demonstrated and found that the proposed 6-transistor latch is better in terms of power consumption and delay. Since the transistor count is less, thus the proposed design is also area efficient. Hence the 6-transistor latch is better viable option for the low power device designs.

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Figures

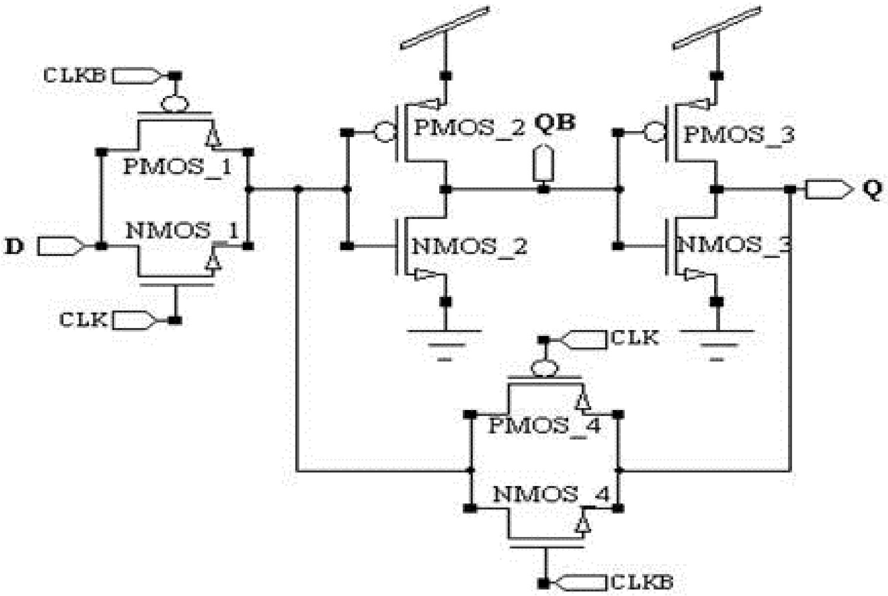

Figure 1. Conventional 8 Transistor Latch

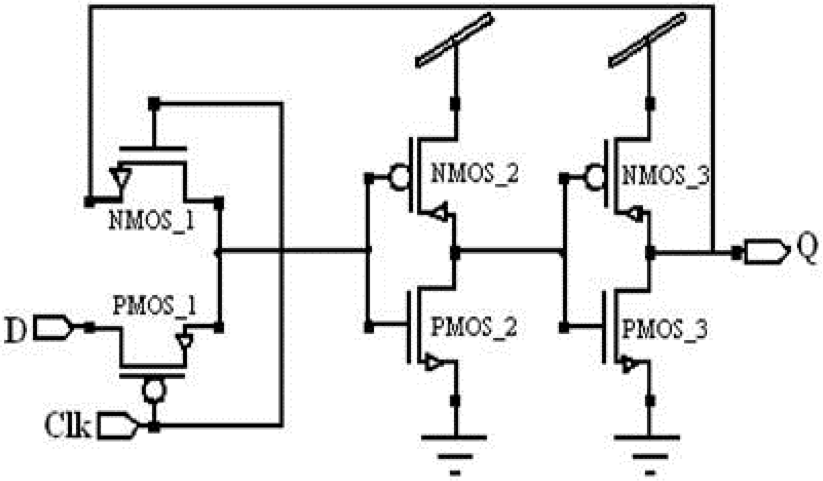

Figure 2. Proposed 6 Transistor Latch

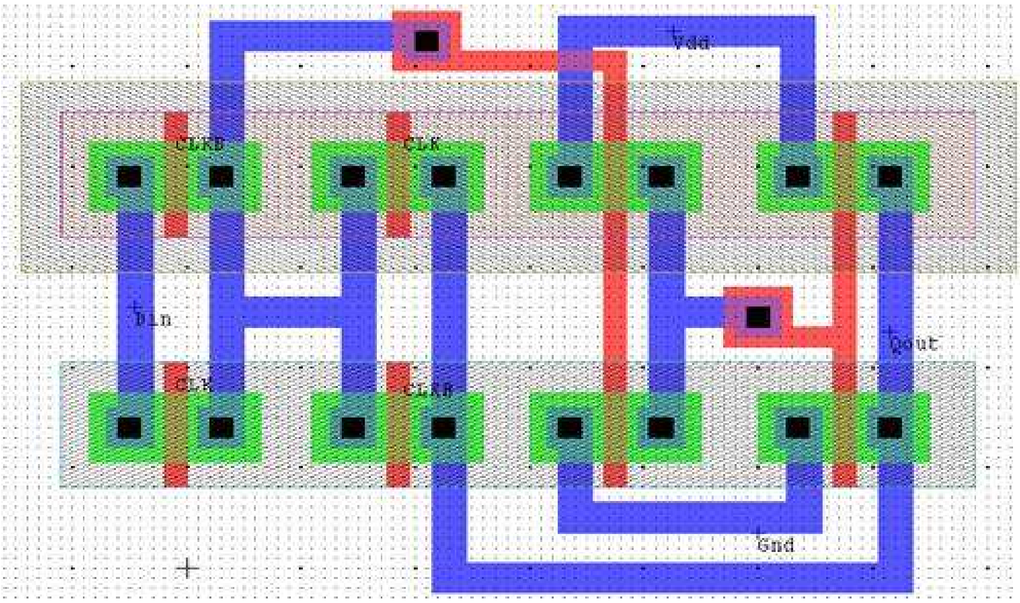

Figure 3. Layout of existing 8T latch

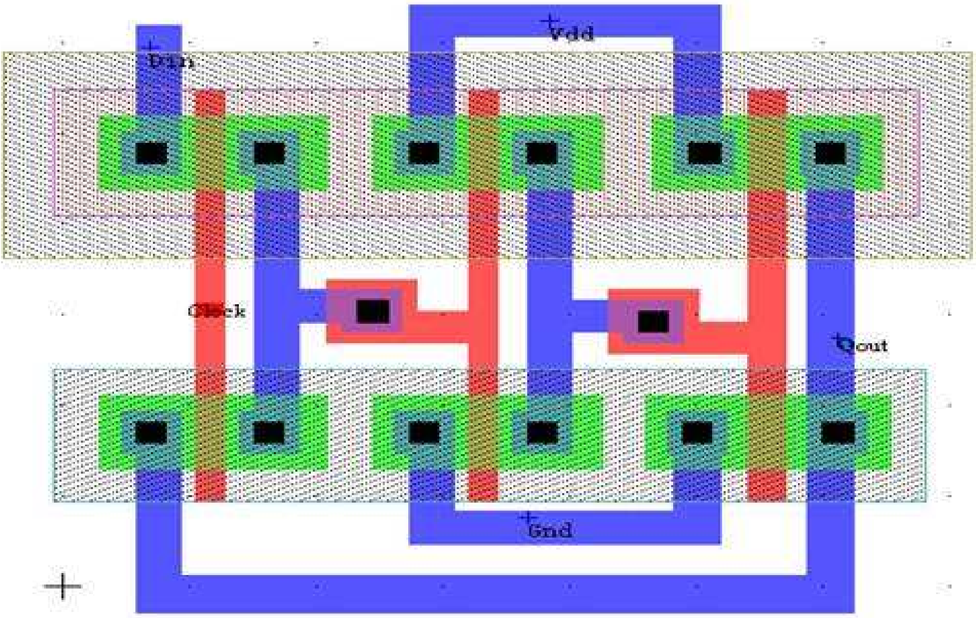

Figure 4. Layout of proposed 6T latch

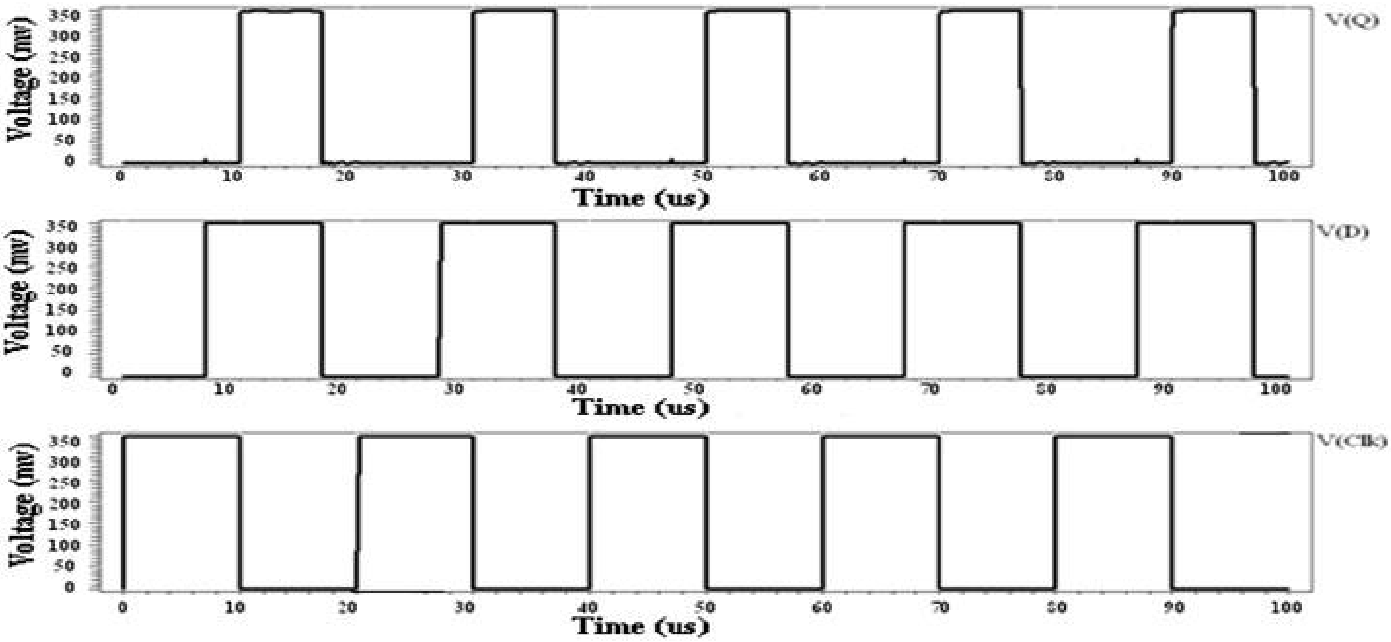

Figure 5. Input-Output waveform of the proposed 6T latch

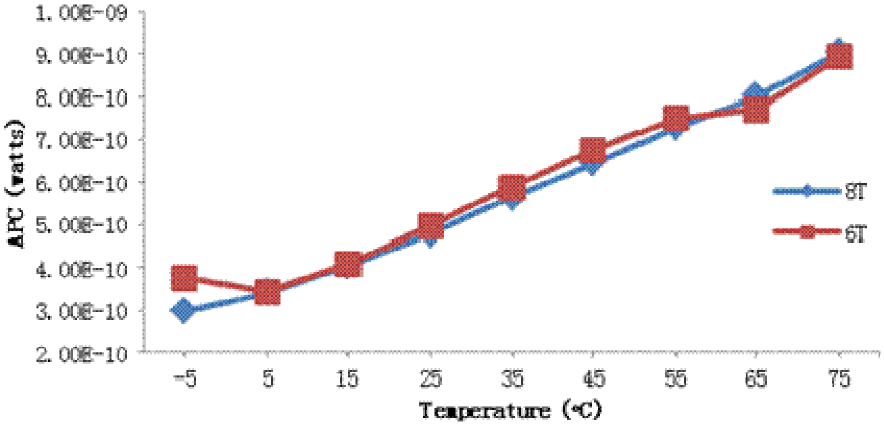

Figure 6. APC at different temperatures

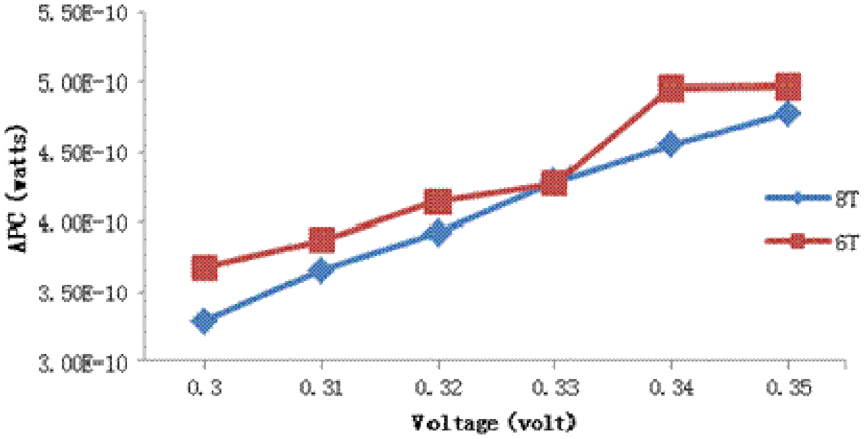

Figure 7. APC at various supply voltages

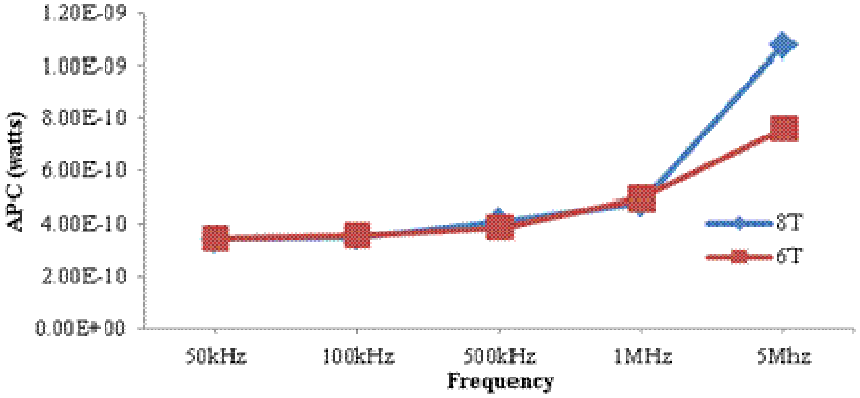

Figure 8. APC at different frequencies

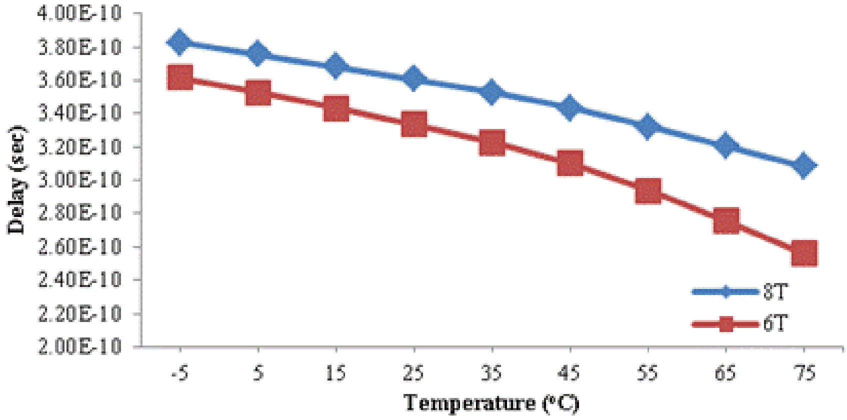

Figure 9. Delay at different temperatures

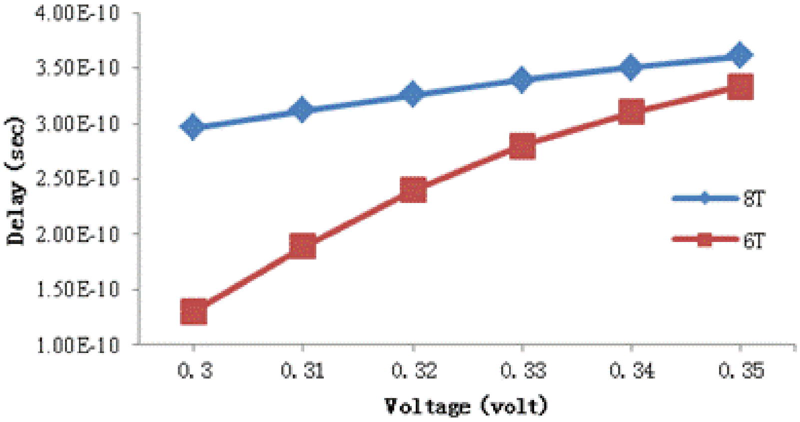

Figure 10. Delay at various supply voltages

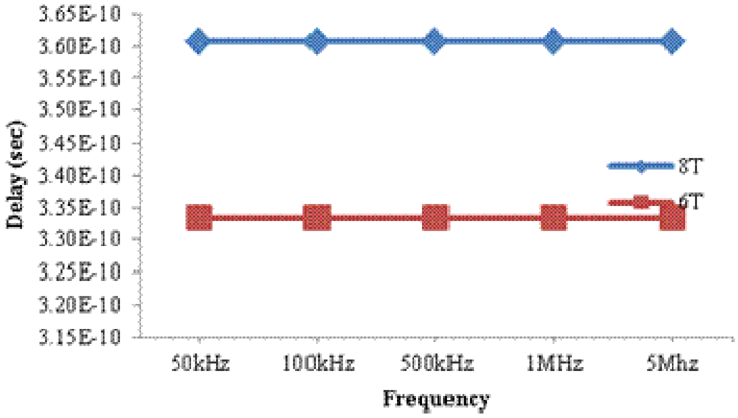

Figure 11. Delay at varying different frequencies

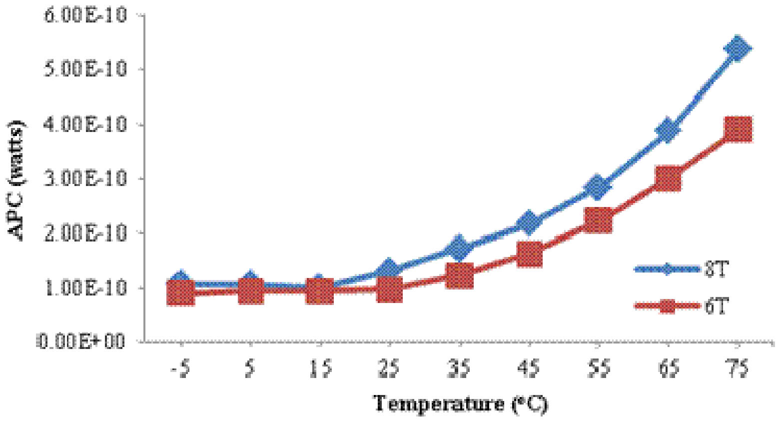

Figure 12. APC at various temperatures

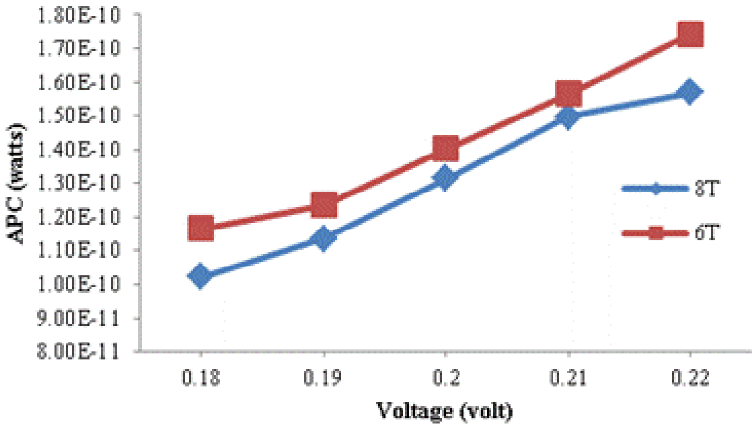

Figure 13. APC at different supply voltages

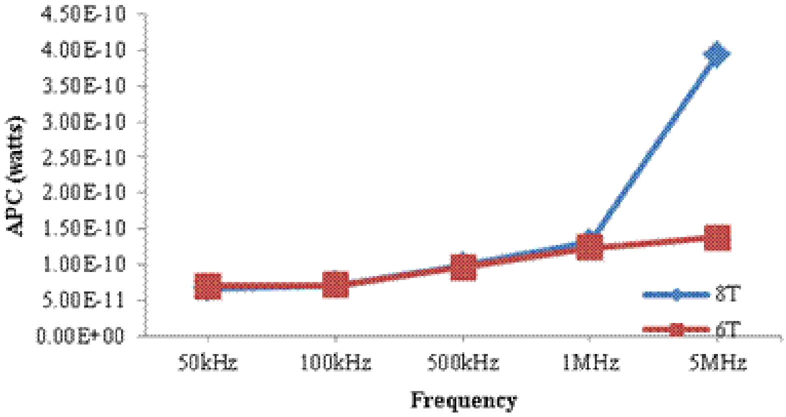

Figure 14. APC at different frequencies

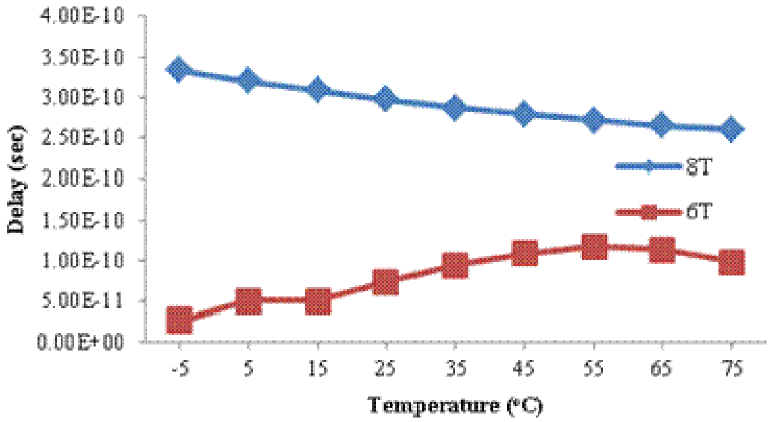

Figure 15. Delay at different temperatures

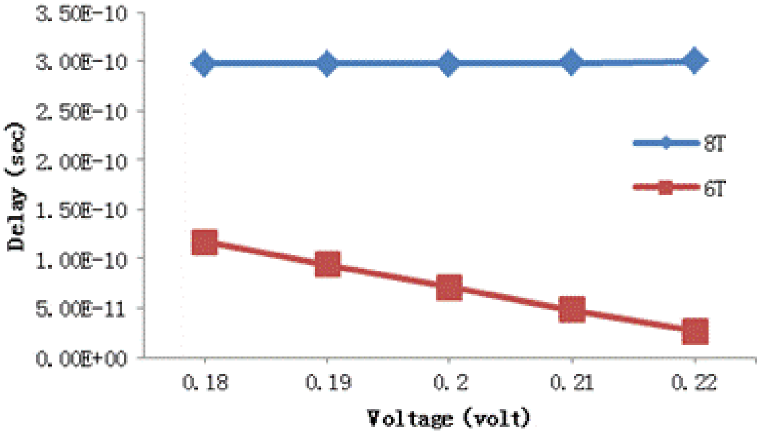

Figure 16. Delay at various supply voltages

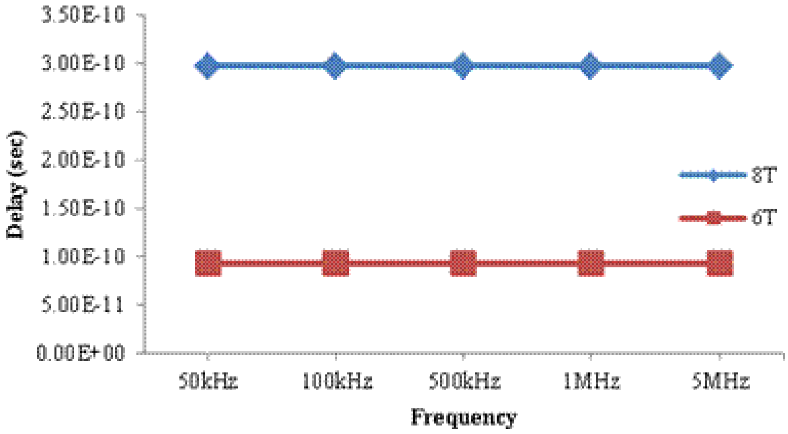

Figure 17. Delay at different frequencies

Tables

Table 1. Parasitic Capacitance of existing and proposed latch

Latch	Parasitic Capacitance (F)	
	Output capacitance	Total capacitance
8T	1.80E-016	7.06E-16
6T	1.29E-016	5.47E-16

Table 2. PDP with increasing temperatures

Temperature(oC)	8T	6T
-5	1.14E-19	1.36E-19
5	1.29E-19	1.22E-19
15	1.49E-19	1.41E-19
25	1.73E-19	1.66E-19
35	1.98E-19	1.90E-19
45	2.22E-19	2.10E-19
55	2.42E-19	2.20E-19
65	2.57E-19	2.12E-19
75	2.78E-19	2.28E-19

Table 3. PDP with varying input voltage and supply voltages

Voltage (volt)	8T	6T
0.30	9.75E-20	4.80E-20
0.31	1.14E-19	7.30E-20
0.32	1.28E-19	9.93E-20
0.33	1.45E-19	1.19E-19
0.34	1.60E-19	1.54E-19
0.35	1.73E-19	1.66E-19

Table 4. PDP with increasing operating frequencies

Frequency	8T	6T
50kHz	1.24E-19	1.16E-19
100kHz	1.27E-19	1.20E-19
500kHz	1.49E-19	1.29E-19
1MHz	1.73E-19	1.66E-19
5MHz	3.88E-19	2.53E-19

Table 5. PDP with increasing temperatures

Temperature(oC)	8T	6T
-5	3.59E-20	2.45E-21
5	3.44E-20	4.76E-21
15	3.11E-20	4.76E-21
25	3.91E-20	7.20E-21
35	4.95E-20	1.16E-20
45	6.04E-20	1.77E-20
55	7.71E-20	2.60E-20
65	1.03E-19	3.42E-20
75	1.40E-19	3.84E-20

Table 6. PDP with varying input voltage and supply voltages.

Voltage (volt)	8T	6T
0.18	3.04E-20	1.36E-20
0.19	3.38E-20	1.16E-20
0.20	3.91E-20	9.99E-21
0.21	4.47E-20	7.47E-21
0.22	4.70E-20	4.59E-21

Table 7. PDP with increasing operating frequencies

Frequency	8T	6T
50kHz	1.99E-20	6.57E-21
100kHz	2.11E-20	6.74E-21
500kHz	2.93E-20	9.08E-21
1MHz	3.91E-20	1.16E-20
5MHz	1.17E-19	1.30E-20