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MTCA.4 - modular measurement and control system with sub-nanosecond time synchronization and support for RF applications

Grzegorz Kasprowicz

***Abstract*—The Micro TCA platform [1] is rapidly developing modular technology for measurement and control systems. There are available versions for laboratories, military and aviation. The newest release of the standard (MTCA.4) supports high frequency RF applications like particle accelerators, radio, telecom and radar. The PERG group together with partners from Europe and Poland takes active part in development process, i.e. implementation of sub-ns [2] synchronization, event and RF distribution system over fibre networks. It enhances significantly capabilities of MTCA platform in distributed measurement systems (i.e. passive radars) and enables fully deterministic operation of hard real time control systems.**

***Keywords*—Micro TCA, MTCA.4, FPGA, SDR, FMC, PCIe, RF, time synchronisation, White Rabbit**

I. Introduction

THE aim of the article is brief introduction of integrated, modular measurement and control system with embedded sub-nanosecond time synchronization system and distribution of RF signal. Such systems are utilized by scientific laboratories (i.e. high energy physics), industry (Automated Test Equipment), military and space institutions (passive radars, ground stations)

A. The MTCA architecture

The MTCA platform is available on the market for over ten years. It evolved from telecommunication ATCA standard [3]. The MTCA sandard utilizes ATCA-defined AMC boards used directly in dedicated chassis. It also defines MTCA Carrier Hub (MCH) which consists of Ethernet hub and crate management system. The MTCA crates are available in several form-factors for industrial, aviation and military use. Fig.1 presents examples of available versions where common factor is AMC module. In this way user can easily extend and adopt the standard to particular application by selection of proper chassis, cooling method, computing and connectivity technology while keeping same mechanical, electrical standard and software architecture.

The newest incarnations of the standard support 40G communication speed between hub an AMCs and up to 10G between the AMC modules. Fig.2 depicts the MTCA architecture with fully redundant power, cooling, communication hub and management. Practical applications usually implement simplified architecture optimized for cost, adopted to functional or mechanical requirements, i.e.

G.Kasprowicz is with the Institute of Electronic Systems, Warsaw University of Technology, Poland (e-mail: G.Kasprowicz@elka.pw.edu.pl).

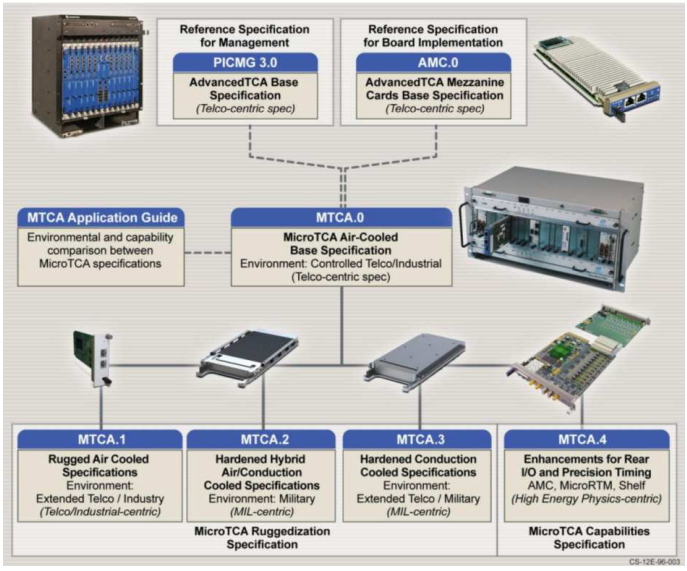

Fig. 1. MTCA standard versions [4]

- single embedded computer and concentrator but with redundant power and cooling due to high reliability requirements,
- cost optimized chassis with simplified power and management, where external computer performs function of hub, crate management and controller,
- stand alone miniature chassis with 2 or 3 AMC slots, simplified power and management for space-constrained applications and low voltage supply.

Figure 3 presents example of complex device based on MTCA chassis with custom CPU and FMC AMC carriers [5] with analogue and digital inputs and outputs developed in cooperation with industrial partner. It is part of experimental tokamak high voltage power supply control system. Figure 4 is an example of miniature, cost optimized MTCA case for two AMC modules. It is also available version of it with Rear Transition Module. External PC computer takes over the roles of Ethernet hub, management and PCIe switch using multimode fibres and SFP+/QSFP+ connectors.

1) Modular control system with embedded sub-ns time synchronization: The Warsaw University of Technology Photonics and Web Engineering Research Group (PERG) together with industrial partners (N.A.T, Pentair) developed concept of timing synchronization embedded into existing MTCA

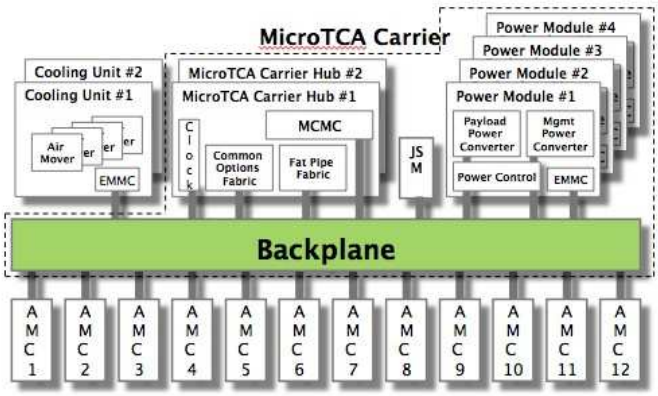

Fig. 2. Example MTCA architecture [**?**]

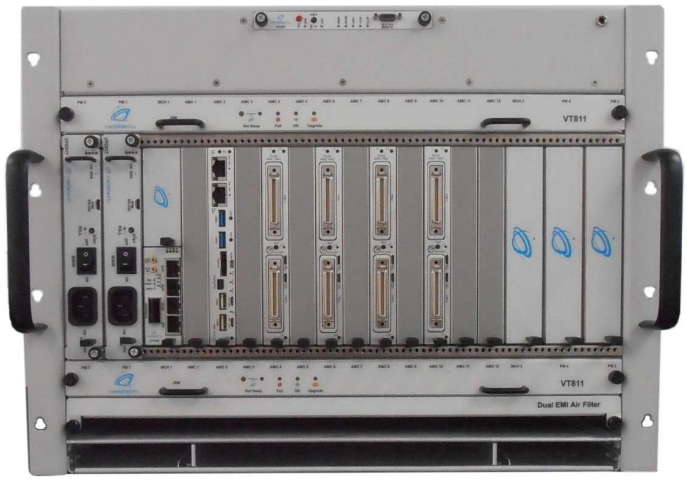

Fig. 3. Example MTCA system for MAST Tokamak [6]

Fig. 4. Miniature MTCA case for two AMC modules [6]

standard. It is entirely based on standard AMC/FMC modules, modified MTCA backplane and dedicated MCH timing mezzanine. The White Rabbit (WR) time synchronization system [2] was developed by High Energy Physics institutes working in the framework of Open Hardware Repository initiative [7].

Fig. 5. AMC carrier with FMC connectors together with high speed ADC FMC card developed and shared on OHL license [9]

Members of the group are: CERN, GSI, WUT and several scientific and industrial partners. The White Rabbit system provides time synchronisation with accuracy below 1ns and reference clock signal distribution among nodes separated by tens of kilometres. It is based on Synchronous Ethernet, PTP and Gigabit Ethernet technologies. The WR standard is intensively developed and provides support for applications like event acquisition and distribution, RF reference frequency transfer and related technologies. All the building components of the system are electronic modules developed and published under CERN OHL license [8]. The license defines the conditions under which a licensee will be able to use or modify the licensed material. Thanks to this it is possible to develop open hardware solutions in close cooperation with clients and industrial partners. It is attractive offer for parties that want to keep possibility to modify, improve, repair or produce the hardware and firmware. Figure 5 depicts example of complex device developed and published under Open Hardware License.

The MTCA system is an alternative for platform based on PXI/PXIe standard. The main difference is support for analogue and RF applications, embedded sub-ns synchronization and fully redundant architecture. From hardware point of view the MTCA platform enables effective integration of analogue and digital subsystems. Existing solutions usually separate these tasks to individual crates while MTCA.4 simplifies this task by integration of dedicated Rear Transition Modules (RTM) together with special backplane and power supplies. RTM facilitates integration of precision analogue and RF subsystems with digital FPGA based processing chains. It is critical for applications like radars, Software Defined Radio, accelerator diagnostics, low lever RF for linear accelerators. Thanks to modular architecture, embedded time synchronisation, support for analogue and digital processing chain further miniaturization of complex data acquisition and processing systems is possible. Existing real time systems like PXI/PXIe are baed on IEEE1588 solutions which provide only submicrosecond synchronisation capability without synchronous reference signal distribution. Described system provides 1000-fold improvement providing time and frequency synchronization and in addition, distribution of RF signal utilizing DDS over WR technology [10].

2) MTCA.4 support for analogue and RF applications: Noise and interference immunity in precise measurement devices plays key role because it influences overall performance

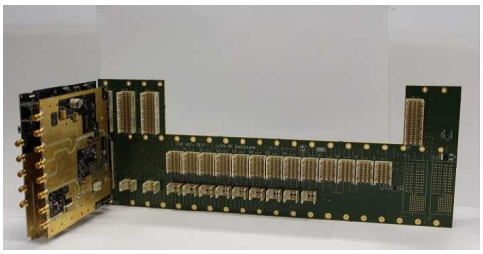

Fig. 6. Radio Frequency Backplane [11]

of the system. Integration of high performance, high speed digital processing subsystem with high sensitivity, analogue sections is not trivial task due to their mutual influence in terms of interference generation and propagation. There are many interference sources and ways of their propagation. Degradation of analogue signal quality must be addressed during development of the system. One can describe three most relevant interference sources:

- interferences from external sources that propagate through not efficient shielding and cabling, i.e. radio diffusion,
- interferences from internal sources, due to coupling between digital and analogue subsystems, coupling with adjacent modules,
- interferences from power supplies.

The MTCA.4 platform was designed to mitigate these issues. The architecture defines dedicated RF Backplane for analoge RTM modules (fig.6). It provides low jitter clock signal, low noise power supply and control signals distribution. The backplane has dedicated connector for low jitter clock generation module and two slots for low noise power supplies. The RF Backplane was developed by DESY in cooperation with Institute of Electronic Systems. Commercial supplier is N.A.T.

MTCA.4 enclosure provides electromagnetic shielding for installed AMC, RTM and supply modules. All the modules have dedicated panels with EMC gaskets. The crate construction was optimized to minimize interference coupling between analogue and digital compartments. The AMC modules are optimized for high speed connectivity, management and digital processing while separated RTM modules are dedicated for analogue processing chains, RF and low level signal conditioning. The aforementioned properties cause that MTCA.4 is often selected as building platform for mixed signal systems. Main applications are: integrated radiocommunications systems utilizing software defined ratio technology, low level RF circuits for free electron laser facilities (i.e. FLASH, DESY). Additional advantage of the system is much lower occupied space because analogue modules are installed in rear compartment of the same MTCA crate.

3) WR-MCH timing module: Standard MTCA backplane defines Fat Pipe interfaces between MCH and AMC slots. These interfaces consist of 4 bi-directional gigabit lanes. Even with utilisation of PCIe Gen 3 interface, available bandwidth is limited to 32GT/s. It is not sufficient for many applications, because effective data rate available by application usually does not exceed half of theoretical link rate. Another limitation of high speed processing systems is available electrical power per computing module in AMC form-factor. Recently introduced (by N.A.T.) high speed optical and copper links which consists of MCH-PHYS module with 16-lane PCIe gen 3 connectivity and optional PCIe extension card enable either utilisation of full PCIe bandwidth between MCH and CPU or even external workstation. Such integrated solution is optimal choice for applications related with processing of massive amounts of data where cooperation of several crates is required. However, in such systems there are required additional functionalities that were not addressed entirely during MTCA.4 standard development. On of the functionality is precise time synchronization of the modules, distribution of common clock and synchronization to the external local oscillator. Practical implementation of mentioned functionality is possible by utilisation of dedicated AMC board with timing receiver, but such solution has several drawbacks like clock signal jitter degradation by multiple passages via MCH and occupation of precious slots in the crate.

Due to limitations specified above, Author developed novel solution which extends functionality of existing N.A.T MCH with White Rabbit receiver capability.

The PICMG standard defines the MCH features:

- IPMI management (1-st Tongue)
- Gigabit Ethernet switch (1-st Tongue)
- clock generation and distribution (2-nd Tongue)
- Fat Pipe switch, PCIe, Ethernet or SRIO

The WR receiver is tightly coupled with existing Tongue 1 management board and Tongue 3 PCIe Hub module and replaces existing Tongue 2 clock distribution board. The receiver is perfect solution for low RF, signal detection, processing and real time control applications. All synchronisation features are available with WR-enabled Pentair MTCA backplane. Main feature is ability to generate custom clock signals locked to main WR-clock with any frequency and phase locked to the source installed within WR network.

The block schematic of WR-MCH is presented in fig.8. The module was designed to perform following functions:

- Dual, redundant White Rabbit (WR)/PTP timing receiver with sub-ns accuracy provides crate-wide timing reference over the M-LVDS bus. It is also possible to implement other custom time synchronization protocols like SyncE or TTC.
- Dedicated SFP+ cage for WR available on front panel. Second, redundant SFP+ is available on double width panel.
- Distribution of low jitter clock signals with up to three different frequencies locked to same WR 125MHz reference, common for whole WR domain.
- Dual channel DDS-RF generator. It provides ability to generate any frequency which is phase-locked to the source installed in any place of WR network
- Dual, ultra-low jitter bi-directional MTCA-compliant clock mux for both CLKA and CLKB clock trees
- Trigger and interlock distribution generated by WR timing receiver

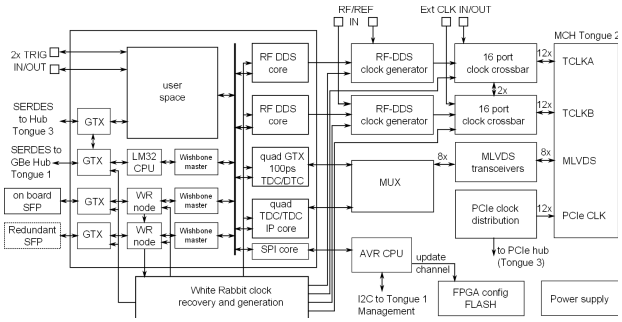

Fig. 7. WR-MCH module block schematic

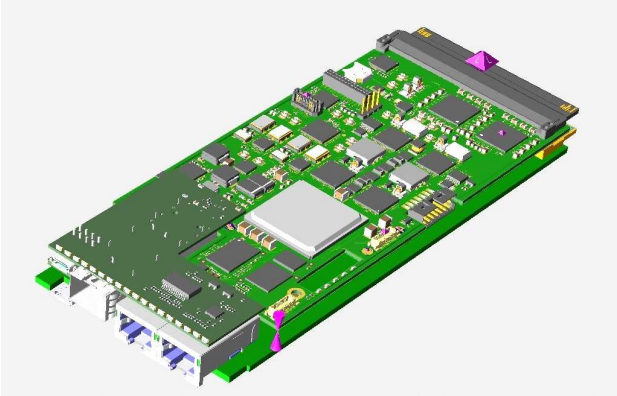

Fig. 8. view of WR-MCH module (PCIe hub module not visible)

- Trigger generation based on local trigger inputs which can be routed to the MLVDS bus.
- Dedicated two MMCX clock and trigger input/output connectors on the front panel
- Single width PCB form-factor and electrical compatibility with existing N.A.T. MCH (fig.7)

All M-LVDS features are available only in WR-enabled MTCA backplanes which need to have the MLVDS lines routed to the Tongue 2 connectors. Pentair backplanes can be delivered with WR-capability on request. User can also enable or disable such configuration by replacement of the resistor bridges.

II. Conclusion

The MTCA.4 is unviersal platform dedicated for real time measurement and control systems, RF front-end stations [12]. WR-enabled MCH opens new possibilities for MTCA.4 standard. Example applications that fully utilize described features are: control system for quantum computing and processing front-end for passive radars. It offers completely new possibilities for applications which were not yet identified

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References

[1] https://www.picmg.org/openstandards/microtca/
[2] http://www.ohwr.org/projects/white-rabbit/wiki/synchronization
[3] https://www.picmg.org/openstandards/advancedtca/
[4] https://picmg.org/wp-content/uploads/MicroTCA_Application_Guide_final-_rev1_1.pdf
[5] http://www.vita.com/fmc
[6] B Juszczyk et al., *Management and protection system for superconducting tokamak*, Proceedings of SPIE, 2015, Pages 96622O-96622O-7, doi:10.1117/12.2205486
[7] http://www.ohwr.org/
[8] http://www.ohwr.org/projects/cernohl/wiki
[9] http://www.ohwr.org/projects/afck
[10] http://www.ohwr.org/projects/wr-d3s/wiki/RF_distribution_demo
[11] http://accelconf.web.cern.ch/accelconf/IPAC2014/papers/ wepme069.pdf
[12] http://spaceops2012.org/proceedings/documents/ id1240286-Paper-001.pdf