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Electron and Hole Current Switching n-i-p-Type Semiconductor Quantum Dot Transistor

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Abstract For the future development of semiconductor quantum dot transistors, a novel n-i-p-type semiconductor quantum dot transistor consisting of an n-type source, an i-type dot, and a p-type drain is presented in this paper. The explicit steady-state solution to a set of an infinite number of stochastic theoretical probability equations is given. The solution is applicable to both metal and semiconductor quantum dot transistors. The electron and hole current characteristics controlled by means of the gate voltage are computed numerically, and it is pointed out that the electron or hole current state can be selected by applying a positive or negative gate voltage.

1 Introduction

Quantum transistors are regarded as being the most suitable key component for next-generation advanced high-density integrated circuit technology. Therefore, quantum transistors have been the subject of active research in recent years, in particular, with relevance to the fields of nano- and/or atomic-scale technologies. Although quantum transistors still need to be improved for use as commonly applicable performance transistors in conventional integrated circuit technology, it is widely believed that they will provide innovative paths for future development of low-power, high-speed digital information technologies.

Among quantum transistors, the quantum dot transistor in particular is considered to be a fundamental building block for quantum device technologies, and has been intensively explored both experimentally and theoretically [1]. Technologies for fabricating quantum dot transistors have now reached such a level that the electrical characteristics can be precisely controlled by the accurate control of the device structure configuration processes [2]. Therefore, it is important to develop a simple theoretical method applicable to practical device analysis and design.

The foundations for the development of quantum dot transistors were first established through the theoretical study of the resistance properties of thin metal films [3], the concept of the tunneling resistance at the contact boundary of two metals having different Fermi levels [4], and consideration of charging quantization [5]. On the basis of the above considerations, theoretical concepts, including the Coulomb blockade phenomena for a prototype quantum dot transistor, were developed [6] [7]. The theory has been extended to include a method of stochastic theoretical probability equations, effects of quantum energy levels, and the discrete charging energy in the dot [8]. Furthermore, simulation studies based on the above theoretical considerations and simplified analytical treatments have been reported [9]-[12]. It is useful if an explicit solution is obtained for above problems, however, the derivation of such an explicit solution is generally complex, and an explicit solution for such the problems has not yet been reported.

Although a solution that includes the time variation of the probabilities is mathematically advantageous for detailed descriptions of device operation, a steady-state solution generally comprises a simpler formula and is sufficiently useful for practical analyses and design. The derivation of the explicit

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steady-state solution for the equations is considered in this paper. For the derivation, a charging process is treated as a synthesis of four transitions. The transitions are flow-in tunneling from the source to the dot and from the drain to the dot, and flow-out tunneling from the dot to the source and from the dot to the drain.

For a quantum dot, a semiconductor dot can be implemented as well as a metal dot. An n-i-p-type semiconductor quantum dot transistor is suggested as a novel type structure in this paper. The n-i-p-type structure consists of an n-type source, an i-type dot, and a p-type drain. As is well known, there is electron current in an n-type semiconductor and a hole current in a p-type semiconductor. Experiments on the point contact channel connecting n-type and p-type source/drain have been reported, and the electron current in n-type source/drain under a positive gate voltage and hole current in p-type source/drain under a negative gate voltage have been demonstrated [13]. These experimental results support the possibility that the n-i-p-type device introduced in this paper can yield a new function to select an electron current or a hole current.

It is therefore expected that some particularly useful characteristics could be obtained by introducing the n-i-p-type structure. Analyses of the n-i-p-type quantum dot transistor and device are thus very important for the development of quantum transistors. From the viewpoint of a future no-error information system based on all-error-detecting and all-error-correcting rules, a no-error electronic circuit system and a no-error communication system are necessary. The feasibility of a no-error optical communication system has been experimentally demonstrated [14], and the quantum dot transistor is considered be important to demonstrate feasibility of the no-error electronic circuit system [15].

In the second section, the metal quantum dot transistor is considered as a fundamental step for analyses of the semiconductor quantum dot transistor. The semiconductor quantum dot transistor is considered in the third section. The electron and hole current characteristics controlled by means of the gate voltage are considered in detail.

2 Characteristics of the Metal Dot Transistor

2.1 Stochastic Equations and Steady-State Solution

In this section, quantum dot transistors implementing metal quantum dots are considered, and an analytical method based on a stochastic theory that can be generally applied to the semiconductor quantum dot transistor to be presented later is introduced. The circuit model for the quantum dot transistor is shown in Fig. 1. In the circuit model, R_S and R_D represent the tunneling resistances of the source- and drain-side barriers, and C_S, C_D, and C_G are the dot-to-source, the dot-to-drain, and the dot-to-gate capacitances, respectively.

The fundamental concept for analyses of the current-voltage characteristics of the quantum dot transistor is based on the assumption that tunneling transitions of electrons to or from the dot occur one by one. For the analyses, let $P_N(t)$ be the probability of the charging state that N electrons are confined in the dot at time t, and the probability that an electron tunnels into or out from the dot in the charging state N in an infinitesimally short time interval dt is given by $\lambda_N\, dt$ or $\mu_N\, dt$, respectively. It is reasonable to assume that the probability of two or more electrons tunneling in the time interval dt is of second or higher order smallness with respect to dt. Since higher order simultaneous tunneling of two or more electrons is not common in normal conduction, and is seen as a cooper pair transition, being a particular phenomenon observed at superconductor junctions, it is permissible to neglect the higher order tunneling in the

treatment of tunneling in the quantum dot transistor. Furthermore, a co-tunneling phenomenon should also

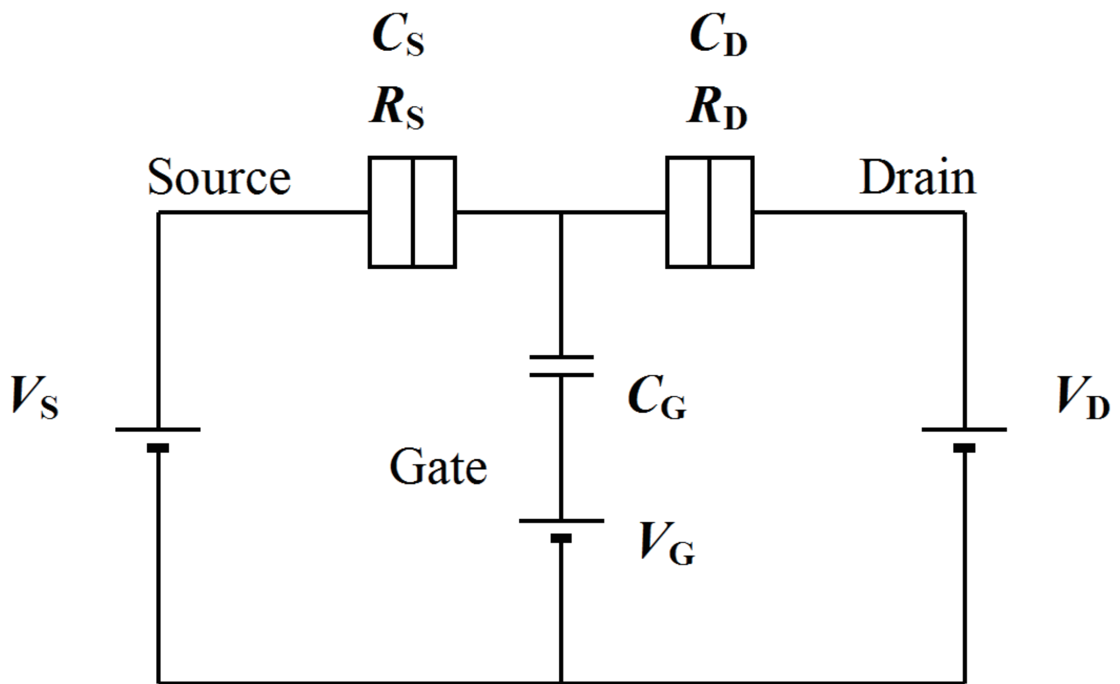

Fig. 1 Quantum dot transistor model.

be considered for accuracy; however, it can be neglected for the treatment as a fundamental step. The charging electron number state transition diagram is depicted in Fig.2.

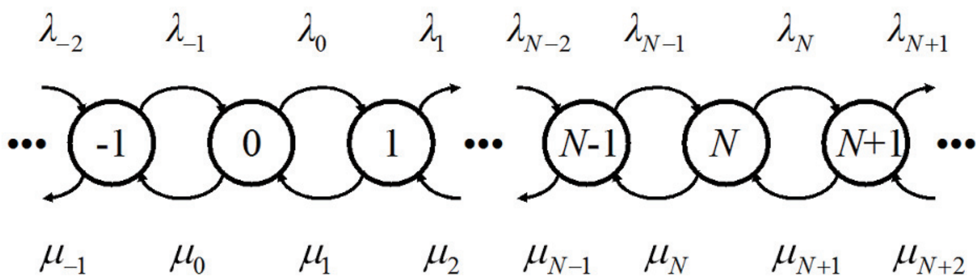

Fig. 2 State transition diagram.

From the above discussions, a set of equations for the probabilities of the states, where N electrons are confined in the dot at time t, is given by

$$\frac{d}{dt}P_N(t) = -(\lambda_N + \mu_N)P_N(t) + \lambda_{N-1}P_{N-1}(t) + \mu_{N+1}P_{N+1}(t) \quad (-\infty < N < \infty) \tag{1}$$

From a mathematical point of view, Eq. (1) is an equation that describes creation and destruction processes in the stochastic theory. A time-varying probability solution is useful for detailed analyses, and can be obtained if the above equations are exactly solved. The steady-state solution, however, is also important and useful for practical analyses of the quantum dot transistors because of its simplicity. Therefore the derivation of the steady-state solution is considered.

Assuming that p_N is the probability in a steady-state, Eq. (1) becomes

$$(\lambda_N + \mu_N)p_N = \lambda_{N-1}p_{N-1} + \mu_{N+1}p_{N+1} \quad (-\infty < N < \infty) \tag{2}$$

It can be assumed here that the upward and downward transition rates illustrated in Fig.2 are equivalent because of the steady-state, and thus, the above equations are simplified and become:

$$\lambda_N p_N = \mu_{N+1}p_{N+1} \qquad (-\infty < N < \infty) \tag{3}$$

Using the probability p_0 as a initial term to solve the above recurrence formula Eq. (3), solutions for the probability p_N for positive and negative values of N are respectively given by:

$$p_N = p_0 \prod_{r=1}^{N}\left(\frac{\lambda_{r-1}}{\mu_r}\right) \qquad (1 \le N < \infty) \tag{4a}$$

$$p_{-N} = p_0 \prod_{r=1}^{N}\left(\frac{\mu_{-r+1}}{\lambda_{-r}}\right) \qquad (1 \le N < \infty) \tag{4b}$$

The undetermined probability p_0 in the above equations can be fixed by using the axiom in probability theory that requires the sum of all probabilities to be equal to unity.

$$\sum_{N=-\infty}^{\infty} p_N \equiv 1$$

The application of the formula gives the following expression for p_0.

$$p_0 = \frac{1}{1 + \sum_{N=1}^{\infty}\prod_{r=1}^{N}\left(\frac{\lambda_{r-1}}{\mu_r}\right) + \sum_{N=1}^{\infty}\prod_{r=1}^{N}\left(\frac{\mu_{-r+1}}{\lambda_{-r}}\right)} \tag{5}$$

In the above analyses a negative value of N represents positively charged states of the dot, and corresponds to a lack of N electrons in the metal dot or to an excess of N holes in a semiconductor dot introduced in a later section.

2.2 Gate Voltage and Electron Tunneling

Before analyzing the semiconductor quantum dot transistors, it is important to understand the precise characteristics of a basic and simple metal quantum dot transistor. Fig. 3 and 4 show potential diagrams for the metal quantum dot transistor when positive and negative gate voltages are applied, respectively. In the metal quantum dot transistor, the current is carried only by electrons.

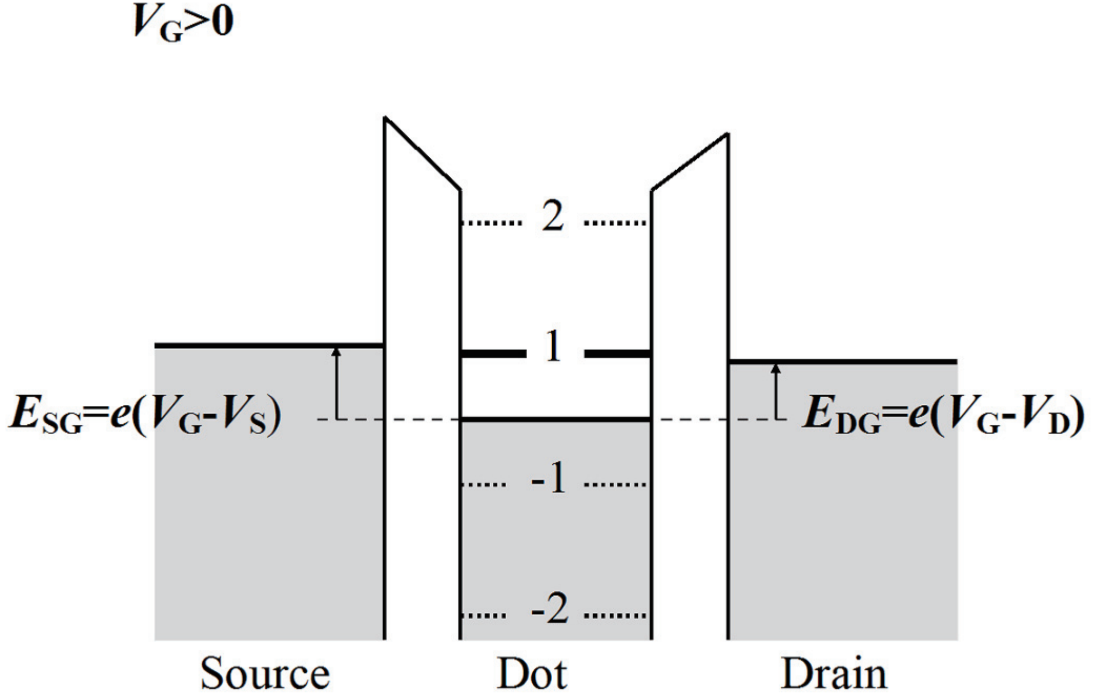

Fig. 3 Potential diagram when positive gate voltage is applied.

The flow-in rate of electrons to the dot λ_N when N electrons are charged in the dot can be derived on the basis of the concepts given in the above figures. The equivalent voltage in the dot to an electron flowing into the dot, which is an increment in energy resulting from the addition of the electron to the dot, can be represented by an equation independent of the sign of N in this case and is given by:

$$\frac{1}{e}\left\{\frac{(N+1)^2}{2C_\Sigma}e^2-\frac{N^2}{2C_\Sigma}e^2\right\}=\frac{1}{C_\Sigma}\left(N+\frac{1}{2}\right)e$$

The above equation is independent of the sign of N, and the following representations $C_\Sigma=C_S+C_D+C_G$ and e for the positive elementary electric charge are used. A total flow-in rate λ_N of electrons to the dot is given

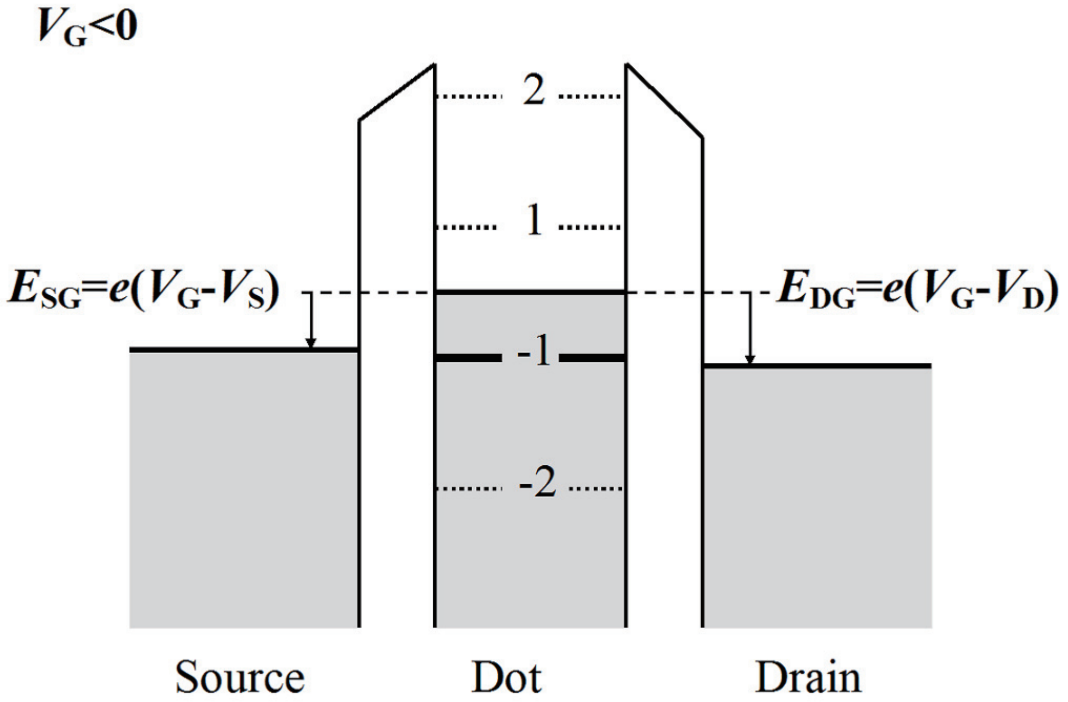

Fig. 4 Potential diagram when negative gate voltage is applied.

by a sum of flow-in rates from both sides.

$$\lambda_N = \lambda_{SN} + \lambda_{DN} \tag{6a}$$

In the above equation, λ_{SN} and λ_{DN} represent the flow-in rates of electrons from the source and drain, respectively. The flow-in rate from the source λ_{SN}, which can be derived from the orthodox theory [6] [7], is given by

$$\lambda_{SN} = \frac{V_G - (N+1/2)e/C_\Sigma - V_S}{eR_S\left(1 - e^{\frac{-e\{V_G-(N+1/2)e/C_\Sigma - V_S\}}{kT}}\right)} \tag{6b}$$

$$(-\infty \le N < \infty)$$

The flow-in rate from the drain λ_{DN} is given by a similar equation in which the subscript S is replaced with D.

Similarly, the flow-out rate of electrons μ_N can also be obtained. The equivalent voltage to an electron flowing out from the dot, which is a decrement in energy resulting from the subtraction of the electron from the dot, becomes an equation independent of the sign of N in this case and is given by:

$$\frac{1}{e}\left\{\frac{(N-1)^2}{2C_\Sigma}e^2-\frac{N^2}{2C_\Sigma}e^2\right\}=\frac{1}{C_\Sigma}\left(N-\frac{1}{2}\right)e$$

Therefore the flow-out rate μ_N is given by

$$\mu_N=\mu_{\mathrm{S}N}+\mu_{\mathrm{D}N} \quad \text{(7a)}$$

where $\mu_{\mathrm{S}N}$ and $\mu_{\mathrm{D}N}$ are the flow-out rates of an electron flowing from the dot to the source and from the dot to the drain, respectively. The flow-out rate to the source $\mu_{\mathrm{S}N}$ is given by:

$$\mu_{\mathrm{S}N}=\frac{V_\mathrm{G}-(N-1/2)e/C_\Sigma-V_\mathrm{S}}{eR_\mathrm{S}\left(\mathrm{e}^{\frac{e\{V_\mathrm{G}-(N-1/2)e/C_\Sigma-V_\mathrm{S}\}}{kT}}-1\right)} \quad \text{(7b)}$$

$$(-\infty\leq N<\infty)$$

and the flow-out rate to the drain $\mu_{\mathrm{D}N}$ is given by a similar equation in which the subscript $_\mathrm{S}$ is replaced with $_\mathrm{D}$.

2.3 Gate Voltage and Current Characteristics

Using the probabilities derived in Section 2.1 and the flow-in and flow-out rates given in Section 2.2, the steady-state current in the quantum dot transistor is obtained and is given as:

$$I=e\sum_{N-\infty}^{\infty}(\lambda_{\mathrm{S}N}-\mu_{\mathrm{S}N})p_N=e\sum_{N-\infty}^{\infty}(\mu_{\mathrm{D}N}-\lambda_{\mathrm{D}N})p_N \quad \text{(8)}$$

In the central part of Eq. (8), the summation of the first term corresponds to the flow-in current from the source to the dot, and summation of the second term corresponds to the flow-out current from the dot to the source. The first and second terms in the right-hand side of Eq. (8) correspond to the flow-out current from the dot to the drain and the flow-out current from the drain to the dot, respectively.

Fig. 5 shows the current-voltage (I-V_G) characteristics of the quantum dot transistor when positive and negative gate voltages are applied. Two current-voltage characteristics for temperatures of T=30 and 300 K are presented. The device parameters describing the transistor structure are taken as $C_\Sigma=1.0\times10^{-18}\,\mathrm{F}$ and $R_\mathrm{S}=R_\mathrm{D}=1.0\times10^{5}\,\Omega$. The values of $V_\mathrm{S}/(e/C_\Sigma)$=-0.1 and $V_\mathrm{D}/(e/C_\Sigma)$=0.1 are assumed for both the source-gate and drain-gate voltages. As shown in Fig.5, symmetric current-voltage characteristics are observed when both negative and positive gate-voltages are applied to the metal quantum dot transistor.

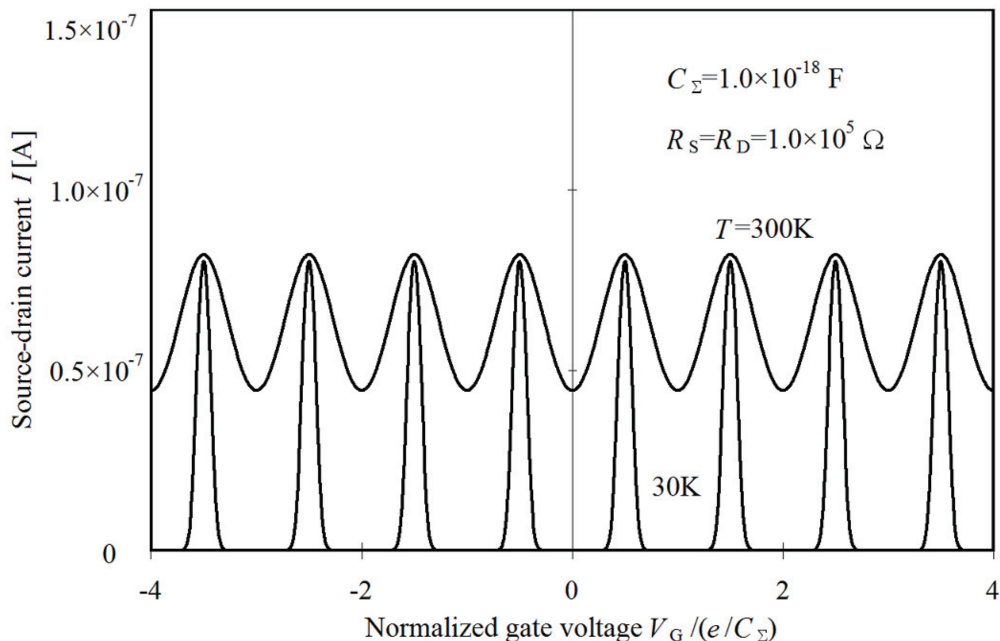

Fig. 5 Current characteristics when positive and negative gate voltages are applied.

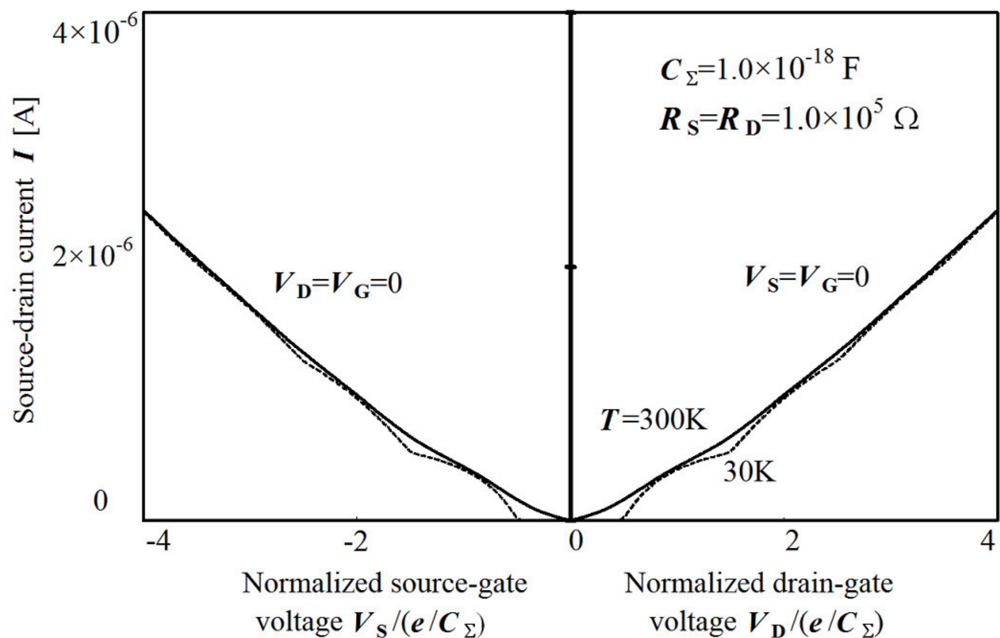

Fig. 6 Temperature characteristics of staircase on the metal quantum dot transistor when a drain or a source voltage only is varied.

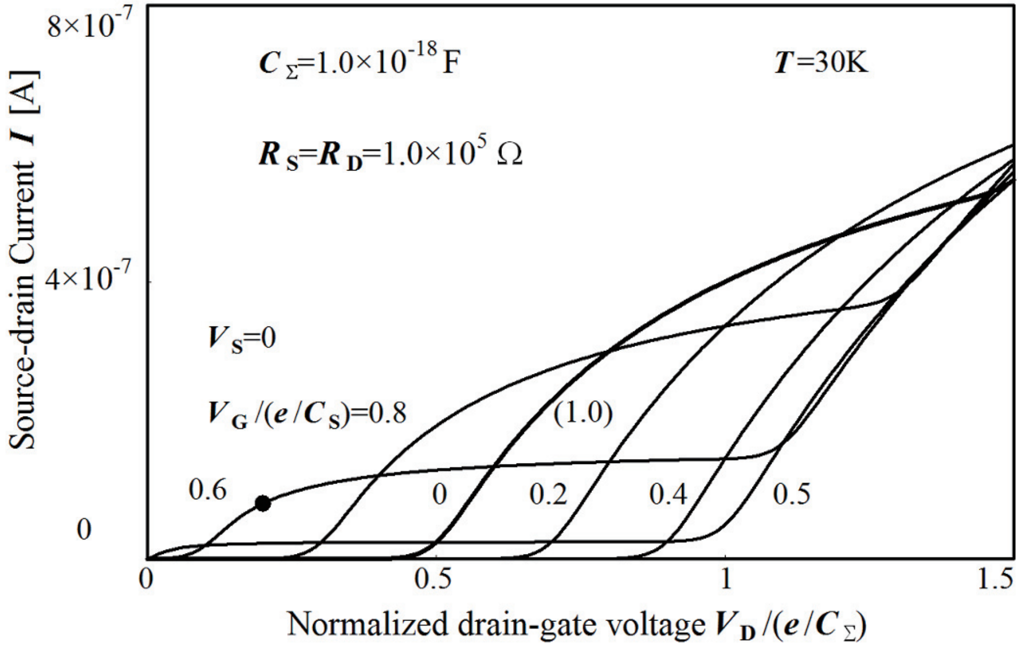

Fig. 7 Gate voltage characteristics of staircase on the metal quantum dot transistor when a drain voltage is varied. (● ; the current for V_S=0, $V_G/(e/C_\Sigma)$=0.6, and $V_D/(e/C_\Sigma)$=0.2)

To analyze the above characteristics, computations of the staircases are necessary. Fig. 6 shows the temperature dependence of the source-drain currents controlled by the source-gate and drain-gate voltages in the cases of T=30 K and 300 K. Clear steps can be seen on the T=30 K curve, though not in the case of T=300 K. For large values of V_D and $-V_S$, both the currents for 30 and 300 K increase linearly and overlap asymptotically. For T=0 K, while no curve is drawn in the figure, the lower corners of steps have more sharpness, however, the fundamental characteristics are similar to both the 30 and 300 K cases.

Fig. 7 shows the gate voltage dependence of the currents controlled by the drain-gate voltage for T=30 K. The currents are computed for the values of the normalized gate voltage $V_G/(e/C_\Sigma)$=0, 0.2, 0.4, 0.8, and 1.0, and the results show cyclic properties. The current in the case of the normalized gate voltage of 1.0 becomes the current in the case of the normalized gate voltage 0 recurrently. The symbol ● indicates the current value for conditions of V_S=0, $V_G/(e/C_\Sigma)$=0.6, and $V_D/(e/C_\Sigma)$=0.2. The conditions equivalently correspond to the case of $V_S/(e/C_\Sigma)$=-0.1, $V_G/(e/C_\Sigma)$=0.5, and $V_D/(e/C_\Sigma)$=0.1, and the current value is equal to the peak values of the oscillation for T=30 K in Fig.5. Based on Fig.7, several combinatorial conditions can be selected for various transistor operations.

3 Characteristics of n-i-p-Type Semiconductor Quantum Dot Transistor

3.1 n-i-p-Type Structure

In this section, a novel n-i-p-type semiconductor quantum dot transistor, consisting of an n-type source, an i-type dot, and a p-type drain, is presented, and the structure and the operational principle of the

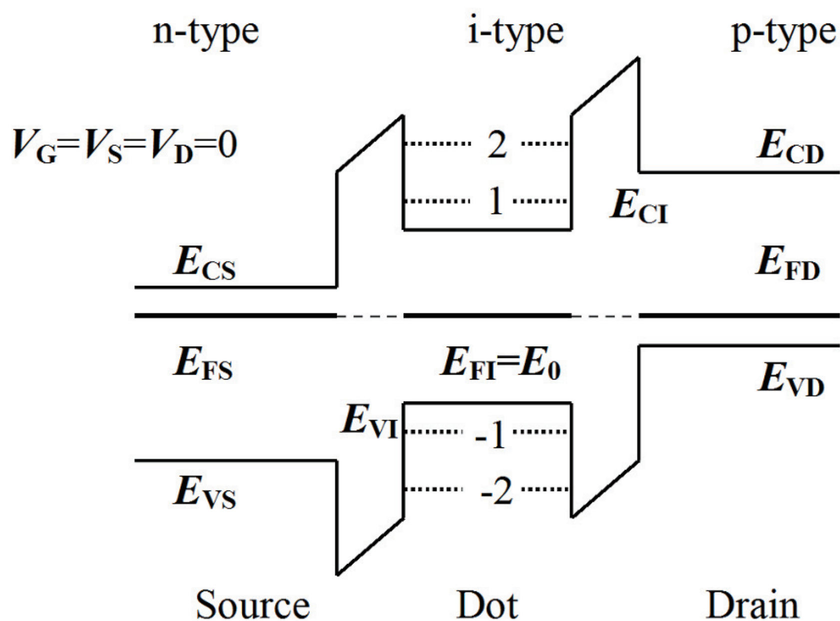

Fig.8 Band diagram of an n-i-p-type quantum dot transistor when zero voltages are applied.

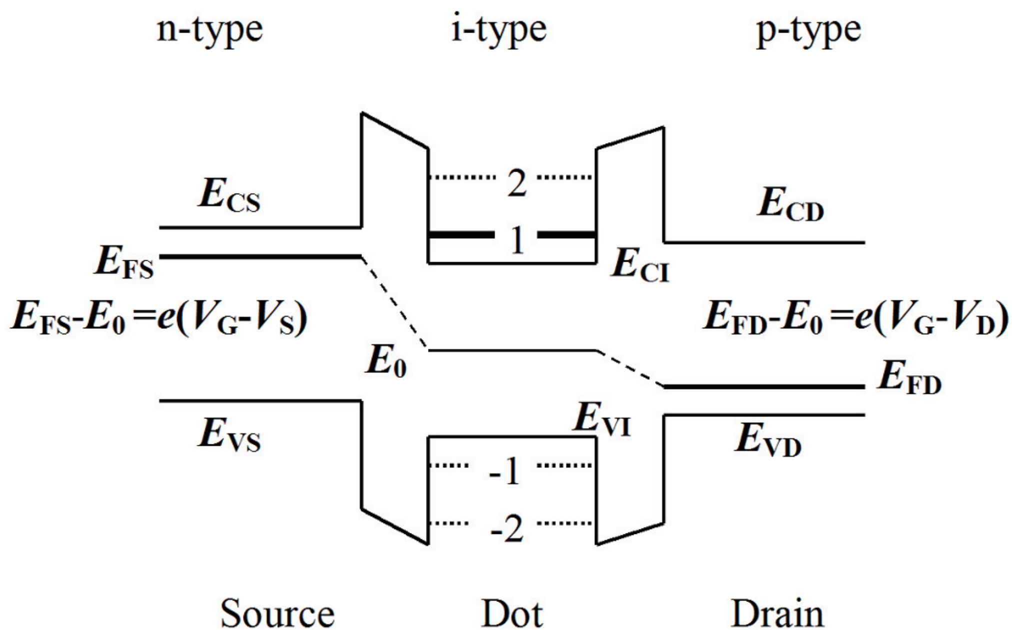

Fig.9 Band diagram of the n-i-p-type quantum dot transistor when a positive gate voltage is applied.

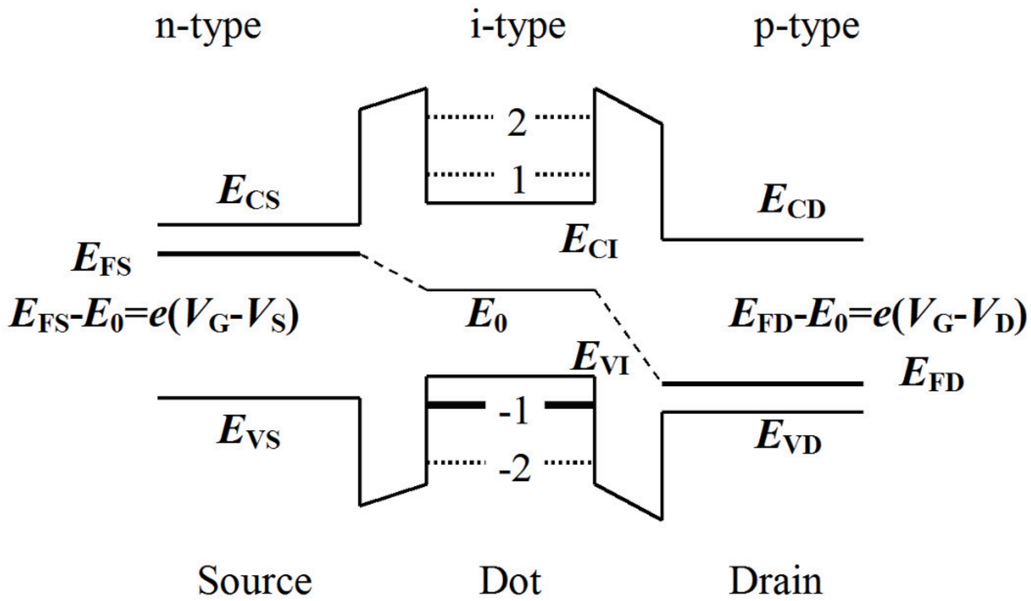

Fig.10 Band diagram of the n-i-p-type quantum dot transistor when a negative gate voltage is applied

transistor are discussed. The band diagram of the n-i-p-type transistor in thermal equilibrium is shown in Fig.8. Under these conditions, the applied voltages are zero ($V_G=V_S=V_D=0$), and the Fermi levels at the source E_{FS}, the dot E_{FI} , and the drain E_{FD} are aligned.

The current control phenomenon of the semiconductor quantum dot is similar to that of the metal quantum dot transistor. In the n-i-p-type semiconductor quantum dot transistor, however, both electrons and holes can be carriers of current, and the theory therefore has to be configured to include both electron and hole effects. The theory for both currents caused not only by electron tunneling but also by hole tunneling will be considered in a later section, and detailed analysis of the characteristics of the n-i-p-type transistor will be carried out.

3.2 Electron and Hole Tunneling

The band diagram of the n-i-p-type quantum dot transistor, when a positive gate voltage is applied, wherein the bottom of the conduction band at the source E_{CS} is adjusted to be slightly higher than the bottom of the conduction band at the drain E_{CD} by appropriately setting the external voltages V_S and V_D, is illustrated in Fig.9. As shown in the figure, the voltage differences applied to the source-dot and the dot-drain are given by V_G-V_S and V_G-V_D respectively. Under such bias conditions, the electrons and holes in the source and drain can be considered to be in quasi-thermal equilibrium since the source and the drain are relatively large and the dot is interacting with the source and drain. Therefore, the Fermi level in the dot should be considered under influences from both the source and drain sides, and will be discussed in detail later.

Under these conditions, electrons flow into the dot and holes flow out from the dot when a positive

gate voltage is applied. In the model, the charged particles confined in the dot are assumed to be electrons when a positive gate voltage is applied and holes when a negative gate voltage is applied as shown in Fig.10. In exactly terms, many states, in which infinite combinations of the numbers of electrons and holes giving the same difference N, are possible. It is assumed, however, that almost all electron-hole pairs confined in the dot have recombined since the band gap energy of the intrinsic semiconductor dot is considerably higher than the thermal energy at room temperature in a typical quantum dot transistor. The band gap energy is normally set to a value considerably higher than the thermal energy for operation of the quantum dot transistor.

Similar to the treatment of the metal dot transistor given in the previous section, the negative charge flow-in rate λ_N is given by

$$\lambda_N = \lambda_{\mathrm{S}N} + \lambda_{\mathrm{D}N} \tag{9a}$$

For a positive value of N, a negative charge flow-in rate to the dot λ_N is regarded as a sum of electron flow-in rates from the source $\lambda_{\mathrm{S}N}$ and the drain $\lambda_{\mathrm{D}N}$ to the dot. The two terms on the right-hand side of Eq. (9a) can be estimated in a similar manner to the former metal quantum dot transistor and are obtained by simply extending the orthodox theory giving

$$\lambda_{\mathrm{S}N} = \frac{1}{e^2 R_{\mathrm{Se}}} F_{\mathrm{S}}^{+}(E_{\mathrm{CS}})$$
$$\lambda_{\mathrm{D}N} = \frac{1}{e^2 R_{\mathrm{De}}} F_{\mathrm{D}}^{+}(E_{\mathrm{CD}}) \tag{9b}$$
$$(0 \le N < \infty)$$

where $F_{\mathrm{S}}^{+}(X)$ is given by

$$\boldsymbol{F}_{\mathrm{S}}^{+}(\boldsymbol{X}) = \int_{\boldsymbol{X}}^{\infty} \frac{1}{1+\mathrm{e}^{\frac{\boldsymbol{E}-\boldsymbol{E}_{\mathrm{FS}}}{\boldsymbol{kT}}}} \left(1 - \frac{1}{1+\mathrm{e}^{\frac{\boldsymbol{E}-\boldsymbol{E}_{\mathrm{Qe}}-(\boldsymbol{N}+1/2)\boldsymbol{e}^2/\boldsymbol{C}_{\Sigma}}{\boldsymbol{kT}}}} \right) \boldsymbol{dE}$$

In the above equations, R_{Se} and R_{De} are the tunneling resistances for an electron through the source and drain side barriers, respectively, and E_{Qe} is the lowest state of electrons in the conduction band of the dot biased by $-eV_{\mathrm{G}}$ and E_{FS} is the Fermi level in the source biased by $-eV_{\mathrm{S}}$. (3) The equation for $F_{\mathrm{S}}^{+}(X)$ is derived in a similar manner based on the concept for the derivation of Eq. (6b). The integrant in the equation consists of two parts; the first part is the Fermi-Dirac distribution in the source and the second part is the empty state distribution in the dot. While the Fermi level in the dot, when no electron is charged, is given by E_0, the Fermi level in the dot when an electron is charged, however, becomes the electron energy level of the charged electron, since the highest level of electron energies in the dot at temperature 0

K is the quantum energy level in the conduction band occupied by the last charged electron. Therefore the Fermi level when N electrons are charged into the dot is given by $E_{Qe}+(N+1/2)e^2/C_{\Sigma}$.

For derivation of Eq. (6b) to the metal, the value of the energy E for an electron can take any value between -∞ and ∞. For the semiconductor, however, the integration has to be limited to the conduction band for an electron. X=max{E_{CS}, E_{Qe}} should then be assumed as the lower bound of the integration because the lowest energy level of tunneling electrons is a higher value among both the lower bound levels in the source and the dot. $F_D^+(X)$ is given by an equation similar to the equation for $F_S^+(X)$, where the subscript $_S$ is replaced with $_D$. All other necessary rates can be calculated in a similar manner, and are given in the appendix.

3.3 Switching between Electron or Hole Current

The derived flow-in and flow-out rates in the previous section allow performance of the steady-state current calculations for the n-i-p-type semiconductor quantum dot transistor. The current can be considered separately for cases where positive and negative gate voltages are applied. When the gate voltage is positive, the current is an electron current I_e given by:

$$I_e = e\lambda_{S0}p_0 + e\sum_{N=1}^{\infty}(\lambda_{SN} - \mu_{SN})p_N = -e\lambda_{D0}p_0 + e\sum_{N=1}^{\infty}(\mu_{DN} - \lambda_{DN})p_N$$

The first and second terms in the central part of the above equation represent the flow-in current of electrons to the dot from the source, while the third term represents the flow-out current of electrons from the dot to the source. The right-hand side represents the same current of electrons on the drain side.

The current in the case of a negative gate voltage is a hole current I_h, and is given by:

$$I_h = -e\mu_{S0}p_0 + e\sum_{N--\infty}^{-1}(\lambda_{SN} - \mu_{SN})p_N = e\mu_{D0}p_0 + e\sum_{N--\infty}^{-1}(\mu_{DN} - \lambda_{DN})p_N$$

The first and second terms in the central part of the above equation represent the flow-out current of holes from the dot to the source, while the third term represents the flow-in current of holes from the source to the dot. The right-hand side represents the same current on the drain side.

Fig. 11 shows the dependencies of the electron and hole currents on the applied gate voltage. Two curves corresponding to T=30 and 300 K are shown. It is assumed that the parameters for the n-i-p-type semiconductor quantum dot transistor are taken as $C_{\Sigma} = 1.0\times10^{-18}\,\mathrm{F}$, $R_{Se} = R_{De} = 1.0\times10^{5}\,\Omega$, $R_{Sh} = R_{Dh} = 2.0\times10^{5}\,\Omega$, and 1.1 V for a band gap E_B of the semiconductor dot as a numerical example. Although various effects caused by the dependence of quantum levels on dot size can also be included for detailed analysis, consideration of such complex effects would probably make the characteristics that we have focused on here unclear. Therefore, calculations have been carried out for the case wherein quantum level continuum is permitted for electrons and holes. The Fermi levels in the n-type source and p-type drain, E_{FS} and E_{FD}, are assumed to be equal to E_{CS} and E_{CD} here in the computational model for simplicity. Both the source and drain voltages then become V_S=-E_B/(2e) and V_D=E_B/(2e) to align all the E_{CS}, E_{CI}, and E_{CD}.

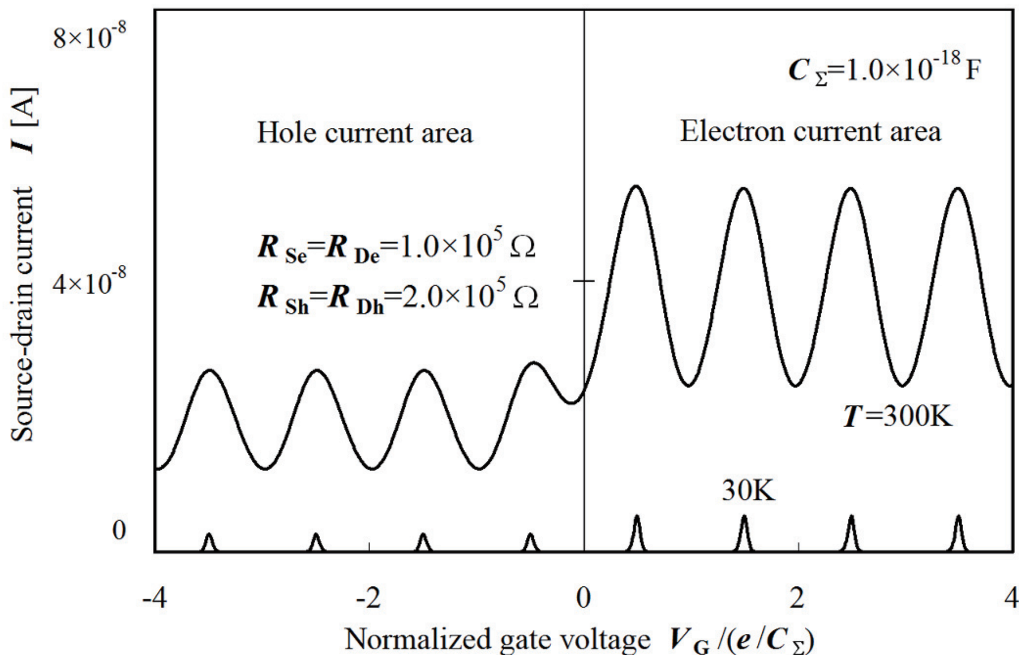

Fig.11 Electron and hole current characteristics.

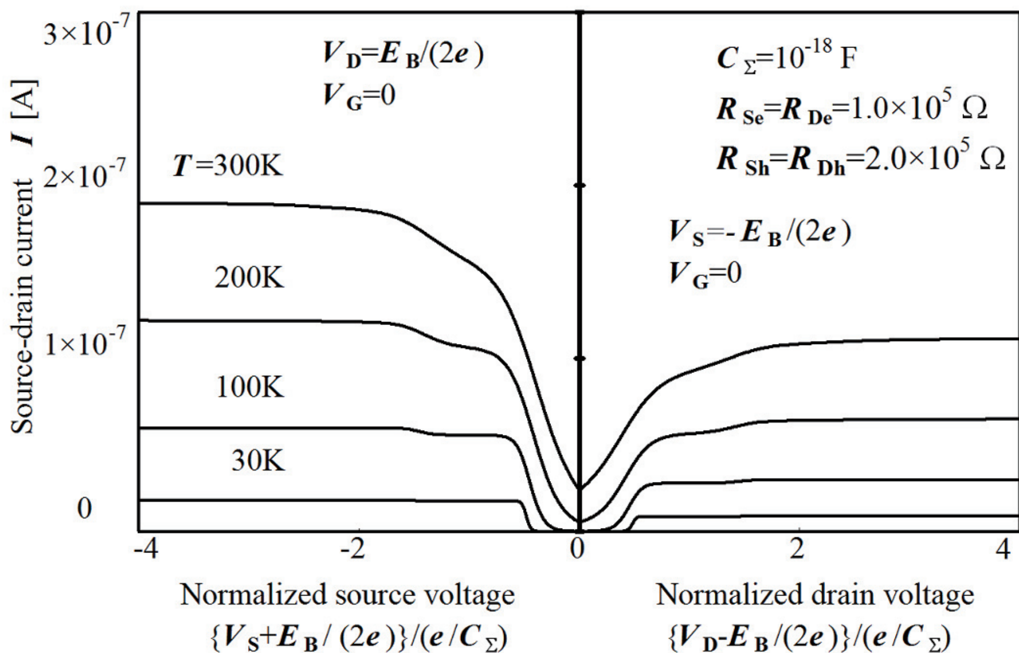

Fig.12 Temperature characteristics of staircase on the n-i-p-type quantum dot transistor when a drain-gate or a source-gate voltage is varied.

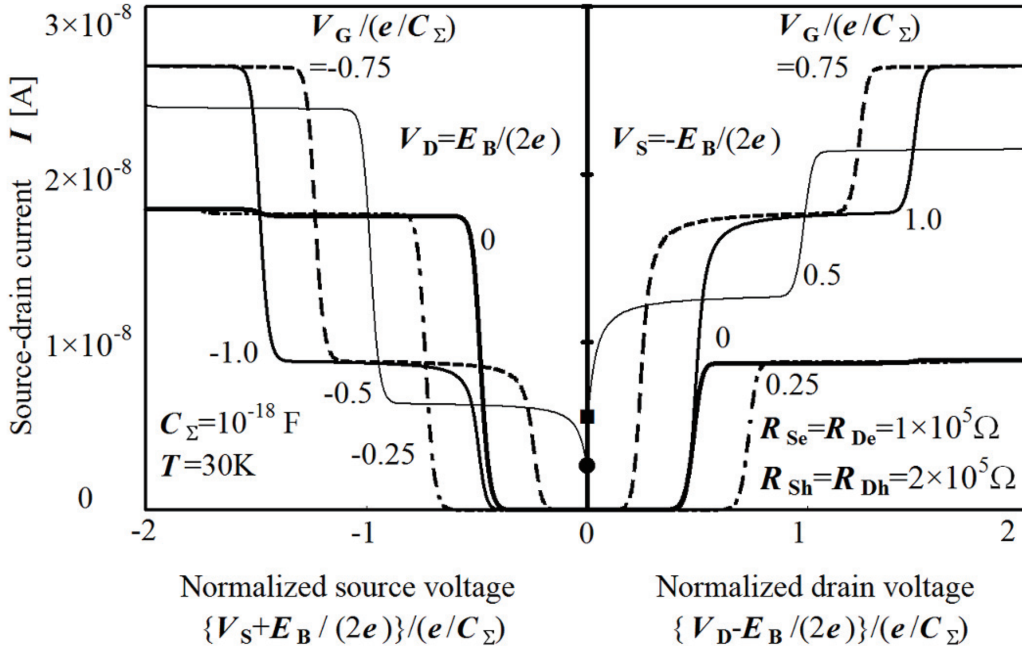

Fig.13 Gate voltage characteristics of staircase on the n-i-p-type quantum dot transistor when a drain-gate or a source-gate voltage is varied. (■ and ● ; the current values for V_S=-E_B/(2e), V_D=E_B/(2e), and V_G/(e/C_S)=0.5 and -0.5)

As shown in the figure, the direction of the current is invariant even if the sign of the gate voltage is changed. The current, however, is carried by electrons when the gate voltage is positive and by holes when gate voltage is negative, and both have different current intensities since the tunneling resistances for the electrons and holes have different values. It is clear that a new phenomenon with no amplitude difference cannot be observed from simple current-voltage characteristics because the sign of the current remains the same for both the positive and negative gate voltages. However, if a magnetic field is applied across the device, the Hall effect output voltage switched by the flows of electrons or holes can be observed.

Fig. 12 shows the temperature dependencies of the staircases for T=30, 100, 200, 300 K, and clear first steps are seen for each temperature. However, the second and higher order steps are not clear and have smaller jumps than the corresponding first order steps. The reason for the smaller jump properties for the second or higher order steps relates to a forbidden band limitation. For the metal case, a large number of electrons can contribute to the currents when large source or drain voltages are applied, and there is no such forbidden band limit. In general, the currents controlled by the drain voltage (right hand side in the figure) have larger values than those controlled by the source voltage (left hand side). The currents controlled by the drain voltage are based on hole current and the current by the source voltage are based on electron current. The differences between the electron and hole currents are caused by tunnel resistances, and are not based on the n-i-p-type structure, while the resistances include the important factors of electron

and a hole tunneling rates, the effective masses, and carrier densities.

The gate voltage dependence of the current controlled by the drain and the source voltages in the case of T=30 K are shown in Fig. 13. Values of 0, 0.25, 0.5, 0.75, and 1.0 are selected for the normalized gate voltage, and small steps due to the hole currents and large steps due to the electron currents appear according to the values of the gate voltage. The cyclic property is not achieved in the semiconductor quantum dot transistor currents because of a saturation effect. The symbols ■ and ● indicate the current values for conditions of V_S=-E_B/(2e), V_D=E_B/(2e), and V_G/(e/C_S)=0.5 and -0.5. Both the current values correspond to the peak currents in the electron and the hole current areas in Fig.11 respectively.

4 Conclusions

In this paper, a novel n-i-p-type semiconductor quantum dot transistor consisting of an n-type source, an i-type dot, and a p-type drain was presented, and electron and hole current characteristics for the transistor were theoretically analyzed. For the problems, an explicit steady-state solution to the stochastic theoretical probability equations was derived. The solution is equivalently applicable to both metal and semiconductor quantum dot transistors. As a result of the analysis, it was shown that an asymmetric property appears in the current-voltage characteristics and the electron or the hole current state can be switched by means of the applied gate voltage.

References

[1] K. K. Likharev "Single-Electron Devices and Their applications" *Proc. IEEE,* vol.87, no.4, pp.606-632, Apr. 1999.

[2] Y. Ono, N. M. Zimmerman, K. Yamazaki, and Y. Takahashi "Turnstile Operation Using a Silicon Dual-Gate Single Electron Transistor" *Jpn. J. Appl. Phys.,* vol.42, Part.2, no.10A, pp.L1109-L1111, Oct., 2003.

[3] C. J. Gorter "A Possible Explanation of The Increase of The Electrical Resistance of Thin Metal Films at Low Temperatures and Small Field Strengths" *Physica*, vol.XVII, no.8, pp.777-780, Aug. 1951.

[4] C. A. Neugebauer and M. B. Webb "Electrical Conduction Mechanism in Ultrathin, Evaporated Metal Films" *J. Appl. Phys*., vol.33, no.1, pp.74-82. Jan. 1962.

[5] J. Lambe and R. C. Jaklevic "Charge-Quantization Studies Using a Tunnel Capacitor" *Phys. Rev. Letters*, vol.22, no.25, pp.1371-1374, Jun. 1969.

[6] I. O. Kulik and R. I. Shekhter "Kinetic Phenomena and Charge Discreteness Effects in Granulated Media" *Sov. Phys.-JETP*, vol.41, no.2, pp.308-316, Feb. 1975.

[7] H. Grabert, G.-L. Ingold, M. H. Devoret, D. Esteve, H. Pothier, and C. Urbina "Coulomb Blockade of Tunneling in Ultrasmall Junctions" *Z. Phys.,* vol.B84, no.143, pp.199-213, 1991.

[8] C. W. J. Beenakker "Theory of Coulomb-Blockade Oscillations in The Conductance of a Quantum Dot" *Phys. Rev. B*, vol.44, no.4, pp.1646-1656, Jul. 1991-II.

[9] S. Amakawa, H. Maejima, H. Fukui, M. Fujishima, and K. Hoh "Single-Electron Circuit Simulation" *IEICE Trans. Electron*., vol.E81-C, no.1, pp.21-29, Jan. 1998.

[10] K. Natori and N. Sano "A Compact Model for The Current-Voltage Characteristics of a single Electron Transistor in The Resonant Transport Mode" *IEICE Trans. Electron.,* vol.E82-C, no.9, pp.1599-1606, Sep. 1999.

[11] A. Scholze, A. Schenk, and W. Fichtner "Effect of The Tunneling Rate on The Conductance Characteristics of Single-Electron Transistors" *IEICE Trans. Electron*., vol.E83-C, no.8, pp.1242-1246, Aug. 2000.

[12] K. Uchida, K. Matsuda, J. Koga, R. Ohba, S. Takagi, and A. Toriumi "Analytical Single Electron

Transistor (SET) Model for Design and Analysis of Realistic SET Circuits" *J. Appl. P* vol.39(2000) Part I, no.4B, pp.2321-2324, Apr. 2000.

[13] H. Ishikuro and T. Hiramoto "On the Origin of Tunneling Barriers in Silicon Single Electron and Single Hole Transistors" Appl. Phys. Lett. Vol.74, no.8, pp.1126-1128, Feb. 1999.

[14] C. Fujihashi "Detection Experiment of Decision Errors Caused by Quantum Noise in an Optical Signal System" *IEEE J. Lightwave Technol*., vol.16, no.1, pp.27-31, Jan. 1998.

[15] C. Fujihashi "The Quantum Control Limit to a Single Electron Transistor and Operation Frequency Improvements" *Proc. 2005 5th IEEE Conference of Nanotechnology,* no.WE-PS1-7, Nagoya, Japan, Jul. 2005.

Appendix

The negative flow-in rate to the dot for a negative value of N is regarded as a sum of hole flow-out rates from the dot to the source and the drain, and the two terms in the right-hand side of Eq. (9a) become

$$\lambda_{\mathrm{S}N} = \frac{1}{e^2 R_{\mathrm{Sh}}} F_{\mathrm{S}}^{-}\left(E_{\mathrm{VS}}\right)$$

$$\lambda_{\mathrm{D}N} = \frac{1}{e^2 R_{\mathrm{Dh}}} F_{\mathrm{D}}^{-}\left(E_{\mathrm{VD}}\right) \qquad \text{(A1)}$$

$$(-\infty < N \leq -1)$$

where $F_{\mathrm{S}}^{-}(X)$ is given by

$$F_{\mathrm{S}}^{-}(X) = \int_{-\infty}^{X} \frac{1}{1+\mathrm{e}^{\frac{E-E_{\mathrm{FS}}}{kT}}} \left(1 - \frac{1}{1+\mathrm{e}^{\frac{E-E_{\mathrm{Qh}}-(N+1/2)e^2/C_{\Sigma}}{kT}}} \right) dE$$

In the above equations, R_{Sh}, R_{Dh} are the tunneling resistances for a hole through the source and drain side barriers, respectively, and E_{Qh} is the lowest state of a hole in the valence band of the dot where X=min{E_{VS}, E_{Qh}}. $F_{\mathrm{D}}^{-}(X)$ is given by an equation similar to the equation for $F_{\mathrm{S}}^{-}(X)$ where the subscript $_{\mathrm{S}}$ is replaced with $_{\mathrm{D}}$.

The negative charge flow-out rate μ_N is derived in a similar manner to the negative charge flow-in rate λ_N .

$$\mu_N = \mu_{\mathrm{S}N} + \mu_{\mathrm{D}N} \qquad \text{(A2)}$$

For positive value of N, negative charge flow-out rates from the dot become

$$\mu_{\mathrm{S}N} = \frac{1}{e^2 R_{\mathrm{Se}}} G_{\mathrm{S}}^{+}\left(E_{\mathrm{CS}}\right)$$

$$\mu_{\mathrm{D}N} = \frac{1}{e^2 R_{\mathrm{De}}} G_{\mathrm{D}}^{+}\left(E_{\mathrm{CD}}\right)$$

$$(\, 0 \le N < \infty)$$

where $G_{\mathrm{S}}^{+}(X)$ is given by

$$G_{\mathrm{S}}^{+}(X) = \int_{X}^{\infty} \left(1 - \frac{1}{1 + \mathrm{e}^{\frac{E - E_{\mathrm{FS}}}{kT}}} \right) \frac{1}{1 + \mathrm{e}^{\frac{E - E_{\mathrm{Qe}} - (N - 1/2) e^2 / C_{\Sigma}}{kT}}} dE$$

For negative value of N, negative charge flow-out rates from the dot become

$$\mu_{\mathrm{S}N} = \frac{1}{e^2 R_{\mathrm{Sh}}} G_{\mathrm{S}}^{-}\left(E_{\mathrm{VS}}\right)$$

$$\mu_{\mathrm{D}N} = \frac{1}{e^2 R_{\mathrm{Dh}}} G_{\mathrm{D}}^{-}\left(E_{\mathrm{VD}}\right)$$

$$(\, 0 \le N < \infty)$$

where $G_{\mathrm{S}}^{-}(X)$ is given by

$$G_{\mathrm{S}}^{-}(X) = \int_{-\infty}^{X} \left(\mathbf{1} - \frac{\mathbf{1}}{\mathbf{1} + \mathrm{e}^{\frac{E - E_{\mathrm{FS}}}{kT}}} \right) \frac{\mathbf{1}}{\mathbf{1} + \mathrm{e}^{\frac{E - E_{\mathrm{Qh}} - (N - \mathbf{1}/\mathbf{2}) e^{\mathbf{2}} / C_{\Sigma}}{kT}}} dE$$