Multistage System High-Speed Clock Difficulty in VLSI

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Abstract A Multi-Synchronization (MS) write-in shared buffer switch architecture is presented for a multistage system to relieve clock timing difficulty on various length connection links between switch elements in ultra high speed VLSI. The above architecture is useful to obtain flexibility and feasibility of VLSI design at sub nsec pulse switching because 30 mm deference in linking wire length on a system VLSI chip gives more than 100 psec delay deference. A necessary buffer size for covering the design difficulty is evaluated by computer simulation. It is shown that a buffer size as same as that of a practical switch only is required for MS switch to ensure a same level with a performance of an ideal Single Synchronization (SS) write-in switch.

1 INTRODUCTION

In the last decade, Asynchronous Transfer Mode (ATM) switching technologies for Broadband Integrated System Digital Network (B-ISDN) have been rapidly developed[1]. Indeed a fabrication of a high speed ATM switch was reported[2], and a high speed ATM switch[3] by a photonic technology also was demonstrated. For a switching system, generally, high-speed technology and scalability are important. For the scalability a multistage system is known as suitable, so an accurate analytical method[4] for a multistage system is proceeded, and a problem for nonuniform bursty traffic[5] is treated.

For a large scale switching system, hardware complexity reduction technology of a switch is important because a large number of switches are used in the system. Though various types of ATM switch were demonstrated, a shared buffer switch type is known as a switch requiring a relatively small buffer size. For the reason, a shared buffer switch[6] is useful for a totally system hardware reduction, and a fabrication of an improved shared multibuffer[7] switch was reported. Furthermore, a shared buffer switch with multicasting[8], a queue manager chip for control[9] of a switch, and performance analysis for nonuniform traffic[10] were reported

On the other hand, ATM switch with 10 Gbits/s serial ports[11] was demonstrated, and it is considered that ultra high speed technology more than 10 Gbits/s is desired for future B-ISDN. For such sub nsec high speed switching, synchronization is a difficult problem[12]. Indeed 30 mm deference in linking wire length on a multistage system VLSI chip gives more than 100 psec delay deference, and a length nonuniformity of links can not be easily dissolved because a circuit is usually limited in 2 dimensions with high density. Therefore some synchronization countermeasure has to be introduced to cover a design difficulty of a multistage switching system VLSI.

A prototype shared buffer switch is known as unsuitable for high speed transferring because high-speed write-in and read-out on the switch are difficult. Therefore a shared buffer switch based on a parallel read-out[13] and write-in structure is presented in this paper for speed-up. Single Synchronization (SS) simultaneous write-in switch can be used in a low speed switching system, however, it is difficult to be used for ultra high-speed switching. Therefore a Multi-Synchronization (MS) write-in shared buffer switch architecture which is free from a timing delay on a link is newly introduced to dissolve the synchronization difficulty.

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2 MULTI SYNCHRONIZATION SHARED BUFFER SWITCH

From a view point of scalability of switching system, a buffered multistage system is suitable and can be used for ATM switching systems. A model for the system is depicted in Fig.1. Though various types of switch elements are applicable for the multistage switching system, an application of shared buffer switches is considered. All circuits in switch elements for conventional low speed ATM can be synchronized with a single clock, so write-in and read-out operations are done simultaneously with a single clock in the system. Such the write-in operation is called a single synchronization (SS) write-in procedure in this paper.

An idealized model of a shared buffer switch employing an SS write-in architecture is shown in Fig.2. For the switch, parallel write-in and parallel read-out based on matrix gate connections are employed for speed-up of transferring. In the ideal model, direct paths are implemented, so an incoming cell can transferred to its destination through the direct paths when no cell toward the same destination of the incoming cell exists in buffers. Because all circuits operate with a single clock CLK_0 in the switch, simultaneous write-in and read-out operations are possible.

The symbols ○ and △ mean write-in permitted and inhibited states of buffers respectively. A cell arriving to the switch can be write-in to one of free buffers or one of buffers from which cells are read-out. The switch architecture offer efficient queueing performance, and realization of a SS simultaneous write-in architecture is not difficult for a low speed switching system, however, it becomes difficult for a ultra high speed switching system.

As shown in Fig.1, many interstage links must be spanned between switches of neighboring two stages, and the lengths of the links are forced to be different each other in a conventional 2 dimensional VLSI circuit design. In such the architecture, arrival times of cells to switches at the latter stage (from switches at the former stage) are mutually deferent. To synchronize the arrival times to a single clock, some delay circuits have to be implemented on the links. Synchronization of the pulses with various delays can be adjusted by fixed delay circuits because the delay times are basically invariant if jitters are excluded. Synchronization by such the delay circuits becomes difficult with increasing of switching speed.

To dissolve the synchronization difficulty, a new shared buffer switch employing a multi-synchronization (MS) write-in architecture shown in Fig.3 is presented. In the switch, write-in operations are done with individual write-in clocks CLK_1, CLK_2, ... CLK_4. Hence clocks for write-in are not synchronized with read-out clock CLK_0, and direct paths which is permitted for only an ideal switch can not be used. In the model, an arriving cell to the switch can be write-in only to one of free buffers indicated by ○ and can not be write-in to any of occupied buffers indicated by △.

Therefore the MS write-in switch degraded queueing performance by the above limitations. Hence an additional buffer size increment is required for the practical MS switch to obtain a performance with a same level to the ideal SS switch.

3 SIMULATION

For the simulation to evaluate a buffer size, it is assumed that an arrival process of a cell is represented by constant time interarrival with an independent arrival probability of ρ. The arrival probability ρ is also regarded as traffic load per incoming line measured in erlang, and takes 1 as a maximum value. All traffic loads to all incoming lines are assumed to be steady and mutually equal, namely uniform traffic is assumed.

As the performance evaluation factors, a cell loss probability and an average waiting time are important, so the both factors have been mainly obtained by the computer simulation. Fig.4 shows cell loss characteristics of the switch where ρ is taken to be 0.6. In the figure a horizontal axis is a total buffer size for a shared buffer switch, and a vertical axis is a cell loss probability. Solid line curves are cell loss probabilities of MS switches of sizes of 2, 4, 8, 16, and 32. Broken line curves are cell loss probabilities of SS switches, and are presented to compare the practical MS switch to the ideal SS switch.

The curves of MS start from a point of the value 1.0 at a buffer size 1. This means that any cell can not be transferred without using a register. On the other hand, the curves of SS start from 0 at the buffer size 0. This property is explained by the fact that transferring through direct paths is performed in SS switch with no buffer.

It is seen from Fig.4 that MS switch necessary about 2 times of buffer size for SS switch. Curves of N=32 shows that 80 of a buffer size is necessary to guarantee 10^{-08} of a cell loss probability for MS switch though only 40 is necessary for SS.

Fig.5 show cell loss characteristics where ρ=0.8. The figure also shows the similar characteristics seen in Fig.4, and curves of MS and SS start from points of 1 slot time and lower than 1 respectively. The value of 0.8 for ρ is regarded as reasonable load because it is not so heavy and not so light.

Fig.6, 7, and 8 show characteristics of waiting times of MS and SS switches in cases of ρ=0.6, 0.8, and 0.95. In the figures, the horizontal axes are a buffer size and the vertical axes are a waiting time. The curves of solid line and broken line indicate waiting time characteristics of MS and SS switches respectively. The waiting times for MS take larger values than that of SS as general tendency. As Fig.6 shows, all the curves of MS start from a point of 1 slot time at neighbor of the waiting time axis though the curves of SS start from 0. The property that the all curves of MS take 1 at buffer size 1 is caused by a fact that an arriving cell in MS switch must stay a time just equal to transfer time of itself. As general tendency, it is seen that the curves of both groups of MS and SS take saturation values at large buffer area, and the curves of MS take larger values than SS.

Fig.7 also shows all the curves indicate saturation tendency. As an interest property, crossing of both curves of MS and SS is seen for a case of N=32. The property is discussed later in relation to characteristics of curves in Fig.8.

It is considered that Fig.8 corresponds to a case of heavy traffic and shows the waiting time of MS is shorter than SS for same N, and the tendency is similar to the characteristics shown in the above two figures.

Remarkable property seen in Fig.7 and 8 is a fact that both the curves of MS and SS for N=32 in Fig.8 and for all the switch sizes in Fig.8 cross mutually. The cause of the crossing can be understood from the loss curves in Fig.5 corresponding to the above waiting times. At the buffer size area of the crossing, the loss probability of MS takes significantly large value around 0.1. Namely all the buffers implemented to MS switch are not used efficiently. The inefficiency, which is seen normally in a conventional switch, is caused by a lack of the direct paths and the simultaneous write-in and read-out architecture. Hence it can be resulted that a necessary buffer size for MS switch is equivalent level to a practically used switch.

4 CONCLUSION

A shared buffer switch for a multistage system based on a multi-synchronization write-in architecture is presented to cover the VLSI clock timing difficulty. The multi-synchronization architecture is useful for a practical design to implement a sub nsec switching system on VLSI in which wiring is limited in 2 dimensions and same length interstage linking of switch elements is difficult. The simulation results show that a practically reasonable size increment only is necessary for the switch to ensure a same level with a performance of an ideal switch.

REFERENCES

[1] M. J. Karol, M. G. Hluchyj, and S. P. Morgan "Input Versus Output Queueing on a Space Division Packet Switch" *IEEE Trans. Commun*., vol.COM-35, no.12, pp.1347-1356, 1987.

[2] N. Yamanaka, K. Endo, K. Genda, H. Fukuda, T. Kishimoto, and S. Sasaki "320Gb/s High-Speed ATM Switching System Hardware Technologies Based on Copper-Polyimide MCM" *IEEE Trans. Component, Package. and Manufacture. Technol.-Part B*, vol.18, no.18, pp.83-91, 1995.

[3] M. Tsukada and H. Nakano "Ultrafast Photonic ATM (ULPHA) Switch and a Video Distribution Experiment" *IEEE J. Lightwave Technol*., vol.14, no.10, pp.2154-2161, 1996.

[4] B. Zhou and M. Atiquzzaman "Performance Study of Multistage ATM Switches Using an Accurate Model of the Behavior of Blocked Cells" *IEICE Trans. Commun*., vol.E79-B, no.11, pp.1641-1635, 1996.

[5] B. R. Collier and H. S. Kim "Performance of Multistage ATM Switch Architectures under Nonuniform Bursty Traffic" *Proc. IEEE INFOCOM'95*, pp.667-674, 1995.

[6] T. Kozaki, N. Endo, Y. Sakurai, O, Matsubara, M. Mizukami, and K. Asano "32×32 Shared Buffer Type ATM Switch VLSI's for B-ISDN's" *IEEE J. Selected Area Commun*., vol.9, no.8, pp.1239-1247, 1991.

[7] H. Yamanaka, H. Saito, H. Yamada, H. Kondoh, H. Notani, Y. Matsuda, and K. Oshima "Shared Multibuffer ATM Switches with Hierarchical Queueing and Multicast Functions" *IEICE Trans. Commun*., vol.E79-B, no.8, pp.1109-1120.

[8] J. Wu and C. Ke "ATM Shared Memory Switch with Multicasting Balancing" *IEICE Trans. Commun*., vol.E78-B, no.9, pp.1262-1268, 1996.

[9] Y. Lin, H. Huang, and C. B. Shung "A Queue Manager Chip for Shared Buffer ATM Switches" *IEICE Trans. Commun*., vol.E79-B, no.11, pp.1623-1631, 1996.

[10] E. Valdimarsson "Queueing Analysis for Shared Buffer Switching Networks for Non-Uniform Traffic" *IEEE INFOCOM'95*, pp.8-15, 1995.

[11] S. Hino, M. Togashi, and K. Yamasaki "Asynchronous Transfer Mode Switching LSI Chips with 10-Gb/s Serial I/O Ports" *IEEE J. Solid-State Circuit*., vol.30, no.4, pp.348-352, 1995.

[12] R. C. Lau and P. E. Fleischer "Synchronous Techniques for Timing Recovery in BISDN" *IEEE Trans. Commun*., vol.43, no.2/3/4, pp.1810-1818, 1995.

[13] C. Fujihashi and H. Hikita "Speed-Up of Input Buffer Asynchronous Transfer Mode Switch by Introducing of Parallel Read-Out Structure" *IEEE Golbecom'96*, vol.2, no.21-1, pp.819-824, 1996.

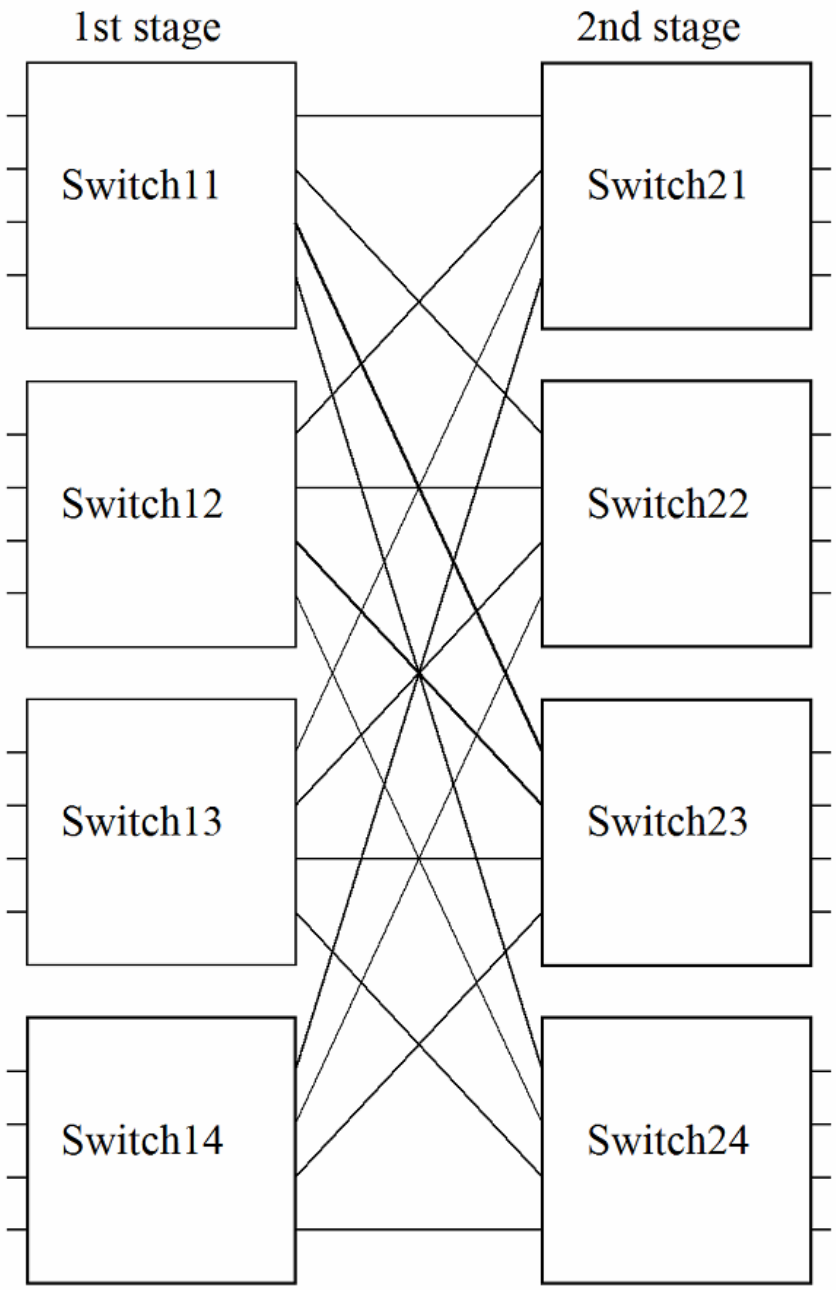

Fig.1 Multi(two)-Stage switching system and interstage links of various lengths.

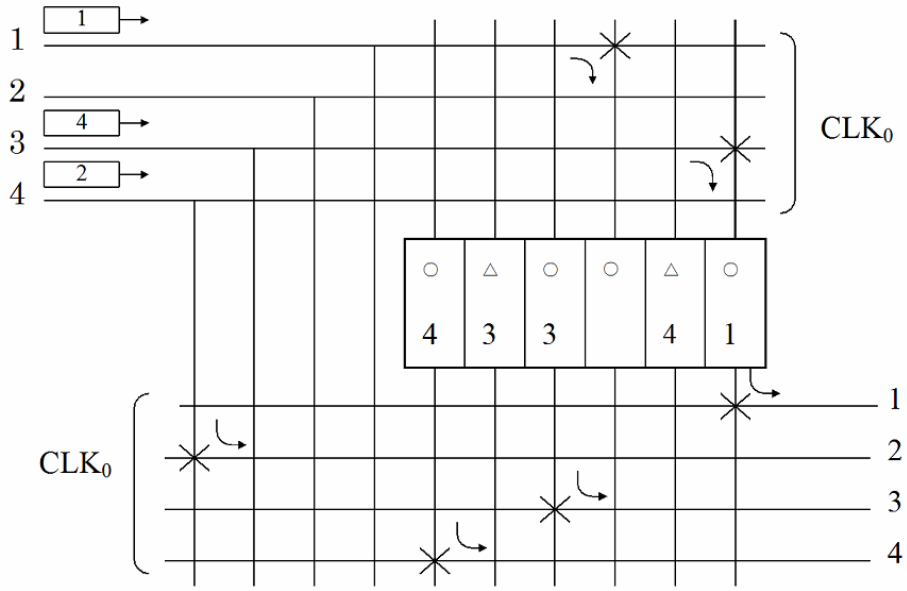

Fig.2 Shared buffer switch structure based on single synchronization simultaneous write-in procedure including direct paths and simultaneous write-in read-out function.○:write-in permitted. △:write-in inhibited.

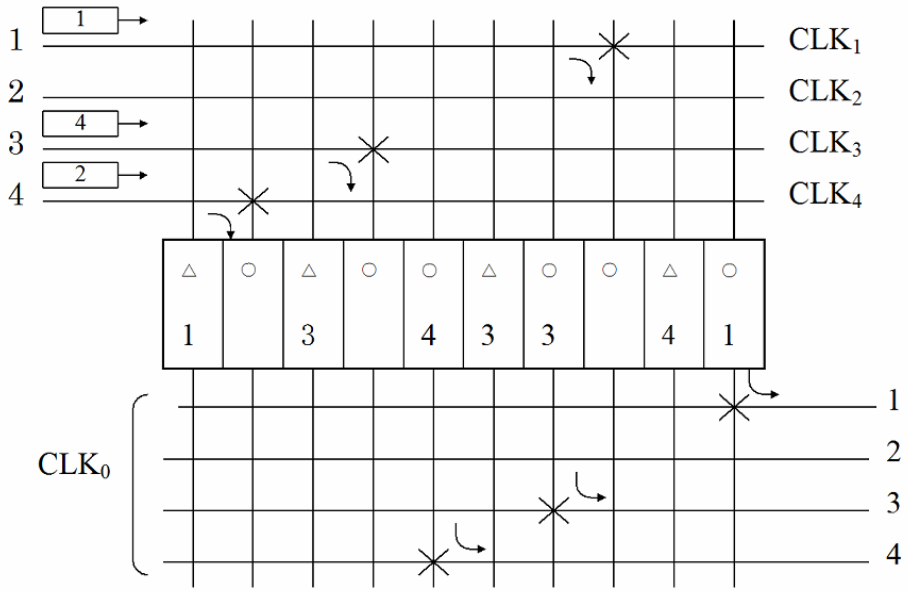

Fig.3 Shared buffer switch structure based on multi-synchronization individual write-in procedure. ○:write-in permitted. △:write-in inhibited.

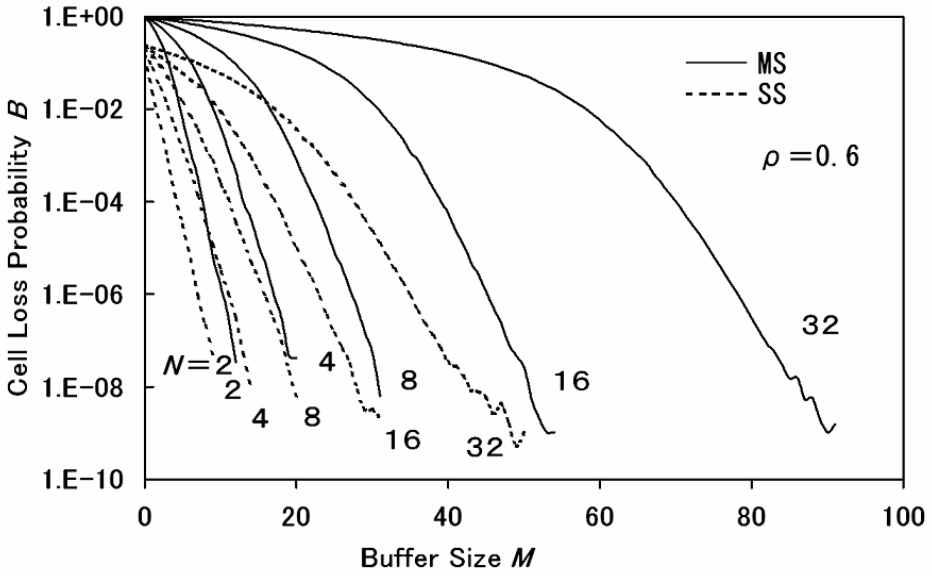

Fig.4 Cell loss probabilities of multi-synchronization (MS) and single synchronization (SS) switches where ρ=0.6.

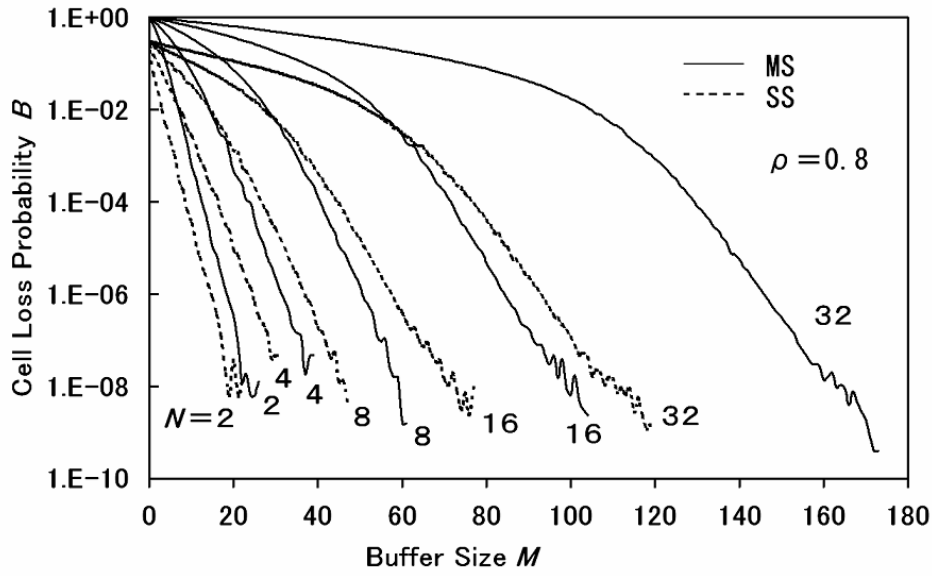

Fig.5 Cell loss probabilities of MS and SS switches where ρ=0.8.

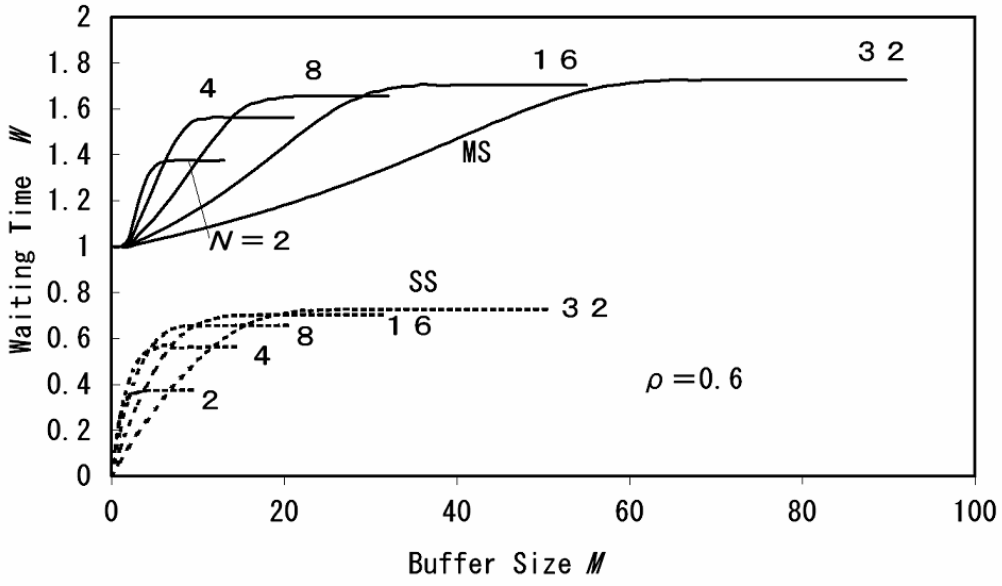

Fig.6 Waiting times of MS and SS switches where ρ=0.6.

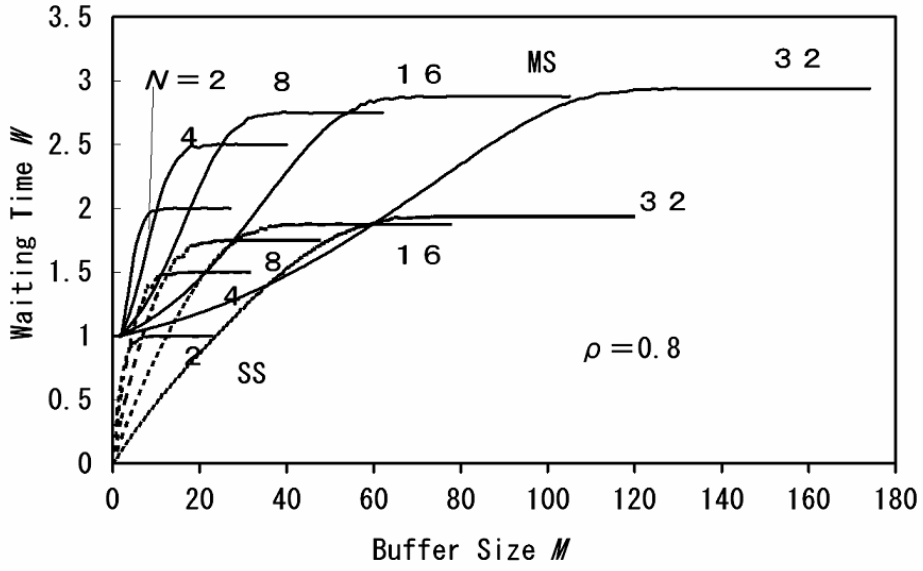

Fig.7 Waiting times of MS and SS switches where ρ=0.8.

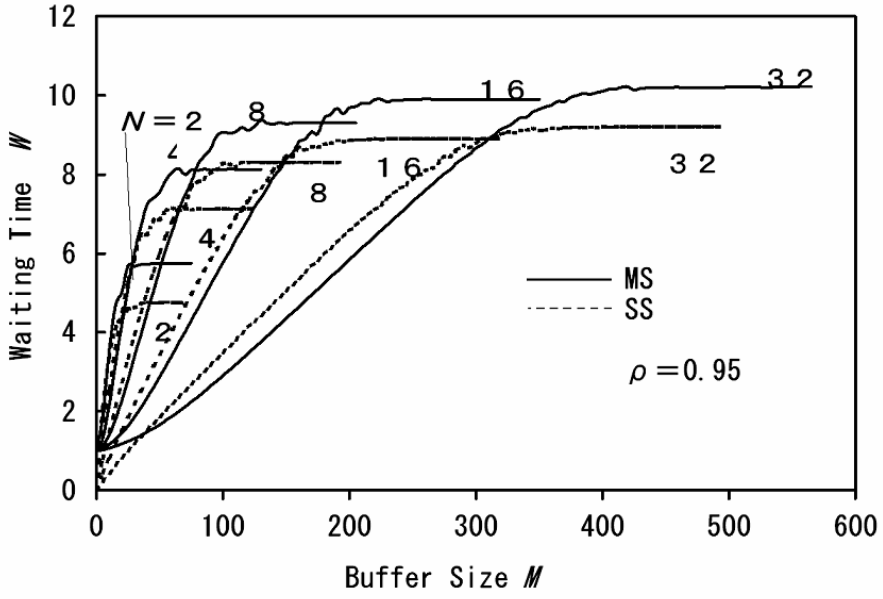

Fig.8 Waiting times of MS and SS switches where ρ=0.95.

Captions

Fig.1 Multi(two)-Stage switching system and interstage links of various lengths.

Fig.2 Shared buffer switch structure based on single synchronization simultaneous write-in procedure including direct paths and simultaneous write-in read-out function.○:write-in permitted. △:write-in inhibited.

Fig.3 Shared buffer switch structure based on multi-synchronization individual write-in procedure. ○:write-in permitted. △:write-in inhibited.

Fig.4 Cell loss probabilities of multi-synchronization (MS) and single synchronization (SS) switches where ρ=0.6.

Fig.5 Cell loss probabilities of MS and SS switches where ρ=0.8.

Fig.6 Waiting times of MS and SS switches where ρ=0.6.

Fig.7 Waiting times of MS and SS switches where ρ=0.8.

Fig.8 Waiting times of MS and SS switches where ρ=0.95.