Parallel Read-Out High-Speed Input Buffer ATM Switch Architectures

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The prototype first in first out (FIFO) input buffer asynchronous transfer mode (ATM) switch is known as the architecture on which the transfer capacity is considerably limited, and is necessary to be given some improvement. In this paper, a novel parallel read-out structure is introduced to the input buffer ATM switch design to remove such the above limitation. Transfer performances of cell traffics on the novel switch with the three control rules of a cyclic read-out (CRO) cell selection, a parallel read-out random (PROR) cell selection, and a parallel read-out maximum (PROM) queue selection are evaluated by simulations. The simulation results show that the introduced parallel read-out structure gives a drastic buffer size reduction. Especially, PROR and PROM architectures totally offer large amounts of hardware reductions though small hardware increments may be required for paralleling. Consequently it is shown that PROR and PROM input buffer switches give loss performances lower than that of the corresponding output buffer switches with the same level transfer delays.

1 INTRODUCTION

Asynchronous transfer mode (ATM) type packet communication is appropriate for effective utilizing of transmission line and high speed switching, and is regarded as indispensable technology for the achievement of an advanced future broadband digital network. The development of ATM switching system becomes a cornerstone for next age communications, and is actively researched from various points of views in resent years. The most important factor for the achievement of the switching system depends on performances of switch elements. The architectures researched until today are basically classified into four types of input, output, cross point, and shared buffer switches.

Among them the input and the output buffer switches are fundamental, and they have been researched since the beginning of ATM development, and is pointed out that there is considerable limit to transfer capacity on the prototype input buffer switch[1][2]. Performance of the switches and optimum design methods for them, however, are not known in detail. For the problems, the report[3] on analysis of nonuniform traffic characteristics on knockout switch that is one of improved architectures of output switches, and the report[4] on an analysis of transfer capacity limit on the input switch are given. Thus the transfer capacity limit appears on the conventional input buffer ATM switch, so that some appropriate improvement have to be given for the input type switch design for speed-up.

For the improvements, the approaches by internal speed-up[5][6], by grouping[7][8], and by the algorithm based on the cell selection for the all cells including not only first cells at heads of lines but also later waiting cells[9] are presented. The internal speed-up, however, may give a restriction for ultimate high-speed design for advanced future ultra broadband communication. The grouping is useful, however, is conceptually an improving method to modify an input buffer structure closing to a shared buffer switch type, and the algorithm in considering with also later waiting cells has difficulty for further high speed

control because of control program complexity. As examples for high speed communication, 100 Gbits/s optical transmission gate device[11] are reported. Hence further speed-up technology must be researched for the advanced future ultra high speed switching system covering such the transmission band widening.

For the above reasons, it is necessary to find out some switch architecture removing the transfer capacity limit and being based on the structure which is able to meet speed-up demanding. Then an input buffer switch newly adopting the parallel read-out structure is presented in this paper. Because the structure can remove the transfer capacity limit appearing on the conventional input buffer switches due to no cell transferring caused by selection contention, large improvement in switching speed is expected. The structure can be applied for a presently being developed electronic integrated circuit switch[12], an optical switch[13], and a superconduction switch[14]. For buffer circuits in the architecture, shift registers in which destinations of cells are directly read-out[15] are applied. The combination of direct and parallel read-out technologies allows high speed transferring.

In chapter 2, architectures on parallel read-out input buffer ATM switch with various cell selection rules are introduced. The traffic simulations to evaluate the switch performances are treated in chapter3 and discussions on the performances are given in chapter 4.

2   PARALLEL READ-OUT STRUCTURE and CELL TRANSFER CONTROL

The architectures of considering switches with various cell selection rules are discussed in this chapter. Fig.1 shows the most conventional first in first out (FIFO) head of line selection input buffer ATM switch. The architecture is known as the prototype for the input buffer switch, and is picked out to compare the performance with that of the novel switches later presented in this chapter. As shown in Fig.1, because only one cross point is allowed for connecting of a read-out line and an output line, only one cell can be transferred from an input buffer. Furthermore the cell selection is allowed on the head of line rule, the degrees of selection freedom is restricted and then transferring on the architecture may be inefficient.

Fig.2 shows the novel input buffer switch introducing the parallel read-out structure in the case of switch size N=4. The switch is consisted of N input buffers with parallel read-out lines and a parallel input transfer switch. As shown in Fig.2, a set of N read-out lines (a read-out line is prepared for each on N output lines) is implemented for each of the input buffers, and multiple cross points can be connected for a set of read-out lines, then the degrees of cell selection freedom is largely expanded. In the architecture, the read-out lines implemented for paralleling are taken to be N and is equal to the switch size. Then, even so all the cells are concentrated to a particular buffer as the worst case, if the cells have two or more different destinations, two or more cells can be transferred from the buffer. Hence if there is one or are more cells toward an output line in the switch, one cell can be always transferred to the output line.

Let three control rules of a cyclic read-out (CRO) cell selection, a parallel read-out random (PROR) cell selection, and a parallel read-out maximum (PROM) queue selection for transfer control be applied to the above introduced switch. CRO is the cell selection rule in which one cross point connecting on a read-out line is allowed and closing patterns in the transfer switch are taken in the cyclic process as shown in Fig.3. In the cycle, the diagonal cross points are connected at first step, and the cyclic next cross points of the first connected cross points are connected at second step, and the corresponding cross points are connected at each of the third and fourth steps.
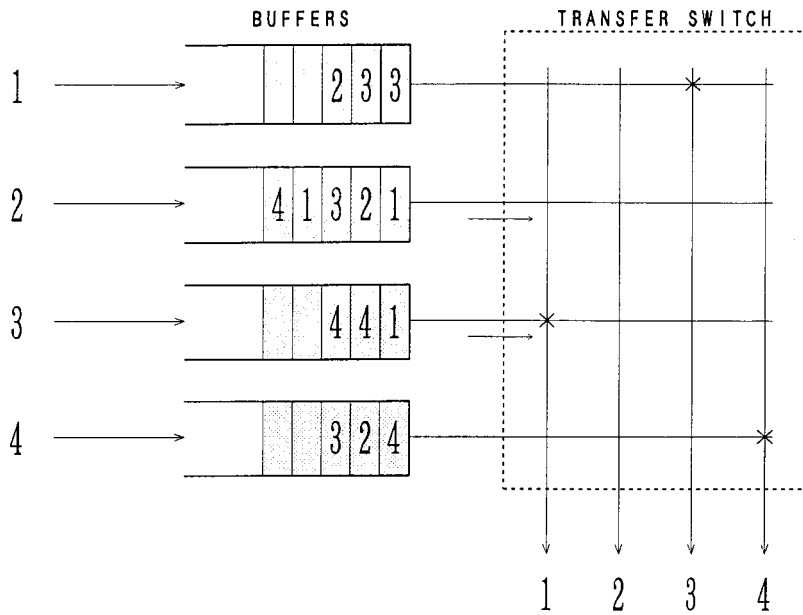
Fig.1   A conventional FIFO head of line selection input buffer switch architecture (*N*=4).
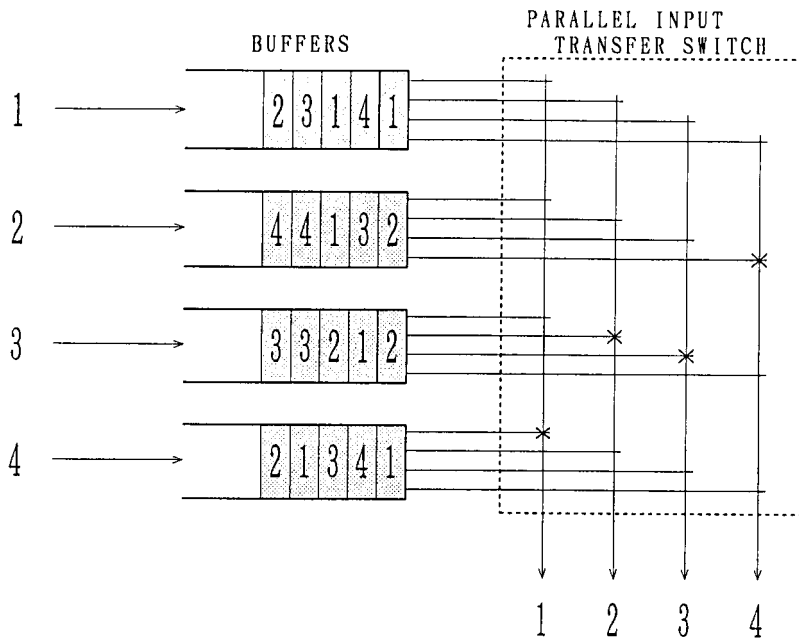   (×   A connected cross point)

Fig.2   The parallel read-out input buffer switch architecture (*N*=4) consisting of the parallel
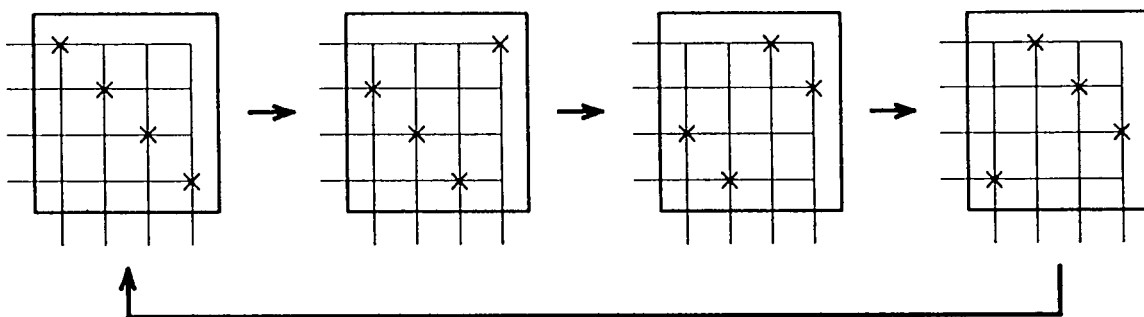   input transfer switch and the parallel read-out buffers.

Fig.3   The closing patterns in the cyclic read-out (CRO) on the cross points of the parallel input
         transfer switch.   A set of multiple lines for a parallel input is represented by one line.

From the input buffer connected to an output line through an read-out line closed at the cross point in CRO selection rule, one of the cells toward the output line is selected and transferred if there are one or more cells in the buffer. If there is no cell toward the output line in the buffer, no cell is transferred. If the no cell transferring events frequently occurs, the events lead to an inefficient factor. The events may frequently occur in light load case where a small number of cells are found in the buffer, however, the events may rarely occur in a heavy load case. Hence the cell selection rule may be useful at heavy load case for removing of the transfer capacity limit.

In PROR and PROM cell selection rules, one of all the cells toward a same destination in all the buffers if there are is selected and transferred. A remarkable benefit of the parallel read-out (PRO) is on the permission of multiple cross point connecting for an input buffer. Then multiple cells (N in maximum) can be read-out in parallel and simultaneously transferred to the corresponding different output lines. Hence, in the two selection rules of PRO, whenever there are one or more cells toward any of the destinations from any of the buffers, one of the cells can be transferred to output line of the destination. Thus there is no contention in the cell selection rules of PRO, then the transfer capacity limit seen in the prototype is removed and then the transfer efficiency must be improved.

The different point between PROR and PROM as cell selection rules is as follows. In PROR, any of the cells having the same destination and existing in all the buffers is selected in random manner with the same probability. On the other hand, in PROM one cell is selected from the maximum one of the queues formed in the buffers by cells having a same destination. Hence PROM is an active procedure aiming large improvement, and PROR is procedure with no idea in cell selection while transfer speed improvement by paralleling is used.

The structure of the parallel read-out input buffer switch is shown in Fig.4 and is drawn as an example for the read-out line number of 4. The buffer is consisted of a cell unit and the unit is based on a shift register. The read-out line is given for each of the units, and the units putted numbers at lower ends are cell storing units, and the numbers are destinations of the stored cells. The read-out lines are going to each of output lines, and then small hardware increment is necessary for the matrix switch and the parallel read-out lines. Then it is the problem that total hardware reduction overwhelming the above hardware increment is possible or not by the buffer size reduction due to transfer speed improvement based on the paralleling.
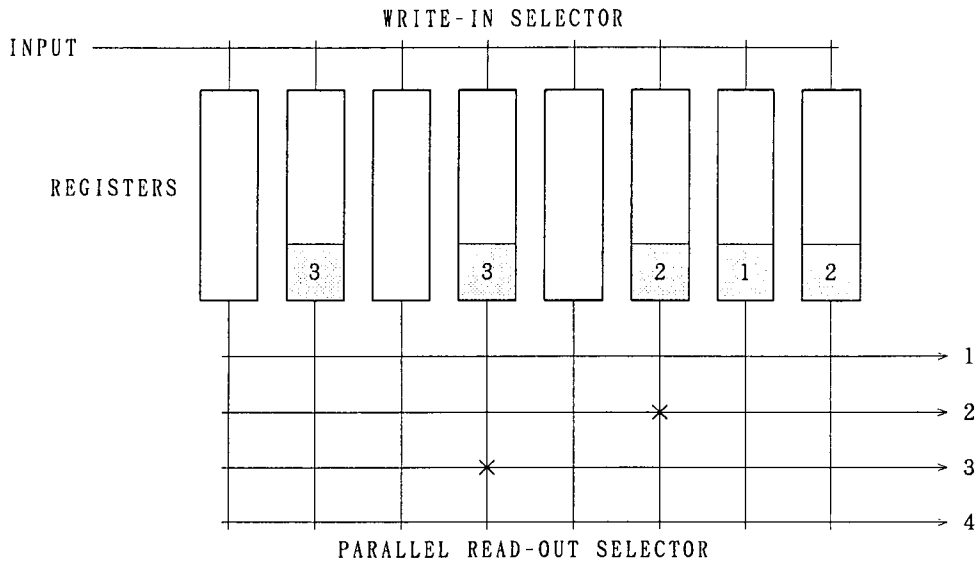
Fig.4   The parallel read-out input buffer structure consisting of the registers, the write-in
        selector, the parallel read-out selector.

        Because a shift register is applied to the unit of buffer, a destination of a stored cell can be
directly read. Then some other equipment like an address queue for cell destination read-out is not
necessary, and a read-out control is done in parallel by using the direct read-out of a destination data. A
circuit implementation quantity for the control in parallel may increases, however, complexity of the
control algorithm conceptually may be simplified.

3   SIMULATION

        In the previous chapter, the three novel input buffer ATM switch architectures are presented. To
evaluate the performances of the switches, computer simulations had been done. As conditions for the
simulations, it is assumed that an arrival process of a cell to an input buffer is random with a constant
arrival rate   (an appearing probability of a cell in a time slot) and process for all the input buffers are
equivalent. Furthermore all of the transfer rates on an input line, on a read-out line, and on an output line
are taken to be equal.
        A transfer capacity often is used as a performance measure, however, it is generally obtained as
an asymptotic value when infinite number is taken for a buffer size. Then the transfer capacity is not
appropriate as the performance measure for practical design where a finite buffer size only is allowed. On a
relation to the finiteness of buffer size, the most important performance measure is a cell loss probability.
Then the cell loss probability characteristics in the presented switches are evaluated by simulation. A
transfer delay also is important, and the waiting time characteristics in the switches are evaluated. Thus the
switches of 4 types FIFO, CRO, PROR, and PROM had been simulated and compared with the
corresponding characteristics of the output buffer switch.
        Fig.5 shows the cell loss probability dependency on the number of buffer size per line on the
FIFO input buffer switch. The vertical and horizontal axes are taken for the cell loss probability and the

buffer size respectively. Curves of the solid lines are resulted from the simulation for the input buffer switch and of the broken lines are resulted from the numerical computation[1] for the output buffer switch. All curves are plotted under the parameter of the number of switch size N, and the curves of small size switches take losses lower than that of thelarge switch. The load per line is taken to be 0.8, namely 0.8 for the arrival rate are taken, and the same load is taken for all the figures in the following discussions. Although the broken line curves have a tendency of decreasing with increasing of the buffer size, the solid line curves have no decreasing tendency and are staying on constant values in independent from the buffer size increasing. This is the characteristic based on the transfer capacity limit always appearing on such the conventional FIFO input buffer switch. The result shows that increasing of the buffer size can not reduce the loss of FIFO type, and then some counter measure have to be given.

Fig.6 shows the cell loss characteristics of CRO input buffer switch (solid line) in comparison with that of output switch (broken line). Decreasing tendency on the curves of CRO is seen, and is caused by removing of the transfer capacity limit due to avoiding of a cell selection contention. Thus the performance of CRO is improved to have the loss lower than the loss of FIFO, however, is not reached to have the loss lower than the loss of output buffer switch.

Fig.7 shows the cell loss characteristics of PROR input buffer switch (solid line) and that of the output buffer switch (broken line). It is shown that the solid line curves generally take values lower than the values of the broken line curves. The result means that the input buffer ATM switch can take the transfer capacity higher than that of the output buffer switch at the same finite buffer size. On the solid line curves, crossing property at around the buffer size 6 o 7 is seen. The property is caused by the fact that the degrees of selection freedom in combination of cell destinations is expanded by the number of switch size
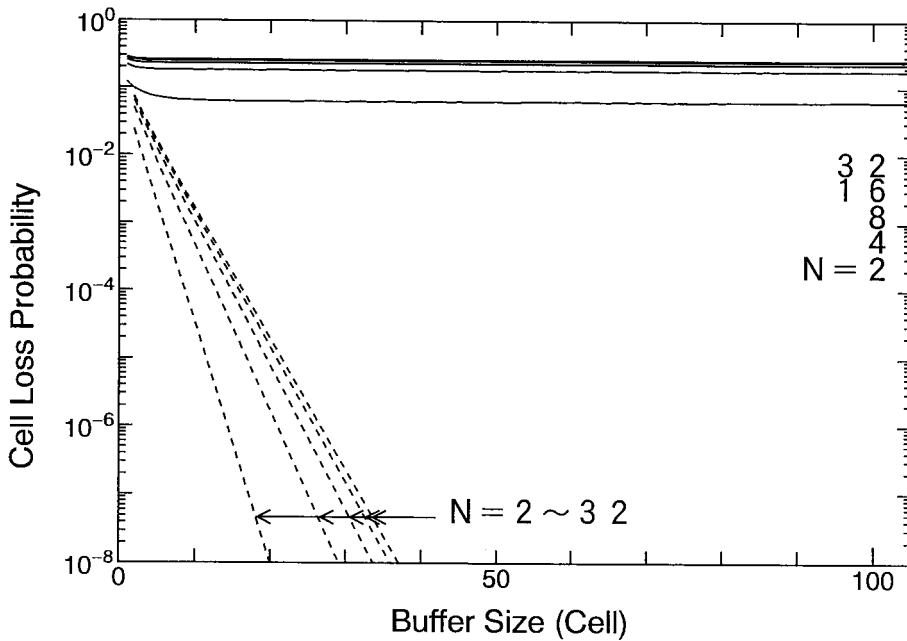

Fig.5   The cell loss of the FIFO head of line selection input buffer switch (solid line) in comparison with the cell loss of the corresponding output buffer switch (broken line).

N. Namely the property means that the number of inefficient cell destination combinations (where no cell exists to several output lines) increases in probability according to decreasing of the switch size.
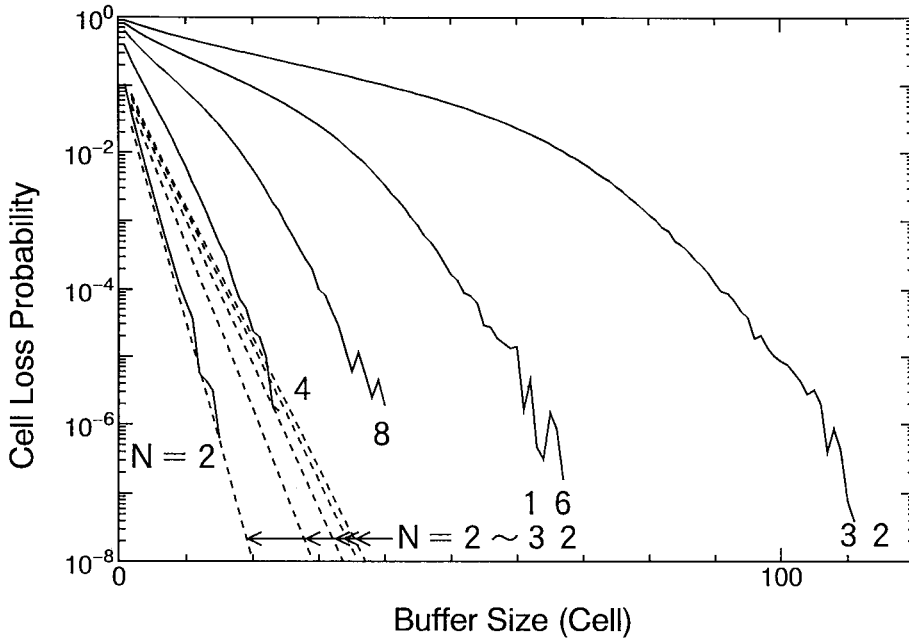

Fig.6 The cell loss of the CRO input buffer switch (solid line) and the loss of the output buffer switch (broken line).
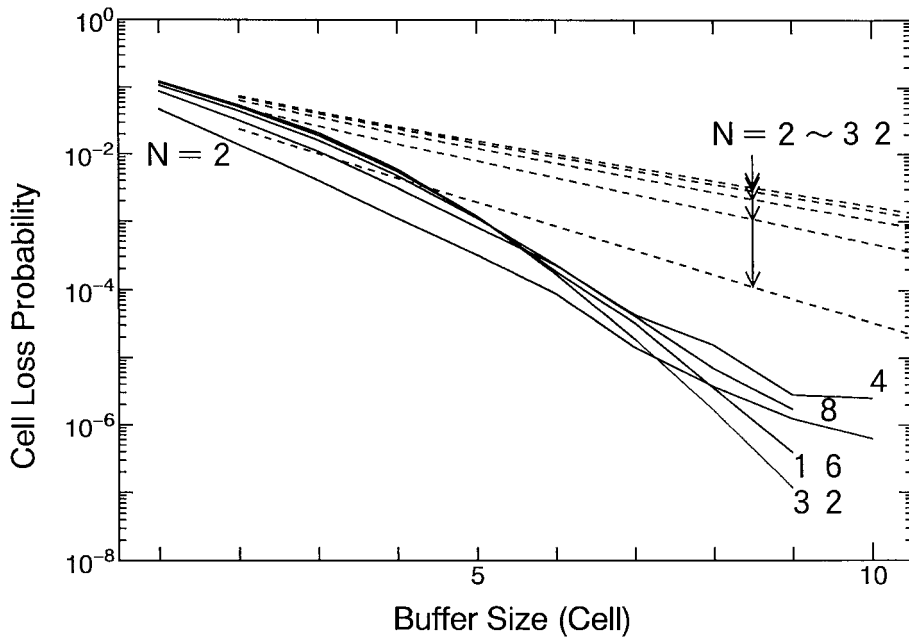

Fig.7 The cell loss of the PROR input buffer switch (solid line) and the loss of the output buffer switch (broken line).

Fig.8 shows the low loss characteristics of the input buffer switch of PROM. The high performance is achieved by the high efficiency of the cell selection rule that a cell of the maximum queue among the queues formed by the cells for the same destination in all the input buffers is selected. Thus the loss obtained at around the buffer size 9 in PROR can be achieved at around the size 7 in PROM.

Fig.9-12 show the waiting times in the input switches FIFO, CRO, PROR, and PROM. It is understood from Fig.9 that the waiting time in FIFO input buffer switch is extremely large and linearly growing up with increasing of the buffer size. On the other hand, CRO selection suppresses the waiting time considerably as shown in Fig.10. In Fig.11 and 12, the results for PROR and PPOM together show that the waiting times of the input buffer switches at relative large buffer size with low loss take waiting times similar to the values in the output buffer switch.
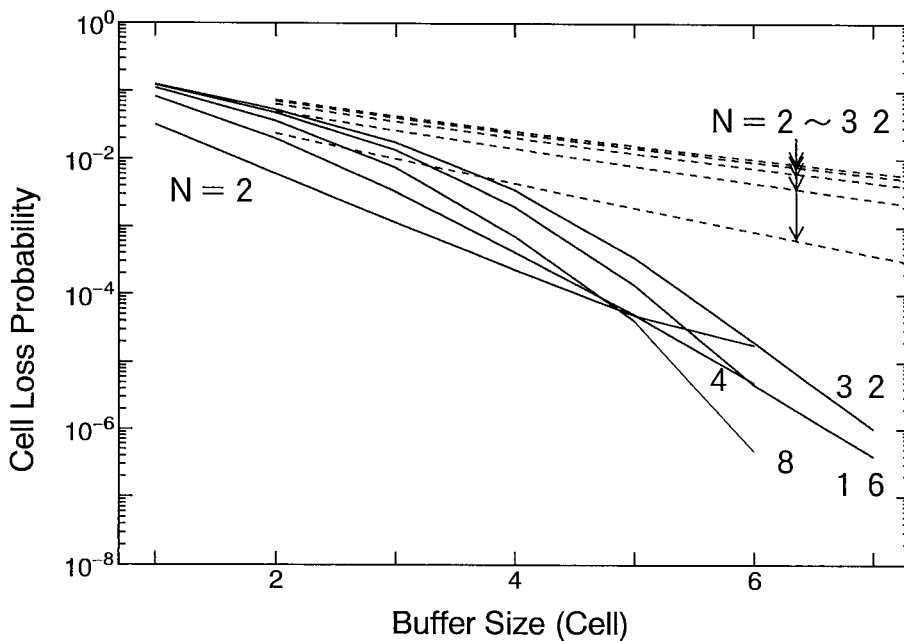

Fig.8   The cell loss of the PROM input buffer switch (solid line) and the loss of the output
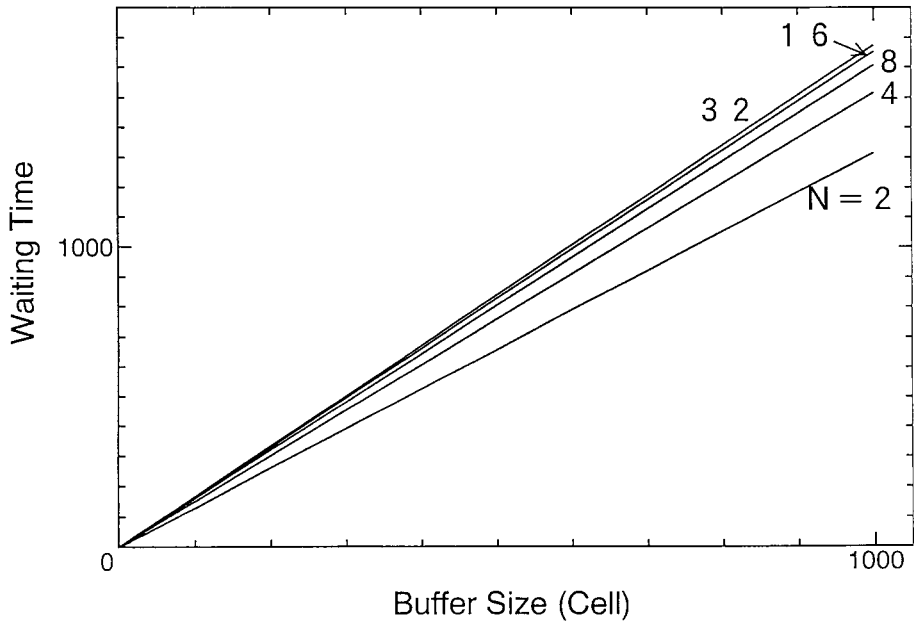   buffer switch (broken line).

Fig.9   The waiting time of the FIFO input buffer switch.   Because the waiting time is extremely
        larger than the waiting time of the output buffer switch, the latter time is omitted.
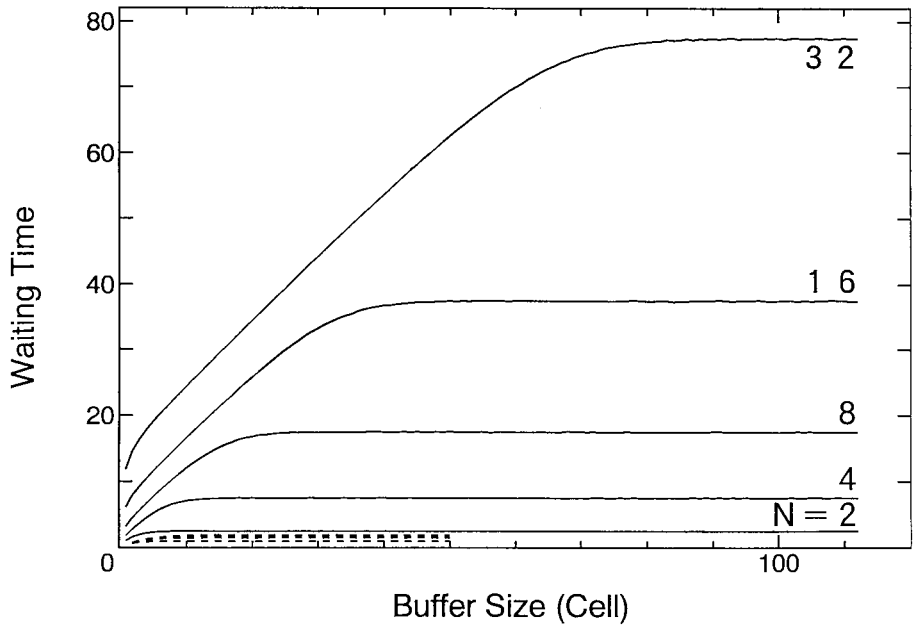
Fig.10 The waiting time of the CRO input buffer switch (solid line) in comparison with the waiting
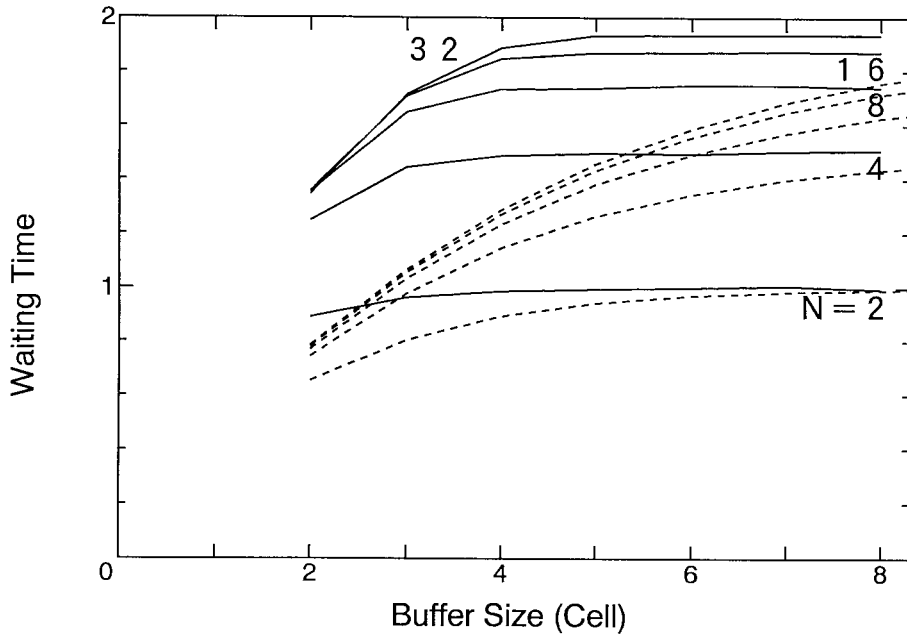   time of the corresponding output buffer switch (broken line).

Fig.11 The waiting time of the PROR input buffer switch (solid line) and the waiting time
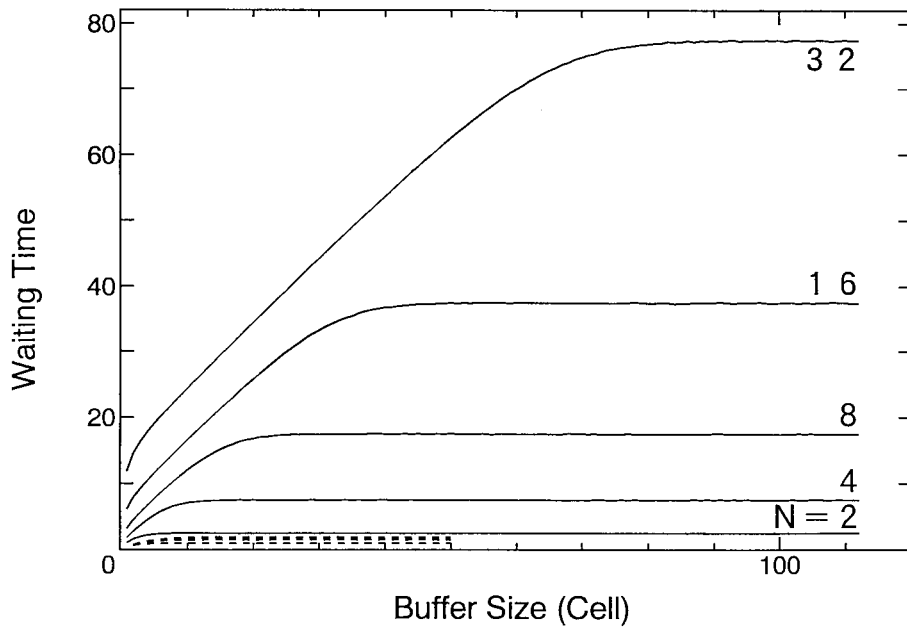of the output buffer switch (broken line).

Fig.12 The waiting time of the PROM input buffer switch (solid line) and the waiting time
of the output buffer switch (broken line).

4   DISCUSSIONS

The equivalency of both the waiting times of the input and the output switches seen in Fig.11 and 12 is due to that the transfer efficiencies of both the switches are intuitively equivalent for relative large buffer size with low loss, and then the result can be regarded as a proof for justification of an accuracy of the simulation. The fact that the cell loss probability of the input buffer switch takes the value smaller than that of the output buffer switch is based on that an arrival process to an input buffer is a single cell arrival while a batch arrival is for an output buffer.

5   CONCLUSION

To obtain a performance free from the transfer capacity limit seen at the conventional input buffer ATM switches, and to lighten a speed-up difficulty on a circuit design for an advanced future high speed switching system, the various parallel read-out input buffer switch architectures are presented. Performances of the presented architectures controlled by CRO, PROR, and PROM cell selection rules are evaluated from simulations. The simulations show that the introducing of the parallel read-out structure gives a large hardware reduction in total because a drastic decrement in terms of buffer size is obtained in spite of a small hardware increment is indebted for the paralleling. Consequently, it is resulted that loss of the novel input buffer switch takes the values lower than the loss of the output buffer switch where the delay of the both switches are kept to be almost equivalent.

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