Bulletin of Advanced Scientific Research 01 [04] (2015)
e-ISSN: 2454-3691
www.asdpub.com/index.php/basr

Original Article

Designing and analysis of gates based on adiabatic logic

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Keywords:
Power dissipation,
CMOS (Complimentary Metal-Oxide Semiconductor),
Adiabatic, Switching logic,
Inverter, NAND, NOR,
VLSI (Very Large Scale Integration),
LSI (Large Scale Integration),
LPHS (Low Power High Speed).

Abstract

Due to various advantages, CMOS are being widely used in designing of LSI (Large Scale Integration) & VLSI (Very Large Scale Integration).However there are some other sources present in CMOS which are responsible for the power dissemination that can be pigeonholed as follows: Dynamic Power Consumption, Short Circuit Currents, and Leakage Current. To reduce this power consumption another CMOS logic family called the adiabatic switching logic based on adiabatic switching principle. The adiabatic logic structure significantly decreases the power scattering. The switching technique puts forward a methodology to reuse the energy put away in the load capacitors as opposed to the conventional method which used to release the energy of capacitors into the ground and squandering this energy. Present paper discusses the standards of adiabatic logic, its arrangement and classification of different adiabatic logic circuits. An endeavor has been made in this paper to change 2PASCL (Two Phase adiabatic Static CMOS Logic) adiabatic logic circuit by replacing the MOS diode with simple PN diode which decreases the impact of Capacitances at high clock frequency.

1. Introduction

Power dissemination can be reduced by utilizing distinctive methods at diverse levels of deliberation of the IC configuration process. General methodologies for decreasing power utilization at circuit level are cutting down the force supply voltage, lessening switching action or diminishing load capacitance. An alternate methodology for reducing power dissemination at the circuit level is utilization of AC power supply for reusing vitality of hub capacitances. The standard is known as adiabatic which is taken from thermodynamics. Practically there are two classes of adiabatic switching logic circuits one is the fully adiabatic and other is semi adiabatic or partial adiabatic circuits. The loss of energy in adiabatic circuits can be primarily classified into two types: The first one is the adiabatic loss and another one is the non adiabatic loss. The former is caused by the switching resistance of the transistor during the time when current passes through the transistor. This is connected with the working frequency of the transistor. Thus In adiabatic switching, the increment of a transition time will lead to a less energy loss. Still the adiabatic loss cannot be neglected. The latter happens because of threshold voltage of the transistor. This loss is independent of the working frequency. It is characterised by the voltage drop, the hub capacitance and the falling time. Adiabatic switching which conceivably works as a reversible thermodynamic procedure, without loss or addition of energy. Adiabatic calculation meets expectations by rolling out little improvements in energy levels in circuits sufficiently moderate, in a perfect world bringing about no energy dissemination.[12]

2. Previous Work

In conventional CMOS logic we use constant voltage source to charge the load capacitance but in case of adiabatic logic switching circuits we use constant current source instead of constant voltage source. Figure 1 depicts clearly how this can be achieved with subsequent explanation. Here the load capacitance is charged by a constant current source. Here R is the resistance of PMOS network. A constant charging current resembles to a linear voltage ramp.[9,12]

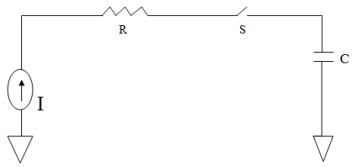

Figure1: Constant Current Source used for Adiabatic Logic Circuit

Dissipation in the switch	$P = I^2*R$	(1.1)
Energy during charging	$E = (I^2*R)*T$	(1.2)
Also,		
The voltage across the switch	$V = I*R$	(1.3)
	$Q = C_L*V_{dd}$	(1.4)
	$I = (C_L*V_{dd})/T$ (1.5)	
	$E= (I^2*R)*T = (R\,C_L) / T * C_L*V_{dd}^2$	(1.6)

Few observations can be made based on Equation (1.6) are as follows:[12]

i. The energy dissipated for adiabatic circuits is smaller if the charging time T is larger than $2RC_L$.

ii. Since, the dissipated energy is proportional to R thus reducing the on-resistance of the PMOS reduces the energy dissipation.

3. Circuit Simulations and Results

Above observations will be authenticated with the help of experimental & simulation results drawn by realising various gates on cadence VIRTUOSO software with 45nm technology. Schematic Designs & Simulation results are given below for the clear understanding of the use of adiabatic logic for the reduction in power requirement. A load capacitance of 1fF was connected at the output.

In the designed circuits two diodes are connected, one from the output node to the power clock supply and another from nMOS logic to another power clock. Both the diodes are used to re-cycle the charges from the output node. Also, Vdd is replaced by a positive sinusoidal waveform and Vss by a negative sinusoidal waveform because a

sinusoidal waveform gives lower energy dissipation as compared to other waveforms. Hence by using the above changes we can reduce the charging and discharging activities thus reducing the voltage difference.

Virtuoso Schematic Editor provides a complete design and constraint composition environment for front-to-back analog, custom-digital, RF, and mixed-signal designs. Virtuoso Analog Design Environment Provides a comprehensive array of capabilities for electrical and statistical analysis, verification, and optimization of analog/mixed-signal designs, including the interfaces to many industry-standard simulators. Virtuoso Visualization and Analysis is a waveform display and analysis tool that efficiently and thoroughly analyzes the performance of analog, RF, and mixed-signal designs.

A. NOT Gate or INVERTER

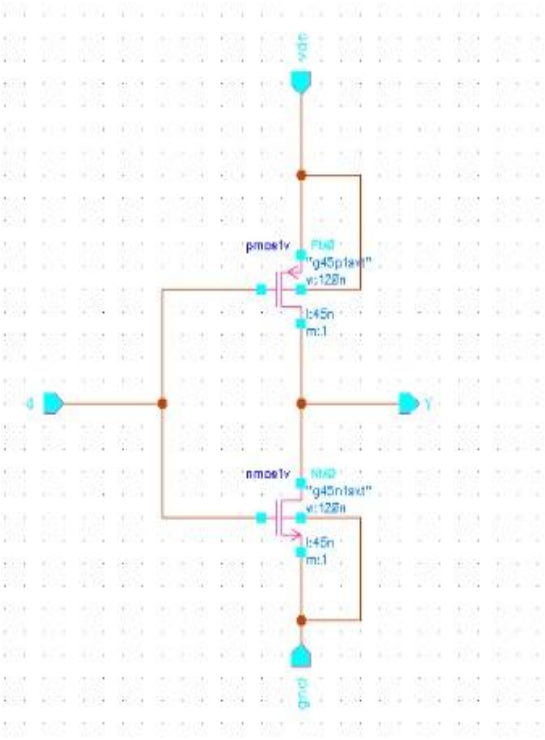

Figure 2: Inverter Schematic

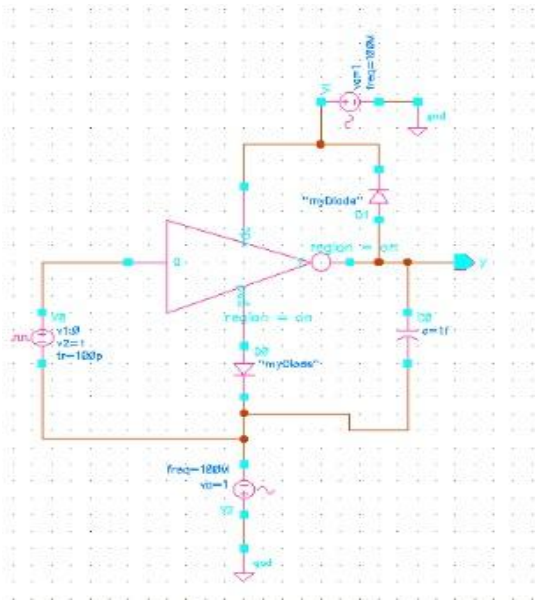

Figure 3: Inverter Testbench

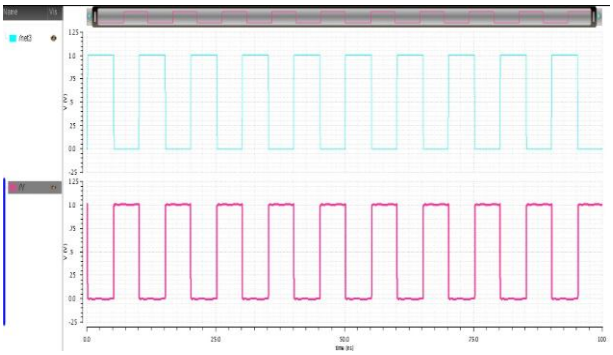

Figure 4: Inverter Waveform

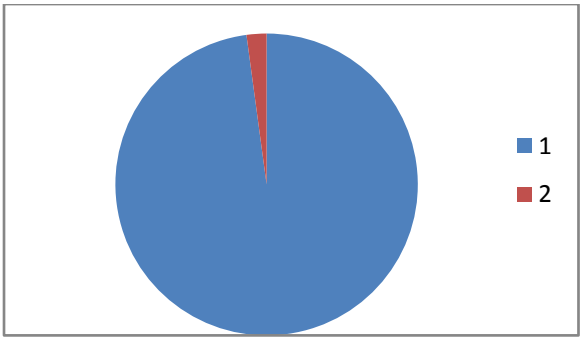

Figure 5: Power Dissipation in 1) CMOS & 2) LPHS Inverter

Following Facts are concluded from simulations of Inverter

1. The power dissipated in CMOS Inverter is **489.9E-3**
2. The power dissipated in designed Circuit is **10.67E-3.**

B. NAND Gate

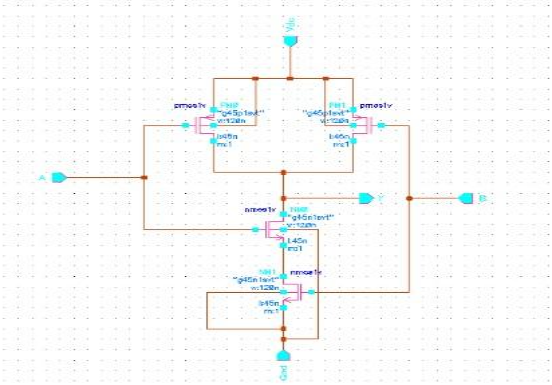

Figure 6: NAND Schematic

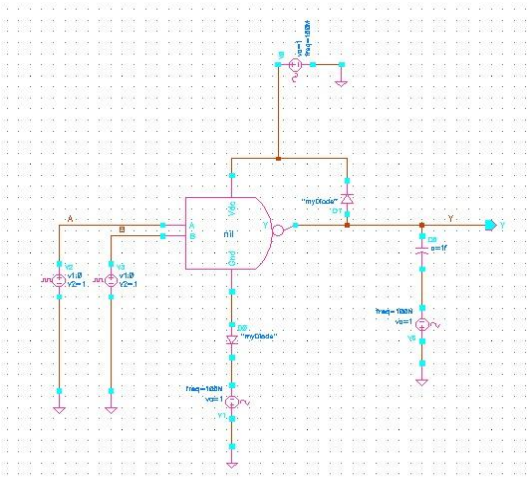

Figure 7: NAND Test bench

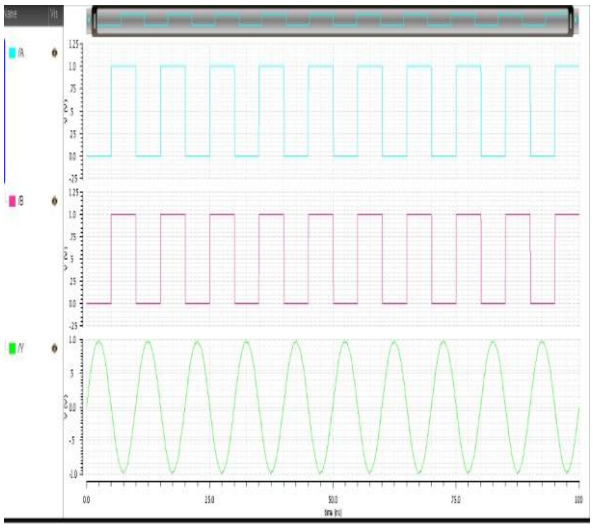

Figure 8: NAND Waveform

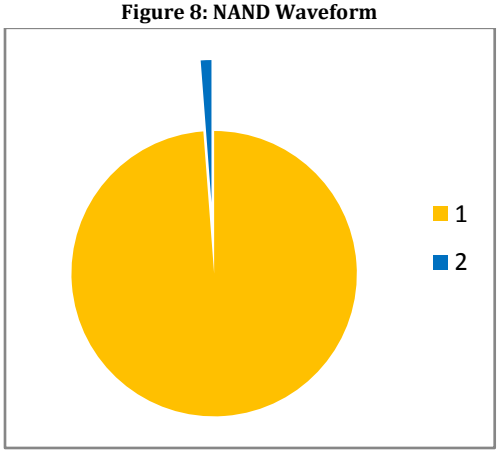

Figure 9: Power Dissipation in 1) CMOS & 2) LPHS NAND Gate

Following Facts are concluded from simulations of NAND Gate

1. The power dissipated in CMOS NAND gate is **493.3E-3**
2. The power dissipated in designed Circuit is **6.026E-3.**

C. NOR Gate

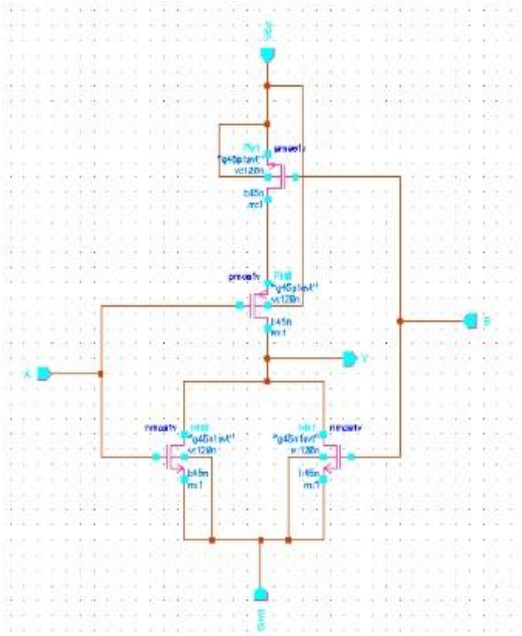

Figure 10: NOR Gate Schematic

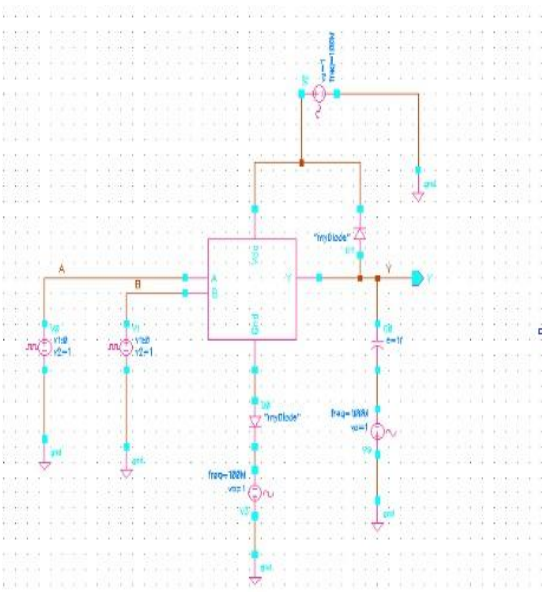

Figure 11: NOR Testbench

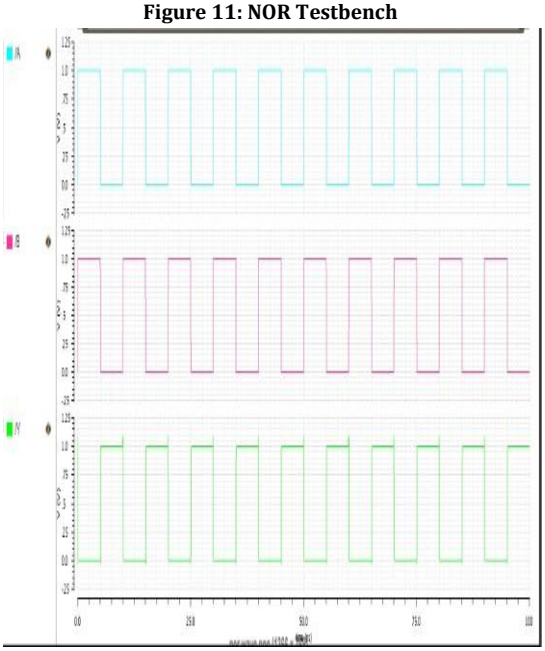

Figure 12: NOR Waveform

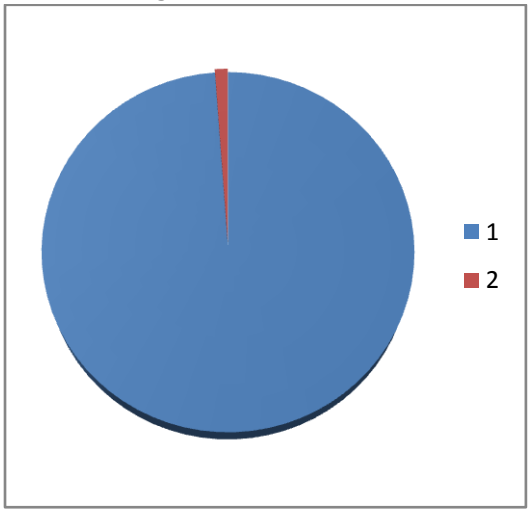

Figure 13: Power Dissipation in 1) CMOS & 2) LPHS Nor Gate

Following Facts are concluded from simulations of NOR Gate

1. The power dissipated in CMOS NOR Gate is **498.6E-3**
2. The power dissipated in designed Circuit is **5.786E-3.**

D. EX-OR Gate

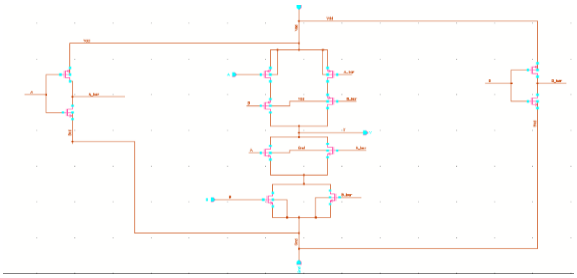

Figure 14: EX-OR Gate Schematic

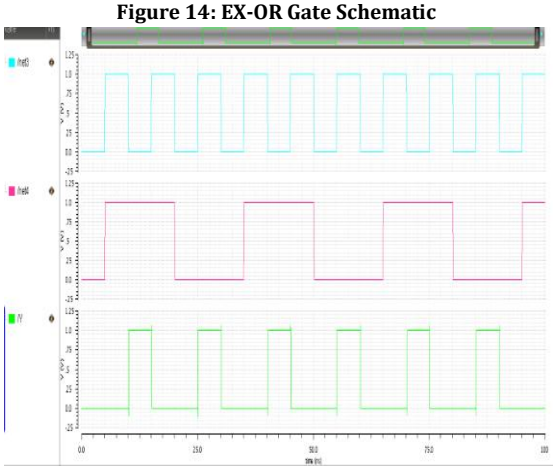

Figure 15: EX-OR Waveform

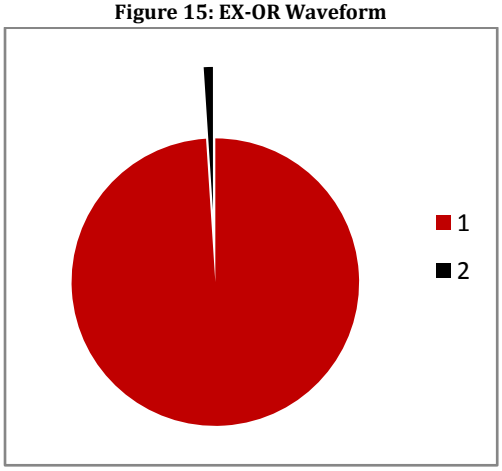

Figure 16: Power Dissipation in 1) CMOS & 2) LPHS EX-OR Gate

Following Facts are concluded from simulations of EX-OR Gate

1. The power dissipated in CMOS EX-OR Gate is **502.4E-3**
2. The power dissipated in designed Circuit is **5.236E-3.**

4. Conclusion

By using Adiabatic Logic various gates were designed and an improvement of 70-80 % in power consumption as compared with conventional CMOS circuits is achieved. As such designs are useful in applications where power reduction is of prime importance. The very fact is clear from the table no-1 given below that the power reduction is a greater factor in these circuits but the complexity of the circuit and the area required by layout also increases. So, the compromise between the two has to be chosen as to achieve an optimized design and as per required application which is the need of an hour.

Table 1: Power dissipation in various gates

LOGIC	INVERTER	NAND	NOR	EX-OR
CMOS	489.9E-3	493.3E-3	498.6E-3	502.4E-3
LPHS	10.67E-3	6.026E-3	5.786E-3	5.236E-3

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