

Washington University in St. Louis

## Washington University Open Scholarship

---

All Computer Science and Engineering  
Research

Computer Science and Engineering

---

Report Number: WUCS-92-50

1993-05-11

### Mini-ATMizer User's Guide and Technical Manual

David M. Zar

Follow this and additional works at: [https://openscholarship.wustl.edu/cse\\_research](https://openscholarship.wustl.edu/cse_research)

---

#### Recommended Citation

Zar, David M., "Mini-ATMizer User's Guide and Technical Manual" Report Number: WUCS-92-50 (1993). *All Computer Science and Engineering Research*.  
[https://openscholarship.wustl.edu/cse\\_research/612](https://openscholarship.wustl.edu/cse_research/612)

Department of Computer Science & Engineering - Washington University in St. Louis  
Campus Box 1045 - St. Louis, MO - 63130 - ph: (314) 935-6160.

**Mini-ATMizer User's Guide and Technical Manual**

**David M. Zar**

**WUCS-92-50**

**May 1993 (revised)**

**Department of Computer Science  
Washington University  
Campus Box 1045  
One Brookings Drive  
St. Louis MO 63130-4899**



Washington Univeristy  
ARL/ERL  
St. Louis, MO 63130

---

**Mini-ATMizer  
User's Guide  
and  
Technical Manual**

---

Prepared by  
David M. Zar

Under the Direction of  
William D. Richard

May 17, 1993



# Table of Contents

<b>Using The Mini-Atmizers .....</b>	<b>1</b>
How To Set Up The Mini-ATMizer Transmitter .....	1
Setting The ATM Headers .....	4
Using The Error Counter .....	5
How to Debug the Transmitter .....	5
Images Are Sent But Not Received .....	5
The Error Counter Always Shows 8 .....	6
How To Set Up The Mini-ATMizer Receiver .....	7
Using The Error Counter .....	10
How to Debug the Receiver .....	10
Images Sent But Not Displayed .....	11
The Error Counter Always Shows 8 .....	11
<b>Mini-ATMizer Technical Manual .....</b>	<b>12</b>
Introduction .....	12
Overview Of The Mini-ATMizers .....	12
Mini-ATMizer Transmitter .....	12
Mini-ATMizer Receiver .....	14
Setup And Configuration .....	15
Configuring The Transmitter Twisted Pair Connector .....	16
Setting The ATM Headers .....	17
Theory Of Operation .....	19
Transmitter PAL Definitions .....	19
Receiver PAL Definitions .....	22
Clocking .....	23
Transmitter Data Path .....	23
Receiver Data Path .....	25
Design Considerations .....	27
Transmitter FIFO Selection .....	27
Receiver FIFO Selection .....	28
Software Control .....	29

Timing Analysis .....	31
Transmitter: Receive Imlogix Data .....	31
Transmitter: FIFO Read and Packetize .....	32
Receiver: Receive ATM Packets .....	33
Receiver: Data out to EVB .....	35
<b>References .....</b>	<b>37</b>
<b>Appendix A .....</b>	<b>38</b>
<b>Appendix B .....</b>	<b>44</b>
<b>Appendix C .....</b>	<b>47</b>
<b>Appendix D .....</b>	<b>58</b>

Washington Univeristy  
ARL/ERL  
St. Louis, MO 63130

---

**Mini-ATMizer**

**User's Manual**

---

Prepared by  
David M. Zar

May 17, 1993



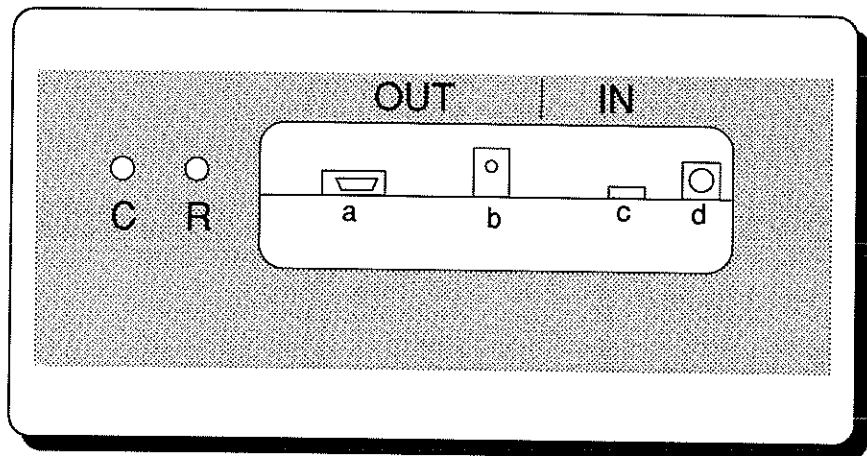


# Using The Mini-Atmizers

## How To Set Up The Mini-ATMizer Transmitter

The mini-ATMizer transmitter is used to convert the Imlogix data stream into a packetized ATM format for use over an ATM network. Its input is an Imlogix data stream - from an image server such as Megascan - and its output is ATM. The front, or connector side, of the transmitter is shown in Figure 1. The transmitter may be fitted with either a fiber or a mini-DIN3 twisted pair input. This is done by swapping the transmit and receive chips from FOXIs to TAXIs or vice versa. If the fiber connector is present (i.e. a FOXI is inserted) then that connector must be used as the twisted pair connector is disabled when the FOXI is used.

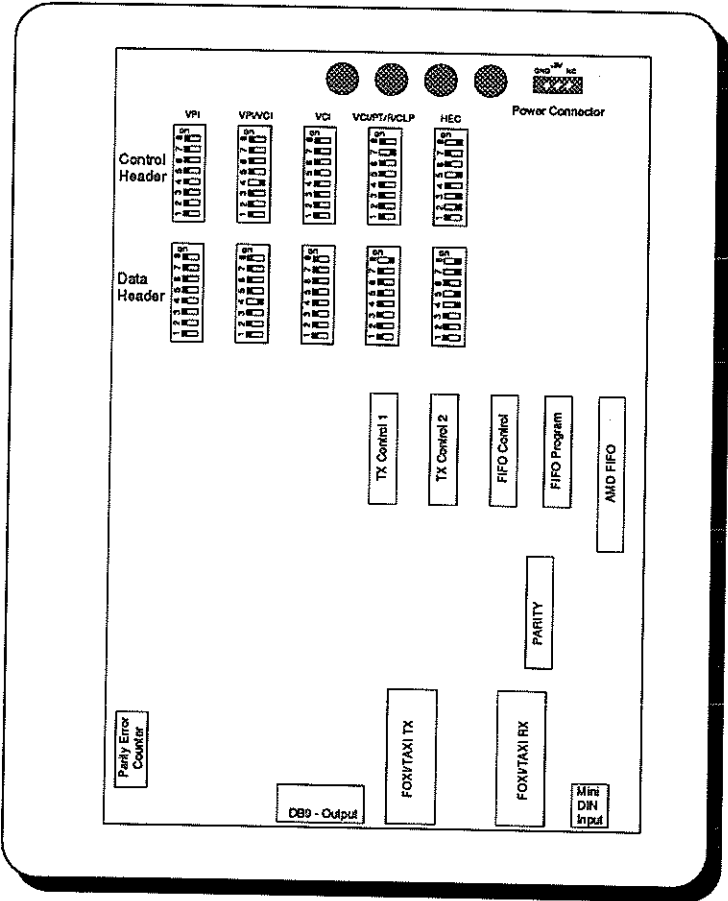
In a similar manner, the output may be fitted with either a fiber or a DB9 twisted pair output.



**Figure 1:** Front view of Transmitter showing the connectors and push buttons. a) DB9 twisted pair output; b) FOXI/TAXI transmitter for selecting fiber or twisted pair (FOXI shown) output; c) FOXI/TAXI receiver for selecting fiber or twisted pair (TAXI shown) input; d) mini-DIN3 twisted pair input.

To change the FOXI to a TAXI, turn off the power to the transmitter and open the case of the transmitter. The top of the case is held on by one set screw. Once this screw is removed, the top may be slid back to expose the circuit board. Figure 2 shows the placement of the receive and transmit FOXI/TAXI chips. Note which one you will be replacing and obtain the replacement part.

- The AM7968 is a transmitter.
- The AM7969 is a receiver.
- The FOXI parts have arrows denoting the direction of data flow. An arrow pointing into the chip denotes a receiver. An arrow pointing into the connector denotes a transmitter.



**Figure 2:** Transmitter circuit board showing the major components and their relative positions. The header DIP switches are shown in their default positions.

Be careful not to bend the pins or the fiber connectors when removing or inserting the part.

Gently remove the part to be replaced. Insert the new part into the socket. Be sure all pins are firmly in the socket and that the chip is oriented correctly.

The FOXI's fiber connector should be facing the opening in the case and the TAXI chip's indentation on the chip should also be facing the opening.

Once all chips have been inserted as desired, replace the top of the case. The transmitter should now be connected to the image source and the ATM network. Depending on which chips were placed in the transmitter, you will need to make the appropriate connections to the transmitter. Table 1 shows the possible connections that need to be made to the transmitter.

		Transmitter Chip	
		FOXI	TAXI
Receiver Chip	FOXI	fiber from server fiber to ATM	fiber from server DB9 twisted pair to ATM
	TAXI	mini-DIN3 from server fiber to ATM	mini-DIN3 from server DB9 twisted pair to ATM

**Table 1:** Transmitter connector types based on chip selection.

When the mini-DIN3 connector is used, it originates from a distributor box and is connected as if it were an EVB. No special connections need be made. When the fiber connector is used for the input to the transmitter, the fiber originates from the image server or may be connected as the last fiber on a distributor box daisy chain.

If the transmitter is not placed at the end of a distributor box daisy chain, the transmitter should use the mini-DIN3 input, only.

For the connections to the ATM network, be sure the network will support the connector you will use. If the twisted pair connector is to be used, please refer to the technical documentation to see the details of properly setting up the twisted pair connector.

Once all connections are made, turn on the power to the transmitter. You should then press the *clear* button (C) to clear the error counter. The transmitter is now ready for use.

If the first few images are not received properly, or at all, then you may need to reset the transmitter. This is done using the *reset* (R) button. Please see the section *How to Debug the Transmitter* later in this manual for more detailed instructions.

---

### Setting The ATM Headers

---

The transmitter has two banks of five 8-position DIP switched which are used to select the ATM headers. There are two headers which are used: control and data. Figure 2 shows the switches in their default positions which correspond to 0008004096h for control and 00080080D8h for data.

NOTE: Bit 8 of the DIP switches is the LSB for each byte and bit 1 is the MSB. In addition, the *on* position is a logic 0.

The control header is used to start a *control* packet when sent. The data header is used to start a *data* packet. These two headers **must** be different. The default switch positions are shown below in Table 2. These headers correspond to a VCI of 4 for control and a VCI of 8 for data packets. If the mini-ATMizer receiver is to be used, refer to the technical documentation for the valid control and data VCIs. If no mini-ATMizers are being used, then any VCI may be used. Please refer to the technical documentation for more information on changing the headers.

---

## Using The Error Counter

---

The error counter on the transmitter will count the number of parity errors on the input data stream. This should always be zero. There are several reasons why the counter may not be zero.

- A parity error was detected in the input data stream.
- The counter was not reset after powering up the transmitter.
- The input fiber or twisted pair connector is not properly connected.
- The **reset** button is pressed and not released.

To reset the counter to zero, press the **clear** (C) button on the front of the transmitter. This should be done whenever the transmitter is powered up, or whenever the **reset** (R) button was used to reset the transmitter.

This error counter is used only for debugging purposes. It has no effect on the input or output data streams. Hence, if an error was detected, the data is passed through the transmitter as if no error occurred. Please see the technical documentation for more information.

---

## How to Debug the Transmitter

There are several common problems which may be encountered after the transmitter is first placed on-line with the ATM network. Each is described below with its most common solutions. For further information, please see the technical documentation.

---

### Images Are Sent But Not Received

---

- Check both the input and the output connectors. If twisted pair output to the ATM network is being used, be sure the

twisted pair interface is compatible with the ATM network. See the technical documentation for more information.

- Check the transmitter error counter. Is it a zero? If not, press the **clear** (C) button on the front of the transmitter. Is it now zero? If not, the input data stream is probably not connected properly. Be sure the right connector type is used and be sure it is properly connected. Also be sure to check the image server connection.
- Reset the transmitter by pressing the **reset** (R) button on the front of the transmitter. Also, clear the error counter with the **clear** (C) button. This may have to be done several times before the transmitter and the ATM switch synchronize. The operator of the switch can help determine if this is the problem and if any data is being sent by the transmitter to the switch. See the technical documentation for more information.

---

### The Error Counter Always Shows 8

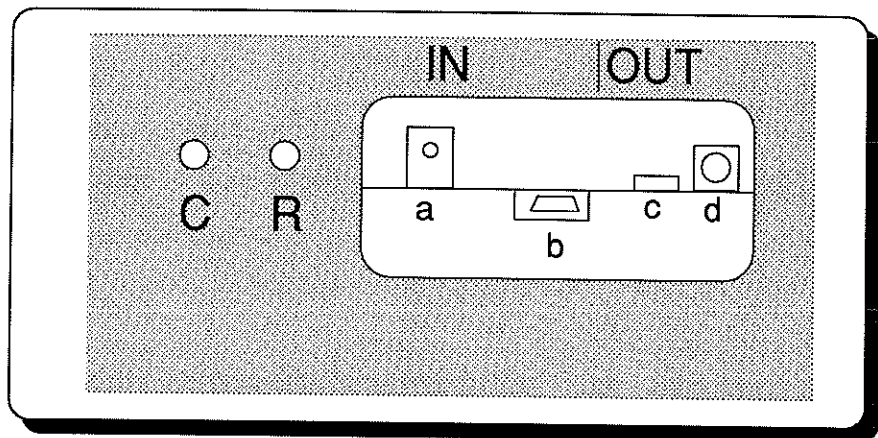
---

- Press the **clear** (C) button to clear the counter display.
- If 8 still appears, then this indicates that the input to the transmitter is *floating*. *Check to be sure you have the correct connector (fiber or twisted pair) connected and that the other end of the input (i.e. the server) is also on-line and connected.*

## How To Set Up The Mini-ATMizer Receiver

The mini-ATMizer receiver is used to convert the ATM data stream into an Imlogix format for display on an EVB. Its input is an ATM data stream - from an ATM network - and its output is Imlogix format. The front, or connector side, of the receiver is shown in Figure 3. The receiver may be fitted with either a fiber or a mini-DIN3 twisted pair output. This is done by swapping the transmit and receive chips from FOXIs to TAXIs or vice versa. If the fiber connector is present (i.e. a FOXI is inserted) then that connector must be used as the twisted pair connector is disabled when the FOXI is used.

In a similar manner, the input may be fitted with either a fiber or a DB9 twisted pair connector.



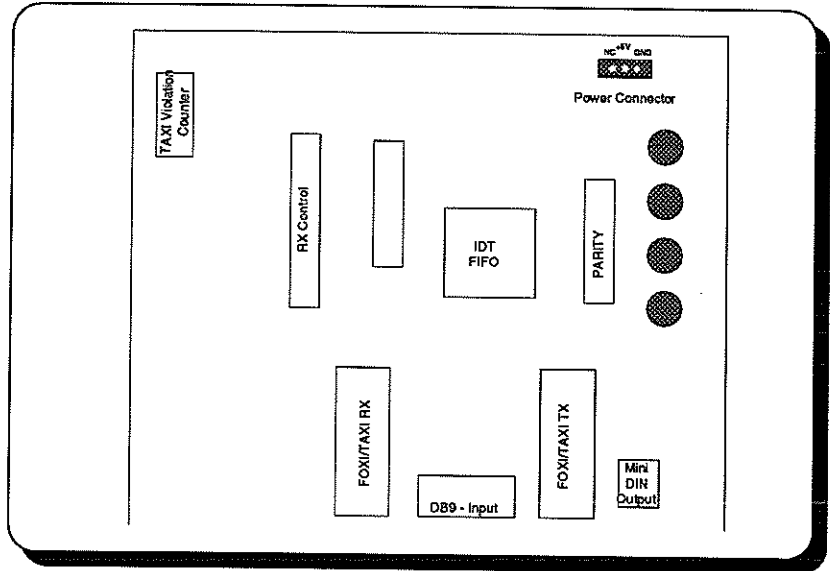
**Figure 3:** Front view of receiver showing the connectors and push buttons. a) FOXI/TAXI transmitter for selecting fiber or twisted pair (FOXI shown) input; b) DB9 twisted pair input; c) FOXI/TAXI transmitter for selecting fiber or twisted pair (TAXI shown) output; d) mini-DIN3 twisted pair output.

To change the FOXI to a TAXI, turn off the power to the receiver and open the case of the receiver. The top of the case is held on by one set screw. Once this screw is removed, the top may be slid back to expose the circuit board. Figure 4 shows the placement of the receive and



transmit FOXI/TAXI chips. Note which one you will be replacing and obtain the replacement part.

- The AM7968 is a transmitter.
- The AM7969 is a receiver.
- The FOXI parts have arrows denoting the direction of data flow. An arrow pointing into the chip denotes a receiver. An arrow pointing into the connector denotes a transmitter.



**Figure 4:** Receiver circuit board showing the major components in their relative positions.

Be careful not to bend the pins or the fiber connectors when removing or inserting the part.

Gently remove the part to be replaced. Insert the new part into the socket. Be sure all pins are firmly in the socket and that the chip is oriented correctly.

The FOXI's fiber connector should be facing the opening in the case and the TAXI chip's indentation on the chip should also be facing the opening.

Once all chips have been inserted as desired, replace the top of the case. The receiver should now be connected to the ATM source and the EVB. Depending on which chips were placed in the receiver, you will need to make the appropriate connections to the receiver. Table

3 shows the possible connections that need to be made to the receiver.

		Transmitter Chip	
		FOXI	TAXI
Receiver Chip	FOXI	fiber from ATM fiber to EVB	fiber from ATM mini-DIN3 twisted pair to EVB
	TAXI	DB9 twisted pair from ATM fiber to EVB	DB9 twisted pair from ATM mini-DIN3 twisted pair to EVB

**Table 3:** Receiver connector types based on chip selection.

If the mini-DIN3 output is used, only one EVB may be driven from the receiver.

When the mini-DIN3 connector is used, it originates from a receiver and terminates at an EVB. No special connections need to be made and a distributor box is not used. When the fiber connector is used for the output of the receiver, the fiber terminates at a distributor box.

For the connections from the ATM network, be sure the network will support the connector you will use.

Once all connections are made, turn on the power to the receiver. You should then press the *clear* button (C) to clear the error counter. The receiver is now ready for use. Be sure the EVB is powered up on not displaying an error condition.

---

## Using The Error Counter

---

The error counter on the receiver will count the number of violations on the input data stream. This should always be zero. There are several reasons why the counter may not be zero.

- A violation was detected in the input data stream.
- The counter was not reset after powering up the receiver.
- The input fiber or twisted pair connector is not properly connected.
- The **reset** button is pressed and not released.

To reset the counter to zero, press the **clear** (C) button on the front of the receiver. This should be done whenever the receiver is powered up, or whenever the **reset** (R) button was used to reset the receiver.

This error counter is used only for debugging purposes. It has no effect on the input or output data streams. In the event of a violation, however, no valid data was present and no data will be passed through the receiver. Please see the technical documentation for more information.

---

## How to Debug the Receiver

There are several common problems which may be encountered after the receiver is first placed on-line with the ATM network. Each is described below with its most common solutions. For further information, please see the technical documentation.

---

### Images Sent But Not Displayed

---

- Is the receiver powered up and is the error counter cleared? If the error counter is not cleared (zero) clear it by pressing the **clear (C)** button on the front of the receiver.
- If the error counter is still not zero, check to be sure the correct type of input connector is being used and that it is properly connected.
- If the error counter is zero, verify that the source transmitting the images has a valid VCI for both control and data packets. See the transmitter documentation and the technical documentation for more information.
- Does the EVB display an error (parity error or TAXI link down)? If it does, check to be sure the output connector is of the correct type and that it is properly connected to both the receiver and the EVB/distributor box.
- If all connections look good and the EVB reports no errors, reset the EVB by turning it off and on. If the EVB has been sitting idle for several tens of hours, it will sometimes lock up and not display images.
- Verify that the EVB's TAXI NET address is correct for the images being sent.

---

### The Error Counter Always Shows 8

---

- Press the **clear (C)** button to clear the counter display.
- If 8 still appears, then this indicates that the input to the receiver is *floating*. Check to be sure you have the correct connector (fiber or twisted pair) connected and that the other end of the input (i.e. the network switch) is also on-line and connected.



Washington Univeristy  
ARL/ERL  
St. Louis, MO 63130

---

**Mini-ATMizer**

**Technical Manual**

---

Prepared by  
David M. Zar

May 17, 1993



# *Mini-ATMizer Technical Manual*

---

## **Introduction**

The mini-ATMizer transmitter and receiver are used to transport Imlogix format images across ATM networks. This manual provides users of the mini-ATMizers with a complete description of the boards and their interfacing to the image server, ATM network, and the EVB.

This document should be skimmed through by anyone who will be installing or configuring the mini-ATMizers. More casual users of the mini-ATMizers should consult the User's Manual for a less technical description and usage hints. For those who will be reconfiguring the mini-ATMizers, this document should be read thoroughly before any changes are made to the boards.

---

## **Overview Of The Mini-ATMizers**

This section will discuss the basic functions of each of the mini-ATMizer boards. For complete schematics of the transmitter and receiver, see Appendices A and B, respectively.

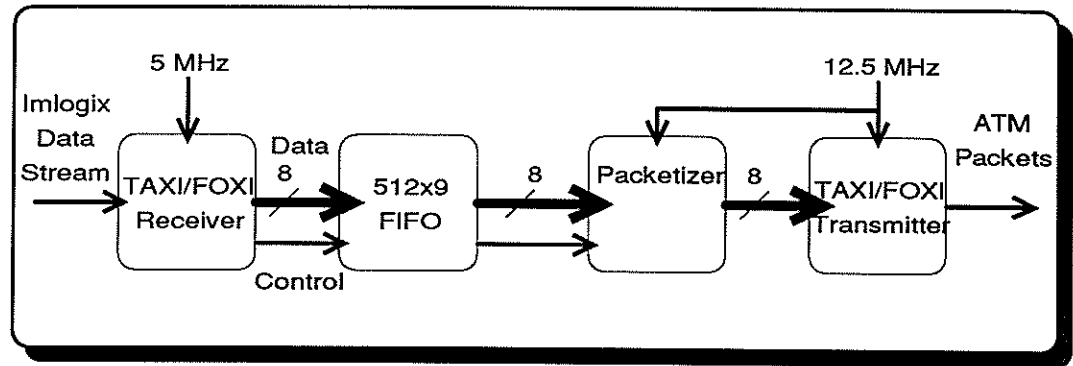
---

### **Mini-ATMizer Transmitter**

---

The mini-ATMizer transmitter is used to convert the Imlogix native image format into a standard ATM packetized data stream. This data stream is then sent into an ATM network where it may be routed to any number of receivers capable of converting the packetized data back into the Imlogix format for display on an EVB. There are four main sections in the transmitter. These are shown in block diagram fashion in Figure 1.





**Figure 1:** Transmitter block diagram showing the major divisions of the mini-ATMizer transmitter.

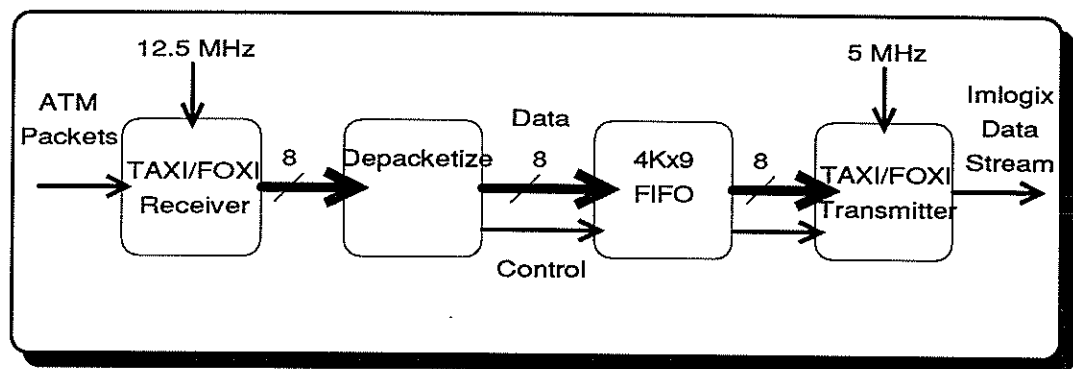
- The TAXI/FOXI receiver is used to accept the Imlogix data from either a fiber or twisted pair source. The twisted pair interface is a mini-DIN3 connector (AppleTalk connector) and will connect to a distributor box output. This TAXI/FOXI is in 10-bit mode - eight data bits and two parity bits. There is one bit used for control signals from the Ironics daughter board. This receiver runs at 5 MHz, or 40 Mb/s.
- The 512x9 FIFO is an AM4601 which is a programmable asynchronous FIFO with full and empty flags. This FIFO is used to buffer the data until 48 bytes are received. The programmable "packet flag" will be asserted to signal the packetizer that at least one packet worth of data is present.
- The packetizer is responsible for building valid ATM packets with correct VCIs for two types of packets: **data** and **control**. The standard ATM packet is 53 bytes long: 48 bytes of data and five bytes of header. The **data** packets are what are normally sent. These contain 48 bytes of image or EVB header data. The control packet is used to signal the EVB that a data stream is about to be sent.
- The packetized data is sent through the TAXI/FOXI transmitter into the ATM network. When a TAXI is used, a DB9 twisted pair interface is supported. This TAXI/FOXI runs in 8-bit mode. The TAXI/FOXI transmitter runs at 12.5 MHz, or 100 Mb/s.

---

## Mini-ATMizer Receiver

---

The mini-ATMizer receiver is used to convert the ATM packetized image data back into the Imlogix format for display on an EVB. The mini-ATMizer has a limited capability for selection of control and data VCIs and is not programmable. This receiver is a dumb device which simply accepts ATM packets, strips off the headers, and sends the data to an EVB. A block diagram is shown in Figure 2.

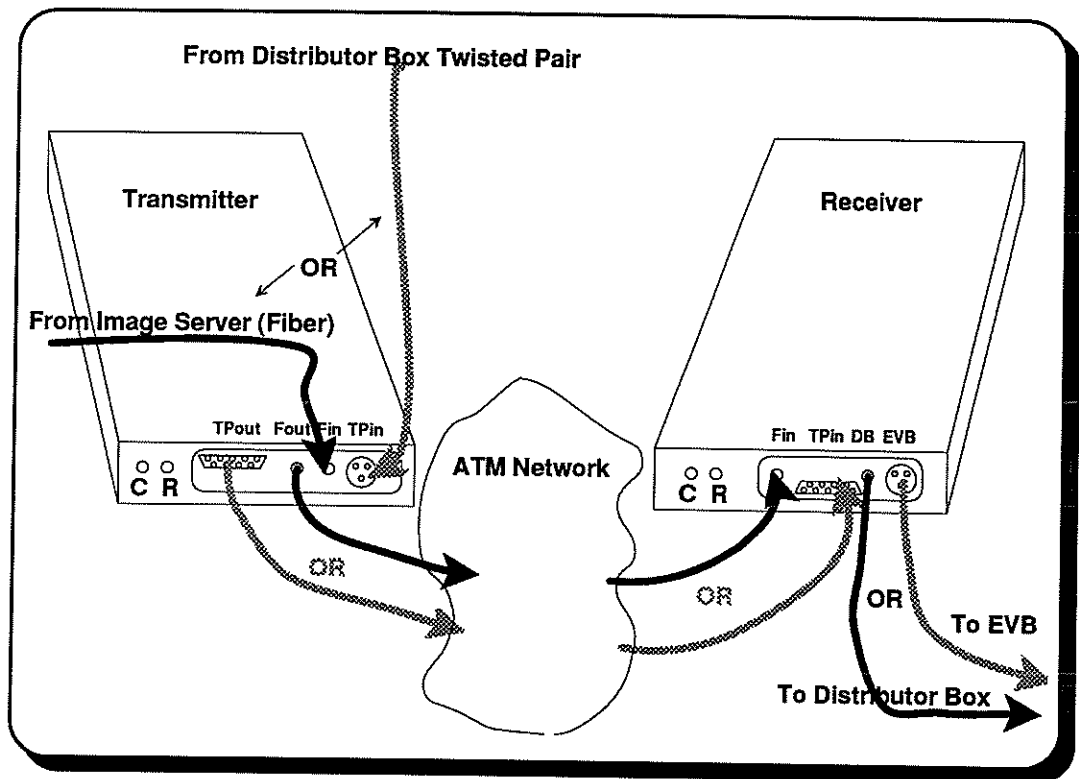


**Figure 2:** Transmitter block diagram showing the major divisions of the mini-ATMizer receiver.

- The TAXI/FOX I receiver accepts ATM packets and moves them into the depacketizer. The TAXI/FOX I is run in 8-bit mode at 12.5 MHz, or 100 Mb/s.
- The depacketizer is nothing more than a sequencer which checks the VCI to determine if the packet is data or control, and then strips the header from the data. The depacketizer will toggle a control line to denote if the packet was data or control and all packet data is placed into the FIFO for further processing.
- The FIFO is a 4Kx9 IDT72240 clocked FIFO with programmable flags and full and empty flags. Only the empty flag is used by the receiver. When the empty flag is deasserted, indicating data in the FIFO, a 9-bit word is read from the FIFO. This word is sent to the TAXI/FOX I transmitter to be sent to the EVB. The ninth bit in the word is the bit which denotes data or control.
- The TAXI/FOX I transmitter accepts data, adds two parity bits, and transmits the data to the EVB. The transmitter is in 10-bit mode and is run at 5 MHz, or 40 Mb/s.

## Setup And Configuration

The mini-ATMizers must be connected to the ATM network via fiber or twisted pair. The connection options are selected by inserting appropriate TAXI/FOXI chips into the transmit/receive IC sockets. This is described in detail in the User's Manual. Figure 3 shows the possible connection to and from the mini-ATMizer receiver and transmitter.



**Figure 3:** This drawing depicts all possible connections to and from the ATM network for the mini-ATMizer transmitters and receivers. Note that only one of the connector types in each direction (in and out) may be active at any time. The connector used is determined by the type of chip - TAXI/FOXI - used.

---

## Configuring The Transmitter Twisted Pair Connector

---

If a twisted pair connection is to be used from the transmitter to the ATM network, certain items must be checked.

- The supported twisted pair connection requires a straight through DB9 twisted pair cable. The only pins which must be connected are 1, 5, 6 and 9. The other pins are not connected on either the transmitter or the receiver.
- If the transmitter to be connected to the ATM network will be connected directly to a **switch**, then capacitors C66 and C67 must be removed and replaced by jumper wires. If the transmitter is to be connected to a repeater box, these capacitors must be installed (0.1 $\mu$ F).

The ATM switch will perform the *reversing* of the transmit and receive pins. If a transmitter and a receiver are to be connected without a switch between them, and twisted pair is used, then a null cable must be used to reverse the pins. Table 1 shows the pin-outs for the DB9 twisted pair connector.

Pin	Function
1	Transmit -
5	Receive -
6	Transmit +
9	Receive +
2, 3, 4, 7, 8	No Connection

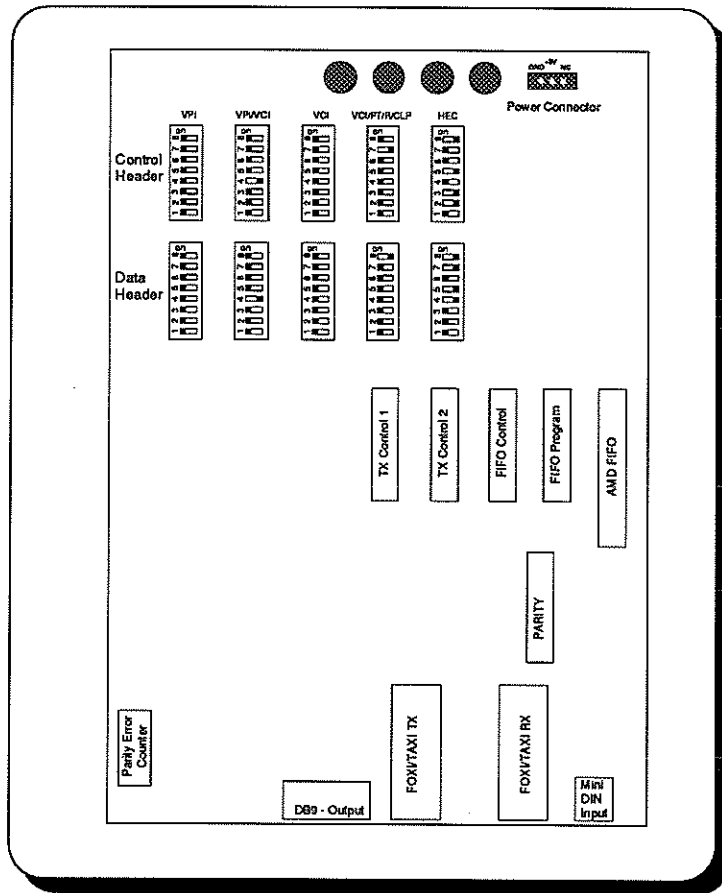
**Table 1:** Pin-outs for the DB9 twisted pair connectors on both the transmitter and receiver.

---

## Setting The ATM Headers

---

Figure 4 shows the general layout of the transmitter. The two banks of DIP switches are used to set the ATM headers. Figure 5 shows the ATM header definition.



**Figure 4:** Transmitter circuit board showing the major components and their relative positions. The header DIP switches are shown in their default positions.

To set the ATM headers to something other than the default (VPI 8, VCI 4 - control; VCI 8 - data), one should first write down the complete header including the header error check (HEC) which is an

8-bit CRC. Please consult the switch owners for a complete description of the ATM header and the HEC.

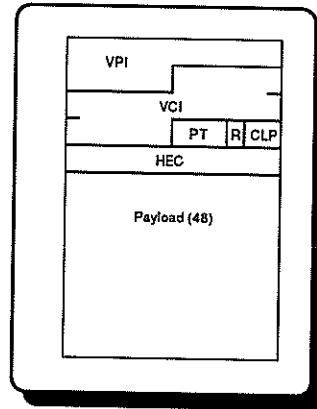


Figure 5: ATM header

Two headers must be formed: control and data. The control header is used to send a *control* packet while the data header is used to send a *data* packet. The packets are identical in form but very different in meaning to the receiver which will convert from ATM back to the Imlogix format. **Be sure the two headers are different.** In addition, if the mini-ATMizer receiver is to be used, there are some limitations as to the VCIs for both the control and data packets. A list of all possible VCIs for both types are listed in Table 2. If some other receiver is used, see its documentation to see what limitations it may impose on the selection of VCIs. Any VCI/VPI combination may be selected on the transmitter via the DIP switches. Please consult the switch owners for more information on VPI selection. As of now, the VPI must be 8.

The DIP switches are set by sliding the switch to the **on** position for a logic 0 and **off** for a logic 1. The most significant bit is switch 8 and the least significant bit is switch 1 in each byte, or DIP switch. The left-most DIP switch in each row is the least significant byte in the header as shown in Figure 5.

Control VCIs (Hex)	Data VCIs (Hex)
0xx4	0xx8
0xx5	0xx9
0xx6	0xxA
0xx7	0xxB

**Table 2:** Valid control and data VCIs when using a mini-ATMizer receiver. An *x* denotes any valid hexadecimal digit. Currently, the switch only looks at the lower 12 bits - three bytes - of the VCI so the most significant byte is ignored. This may change. Please consult the switch documentation for more information.

---

## Theory Of Operation

This section discusses, in detail, the control logic and functional units of the mini-ATMizer boards. This is meant to aid in the understanding, debugging, and modification of the mini-ATMizers. Complete schematics are supplied in Appendices A and B. Complete parts lists are supplied in Appendix D. Complete PAL equations are supplied in Appendix C.

---

### Transmitter PAL Definitions

---

There are three groups of PALs on the mini-ATMizer: FIFO operation, control and parity.

The PALs used for the FIFO operation are U14 and U15, also known as **CONTROL** and **PROGRAM**. As indicated by its name, **CONTROL** is used to generate the necessary control signals for the FIFO operation and programming stage. There are only two signals generated by this PAL: *WR*\ and *RS*\. *WR*\ is a true low write strobe for the AMD FIFO. When this signal goes low, the FIFO is ready to latch the data. The data must be present 15 ns before *WR*\ returns to high and the FIFO is updated at the same rising edge.

There are two cases when this signal will go low. The first is during normal operation when data is received by the input TAXI/FOXI. The TAXI/FOXI will assert *DSTRB* when valid data is received and thus *WR\* will be asserted at the same time to write that data into the FIFO. The second case is when the transmitter is powered up or reset. When this occurs, the AMD FIFO must be programmed to use one of its flags as a packet flag. This flag is programmed to be asserted when at least 48 bytes are resident in the FIFO. The program is written into the FIFO in the same manner as data, but the *C/D\* line is held high to indicate programming mode. The program is four bytes long and must be clocked into the FIFO using the *WR\* signal. Thus, this signal is also asserted on counter numbers 2, 3, 4, and 5 when the *RESET* signal is asserted. Counts 0 and 1 are not used, for during these counts, the FIFO is reset and cleared.

The reset signal *RS\* is used to reset the FIFO, only. The FIFO must be reset for a moment, then it must be programmed before data is sent to the FIFO. For this reason, the PAL will generate a short (40 ns) reset signal for the FIFO at the beginning of a board reset.

The **PROGRAM** PAL contains the program for the AMD FIFO. The PAL is used as a small ROM and contains the four byte program. The program bytes are F0h 70h 30h D0h for registers 0 through 3 as defined in the AMD data book[1]. The outputs of the **PROGRAM** PAL are only on when *RESET* is asserted. In addition, the output values of this PAL are only read into the FIFO when *WR\* is asserted from the **CONTROL** PAL.

The PALs which comprise control of the transmitter are U6 and U7. These PALs generate the correct timing signals to enable the correct headers to be sent, and also if and when data packets are to be sent.

PAL U6 controls the headers for **null** packets and data packets. The signal *ENO\* is used whenever *NULL\* is deasserted or when *RESET*



is asserted. This signal is asserted during the second half of an 80 ns clock cycle. This causes a **null** packet to be sent (header and payload of all zeros). When the board is reset, the ATM network must still be receiving packets, so **null** packets are sent even as the transmitter is being reset.

The signals *END1\* through *END5\* are used to enable data header bytes one through five. These signals are asserted during the second half of an 80 ns clock cycle. They are asserted in order (1..5) on counts 0..4 in order to enable one header byte at a time to be sent. At the same time, *ENBUF\* is asserted to enable the buffer (U28) and allow the header data to pass through to the transmit portion of the circuit. After count four (4), *RD\* is asserted on the second half of an 80 ns clock cycle for 48 cycles. This signal reads a byte from the FIFO and allows it to be sent by the transmit portion of the circuit. This signal is used during counts 5..52, inclusive.

The second control PAL (U7) generates the signal *ENC1\* through *ENC5\*. The signals *ENC1\* through *ENC5\* are used to enable control header bytes one through five. These signals are asserted during the second half of an 80 ns clock cycle. They are asserted in order (1..5) on counts 0..4 in order to enable one header byte at a time to be sent.

The *SYNC* and *CMD* signals are used to generate sync characters and commands through the TAXI/FOXI transmitter. *SYNC* is asserted once every 16 packets and occurs on count 53. When *SYNC* is asserted, it causes a sync character to be transmitted over the TAXI/FOXI. *CMD* is asserted immediately after *SYNC* (on count 54) and causes the command 1111 to be sent.

The signal *ROLL\* is asserted to roll over the byte counters. This will occur on count 52 for packets 1..15 and will occur on count 54 for the

16<sup>th</sup> packet. This signal is also asserted on the second half of an 80 ns clock.

The final PAL used is for parity. The transmitter will check the input data stream for any parity errors in the **PARITY** PAL (U40). This PAL simply regenerates the parity and compares the newly generated parity to the parity sent.

---

### **Receiver PAL Definitions**

---

The receiver has two PALs: **CONTROL** and **PARITY**. The control PAL (U14) contains all of the control signals needed for the operation of the receiver. The parity PAL (U2) generates two parity bits to be sent with the data.

The receiver control PAL will generate a *DSTB*\ signal which is the complement of *DSTRB* when *RESET*\ is deasserted which is generated by the input TAXI/FOXI.

The *LOAD*\ and *CLR*\ signals are used to control the counters. *CLR*\ is generated whenever the command 111 is received from the ATM network. This is used to synchronize the send and receive TAXI/FOXIs. *LOAD*\ is asserted whenever the counter is 52 in order to reset the counter to zero (0).

*WREN*\ is asserted to enable a write into the IDT FIFO. This signal will be asserted when the packet received is a data packet and the byte is 5..52. This will effectively strip off the header bytes and only write the data into the FIFO. In addition, when a control packet is received, this signal will be asserted for one count only (count 5) in order to write the control bit into the FIFO.

*SCLK3* is asserted on count 3 which corresponds to byte four of the received packet. This signal will latch the fourth header byte which determines if the packet is a **control**, **data**, or **null** packet.

---

### Clocking

---

The mini-ATMizer transmitter uses a two-phase clock where phase two is the complement of phase one with a slight delay between  $\phi_{1h}$  and  $\phi_{2bl}$  and  $\phi_{1hl}$  and  $\phi_{2lh}$ . (maximum delay is 6 ns when fully loaded.) The counters and some synchronizing flip-flops are allowed to change during  $\phi_1$  only, and the control signals, from PALs for example, and other synchronizing flip-flops are allowed to change during  $\phi_2$  only. In this way, the counters have almost 40 ns to settle before being read, and the PALs will have almost 40 ns to modify the counters, if needed, before they increment.

A similar scheme is used on the receiver, but it is *DSTRB* which is the reference signal. *DSTRB* and its complement are used to increment the counters and control the receiver PAL. The theory is the same as in the transmitter.

---

### Transmitter Data Path

---

Data is sent from an image server to the transmitter in Imlogix data format via fiber or twisted pair from a distributor box or fiber directly from the image server. This data is being sent at 5 MHz, or 40 Mb/s in TAXI 10-bit format. This format implies two parity bits. These parity bits are checked at the transmitter for any errors and then discarded. If a parity error is discovered, the error counter is incremented by one.

The resultant eight data bits are placed into the AM4601 FIFO to be packetized into valid ATM packets. The data is clocked into the FIFO on the falling edge of *DSTRB*. This allows ample time for setup of the data at the FIFO inputs.

In addition, the control lines (*CO* and *CSTRB*) are watched to see if the image server has sent a reset to the EVB. If this is the case, then guaranteed, the next packet sent will be a **control** packet and not a **data** packet. This signal is not placed into the FIFO. The control signal will also cause the transmitter to reset portions of itself; The FIFO and synchronizing flip-flops will be reset.

In the absence of a reset command, the programmable flag on the FIFO is sampled once every “packet period,” which is every 53 ATM clock cycles, or 2.12 $\mu$ s. The “packet flag” is programmed to be asserted only when 48 or more bytes are in the FIFO. If this “packet flag” is set then this signals the transmitter control to send out a data packet, else a **null** packet is sent. **Null** packets must be sent every time no **data** packet is ready for the ATM link must always be filled with packets.

When at least 48 bytes are in the FIFO and the “packet flag” has signaled the **data** packet transfer, the header for a data packet is sent. These five bytes are determined by the DIP switches. After the header is sent, the FIFO is emptied and the 48 bytes sent. The “packet flag” will then be deasserted and the transmitter will send a **null** packet. A data packet will always be followed by at least one null packet for the transmitter is receiving data at only 5 MHz and sending it at 12.5 MHz.

Aside from **control**, **data** and **null** packets, the ATM switch wants to receive synchronizing characters every 16 packets. This is done by sending out a *sync* character (no *DSTRB*) followed by a 0Fh command on the command lines of the TAXI/FOXI. This adds two 12.5 MHz cycles (or 80ns) to every 16<sup>th</sup> packet sent.

---

### Receiver Data Path

---

Data is received by the receiver over a DB9 twisted pair connection or fiber via the TAXI/FOXI at the input. The data sent is in 8-bit TAXI format and is sent at a constant rate of 12.5 MHz. The incoming data causes the TAXI/FOXI to assert *DSTRB* for every data byte received. This signal is then used to clock the incoming data into the IDT72211 FIFO and into the “header latch” (U2).

The sequencer on the receiver determines which bytes are written to which location (latch or FIFO) and also determines which bytes are discarded. The sequencer count corresponds to the byte number in a valid ATM packet. Since the only portion of the header needed in the receiver is the fourth byte - or the lower four bits of the VCI, then only on count three (count starts at zero) does the data get latched into the “header latch.”

The “header latch” is used to select **command**, **data** or **null** packets. Only the upper two bits in this latch are of importance, and their meanings are shown in Table 3.

bit value	00b	01b	10b	11b
meaning	null packet	data packet	command packet	undefined

**Table 3:** Meanings of upper two bits in the “header latch.” The LSB is bit 8 and the MSB is bit 7 in the latch.

If the packet is a **null** packet, then the data in the packet is discarded. If the packet is a **command** packet, then one byte is clocked into the FIFO with the ninth bit set to a one. This one byte will signal the receiver to send an EVB command rather than data. When the packet is a **data** packet, the data in the packet is clocked into the FIFO in its entirety.

The empty flag (*EF*) on the FIFO is sampled at 5 MHz (200ns) to determine if there are any bytes ready for transmission to the EVB. If the *EF* is asserted, then both the read enable of the FIFO is asserted and the transmit TAXI/FOXI is allowed to clock the data in at the rising edge of *DSTRB*. *DSTRB* will go high after the falling edge of the 5 MHz clock. This allows ample time for the outputs of the FIFO to become stable, and so, too, the inputs of the TAXI/FOXI.

This process will continue until no data remains in the FIFO or until the ninth bit of the FIFO data output is set designating a control packet was sent. In this event, the TAXI/FOXI, when clocked with *DSTRB*, will send the TAXI command 01h which is interpreted at the EVB as a reset command.

The transmit TAXI/FOXI is configured in 10-bit mode. The additional two bits are used for parity. The parity bits are generated in PAL U13 and are appended to the data byte for transmission. No facility for parity across the ATM network is in place at this time. There is an error counter on the receiver which will count the number of violations (*VLTN*) the TAXI/FOXI receiver see from the ATM network. This does not guarantee, however, that the data sent was valid or that it was identical to the data received.

---

## Design Considerations

This section discusses some of the design considerations and trade-offs used in the mini-ATMizers. Where ever possible, quantitative analysis is used, but some of the design choices were based upon qualitative analysis.

---

### Transmitter FIFO Selection

---

The FIFO on the transmitter needs to have a programmable flag to be used as a “packet flag.” This simplifies the control logic needed on the transmitter. In addition, the FIFO must be large enough to buffer new arriving data as the existing data is removed during the packetizing process. A FIFO with enough room for two complete packets would suffice for the FIFO is being emptied at 2.5 times the rate at which it is being filled. It is impossible for a complete new packet to arrive during the time a packet worth of data (48 bytes) is removed from the FIFO. There is, however, the case where a **null** packet is starting to be sent just as new data arrives and becomes the 48<sup>th</sup> byte in the FIFO. In this case, about 21 bytes may arrive before any are removed. Hence,  $47 + 21 = 68$  bytes are in the FIFO when the transmitter starts to send the next **data** packet. Over the time it takes to send the packet, another 21 bytes may arrive. Thus, the FIFO will still have less that a full packet of data in it (42 bytes) and another **null** packet will be sent. It is obvious that it will never occur that more than 68 bytes would ever be in the FIFO. For this reason, a 512 byte FIFO is more than sufficient four the transmitter.

---

### Receiver FIFO Selection

---

The FIFO on the receiver must buffer ATM **data** packets at 12.5 MHz and not overflow when they are removed at 5 MHz. Having chosen a 4096 byte FIFO, it should be shown that this is sufficient. Since the clocks on the two boards are free running and not synchronized, it will be necessary to show that as long as they are within their specified tolerances, the FIFO will not overflow.

Assume the worst acceptable case: 4096 bytes are left in the FIFO after the entire image has been sent.

Thus, for a 10 MB image:

$$10,000,000 - 4096 = 9,995,904$$

are transferred out of the FIFO during the rest of the transfer time.

$$\text{let } t \equiv \text{clock\_rate} \text{ and } k \equiv \text{clock\_skew}$$

$$\text{then } 10,000,000t = 9,995,904kt$$

for the time to send all of the bytes must be equal to the time to process the bytes specified.

So now

$$k = \frac{10,000,000}{9,995,904} \approx 1.0004$$

and

$$t_s = kt = 1.0004t \equiv \text{clock\_skew\_time}$$

$$t_s = t \pm 0.04\%.$$



This says that the total clock skew time must be less than 0.04% in order for the assumptions above to be valid. The crystals used have a tolerance of 0.01% to the total skew is less than or equal to 0.02% which satisfies the above statement. Hence, a 4096 byte FIFO will not overflow and is of sufficient size.

---

### **Software Control**

---

There are a few software issues which must be adhered to if the mini-ATMizers are to be used successfully. Both reflect the desire to simplify the hardware at the expense of slight modifications of the software.

First, the software must pad the EVB headers with zeros to make the length of the header a multiple of 48. This is to ensure that the EVB header will be properly packetized and sent before the data is sent. If the padding is not performed, the last portion of the header will be sent with the first few bytes of data. This will not allow time for the EVB to parse the header and set up its tables before the data arrives. This will result in no image being seen, or a corrupted image.

Along the same reasoning, the data must also be padded out with zeros to a multiple for 48 bytes. This will ensure all data is flushed out of the FIFO on the transmitter and that all data is properly received by the EVB. If this padding is not done, an image time-out will occur at the EVB for not all of the bytes expected were sent.

The final issue is one of timing. After the initial EVB reset command is sent by the software, the software must delay before sending the EVB header. This delay is for several reasons. The first is that the EVB requires some time after the reset before it can receive data. When the EVB is directly connected to the image server, this delay may be simply included in the software. When the command is sent

over the ATM network, however, some buffering and additional delay may occur.

The EVB reset command also has some effects on the mini-ATMizer transmitter. Some state is reset on this board and the FIFO is reprogrammed. Hence, there must be sufficient time for this to complete before any data can be reliably received. The time needed for the resetting of the transmitter board is 4.24 $\mu$ s.

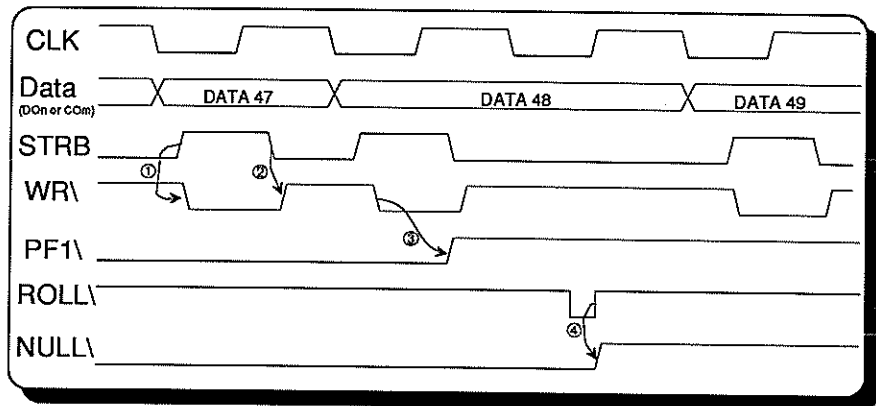
It should be adequate to insert a delay of about one millisecond, and this was tested with success. The current implementation has about a ten millisecond delay which is much more than enough time. It is recommended that this delay be too large as it is only sent once and is still quite a small portion of time to ensure proper operation of the mini-ATMizers.

## Timing Analysis

This section provides some timing analysis of the major portions of the two boards. This analysis is meant to be a guide for understanding how the mini-ATMizers work and as an aid in debugging the boards. The following timing gives relative times and, in most cases, does not include tolerances for actual, measured signals.

### Transmitter: Receive Imlogix Data

This portion of the transmitter contains the TAXI/FOX1 and the AMD FIFO (U1). The transmitter receives data here and buffers it in the FIFO. Figure 6 [2][3] shows the major signals and their relationships. This example assumes the first 46 bytes are already written into the FIFO. The 47<sup>th</sup> byte is being written as the beginning of the trace shown.



**Figure 6:** Timing diagram for the reading of data onto the transmitter board. CLK is the 5 MHz clock. Data are the data out lines from the TAXI/FOX1. STRB is the data strobe. WR\ is the write signal for the FIFO. PF1\ is the FIFO's "packet flag." ROLL\ is the signal that the end of a packet has just passed. NULL\ is the signal which denotes whether to send a **null** packet or a **data** packet.