FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 32, N° 4, December 2019, pp. 601-613
https://doi.org/10.2298/FUEE1904601T

NOVEL SINGLE LAYER FAULT TOLERANCE RCA CONSTRUCTION FOR QCA TECHNOLOGY

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Abstract. *Quantum-dot Cellular Automata (QCA) technology has become a promising and accessible candidate that can be used for digital circuits implementation at Nanoscale, but the circuit design in the QCA technology has been limited due to fabrication high-defect rate. So, this issue is an interesting research topic in the QCA circuits design. In this study, a novel 3-input Fault Tolerance (FT) Majority Gate (MG) is developed. Accordingly, an efficient 1-bit QCA full adder is developed using the developed 3-input MG. Then, a new 4-bit FT QCA Ripple Carry Adder (RCA) is developed based on the proposed 1-bit FT QCA FA. The developed circuits are implemented in the QCADesigner tool version 2.0.3. The results indicate that the developed QCA circuits provide advantages compared to other QCA circuits in terms of double and single cell missing defect, area and delay time.*

Key words: *Nanoelectronics, fault-tolerance, majority gate, QCA FA, ripple carry adder, quantum-dot cellular automata*

1. INTRODUCTION

The QCA technology is a promising computing paradigm that has widespread applications in emerging technologies like Carbon Nano Tube Field Effect Transistor (CNTFET) [1, 2, 3] and Silicon On Insulator (SOI) [4, 5]. In addition, it has the capability to provide better performance compared to other technologies such as conventional CMOS technology [6]. The QCA technology was addressed for the first time by Lent et al. [7]. This technology presents a novel computation and information transformation method [8, 9, 10]. The four-dot square cell is the fundamental unit in the QCA technology, which contains two free electrons [9, 11, 12]. Thus, there exist two stable arrangements for QCA cell. These two arrangements are denoted as cell polarization. Interconnection among the electrons of intercell can make logic '1' and logic '0'. So, the logical states can be computed with the charge configuration of the QCA cell [8, 13]. The basic components in this technology are QCA Majority Gate (MG), QCA Inverter Gate (IG) and QCA wire [9, 14]. This technology has received extensive attention due to the immense practical

Received March 21, 2019; received in revised form June 18, 2019
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applications such as QCA multiplexer [8, 9, 11], QCA multiplier [15], efficient design of QCA Full Adder (FA) [10, 15-35], comparator [14, 36] and shift register [37].

On the other hand, the FA circuit is an inseparable component in the computer arithmetic circuits. Hence, efficient QCA FA construction design is an interesting research topic. The 1-bit QCA FA construction can be designed by employing MG and IG in the QCA technology [10].

The QCA Fault Tolerance (FT) circuit design is also an interesting and necessary in the QCA technology [38-47]. Hence, in order to present the developed digital circuits for future modern computing, many researchers have worked on the characteristics of FT in the QCA full adder constructions.

In this paper, novel 3-input MG is proposed to offer high fault tolerance for double and single missing cell defects. Next, a novel 1-bit FT QCA FA circuit is developed using the developed 3-input MG. In addition, novel 4-bit FT QCA RCA construction is designed using the developed 1-bit FT QCA FA. The developed QCA constructions are implemented with QCADesigner tool version 2.0.3. The simulation results confirm that the developed QCA constructions have considerable advantages compared to other designs.The paper progresses as follows: In section 2, an overview of the QCA technology is presented. Then, the proposed design for new 3-input FT MG, 1-bit QCA FT FA construction, and 4-bit QCA FT RCA construction are presented in section 3. The simulation results and comparison with related works are discussed in section 4. Finally, conclusion is given in section 5.

2. BACKGROUND

2.1. QCA cell

The four-dot squared cell is the fundamental unit in the QCA technology, which contains two free electrons [6]. These electrons occupy two of these four quantum dots due to electrostatic repulsion and diagonally occupy corners of the cell [18]. Thus, there exist two stable arrangements for QCA cell, which are shown in Fig. 1 [9]. These two arrangements are denoted as cell polarization. Interconnection among the electrons of intercell can be shown as logic ‘1’ and logic ‘0’. The logical state in this construction is defined by using the electrons position in quantum dots [20].

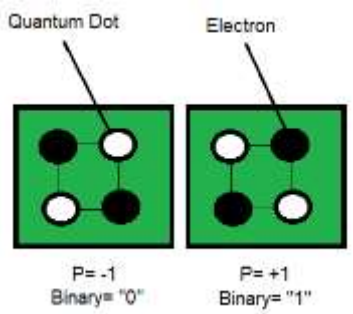

Fig. 1 The polarizations of the QCA cell [9]

2.2. The QCA gates

The MG, XOR and the IG are indispensable building blocks of QCA circuits [48]. Fig. 2 shows a 3-input MG, an IG and XOR gate [12, 48].

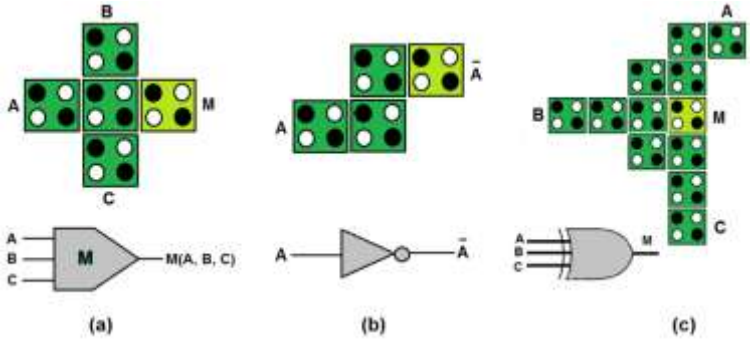

Fig. 2 The basic gates in the QCA technology (a) majority gate, (b) inverter gate, (c) exclusive-OR gate [12, 48]

The 3-input MG logical function is defined as follows [11]:

$$M(A, B, C) = BA + CA + BC \tag{1}$$

The majority gates can work as 2-input OR gates or 2-input AND gates by applying 1 or -1 to one of the inputs, respectively [8].

2.3. The QCA FA

The full adder is an important part of computer arithmetic circuits. If we have A, B, and C_{in} as the inputs, and Carry and Sum as the outputs of 1-bit full adder, the Sum and the Carry outputs can be computed as follows [20]:

$$Cout = \text{Maj } 3(A,B,C_{in}) = AB+AC_{in}+BC_{in} \tag{2}$$

$$SUM = A \oplus B \oplus C_{in} \tag{3}$$

2.4. Defect in QCA circuits

As it is shown in Fig. 3, the defects can be occurred during positioning of the cells to a surface or synthesis in cellular layout of the QCA circuits [29]. In generally, they can be categorized as follows:

- Cell omission (missing cell): In this case, the location of the QCA cell is changed from its original position [44, 45]. The cell omission is displayed in Fig. 3(b).
- Cell displacement: In this case, the QCA cell lost its original direction [41]. The cell displacement defect is displayed in Fig. 3(c).
- Cell misalignment: In this case, the faults are occurred where the QCA cells are shifted from their intended locations [45]. The cell misalignment is displayed in Fig. 3(d).

- Extra (additional) cell: In this case, an extra cell is erroneously deposited on the substrate [29]. The extra cell defect is displayed in Fig. 3(e).
- Cell dislocation or cell rotation: This fault is occurred where QCA cells are rotated proportionate to the other cells in the array [40, 46]. Fig. 3(f) shows this defect.

$$\text{Fault Tolerance (\%)} = \frac{\text{Number of wrong output patterns}}{\text{Number of detective patterns}} \times 100 \tag{4}$$

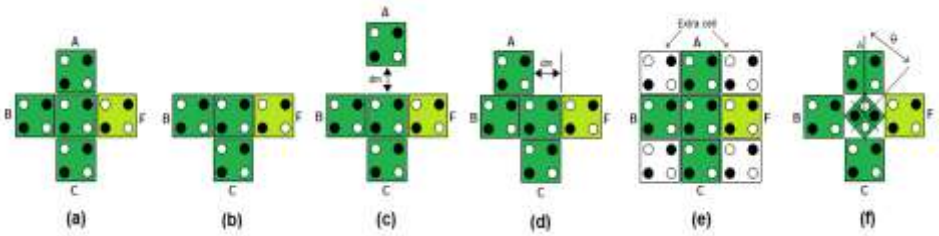

Fig. 3 Defects in the QCA circuits, (a) Fault-free majority gate, (b) Cell omission, (c) Cell displacement, (d) Cell misalignment, (e) Extra cell, (f) Rotation defect [29]

2.5 Related works

A majority gate is a vital component for 1-bit QCA full adder constructions. Hence, previous MGs and 1-bit QCA constructions are reviewed in this section. Note that, the fault tolerance is calculated as follows [42]:

Based on (4), the maximum fault tolerance in terms of the single missing cell defects is 20% for the conventional MG [42]. Fig. 4 shows the MG construction in [47], with 3×3 tile.

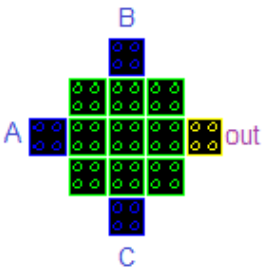

Fig. 4 The utilized MG in [47]

This design has 13 QCA cells. The correct function is 16.67% and 55.6% in terms of the double and single cell missing defects, respectively.

Fig. 5 shows the utilized MG in [42] with 3 × 5 tile. This construction has 19 QCA cells. The number of the correct outputs of this MG is 9 cases out of 15 cases in single cell omission. As a result, it achieves 60% fault tolerance.

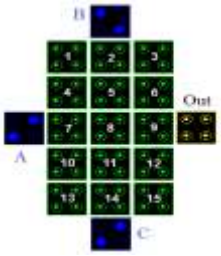

Fig. 5 The utilized MG in [42]

The number of the correct outputs in this MG is 33 cases out of 105 cases in double cell omission. As a result, it achieves 31.4% fault tolerance.

On the other hand, the full adder is an important component in the construction of digital circuits. Roohi et al. [12] have presented 1-bit FT FA by using one 5-input MG, one 3-input MG, and one inverter gate. The percentage of the fault tolerance for the sum and carry outputs are 22.22% and 72.22%, respectively in [12]. This 1-bit FT FA has 0.01 μm^2 area, 23 QCA cells and three clock phases delay. Cho and Swartzlander [17] have presented 1-bit FA that utilizes three MGs and two IGs. This 1-bit FT FA has 0.09 μm^2 area, and four clock phases delay. The fault tolerance for the sum and carry outputs are 32% and 60.49%, respectively in [17]. Du et al. [42] have presented 1-bit FT FA that utilizes one 3-input FT MG, one 5-input MG and one inverter gate. The fault tolerance of the sum and carry outputs are 29.92% and 94.87%, respectively in [42]. The area is 0.08 μm^2 and delay is two clock phases. Kassa and Nagaria [25] have presented 1-bit FA that utilizes one 3-input MG, one 5-input MG and one IG. This 1-bit FA has 0.05 μm^2 area, 48 QCA cells and three clock phases delay. The fault tolerance for the sum output and carry output are 17.94% and 92.30%, respectively in [25]. Hayati and Rezaei [21] have proposed 1-bit FA that utilizes three 3-input MGs and one IG. This 1-bit FA has 0.02 μm^2 area, 38 QCA cells and two clock phases delay. The fault tolerance for the sum output and the carry output are 12.12% and 48.48%, respectively in [21]. Kianpour et al. [22] have presented 1-bit FA that utilizes three 3-input MGs and one IG. This 1-bit FA has 0.07 μm^2 area, 69 cells and three clock phases delay. The fault tolerance for the sum and carry outputs are 12.70% and 71.43%, respectively in [22]. Tougaw and Lent [34] have presented a 1-bit FA that utilizes five 3-input MGs and three inverter gates. This 1-bit FA has 0.2 μm^2 area, 192 cells and five clock phases delay. The fault tolerance for the sum output and carry output are 34.78% and 60%, respectively in [34]. Sen et al. [23] have presented a 1-bit FA that has 0.01 μm^2 area, 31 cells and two clock phases delay. The fault tolerance for the sum output and carry output are 11.54% and 76.92%, respectively in [23]. Angizi et al. [31] have presented a 1-bit FA that utilizes one 3-input MG, one 5-input MG and one IG. This 1-bit FA has 0.09 μm^2 area, 95 cells and five clock phases delay. The fault tolerance for the sum output is 25.55% and for carry output is 74.44%.

3. THE DEVELOPED CONSTRUCTIONS

This section designs a new FT MG as a basic module. Then, a novel 1-bit FT QCA FA and 4-bit FT QCA RCA constructions are implemented using this novel FT MG.

3.1. The proposed FT MG

The proposed construction for the 3-input FT MG is shown in Fig. 6. In this construction, the inputs are denoted by A, B and C, and the output is denoted by Out. The output of the proposed construction is determined as follows [20]:

$$Out = M(A, B, C) = BA + CA + BC \quad (5)$$

In addition, Table 1 shows truth table of the developed 3-input FT MG.

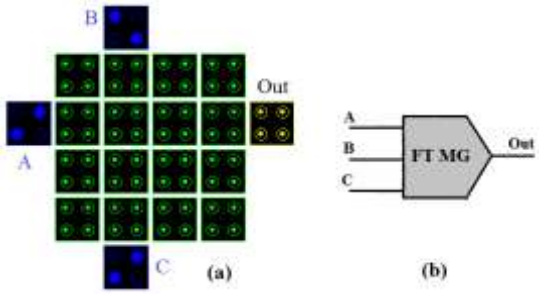

Fig. 6 The proposed 3-input FT MG (a) QCA layout (b) logic diagram

Table 1 Truth table of the proposed FT 3-input MG

A	*B*	*C*	***Out***
0	0	0	**0**
0	0	1	**0**
0	1	0	**0**
0	1	1	**1**
1	0	0	**0**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**

The layout of the proposed 3-input FT MG consists of 20 QCA cells. It also has 0.02 μm^2 area with a 4×4 tile.

3.2. The developed 1-bit FT QCA FA construction

The logical design and layout of the developed 1-bit QCA FT full adder that uses the proposed 3-input FT MG and a 3-input XOR gate as building block, are shown in Fig. 7.

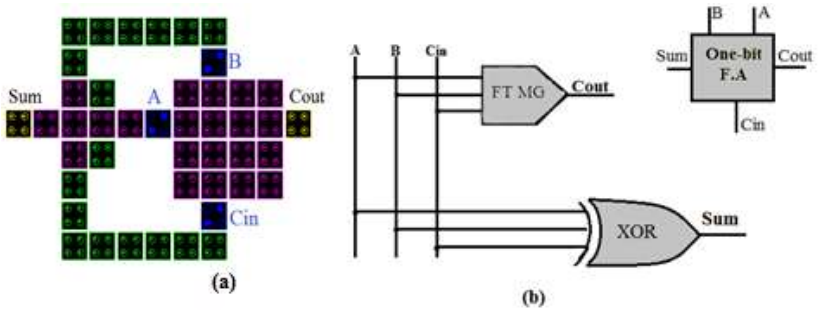

Fig. 7 The proposed 1-bit QCA FT FA (a) QCA layout, (b) logic diagram

As it shown in Fig. 7, the inputs are labeled as A, B and Cin and the outputs are shown by Sum and Cout. The proposed 1-bit QCA FT full adder takes two clock phases to generate the Sum function. The layout of the proposed 1-bit QCA FT full adder includes 44 QCA cells and its occupied area is 0.04 μm^2.

3.3. The proposed 4-bit QCA FT RCA

The logical design and layout of the proposed 4-bit QCA FT RCA are shown in Fig. 8. As shown in Fig. 8, the developed 4-bit QCA FT RCA uses four 1-bit QCA FT full adder modules that is developed in this paper.

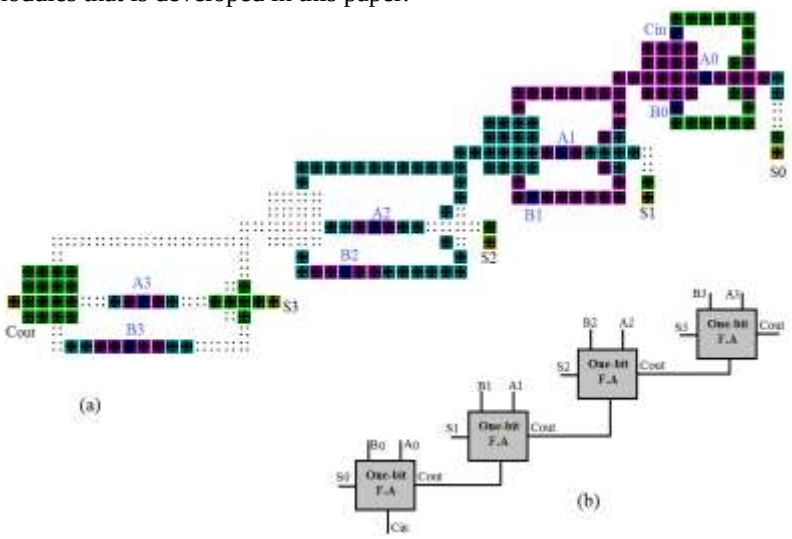

Fig. 8 The proposed 4-bit QCA FT RCA, (a) QCA layout, (b) logic diagram

As it shown in Fig. 8, the inputs are labeled as A (A0, A1, A2, A3), B (B0, B1, B2, B3) and Cin and the outputs are shown by Sum (S0, S1, S2, S3) and Cout. The developed 4-bit QCA FT full adder takes four clock phases to generate the Sum function. The layout of the proposed 4-bit QCA FT RCA consists of 236 QCA cells and its occupied area is 0.49 μm^2.

4. Simulation Results and Comparison

This section presents simulation results and comparison of the proposed FT constructions. The QCADesigner tool version 2.0.3 has been utilized to simulate the proposed constructions.

4.1. The proposed 3-input FT MG

Fig. 9 shows the simulation results of the proposed 3-input FT MG. To fair comparison, the layout of the proposed 3-input FT MG is re-plotted in Fig. 10 in which the QCA cells are shown by number.

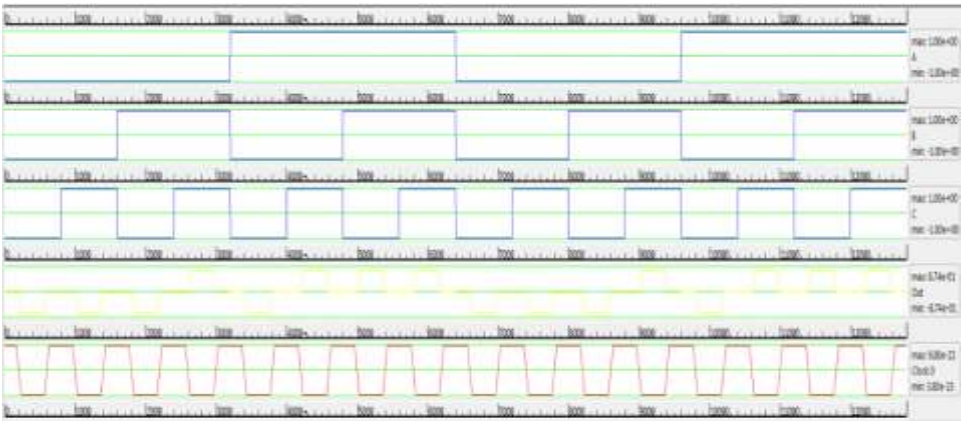

Fig. 9 The output waveform of the designed 3-input FT MG

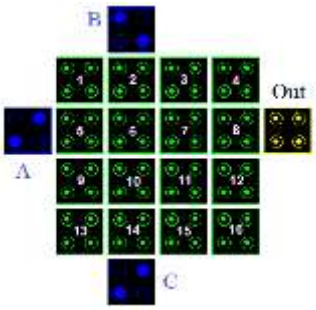

Fig. 10 The proposed MG with cell number

Table 2 shows the simulation results of the 3-input FT MG in terms of the single missing defect. The correct functions and the fault tolerance of the various constructions for the double and single cell missing defects are comparison in Table 3.

Table 2 Single missing cell defect in the proposed 3-input FT MG

Defect cell	Result	Defect cell	Result
1	M(A, B, C) = Correct	9	M(A, B, C) = Correct
2	M(A, B', C) = Incorrect	10	M(A, B, C) = Correct
3	M(A, B, C) = Correct	11	M(A, B, C) = Correct
4	M(A, B, C) = Correct	12	M(A, B, C) = Correct
5	M(A', B, C) = Incorrect	13	M(A, B, C) = Correct
6	C = Incorrect	14	M(A, B, C') = Incorrect
7	C = Incorrect	15	M(A, B, C) = Correct
8	M(A', B', C') = Incorrect	16	M(A, B, C) = Correct

Table 3 The comparative table for the MG for double and single cell missing defects

Reference	(3 × 3-based MG) [47]		(3 × 5-based MG) [42]		This paper	
	One cell missing	Two cells missing	One cell missing	Two cells missing	One cell missing	Two cells missing
M(A, B, C)	5	6	9	33	10	45
Total	9	36	15	105	16	120
Fault Tolerance (%)	55.6%	16.67%	60%	31.4%	62.5%	37.5%

Based on our obtained results that are shown in tables 2 and 3, and Fig. 10, the fault tolerance of the proposed 3-input MG is 62.5% in terms of the single cell missing defect and 37.5% for the double cell missing defect. As a result, the fault tolerance for the double and single cell missing in the proposed 3-input MG are improved compared to MG in [42, 47].

4.2. The developed 1-bit QCA FT FA

The output waveform of the developed 1-bit QCA FT FA are shown in Fig. 11.

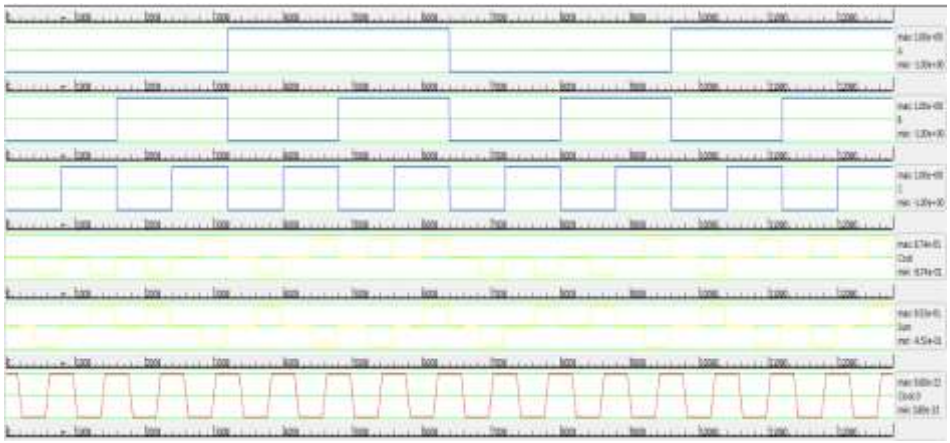

Fig. 11 The output waveform of the developed 1-bit FT QCA FA

The carry output and sum output fault tolerance of the developed 1-bit QCA FT FA are 84.6% and 56.4%, respectively. In addition, the area is 0.04 μm^2 and delay is two

clock phases. Table 4 shows the comparison of the 1-bit QCA FT FA constructers. The cost is calculated as follows:

$$\text{Cost=Area } (\mu m^2) \times \text{Delay (clock phase)} \quad (6)$$

The comparison results between the proposed 1-bit QCA FT FA and other 1-bit QCA FA constructions show that although fault tolerance of the carry output in our design is lesser than the fault tolerance of the carry output in [42, 25], but the fault tolerance of the sum output in the proposed 1-bit QCA FT FA has improved compared to [42, 25]. In addition, the proposed 1-bit QCA FT FA has significant improvement in comparison with [42] in terms of area, and cost by about 50% and 50%, respectively.

It should be mentioned that the percentage improvement is calculated as follows:

$$\text{Improvement } (\%) = \left(1 - \frac{\text{our implemention result}}{\text{previous implemention result}}\right) \times 100 \quad (7)$$

Table 4 Comparative table for 1-bit QCA FA

Reference		[12]	[17]	[42]	[25]	[21]	[22]	[34]	[23]	[31]	This paper
Fault Tolerance (%)	sum	22.22	32.00	26.92	17.94	12.12	12.70	34.78	11.54	25.55	56.4
	carry	72.22	60.49	94.87	92.30	48.48	71.43	60.00	76.92	74.44	84.6
Area		0.01	0.09	0.08	0.04	0.02	0.09	0.20	0.01	0.09	0.04
Delay (clock phase)		3	3	2	2	2	4	5	2	5	2
Cost (Delay ×Area)		0.03	0.36	0.16	0.08	0.04	0.36	1	0.02	0.45	0.08

4.3. The developed 4-bit QCA FT RCA

Fig. 12 indicates the output waveform of the proposed 4-bit QCA FT RCA. For optimum layout, the layout of the proposed 4-bit QCA FT RCA is implemented in only one layer using 236 QCA cells and 0.49 μm^2 area. It also takes four clock phases to generate the outputs.

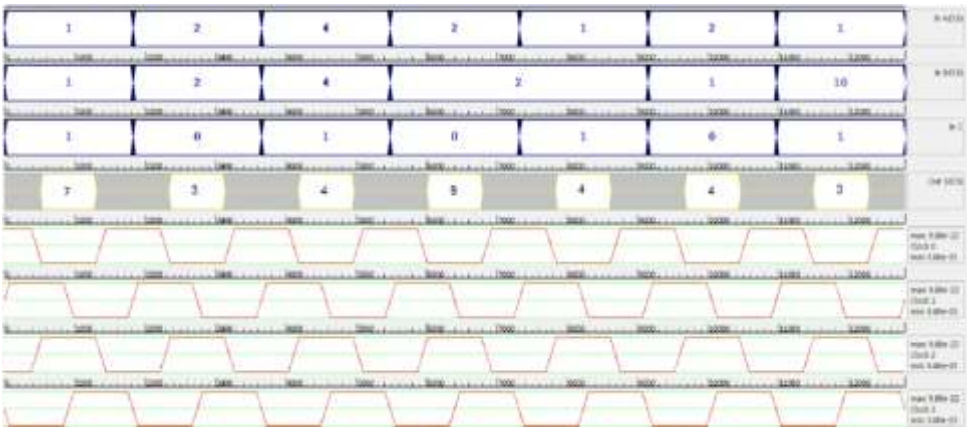

Fig. 12 Simulation results for the proposed 4-bit QCA FT RCA

In order to present a fair comparison, we have compared the proposed 4-bit FT QCA RCA with the existing designs in [12, 17, 32, 33, 42] in terms of the clock phase, occupied area, number of QCA cells and fault tolerance in Table 5.

Based on these results, our design provides a significant reduction on resulting the clock delay, area, number of QCA cells and fault tolerance compared to previous designs in [12, 17, 23, 32, 33, 42]. Moreover, the proposed constructions have significant robustness against the missing cell defects. They can achieve to higher level of fault tolerance. According to equation (8), the 4-bit QCA RCA has approximately 45.2% and 42.8% improvements compared to the presented 4-bit QCA RCA in [42] in terms of the number of QCA cells and clock delay, respectively.

Table 5 Comparative table for 4-bit QCA RCAs

Reference	Number of cells	Area (μm^2)	Delay (clock phase)	Considered fault tolerance
[12]	165	0.18	6	Yes
[17]	371	0.4	6	No
[21]	156	0.18	5	Yes
[42]	431	0.44	7	Yes
[23]	153	0.11	5	No
[32]	308	0.29	8	No
[33]	570	0.68	8	No
This paper	236	0.49	4	Yes

5. CONCLUSIONS

This paper presented and evaluated an efficient 3-input FT MG. The fault tolerance of the proposed 3-input MG has investigated for double and single missing cell defects and compared to previous works. Then, the 1-bit FA and 4-bit RCA have been designed. The developed designs are simulated using QCADesigner tool version 2.0.3. Our simulation results confirm that the proposed 3-input FT MG could reach 62.5% fault tolerance for the single cell missing defect and 37.5% fault tolerance for the double cell missing defect. The proposed 1-bit QCA FT full adder could reach 84.6% and 56.4% fault tolerance for carry output and sum output, respectively. The results show that the developed adder constructions have significant improvements compared to other designs.

REFERENCES

[1] A. Naderi, M. Ghodrati, "Binary An efficient structure for T-CNTFETs with intrinsic-n-doped impurity distribution pattern in drain region", *Turk J Elec Eng & Comp Sci*., vol. 26, no. 5, pp. 2335–2346, 2018.

[2] A. Karimi, A. Rezai, "A design methodology to optimize the device performancein CNTFET", *ECS Journal of Solid State Science and Technology*, vol. 6, no. 8, pp. 97–102, 2017.

[3] M. Shafizadeh, A. Rezai, "Improved device performance in a CNTFET using LaO3high-κ dielectrics", *Journal of Computational Electronics*, vol. 16, no. 2, pp. 221–227, 2017.

[4] M. Zareiee, "A new construction of the dual gate transistor for the analog and digital applications ", *Int. J. Electron. Commun*., vol. 100, no. 1, pp. 114–118, 2019.

[5] A. Naderi, K. Moradi Satari, F. Heirani, " SOI-MESFET with a layer of metal in buried oxide and a layer of SiO2 in channel to improve RF and breakdown characteristics ", *Materials Science in Semiconductor Processing*, vol. 88, no. 1, pp. 57–64, 2018.

[6] M. Zareiee, "A New Structure for Lateral Double Diffused MOSFET to Control the Breakdown Voltage and the On-Resistance", Silicon, https://doi.org/10.1007/s12633-019-0092-5, pp. 1–9, 2019.

[7] C. S. Lent, P. D. Tougaw, W. Porod, G.H. Bernstein, "Quantum cellular automata", *Nano.*, vol. 4, no. 1, pp. 49–57, 1994.
[8] H. Rashidi, A. Rezai, "Design of novel efficient multiplexer construction for quantum-dot cellular automata", *J. Nano Electr. Phys.*, vol. 9, no. 1, pp. 1–7, 2017.
[9] H. Rashidi, A. Rezai, S. Soltany, "High-performance multiplexer construction for quantum-dot cellular automata", J. Comput. Electr., Vol. 15, No. 3, pp. 968–981, 2016.
[10] D. Mokhtari, A. Rezai, H. Rashidi, F. Rabeie, S. Emadi, A. Karimi, "Design of novel efficient full adder construction for quantum-dot cellular automata technology", *Facta Universitatis, Series: Electronics and Energetics*, vol. 31, no. 2, pp. 279–285, 2018.
[11] B. Sen, M. Goswami, S. Mazumdar, B. K. Sikdar, " Towards modular design of reliable quantum-dot cellular automata logic circuit using multiplexers", *Comput. Electr. Eng.*, vol. 45, pp. 42–54, 2015.
[12] A. Roohi, R. F. DeMara, N. Khoshavi, "Design and evaluation of an ultra-area-efficient FT QCA full adder", *Microelectr. J.*, vol. 46, no. 6, pp. 531–542, 2015.
[13] M. Niknezhad Divshali, A. Rezai, S.S. Falahieh Hamidpour, "Design of novel coplanar counter circuit in Quantum-dot cellular automata technology", *In transaction journal of theoretical physics*, 2019.
[14] A Shiri, A Rezai, H Mahmoodian, "Design of efficient coplanar 1-bit comparator circuit in QCA technology", *Facta Universitatis, Series: Electronics and Energetics*, vol. 32, no. 1, pp.119–128, 2019.
[15] I. Edrisi Arani, A. Rezai, "Novel Circuit Design of Serial-Parallel Multiplier In Quantum-dot Cellular Automata Technology", *J. Comput. Electr.*, vol. 17, no. 4, pp.1771–1779, 2018.
[16] H. Roshany, A. Rezai, " Novel efficient circuit design for multilayer QCA RCA", *Int. J. Theor. Phys.*, vol. 58, no. 6, pp. 1745–1757, 2019.
[17] H. Cho, E. E Swartzlander, "Adder and multiplier design in quantum-dot cellular automata", *IEEE Trans Comput.*, vol. 58, no. 6, pp. 721–727, 2009.
[18] Y. Adelnia, A. Rezai, "A novel adder circuit design in quantum-dot cellular automata technology", *Int. J. Theor. Phys.*, vol. 58, no. 1, pp. 184–200, 2019.
[19] M. R. Azghadi, O. Kavehei, K. Navi, "A novel design for quantum-dot cellular automata cells and full-adders", *J. Appl. Sci.*, vol. 7, no. 22, pp. 3460–3468, 2007.
[20] H. Rashidi, A. Rezai, "High-performance full adder construction in quantum-dot cellular automata", *J. Eng.*, vol. 2017, no. 7, pp. 394–402, 2017.
[21] M. Hayati, A. Rezaei, "Design of novel efficient adder and subtractor for quantum-dot cellular automata", *Int. J. Circuit Theor. Appl.*, vol. 43, no. 10, pp. 1446–1454, 2014.
[22] M. Kianpour, R. S. Nadooshan, K. Navi, "A novel design of 8-bit adder/subtractor by quantum-dot cellular automata", *J. Comput. Sys. Sci.*, vol. 80, no. 7, pp. 1404–1414, 2014.
[23] B. Sen, A. Rajoria, B. K. Sikdar, "Design of efficient full adder in quantum-dot cellular automata", *Sci World J.*, vol. 2013, pp. 1–10, 2013.
[24] M. Balali, A. Rezai, H. Balali, F. Rabiei, S. Emadi, " Towards Coplanar quantum-dot cellular automata adders based on efficient three-input XOR gate", *Result Phys.*, vol. 7, pp. 1389–1395, 2017.
[25] S. R. Kassa, R. K. Nagaria, "A novel design of quantum-dot cellular automata 5-input MG with some physical proofs", *J. Comput. Electr.*, vol. 15, no. 1, pp. 324–334, 2016.
[26] R. Farazkish, F. Khodaparast, "Design and characterization of a new FT full adder for quantum-dot cellular automata", *Microprocess Microsyst.*, vol. 39, no. 6, pp. 426–433, 2015.
[27] S. Sheikhfaal, S. Angizi, S. Sarmadi, M. H. Moaiyeri, S. Sayedsalehi, "Designing efficient QCA logical circuits with power dissipation analysis", *Microelecter. J.*, vol. 46, no. 6, pp. 462–471, 2015.
[28] H. B. Sousan, M. Mosleh, S. Setayeshi, "Designing and Implementing a Fast and Robust Full-Adder in Quantum-Dot Cellular Automata (QCA) Technology", *J. Adv. Comput. Res.*, vol. 6, no. 1, pp. 27–45, 2015.
[29] M. Goswami, B. Sen, R. Mukherjee, B. K Sikdar, "Design of testable adder in Quantom-dot Cellular Automata With Fault Secure Logic", *Microelectr J.*, vol. 60, pp. 1–12, 2017.
[30] K. Navi, R. Farazkish, S. Sayedsalehi, M. R. Azghadi, "A new quantum-dot cellular automata full-adder", *Microelectr J.*, vol. 41, no. 12, pp. 820–826, 2010.
[31] S. Angizi, E. Alkaldy, N. Bagherzadeh, K. Navi, " Novel robust single layer wire-crossing approach for exclusive-OR sum of products logic design with quantum-dot cellular automata", *J. Low Power Electr.*, vol. 10, no. 2, pp. 259–271, 2014.
[32] S. Hashemi, M. Tehrani, K. Navi, "An efficient quantum-dot cellular automata full-adder", *Sci. Res. Essays.*, vol. 7, no. 2, pp. 177–189, 2012.
[33] I. Hänninen, J. Takala, "Binary adders on quantum-dot cellular automata", *J. Signal. Proc. Syst.*, vol. 58 no. 1, pp. 87–103, 2010.
[34] P. D. Tougaw, C. S. Lent, "Logical devices implemented using quantum cellular automata", *J. Appl. Phys.*, vol. 75, no. 3, pp. 1818–1825, 1993.

[35] M. Balali, A. Rezai, " Design of low-complexity and high-speed coplanar four-bit ripple carry adder in QCA technology", *International Journal of Theoretical Physics*, vol. 57, no. 7, pp. 1948–1960, 2018.
[36] R. Mokhtarii, A. Rezai, "Investigation and Design of Novel Comparator in Quantum-dot Cellular Automata Technology", *Journal of Nano-& Electronic Physics*, vol. 10, no. 5, p. 05014(4pp), 2018.
[37] M. Niknezhad Divshali, A. Rezai, A. Karimi "Investigation and Design of Novel Comparator in Quantum-dot Cellular Automata Technology", *International Journal of Theoretical Physics*, vol. 57, no. 11, pp. 3326–3339, 2018.
[38] A. Fijany, B. N. Toomarian, "New design for quantum dots cellular automata to obtain Fault Tolerant logic gates", *J. Nano. Res.*, vol. 3, no. 1, pp. 27–37, 2001.
[39] R. Farazkish, K. Navi, "New efficient five-input majority gate for quantum-dot cellular automata", *J. Nano. Res.*, vol. 14, no. 11, pp. 1–6, 2012.
[40] R. Farazkish, S. Sayedsalehi, K. Navi, "Novel design for quantum dots cellular automata to obtain FT majority gate", *J. Nano.*, vol. 2013, pp. 1–7, 2012.
[41] M. Dalui, B. Sen, B. K. Sikdar, "Fault Tolerant QCA logic design with coupled majority-minority gate", *Int. J. Comput. Appl.*, vol. 1, no. 29, pp. 81–87, 2010.
[42] H. Du, H. Lv, Y. Zhang, F. Peng, G. Xie, "Design and analysis of new FT majority gate for quantum-dot cellular automata", *J. Comput. Electr.*, vol. 15, no. 4, pp. 1484–1497, 2016.
[43] B. Sen, M. Dutta, R. Mukherjee, R. K. Nath, A.P. Sinha, B.K. Sikdar, "Towards the design of hybrid QCA tiles targeting high Fault Tolerance", *J. Compu. Electr.*, vol. 15, no. 2, pp. 429–445, 2016.
[44] M. Momenzadeh, M. Ottavi, F. Lombardi, "Modeling QCA defects at molecular-level in combinational circuits", In Proc. IEEE Int. Symp. Defect Fault Tolerance VLSI Syst., 3-5 Oct 2005, pp. 208–216,
[45] Y. Mahmoodi, M. A .Tehrani, "Novel Fault Tolerant QCA Circuits", In Proc. Conf. Electr. Comput. Eng., 20-22 May 2014, pp. 20–22.
[46] M. Rahimpour Gadim, N. Jafari Navimipour "A new three-level Fault Tolerance arithmetic and logic unit based on quantum dot cellular automata", *Microsyst. Technol.*, 2017.
[47] J. Huang, M. Momenzadeh, F. Lombardi, "On the tolerance to manufacturing defects in molecular QCA tiles for processing-by-wire", *J. Electr. Test.*, vol. 23, no. 2-3, pp. 163–174, 2017.
[48] A. Newaz Bahar, Md. Mo. Asaduzzaman, "A novel 3-input XOR function implementation in quantum dot-cellular automata with energy dissipation analysis", *Alexandria Engineering Journal*, vol. 57, no. 2, pp. 729–738, 2018.