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ABSTRACT

An optoelectronic switching network with 2-D optical fiber bundle arrays I/O access device is presented in this paper. A optoelectronic recirculating Banyan network based on CMOS/SEED smart pixel device is used in this configuration. 32×2 single-mode fiber bundle array and 32×2 mutli-mode fiber bundle array are fabricated respectively based on the features of high density, high precision and array permutation of the CMOS/SEED optoelectronic integrated devices. The measuring results show that the center to center spacing between adjacent optical fibers in the same layer of the fiber array is 125um, and the spacing between adjacent layers is 500um. Displacing tolerance of the fiber bundle arrays is less than 2um and the angular tilt error is less than 0.02 degree.

Keywords: Optical switching, 2-D fiber bundle array, CMOS-SEED smart pixel arrays, Optoelectronic integration

1. INTRODUCTION

In recent years, due to continuous progress in optoelectronic devices and VLSI technollogies, hybrid integrated CMOS/SEED (silicon complementary metal oxide semiconductor/self-electro-optic-effect-device) is regarded as one of the extremely attractive optoelectronic device for parallel optical data links through fiber bundle array.[1-3] Due to the demands for increasing bandwidth, large amounts of input data are sent into the optoelectronic switching network and are incidented into the windows of SEED array. As the permutation of the windows of SEED array is regular,[4] 2-D (two-dimension) fiber bundle array device with high precision is needed as I/O access device. In this paper, we propose a novel architecture of optoelectronic circulating Banyan interconnection network switching model based on CMOS/SEED smart pixel switching node array. To ensure that the spot array from the input signal data is imaged upon the array of windows of optoelectronic CMOS/SEED switching node array, a kind of novel architecture of 2-D optical fiber bundle array I/O access device is designed. High precision positing glass box and optical monitor system are used in this method. 32×2 single-mode fiber bundle array and 32×2 mutli-mode fiber bundle array are fabricated respectively based on the features of high density, high precision and array permutation of the CMOS/SEED optoelectronic integrated devices. The measuring results show that the center to center spacing between adjacent optical fibers in the same layer of the fiber bundle array is 125 um, and

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the spacing between adjacent layers is 500um. Displacing tolerance of the fiber bundle arrays is less than 2um and the angular tilt error is less than 0.02 degree. The fabricated 2-D optical fiber bundle array I/O access device can meet the demands of the free-space photonic switching network for high precision in our experiment model.

2. MATRIX DESCRIPTION OF THE BANYAN NETWORK

Free-space optical Banyan network is one of the well-studied multistage regular interconnection networks.[5,6] Schematic diagrams of the Banyan network for $N \times N = 8 \times 8$ (where N is the number of input/output channels) are shown in Fig. 1. Three interconnection stages are needed to construct 8×8 Banyan network. In each stage of the Banyan network, there are a number of switching nodes. Each of them has two possible fan-in and two possible fan-out lines, one corresponds to straight connection while the other to Banyan exchange connection. We define the address of the i-th node in layer j as K_i^j, where i = 0, 1, 2, ..., N-1. At the input of the network, j = 0 while j = 1, 2, and 3, respectively, in the subsequent layers. The output of the i-th node in layer j is either in straight connection or Banyan exchange connection, which are denoted as K_{iS}^j and K_{iB}^j (i = 0, 1, 2, ..., N -1), respectively. The output channel K_{iS}^j or K_{iB}^j of the current stage becomes the input channel K_i^{j+1} of the next stage. The interconnection of the Banyan network can be described as follows.

In the first interconnection stage,

$$K_{Is}^{1} = K_i^0 \quad (i = 0, 1, 2, \ldots, N-1), \tag{1}$$

$$K_{iB}^{1} = \begin{cases} K_{i+N/2}^0 & (i < N/2) \\ K_{i-N/2}^0 & (N/2 \le i < N) \end{cases} \tag{2}$$

In the second interconnection stage,

$$K_{iS}^{2} = K_i^1 \qquad (i = 0, 1, 2, \ldots, N-1), \tag{3}$$

$$K_{iB}^{2} = \begin{cases} K_{i+N/4}^1 & (i < N/4, \quad N/2 \le i < 3N/4) \\ K_{i-N/4}^1 & (N/4 \le i < N/2, \quad 3N/4 \le i < N) \end{cases} \tag{4}$$

In the final interconnection stage,

$$K_{iS}^{3} = K_i^2 \qquad (i = 0, 1, 2, \ldots, N-1), \tag{5}$$

$$K_{iB}^{3} = \begin{cases} K_{i+N/8}^2 & (for \ \ even \ \ i) \\ K_{i-N/8}^2 & (for \ \ odd \ \ i) \end{cases} \tag{6}$$

A matrix theory can be used to make the mathematical analysis of free-space regular optical Banyan interconnection network. The permutation of the input and output channels in each stage can be denoted by a column vector K^j :

$$K^j = (k_0^j, k_1^j, k_2^j, k_3^j, k_4^j, k_5^j, k_6^j, k_7^j)^T \qquad (j = 0, 1, 2, 3) \tag{7}$$

where k_i^j (i = 0, 1, 2, 3, 4, 5, 6, 7) is the order number of the j-th stage. We can describe the operations in every stage of the network with the transform matrix M^j of size 8×8.

$$K^j = M^j K^{j-1} \qquad (j = 1, 2, 3) \tag{8}$$

For the Banyan interconnection network, the representations of matrix M^j are as follows.

In the first stage,

$$M^1 = \begin{vmatrix} n_0^1(s) & 0 & 0 & 0 & n_0^1(c) & 0 & 0 & 0 \\ 0 & n_1^1(s) & 0 & 0 & 0 & n_1^1(c) & 0 & 0 \\ 0 & 0 & n_2^1(s) & 0 & 0 & & n_2^1(c) & 0 \\ 0 & 0 & 0 & n_3^1(s) & 0 & 0 & 0 & n_3^1(c) \\ n_4^1(c) & 0 & 0 & 0 & n_4^1(s) & 0 & 0 & 0 \\ 0 & n_5^1(c) & 0 & 0 & 0 & n_5^1(s) & 0 & 0 \\ 0 & 0 & n_6^1(c) & 0 & 0 & 0 & n_6^1(s) & 0 \\ 0 & 0 & 0 & n_7^1(c) & 0 & 0 & 0 & n_7^1(s) \end{vmatrix} \tag{9}$$

In the second stage,

$$M^2 = \begin{vmatrix} n_0^2(s) & 0 & n_0^2(c) & 0 & 0 & 0 & 0 & 0 \\ 0 & n_1^2(s) & 0 & n_1^2(c) & 0 & 0 & 0 & 0 \\ n_2^2(c) & 0 & n_2^2(s) & 0 & 0 & 0 & 0 & 0 \\ 0 & n_3^2(c) & 0 & n_3^2(s) & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & n_4^2(s) & 0 & n_4^2(c) & 0 \\ 0 & 0 & 0 & 0 & 0 & n_5^2(s) & 0 & n_5^2(c) \\ 0 & 0 & 0 & 0 & n_6^2(c) & 0 & n_6^2(s) & 0 \\ 0 & 0 & 0 & 0 & 0 & n_7^2(c) & 0 & n_7^2(s) \end{vmatrix} \tag{10}$$

In the third stage,

$$M^3 = \begin{vmatrix} n_0^3(s) & n_0^3(c) & 0 & 0 & 0 & 0 & 0 & 0 \\ n_1^3(c) & n_1^3(s) & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & n_2^3(s) & n_2^3(c) & 0 & 0 & 0 & 0 \\ 0 & 0 & n_3^3(c) & n_3^3(s) & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & n_4^3(s) & n_4^3(c) & 0 & 0 \\ 0 & 0 & 0 & 0 & n_5^3(c) & n_5^3(s) & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & n_6^3(s) & n_6^3(c) \\ 0 & 0 & 0 & 0 & 0 & 0 & n_7^3(c) & n_7^3(s) \end{vmatrix} \tag{11}$$

where $n_i^j(c)$ and $n_i^j(s)$ denote the state of the i-th switching node in the j-th stage. They must satisfy the following conditions.

$n_i^j(c) = 1$, and $n_i^j(s) = 0$ for Banyan exchange connection,

$n_i^j(c) = 0$, and $n_i^j(s) = 1$ for straight connection

As a result, the input-output relationship of the crossover interconnection network and the Banyan interconnection network

for $N = 8$ is given by

$$K^3 = M^3 M^2 M^1 K^0 \tag{12}$$

From the formula shown above, we can see that the matrix theory for the multistage banyan interconnect network provides a convenient way to understand the features of the banyan interconnect network.

3. OPTOELECTRONIC RECIRCULATING BANYAN SWITCHING NETWORK

In order to implement optoelectronic recirculating banyan switching network, an optoelectronic switching network model has been constructed which is shown in Fig. 2. It consist of three main parts: one is the free-space optical interconnect network path; Second is the optoelectronic hybrid CMOS/SEED smart pixel array device; Third is 2-D optical fiber bundle array I/O access device. The free-space optical interconnect path is composed of the polarization beamsplitter (PBS), the beamsplitter (BS), the quarter waveplate (QWP), the imaging lenses (L), the binary phase grating (BPG), the reflector (R), and the pumped quantum well semiconductor laser diode (PLD). A flip-chip assembled CMOS/SEED smart pixel array is used as the switching nodes. The SEED array is composed of a number of detectors (receivers) and modulators (transmitters) while the CMOS chip makes efficient logical processing. Input signal light beams are sent into the end of 2-D input fiber bundle array, then travels through high-bandwidth free-space Banyan interconnection network that is implemented by an optical imaging system to form 2-D spot array on the windows of the receivers of the SEED array interface of OE-VLSI chip. Light beam from a semiconductor laser diode is first split into 2-D spot array by a binary phase grating (BPG) splitter which provides the necessary pumped light source for the modulators of the SEED array. After switched by the CMOS/SEED node array, the output signal beams will be sent into the end of 2-D output fiber bundle array to implement the photonic switching. In order to implement the banyan switching network in a recirculating method, a switching logic circuit of the CMOS/SEED smart pixel node array has been designed which is shown in Fig. 3. For a 8×8 channels banyan network, only the 1:4 selector has been used for three stage banyan interconnect network. The input optical signals pass through the free-space optical interconnect network and incident onto the windows of the receiver array on SEED array chip. The input optical signals are first converted to electrical signals through the O/E conversion function of the receivers of SEED pixel array, the converted signals are then fed into the 1:4 selectors of the CMOS logic circuit in a special arrangement. The 1:4 selector has four input ports and one output port, so it can choose one of the four input signals as the output one in a time. The input signals to the 1:4 selector of output channel 0′ come from one of the input channels 0, 1, 2, & 4 in all three interconnect stages; while those to the 1:4 selector of output channel 1′ are from input channels 0, 1, 3, & 5. Similarly, in the last channel, the input signals to the 1:4 selector come from the input channels 3, 5, 6, & 7. The output electrical signals chosen by the 1:4 selectors are converted to optical signals again through the E/O conversion function of the modulators of the SEED pixel array. They are sent to the output channels of the stage. In each recirculating stage of the banyan network, only two of the four input channels are chosen by each 1:4 selector to perform straight or banyan exchange connection according to the requirement of the corresponding interconnection. In the first stage, the output channel 0′ selects input channel 0 when a straight connection is required. Otherwise, input channel 4 is chosen. Similarly, output channel 7′ selects input channel 7 and 3 for straight and exchange connection, respectively. After all the interconnections required in the first stage of the banyan network have been performed, the output optical signals are fed back to the input channels of the recirculating setup. Similar operations are carried out in the subsequent stages until the third one. As a result, the whole multistage banyan interconnection switching network can be realized.

4. 2-D FIBER BUNDLE ARRAY I/O ACCESS DEVICE

As the winders of the SEED receiver/modulator array are permuted regularly and the spacing between windows of the SEED pixel array is multiple of 125μm, the spacing between optical fibers in an optical fiber bundle array must be 125μm, 250μm, or 500μm. In order to meet the optical switching network based on optoelectronic CMOS/SEED smart pixel array device, the 2-D optical fiber bundle array I/O access devices are made and are used in our optical switching experimental model. a novel architecture and assembling technique for two dimensional optical fiber bundle array has been developed. High precision positional glass box is used for assembling optical fiber bundle array. A set of optical monitoring system is set up to control the precision in the process of the optical fiber array adjustment. 32×2 single-mode optical fiber bundle array for input O/I conversion and 32×2 multi-mode optical fiber bundle array for output I/O conversion are fabricated respectively, which are shown in Fig.4 (a) and (b). The center to center spacing between adjacent fibers in a layer is 125μm, and the spacing between two layers is 500μm. In order to examine the precision of the 2-D optical fiber bundle array, a computer-aided CCD image measurement system is used to test the fiber bundle array. The ends of the fiber array are imaged by a CCD image camera and the picture is shown on the screen of the monitor. The spacing between the optical fibers can be measured by shifting the scan line on the screen. Each pixel passed by the scan line has a certain size, so the spacing between optical fibers is confirmed according to the number of the pixels passed from the center of the end of one fiber to the center of the end of the other fiber by the scan line. The measurement results are shown in Fig. 5 (a) to (c). The Fig. 5 (a) is the measuring picture for the spacing between two layers of the optical fiber bundle array. The Fig. 5(b) is the measuring picture for the position error between a pair of relative fibers in different fiber layers. The fig. 5(c) is for the spacing between adjacent fibers in a layer. The measurement results show that the displacement errors in a fiber layer and between two fiber layers are both less than 2μm, and the angular tilt is less than 0.02 degree.

5. CONCLUSIONS

An optoelectronic banyan switching network with a recirculating implementation model has been constructed in this paper. The 2-D single-mode and multi-mode fiber bundle arrays are fabricated and are used in the banyan switching experimental model. The measuring results show that the displacement errors in a fiber layer and between two fiber layers are both less than 2μm, and the angular tilt is less than 0.02 degree. This precision can satisfy the demands of the optoelectronic banyan switching network model based on the CMOS/SEED smart pixel switching node array in our experimental system.

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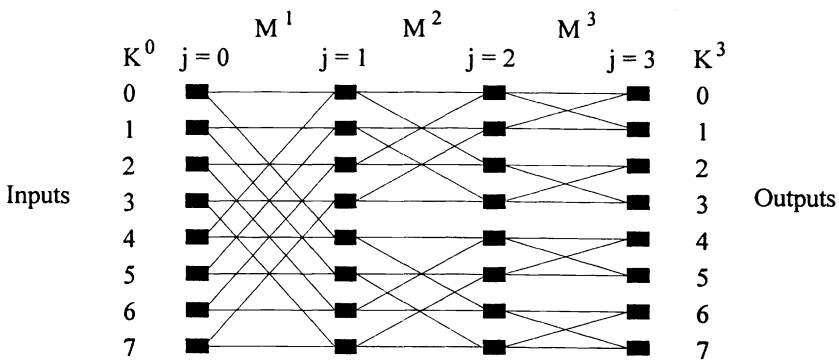


Fig. 1. Schematic diagram of the banyan interconnection network.

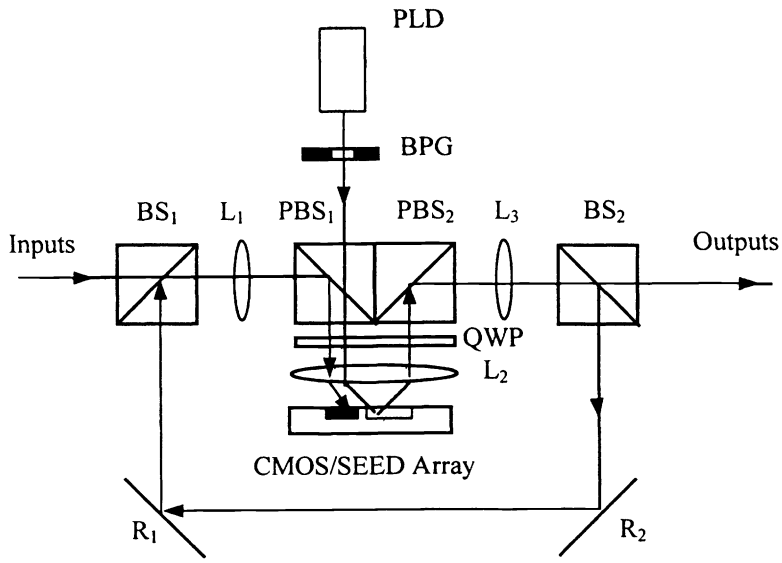
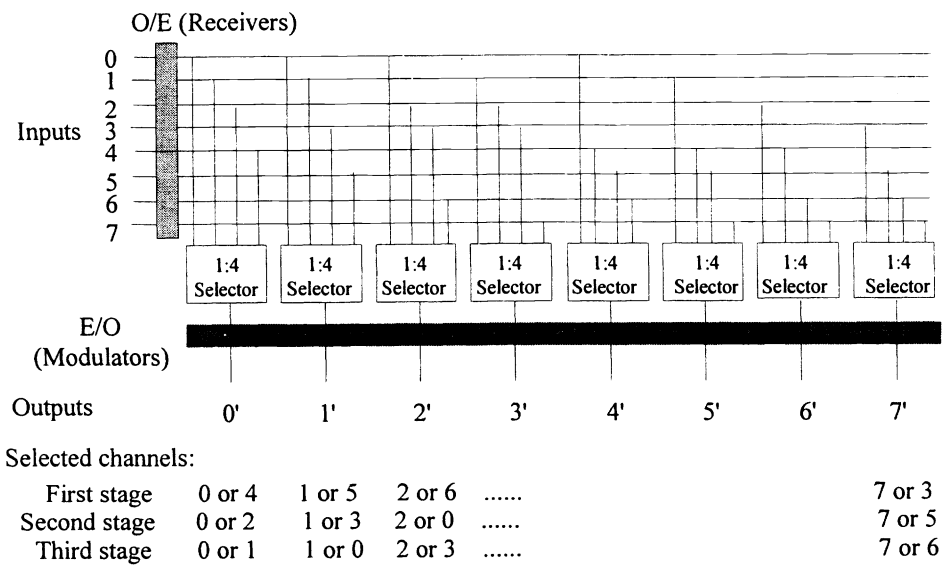


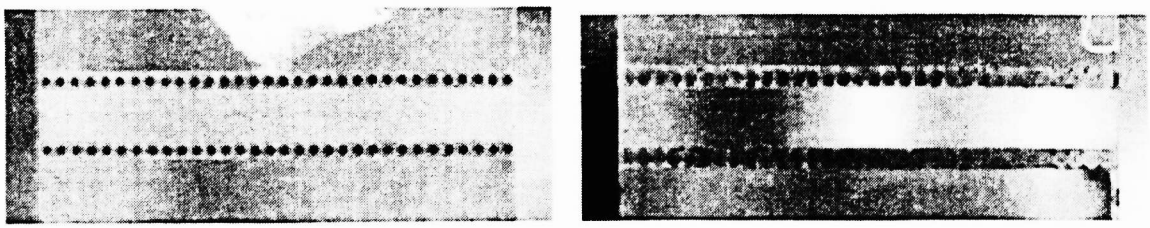
Fig. 2. Optoelectronic switching system of the banyan recirculating network.



Selected channels:

First stage	0 or 4	1 or 5	2 or 6	..... 7 or 3
Second stage	0 or 2	1 or 3	2 or 0	..... 7 or 5
Third stage	0 or 1	1 or 0	2 or 3	..... 7 or 6

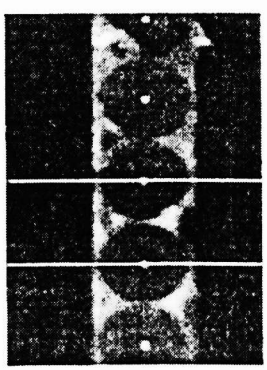
Fig. 3. Schematic diagram of the logic circuit of the CMOS/SEED smart pixel array for banyan network.



(a) (b)

Fig. 4. (a) 32×2 single-mode optical fiber bundle array, and
(b) 32×2 multi-mode optical fiber bundle array.

(a) (b)



(c)

Fig. 5. Measuring pictures of the 2-D optical fiber bundle array.