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Crossover photonic switching network with CMOS/SEED smart pixel device and 2D optical fiber bundle array

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ABSTRACT

A 16×16 Crossover photonic switching network with hybrid integrated CMOS/SEED smart pixel device and 2D optical fiber bundle array I/O access device is reported in this paper. SEED array devices are used as light receivers and transmitters(modulators), while CMOS devices make efficient logical processing. 4×40 2D multilayer optical fiber bundle arrays are fabricated and are used as I/O access devices in the crossover photonic switching network. The center to center spacing between adjacent optical fibers in the same layer of the fiber array is 125 μm , and the spacing between adjacent layers is 250 μm . Displacing tolerance of the fiber bundle arrays is less than 4 μm and the angular tilt error is less than 0.03 degree. It has the feature of high density, high precision, array permutation and easy to couple with 2D CMOS/SEED smart pixel device.

Keywords: Photonic switching; Crossover interconnection network; CMOS/SEED smart pixel devices; 2D optical fiber bundle array

1. INTRODUCTION

Optical interconnection networks are mainly divided into two kind of interconnection ones. One is single stage interconnection network, and the other is multistage interconnection network. In one hand, although single stage interconnection network (such as crossbar network) has the feature of simple construction, the numbers of the switching nodes needed in the interconnection network system are much higher.¹ On the other hand, multistage interconnection network (such as Omega network, crossover network, banyan network) use less numbers of the switching nodes, but the optical hardwares needed in the whole multistage interconnection network are increased greatly because of different interconnection stages.²⁻⁵ If one can find a recirculating method to realize different interconnection stages of multistage interconnection network by using a same single stage optical setup, the optical hardwares used in multistage optical interconnection network will be reduced greatly. In recent years, Owing to rapid evolution in optoelectronic devices and VLSI technologies,⁶⁻⁸ hybrid integrated smart pixel CMOS/SEED (silicon complementary metal oxide semiconductor/self-electro-optic-effect-device) is regarded as one of the extremely attractive optoelectronic device for optical communications, optical computing, photonic switching and information processing. It also supplies a possibility to construct multistage optical interconnection network with single stage circulating setup. In this paper, we propose a kind of optical circulating

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implementation method for the optical crossover switching network with optoelectronic smart pixel devices and 2D optical fiber bundle array. A 16×16 crossover recirculating implementation setup has been constructed. SEED array devices are used as light receivers and transmitters(modulators), while CMOS devices make efficient logical processing. In order to couple with 2D light window array of the SEED device, 4×40 high density multilayer optical fiber bundle array has been fabricated in our experiment. This photonic switching network system has the features of high density, small size, simple architecture and easy to realize.

2. MULTISTAGE CROSSOVER INTERCONNECTION NETWORK

The optical crossover interconnection network is one of the main multistage regular interconnection networks. Schematic diagrams of the crossover network for $N=16$ (where N is the number of input/output channels) are shown in Fig. 1. Four interconnection stages are needed to construct 16×16 crossover network. In each stage of the crossover network, there are a number of switching nodes. Each of them has two possible fan-in and two possible fan-out lines, one corresponds to straight connection while the other to cross exchange connection. We define the address of the i -th node in layer j as K_i^j , where $i = 0, 1, 2, \dots, N-1$. At the input of the network, $j = 0$ while $j = 1, 2, 3$ and 4 , respectively, in the subsequent layers. The output of the i -th node in layer j is either in straight connection or cross exchange connection, which are denoted as K_{iS}^j and K_{iC}^j ($i = 0, 1, 2, \dots, N-1$), respectively. The output channel K_{iS}^j or K_{iC}^j of the current stage becomes the input channel K_i^{j+1} of the next stage. The interconnection of the crossover network can be described as follows.

In the first interconnection stage,

$$K_{iS}^0 = K_i^1 \quad (i = 0, 1, 2, \dots, N-1), \quad (1)$$

$$K_{iC}^0 = K_{N-1-i}^1 \quad (i = 0, 1, 2, \dots, N-1), \quad (2)$$

In the second interconnection stage,

$$K_{iS}^1 = K_i^2 \quad (i = 0, 1, 2, \dots, N-1), \quad (3)$$

$$K_{iC}^1 = \begin{cases} K_{N/2-1-i}^2 & (i < N/2) \\ K_{3N/2-1-i}^2 & (N/2 \leq i < N) \end{cases} \quad (4)$$

In the third interconnection stage,

$$K_{iS}^2 = K_i^3 \quad (i = 0, 1, 2, \dots, N-1), \quad (5)$$

$$K_{iC}^2 = \begin{cases} K_{N/4-1-i}^3 & (i < N/4) \\ K_{3N/4-1-i}^3 & (N/4 \leq i < N/2) \\ K_{5N/4-1-i}^3 & (N/2 \leq i < 3N/4) \\ K_{7N/4-1-i}^3 & (3N/4 \leq i < N) \end{cases} \quad (6)$$

In the final interconnection stage,

$$K_{iS}^3 = K_i^4 \quad (i = 0, 1, 2, \dots, N-1), \quad (7)$$

$$K_{iC}^3 = \begin{cases} K_{i+N/8}^4 & (\text{for even } i) \\ K_{i-N/8}^4 & (\text{for odd } i) \end{cases} \quad (8)$$

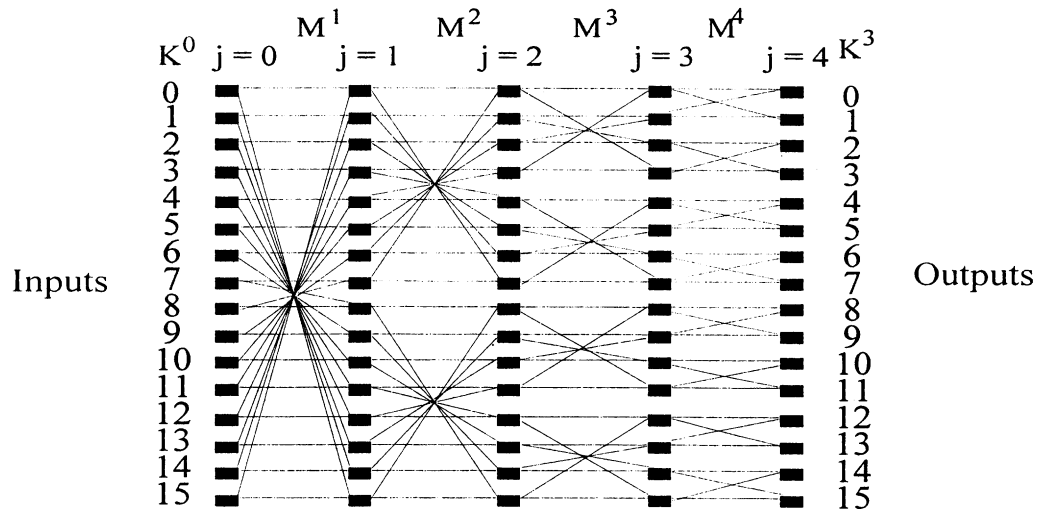


Fig. 1. Schematic diagrams of the four stage crossover network for $N=16$

3. RECIRCULATING IMPLEMENTATION OF CROSSOVER SWITCHING NETWORK

In order to implement optoelectronic recirculating crossover switching network, an optoelectronic switching network module has been constructed which is shown in Fig. 2. It consists of three main parts: one is the free-space optical interconnect network path; Second is the optoelectronic hybrid CMOS/SEED smart pixel array device; Third is 2D optical fiber bundle array I/O access device. The free-space optical interconnect path is composed of the polarization beamsplitter (PBS), the quarter waveplate (QWP), the imaging lenses (L), the binary phase grating (BPG), and the pumped quantum well semiconductor laser diode (PLD). A flip-chip assembled CMOS/SEED smart pixel array is used as the switching nodes. The SEED array is composed of a number of detectors (receivers) and modulators (transmitters) while the CMOS chip makes efficient logical processing. Input signal light beams are sent into the end of 2D input fiber bundle array, then travel through high-bandwidth free-space crossover interconnection network that is implemented by an optical imaging system to form a 2D spot array on the windows of the receivers of the SEED array interface of OE-VLSI chip. Light beam from a semiconductor laser diode is first rectified and collimated, then split into a 2D spot array by a binary phase grating splitter (BPG) which provides the necessary pumped light source for the modulators of the SEED array. After switched by the CMOS/SEED node array, the output signal beams will be sent into the end of 2D output fiber bundle array to implement the photonic switching. In order to implement the 16×16 crossover switching network in a recirculating

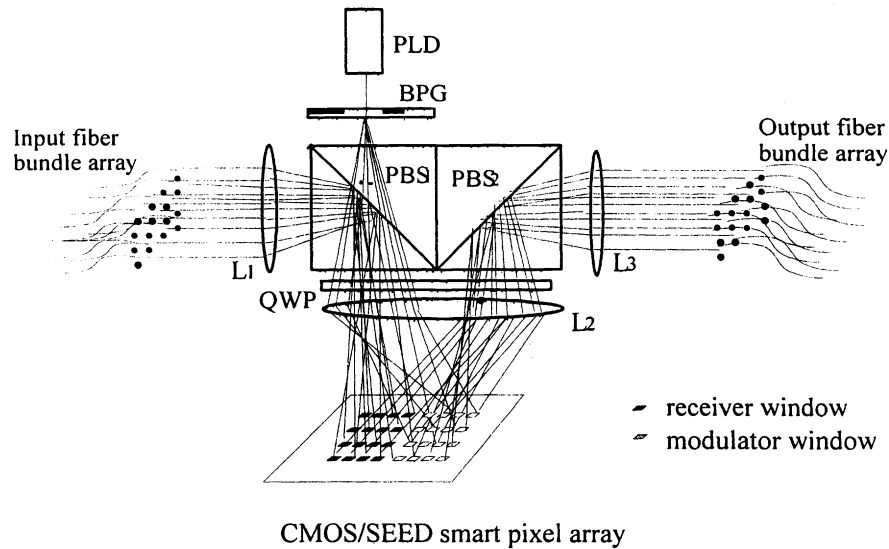


Fig. 2. The crossover optoelectronic switching network

method, a switching logic circuit of the CMOS/SEED smart pixel node array has been designed which is shown in Fig. 3. For a 16×16 channels crossover network, only the 1:5 selector has been used for four stage crossover interconnect network. The input optical signals pass through the free-space optical interconnect network and incident onto the windows of the receiver array on SEED array chip. The input optical signals are first converted to electrical signals through the O/E conversion function of the receivers of SEED pixel array, the converted signals are then fed into the 1:4 selectors of the CMOS logic circuit in a special arrangement. The 1:5 selector has five input ports and one output port, so it can choose one of the five input signals as the output one in a time. The input signals to the 1:5 selector of output channel $0'$ come from the input channels 0, 1, 3, 7, & 15 in all four interconnect stages; while those to the 1:5 selector of output channel $1'$ are from the input channels 0, 1, 2, 6, & 14. Similarly, in the last output channel, the input signals to the 1:5 selector come from the input channels 0, 8, 12, 14, & 15. The output electrical signals chosen by the 1:5 selectors are converted to optical signals again through the E/O conversion function of the modulators of the SEED pixel array. They are sent to the output channels of the stage. In each recirculating stage of the crossover network, only two of the five input channels are chosen by each 1:5 selector to perform straight or cross exchange connection according to the requirement of the corresponding interconnection. In the first stage, the output channel $0'$ selects input channel 0 when a straight connection is required. Otherwise, input channel 15 is chosen. The output channel $1'$ selects input channel 1 when a straight connection is required. Otherwise, input channel 14 is chosen. Similarly, output channel $15'$ selects input channel 15 or input channel 0 for straight or exchange connection, respectively. After all the interconnections required in the first stage of the crossover network have been performed, the output optical signals are fed back to the input channels of the recirculating setup. Similar operations are carried out in the subsequent stages until the fourth one. As a result, the whole multistage crossover interconnection switching network can be realized. In order to comparison, a switching logic circuit of the CMOS/SEED smart pixel node array for the single stage crossbar interconnection network is shown in Fig. 4. The 1:16 selector must be needed for 16×16 crossbar interconnect network in this constructure. The numbers of the logic gates in the crossbar switching network is

much larger than the numbers of the logic gates in the crossover switching network. Therefore, the optoelectronic recirculating crossover switching network based on the CMOS/SEED smart pixel array device has the advantages over the crossbar switching network.

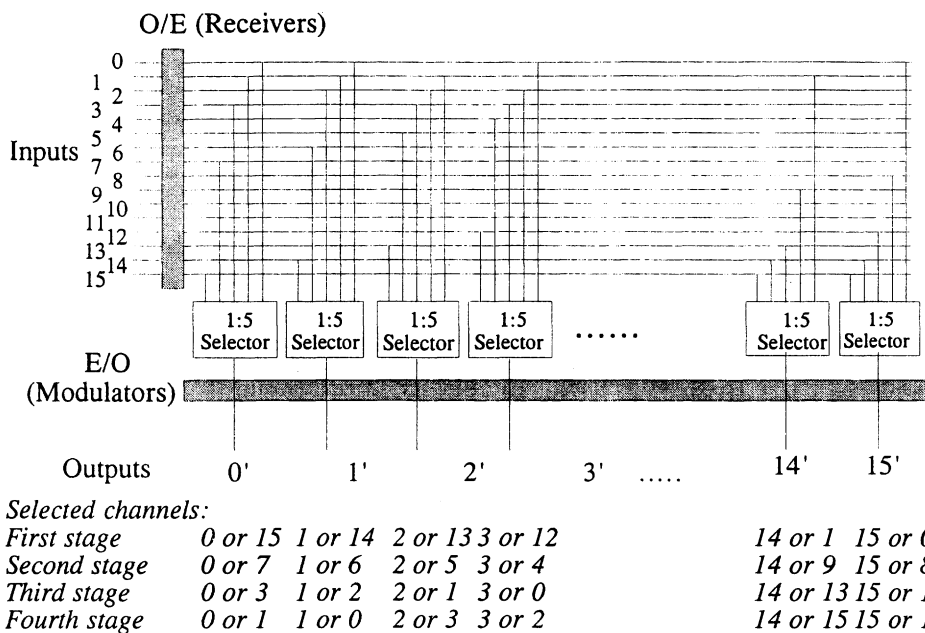


Fig. 3. Switching logic circuit of the CMOS/SEED smart pixel node array for the crossover network

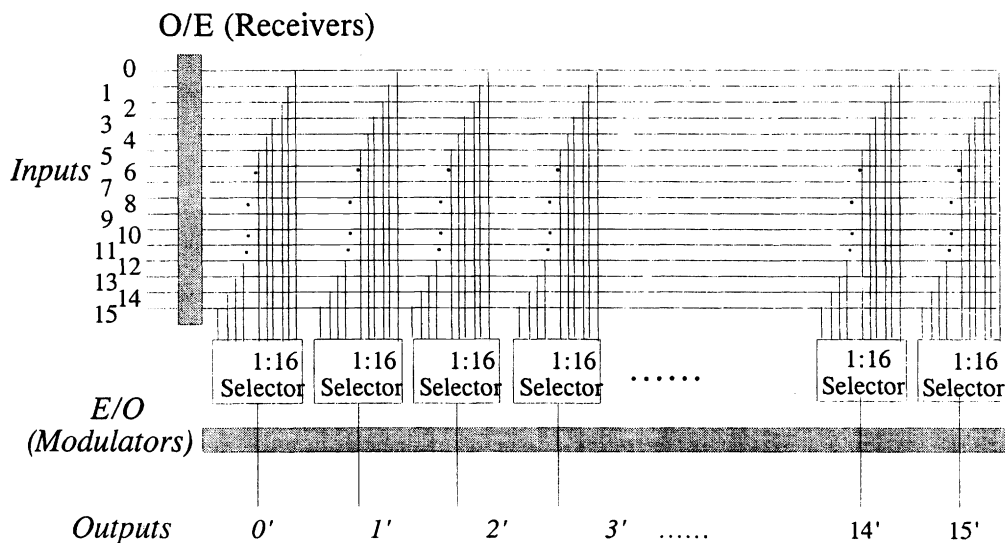


Fig. 4. Switching logic circuit of the CMOS/SEED smart pixel node array for the crossbar network

4. 4×40 MULTILAYER FIBER BUNDLE ARRAY I/O ACCESS DEVICE

As the demands for bandwidth increasing in photonic switching network, large amounts of input data are sent into the photonic switching network and are incidented to the windows of SEED array, then output modulated data signals after switching. As the permutation of light windows of the SEED array is regular, 2D optical fiber arrays are required for I/O access. In order to couple with 2D light window array of the SEED device, on the basis of 2×32 optical fiber bundle array, 4×40 high density multilayer optical fiber bundle array has also been fabricated in our experiment. a novel architecture and assembling technique for two dimensional optical fiber bundle array has been developed. High precision positional glass box is used for assembling optical fiber bundle array. A set of optical monitoring system is set up to control the precision in the process of the optical fiber array adjustment. The micrograph of the ends of 4×40 single-mode optical fiber bundle array are shown in Fig.5. The center to center spacing between adjacent fibers in a layer is $125\mu\text{m}$, and the spacing between two layers is $250\mu\text{m}$. In order to examine the precision of the 2D optical fiber bundle array, a computer-aided CCD image measurement system is used to test the fiber bundle array. The ends of the fiber array are imaged by a CCD image camera and the picture is shown on the screen of the monitor. The spacing between the optical fibers can be measured by shifting the scan line on the screen. Each pixel passed by the scan line has a certain size, so the spacing between optical fibers is confirmed according to the number of the pixels passed from the center of the end of one fiber to the center of the end of the other fiber by the scan line. The measurement results show that the displacement errors in a fiber layer and between two fiber layers are both less than $4\mu\text{m}$, and the angular tilt is less than 0.03 degree. In our

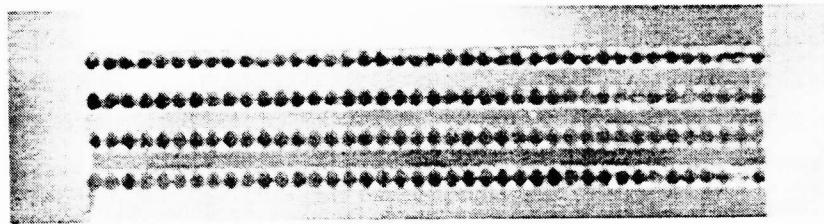


Fig. 5. Micrograph of the ends of 4×40 optical fiber bundle array

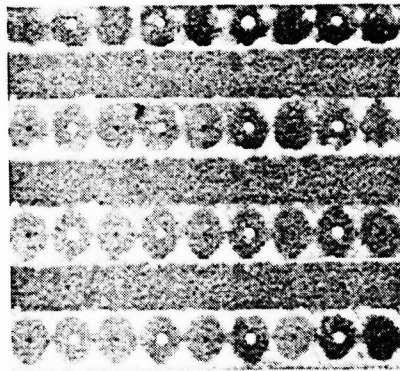


Fig. 6. Micrograph of 4×4 light spots from 2D fiber bundle array

experiment system, only 16 (4×4) data channels are needed. We can only choose 4×4 optical fiber array from 4×40 optical fiber bundle array as the I/O access of the CMOS/SEED smart pixel array. The micrograph of 4×4 light spots from 2D optical fiber bundle array is shown in Fig. 6.

5. CONCLUSIONS

A 16×16 optical recirculating implementation of CMOS/SEED optoelectronic integrated crossover switching network with 2D optical fiber bundle array is presented in this paper. The CMOS/SEED smart pixel arrays with O/E light windows are used as logical controlling switch nodes. High-precision 2D optical fiber bundle arrays are used as the I/O access devices. 4×40 high density multilayer optical fiber bundle array is fabricated. 16×16 optical crossover switching network is constructed using single stage recirculating setup.

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