RELATIVELY LOW-TEMPERATURE PROCESSING AND ITS IMPACT ON DEVICE PERFORMANCE AND RELIABILITY

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Non-silicon, large-area/flexible electronics for the internet of things (IoT) has acquired substantial attention in recent years. Key electron devices to enable this technology include metal-oxide-semiconductor field effect transistors (MOSFETs), where ultra-thin and/or low-dimensional (i.e., 2D to a few layers) semiconductor materials may be required, like those found in thin-film transistors (TFTs) and transition metal dichalcogenide (TMD) FETs [1,2]. Whether TFT or TMDFET, a relatively low-temperature process commensurate with large-area/flex applications to enable large (i.e., greater than 300 mm) and/or flexible substrate fabrication is required. Furthermore, TMD materials may be implemented as the channel semiconductor to function as an ultra-thin body to mitigate short channel effects and extend further scaling as the future progresses in CMOS scaling. In addition, the gate dielectric insulator is another vital component of any MOSFET that requires investigation as part of the MOS stack in these types of transistors. Lastly, semiconductor materials mentioned herein do not have a universally accepted way to introduce dopants to form sources and drains. Thus, metal-semiconductor contacts are employed where the interface region of the contact plays a critical role in determining the conductivity/resistivity of the contact. Moreover, how the metal-semiconductor interface are formed also impacts the quality of the contact. Therefore, exploration of low-temperature processing, interfaces, and their impact on device performance and reliability will be critical to eventual implementation in future technologies. To ascertain the impact of low-temperature fabrication and critical interfaces, several process approaches and electrical characterization methods were employed [1-6]. In one case, for a TMD FET contact study, an oxygen plasma exposure in the contact region on MoS_2 (a TMD material) is done prior to titanium deposition. The results demonstrate that contaminants and photoresist residue that still reside after development can noticeably impact electrical performance (Fig. 1). The O_2 plasma removes the residue present at the surface of MoS_2 without the use of a high temperature anneal, and subsequently improves the device performance significantly (Fig. 1) [1]. In another case, for a MOS-based TFT study, an investigation of low-temperature (> 115°C) deposited zinc-based semiconductors was executed (Fig. 2). For ZnO and IGZO, saturation mobilities of 14.4 and 8.4 cm^2/V-s, along with threshold voltages of 2.2 V and 2.0 V were obtained, respectively, demonstrating robust devices that also have an on/off ratio > 10^8, with I_{OFF} lower than 10^{-12} A. Furthermore, a hot carrier stress methodology demonstrated threshold voltage (V_{TH}) shifts of 0.4 V and 1.8 V for ZnO and IGZO, respectively, after stress (Fig. 2) [2]. Continued research is required to ascertain the electrically active defects responsible for the V_{TH} shift.

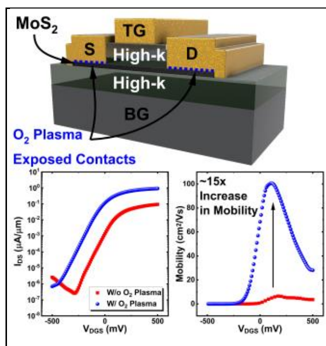

Fig. 1. MoS_2 TMD FET with and without an oxygen plasma treatment, where clear benefits are obtained from having the S/D contact regions exposed to an oxygen plasma prior to metal deposition.

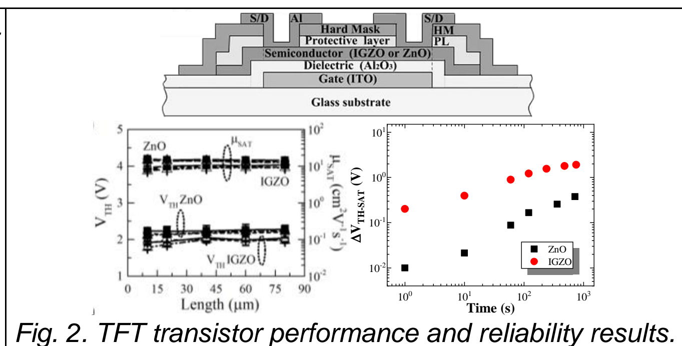

Fig. 2. TFT transistor performance and reliability results.

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