# RELIABILITY OF FLEXIBLE LOW TEMPERATURE POLY-SILICON THIN FILM TRANSISTOR

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Key Words: Flexible LTPS TFT, Mechanical bending stress, Abnormal hump

This work reports the effect of mechanical stress-induced degradation in flexible low-temperature polycrystalline-silicon thin-film transistors. After 100,000 iterations of channel-width-direction mechanical compression at R=2mm, a significant shift of extracted threshold voltage and an abnormal hump at the subthreshold region were found. Simulation reveals that both the strongest mechanical stress and electrical field takes place at both sides of the channel edge, between the polycrystalline silicon and gate insulator. The gate insulator suffered from a serious mechanical stress and result in a defect generation in the gate insulator. The degradation of the threshold voltage shift and the abnormal hump can be ascribed to the electron trapping in these defects. In addition, this work introduced three methods to reduce the degradation cause by the mechanical stress, including the quality improvement of the gate insulator, organic trench structure and active layer with a wing structure.

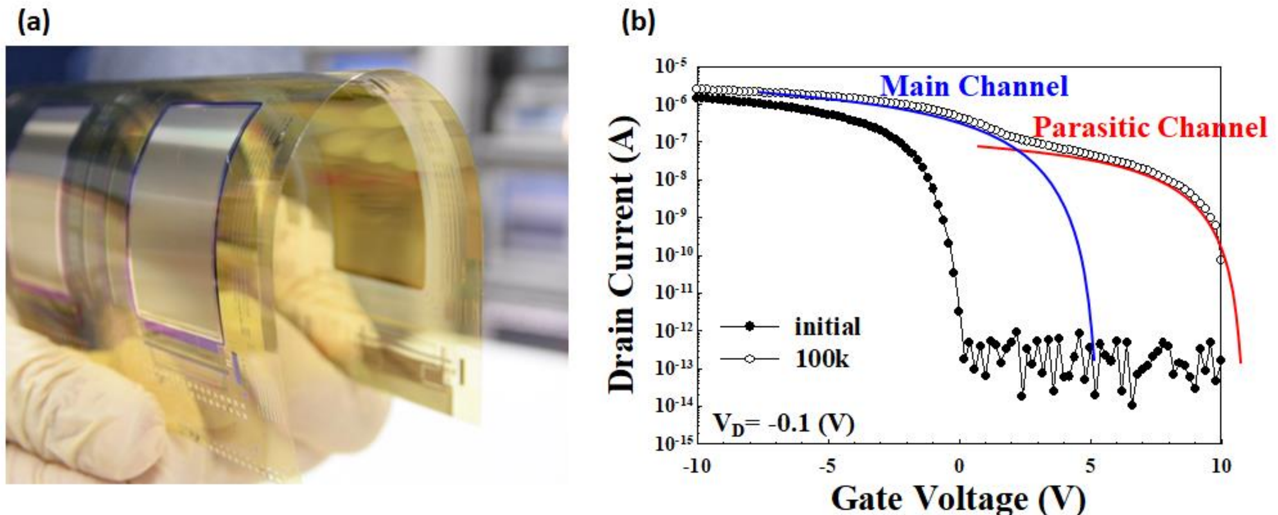


*Figure 1 – (a)Photo of our flexible LTPS TFT. (b)$I_D$-$V_G$ transfer characteristics with $V_D$=-0.1V for devices undergoing 100,000 iterations of width-axis compression bending.*