FLASH LAMP ANNEALED POLYCRYSTALLINE SILICON AS A POTENTIAL CANDIDATE FOR LARGE PANEL MANUFACTURING

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The flat-panel display industry is in pursuit of TFT manufacturing processes which are cost-effective, easily scalable to large glass panels, and meet the performance requirements of advanced display products. While excimer laser anneal (ELA) low-temperature polycrystalline silicon (LTPS) can offer exceptional TFT performance, a lower grade LTPS may still satisfy product requirements at a lower production cost. Flash-Lamp Annealing (FLA) is an emerging candidate for the manufacture of LTPS. Multi-lamp exposure systems with high repetition pulse rates would potentially offer significant advantages in manufacturing throughput and cost over ELA. Techniques to overcome challenges that have hindered device scaling and reduction in variation of device operation are under investigation. The following presents a status update on the development of FLA Polycrystalline Silicon (FLAPS) technology.

The FLA equipment used for this work was a NovaCentrix PulseForge 3300 system, capable of uniform exposure of a 7 cm x 12 cm area at intensities as high as 50 kW/cm^2 over microseconds pulse duration. PMOS TFTs were fabricated using combinations of FLA, ion implantation and furnace annealing to define the source/drain and channel regions. Predefined polygons of 60 nm thick amorphous silicon vertically sandwiched between layers of SiO_2 were crystallized on Corning Lotus NXT display glass using single-pulse FLA exposure. The amorphous silicon melts while absorbing a sufficient fraction of the xenon emission spectrum, and becomes polycrystalline while staying within the thermal constraints of the underlying glass substrate. Boron dopant ions were implantation into the source/drain regions defined by lithographic patterning or a self-aligned gate strategy. Boron activation was realized by combinations of FLA, furnace annealing, and pre-amorphization using an electrically inactive species. FLA conditions following dopant introduction avoided silicon melting which causes significant lateral diffusion. Representative electrical characteristics are shown in figure 1. While the device operation demonstrates a general dependence on the degree of dopant activation, observations on the electrical characteristics indicate a complex relationship between defect states and the specific implant/activation strategy applied. The influence of doping strategy on both device performance and resistance to failure is the primary focus of this work. Additional experiments involving variations in the FLAPS morphology will also be discussed.

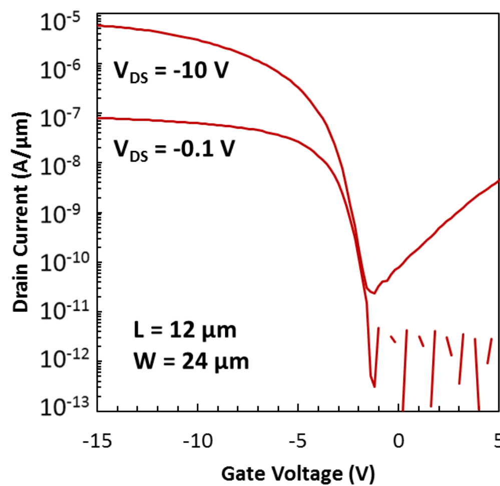

Figure 1 – I_D-V_{GS} Transfer Characteristics of FLAPS PMOS TFT which utilized $^{28}Si^+$ pre-amorphization prior to boron introduction and activation