

INVESTIGATION OF DEGRADATION CAUSED BY CHARGE TRAPPING AT ETCHING-STOP LAYER UNDER AC GATE-BIAS STRESS FOR InGaZnO THIN FILM TRANSISTORS

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A great amount of literatures has been focusing on bias-induced instability issues including threshold voltage shift (ΔV_t) and subthreshold swing (S.S) degradations [1]. However, in practical TFT operation circuits, very limited knowledge could be applied since operation modes are mostly applied with alternative current (AC). Based on these backgrounds, in this work, Indium-Gallium-Zinc-Oxide Thin Film Transistors (IGZO TFTs) are applied with AC PBS degradations. Compared with previous work, this work observed a structure dependent degradation. An etch-stop structure IGZO TFT observed a serious threshold voltage shift after AC stress but shown great stability after direct current (DC) stress. The device structure and transfer characteristic curves are demonstrated in Figure 1(a) and (b) respectively. From results of DC PBS/NBS, a favorable stability indicating a great quality of gate insulator. Therefore, the positive threshold voltage shift is believed to be origin from electron trapping at the etching stop layer (ESL), since ESL possesses a relatively poor quality compared to the gate insulator. The charge trapping at etching stop layer could be confirmed by results of asymmetric source/drain metal under AC stress, illustrated in Figure 1(c).

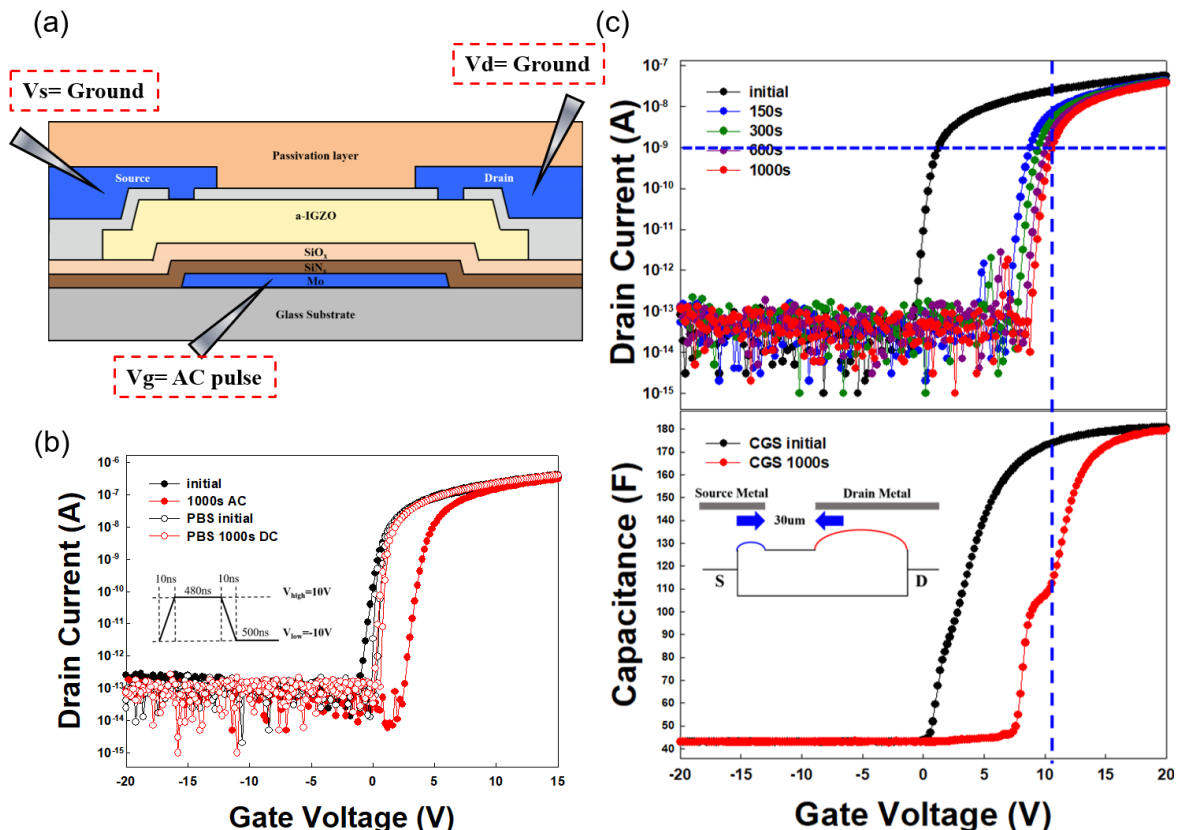


Figure 1 – (a) Cross-section of etching-stop layer a-IGZO TFT (b) Transfer characteristic curve of before and after both AC and DC PBS (c) Transfer characteristic curve of asymmetric source/drain metal after 1000s AC PBS stress. The blue line indicates the turn on voltage of I_d - V_g matches to the turn on of C-V curve.

Reference:

[1] Lee, Jeong-Min, et al. "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors." *Applied Physics Letters* 93.9 (2008): 093504