MECHANISM OF THERMAL FIELD AND ELECTRIC FIELD IN RESISTIVE RANDOM ACCESS MEMORY USING THE HIGH/LOW-K SIDE WALL STRUCTURE

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In the Internet of things (IoT) era, low power consumption memory will be a critical issue for further device development. Among many kinds of next-generation memories, resistive random access memory (RRAM) is considered as having the most potential due to its high performance. To prevent unrecoverable hard break-down of a RRAM device, the RRAM should be collocated with a transistor for external current compliance. With decreasing device cell size, however, the operating voltage of the transistor will become smaller and smaller. Previous study has determined that the forming voltage of RRAM increases when device cell size is reduced, which is a very crucial issue especially when the device is scaled down. We have proposed a high-k sidewall spacer structure in RRAM to solve the dilemma of increasing forming voltages for device cell scaling down. Based on the COMSOL-simulated electrical field distributions in the high-k RRAM. In addition, thermal conductivity of sidewall spacer influenced resistive switching behavior. Suitable thermal conductivity of sidewall materials can enhance resistive switching behavior.

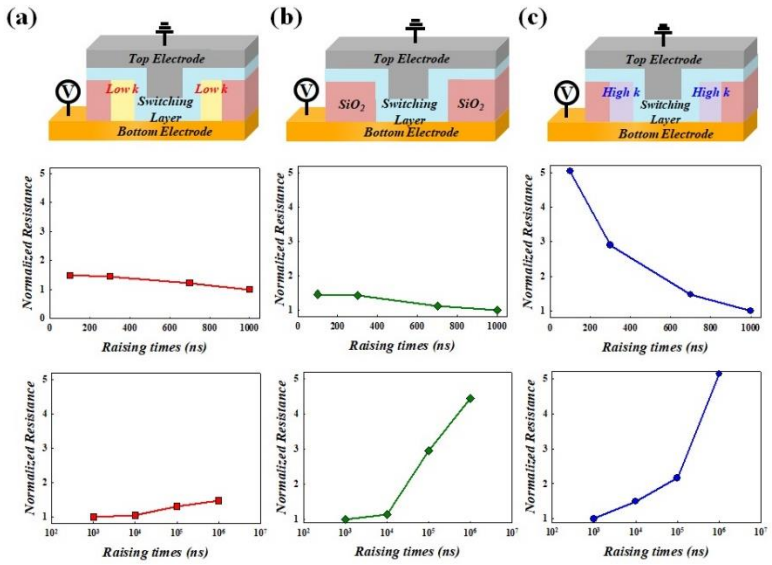

Figure 1 – Increasing forming voltage of scaling down is solved by varying permittivity of the switching layer. Three devices were fabricated by RF-sputter, including (a) Low-k, (b)SiO_2 and (c)High-k side walls. After applying reset process with fast IV of Waveform Generator/Fast Measurement Unit (WGFMU), the trend of HRSs of low-k and SiO_2 side walls was slowly, and the trend of HRSs of high-k side walls increased during the rising time decreasing. As rising time increased between 1us to 100us, the trend of SiO_2 and high-k side walls was upward. In contrast, the trend of low-k side wall was slowly.

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