

RELIABILITY OF PLASMA-ETCHED COPPER LINES ON A GLASS SUBSTRATE

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Copper (Cu) thin films can be etched into 0.3 micrometer Cu patterns, as shown in Figure 1. This process has been used in the fabrication of large-area thin film transistor (TFT) arrays for LCDs, interconnect lines in high density BiCMOS circuits, and source, drain and gate electrodes of a-Si:H TFTs (1,2). The reliability of the Cu line is usually investigated with the isothermal electromigration (EM) method (3).

In almost all studies, the Cu line was prepared on the silicon substrate coated with a dielectric layer. There are few studies on Cu line lifetime on the glass substrate. Also, the EM failure investigation was focused on the line broken time, which could be influenced by the edge roughness, step coverage, current density, etc. (4). The physical and structure changes of the Cu line during the EM stress time are often neglected (5). In this paper, authors discuss the application of the plasma etched Cu line for the SSI-LED array. It allows the driving of the individual device for light emitting at specified conditions, which enables applications in displays, optical interconnects, etc. The transformation of the Cu line from a continuous pattern to the broken state will be reviewed. The temperature change with respect to the stress current density and the lifetime will be discussed. In summary, the room temperature plasma-based Cu etch process can be applied to a wide range of electronic and optoelectronic products. The understanding of the reliability of the Cu line is important for these applications.

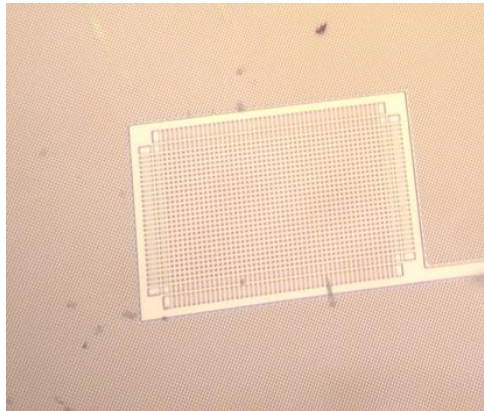


Fig. 1. 0.3 micrometer Cu pattern etched with the plasma-based process.

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