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DESIGN OF A MACHINE VISION CAMERA FOR SPATIAL AUGMENTED REALITY

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DESIGN OF A MACHINE VISION CAMERA FOR SPATIAL AUGMENTED REALITY

THESIS

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering in the College of Engineering at the University of Kentucky

By
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Lexington, Kentucky 2018

ABSTRACT OF THESIS

DESIGN OF A MACHINE VISION CAMERA FOR SPATIAL AUGMENTED REALITY

Structured Light Imaging (SLI) is a means of digital reconstruction, or Three-Dimensional (3D) scanning, and has uses that span many disciplines. A projector, camera and Personal Computer (PC) are required to perform such 3D scans. Slight variances in synchronization between these three devices can cause malfunctions in the process due to the limitations of PC graphics processors as real-time systems. Previous work used a Field Programmable Gate Array (FPGA) to both drive the projector and trigger the camera, eliminating these timing issues, but still needing an external camera. This thesis proposes the incorporation of the camera with the FPGA SLI controller by means of a custom printed circuit board (PCB) design. Featuring a high speed image sensor as well as High Definition Multimedia Interface (HDMI) input and output, this PCB enables the FPGA to perform SLI scans as well as pass through HDMI video to the projector for Spatial Augmented Reality (SAR) purposes. Minimizing ripple noise on the power supply by means of effective circuit design and PCB layout, realizes a compact and cost effective machine vision sensing solution.

KEYWORDS: Image Sensor, Machine Vision, PCB Design, Spatial Augmented Reality

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Date: December 14, 2018

DESIGN OF A MACHINE VISION CAMERA FOR SPATIAL AUGMENTED REALITY

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Date: December 14, 2018

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Chapter 1 Introduction

Creating a three dimensional (3D) digital representation, or digital reconstruction, of an object using Structured Light Illumination (SLI) is an active area of research [5, 6]. SLI enables the determination of an object's profile by measuring the warping that occurs when a series of stripes are cast onto the object. A system which employs this method of 3D scanning includes three main components: a light source (usually a projector); a camera; and a control module. This component overview is shown in Fig. 1.1.

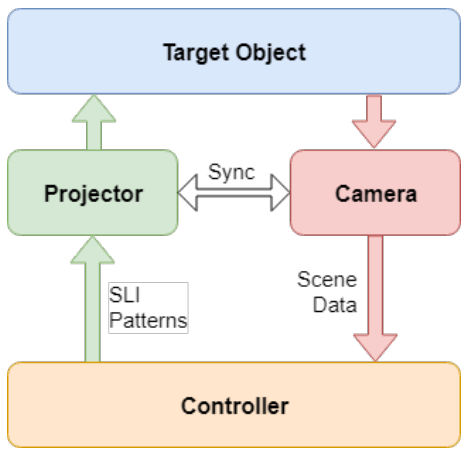

Figure 1.1: High level visualization of a typical SLI scanner.

Current industrial state of the art solutions incorporate all three major system components into one package, but can cost over $24,000 as in the Artec3D scanner [7]. The components of such industrial 3D scanners can be purchased individually for a significantly lower price. In this way, equivalent 3D scanning solutions can be realized using Commercial off the Shelf (COTS) projectors and machine vision cameras [8].

The timing between the projecting light source and camera is critical to the success of SLI as a method of digital reconstruction. In order for SLI to correctly operate, the camera must capture one, and only one, frame of projected pattern. If the camera exposure does not fall within the time when a single pattern is being projected, the captured image will include multiple patterns and the reconstruction efforts will fail. This creates a challenge: camera synchronization.

The solution is to use a Field Programmable Gate Array (FPGA) to drive the projector. Camera hardware triggers can be directly interfaced to the Programmable Logic (PL) fabric of the FPGA. With this method, timing requirements are more easily met rather than by simply connecting the projector to a PC [9]. This also relieves the host PC from generating structured light patterns. One limitation to this setup is that by eliminating the video link from PC to projector and using an FPGA to generate patterns, the ability to send custom video directly to the projector is sacrificed.

Typical commodity projectors do not offer hardware interfaces for determining when a particular frame of video will be shown on the target. The only way to determine when a frame of video is projected is from PC software. A convenient video interface in modern projectors is the High-Definition Multimedia Interface (HDMI) standard. This leaves the task of camera synchronization to the host PC, however the PC has no way of knowing when a particular frame is displayed since Graphics Processing Units (GPUs) are not real-time devices. There is no way of knowing or controlling the delay between or number of times a particular frame might get repeated [10].

This user-video pass-though to the projector, namely the projector of an SLI scanning system, facilitates an ongoing area of research known as Spatial Augmented Reality (SAR) [11, 12, 13]. In scanning the target object with structured light, a mapping between scene coordinates and projector coordinates is created. Video pass-through functionality is then utilized to "paint" the scene or render relevant information onto an object or surface.

Since there is now a need for video pass-through, why not use HDMI as the only connection to the machine vision camera system other than the method by which video frames are received from the sensor (e.g. USB3 or Gigabit Ethernet). We propose using an FPGA to multiplex HDMI video, enabling a versatile SAR system powered by 3D reconstruction by means of SLI. All HDMI signals must then pass through the FPGA, by which it derives its own pixel clock via PLL. This synchronizes all FPGA operations, which includes camera synchronization, to the host PC. This eliminates timing variations that could occur when using a PC to communicate with the projector and machine vision sensor separately. Such a system would be able to synchronize the camera exposures needed for 3D scanning, as well as remove the problems of GPU timing and camera synchronization, solving both problems.

Adding HDMI input and output connections to a machine vision sensor enables several other benefits besides solving synchronization issues between host PC, SLI pattern generation and camera exposure. By hijacking display identification protocols within the HDMI standard, namely the Extended Display Identification Data (EDID) channel [14], camera features like automatic enumeration, part identification, and daisy chain synchronization can be realized.

A state of the art SAR/SLI Scanner Controller developed at the University of Kentucky that supports the aforementioned pattern generation and display identification features is shown in Fig. 1.2. This system is based on the MojoV3 FPGA and utilizes this HDMI pass-though technology to synchronize the PC, projector and camera. The connectors on the right of the figure are for interfacing with machine vision cameras. It also sports two HDMI ports for input and output.

Based on machine vision cameras already making use of an FPGA for image sensor interfacing, this thesis proposes a machine vision image sensing system with dual HDMI ports for the purpose of synchronization provides an FPGA based SLI controller with a local high speed machine vision camera for SLI scanning and HDMI pass-through for SAR. This is achieved by designing, creating and populating a Printed Circuit Board (PCB) which stacks on an FPGA equipped Single Board Computer System-on-a-Module (SoM). Combining the image sensor, HDMI interface and

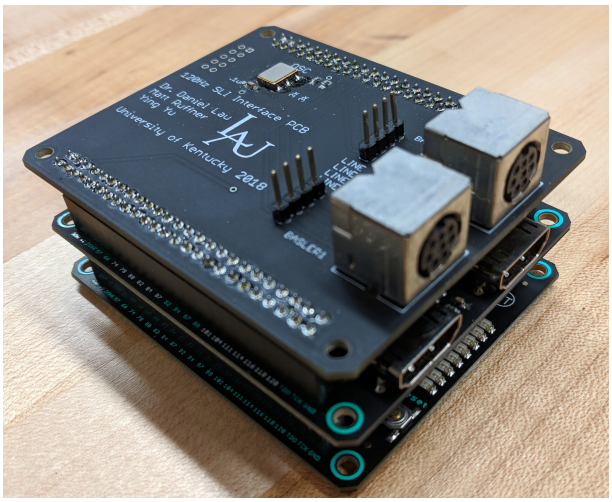

Figure 1.2: SLI Scanner + SAR Controller with external camera interface.

SLI pattern generation aspects of a traditional SAR setup creates a novel machine vision sensing solution by combining the camera and projector control logic.

The proposed ***Smart Camera with SAR Controller*** is a highly integrated device comprised of several subsystems to handle separate tasks. By designing custom interface circuitry, several commodity components are combined into a single compact solution. A breakdown of which subsystems are comprised of custom circuitry and which are COTS components is shown in Table 1.1.

Table 1.1

Subsystem	Implementation
Communication Subsystem	Avnet MicroZed Single Board Computer
Vision Subsystem	LUPA300 VGA CMOS Image Sensor
Power Delivery Subsystem	Custom Printed Circuit
Projector Control Subsystem	Custom Printed Circuit

Table 1.1: The different subsystems which comprise the proposed machine vision SAR controller.

For the communication subsystem, an Avnet MicroZed System on a Module (SoM) is chosen. This SoM features an integrated Zynq 7010 which has an Artix-7 FPGA and dual core ARM-A9 processor capable of running embedded Linux, with underlying connections to the FPGA. This creates a software interface for collecting and processing image data received from the vision subsystem. A 100MBit Ethernet port on the MicroZed enables high speed transfer of video frames back to the host PC. A picture of the ZedBoard can be seen in Fig. 1.3

The LUPA300 VGA CMOS camera module is chosen as the vision subsystem due to its ability to operate at a sufficiently high frame rate and Non-Destructive Readout (NDR) capability. Sufficiently high is defined as greater than 120fps since the highest

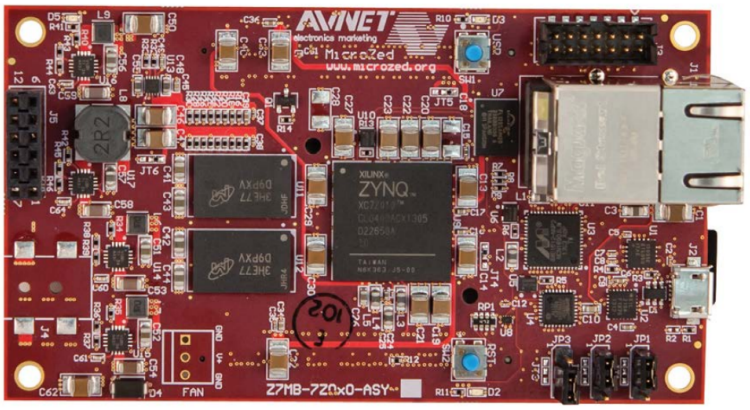

Figure 1.3: The MicroZed board, featuring the Zynq-7010 SoC

speed at which commodity projectors are able to operate is 120Hz when outputting video over HDMI. In this way, the system will be able to utilize the full capacity of modern high speed commercial projectors. Using an image sensor which supports NDR capability enables High Dynamic Range (HDR) imaging applications [15]. Using this HDR technology in SLI applications can lower the Signal to Noise Ratio (SNR) of the resultant scan, facilitating a more precise SAR projection mapping.

Interfacing with the control and communications subsystem requires provision of custom power supply and start-up sequencing that monitors system power-up signals from the MicroZed. This circuitry comprises the Power Delivery (PD) subsystem and also contains the low noise Power Delivery Network (PDN) for the vision subsystem.

The final component of the design is the integrated projector controller. It is responsible for providing an interface by which HDMI video may be received and transmitted. In order to achieve this, a 2 port HDMI interface was added to the PCB design for the MicroZed carrier card which houses the vision and PD subsystems. The finished product is a four layer PCB, hosting the image sensor, HDMI ports and MicroZed interface. The PCB, shown in Fig. 1.4, also filters and supplies power to the image sensor and MicroZed.

Having outlined the necessary components of the system, it is clear that there are several high speed digital interfaces as well as the analog processes, i.e. vision subsystem, that need to be supported on the same carrier card. This poses several design challenges in terms of PCB and electrical design, not to mention the inherent space limitation of wanting to make the package the same size as the MicroZed board.

Across three iterations of image sensor interface and power supply circuitry, significant reduction in power supply noise is achieved. Implementing effective supply bypassing and filtering techniques as well as informed PCB routing schemes achieves a 17-fold reduction in power supply ripple. This reduction in supply noise is sufficient to achieve good-quality images from the LUPA300 image sensor, verifying the operation of the communications and vision subsystems. Projector control subsystem verification by means of HDMI output is also confirmed operational. FPGA control logic has not yet been implemented to test HDMI input for full projector control subsystems verification.

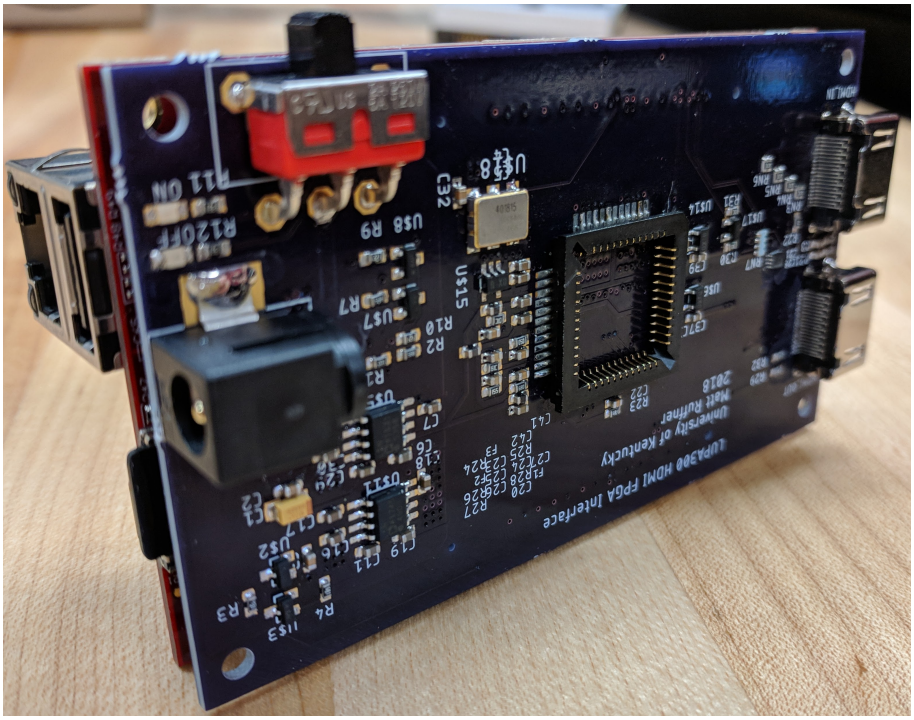

Figure 1.4: The final populated PCB

The main challenge faced in the design and testing of this system was obtaining a good quality image from the vision subsystem. Noise created by the connections between vision and communication subsystems induced noise into the power delivery subsystem, directly affecting image quality. The following chapters of this thesis outline the electrical and PCB design choices made in order to minimize power supply noise, as well as showcase the final design of the system and proof of image quality.

Chapter 2 explains the design of the PD subsystem. This includes the necessary power supply circuitry and start-up sequencing logic for the MicroZed to properly operate as well as the power requirements of the LUPA300 sensor. Also featured in this chapter are the PCB design methodologies for minimizing the coupling of high frequency noise into the PDN. Measurement and quantization of power supply noise reduction across design iterations and the direct correlation with image quality are also shown.

Chapter 3 outlines the projector control subsystem and the circuitry necessary for transmitting and receiving HDMI video. Details of the differential signaling used by HDMI and the PCB layout techniques required to achieve adequate signal integrity when routing are explained in the chapter. Also included is the necessary level shifting circuitry to interface the display identification protocol to the FPGA and generate HDMI pixel clock sources for 120Hz HDMI output.

Chapter 4 explains the operational details of the LUPA300 VGA CMOS image sensor. Details of data output and control interfaces are discussed as well as the interfacing of the sensor to the communication subsystem. This Chapter also includes details about image data transmission schemes via the communication subsystem and

the methodology by which image sensor parameters can be configured on the fly. An overview of prior research performed with this image sensor is included,

Finally, in Chapter 5, the completed work is summarized and novel contributions to the field are stated. A final list of system components and comparison to other smart cameras is included along with a discussion of enhancements that can be made to the presented system.

Chapter 2 Power Management

Ripple in high-speed device power supplies can cause clock jitter that impacts digital systems and can bias sensitive analog circuitry which are part of mixed signal systems. Minimizing the impact that increasingly fast digital systems have on their analog neighbors is necessary for ensuring correct operation of the entire system. The vision and projector control subsystems both contain high frequency data and communication channels with fast switching digital signals. Proper provisions for these fast transitions must be taken to minimize the radiated noise from these signals which can cause interference in other subsystems. The vision subsystem is especially susceptible to this noise as it is a mixed signal integrated circuit (IC) with sensitive analog components.

In this Chapter, the design, layout and implementation details describing an effective low-noise PDN are explained. Quantization of the interference of high speed vision and projector control subsystems on the power subsystem is also discussed, including overheads imposed by the communication subsystem. PCB layer assignments, application specific component selection and the individual power requirements of the communication and vision subsystems are discussed. The circuit schematics and PCB layouts that realize and implement this design on a MicroZed CCC are shown, along with the actual populated, soldered and tested PCBs. A visualization of the design process will also be presented, with an explanation of the improvement in noise immunity of the PDN and in turn the improvement of image quality.

2.1 Background

Several iterations of design and prototype process were performed in order to efficiently interface the LUPA300 sensor to the MicroZed SoM. The MicroZed Breakout Carrier Card (MBCC) was initially used as a prototype, and was eventually replaced. This carrier card can be seen in Fig. 2.1. The headers on either side of the carrier provided a easy-to-use interface for initial circuitry. Replacing the MBCC involved recreating circuitry for the proper supply and sequencing of power to the MicroZed module itself. This section explains the initial circuitry used to interface the LUPA300 to the MBCC as well as the requirements for creating a CcC for the MicroZed.

The correct operation of the LUPA300 image sensor needed to be confirmed first since prior work to create an interface solution yielded unstable output from the sensor. After verification of the sensor, preliminary noise reduction techniques were employed to improve the image quality of the system. Finally, the main hurdle to creating a custom host PCB for the MicroZed platform was recreating the power regulation and conditioning circuitry for the MicroZed. This circuitry was originally hosted on the MBCC. This process also verified that it was feasible to solder the necessary high density board-to-board connectors by hand.

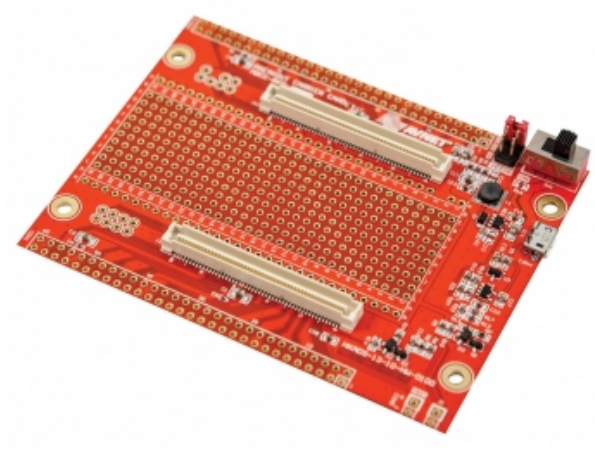

Figure 2.1: The Avnet Breakout Carrier Card allows for quicker prototyping with the MicroZed.

Initial Sensor Evaluation

Several previous attempts had been made to create a viable interface solution between the LUPA300 and MicroZed board, the last of which can be seen in Fig. 2.2, where it is attached to the MBCC. These PCBs, which were fabricated in-house at the University of Kentucky (see Fig. 2.3), had a maximum of two layers and inter-layer connections (vias) which had to be manually populated. This imposed several design overheads that are not incurred when a professional service is utilized.

Since many hours were spent on numerous failed iterations of this in-house design, an initial round of PCBs were first designed in order to verify key signals of operation from the LUPA300 sensor. These signals effectively act like a heartbeat signal and are explained more in Chapter 4. With these signals showing intermittent prevalence on the in-house designs, thoughts were forming that there might be reliability issues with the image sensor itself. For this reason, two versions of this initial sign of life PCB were designed: One for interfacing with the MBCC, and one for interfacing with a Teensy 3.2 ARM CortexM Arduino compatible microcontroller [16].

The choice to create a breakout for the Teensy3.2 was made to ease the sensor verification process. In order to do any testing with an interface for the MBCC, the PL module inside the MicroZed must be configured. This entails a lengthy compilation, synthesis and bitstream generation step to convert Verilog code into a `.bit` file.

Three PCBs were designed as part of this sensor evaluation step. They are listed in Table 2.2. In order to save on routing, an image sensor breakout was made that would facilitate the transfer of one image sensor to the other carrier. In this way, a particular image sensor can be verified in the Teensy configuration, then removed and plugged into the MBCC adapter board for testing with the FPGA based system. This also minimized extraction and insertion counts on a particular sensor, lessening the chance of damage to it.

These three boards are meant to be combined in two configurations in order to interface with both communication controllers i.e a Teensy 3.2 and MBCC. Assembled

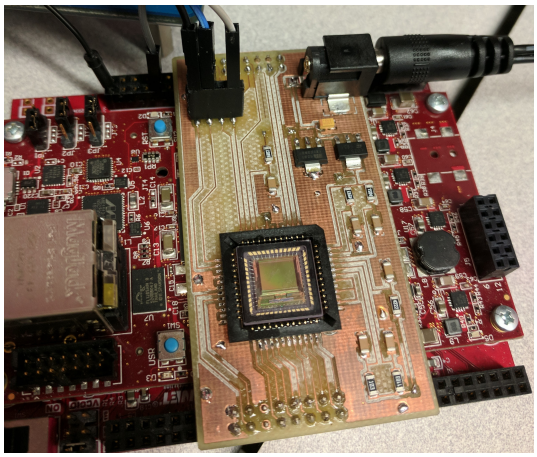

Figure 2.2: Initial LUPA300 interface PCB.

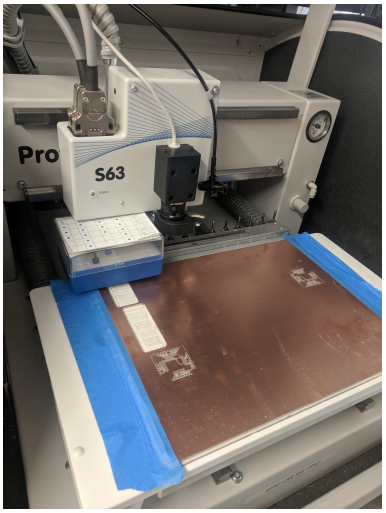

Figure 2.3: Milling machine used to create in-house prototypes.

configurations can be seen in Fig. 2.4 and Fig. 2.5.

Table 2.1

Board name	Purpose
LUPA300 breakout board (BB)	Provide common pin interface
Teensy 3.2 adapter	Interface the LUPA300 BB and Teensy 3.2
MBCC adapter	Interface the LUPA300 and FPGA via MBCC

Table 2.2: Modules part of the initial sensor evaluation prototye PCBs.

During testing of the sensor evaluation platform, a lower frequency clock (4Mhz) was supplied in order to verify the output of several timing signals related to exposure and image data readout from the sensor. This frequency is much lower than the 80MHz clock required to achieve the desired frame rate from the system, however this method confirmed the expected timing and exposure signals from the sensor.

The initial modular prototypes for the Teensy3.2 and MBCC were acceptable to confirm expected timing signals from the LUPA300 image sensor, however they did not possess the Power Supply Noise Supression (PSNR) required to achieve an acceptable image from the sensor.

An adequate level of noise suppression and immunity cannot be realized by including the MBCC in the design. The 0.1” headers on the board introduce too much extra path length in these timing critical signals and cannot be tolerated. For this reason it is necessary to move away from including the handy MBCC in the design, and create a custom carrier card (CCC).

Removing the MBCC created design and technical challenges towards realizing the final system, including testing and evaluation of MicroZed PDN circuitry, as well

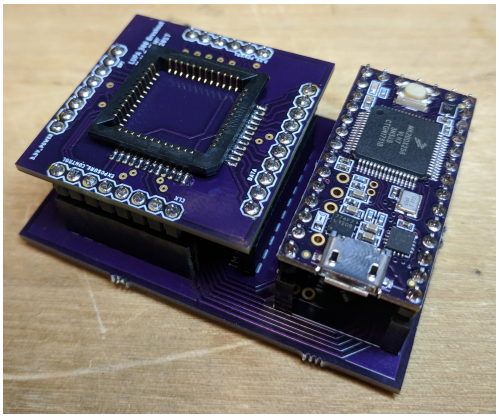

Figure 2.4: Initial testing PCB for interfacing with the Teensy 3.2.

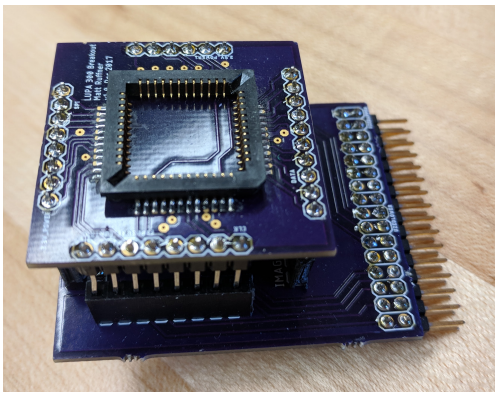

Figure 2.5: Initial testing PCB for interfacing with the MBCC.

as the hand soldering of the high density mezzanine connectors used for interfacing with the MicroZed (MicroHeaders). Each of these 100 pin connectors on the bottom of the Zed board, expose PL input/output (I/O) lines from the FPGA as well as signals for proper sequencing and initialization of the MicroZed board itself.

2.2 Power Requirements

When combining multiple subsystems together, the individual power requirements of each must be considered. The communication subsystem can draw varying amounts of power depending on CPU load and currently utilized peripherals. The vision subsystem's power utilization can vary quickly with time, depending on sensor operating mode. Effective circuit designs are employed to ensure quick changes in current consumption by the sensor subsystem. The projector control subsystem draws little power, compared to the other two subsystems, for nominal HDMI compliance.

In addition to voltage and current requirements, there are also certain timing considerations that must be made in the power-on of the system.

In order to properly support a MicroZed SoM on a CCC, several timing and power requirements must be satisfied. The on-board ARM processor and FPGA on the Zynq SoC require different supplies and must be supplied in a specific order.

The actual boot and FPGA configuration process does not start when power is applied to the board. Instead, there are startup signals exposed on the board-to-board connector on the bottom of the MicroZed. A five volt supply is required before any other voltages i.e. VCC_{IO} are applied to the MicroZed.

The PL module of the FPGA has two banks of I/O pins that can operate at different signal levels, called the VCC_{IO} level. The MBCC provided a jumper to select between several multiple VCC_{IO} levels (3.3v, 2.5v, 1.8v) depending on the end user's application. This functionality is unnecessary in the final application, and was fixed at 3.3v.

Avnet provides documentation for designing a CCC [17]. This documentation contains a plethora of information regarding recommended layout, trace length con-

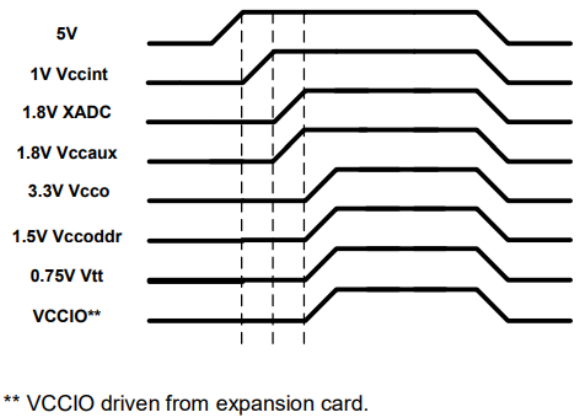

Figure 2.6: Timing diagram showing the necessary order in which regulators must come up at the time of system initialization [1].

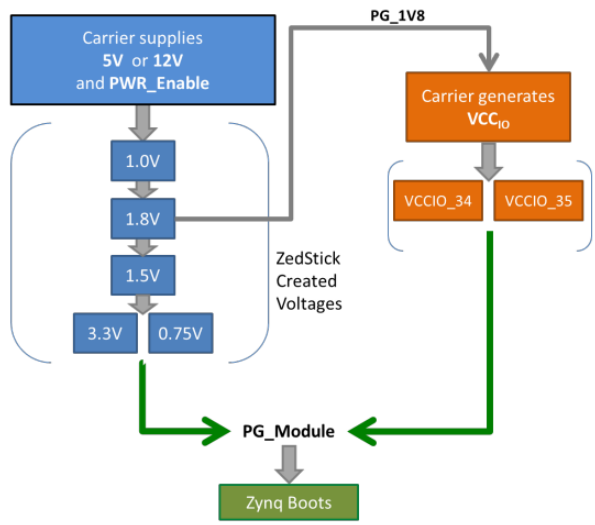

Figure 2.7: On-board power-up sequence of the MicroZed board showing necessary input and output signals to and from the daughter card [1].

siderations and necessary mechanical dimensions relevant when designing such a PCB. Some of the most pertinent information is the start-up timing required to achieve a correct initialization of the MicroZed. For reference, the bring-up order and modules involved in this process are shown in Figs. 2.6 and 2.7, respectively.

The timing diagram also includes the supplies that are on the MicroZed itself. It should be noted that some of these voltages are not exposed on the board-to-board connector, and are of no concern to the design of this system.

The schematics of the MBCC are available online to be used as reference designs [18]. The crucial part of this circuitry adapted for the CCC was that which dealt with system initialization. The *PWR_enable* signal is an input to the MicroZed. It must be kept low to keep the MicroZed in a power off state, even though five volts is already applied to the module by the carrier card. The physical switch on the CCC controls an N-channel MOSFET to keep this signal low until the switch is turned on. Once this *PWR_enable* is asserted to the MicroZed, the *PG_1V8* signal from the MicroZed must be monitored as it signals that the module is ready for VCC_{IO} bring-up. Much of this circuitry was adapted onto the initial test iteration of a custom PCB to supply power and facilitate a correct initialization and boot of the MicroZed.

A picture of an initial recreation of this reference circuity for proper start-up and initialization of the MicroZed can be seen in 2.8. This was a preliminary test to verify the operation of the MicroZed board from a bare-bones CCC. Creating this PCB also served as practice for hand soldering and using the reflow oven to solder some of the surface mount components.

The LUPA300 sensor in the vision subsystem is extremely sensitive to power supply noise, with multiple 2.5V power supply rails that are noted as especially

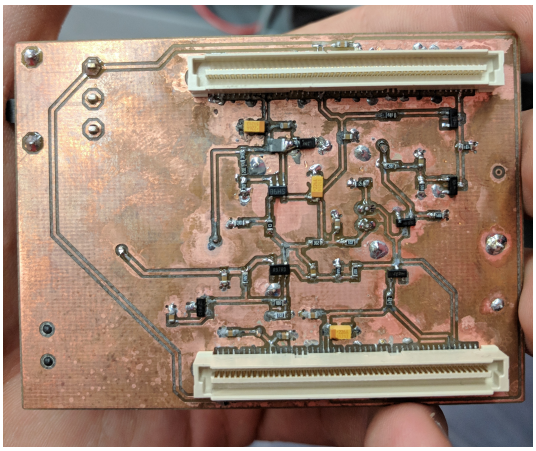

Figure 2.8: Initial test of power supply and start-up sequencing circuitry for the MicroZed board.

susceptible to noise in the sensor's data sheet (V_{DDA}, V_{ADC} and V_{PIX}) [19]. Any noise on these power rails directly corresponds to irregularities and artifacts in the resulting image read from the sensor. Indeed, this was the main problem plaguing previous design iterations of a interfaces designed for the LUPA300 and MicroZed.

In order to summarize the power requirements of the system, individual requirements of subsystems are compiled in Table 2.3. The MicroZed module itself consumes a significant amount of power for its Ethernet, USB and FPGA subsystems. The power budget for the MicroZed module is taken from the users guide [1] and assumes 80% regulator efficiency. In this way, the actual current drawn by the MicroZed will be, in practice, less than stated. The HDMI communication standard consumes some power, depending on whether transmitting or receiving video. Power budgets for sending and receiving are combined to estimate the power usage of the whole projector control subsystem. Together, the power consumption of all the subsystems combined is just over 1.8A. For this reason, it is determined that a 5V 2A wall mount power supply is sufficient to power the final system. The power switch and input filtering circuitry, discussed more in section 2.3 is shown in Fig. 2.9.

These power requirements are met by the combination of several efforts. High current and low noise rated power supplies are used, as well as separate, lower capacity regulators for supplies to output and digital drivers of the LUPA300. These output drivers and digital control logic drivers generate especially fast switching digital signals. By providing a separate regulator for these supply lines, the fast digital switching noise induced into other supply lines is minimized. An example of a separate regulator supplying the LUPA300 digital logic circuitry is shown in Fig. 2.13. There is an equivalent schematic for the output drivers (V_{DDO}) of the sensor that is not shown.

Table 2.3

Name	Peak Current	Voltage	Description
VCC_{ZYNQ}	1.2A	5V	Power for MicroZed module
VCC_{HDMI}	65mA	5V	Minimum current for HDMI compliance [4]
V_{DDA}	50 mA	2.5V	Power supply analog readout module
V_{DDD}	50 mA	2.5V	Power supply digital modules
V_{ADC}	100 mA	2.5V	Power supply of ADC circuitry
V_{DDO}	100 mA	2.5V	Power supply output drivers
V_{PIX}	100 mA	2.5V	Power supply pixel array
V_{RES}	10mA	3.3V	Power supply reset drivers

Table 2.3: Power requirements of the communication, projector control and vision subsystems.

Schematics

In this section, schematics of the circuitry designed in order to create a viable MicroZed CCC are presented. This includes circuitry adapted from the MBCC reference schematics as well as custom designs for the final version of CCC PCB with dual HDMI ports. All schematic and board designs were done using Autodesk EAGLE software. Many components such as the high density board-to-board connectors, regulators, programmable oscillator and ferrite beads, required the design of custom footprints in EAGLE. For this, a custom library (`.lbr`) file was made to contain all the footprints and schematic symbols that had to be created.

The schematics are broken down into functional groups depending on what subsystem they control or supply power to. First, circuitry to supply power to control the proper start-up of the MicroZed is shown. The schematics relating to the input of power to the PCB from an external source and the enable circuitry necessary to boot the MicroZed are shown in Figs. 2.9 and 2.10. The 5V line goes high when the user slides the power switch to the "ON" position. This pulls the PWR_EN line high, signifying the MicroZed to start initial power-on steps. There are also on and off status indicators in the form of green and red Light Emitting Diodes (LEDs) for ease of use.

The schematics for enabling and supplying the VCCIO rail to the PL module of the MicroZed is shown. The MicroZed supports two separate VCCIO levels on each of its PL banks, however for this application the two banks are assigned to the same supply. It should be noted that bypass capacitors to ground are placed by each PL supply connection on the MicroHeaders. Much of this circuitry was adapted from the MBCC reference schematics [18].

A portion of the circuitry was simplified, as the regulator used to supply VCCIO for the MicroZed supports a 1.8V enable signal. The regulator used in [18] does not support this, so there is extra op-amp circuitry for boosting the 1.8V VCCIO_EN signal from the MicroZed. This signal informs the user that the MicroZed has suc-

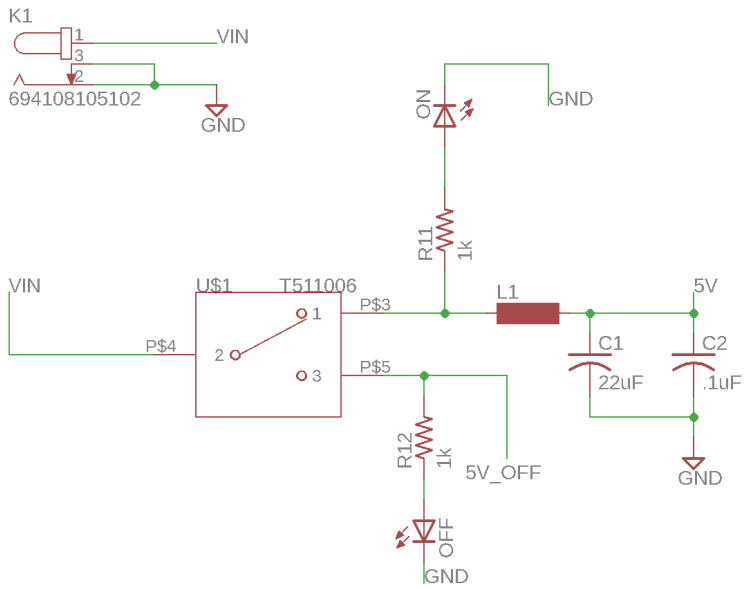

Figure 2.9: Power input and switch circuitry as well as status LEDs.

cessfully enabled its on-board regulators. The VCCIO_EN signal controls A 3.3V version of this regulator is used for VCCIO to the PL fabric of the FPGA, shown in Fig. 2.11. Figure 2.12 depicts the 2.5V version of the same regulator with added ferrite beads for input to the sensitive supply lines of the vision subsystem. In Fig. 2.13 the other Torex regulator is shown in the reccommended configuration. Two of these regulators are used for VDDD and VDDO of the LUPA300 sensor.

2.3 Supply Conditioning

Proving a noise free power supply for sensitive devices such as image sensors or other mixed signal and analog devices is critical for correct device operation. Noise introduced to supply lines for technology such as analog to digital converters (ADC) can directly induce error on the conversion result. In the case of the high-speed ADCs used in the LUPA300 sensor, this power supply noise manifests itself as sinusoidal stripes in the final image, presumably due to a bias in the ADC circuitry.

The initial sensor evaluation focused strictly on the correct assignment of signals and understanding the timing of the sensor. This was achieved, as an image was able to be read out from the sensor. However, effort was not put into the correct filtering and supply of power to the LUPA300 sensor. This is made evident by the large amount of noise visible in the resulting image, these results are discussed in section 2.5. By the final PCB design, power supply noise was reduced 17x from the initial sensor evaluation, and image sensor noise was eliminated. [1]

Filtering supply inputs to sensitive components as well as the output of regulators helps reduce noise on the power supply. Utilizing separate regulators is another technique, especially when the voltage rail has high instantaneous current usage. Use

[1]Except fixed pattern noise (FPN) which is expected as per the image sensor data sheet.

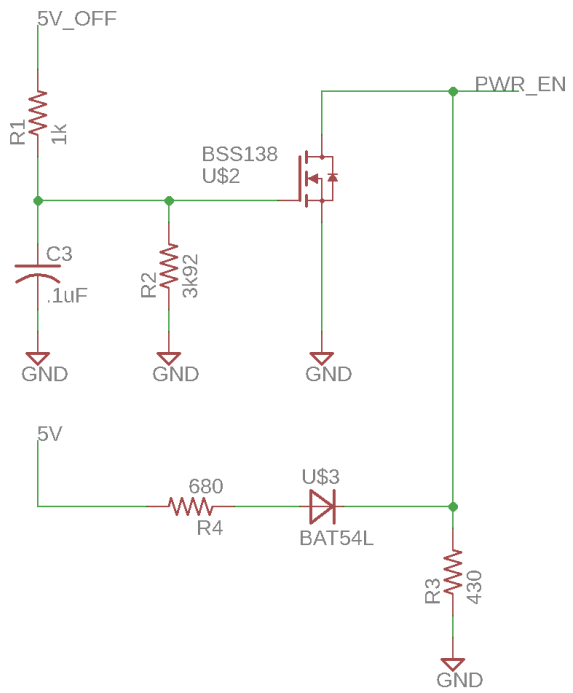

Figure 2.10: MicroZed power enable circuitry.

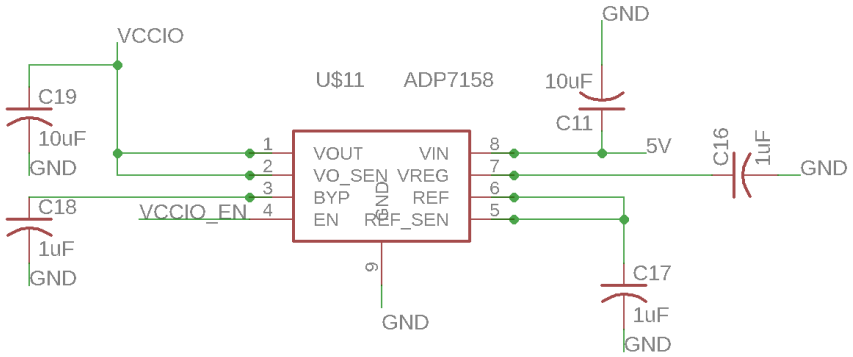

Figure 2.11: VCCIO regulation circuitry.

of ferrite beads helps ensure high frequency noise immunity of the system, and is used for isolating sensitive analog supplies from the shared voltage rail. These methods of power supply noise reduction are collectively referred to as supply conditioning and are crucial to an effective implementation of the proposed system. In this section, power supply conditioning circuitry seen in the schematics is expanded upon.

Supply Bypassing

When the outputs of Complimentary metaloxidesemiconductor (CMOS) devices are stationary, minimal current flows. It is when a transition occurs (rising or falling) that

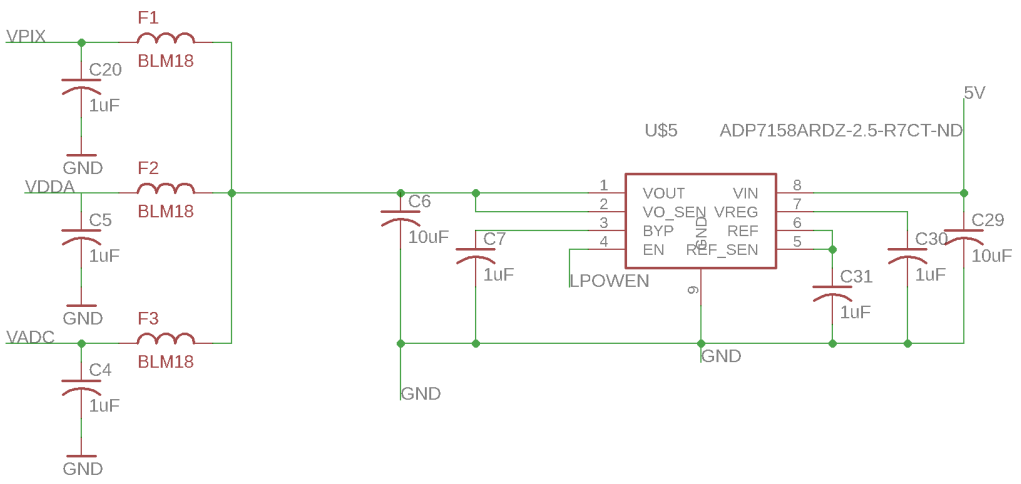

Figure 2.12: LUPA300 analog supply circuitry.

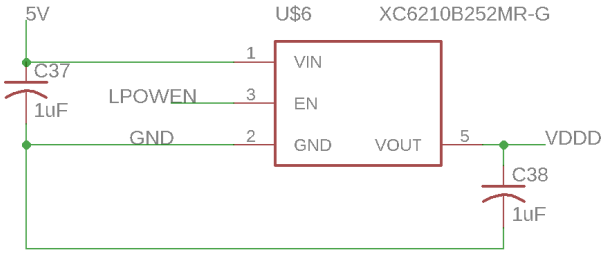

Figure 2.13: LUPA300 digital supply circuitry.

current consequently flows through the power supply and ground. Due to inherent gate capacitance on CMOS devices, these fast-switching currents in turn cause corresponding fluctuations in the power supply, leading to faulty or unexpected operation of the circuit [20].

Placing bypass (decoupling) capacitors between the different power supply points on an IC can help prevent this phenomenon. Bypass capacitors provide a pool of instantaneous current, eliminating possible ripple in the supply due to many switching DC signals with high di/dt. Minimizing the distance these high speed switching currents have to travel before reaching the capacitor is also beneficial to the noise reduction process. It is best practice to place the bypass capacitors as close as possible to the power connection on the IC of interest. Placing multiple capacitors in parallel across the supplies of high speed devices is also a common practice, as the smaller a capacitor value is, the higher frequency noise it will be effective at conducting.

Keeping the length of the traces connecting the bypass capacitor to power and ground as short as possible also increases effectiveness of the decoupling circuit. High speed PCB layouts often utilize multiple layers of copper, designated specifically to power and ground, making this process easy by way of though-board connections, known as vias. The physical capacitor can then be placed very close to the target IC, with vias directly under the capacitor pads, to power and ground planes.

Supply Filtering

In an effort to create a PDN with low output ripple and high noise immunity, regulators were sourced that featured internal noise suppression and filtering. The regulators chosen also required minimal external passive components and the ability to supply sufficient current for the system. These regulators are 2A ultra-low noise regulators from Analog Devices [2]. The high current rating allows them to be a common supply line for the 2.5V supplies of the LUPA300 sensor. Another 3.3V version of this regulator was used as the VCCIO regulator for the PL power to the MicroZed. These regulators are supplied from the 5V input to the CCC PCB. This 5V input is from a wall adapter and is first filtered with an inductor capacitor low pass circuit, as well as several decoupling capacitors, before being supplied to the input of the 2A regulators.

One way to measure the noise suppression ability of a voltage regulator is a metric known as power supply rejection ratio (PSRR). This is the ratio of the change in input voltage to the equivalent (differential) output voltage of a particular regulator. The 2A regulators chosen have excellent PSRR characteristics, as shown in Fig. 2.14. Note that PSRR can be measured in either positive or negative decibels (dB) and that it is the magnitude of the metric that is important. As you can see, the noise supression abilities of the ultra-low noise regulator exceeds 60dB, even at full 2A current draw, at 100kHz ripple frequency. Compare this to the lower capacity regulator's PSRR plot in Fig. 2.15, and you can see that this 700mA has only 30dB of noise suppression ability for much less of a load current. For this reason, these 700mA regulators were chosen to be dedicated regulators for the less sensitive V_{DDO} and V_{DDD} supplies of the LUPA300 sensor.

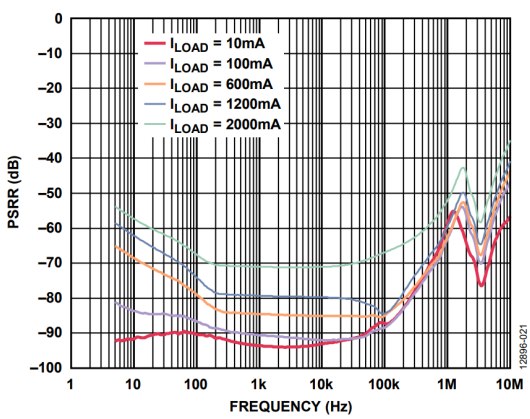

Figure 2.14: PSRR of ultra low noise regulator [2].

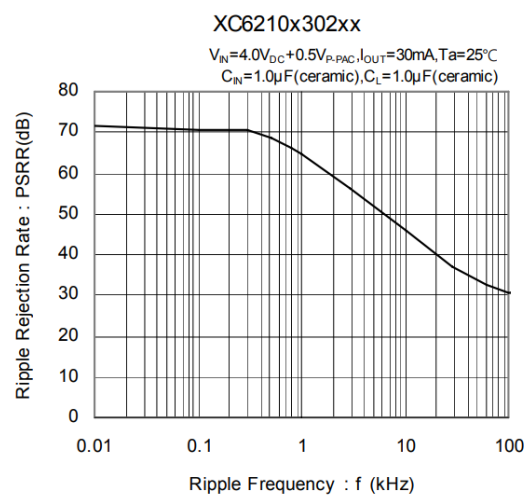

Figure 2.15: PSRR of Torex regulator used for digital supplies [3].

Ferrite Beads

Several power supplies to the LUPA300 image sensor in the vision subsystem are extremely susceptible to high frequency noise and jitter. Bypass capacitors on the power rails help to mitigate these effects but cannot suppress them entirely. Ferrite beads are effective for filtering high frequency power supply noise and cleanly sharing similar voltage supply rails while preserving high frequency isolation. The component acts like a resistor, which impedes high frequency noise and dissipates it as heat [21].

Ferrite beads are used in the design of the power delivery network for the vision subsystem. They are put in series with the 2.5V rail to each of the V_{DDA}, V_{ADC} and V_{PIX} supply lines. This configuration is aided by the inclusion of additional bypass capacitors on the sensor-side of the ferrites. This circuit configuration can be seen in Fig. 2.12.

There are several key aspects of a ferrite bead that make it effective at high frequency noise suppression. It is a passive device and can be modeled with the equivalent circuit seen in Fig. 2.16. When characterizing this equivalent model in circuit simulation, three key components are taken into account: impedance (Z); resistance (R); and reactance (X). The ZRX plot of the ferrite bead used to filter the 2.5V rail to sensitive vision subsystem supplies is shown in Fig. 2.17. To reduce high frequency noise, the bead must be in the resistive region [21]. As you can see, the chosen ferrite bead has high impedance around the high operating frequencies of the vision subsystem, namely the 80MHz pixel clock of the LUPA300 image sensor. Since the HDMI pixel clocks are in a similar frequency range, these ferrite beads help isolate the vision subsystem's power from the projector control subsystems data interface as well.

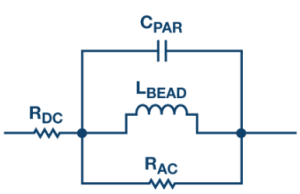

Figure 2.16: The equivalent circuit model of a ferrite bead.

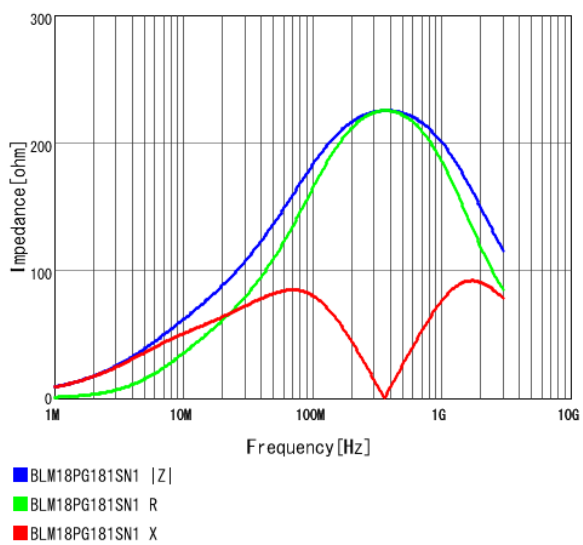

Figure 2.17: ZRX plot of the ferrite bead used in the system.

2.4 PCB Layout Considerations

A stable and reliable power supply is a crucial component of any electronic system. Supplying power to mixed signal devices creates several design challenges. The resulting system must ensure noise immunity by eliminating cross-talk between analog and digital subsystems. There are several methods to mitigate and prevent the introduction of radio frequency (RF) and electromagnetic (EM) noise into the system using effective electrical circuit and printed circuit board design [20, 22, 20, 23, 21].

The many considerations that go into the design of a PCB for robust PDN include dealing with component placement, trace routing and layer configuration of the actual board. Considerations such as power supply routing and ground plane configuration help avoid ground loops and allow optimal return current paths. The use of multiple-layer PCBs with dedicated power and ground planes is another technique [24] which allows for microstrip routing of high-speed signals. Dedicated power planes (especially ground) also allow effective routing of differential pairs. Appropriate circuitry for power supply filtering, PCB design and component choice, create sufficient noise immunity in mixed signal systems with increasingly high operating frequencies.

When designing a circuit board for high speed applications, the introduction of multiple layers for power and ground planes is an industry accepted method [24, 23]. In applications with advanced complexity and very high routing density, such as PC motherboard designs, stack-ups can be seen with 6, 8 and 12 layers. For the purpose of this design, a four layer board stack-up, shown in Fig. 2.18, was chosen. This type of design has multiple advantages over a 2 layer configuration including the availability of extra copper for dedicated power and ground planes. A solid ground plane is not only helpful for optimizing return current paths of high speed digital signals [25], it is also essential to minimizing radiated noise power from these signals by means of microstrip routing techniques [24].

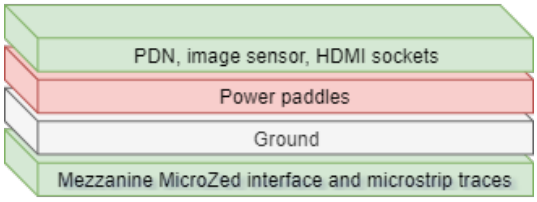

Figure 2.18: Four layer PCB stack-up used in final design.

High speed signals in consideration are the projector control subsystem (discussed more in Chapter 3), and the vision subsystem's clock, data and control interfaces. By placing the ground plane adjacent to the layer on which the majority of these high speed signals are routed, return current paths are minimized. This layout also provides isolation for the PDN and sensitive mixed signal vision subsystem.

The majority of the PDN can be seen in Fig. 2.19, in blue. This includes other signals, such as the termination for both HDMI ports. However, these signals are taken to the other side of the board quickly to mitigate their noise contribution. The light gray of the image is the internal power plane as depicted in Fig. 2.18.

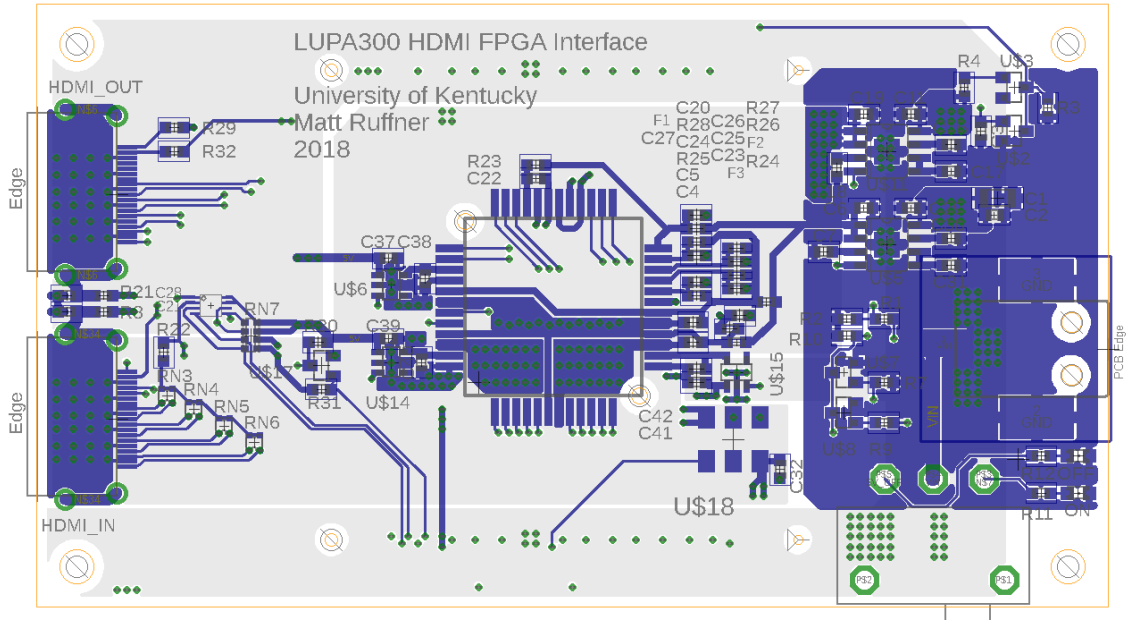

Figure 2.19: Power layout on the final iteration of PCB.

Large polygons for the 5V rail (outside edges) and VCCIO for the MicroZed (internal polygon) were created in this layer to aid the low-capacitance distribution of power to regulators and subsystems. This enables quick and easy connections to the power rail at varying places on the board with a simple via. Multiple vias are used in a grid pattern, rather than a single via, to provide a path with high current capability and lower resistance.

2.5 Noise Characterization

The improvement in power supply noise suppression ability, across the revisions of PCBs designed to support a LUPA300 sensor interface circuit boards, is quantified by ripple in the 2.5 volt supply rail. This ripple directly affects the voltage differential between the sensitive analog and digital logic of the vision subsystem. Measuring this value, as well as observing the apparent noise on the resultant image from the sensor, are the two ways that improvement has been quantified throughout the design process.

The different techniques to minimize power supply noise and their inclusion in various PCB iterations is shown in Table 2.4. Tactics used are expressed in this table and include use of low noise (LN) regulators, bypass capacitors, number of PCB layers and the inclusion of ferrite beads in the circuit design. It should be noted that V1 refers to the breakout board shown in Fig. 2.4, V2 refers to an intermediate PCB, not shown, and V3 refers to the final PCB with dual HDMI output shown in Fig. 1.4.

The first version of the vision subsystem interface boards allowed a single sensor to be plugged into multiple interface carriers for both the Teensy3.2 and MBCC.

Table 2.4

System Version	LN Regulators	Bypass Caps	PCB Layers	Ferrites
V1	N	N	2	N
V2	N	Y	4	N
V3	Y	Y	4	Y

Table 2.4: Noise reductions techniques used across versions of PCB on which noise is measured.

In this design, a minimal number of power supply reduction techniques were used, resulting in poor image quality. The inclusion of LN regulators and ferrite beads in future designs greatly improved the image quality and resulted in 17x reduction in power supply ripple.

Testing Process

The process of streaming live video from the custom PCB involves many components as well as a variety of custom code. The PCB itself must be tested for correct electrical connections and no shorts between the many fine-pitch connectors involved in the design. There are four main components that are critical to an operational system. These are: PCB population and soldering; FPGA code; MicroZed Qt code and host PC Qt code.

Once the PCB has been tested to ensure no shorts and correct supply output, the system is powered on, which in turn configures the FPGA with the `.bit` file on the microSD card. Once this happens, data is ready to be read from the FPGA by the host Linux system. Next, the MicroZed is logged into over the network via Secure Shell (SSH). From here, custom C++ (Open source Qt) code is compiled and run which then reads the image data from the FPGA by means of a special file descriptor (more on this in Chapter 4). The custom MicroZed Qt code then publishes a service on the local network that lets the host PC know a stream is available. On the host computer, a custom video client program is run which opens the network socket and interprets the video feed from the LUPA300 image sensor and displays it to the user. This interface can be seen in Figs. 2.20 and 2.21. It should be noted that only local discovery has been implemented in the server/client code and the MicroZed and host PC must be on the same local network.

The image viewer supports the ability to save the received image as a `.tiff` file, facilitating easy post processing, experimentation and analysis in MATLAB. This functionality is used to demonstrate the ability to perform fixed pattern noise (FPN) reduction and will be explained later on.

Supply Noise Reduction

The main contribution to noticeable noise artifacts in the resulting image is ripple in the vision subsystem power supply, as has been thoroughly discussed. The quan-

tification of reduction in this noise in the vision subsystem's power supply is shown in Table 2.5. Power supply ripple is calculated as a percent of the supply voltage for the 3.3V and 2.5V power supply rails that are used by the LUPA300 image sensor. As you can see, a 17x decrease in power supply noise is achieved by the final PCB and is a great improvement over the first version of PCB.

Table 2.5

System Version	2.5V Supply Ripple	3.3v Supply Ripple
V1	149%	153%
V2	42%	33%
V3	10%	9%

Table 2.5: Power supply ripple reduction results for the different versions of PCB design.

Image Quality Improvement

Another way to quantify the reduction in power supply noise across iterations of PCB is the improvement in perceivable image quality that ends up being streamed over the network. As you can see in Figs. 2.20 and 2.21, the fact that the video streaming system is functional does not necessarily imply that the image quality will be acceptable. The images in these two figures correspond to received images from the V1 and V2 PCBs, respectively.

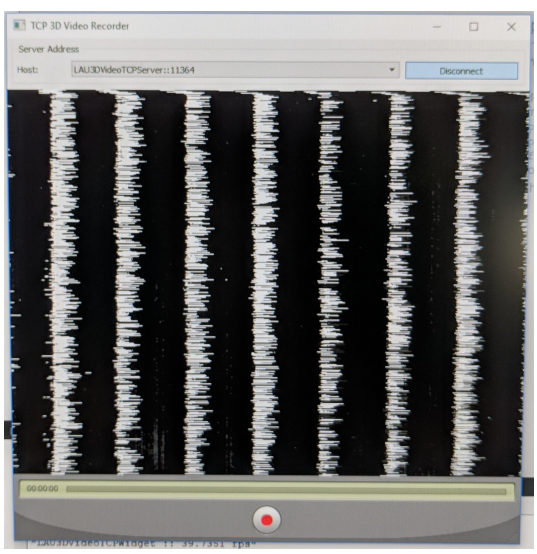

Figure 2.20: Noise from poor supply filtering on V1 PCB.

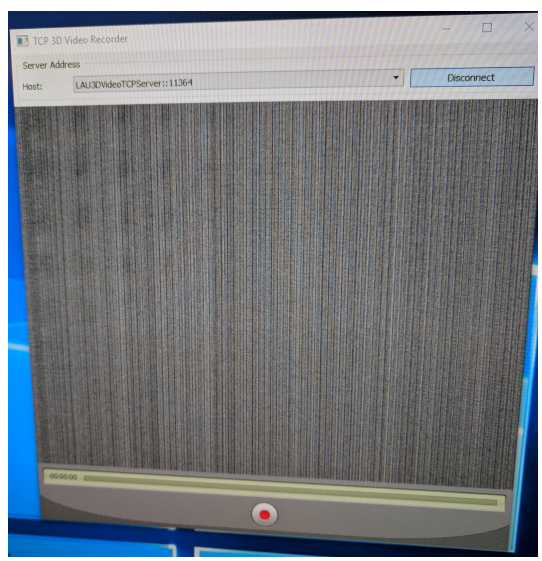

Figure 2.21: Improved noise on V2 PCB, still no discernible image.

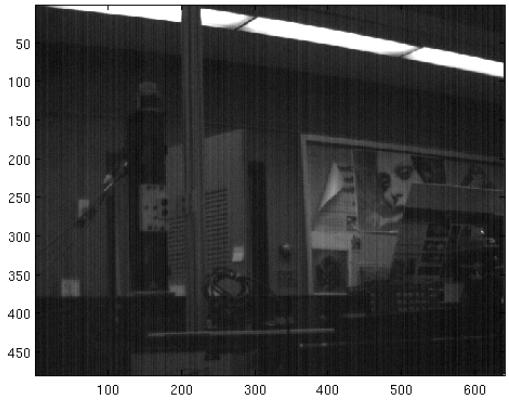

Figure 2.22: Image from V3 PCB. Discernible image, only noise is fixed pattern noise able to be removed in post processing by the FPGA or MATLAB.

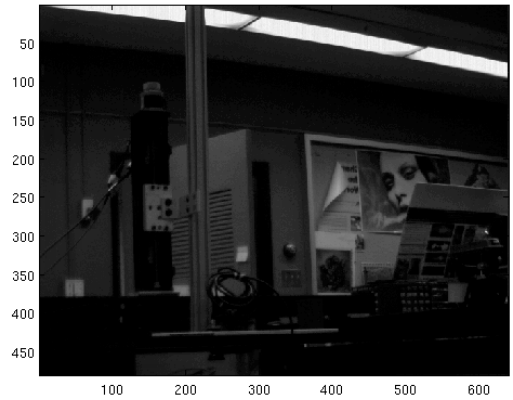

Figure 2.23: Final image from the LUPA300 image sensor after elimination of FPN via subtraction of noise image in MATLAB.

Fixed Pattern Noise Reduction

Fixed pattern noise, or FPN is the inherent random variation that occurs in an image sensor [19]. In conventional machine vision cameras, this is removed in image data post-processing on the FPGA controller. This implementation is also possible on the proposed system, however it is experimented with in MATLAB first. Since the streaming video client allows for the saving of frames of video as `.tiff` files, loading in to MATLAB is easy. By first covering the image sensor so that no light may approach it, and then taking a snapshot, the FPN of a particular sensor is captured. This 640x480 10 bit matrix of values can then be simply subtracted from an actual image. Thus the set of steps taken to experimentally remove FPN from a sample image captured, is to subtract the FPN image from the target image. The resulting image, after FPN reduction is shown in Fig. 2.23.

Chapter 3 HDMI

The use of an FPGA for the input, output and real time analysis of HMDI video is an active area of research [26]. HDMI is an accepted standard for uncompressed video transmission. It has high bandwidth, is an efficient means of data transmission, and if correct decoding methods are employed, similar to the work in [27], it can even be used to transmit encoded data other than that of raw video. In this work, a realtime 3D video system is implemented with a camera controlled by an FPGA. The FPGA performs the calculations necessary to create the realtime 3D information and then transmits that over the HDMI interface.

Pass through and analysis of HDMI with an FPGA is also possible, as the HDMI packet sniffer in [28] demonstrates. In this work, HDMI is inputted, and frames are duplicated so that they may be output over a local link as well as streamed over a network link. This implementation requires more work to establish a working HDMI implementation, as both input *and* output must be implemented. Existing FPGA development boards with integrated HDMI input and output are available such as the miniSpartan6+ from ScarabHardware [29] and the MojoV3 seen back in Fig. 1.2, with available HDMI shields. However, there is no existing dual HDMI solution with a high speed data interface, i.e. Ethernet, on the MicroZed. This is needed for the video streaming aspect of the proposed smart camera and thus HDMI must be added to the CCC PCB to complete the design.

HDMI devices can be one of two types: source or sink. This Chapter outlines the steps taken to design and test these two different modes of HDMI operation, as well as the schematics and PCB layout that implemeent them. Signaling inside an HDMI cable varies in type. There are static signals as well as two types of communication channels of varying use (see Fig. 3.1). Proper PCB routing and interface to these signals is taken into account in the propsed systems PCB design in order to ensure correct and reliable operation of the projector control interface.

3.1 Background

There are several different types of signaling involved in the HDMI standard. There is high speed differential signaling for audio and video data as well as the Display Data Channel (DDC) Inter-Integrated Circuit (I^2C) bus for communication of Extended Display Identification Data (EDID). HDMI uses four differential signal pairs to transfer data [30]. Three channels of Transition Minimized Differential Signaling (TMDS) are used for transferring the red, greeen and blue (RGB) color space information, as well as audio information. One differential channel is dedicated to the pixel clock, which provides a reference for decoding the TMDS encoded data on the three data channels. For the purposes of this work audio information from the HDMI cabling is not taken into account.

Many modern appliances and devices utilize HDMI as an audio/video (A/V) transport standard, including monitors, TVs and projectors. We are interested in

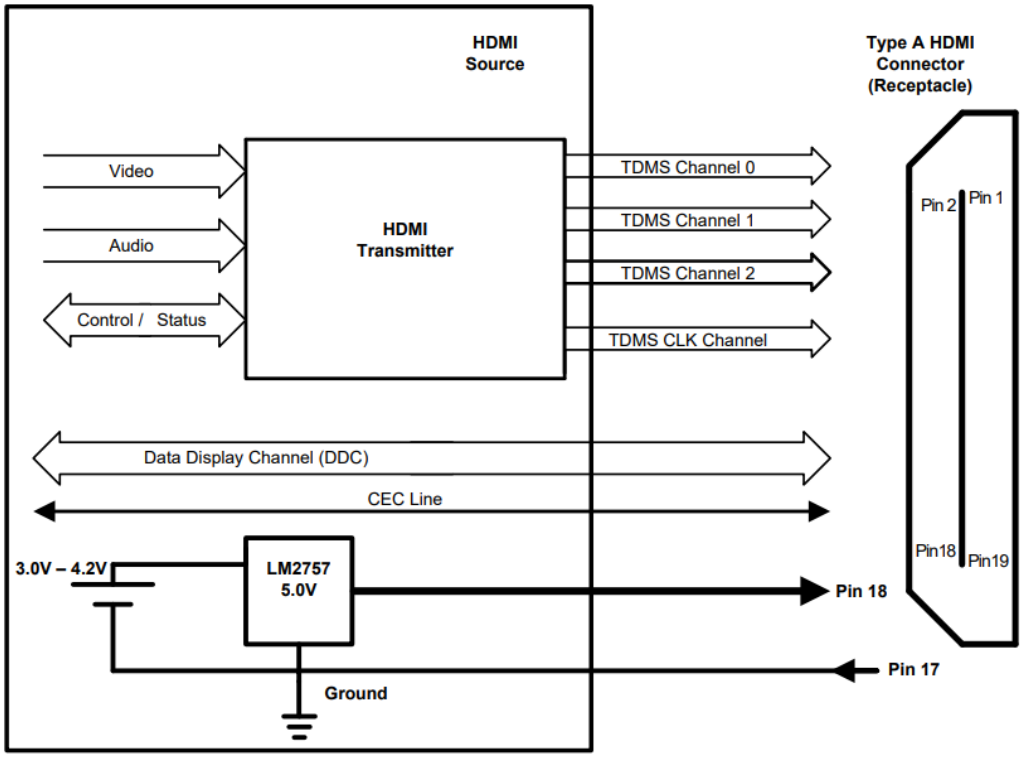

Figure 3.1: Overview of an HDMI source configuration [4].

projectors. specifically projectors that are 3D Ready, such as the Optoma ML750 [31]. 3D Ready means the HDMI input circuitry inside the projector is capable of the increased pixel clock rate which is needed for 120Hz video streaming.

3.2 Design Considerations

Designing a PCB for a communication standard that uses differential signaling technology like TMDS, requires that certain routing precautions and styles are followed [32]. Optimal differential pair signal routing is a best-effort exercise, as some implementations may work, but may not be *as* reliable as others. Having a PCB layer configuration that puts the differential pairs directly over a ground plane limits radiated power.

HDMI input and output schematics were implemented from the open source reference schematics provided by Scarab Hardware [29] for the miniSpartan6+, seen in Fig. 3.2. The TDMS signals, eight per HDMI port, are routed to differential pairs of the FPGA as the I/O pins on the Zynq7010 are in positive and negative pairs. This requires some tricky routing since the positive and negative pairs are in the same order on the MicroZed MicroHeader. The layer transition in the HDMI TDMS signals was used to swap the positive/negative pair orientation so that they could correctly line up with the MicroHeader pads. This is visualized by looking at the layout in Fig. 3.4; only the inside facing pins of the Micro header are convenient to access.

The circuitry needed for the input and output of HDMI are somewhat different. In the input configuration, the smart camera acts as an HDMI sink, which means it is responsible for telling the source what sort of resolution standards it supports. Currently, the FPGA is programmed to run at 800x600 @ 60Hz, as evidenced by Fig. 3.3. The resolutions supported (EDID) are communicated over the DDC to the HDMI source. The DDC bus is a 5V I^2C bus, so logic level converters are needed to shift it down to 3.3V. This circuitry was also adapted from the miniSpartan6+'s schematics.

As a SAR equipped smart camera, the proposed device will accept HDMI input from the host PC, and have it's HDMI output connected to a suitable projector, ready to create SAR scenes with a quick SLI 3D scan. In this configuration, the on-board FPGA can derive the HDMI output pixel clock from the HDMI input signal from the PC. The device can also operate in a strictly SLI scan mode, where no HDMI connection is required to the host PC. In this case, the FPGA is incapable of generating a fast enough 120Hz HDMI pixel clock with its Phase Locked Loops (PLLs). For this reason, a programmable oscillator [33] is also included in the design. This IC provides a HDMI pixel clock for the FPGA when 120Hz video output is desired and there is no HDMI input clock.

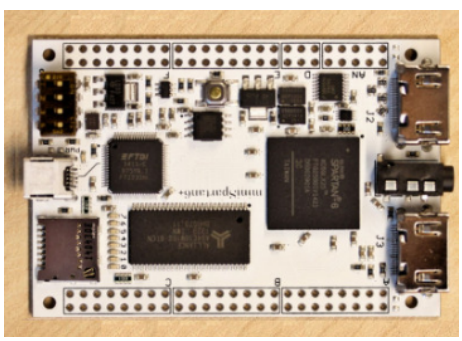

Figure 3.2: ScarabHardware miniSpartan6+ FPGA board with dual HDMI ports.

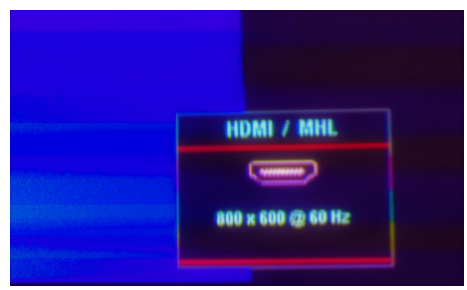

Figure 3.3: The Optoma ML750 short throw projector identifying the HDMI input signal from the custom MicroZed carrier card.

3.3 Testing

As mentioned earlier, the DDC bus is the means by which supported resolutions are indicated to the HDMI source by the HDMI sink. Fig. 3.3 shows the Optoma projector identifying the CCC PCB driven by the FPGA displaying a static blue test image. The two systems connected together, again, displaying the same static test image, can be seen in Fig. 3.5. The HDMI input functionality is untested due to a lack of FPGA code to test it. This is outside the scope of this thesis and HDMI input results are of a future concern.

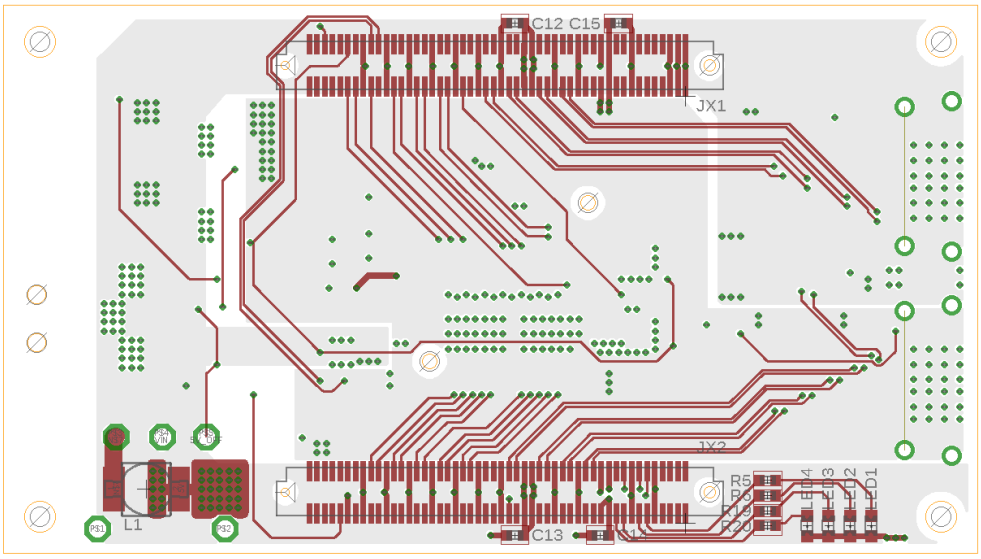

Figure 3.4: Final PCB layout showing the TDMS HDMI signal routing.

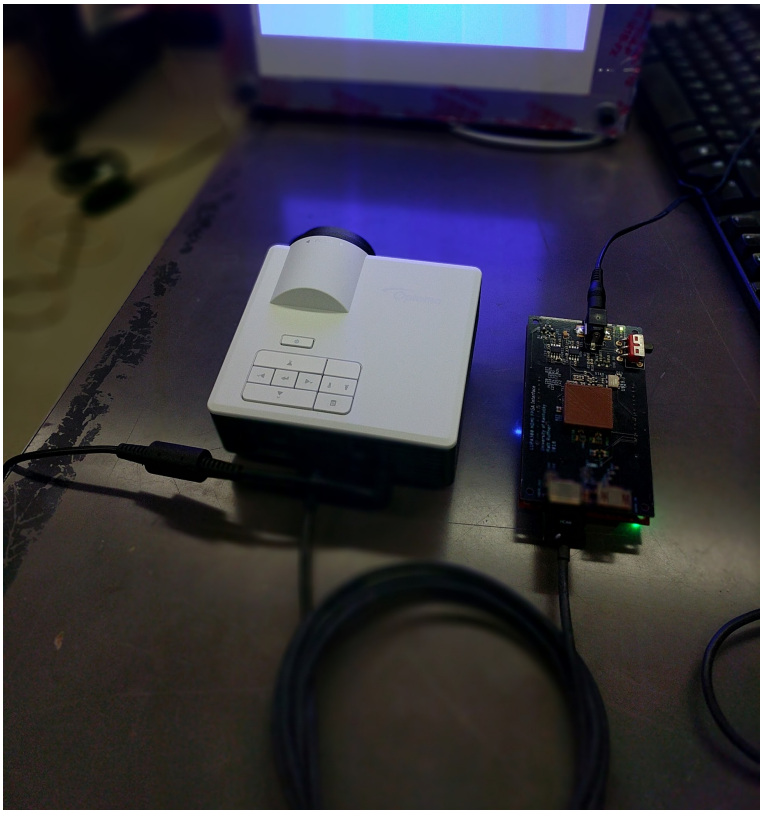

Figure 3.5: The custom MicroZed carrier card driving an Optoma ML750 projector via with on-board HDMI output capability.

Chapter 4 LUPA300 Image Sensor

The integration of a high speed machine vision sensor into a device by means of designing custom power and interface circuitry has several advantages over using COTS machine vision sensing solutions. These advantages include a reduction in cost and required physical footprint as well as low level access to sensing device functionality. Machine vision camera solutions already employ an FPGA for timing critical sensor readout operations. Utilizing the existing system controller, i.e. an FPGA, to handle image sensor control and data readout operations, as well as existing system duties, greatly simplifies overall design.

Machine vision cameras for 3D scanning and SLI applications must be able to operate at a speed which is at least that of the projector. In order to fully utilize the maximum frame rate from the projector in a SLI scanning system, the machine sensing solution must be capable of operating at a frame rate greater than or equal to that of the projector.

In the proposed Smart Camera with SAR Controller, the projector control subsystem is designed to support 3D ready projectors [31] which are capable of operating at a refresh rate of 120Hz. Accordingly, when such a projector is utilized at this high frame rate in SLI applications, a single pattern can be displayed in as little as 1/120th of a second. Thus, a suitable image sensor for this proposed system must be able to operate at no less than 120 FPS.

Due to its small package size, simplicity of data and control interfaces and suitably high frame rate, the LUPA300 CMOS image sensor [19] was chosen as the machine vision sensing element in the proposed system. The LUPA300 is a high speed (250fps) image sensor and has been used in several integrated machine vision sensing applications [34, 35]. The ability to implement real-time non-uniformity correction, e.g. Fixed Pattern Noise (FPN) elimination, with an FPGA based controller has also been demonstrated [36].

The LUPA300 is packaged in a 48 pin Leadless Chip Carrier (LCC) (see Fig. 4.1) with glass cover and is offered in monochrome and Bayer filter varieties. It features a resolution of 640x480 with 10 bit Analog to Digital Converters (ADCs) for quantizing subject illumination. Capable of achieving a maximum frame rate of 250 FPS when supplied with an 80MHz pixel clock, this sensor fulfills the system requirement of operating at greater than 120 FPS. The sensor also features dual and triple slope readout functionality, allowing HDR scenes to captured. All of these features combined with research precedent and a straight forward data and control interface, make the LUPA300 a suitable machine vision image sensor for the proposed Smart Camera with SAR controller.

This Chapter explains details of the vision subsystem such as timing requirements and data and control interfaces. Data readout functionality of the system is explained as well as the serial peripheral interface (SPI) by which the sensor is configured. Also covered in this chapter are the means by which image data is interpreted, processed and prepared by the communication subsystem to be sent over the network.

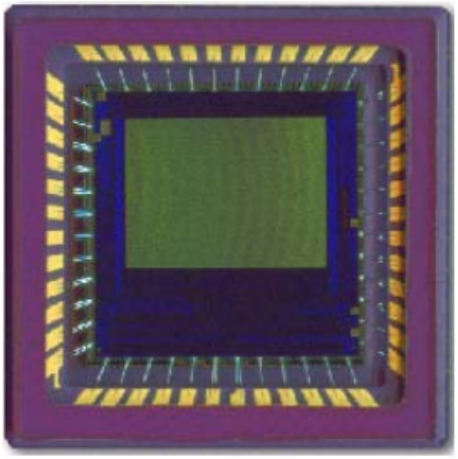

Figure 4.1: The LUPA300 CMOS Image sensor.

4.1 Data Interface

Part of the reason this sensor was chosen is the simplicity of its data interface. Being only 640x480, the pixel clock required for a 250 FPS is only 80MHz. Image sensors that feature higher resolution pixel arrays require more complex data readout systems, as well as higher pixel clock frequencies, in order to sustain the increased image data throughput.

Retrieving image data from the LUPA300 image sensor is a joint effort of FGPA and PC programming. The CCC PCB provides the connections necessary for the FPGA software to configure and read data from the image sensor. Image data is then written to a Xillybus IP core first-in-first-out (FIFO) buffer [37]. The underlying physical connections between the ARM processor and FPGA on the MicroZed in combination with kernel drivers on the ARM side, enable an FPGA FIFO to be read as if it were a Linux device file. This process is visualized in Fig. 4.2.

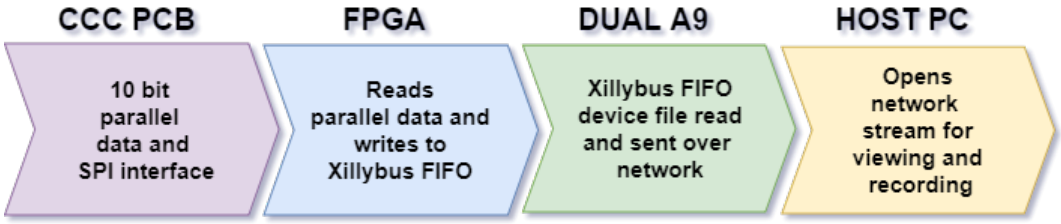

Figure 4.2: Data flow.

The LUPA300 operates in two main modes; slave mode and master mode. Only master mode will be considered, as it is simpler and provides sufficient operation for testing. In master mode, the sensor automatically begins outputting data on its 10 bit parallel output channel. Lines of image sensor values are read out one pixel at a time and clocked at the pixel clock (80MHz). There are a few signals that are pertinent to the readout of data in master mode. They are presented in Table 4.1.

Table 4.1

Signal Name	Function
Clock	Main pixel and logic clock
Reset	Pixel Reset
Frame valid	Signals that an entire new frame is ready
Line valid	Signals that a line of pixels is ready
D0-D9	10 bit parallel data output

Table 4.1: Important LUPA300 control and data output signals.

To start a readout, the reset line is first pulsed by the FPGA. A period of time later, the frame valid signal indicates that a new frame of video is ready to start being read. While the frame is valid, the line valid signal indicates that a particular row of pixels is ready to be read. The FPGA uses these signals, in combination with the 80MHz pixel clock, to sequentially sample the 10 data lines a total of 307200 (640x480) times. While it is taking these samples, each one representing a pixel value from the sensor, it is at the same time pushing these values into the Xillybus FIFO as 16 bit unsigned integers.

The Xillybus software guide for Linux [38] provides C code examples of reading from a device file FIFO that accompany their Verilog IP core. Similarly, the video server C++ code running on the MicroZed's A9 processor reads image pixel values rapidly from the device file, so as not to miss any, and then sends them over a network socket via Ethernet. Once this network socket has been published, a remote host may open the stream and view the frames of video read from the LUPA300 sensor. In this way, remote SLI scans and/or SAR projections could be controlled from a remote location with the addition of a wireless network interface added to the MicroZed via USB.

4.2 Control Interface

The CCC PCB also provides the physical connections between the LUPA300 image sensor's Serial Peripheral Interface (SPI) port and the FPGA such that a register value can be configured within the sensor. SPI register upload can be done at system initialization or during operation of the sensor to change programmable gain and offset on the fly.

There are a total of 16 registers in the sensor, and configuration values are composed of 12 bits. Each SPI transaction is made up of 2 bytes, with the 4 most significant bits of the first byte sent representing the sensor register address. The upload process as part of system initialization is shown in Fig. 4.3.

Another Xillybus FIFO facilitates this register configuration, having data written to it by the video server application running on the MicroZed, and the FPGA reading FIFO data. The values are read by the FPGA and compared to a previous copy of

Figure 4.3: The initialization process of the CCC, showing power-on, SPI register upload and start of image output from the LUPA300 sensor.

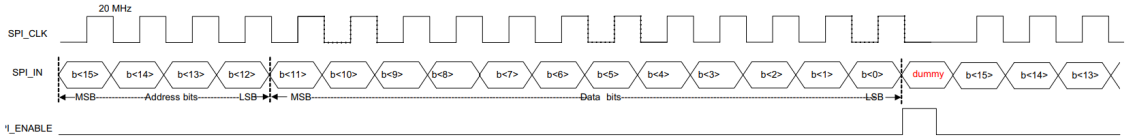

Figure 4.4: An example SPI upload sequence showing the byte order and clock polarity of the interface.

the register values to determine whether or not it should re-upload the new values over SPI.

A timing diagram showing a typical register upload sequence to the sensor is shown in Fig. 4.4. In this diagram you can see the clock polarity of the SPI register upload interface as well as the byte order and how the 4 most significant bits are used to indicate the target register of the sensor. Since data must be put on the Xillybus in byte increments, register data and address bits must be carefully arranged within the two bytes written to the FIFO handle. If byte order is mismatched between the C++ and FPGA code, the SPI registers will not be configured properly.

Presented here is the bare-bones configuration of LUPA300 image sensor for basic operation. With the physical connections in place, courtesy of the CCC PCB, all it will take to implement a variety of functionality in the resulting system are modifications to the FPGA and ARM software.

Chapter 5 Conclusions

In this thesis, the design of a Smart Camera with SAR Controller was presented. The idea was developed through iterations, achieving increasing levels of sophistication and integration at each stage. SAR functionality was achieved by integrating HDMI input and output onto a custom PCB which also features a high speed image sensor, that eliminates the need for a separate camera as in other SAR setups. HDMI input and output integration allows for video pass-through for SAR as well as a direct connection to a 3D ready 120Hz projector for SLI scanning. Creating a noise-immune PCB to support a high speed image sensor requires the effective design of a power delivery network as well as informed PCB routing techniques to avoid PDN noise. Circuitry was designed to supply clean power to the mixed signal LUPA300 CMOS image sensor as well as the chosen ARM+FPGA controller solution.

The total costs of subsystems that make up the proposed device are shown in Table 5.1. The projector control subsystem is part of the CCC PCB and is therefore part of its cost. This system, combined with a high performance 3D ready projector, can be acquired for roughly $1,000. This is 5% of the cost of an industrial 3D scanner.

Table 5.1

Component	Cost
MicroZed Module	$199
LUPA300 Sensor	$193
Assembled CCC PCB	$80
Total Cost	$472

Table 5.1: Major system components and their associated cost, as well as the overall system cost.

Several iterations of PCB design and power supply filtering experimentation were conducted. Initial sensor evaluation was performed to understand timing and frame rate parameters of the image sensor. Custom EAGLE footprints were created to support the MicroHeaders and a PDN was designed to enable correct start-up and operation of the MicroZed module. Experience was gained in multi-layer PCB stack-ups and the benefits of dedicated internal power and ground planes. Proper power supply filtering and bypassing was used in combination with LN regulators to provide minimized power supply ripple to the vision subsystem.

As you can see, this device offers a significantly cheaper alternative to industrial 3D scanners which utilize SLI as a means of 3D reconstruction. The presented PCB design is also easily modifiable and configurable. The design of the proposed system provides a starting point for other SAR enabled smart cameras. The PCB designed can be adapted to use a different image sensor or interface to a different FPGA such as the PicoZed, a similar Zynq7020 based SoM with a smaller footprint.

The proposed design can also be adapted to utilize more modern FPGA's such as the Artix-9 FPGA. There are development boards which feature this FPGA with a high speed (2880MBit/s) USB3 interface, which would allow for higher speed image sensors to be used on proposed PCBs in the future. Utilizing this high speed USB3 interface would allow even more FPS throughput from an even faster image sensor. ON Semiconductor produces an image sensor in the same LCC package which is capable of 815fps at the same resolution as the LUPA300 image sensor. This sensor, the PYTHON300 [39], is essentially a drop in replacement for the LUPA300.

In conclusion, this thesis details a novel incorporation of an HDMI SLI projector controller and machine vision image sensor onto a single PCB with integrated power supplies. This system design solved synchronization issues between the camera, projector and host PC and the final product is small, compact and more affordable.

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Vita

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