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Quantitative analysis of the density of trap states at the semiconductor-dielectric interface in organic field-effect transistors

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The electrical properties of organic field-effect transistors are governed by the quality of the constituting layers, and the resulting interfaces. We compare the properties of the same organic semiconductor film, 2,8-difluoro- 5,11-bis (triethylsilylethynyl) anthradithiophene, with bottom SiO_2 dielectric and top Cytop dielectric and find a $10\times$ increase in charge carrier mobility, from $0.17 \pm 0.19 \, cm^2 \, V^{-1} \, s^{-1}$ to $1.5 \pm 0.70 \, cm^2 \, V^{-1} \, s^{-1}$, when the polymer dielectric is used. This results from a significant reduction of the trap density of states in the semiconductor band-gap, and a decrease in the contact resistance. © *2015 AIP Publishing LLC.*
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The performance of organic field-effect transistors (OFETs) has improved steadily over the last decade due to the development of new materials, the optimization of electrodes, and transition to novel dielectrics.[1–4] A large variance in device characteristics can be obtained in OFETs employing the same semiconducting material as a result of changing the deposition method, or even modifying details within the same process, such as the solvent type, the deposition temperature, or the chemistry at the interfaces.[5–9] This was attributed to film microstructure or material polymorphism.[7,10] The mobility also responds to the type of dielectric used, with the high-k dielectrics causing an increase in the effective mass of the charge carriers due to the formation of Fröhlich polarons.[5,11] The performance of organic transistors with polymer dielectrics of lower permittivities has displayed a similar trend; in this weak coupling regime, this trend was explained in terms of the broadening of the density of states (DOS) as a result of the energetic disorder caused by static dipoles at the dielectric/semiconductor interface.[12,13]

The Si/SiO_2 combination has historically been used as a convenient test-bed due to its high availability and robust fabrication protocols, which allow for a quick screening of a large number of compounds and for testing the effectiveness of novel processing methods. Alternative gate dielectrics are gaining popularity due to better mechanical flexibility, relaxed processing parameters, and, in many cases, improved device performance. Cytop dielectric was successfully used in electrostatic gating of both organic-inorganic hybrid materials and organic semiconductors.[14,15] These OFETs exhibit high mobilities ($\mu = 13.9 \, cm^2 \, V^{-1} \, s^{-1}$ for rubrene single crystals), low subthreshold swings ($S = 65 \, mV \, dec^{-1}$), low operating voltages, and band-like charge transport.[5,15–17] These properties, however, were significantly inferior in devices of the same organic semiconductors in similar structures, but with other dielectrics. For example, 2,8-difluoro-5,11-bis (triethylsilylethynyl) anthradithiophene (diF-TES

ADT) deposited on fluorinated contacts, or vertically segregated from blends with amorphous semiconducting polymers, typically exhibits mobilities in the order of $10^{-1} cm^2 \, V^{-1} \, s^{-1}$ in bottom-gate, bottom-contact (BG-BC) OFETs with SiO_2 dielectric, and greater than $1 \, cm^2 \, V^{-1} \, s^{-1}$ in top-gate, bottom-contact (TG-BC) devices with Cytop dielectric.[18–22] In blends, this was assigned to the high grain boundary conductivity due to polymer intercalation.[21] This, however, cannot account for the differences consistently observed between the two geometries in the case of neat small-molecule organic semiconductor films. One possible cause for the observed phenomena in this case is the reduced density of trap states afforded at the interfaces with the Cytop dielectric, as proposed by several reports.[23–25] Nevertheless, all these measurements were performed on different samples, where disentangling the effects arising from differences in the interface properties from those originating from sample-to-sample-variation is challenging. For example, Krellner *et al.* have shown that even for single crystal devices that should nominally be identical, a large difference, of up to two orders of magnitude, in the trap density of states can be detected as a result of sample quality variations.[26] In addition, the differences in the device structure may also play a role.[27,28] Here, we investigate the electrical characteristics of OFETs based on the same organic semiconductor film with SiO_2 and Cytop as bottom- and top- gate dielectrics, respectively (Figure 1(a)). This device structure allows us to characterize the *same* semiconducting film in the two transistor architectures, and to directly compare the two semiconductor/dielectric interfaces and device geometries, thus minimizing the differences arising from sample fabrication and the variability from device to device. We note, however, that the top and bottom semiconductor surfaces are not identical, as we will discuss in detail later. Since poorer performance (i.e., decreased mobility, increased subthreshold swing, and larger threshold voltage (V_{th})) are generally attributed to trapping states, we focused on the trap
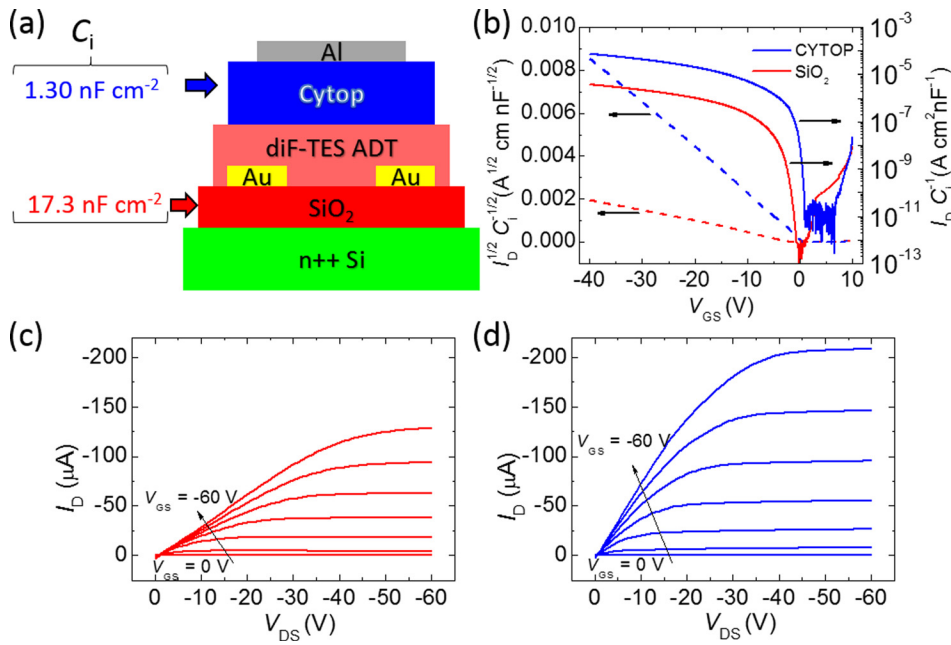
FIG. 1. (a) Structure of the devices used in this study: top- and bottom-gate OFET geometry. (b) Drain current (I_D) versus gate voltage (V_{GS}) characteristics measured in the saturation regime ($V_{DS} = -40$ V) and scaled to the areal capacitance of the gate dielectric (device geometry: L/W = 30/1000). Transport characteristics measured for the SiO$_2$ (c) and Cytop (d) devices fabricated on the same diF-TES ADT film.

DOS as one of the essential metrics for comparison. In parallel, we evaluate the contribution of the contact resistance on the measured device properties.

OFET devices were fabricated on the surface of test-beds consisting of a heavily n++ doped Si gate electrode with a thermally grown gate dielectric of 200 nm SiO$_2$ and an array of Ti (5 nm)/Au (45 nm) source-drain contacts defined by photolithography and deposited by e-beam evaporation. The Au electrodes were treated with a pentafluorobenzenethiol (PFBT) self-assembled monolayer (SAM) to improve the microstructure and injection.[18] This was applied by immersing the UV/ozone-cleaned substrate in a 30 mM solution of PFBT in room temperature ethanol for 30 min followed by a 5 min sonication in pure ethanol. The semiconductor diF-TES ADT was then dissolved in chlorobenzene (Sigma Aldrich) to create a 1–2 wt. % solution and spun-cast to form a thin film. The Cytop layer was subsequently deposited by spin-coating in a nitrogen glovebox, and heated at 50 °C overnight in a vacuum oven to create a 1400 nm thick film. Finally, the Al top-gate electrode was thermally evaporated through a slotted shadow mask in order to pattern the gates above the active channel of each OFET. The surface roughness was determined by atomic force microscopy (AFM), with a Nanoscope IIIA (Veeco Instruments). Single crystal devices were fabricated for comparison. Crystals of diF-TES ADT were grown by physical vapor transport and laminated on either a substrate with SiO$_2$ or Cytop as the bottom-gate dielectric.[29]

We extracted the mobility, μ, in the saturation regime while applying a drain-source voltage of $V_{DS} = -40$V using the expression

$$I_D = \frac{W}{L}\frac{C_i}{2}\mu(V_{GS} - V_{th})^2, \quad (1)$$

where I_D is the drain current, W and L are the width and length of the channel, respectively, C_i is the areal capacitance of the dielectric, and V_{GS} is the gate-source voltage. Low-temperature electrical measurements were performed in a

vacuum probe station, in the temperature range 220 K < T < 300 K, where no phase-transitions are present.[30]

Figure 1(b) shows the transfer curves for the devices on the same semiconductor film with Cytop (blue) and SiO$_2$ (red) as the dielectric. Here, the $I_D^{1/2}$ was scaled by the areal capacitance in order to better compare the corresponding currents ($C_i = 1.30$ nF cm^{-2} for the Cytop dielectric and 17.3 nF cm^{-2} for SiO$_2$). We found that the Cytop device exhibits a mobility of $\mu_{Cytop} = 3.14$ cm^2 V^{-1} s^{-1}, whereas the SiO$_2$ device has mobility, $\mu_{SiO2} = 0.20$ cm^2 V^{-1} s^{-1}. The linear regime mobilities for this film are slightly lower, due to the contact effects, but follow the same trend: $\mu_{Cytop} = 3.04$ cm^2 V^{-1} s^{-1} and $\mu_{SiO2} = 0.18$ cm^2 V^{-1} s^{-1}. Additionally, $S_{Cytop} = 0.29$ V dec^{-1} and $V_{th, Cytop} = 0.35$ V for the OFET with the channel forming at the Cytop interface, whereas the SiO$_2$ device shows larger values, of $S_{SiO2} = 1.5$ V dec^{-1} and $V_{th, SiO2} = 0.58$ V. The evolution of the drain current with the drain voltage for different gate voltages for the same devices is shown in Figures 1(c) and 1(d), and these graphs were used for the determination of the contact resistance, as detailed later.

We measured 200 similar devices and the results are presented in Figure 2. The average mobility was estimated to be $\mu_{Cytop, avg} = 1.5 \pm 0.70$ cm^2 V^{-1} s^{-1} for the Cytop FETs and $\mu_{SiO2, avg} = 0.17 \pm 0.19$ cm^2 V^{-1} s^{-1} for the SiO$_2$ FETs, respectively. These values agree well with those reported in the literature for diF-TES ADT on Cytop and SiO$_2$ dielectrics with similar configurations.[18,31]

In order to understand the observed difference in performance, we examined the two interfaces where the transistor channel forms, the diF-TES ADT/Cytop and the diF-TES ADT/SiO$_2$ interface. We used Grünewald's method to analyze the trap DOS.[32,33] By determining the dependence of the drain current on the electric field due to the gate-source voltage in the linear regime ($V_{DS} = -2$V), the trap DOS was extracted as a function of the energy within the bandgap. This was accomplished by first developing the function for the gate-dependent dielectric/semiconductor interface potential, $V_0 = V_0(U_g)$, by numerically solving the equation below
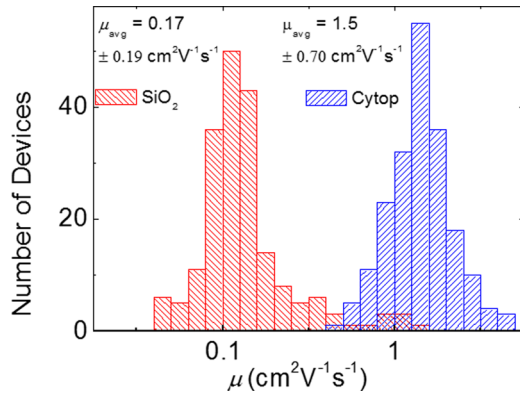
FIG. 2. Histogram showing the values of saturation mobility measured on 200 diF-TES ADT devices with SiO$_2$ (red) and Cytop (blue) dielectrics. The average values are indicated in the inset.

$$\exp\left(\frac{eV_0}{kT}\right) - \frac{eV_0}{kT} - 1 = \frac{e}{kT}\frac{\epsilon_i d}{\epsilon_s l \sigma_0}$$

$$\times \left[U_g \sigma(U_g) - \int_0^{U_g} \sigma(\tilde{U}_g) d\tilde{U}_g\right], \tag{2}$$

where $U_g = |V_{GS} - V_{FB}|$, the field-effect conductivity $\sigma(U_g) = \frac{L}{W}\frac{I_D}{V_{DS}}$, $\sigma_0 = \sigma(U_g = 0)$, ϵ_i and ϵ_s are the dielectric constants of the insulator and semiconductor, respectively (3.9 for SiO$_2$, 2.05 for Cytop, and 3 for the diF-TES ADT).[34,35] V_{FB} is the flat-band voltage which was assumed to be the onset gate voltage of the device, and e, k, and T are the elementary charge, Boltzmann constant, and absolute temperature, respectively. The interface potential versus gate voltage above the flat-band, $V_0 = V_0(U_g)$, for the Cytop and SiO$_2$ dielectrics are included in Figure SI 1 in the supplementary material.[36] The total hole density (p) was calculated from

$$p(V_0) = \frac{\epsilon_0 \epsilon_i^2}{\epsilon_s l^2 e} U_g \left(\frac{dV_0}{dU_g}\right)^{-1}. \tag{3}$$

Finally, the trap DOS was found to be

$$N(E) \approx \frac{1}{e}\frac{dp(V_0)}{dV_0}, \tag{4}$$

in which $E = eV_0$ is the energy relative to the Fermi energy E_F.[33,37]

In Figure 3(a), we plot the DOS calculated at the organic semiconductor interface with Cytop (blue) and SiO$_2$ (red) dielectrics. Our data indicates that improvements observed in Cytop-based devices are due to a drastic reduction of the trap density within the band gap of the organic semiconductor. The sub-gap DOS at both interfaces decrease abruptly from the valence band edge and the calculated trap DOS for the top-gate Cytop device is roughly two orders of magnitude lower than that of the bottom gate device of the same active layer using SiO$_2$ dielectric. This trend was consistent for all devices investigated here (more than 10).[25] By modeling each of these curves with an exponential function[38]

$$N(E) = \frac{N_t}{E_B}\exp\left(-\frac{E}{E_B}\right), \tag{5}$$

where N_t and E_B are the total trap density and characteristic energy decay of the distribution, we found a higher density of both shallow ($N_t = 6 \times 10^{19}\,\text{cm}^{-3}$) and deep traps ($N_t = 3 \times 10^{19}\,\text{cm}^{-3}$) at the SiO$_2$ interface, compared to $N_t = 10^{18}\,\text{cm}^{-3}$ and $N_t = 6 \times 10^{17}\,\text{cm}^{-3}$ for the shallow and deep traps at the Cytop interface. Here, we used one exponential function for the states located at energies within a few kT ($<100\,\text{meV}$) from the valence band edge—the "shallow traps"—and another exponential for the "deep traps."[39] For both dielectrics, the shallow traps exhibit a steeper decrease ($E_B = 24\,\text{meV}$ for SiO$_2$ and $E_B = 21\,\text{meV}$ for Cytop), which is followed by a moderate decay for the deep traps ($E_B = 30\,\text{meV}$ for SiO$_2$ and $E_B = 28\,\text{meV}$ for Cytop). The DOS results are also supported by the increased S and V_{th} at the SiO$_2$ interface, as well as the temperature dependent electrical measurements, which show a significantly more activated mobility for the SiO$_2$-gate structure. The activation energy, E_A, was calculated from the Arrhenius plot, and a value of $51.0\,\text{meV}$ was obtained for the SiO$_2$ OFETs, and $16.1\,\text{meV}$ of the Cytop-top gate OFET, as seen in Figure 3(b).

The traps at the semiconductor/dielectric interface originate from both the semiconductor and the dielectric layers. When impurities are present in the semiconductor film, they disrupt the pristine crystal lattice and create additional states that may energetically invade the bandgap.[35] In addition, structural defects resulting from molecular displacement from the equilibrium position induce local variation in the transfer integral, which also leads to the formation of trap states, with the trap depth and density being directly related with the structural imperfections.[40,41] The molecular misalignment of the organic molecules assembled in the first layer, at the SiO$_2$/diF-TES ADT interface, diminishes the electrical performance of the OFETs by increasing the trap density in the semiconductor bandgap.[41] We were able to reduce the interfacial trap density by a factor of two by applying gentle mechanical vibrations during crystal growth, but this method was not used here.[41] The microstrain present in the film is more severe in its first layers, at the interface with the SiO$_2$ dielectric, where the growth is initiated, and it gradually decreases throughout the film thickness, as the structure becomes more relaxed. Therefore, the DOS originating from molecular sliding is lower at the top-surface, in contact with Cytop, in agreement with our experimental observations. The film roughness is also known to impact the charge transport, with high values lowering mobility by increased charge scattering.[42,43] We evaluated the roughness at each interface using AFM (see Figure SI 2 in the supplementary material). We found that the oxide surface (Figure SI 2(a)), where the charge transport occurs in the SiO$_2$/diF-TES ADT devices is quite flat, with an RMS roughness of $\approx 0.2\,\text{nm}$.[43] The roughness at the organic semiconductor film surface (Figure SI 2(b)), where the diF-TES ADT/Cytop channel forms, is significantly higher ($\approx 1\,\text{nm}$). Thus, in spite of the increased roughness, the Cytop devices consistently showed superior electrical characteristics, suggesting that other factors play a key role in charge transport in these devices. The nature and structure of the dielectric layer can also
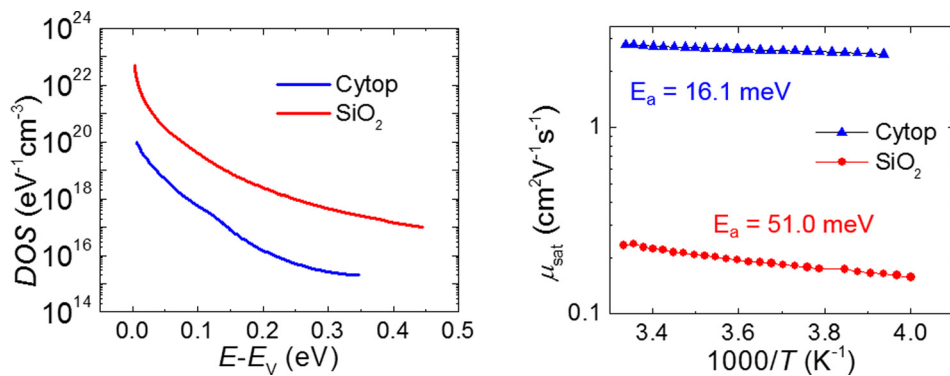
FIG. 3. (a) Trap DOS in diF-TES ADT OFETs with Cytop (blue) and SiO_2 (red) dielectrics. (b) Arrhenius plots for both Cytop (blue triangles) and SiO_2 (red circles) with activation energies, E_A of 16.1 meV and 51.0 meV, respectively.

give rise to trapping sites in the FET channel. SiO_2 surfaces often form bonds with hydroxyl groups which create surface dipoles. These surface states have been shown to be charge trapping centers for electrons.[44] In contrast, Cytop is both chemically inert and highly hydrophobic due to its fluorination, which helps reduce contaminants that may otherwise migrate to the semiconductor/dielectric interface.

In the following, we evaluate the impact of the device geometry on the observed performance differences. The structures in which the contacts are deposited on the opposite side of the dielectric/semiconductor interface (i.e., bottom-gate with top-contacts or top-gate with bottom-contacts) are expected to yield higher performance as a result of lower contact resistance characteristic to this architecture.[45] Indeed, we calculated the contact resistance in our devices using the gated transmission line method (TLM)[45] and found that the top-gate, Cytop device, displays a contact resistance of $R_c = 45$ Ωm, compared to $R_c = 177$ Ωm for the bottom-gate, SiO_2 device (both measurements were performed at $V_{GS} = -60$ V). The mobilities corrected for the contact resistance for the device in Figure 1 are: $\mu_{Cytop,c} = 3.9$ cm^2 V^{-1} s^{-1} and $\mu_{SiO2,c} = 0.8$ cm^2 V^{-1} s^{-1} for the linear regime and $\mu_{Cytop,c} = 3.3$ cm^2 V^{-1} s^{-1} and $\mu_{SiO2,c} = 0.3$ cm^2 V^{-1} s^{-1} for saturation.[27,28] When comparing the corrected mobilities, it can be observed that the differences are mitigated, confirming the fact that the contact resistance is an important factor in the observed discrepancies between the top and bottom-gate devices. Unfortunately, because of challenges related to processing, the complementary thin-film FET structures, with top SiO_2 and/or bottom Cytop gate were impossible to fabricate. In order to separate the interface and contact effects, we tested single crystals devices on identical bottom-gate, bottom-contact structures, with both dielectrics. The interface potential versus gate voltage above the flat-band, $V_0 = V_0(U_g)$, for representative devices are included in Figure SI 3 in the supplementary material.[36] We measured 10 devices for each type of structure and found that the trap DOS of the bottom contact, single crystal devices is about two orders of magnitude lower for the devices with the Cytop dielectric when compared with the SiO_2 devices. These results are in agreement with the previous reports on single crystal devices. We note, however, that in these devices the surface of the crystals is similar in both type of samples, as the crystals are grown *ex-situ* and laminated over the transistor structures, as opposed to the thin-film samples, where the molecular packing and roughness may vary, as described above. In addition, these measurements were prone

to variations due to different crystal qualities and anisotropy. Nevertheless, the results support our claim that the source of the improvement observed in Cytop devices cannot be explained in terms of device geometry alone and that the phenomena taking place at the semiconductor/dielectric interfaces play a key role in the resulting device characteristics.

In summary, we fabricated diF-TES ADT thin-film transistors with average mobilities of 1.5 cm^2 V^{-1} s^{-1} in the bottom-contact, top-gate configuration, with Cytop dielectric, and 0.17 cm^2 V^{-1} s^{-1} in the bottom-contact, bottom-gate architecture, with SiO_2 dielectric. We showed that the Cytop OFETs outperform those made with SiO_2 due to a lowering of the trap DOS at the dielectric/organic semiconductor interface and reduction in the contact resistance. Since we fabricated the test devices such that the same semiconducting layer of diF-TES ADT is shared for both dielectrics, we conclude that the major source of additional induced traps originates from the surface states at the SiO_2 interface. In addition, the structural imperfections due to molecular misalignment at this interface induced during film growth can give rise to additional trapping sites.

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