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Low-voltage polymer/small-molecule blend organic thin-film transistors and circuits fabricated via spray deposition

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Organic thin-film electronics have long been considered an enticing candidate in achieving high-throughput manufacturing of low-power ubiquitous electronics. However, to achieve this goal, more work is required to reduce operating voltages and develop suitable mass-manufacture techniques. Here, we demonstrate low-voltage spray-cast organic thin-film transistors based on a semiconductor blend of 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene and poly(triarylamine). Both semiconductor and dielectric films are deposited via successive spray deposition in ambient conditions (air with 40%–60% relative humidity) without any special precautions. Despite the simplicity of the deposition method, p-channel transistors with hole mobilities of $>1 \text{ cm}^2/\text{Vs}$ are realized at -4 V operation, and unipolar inverters operating at -6 V are demonstrated. © 2015 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4922194>]

In order for organic thin-film transistors (OTFTs) to find application in portable, battery-powered electronic devices, their operating voltages must be reduced significantly from the often reported bias range of $\pm 30 \text{ V}$ to below $\pm 4 \text{ V}$. This technological development is critical since it would make OTFTs and the resulting integrated circuits compatible with common lithium-polymer batteries, which supply a 3.7 V bias.¹ Low-voltage operation of OTFTs has been demonstrated for devices fabricated via numerous techniques including, roll-to-roll (R2R) printing,² thermal evaporation,^{3,4} vapour-phase deposition,^{5,6} and spin-coating methods,^{7–9} as well as through the use of self-assembled monolayer nano-dielectrics,^{10–12} electrolyte dielectrics,^{13–15} and ultra-thin polymer dielectrics.^{3,7,8} However, with the exception of R2R processing, none of these fabrication techniques are suitable for high-throughput manufacturing, which is critical for the development of ubiquitous, disposable electronics based on OTFTs.

R2R-compatible manufacturing techniques are commonly found in the literature, however it is rare that they are used to deposit both dielectric and semiconductor layers, something that would be required for true R2R processing.¹⁶ Examples of gravure^{17,18} and all-inkjet printing¹⁹ can be found in the literature, and while there have been many reports of spray deposition of organic semiconductors,^{20–23} spray deposition of consecutive device layers (e.g., semiconductor and dielectric layers) has not been previously demonstrated. Spray deposition involves creating an aerosol of an ink and using a carrier gas to direct the droplets on a substrate. While the technique is very simple in principle, achieving high film homogeneity and low surface roughness is extremely challenging.²⁴

Here, we demonstrate the fabrication of high hole mobility, low operating voltage OTFTs through successive

spray deposition of the semiconductor and the dielectric layers in air. For the semiconductor film, a blend of 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TES ADT) and poly(triarylamine) (PTAA) was used, while the dielectric was the fluoropolymer Cytop. The combination of these materials has previously been shown to yield OTFTs with hole mobilities of $>2 \text{ cm}^2/\text{Vs}$ in a top-gate architecture, with limited grain-boundary influence—a highly desirable characteristic for facile device fabrication.^{25,26} The spray-deposited organic films were studied using atomic force microscopy and electrically characterized at room temperature under nitrogen. Despite the simplicity of the manufacturing process, hole mobility values as high as $1.8 \text{ cm}^2/\text{Vs}$ were obtained, with an average of $0.5 \pm 0.2 \text{ cm}^2/\text{Vs}$. Low-voltage unipolar inverters were also fabricated, demonstrating excellent functionality at -6 V operation.

The top-gate, staggered transistors (Figure 1(c)) were fabricated on glass substrates. The substrates were initially ultrasonically cleaned for 10 min in a Decon 90-deionised water solution, before Au source and drain contacts were deposited via thermal evaporation through a stencil shadow mask. The semiconductors PTAA and diF-TES ADT were combined in a ratio of 1:1 and dissolved in tetralin at a concentration of 20 mg/ml. This solution was deposited using a hand-held airbrush employing an N_2 carrier gas at a pressure of 15 psi. The airbrush was held statically at a height of 30 cm above the substrates, and deposition was conducted in an ambient environment at 25°C , with a spray duration of approximately 2 s. Solvent was removed from the resulting liquid film using a hot plate held at 110°C . The Cytop was then deposited either manually or using an automated spray deposition system. For the low-voltage devices, a reduction in dielectric thickness was achieved by reducing the Cytop concentration. Hand-deposited Cytop films were cast from a solution of one part Cytop (as provided by Asahi Glass) to

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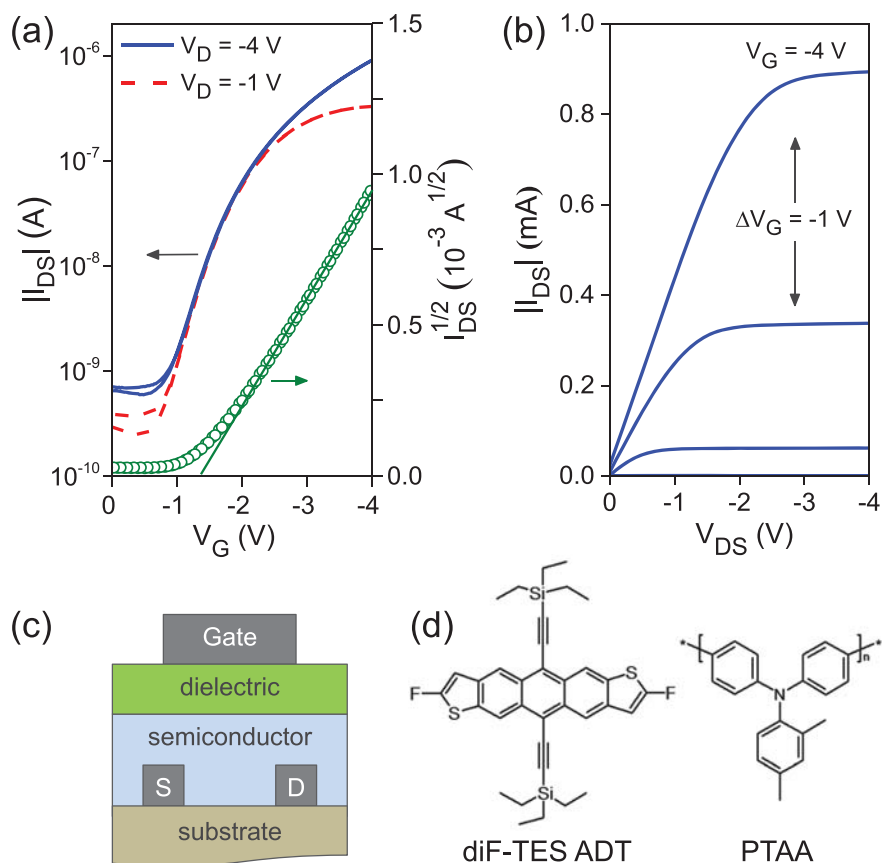


FIG. 1. (a) Transfer and (b) output characteristics of a typical all spray-cast blend-based OTFT with Cytop dielectric. Device dimensions were $W = 1000 \mu\text{m}$ and $L = 30 \mu\text{m}$. (c) Diagram of the top-gate OTFT structure used in this study. (d) Molecule structures of the small molecule diF-TES ADT and the binder polymer PTAA used in this work.

four parts fluorinated solvent, FC-43 (boiling point = 174°C , Acota Ltd), by volume. The Cytop films were dried at 100°C for 20 min before being slowly cooled to room temperature.

Cytop films were also deposited from the automated system using a modified Iwata Kustom TH airbrush with a 0.5 mm fan nozzle, in a home-built spray system. The dielectric solution used consisted of an 8:1 wt. % ratio of CT-Solv 180 (boiling point = 174°C , Asahi Glass) and Cytop, respectively. The spray-deposition system was developed based on the Prusa Mendel (iteration 2) 3-D printer framework, an open-source design. This design, coupled with a solenoid valve to initiate carrier gas flow, allows independent spatial control of processing in three orthogonal axes of translation. The solution was drawn from its cartridge via a venturi-based suction and was sprayed onto a 25°C substrate from a height of 6 cm using a N_2 carrier gas pressure of 8 psi. The travel rate of the airbrush was kept constant, at 2 cm s^{-1} . The resulting film was cross-linked by annealing the film for 30 min at each of the following temperatures: 50°C , 70°C , and 90°C , and then slowly cooled to room temperature. The semiconductor and dielectric layers were deposited and cured in ambient conditions. Finally, Al gate electrodes were deposited via thermal evaporation through a shadow mask.

High operating voltage (-40 V), hand-sprayed blend OTFTs were fabricated with an 800-nm-thick Cytop layer (determined by atomic force microscopy); comparable to that achieved by spin-casting in the work by Smith *et al.*²⁵ Resulting device characteristics of >70 such OTFTs are plotted in Figure S1, while Figures S2 and S3 display the polarized optical microscopy (POM) images of the spray-casted

and spin-coated blend films, respectively, for comparison.²⁷ These results show that while comparable hole mobilities between spin and spray-casting techniques can be achieved, hand spray-casting leads to a noticeable decrease in device-to-device uniformity. Interestingly, however, the spray-casting technique also leads to a greatly reduced threshold voltage (V_{TH}), suggesting an improved semiconductor-dielectric interface in comparison to spin-cast films. In particular, the mean V_{TH} value drops from -17 V to -4 V on spray depositing the Cytop—a significant reduction which is important for realizing low-voltage operation. Overall, low-voltage, hand-sprayed OTFTs performed well, yielding a maximum saturation hole mobility (μ_{SAT}) of around $1.8 \text{ cm}^2/\text{Vs}$ and a mean value of $0.5 (\pm 0.3) \text{ cm}^2/\text{Vs}$ with operating voltages down to -4 V . Exemplary transfer and output characteristics are depicted in Figures 1(a) and 1(b). The error given is one standard deviation of μ_{SAT} exhibited by the population of devices.

Devices were also fabricated using an automated spray deposition of the Cytop. These OTFTs also performed well, with a slightly increased uniformity in performance levels as compared to the hand sprayed Cytop-based devices, exhibiting a saturation mobility of $0.5 (\pm 0.2) \text{ cm}^2/\text{Vs}$. The improved uniformity of carrier mobility may be attributed to the more uniform dielectric thickness and, therefore, its capacitance. The dielectric thickness for hand-sprayed Cytop was 120 nm, with a roughness of $\sim 10 \text{ nm}$; however, by automating the dielectric deposition process, a 100 nm film with a roughness of $\sim 3 \text{ nm}$ was achieved, i.e., comparable to that of a spin-cast film, which typically exhibits a roughness of $<1 \text{ nm}$. AFM images of hand-sprayed and automated spray films are depicted in Figure 2.

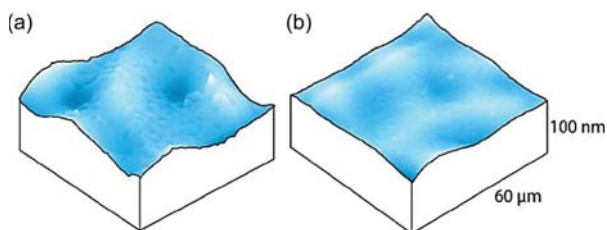


FIG. 2. AFM topography maps of $60 \times 60 \mu\text{m}$ regions of hand sprayed (a) and automated-sprayed (b) Cytop films. Film thicknesses were 100 nm and volumes are added to the topography maps to give context to the film roughness in both cases. The 100 nm scale is consistent with the topography of the AFM map.

While the mean saturation mobility is slightly lower than that demonstrated in spin-cast devices (Figure S1),²⁷ the sprayed OTFTs present three distinct advantages: (i) lower operating voltages (the spun transistors operate at -60 V), (ii) higher throughput manufacturing, and (iii) compatibility with large-area electronics manufacturing. In addition, note that while mean hole mobilities are lower than in spin-cast devices, the best performing spray-cast OTFTs exhibited a performance on-par with their spin-cast, high operating voltage equivalents and similar to the best hole mobilities reported on diF-TES ADT films.²⁸ The best performing device that was fabricated from spray-casting exhibited a saturation mobility of $\sim 1.8 \text{ cm}^2/\text{Vs}$ at -4 V operation. When compared with a mean saturation mobility of $\sim 2 \text{ cm}^2/\text{Vs}$ at -60 V for the spin-cast devices, this suggests that with further control and automation of the semiconductor deposition, performance on par with the best spin-cast devices can be expected. As for the origin of the reduced carrier mobility at lower operating voltages, a Poole-Frenkel (PF) interpretation of lateral field-dependent hole mobility can be discounted as we found that the PF effect is not significant in these diF-TES ADT:PTAA devices, in agreement with previously published work.²⁹ Figure 3(a) shows how hole mobility as a function of gate bias is not influenced by V_D , for operation between 3.3 V and 10 V.

The dominant cause of the reduced carrier mobility in OTFTs is believed to be the relatively high contact resistance between the S/D electrodes and the channel, which may be influenced by the film morphology (Figures S2 and S3).²⁷ The particular semiconductor blend films used here rely on strong vertical phase separation to form the high hole mobility, crystalline channel. However, this means that if the semiconductor film thickness is not accurately matched to the height of the source and drain electrodes, it is necessary that the charge carriers penetrate the low-carrier-mobility matrix polymer (PTAA in this case) to reach the high-mobility crystalline transistor channel. As spray deposition of the semiconductor film leads to less uniform film thickness than spin-casting, it is expected that the device contact resistance is generally higher than in spin-cast films. Figure 3(b) demonstrates that not only is the mean contact resistance in OTFTs based on spray-cast films twice as high as in devices based on spin-cast films, but the variance is also higher. Therefore, further efforts to improve the uniformity of semiconductor spray-deposition are expected to bring device performance in line with the best-performing spin-cast devices, with hole mobilities $> 2 \text{ cm}^2/\text{Vs}$.

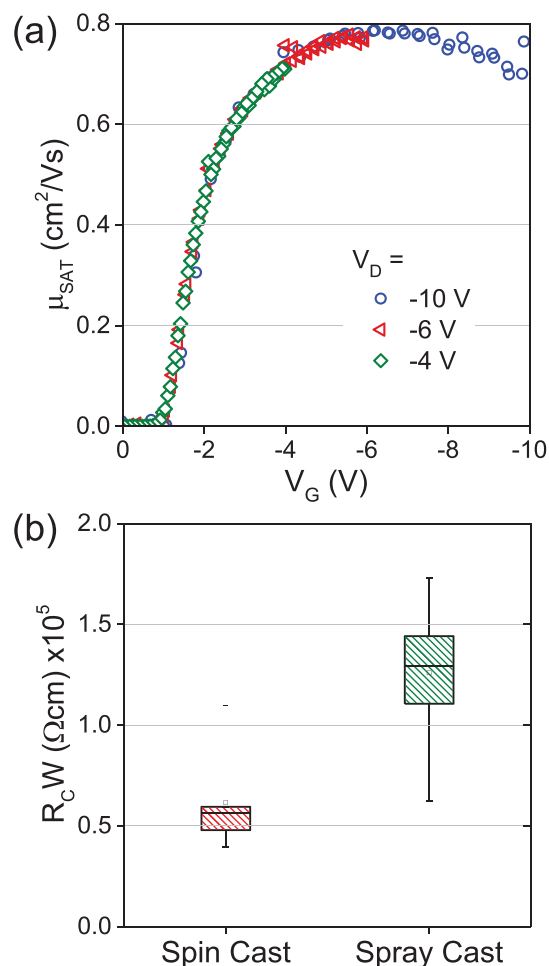


FIG. 3. (a) Hole field-effect mobility measured in saturation (μ_{SAT}) as a function of drain (V_D) and gate (V_G) bias. (b) Contact resistance ($R_{\text{C}W}$) distribution calculated for spin-cast and spray-cast blend OTFTs. The $R_{\text{C}W}$ values were calculated via the transfer line method (TLM).

To demonstrate the potential of the low-voltage OTFTs fabricated using the high-throughput spray-casting technique, simple unipolar inverters were fabricated. A saturated load circuitry configuration was employed, as depicted in the inset of Figure 4. In this configuration, two OTFTs are combined that have different channel widths, such as to create a ratio of conductivities between the drive and load OTFTs. In this work, two OTFTs with channel lengths (L) of $50 \mu\text{m}$ and channel widths (W) of $100 \mu\text{m}$ and $1000 \mu\text{m}$ were integrated, creating a drive-to-load ratio $W/L = 10$. Figure 4 depicts a transfer curve of such an inverter operating at -6 V . Strong inversion and a gain of 6 are achieved, while a noise margin of 1.3 V is very respectable for unipolar inverters operating at such low voltage. On the basis of these results, we conclude that the spray-casting process is highly promising for high-throughput manufacturing of plastic electronics. To this end, the method could prove unique for manufacturing of unconventional conformable electronics onto non-flat substrates, i.e., surfaces with different form factors.

In summary, we have demonstrated OTFTs fabricated by depositing both the semiconductor and dielectric films using a high-throughput spray-casting technique. The resulting devices exhibited hole mobilities of up to $1.8 \text{ cm}^2/\text{Vs}$ and low voltage operation (-4 V), thus making them compatible

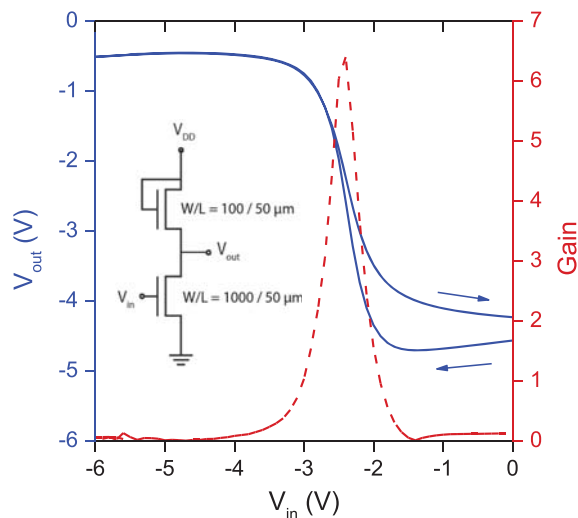


FIG. 4. Transfer characteristics measured for a unipolar p-channel inverter (NOT gate) comprised of two low-voltage OTFTs fabricated via spray-casting. The circuit exhibits excellent operation with a gain of >6 . Inset shows the saturated load circuitry employed.

with battery-powered systems, with only minimal compromise in performance. Additionally, unipolar p-channel inverters were demonstrated, operating at -6 V, with a signal gain of 6 and excellent noise margin of 43%.

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