University of Kentucky
UKnowledge

Theses and Dissertations--Electrical and Computer Engineering

Electrical and Computer Engineering

2015

Nanostructured Semiconductor Device Design in Solar Cells

Hongmei Dang
University of Kentucky, hdang2@g.uky.edu

Right click to open a feedback form in a new tab to let us know how this document benefits you.

Recommended Citation

Dang, Hongmei, "Nanostructured Semiconductor Device Design in Solar Cells" (2015). *Theses and Dissertations--Electrical and Computer Engineering*. 77.
https://uknowledge.uky.edu/ece_etds/77

This Doctoral Dissertation is brought to you for free and open access by the Electrical and Computer Engineering at UKnowledge. It has been accepted for inclusion in Theses and Dissertations--Electrical and Computer Engineering by an authorized administrator of UKnowledge. For more information, please contact UKnowledge@lsv.uky.edu.

STUDENT AGREEMENT:

I represent that my thesis or dissertation and abstract are my original work. Proper attribution has been given to all outside sources. I understand that I am solely responsible for obtaining any needed copyright permissions. I have obtained needed written permission statement(s) from the owner(s) of each third-party copyrighted matter to be included in my work, allowing electronic distribution (if such use is not permitted by the fair use doctrine) which will be submitted to UKnowledge as Additional File.

I hereby grant to The University of Kentucky and its agents the irrevocable, non-exclusive, and royalty-free license to archive and make accessible my work in whole or in part in all forms of media, now or hereafter known. I agree that the document mentioned above may be made available immediately for worldwide access unless an embargo applies.

I retain all other ownership rights to the copyright of my work. I also retain the right to use in future works (such as articles or books) all or part of my work. I understand that I am free to register the copyright to my work.

REVIEW, APPROVAL AND ACCEPTANCE

The document mentioned above has been reviewed and accepted by the student's advisor, on behalf of the advisory committee, and by the Director of Graduate Studies (DGS), on behalf of the program; we verify that this is the final, approved version of the student's thesis including all changes required by the advisory committee. The undersigned agree to abide by the statements above.

Hongmei Dang, Student

Dr. Vijay Singh, Major Professor

Dr. Caicheng Lu, Director of Graduate Studies

NANOSTRUCTURED SEMICONDUCTOR DEVICE DESIGN IN SOLAR CELLS

DISSERTATION

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the College of Engineering at the University of Kentucky

By
Hongmei Dang

Lexington, Kentucky

Director: Dr. Vijay P. Singh, Professor of Electrical and Computer Engineering

Lexington, Kentucky

2015

Copyright © Hongmei Dang 2015

ABSTRACT OF DISSERTATION

NANOSTRUCTURED SEMICONDUCTOR
DEVICE DESIGN IN SOLAR CELLS

We demonstrate the use of embedded CdS nanowires in improving spectral transmission loss and the low mechanical and electrical robustness of planar CdS window layer and thus enhancing the quantum efficiency and the reliability of the CdS-CdTe solar cells. CdS nanowire window layer enables light transmission gain at 300nm-550nm. A nearly ideal spectral response of quantum efficiency at a wide spectrum range provides an evidence for improving light transmission in the window layer and enhancing absorption and carrier generation in absorber. Nanowire CdS/CdTe solar cells with Cu/graphite/silver paste as back contacts, on SnO_2/ITO-soda lime glass substrates, yield the highest efficiency of 12% in nanostructured CdS-CdTe solar cells. Reliability is improved by approximately 3 times over the cells with the traditional planar CdS counterpart. Junction transport mechanisms are delineated for advancing the basic understanding of device physics at the interface. Our results prove the efficacy of this nanowire approach for enhancing the quantum efficiency and the reliability in window-absorber type solar cells (CdS-CdTe, CdS-CIGS and CdS-CZTSSe etc) and other optoelectronic devices.

We further introduce MoO_{3-x} as a transparent, low barrier back contact. We design nanowire CdS-CdTe solar cells on flexible foils of metals in a superstrate device structure, which makes low-cost roll-to-roll manufacturing process feasible and greatly reduces the complexity of fabrication. The MoO_3 layer reduces the valence band offset relative to the CdTe, and creates improved cell performance. Annealing as-deposited MoO_3 in N_2 reduces series resistance from 9.98 Ω/cm^2 to 7.72 Ω/cm^2, and hence efficiency of the nanowire solar cell is improved from 9.9% to 11%, which efficiency comparable to efficiency of planar counterparts. When the nanowire solar cell is illuminated from MoO_{3-x}/Au side, it yields an efficiency of 8.7%. This reduction in efficiency is attributed to decrease in J_{sc} from 25.5mA/cm^2 to 21mA/cm^2 due to light transmission loss in the MoO_{3-x}/Au electrode. Even though these nanowire solar cells, when illuminated from back side exhibit better performance than that of nanopillar CdS-CdTe solar cells, further development of transparent back contacts of CdTe could enable a low-cost roll-to-roll fabrication process for the superstrate structure-nanowire solar cells on Al foil substrate.

KEYWORDS: Nanowire CdS-CdTe Solar Cells; Light Transmission; Quantum Efficiency; Reliability; MoO_{3-x} Back Contact.

Hongmei Dang

Student's Signature

March 10, 2015

Date

NANOSTRUCTURED SEMICONDUCTOR DEVICE DESIGN IN SOLAR CELLS

By

Hongmei Dang

Dr. Vijay Singh
Director of Dissertation

Dr. CaiCheng Lu
Director of Graduate Studies

March 10, 2015
Date

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my advisor, Dr. Vijay P. Singh, who first introduced me to the fields of solar cell and nanotechnology. He gave me the best opportunity to work on this interesting and challenging research topic. Special thanks also goes to Drs. Zhi Chen, Todd Hastings, Y-T Cheng, and William Murphy, who served as my Ph.D. dissertation committee. I extend my thanks as well to the numerous professors whose classes I attended in the doctoral program at the University of Kentucky. Finally I would like to honor my parents who greatly supported me to pursue my graduate studies in the United States.

Table of Contents

List of Tables

List of Figures

Chapter 1 Introduction

1.1 World Energy Outlook

World annual energy consumption is predicted to grow from the approximately 15 TW/year (1 TW = 10^{12} W) at present to about 30 TW/year by 2050[1]. Struggling to meet this huge demand, the global energy sector will also face two pressing issues: declining fossil reserves and climate change caused by artificially produced greenhouse gas emissions. According to statistics of international energy agent[2], it can be predicated that at our current burn rate of oil, oil reserves are between 40 and 80 years globally and between 50-150 years if the resource base is included[2]. Nature gas reserves can maintain between 200-500 years[2]. Similarly, coal reserves are estimated between 200-2000 years[2]. Although fossil energy is likely to be relatively inexpensive resource for hundreds of years, obviously beyond 2050, they are exhaustible and recovery of coal, oil and natural gas presents impossible. Further, associated release of CO_2 has dramatically altered and continues to changing the composition of the atmosphere and could create detrimental effect on global temperature, sea levels, and weather patterns[2]. In addition, price of fossil energy will naturally rise due to strongly increased energy demand and their exhausted supply. Hence, driving future energy policy scenarios is based on renewable energy. (And the discussion above also shows that fossil energy is likely to be a relatively inexpensive method of obtaining primary power even in 2050 and beyond, given its adequate supply globally in the various forms of oil, gas, and coal).

There is a wide variety of renewable energy sources: nuclear power, hydroelectric power, wind, biomass and solar energy. Nuclear power is considered a leading candidate for reduced-carbon-emission electricity production. There is many concerns, however,

including uncertainty about the size of nuclear fuel reserves, the efficiency of nuclear reactors when using lower-grade uranium ores, and the likelihood of finding satisfactory solutions for nuclear waste disposal[2]. In terms of renewable sources, hydroelectricity is relatively inexpensive, benign, and available in many areas of the world. However, globally, the amount of technically feasible hydroelectric power has been estimated to be approximately 1.5 TW[3]. Hence, hydroelectricity will not make a significant contribution toward meeting the 10-20 TW global carbon-free power requirements in 2050 year[3]. Wind power is approaching competitiveness with conventional power production and may be considered as an important source in meeting future energy needs. Considering practical sitting constraints, total usable wind energy production over the entire globe is estimated about 2-4 TW, much less than the 30 TW level[3]. In addition, biomass is impossible to become an alternative power for massive deployment in the future due to very inefficient property and only storing less than 1% of the total incident energy.

Solar energy is a renewable, and a pollution–free source of energy that is ubiquitously available in sufficient quantity. With roughly 175,000 TW of solar power striking the earth's surface, a practical and feasible solar power potential is estimated about 600TW for terrestrial application[1,4]. Thus, for a 10% efficient solar farm, at least 60 TW of power could be supplied from terrestrial solar energy resources, and this amounts to twice the projected world energy need by 2050[4]. Hence, solar energy is, in fact, the only renewable resource that has enough terrestrial energy potential to produce 10-20 TW carbon-free power by 2050 year[5]. In a word, solar technology becomes as an integral part of the solution to meet the world's energy demand.

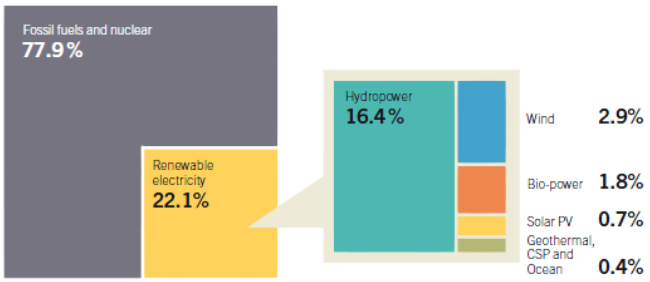
1.2 Solar Energy Current status and Future Prospects

Solar energy makes our society clean from one that relies on fossil fuels to one that utilizes sustainable energy sources. World solar power generation grew rapidly and growth rate was 35% in 2013[5]. The growth of solar power accounted for more than half of renewable energy generation growth. Solar photovoltaic (PV) electricity constitutes the fastest growing renewable energy technology in the world. In Germany, more than 1.3 million solar power plants generated 5.3% of electricity consumption[6], in Italy; PV systems generated 7% of electricity consumption, Belgium, Bulgaria, Czech Republic[6], Greece and Spain PV generation also exceeded 3% of electricity demand[6]. While fast growth rate, due to a small base, global 135GW of solar PV installation capacity in 2013 is only 0.7 percent of total amount of electricity that was generated that year by all sources[6]. Figure 1a and 1b shows global electricity production from various power sources at the end of 2013 and 2050[7]. As shown in Figure1, fossil fuels dominated and generated 78% of global electricity. Power capacity from renewable energy increased from 19% at 2012 to 22.1% at 2013[7], primarily due to growth of hydropower. Solar electricity accounted for a very small amount of electrical generation in most of countries. Therefore, it is expected that solar energy deployment will be greatly increased.

From renewable market report forecast, solar energy will supply 2% of global electricity generation before 2019[5]. By 2030, without major changes of policy, contribution of PV to the global electricity demand could be between 7% and 11%[5], and renewable energy will provide one-third of total generation. The latest long-term photovoltaic (PV) technology roadmap shown that, by 2050, approximately 16% of world electricity supply could be delivered by PV[5], and concentrating solar power (CSP)

plants will provide an additional 11% of solar thermal electricity, and total renewable energy will provide 79% of global electricity production[5]. In short, by 2050, these solar technologies will prevent the emission of more than 6 billion tons of carbon dioxide per year[5]. This amount is more than all current energy related CO_2 emissions from the United States or almost all of the emissions from the transport sector worldwide today[5]. It is predicted that 1700 GW of PV will be deployed by 2030, and at 2050, PV power will be deployed 4670GW[5]. To achieve the vision, the installation of total PV capacity each year needs to rise rapidly, from 36 GW in 2013 to 124 GW per year on average, with a peak of 200 GW per year between 2025 and 2040[5].

a



b

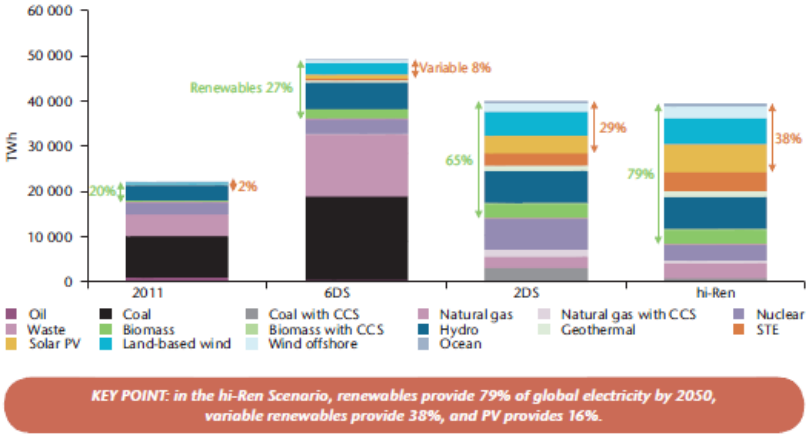


Figure 1, Estimated renewable energy share of global electricity production, a)end of 2013, b)2050.

1.3 Potential PV Cost Reduction

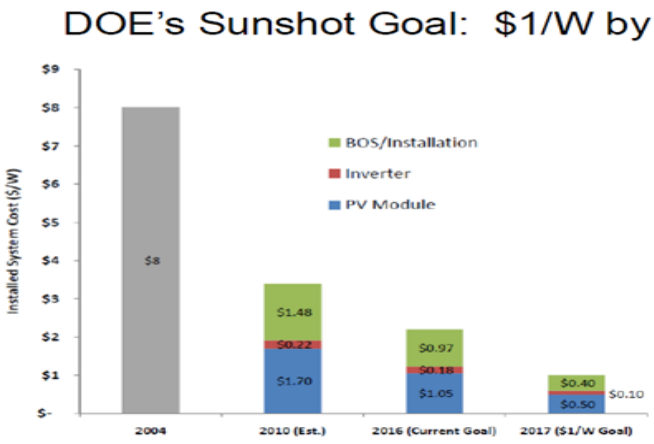
Wide-scale deployment of solar cells to date has been blocked by their cost. To achieve large deployment of 300-600GW of PV at 2019, 1700GW of PV at 2030 and 4670GW of PV at 2050 from current deployment of 135GW of PV, it is important to make the solar electricity cost competitive with other sources of energy at least by 2020. As compared with the cost of coal-based electricity with approximately $0.04/kilowatt-hours (kWh)[1], the present cost of photovoltaic-generated electricity is in the range of $0.20 to $0.35/kWh[1]. Costs of cells and modules will decline further when deployment increases and technology improves in the next two decades. Figure 2a and 2b show the roadmap of expecting module cost. According to Figure2a, it is expected that module costs will be fallen to $0.3/W to $0.4/W by 2035[5]. Utility-scale capital expenditures cost will reach the lowest at about 2020, and would fall below $1/W by 2030 on average, and would then reach a level of $0.7/W by 2050[5].

The SunShot Initiative strongly supports development of low-cost and high-efficiency photovoltaic (PV) technologies in order to achieve roadmap cost reduction. According to Figure 2b, SunShot Initiative has made cost target of $0.06 per kilowatt-hour for utility-scale PV by 2020. Currently, the solar industry is already more than 60% of the way to achieve the Sunshot cost target[8].

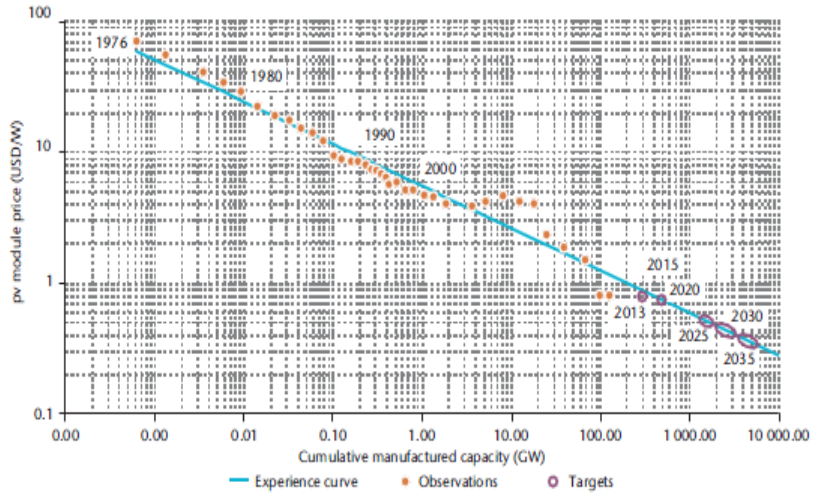
Hence, in support of cost reduction target to double renewable energy generation by 2020, the Energy Department invested more than $59 million funding to support solar energy innovation today. The Department of Energy is making $45 million funding to quickly transfer innovative solar manufacturing technologies to market, and is also awarding more than $14 million to help communities develop multi-year solar

deployment plans for installing solar electricity in homes, communities and businesses[9]. These funding investments will greatly promote development of cost-effective solar electricity competitive with fossil fuel electricity.

a



b



Notes: Orange dots indicate past module prices; purple dots are expectations. The oval dots correspond to the deployment starting in 2025, comparing the 2DS (left end of oval) and 2DS hi-Ren (right end).

KEY POINT: This roadmap expects the cost of modules to halve in the next 20 years.

Figure 2, Roadmap of expecting module cost a) Sunshot Initiative target at 2017 year, and b) at 2035.

1.4 Current Photovoltaic Materials and Devices

Photovoltaics (PV) use semiconductor materials to generate electricity from solar energy. The PV effect was discovered in 1839 through studying the effect of light on electrolytic cells by Becquerel[10]. Solar cells developed rapidly in the 1950s owing to space programs and satellites utilization of crystalline Si solar cells with efficiency of 6–10%, in addition, the energy crisis of the 1970s greatly stimulated research and development for PV[10]. Current PV materials devices are dominated by crystalline Si solar cells, multicrystalline Si solar cells, thin-film amorphous Si solar cells, CdTe thin film solar cells, CIGS solar cells, CZTSSe(CZTS)solar cells, and perovskite solar cells. The recent results on these leading types of solar cells are described in the following.

1.4.1. Shockley and Queisser Efficiency Limits

The limiting efficiency of a single junction solar cell was analyzed by Shockley and Queisser (1961). According to Shockley and Queisser model, the thermodynamic efficiency of an ideal single homojunction solar cell is estimated as 31%. The efficiency of a single homojunction solar cell is limited by absorption losses of photons with energies below the bandgap energy and thermal relaxation of carriers created by photons with energies above the bandgap energy[10]. Figure 3 shows the evolution of world-record efficiencies of laboratory cells. Table 1 shows currently confirmed terrestrial cell and module efficiencies measured under the global AM1.5 spectrum at 25°C.

1.4.2. Silicon Solar Cells

1.4.2.1 Crystalline Silicon Solar Cells

Crystalline silicon is the most mature technology and has been benefitted from decades of development by the integrated circuit (IC) industry. Most commercial Si solar

cells utilized boron-doped single-crystal wafers (around 400 μm thick) grown by the Czochralski (CZ) process. As shown in figure 3, the average efficiency of silicon solar cell has improved in the last twenty years by about 0.3% per year[10]. The improvement of these efficiencies was due to improved contact and surface passivation of the cells along the front and rear surfaces, as well as an improved understanding of the role of light-trapping in Si solar cells. By the end of 2014, crystalline Si solar cells have achieved open-circuit voltage V_{oc} of 740 mV, short-circuit current density J_{sc} of 41.8 mA/cm^2, fill factor of 82.7% and power conversion efficiency of 25.6%, which were fabricated by the Panasonic HIT[11].

Modules usually have to guarantee a lifetime of 25 years at minimum 80% of their rated output, or a lifetime for 30 years at 70% of the rated output. The module efficiencies lag efficiency of the laboratory cells. The best-performing commercial modules were based on back-junction and interdigitated back-contact. At the beginning of 2015, the commercial crystalline Si modules have reached fill factor of 80.3% and efficiencies of 22.9% by UNSW/Gochermann, and fill factor of 80.1% and efficiencies of 22.4% by SunPower company[11].

1.4.2.2 Multi-Crystalline Silicon Solar Cells

Multi-crystalline silicon solar cells have the greatest market share followed by mono-crystalline silicon photovoltaics. Multi-crystalline silicon solar cells can reduce the cost requirements for the mounting structure and installation. The Multi-crystalline Silicon industry was expecting to reduce polysilicon prices, and improve wire cutting technology, which leads to reduced wafer thicknesses and keeps multi-crystalline silicon solar cells competitive. For world-record efficiencies of laboratory cells, the multi-crystalline Si solar cells has achieved open-circuit voltage V_{oc} of 662.6 mV, short-circuit current

density J_{sc} of 39.03 mA/cm^2, fill factor of 80.3% and power conversion efficiency of 20.8%, demonstrating efficiencies of more than 20%[11]. The For confirmed module efficiency, multi-crystalline silicon modules have demonstrated fill factor of 76.2% and efficiencies of 18.5%[11]. Although multi-crystalline Si modules have lower module efficiency compared with crystalline Si modules, their lower cost manufacture techniques make them cost-effective PV modules, hence having larger market share than crystalline Si modules.

1.4.2.3 Thin-film Amorphous and Polycrystalline Silicon Solar Cells

Amorphous and thin-film polycrystalline silicon solar cells are all alternatives to crystalline Si solar cells. Compared to crystalline silicon cells, thin-film Si solar cells have the following important advantages that: i) The thickness of Si can be reduced from 400μm to 50 μm; ii) devices can be deposited at low temperature (< 200 °C), enabling the fabrication of lightweight, flexible laminates on low-cost substrates; iii) devices can be fabricated by low cost and high throughput roll-to-roll processing on flexible substrates. The unique features provided competitive advantages in consumer products and building integrated photovoltaics markets. However dangling (Si-H) bonds can be destroyed under visible light, the amorphous Si cells were hampered by poor stability and inferior efficiencies. Thin film amorphous Si techniques usually applied hydrogen passivation techniques to reduce dangling bonds and increase material quality. The best successful laboratory amorphous cells were achieved as 10.2% conversion efficiency (V_{oc}=896mV, J_{sc}=16.36 mA/cm^2, and FF=69.8%)[11]. In addition, for the best commercial modules, stabilized efficiency remains low and was 6–7%. At present, about 8–10% of the worldwide PV production uses amorphous Si technology[10].

1.4.3 Thin-Film Chalcogenide Solar Cells

1.4.3.1 Cadmium Telluride (CdTe) Solar Cells

CdTe solar cells were manufactured by single company of First Solar and have the lowest manufacturing costs currently. First Solar's success has been due to their ability to integrate various process steps into an in-line manufacturing process which reduce the processing time from glass to a finished module down to 2.5 hours. The biggest challenge for CdTe lies in the improvement of device efficiency. First solar collaborated with General Electric company and made significant process for efficiency improvement. The recorded laboratory cells have been confirmed with V_{oc} of 876mV, J_{sc} of 30.25 mA/cm^2, FF of 79 .4% and power conversion efficiency of 21% at 1.0623 cm^2 area[11]. Module efficiency has been raised from 13.5% to current levels of 17.5% by the end of 2014 through a combination of process integration, research, and development[11]. In the short term First solar is targeting over 18% as an achievable goal for module efficiency. The main progress has been made in enhancement of photocurrent by replacing the FTO with advanced TCOs such as cadmium stannate and ITO. However, the improvement was not trivial because ITO is expensive and cadmium stannate is a complex material.

One issue about large-scale CdTe manufacturing is related with cadmium toxicity and tellurium availability. Cadmium is a toxic element, and it can continue to be produced as a natural byproduct of Zn mining. However tellurium availability is limited. Hence, the optimum solution for CdTe PV technique is to sequester cadmium in an environmentally beneficial manner, and to implement 100% recycling in order to address the issue of Te availability.

1.4.3.2 Copper Indium Gallium Selenide (CIGS) Solar Cells

Among I–III–VI compounds, copper indium diselendide ($CuInSe_2$ or CIS) CIS has beneficial properties for thin-film solar cells. CIS has a band gap of 1.05eV slightly off the maximum efficiency energy gap of 1.5eV. The real breakthrough in CIS thin-film solar technology was from the pioneering work of Boeing Corporation, where three-source co-evaporation of Cu, In, and Se elements raised the efficiency from 5.7% in 1980 to above 10% in 1982[10]. Efficiency improvements attained by NREL were due to bandgap engineering for 1.5eV by adding Ga and S and improvement of the absorber layer by adding Na, resulting in CIGS solar cells.

CIGS was the efficiency leader among thin film technologies cells but were currently exceeded by CdTe solar cells with 21% efficiency. At the beginning of 2015 year, the world-record efficiency in the laboratory is 20.5% with V_{oc} of 752mV, J_{sc} of 35.3 mA/cm^2, FF of 77.2% and was achieved by Solibro company[11]. At present, the performance of commercial modules is only about 15.7%, which is much lower than that of CdTe modules[11]. Difference between laboratory cells and module was attributed to the quality of the absorber layer.

Commercial production of CIGS began in 2007, with a few companies operating facilities with 10-30 MW/year capacities but the large production has not happened because reproducibility and production yield have proven to be challenging[12]. In terms of large-scale terrestrial applications, this material has a disadvantage because indium and gallium are very limited resources.

1.4.3.3 Earth Abundant Copper Zinc Tin Sulfide Selenide (CZTSS) Solar Cells

Driven by concerns about the availability of In, Te, Ga and Ge in the current 2nd generation CIGS thin-film solar cells, earth abundant materials including oxides and

sulfides of base metals (e.g., Fe, Cu) with band gaps in the range of 1-2 eV were developed. The most successful system to date has been copper-zinc-tin-sulfide (selenide), or CZTS, which were investigated by IBM group[13]. CZTS shares similar device structures and fabrication techniques with CIGS. The similarities to CIGS solar cells have accelerated CZTS solar cells' initial success, and champion CZTS devices in the laboratory has approached 12.6% efficiency with V_{oc} of 513.4mV, J_{sc} of 35.21mA/cm^2 and FF of 69.8%[11]. Even so, these same similarities may become limitations in the long run. Currently, the CZTS solar cells are in the experimental research stage and haven't been commercially manufactured by industry. It needs further investigation that the CZTS solar cells deserve for further investment.

1.4.3.4 Perovskite Solar Cells

Perovskite solar cells are one of the hottest prospects in current solar energy research, offering high power outputs from low-cost materials that utilized low-cost and simple solution processes to form devices. Organic/inorganic halides perovskite solar cells have strongly attracted the attention of the photovoltaic community when efficiencies of 10% were first achieved since late 2012. Interest has soared in the innovative device structures as well as new materials, promising further improvements. The excellent properties and the innovative device structures in perovskite solar cells have resulted in a enormous increase of publications. Solution processed perovskite photovoltaics have achieved efficiencies of 20.1% for a very small area 0.1cm^2, with V_{oc} of 1059mV, J_{sc} of 24.65mA/cm^2 and FF of 77%[11]. The cells were fabricated by the Korean Research Institute of Chemical Technology (KRICT) and measured at Newport Technology and Applications Center. Hence perovskite solar cells have been established as a robust candidate for commercialization.

However, perovskite cells' power conversion efficiency often varies depending on how it is measured, suggesting an underlying instability in the cells' light-gathering perovskite materials. In addition, perovskite cells' performance is greatly degraded from about 15% efficiency to around 5% efficiency in two days, and the most reliable perovskite cells can maintain 17 days[14]. Hence, it is impossible to photovoltaic panels working for a decade or more. Secondly, the highest efficiency solar cells were reported with CH3NH3PbI3 which includes unfriendly element lead, and when without inclusion of lead, perovskite solar cells showed obviously reduced power conversion efficiency. Thirdly, researchers are struggling to extend the range of the light absorption wavelengths, which is a key strategy for improving their efficiency or so achieved by typical silicon or thin-film solar cells. In addition, the basic working mechanisms are still being debated, which will be crucial to design the optimum device configuration and maximize solar cell efficiencies. Hence the scientific challenges developing environment friendly perovskite materials and addressing efficiency and reliability issues are keys to make this technology market-viable.

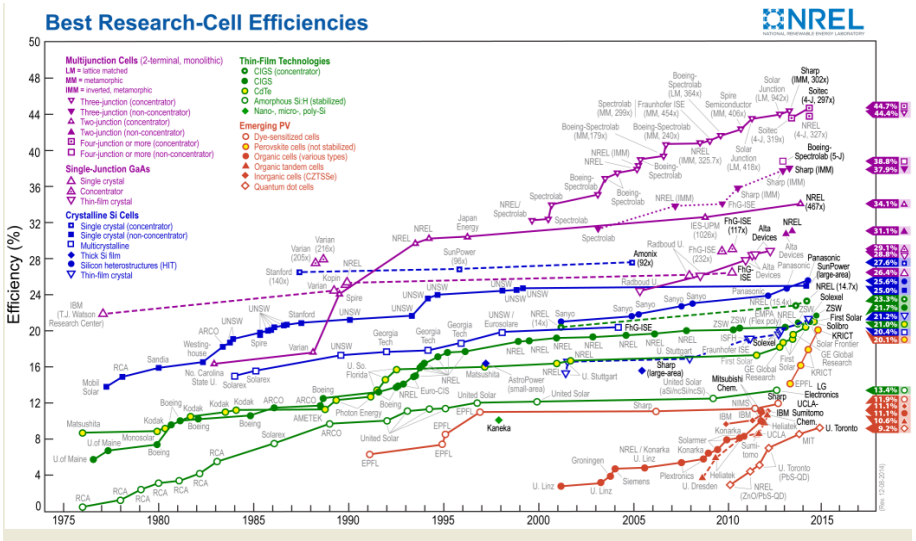


Figure 3, The evolution of world-record efficiencies of laboratory cells[15].

Table 1 Confirmed terrestrial cell and module efficiencies measured under the global AM1.5 spectrum (1000 W/m^2) at 25°C[11]

Materials	Efficiency (%)	Area(cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	I_{sc} (A)	Fill Factor(%)
Si Cell (crystalline)	25.6 ± 0.5	143.7	0.74	41.8		82.7
Si Module (crystalline)	22.9 ± 0.6	778	5.60		3.97	80.3
Si Cell (multicrystalline)	20.8 ± 0.6	243.9	0.6626	39.03		80.3
Si Module (multicrystalline)	18.5 ± 0.4	14661	38.97		9.149	76.2
Si Cell (amorphous)	10.2 ± 0.3	1.001	0.896	16.36		69.8
Si Cell (microcrystalline)	11.4 ± 0.3	1.046	0.535	29.07		73.1
a-Si/nc-Si (thin-film cell)	12.7 ± 0.4	1.000	1.342	13.45		70.2
a-Si/nc-Si (tandem)	12.2 ± 0.3	14322	202.1		1.261	68.8
CdTe Cell	21.0 ± 0.4	1.0623	0.8759	30.25		79.4

CdTe Module	17.5 ± 0.7	7021	103.1		1.553	76.6
CIGS Cell	20.5 ± 0.6	0.9882	0.752	35.3		77.2
CIGS Module	15.7 ± 0.5	9703	28.24		7.254	72.5
CZTSS Cell (thin film)	12.6 ± 0.3	0.4209	0.5134	35.21		69.8
CZTS Cell (thin-film)	8.5 ± 0.2	0.2382	0.708	16.83		70.9
Perovskite (thin film)	20.1 ± 0.4	0.0955	1.059	24.65		77.0
GaAs Cell (thin film)	28.8 ± 0.9	0.9927	1.122	29.68		86.5
GaAs Module (thin film)	24.1 ± 1.0	858.5	10.89		2.255	84.2

1.5 Current PV Module Manufacturing Cost and Market Shares

To been projected to meet the U.S. Department of Energy SunShot Initiative goal of $1/W by 2020, most of the PV leading technologies are emphasized on reducing manufacturing costs. For most of the commercial module technologies, efficiency is adequate, and emphasis is on developing cost-effective manufacturing technologies that

can significantly lower the production cost below $1/W. Table 1 shows manufacturing costs and market shares of the leading PV technologies.

The manufacture of solar PV systems basically comprises of four phases: 1) production of the semiconducting material; 2) production of the PV cells; 3) production of PV modules, a process whereby the cells are encapsulated with protective materials and frames to increase module strength; and 4) installation of PV modules, including the inverter to connect the PV system to the grid, the power control systems, energy storage devices and the final installation in residential or commercial buildings or in utility-scale plants. The cost of a PV module typically ranges between 30-50% of the total cost of the system. The remaining costs include the balance of system and the installation, which can be 20% for utility-scale PV plants, 50-60% for residential applications, and as a high as 70% for off -grid systems, including energy storage and back-up power[5].

Hence, to make PV system price to $1/W of Sunshot Initiative goal, price of PV module has to be reduced to around $0.5/W. PV module prices have declined very rapidly due to market competition, increasing industrial production and improved efficiency. The module cost of crystalline Si PV systems have fallen by more than 60% over the last several years. In 2012, average manufacturing cost of Si PV modules was $0.75/W, and currently, the cost of silicon PV modules is $0.65/W[16].

Compared with crystalline Si PV systems, the production of thin film PV system is less energy intensive and requires significantly less semiconducting material. Thin film PV modules are therefore generally cheaper. First Solar sets thin-film CdTe module efficiency of 17.5%, which makes that average manufacturing cost of CdTe modules is reduced to $0.61/W, becoming the cheapest of solar modules[17]. First Solar expects its

average manufacturing cost to be reduced to $0.35/W in 2018[17]. That will make the total installed cost of a CdTe module (including racking and inverters) from approximately $1.59/W at present to below $1/W by 2017, meeting the US Sunshot Initiative goals at least three years ahead of time, and occupying a large market share.

While the CdTe technology is growing sufficiently fast, thin-film CIGS module production is still in the beginning stages. This is due to difficulties between laboratory and large-scale production technologies. 15.7% module efficiency made by Solar Frontier has promoted that the average manufacturing cost of CIGS models is reduced to $0.64/W[16]. It is expected that rate of decline will be steep for CIGS thin-film modules, and module manufacturing cost will be reduced to $0.5/W in next several years. Continued cost reductions of PV systems are essential for accelerating the attainment of grid-parity of electricity generated using on-grid solar PV systems .

Currently, crystalline silicon and the so-called thin-film technologies dominate the global PV market. Crystalline silicon PV is the most developed technique and currently dominant PV technology with approximately 85-90% of the PV market share[18]. All the thin-film technologies combined have 13% of the market, where CdTe and CIGS PV techniques share 6% and 2% of the market respectively[18]. With increased deployment of solar electricity and shortage of Si materials, quick penetration of the thin film PV technologies into the world PV market is therefore required. It is expected that CdTe and CIGS modules will increase their market share in the world PV market in coming years due to their lower costs.

1.6 PV Future-Low Cost, Reliable and Earth Abound Solar Cells

1.6.1 Current PV Issues and Requirements for Future PV Technologies

While significant reductions in manufacturing costs of various commercial PV modules has been made, research are doubting whether these materials and synthesis methods can achieve truly inexpensive and global-scale solar electricity. Considering monocrystalline silicon solar cells, the most important factor limiting the development of crystalline Si solar cells is the production cost of the 250-300mm thick crystal Si wafer due to indirect energy gap and low absorption coefficient property of Silicon. Production of the high-purity silicon, high-temperature crystal growth, and vacuum processing methods used for doping and contact application are all energy-intensive techniques. It has been reported that a third or more of the total energy was consumed on the purification of metallurgical grade silicon to solar grade. Material cost is the largest contributor to the overall cost of crystalline Si cells. Due to the directionality and strength of the covalent bond in Si, Si is hard to cut through and requires high temperatures to process Si[19]. It excludes attempts to synthesize Si by low-cost methods. Therefore, the electricity consumption for Si solar modules is very high. For example, if crystalline Si cells are deployed to generate about 4% of the worldwide electricity production, the amount of crystalline Si wafers required is about 2,350,000 tons/year[19]. This amount of crystalline Si wafers would require about 1.6×10^{12} kWh or about 10% of the world electricity production[19]. High energy requirement for production of crystalline Silicon modules is a fundamental limit to make a noticeable contribution to electricity generation. Thin film CdTe and CIGS solar cells use very thin layers of semiconductor material deposited on a low cost material such as glass, plastic or metal, hence they have been projected to meet SunShot Initiative cost goal. However, the high performance CdTe and CIGS solar modules require high-

temperature and high vacuum processing, specifically deposition and annealing at around 500C-600 °C, resulting in high energy consumption for a solar cell module[1]. III-V GaAs compound semiconductor solar cells are usually fabricated on single crystal substrates using expensive epitaxial deposition techniques and hence are extremely expensive[1]. In other words, all commercial PV technologies involve the use of energy intensive thermal and vacuum-based techniques, which actually offset their advantages to the world electricity generation.

To achieve approximately 5TW deployment of PV at 2050 (16% of world electricity supply delivered by PV), materials availability is the important for low-cost solar cells. It is inevitable that silicon will face shortages. For CdTe solar cells, it has been estimated that existing mineral reserves would achieve 0.3TW of installed capacity before tellurium scarcity becomes a limiting factor in cost. Based on current tellurium refinery output, a maximum production rate of CdTe solar cells is 5GW/year[1]. For CIGS solar cells, according to the limited availability of indium, Ga and Se, similar capacity and growth limits were estimated as 0.09TW and 7GW/year respectively[1]. In addition, these cells also contain extremely rare and toxic elements. It is the potential dangerous to introduce large quantities of the toxic elements into the ecosphere through manufacturing and waste handling[1]. Thus, while Silicon, CdTe and CIGS solar cells may be important parts of a diversified renewable energy solution, their overall deployment of less than 1TW has limited impact on the 30TW energy demand by 2050[1].

1.6.2 Solution Processed and Earth Abundant Solar Cells

In response to truly inexpensive and wide-scale photovoltaic electricity generation, there are needs for less energy-intensive deposition methods such as solution-based

deposition. Solution-based deposition methods have the advantage of being low-temperature and scalable as well as no vacuum requirements, hence avoiding abundant energy consumption on thermal and vacuum system and greatly reducing manufacturing costs. The solution based deposition methods are suitable for wide-scale fabrication of inexpensive solar cells on a variety of supporting substrates. The methods can not only fabricate traditional solar panels but also coat non-planar objects, which make them possible for integration of photovoltaics into various form components. Thus, solution synthesis methods are necessary to produce low cost photovoltaic modules for various home, business and on-grid and off-grid applications.

To meet massive deployment of low cost PV modules by 2050, several basic requirements for ultra-low-cost photovoltaics can be summarized: abundant, inexpensive materials; low-temperature, atmospheric fabrication of crystalline materials; scalable synthesis on low-cost substrates; suitable efficiency and stability and low-toxicity[1]. There are nine inorganic materials which have been identified as having both the potential for annual electricity production in excess of worldwide demand and material extraction costs less than that of crystalline Si. It is possible, through low temperature solution synthesis, to synthesize polycrystalline thin films of the earth abundant, stable and non-toxic materials. For example, polycrystalline Cu_2O, Cu_2S, and CuO, have been known as earth abound materials for solar cells, can be produced by electrochemical deposition near room temperature[1]. The ability to synthesize abundant photovoltaics using low-temperature, solution-based synthesis methods is essential to reduce PV system cost for wide-scale implementation of low-cost photovoltaic electricity generation, and is a great interesting area for future research.

1.6.3 Nanostructured Earth Abundant Solar Cells by Low-Temperature, Solution Synthesis Methods

Ultra-low cost solution-based synthesis generally results in materials of poorer crystallinity and phase purity and more defects than those produced by vacuum and high temperatures deposition methods[1]. Thus, the solution based methods can significantly reduce costs, however, they will create high concentrations of grain boundaries, charge traps and recombination centers, which limit the distances over which photogenerated carriers can be transported and collected. Thus, techniques need to be developed for producing suitable structures of these solution-synthesized materials that enable the efficient carrier collection.

Photovoltaic nanostructure allows the use of these solution-based methods to achieve high efficiency and low cost solar cells. Usually, materials synthesized by low cost solution methods have a large number of defects and impurity, reducing minority carrier lifetime[1]. Nanostructure diameter can be tuned to match the diffusion length of minority carriers and the thickness can be tailored to maximize light trapping and absorption. Hence, the nanostructure solar cells are still thin enough that photogenerated carriers can be efficiently transported before combination, while the overall cell thickness is sufficient to absorb all incident radiation. Nanostructure can provide considerable performance enhancements for low grade photovoltaic materials fabricated by low cost solution methods. Hence, photovoltaic materials have been nanostructured to simultaneously achieve high efficiencies and low cost.

The development of ultra-low-cost nanostructure inorganic solar cells, which utilize abundant materials and inexpensive solution based fabrication methods, is in the early stage and promising. These devices are inherently more stable than organic-based

equivalents, which make them considerably interesting and are extremely promising as the cheapest solar cells. Through continued development of nanoscale materials and devices, inexpensive solar power will be able to meet world energy demands.

Chaper 2 Fundamental Theory of Solar Cells

2.1 Solar Cell Operation Principle

2.1.1 p-n junction

A solar cell is a device which converts sunlight into electricity. Light shining on the solar cell produces both a current and a voltage. This process requires a material to absorb light and raise electrons to a higher energy state, and the transport of this higher energy electron from the solar cell into an external circuit. Then, electrons dissipate their energy in the external circuit and returns to the solar cell. Photovoltaic energy conversion often uses semiconductor materials and inorganic-organic materials in the form of a p-n junction.

In a typical photovoltaic cell, p-n junctions are formed by joining *n*-type and *p*-type semiconductor materials, as shown in figure 4. Since the *n*-type region has a high concentration of electrons and the *p*-type region has a high concentration of holes, electrons diffuse from the *n*-type side to the *p*-type side. Similarly, holes diffuse from the *p*-type side to the *n*-type side. In a *p*-*n* junction, when the electrons and holes diffuse to the other side of the junction, they leave behind exposed charges on dopant atom sites, which are fixed in the crystal lattice and are unable to move. On the *n*-type side, positive ions are exposed, and on the *p*-type side, negative ions are exposed. An electric field forms between the positive ions in the *n*-type material and negative ions in the *p*-type material. This region is called the "depletion region" since the electric field quickly sweeps free carriers out, hence the region is depleted of free carriers. A "built in" potential V_{bi} due to electrical field of depletion region is formed at the junction, which is a difference between the electric potential at the edges of the depletion layer.. The electric file at depletion region creates a energy barrier that prevents electrons from diffusing into

p-type side, and similarly, prevents holes from diffusing into n-type side. Most of electrons in the n-type region are unable to move into the p-type side because they can not have enough energy to overcome the energy barrier at the p-n junction. On the other hand, any electron from the p-type region as minority carriers can move into the n-type region, because there is no any barrier to stop it. Because they are minority carriers, the concentration of these electrons is very small, however, it is sufficient to produce transitions of electrons from the p-type to the n-type side that exactly compensate for the diffusion current in the opposite direction. In an equilibrium condition, diffusion current is equal to drift current, and the electron current through the junction is zero[20].

2.1.2 Photovoltaic Effect

Figure 4 illustrates the basic operation of a solar cell. The generation of current in a solar cell involves two key processes. The first process is the absorption of incident photons to create electron-hole pairs. When the incident photon has an energy greater than the bandgap of the semiconductor, the solar cell generates electron-hole pairs, i.e., excess charge carriers. Most holes generated in the n-region, as well as electrons generated in the p-region, far from the junction are minority carriers and recombine with the majority carriers before they can diffuse to the junction. If the carrier recombines, then the light-generated electron-hole pair is lost and no current or power can be generated. Therefore, the lifetime of these carriers has to be sufficient to enable these carriers to reach and traverse the field region of the collecting diode. Only minority carriers generated within a diffusion length of each side of the junction can diffuse to the edge of the depletion region and are immediately accelerated by the electric field to the opposite side of the junction, which produces photocurrents. For example, only those

electrons generated in the p-region which have not recombined before can reach the n-region. These electrons need to be generated at a distance not farther than a diffusion length from the n-region. Similarly, only those holes generated a distance within diffusion length from the n-region can diffuse and reach the p-region. When the light-generated minority carrier reaches the *p*-*n* junction, it is swept across the junction by the electric field at the junction, where it is now a majority carrier. Moreover, since the electric field in the space charge region is high, all the electrons and holes generated in the space charge region are accelerated toward the opposite directions, contributing to the photocurrent. Photocurrents come from electron-hole pairs generated in the depletion region and within a diffusion length of their respective n-type or p-type partners. When the minority charge carriers have traversed the electric field region, they become the majority carriers. When the emitter and base of the solar cell are connected together, i.e., the solar cell is short-circuited, the light-generated carriers flow through the external circuit.

The collection of light-generated carriers does not by itself give rise to power generation. A voltage must be generated as well as a current for power generation. The collection of light-generated carriers by the *p*-*n* junction causes a movement of electrons from p-type side to the *n*-type side and holes from n-type side to the *p*-type side of the junction. Under short circuit conditions, there is no build up of charge, therefore the photogenerated carriers exit the device as light-generated current and voltage is zero.

However, when the photogenerated carriers are prevented from leaving the solar cell, then the collection of photogenerated carriers causes an increase in the number of electrons on the *n*-type side of the *p*-*n* junction and, a similar increase in the number of

holes in the *p*-type side. This separation of charge creates an electric field at the junction which is in opposition to that already existing at the junction, thereby reducing the net electric field. Since the electric field represents a barrier to the flow of the forward bias diffusion current, the reduction of the electric field increases the diffusion current. A new equilibrium is reached in which a voltage exists across the *p*-*n* junction. The current from the solar cell is the difference between I_L and the forward bias current. Under open circuit conditions, the forward bias of the junction increases to a point where the photogenerated current is exactly balanced by the forward bias diffusion current, and the net current is zero. The voltage required to cause these two currents to balance is called the "open-circuit voltage"[21].

2.1.3 Operation of Thin Film Solar Cells

For thin film solar cells, due to the close proximity to the surface with its high surface recombination, electron-hole pairs recombine rapidly near the surface, resulting in low quantum efficiencies. Since electron-hole pairs should not be generated in this layer, it must have a large energy gap. It is called a window layer, through which photons pass unimpeded, but which protects electrons and holes from recombining at the front contact. The interface between the window layer and the absorber should have a low density of interface states in order to prevent recombination at the interface and enhance photocurrent.

A disadvantage of many materials with direct transitions and favorable energy gaps, is that they can’t be doped equally well n-type and p-type. Thus, the structure required for solar cells demands heterojunctions. Generally, cadmium sulfide (CdS) has a wide bandgap (2.41 eV), and function as window layer and protects electrons and holes from

recombining at the front surface. CdS can be natively *n*-doped and the interface between the CdS window layer and the absorber has a low density of interface states. The heterojunction solar cells with window layer and absorber include n-type CdS/p-type CdTe, n-type CdS/p-type CIGS, and n-type CdS/p-type CZTS.

It is interesting to note that amorphous silicon is the class of thin-film materials. Amorphous silicon is silicon without a crystalline structure. Because of the lack of long-range order, the momentum of electrons in bound states and unbound states is largely undetermined. As a result, no phonons are required for transitions between these states in order to satisfy the conservation of momentum. The transitions are direct and have large absorption coefficients. However, the lack of order has the disadvantage that the states for electrons and holes are not confined to bands, the states fill the entire forbidden zone. The inclusion of about 10% hydrogen serves to saturate many of the dangling bonds of the silicon atoms in the amorphous structure. The density of states in the forbidden zone is drastically reduced, and the material can now be doped. However, the saturation of dangling bonds with hydrogen is not stable. During illumination, the bonds are broken by the capture of holes. This property, (Staebler-Wronski effect) leads to a continuous decrease in the efficiency of solar cells made of a-Si:H[22].

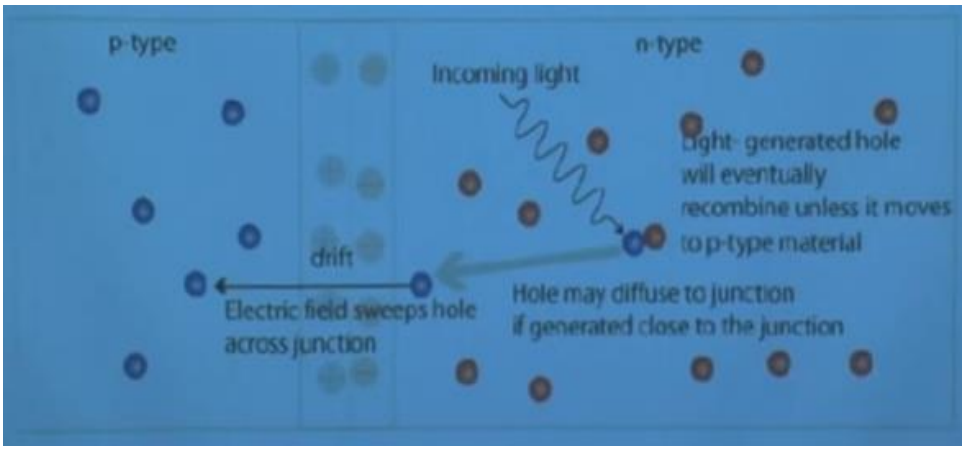


Figure 4, Basic operation of a solar cell.

2.1.4 Absorption of Materials

For solar cells, the generation of electrons and holes by the absorption of photons is the most important process. The absorption determines the thickness of the absorber required to absorb all the radiation falling on it when the photon energy is greater than the bandgap. Absorber thickness is very important because it impacts efficiency and material and time of deposition costs. Because of these two facts, highly absorbing, robust, and inexpensive absorbers give the best optimization and highly attractive for reduce manufacturing costs.

The probability for the absorption of a photon of energy is defined by the absorption coefficient α, which depends on the material properties and also on the wavelength of light. Semiconductor materials have a sharp edge in their absorption coefficient, since light which has energy below the band gap does not have sufficient energy to excite an electron into the conduction band from the valence band. Consequently this light is not absorbed. The absorption coefficient for several semiconductor materials is shown figure 5.

The most widely used absorber material, silicon has a poor absorber because it is an indirect bandgap semiconductor, and the transition for electrons from the valence band to

the conduction band minima requires a momentum exchange at the time of absorption and this reduces the probability for absorption. For crystalline silicon absorbers, the indirect bandgap gives a range of values for $\alpha(\lambda)$ from $1*10^2$ cm^{-1} at 953nm to $1*10^4$ cm^{-1} at 2.5eV and 496nm[20], so the challenge is to achieve effective absorption at the near infrared part of the solar spectrum. The consequence for an effective absorption of light in silicon is that the thickness would be 200μm, which is the typical thickness of crystalline silicon solar cell. This will apply a great challenge to achieve silicon of high purity at great thickness of 200μm for silicon solar cell technologies.

Contrasting with indirect bandgap semiconductors, direct bandgap semiconductors rapidly rise absorption coefficient to exceeding $1*10^4$ cm^{-1} above the bandgap energy and can increase to exceeding $1*10^5$ cm^{-1} for higher photon energy. This direct bangap structure is typical for most of the II-VI and III-V classes of direct bandgap semiconductor materials, for the chalcogenides such as copper indium diselenide and earth-abound CZTSSe, and for the perovskite materials. The direct bandgap materials have very strong light absorption and a thickness of only 1–2 micrometers is enough to absorb 90% of the available solar spectrum for photon energy greater than the bandgap. Therefore, the diffusion length of minority carriers can be reduced. A higher impurity concentration and the present of grain boundaries can be tolerated. Therefore, these materials can be formed on thin-film with about 6 micrometer thickness. All these advantages hold the promise of significant cost reductions for the production of solar cells.

The absorption coefficient then has a large value. For the absorption of that part of the solar spectrum which can be absorbed, a thickness of only a few um is sufficient for thin-

film solar cells. For the same number of recombination centers as in a thick silicon cell, a higher impurity concentration and the presence of grain boundaries in the film can be tolerated. Because of the smaller distances to the membranes at the surfaces, the diffusion lengths can also be smaller. This allows the use of materials with lower mobility. All these advantages hold the promise of significant cost reductions for the production of solar cells.

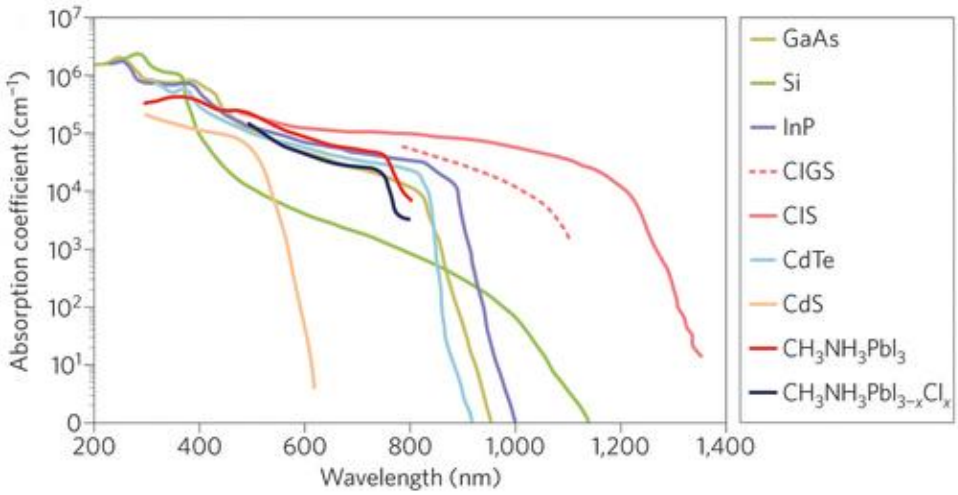


Figure 5, The absorption coefficients of several semiconductor materials.

2.1.5 Quantum Efficiency

Quantum efficiency (QE) is the ratio of the number of carriers collected by the solar cell to the number of photons of a given energy incident on the solar cell. QE can be expressed in the following:

$$\eta = \frac{I_{ph}}{q\emptyset} = \frac{I_{ph}}{q}\left(\frac{h\nu}{P_{opt}}\right) \qquad (1)$$

Where I_{ph} is the photocurrent, φ is the photon flux(=P_{opt}/hν), and P_{opt} the optical power.

When all photons of a certain wavelength are absorbed and the resulting minority carriers are collected, then the quantum efficiency at that particular wavelength is unity.

The quantum efficiency for photons with energy below the band gap is zero. The quantum efficiency for most solar cells is reduced due to recombination, incomplete absorption and reflection.

Quantum efficiency includes external and internal quantum efficiency. The external quantum efficiency of a solar cell includes the effect of optical losses such as transmission and reflection. However, it is interesting to look at the quantum efficiency of the light left after the reflected and transmitted light has been lost. Internal quantum efficiency refers to the efficiency with which photons that are not reflected or transmitted out of the cell (ignore reflection and transmission) can generate collectable carriers. By measuring the reflection and transmission of a device, the external quantum efficiency curve can be corrected to obtain the internal quantum efficiency curve.

The quantum efficiency in the depletion region is approximately unity because the electron-hole pairs are quickly swept apart by the electric field and are collected. Away from the junction, the quantum efficiency drops. When the carrier is generated more than a diffusion length away from the junction, then the quantum efficiency is quite low. When the carrier is generated closer to a region such as a surface, high surface recombination will reduce the quantum efficiency. Therefore, making photocarrier generation in the depletion region, increasing large diffusion length, conducting surface passivation and reducing light absorption at front surface will enhance quantum efficiency and hence the light-generated current.

2.2 Solar Cell Parameters

Typical current–voltage (J–V) curves of a solar cell in the dark and under illumination are shown in figure 6[21]. Power is generated when the cell operates in the fourth quadrant

of the graph where voltage is positive and current is negative. The solar cell operates in the fourth quadrant. Under illumination, the dark curve will be shifted by the photogenerated current density (J_L). The IV curve of a solar cell is the superposition of the IV curve of the solar cell diode in the dark with the light-generated current. The light has the effect of shifting the IV curve down into the fourth quadrant where power can be extracted from the diode. Illuminating a cell adds to the normal "dark" currents in the diode.

$$I = I_0 \left[\exp\left(\frac{qV}{nkT}\right) - 1\right] - I_L \qquad (2)$$

where I_0 is the reverse saturation current, n is diode ideality factor and I_L is light generated current.

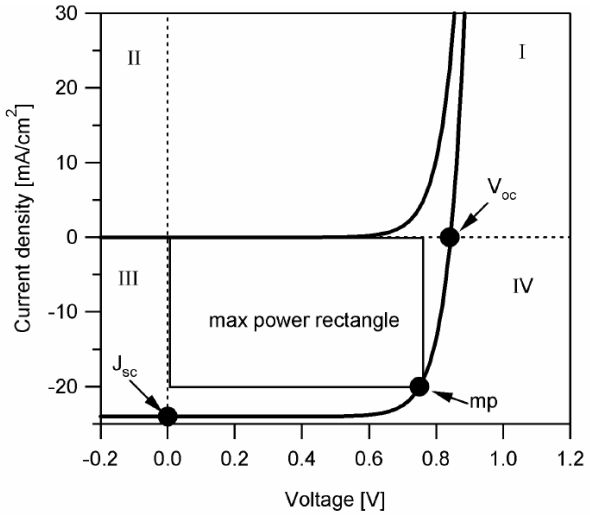


Figure 6, A typical current–voltage characteristic of a solar cell in the dark and under illumination.

Primary parameters that describe the performance of a photovoltaic device are the short-circuit current density(J_{sc}), open-circuit voltage (V_{oc}), fill–factor (FF) and

conversion efficiency.

The short circuit current J_{sc} is the current density that flows through the junction under illumination at zero applied bias. In the ideal case, J_{sc} equals the photogenerated current density (J_L). Therefore, the short-circuit current is the largest current which may be drawn from the solar cell. The short-circuit current mainly depends on quantum efficiency and spectrum of the incident light (the number of photons).

The open-circuit voltage V_{OC} is the maximum voltage available from a solar cell when the current through the junction is zero, and can be expressed as

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{I_L}{I_0} + 1\right) \qquad (3)$$

The above equation shows that V_{oc} depends on the saturation current of the solar cell and the light-generated current. Because I_l typically has a small variation and the reverse saturation current may vary by orders of magnitude, the reverse saturation current plays in a key role in V_{oc}. The saturation current, I_0 depends on recombination and energy band in the solar cell. Open-circuit voltage can identify the amount of recombination and junction quality in the device.

The short-circuit current and the open-circuit voltage are the maximum current and voltage respectively from a solar cell. However, at both of these operating points, the power from the solar cell is zero. The point on the J–V curve that yields the maximum power is referred to as the maximum power point; the corresponding current density and voltage are maximum current J_{mp} and maximum voltage V_{mp}. The fill factor is a parameter which determines the maximum power from a solar cell. The FF is defined as

the ratio of the maximum power from the solar cell to the product of V_{oc} and I_{sc}. The FF is a measure of the squareness of the J–V curve and is also the area of the largest rectangle which will fit in the IV curve. The FF is given by

$$FF = \frac{V_{mp} I_{mp}}{V_{oc} J_{sc}} \qquad (4)$$

The efficiency is the most commonly used parameter to compare the performance of a solar cell. The efficiency of a solar cell is defined as the ratio of the maximum output power P_{max} to the input power (incident power) $P_{incident}$, and can be expressed as

$$\eta = \frac{V_{oc} I_{sc} FF}{P_{in}} \qquad (5)$$

The efficiency depends on the spectrum and intensity of the incident sunlight and the temperature of the solar cell. Therefore, conditions under measurement of efficiency need to be carefully controlled. Terrestrial solar cells are measured under AM1.5 conditions and at a temperature of 25°C. For space applications, solar cells are measured under AM0 conditions.

2.2.1 Efficiency as a function of their energy gap

The short-circuit current of a solar cell depends on the absorbed photon current. It is a maximum for a semiconductor with an energy bandgap of zero and decreases with increasing energy gap. However, the open-circuit voltage V_{oc} is zero when energy bangap becomes zero and increases with increasing energy gap. Therefore, the efficiency is therefore zero while energy bandgap becomes zero and infinite. The efficiency as a function of the energy gap is calculated when only radiative recombination is considered.

Figure 7 shows the conversion efficiency of a solar cell as a function of bandgap. The figure 7 demonstrates that optimal conversion efficiency for a single junction solar cell has a bangap of 1.1eV-1.5eV, and maximum conversion efficiency occurs in the bandgap of approximately 1.5eV. The silicon, GaAs, CdTe are in the range of 1.1eV-1.5eV. In addition, GIS and CZTS have been tuned their bandgaps to 1.5eV by adjusting concentration of the Ga or other element. Therefore, to achieve maximum conversion efficiency for a single junction solar cell, the bandgap of materials has an energy bandgap of approximately 1.5eV.

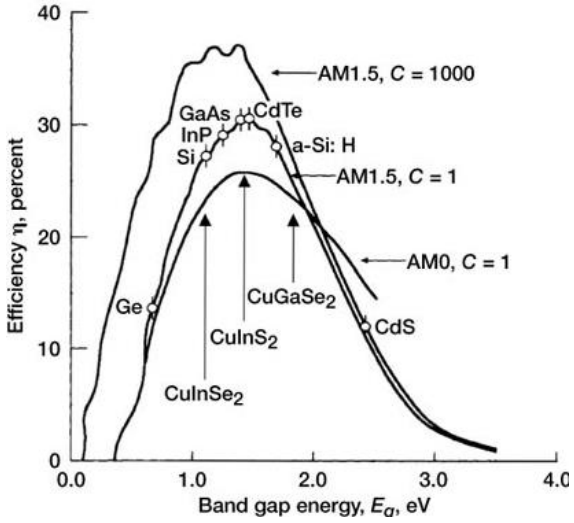


Figure 7, Power conversion efficiency of a solar cell as a function of bandgap.

2.3 Non-ideal Effect and Double Diode Model

A real solar cell has a parasitic series (R_s) and shunt resistance (R_{sh}). There are several physical mechanisms responsible for these resistances. Series resistance, R_s, is composed of the bulk resistance of the semiconductor materials and that of the front and back contacts. Shunt resistance, R_{sh}, is caused by leakage across the p–n junction and around

the edge of the cell. An ideal cell will have high shunt resistance ($R_{sh} = \infty$) and low series resistance ($R_s = 0$). Modest R_s affects mostly the far–forward voltage region above V_{mp} but the open–circuit voltage is not affected by R_s, because no current flows at V_{oc}. The influence of R_{sh} is visible in the low voltage range (near zero voltage). Both, R_s and R_{sh} can reduce the FF by a predictable amount. High values of R_s and low values of R_{sh} can also reduce J_{sc} and V_{oc} respectively. The effects of R_s and R_{sh} on the J–V characteristics are illustrated graphically in figure 8[21].

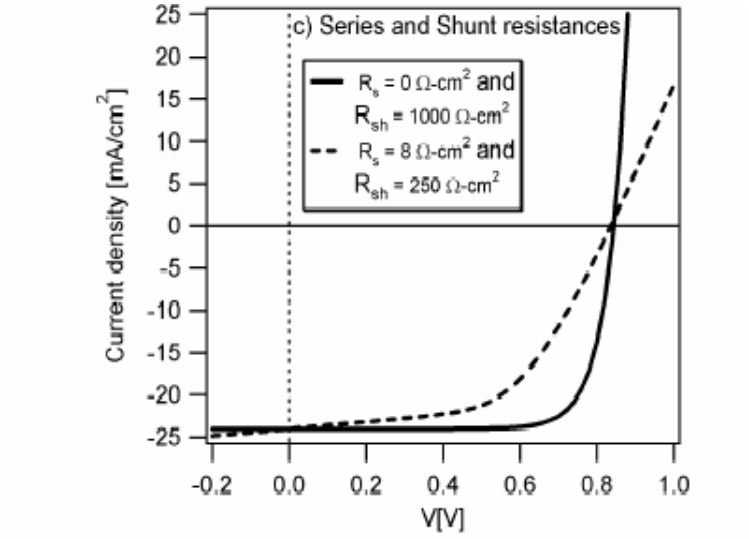


Figure 8, Effect of series and shunt resistances on the J–V curves

Many of the parameters that describe a solar cell are extracted from the current-voltage curves. Non–idealities such as light-to-dark crossover and the current limiting behavior in the far-forward bias are examined in the first quadrant. The shunt resistance R_{sh} is obtained from the plot of the derivative dJ/dV vs. the applied voltage V. Near J_{sc} and in the reverse bias, the dJ/dV plot will be constant and its value equal to the shunt conductance G. The series resistance R_s is determined from the plot of dV/dJ above the V_{oc} region. Diode ideality factor may be calculated from the slope, nkT/q. Depending on

the dominant current transport mechanism the diode quality factor for a well behaved curve, is expected to be in the range between 1 and 2. A diode ideality factor of one is the ideal case, diode ideality factor of two occurs when bulk recombination is the dominant current transport mechanism, and diode ideality factor more than 2 indicates tunneling or interfacing recombination is the dominant current transport mechanism.

Equivalent circuit

Non-ideal effect of a real solar cell can be modeled as a double diode model. Figure 9 shows the double diode model. In this model, the solar cell is modeled as a current source connected in parallel with a rectifying diode (band-band recombination). The current source is also shunted by another diode that models the space charge recombination current due to impurity, and a shunt leakage resistor to account for the partial short circuit current path due to the semiconductor impurities and non-idealities. In addition, the solar cell metal contacts and the semiconductor material bulk resistance are represented by a resistor connected in series with the cell[23].

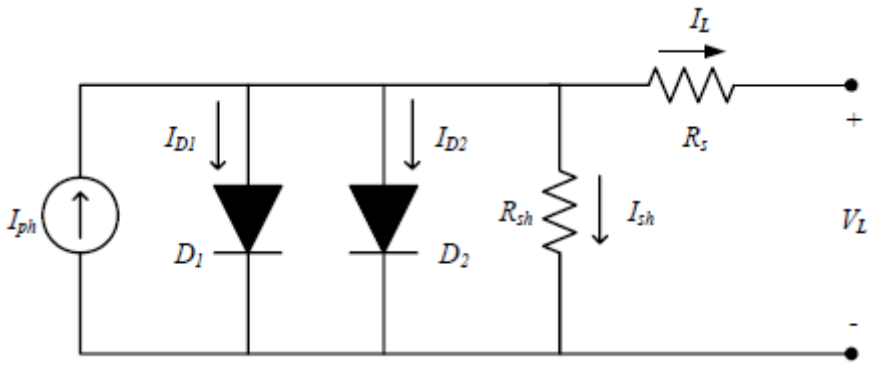


Figure 9, Equivalent circuit of a double diode model

In this double-diode model, the cell terminal current is calculated as follows: $I_L = I_{ph} - I_{D1} - I_{D2} - I_{sh}$

Where I_L is the terminal current, I_{ph} is the cell-generated photocurrent, D_1 and D_2 are the first and second diode currents, I_{sh} is the shunt resistor current. The terminal current of I_L can be expressed by following equation[23] where two diode currents are expressed by Shockley equations.

$$I_L = \begin{Bmatrix} I_{ph} - I_{SD1}\left[\exp\left(\frac{q(V_L + I_L R_s)}{n_1 kT}\right) - 1\right] \\ -I_{SD2}\left[\exp\left(\frac{q(V_L + I_L R_s)}{n_2 kT}\right) - 1\right] \\ -\left[\frac{(V_L + I_L R_s)}{R_{sh}}\right] \end{Bmatrix} \quad (6)$$

Where R_s and R_{sh} are the series and shunt resistances respectively; I_{SD1} and I_{SD2} are the diffusion and saturation currents respectively; V_L is the terminal voltage; n_1 and n_2 are the diffusion and recombination diode ideality factors; k is Boltzmann's constant; q is the electronic charge and T is the cell absolute temperature in Kelvin.

2.4 Semiconductor-Metal Contact

The metal is characterized by the chemical potential of its electrons, and the absolute value of the chemical potential is known as the work function of the metal. In general, metal-to-semiconductor contacts can behave either as a rectifying or as an ohmic contact depending on the characteristics of the interface. Metals with a small work function, therefore, are favorable for the exchange of electrons and make good, so called ohmic, contacts to n-type semiconductors. For a p-type semiconductor with work function ϕ_s and a metal with work function ϕ_m, an ohmic metal/semiconductor contact is formed when

the work function of metal is larger than the work function of p-type semiconductor($\Phi_m > \Phi_s$).This situation produces a dipole-oriented negative in the metal and positive in the semiconductor, and thereby hole accumulation (majority carrier concentration above that dictated by doping) in the semiconductor, and therefore no electrostatic barrier to hole transport into the contact. And also, electrons see a potential barrier from the Fermi energy of the metal to the conduction band of the semiconductor, equal to the difference between the work function of the metal and the electron affinity of the semiconductor. This large-workfunction case produces an ohmic contact for holes in p-type material. There would be a barrier for electrons.

A rectifying contact is formed when the work function of metal is less than the work function of p-type semiconductor ($\Phi_m < \Phi_s$).This means holes would have to be depleted (majority carrier concentration below that dictated by doping) in the p-type semiconductor, an electrostatic barrier to holes would develop in the semiconductor, and we would have actually succeeded in making a rectifying Schottky barrier diode to the p-type material[20].

Both ohmic and Schottky metal/p-semiconductor interfaces are shown in figure 10. At the Schottky-contact interface, holes see a barrier ϕ_b as they travel from the semiconductor towards the metal, but such a barrier is absent in the case of ohmic contact interface.

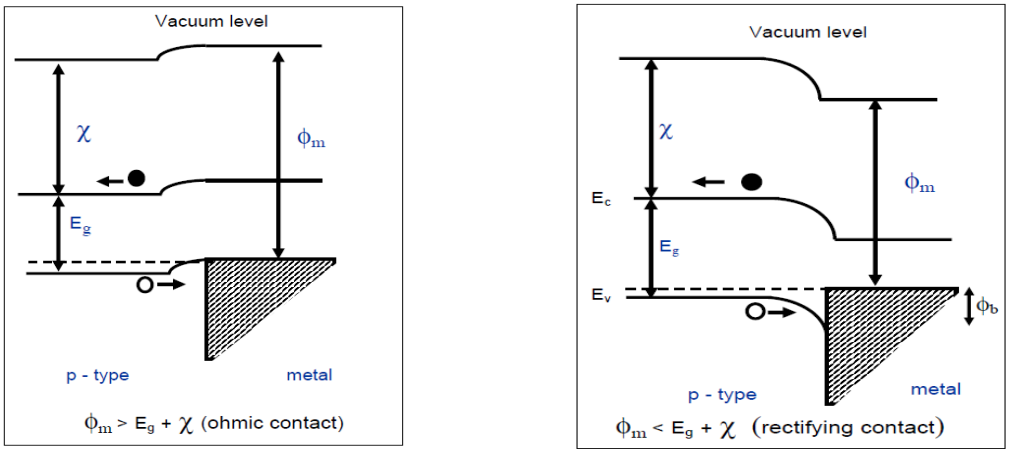


Figure 10, Ohmic and Schottky metal/p-semiconductor interfaces.

Schottky contact is formed at the junction, and the contact barrier height, ϕ_b , for holes at the interface in the absence of interface states, is given by the difference between the valence band edge and the Fermi energy in the metal.

$$\Phi_b < \frac{E_g}{q} + (\chi - \Phi_m) \qquad (7)$$

Though in practice thermal effects make 0.3 eV or less sufficient, the barrier heights at 0.3eV or a zero or negative value would be preferred for making ohmic contact.

For contacts on covalent semiconductors, the band bending in the semiconductor is found to depend less strongly on the work function of the metal than would be expected from the difference in the work functions. This is probably due to the presence of surface states on the semiconductor surface, which are charged due to the contact with the metal. Together with the surface charge on the metal, the surface charge on the semiconductor forms a charge double layer, over which a potential step occurs which depends on the dipole moment of this layer. The potential difference between in the interior of the semiconductor and the interior of the metal is still given by the difference in the work

functions, but it is now divided between the band bending of the space charge layer and the usually unknown, potential difference across the dipole layer.

In additional cases, there is a way a low-work function metal can give ohmic behavior for p-type material. When the semiconductor is very highly doped, at least in the vicinity of the contact, a majority carrier depletion layer caused by an inappropriate work function of a metal is only very thin. It can in fact, for suitably high doping levels, be so thin that the majority charge carriers can tunnel through this potential barrier between the semiconductor and the metal[20].

Chapter 3 Device Design and Experimental Procedures

3.1 Material Property

CdTe photovoltaics have energy return investment exceeding that of traditional fossil fuels, provide the shortest energy payback time among all photovoltaic technologies for terrestrial applications, and has the second largest market share after the conventional crystalline silicon technology. In addition, CdTe photovoltaics have superior tolerance to high energy irradiation and are more suitable for space applications[24]. From basic physic-chemical properties, CdTe is an optimum material for use in thin film solar cells. CdTe has an energy gap of 1.45 eV, well suited to absorb the solar light spectrum. The energy gap is direct, resulting in an absorption coefficient for visible light of $>10^5$ cm^{-1} so that the absorber layer need only be 2μm thick to absorb >90% of light above the band gap. Above 500 ℃, the stoichiometric compound of CdTe is the stable solid phase. In the high temperature phase a slight nonstoichiometry is present in the form of a slight Cd deficiency, leading to a native *p*-doping of films. This property makes it relatively easy to produce CdTe films suited for thin film solar cells. No excessive care has to be taken in preparing CdTe films as long as the substrate temperature is sufficiently high. Due to the strong ionicity of the material, the strong bonding leads to an extremely high chemical and thermal stability, reducing the risk of degradation of performance or any liberation of Cd to a very low level. No degradation intrinsic to the CdTe can be expected.

However, in polycrystalline thin films, doping becomes more difficult because of the enhanced compensation and segregation effects at the grain boundaries. In fact, because of these characteristics of the doping mechanism, the grain boundaries in polycrystalline

CdTe thin films can be made more p-type than the bulk, reducing and the minority carrier recombination at the grain boundaries. Difficulties encountered in doping of CdTe do not affect its PV performance, but they create problems in making a low-resistance ohmic contact to the material.

3.2 Development of Thin-film CdS-CdTe Solar Cells

Thin-film solar cells based on CdTe are the cells with a long tradition. The first thin-film solar cell device was cuprous sulphide/cadmium sulphide heterojunction in 1954 by Reynolds et al[25]. Cuprous sulphide/cadmium sulphide solar cells displayed severe stability problems, and their development was discontinued by the early 1980s. In 1963, the first thin-film cell on CdTe, a p-Cu_2Te/n-CdTe heterojunction, a structure similar to the CdS cells, obtained 6% efficiency reported by Cusano[26]. For 9 years after the work reported by Cusano, there was not much to report about this material. In this interval, n-cadmium sulfide (CdS) was recognized to be most effective heterojunction parter of p-CdTe. In 1972, an efficiency of 6% in CdTe/CdS thin film solar cells reported by Bonnet and Rabenhorst[27]. In 1983, Bulent reported the efficiency of 9.15% in thin film CdS/CdTe heterojunction solar cell formed by electroplated technique[28]. In 1982, Tyan et al in the labs of Kodak reported 10% efficiency in n-CdS/p-CdTe heterojunction solar cells[29]. Furthermore, the cell featured only a very thin CdS-layer was recognized to improve the blue response. In 1992, efficiency in n-CdS/p-CdTe heterojunction solar cells was improved to 14.6% by close-space sublimation in a paper of Chu et al[30]. Britt et al in 1993 reported that a CdS/CdTe solar cell of greater than 1 cm^2 area obtained 15.8% efficiency in an AM1.5[31]. In this paper, CdS films were prepared by chemical bath deposition and p-CdTe films were deposited by close-spaced sublimation[31]. In 2001 and

2004, Wu et al reported a CTO/ZTO/ CdS/CdTe polycrystalline thin-film solar cell with an NREL-confirmed total-area efficiency of 16.5%, which is the highest efficiency ever reported for CdS/CdTe solar cells[32]. In the paper, novel materials CTO film, ZTO buffer Layer were developed to improve performance limited by conventional transparent conductive oxides with an average transmission of only 80%[32]. This is a little over half of the 29% theoretical limit. Currently, CdTe efficiency has been improved to 20.4% by the First Solar[11]. It has been estimated that practical CdTe devices with 25% efficiencies should be feasible in the near future[17]. Thus considerable work will likely be required to optimize the materials as well as the fabrication techniques.

3.3 Technical Issues

Window-absorber type solar cells, including the devices using CdS windolw layer coupled with an absorber layer of CdTe, continue to be the most cost-effective photovoltaic technologies, which are potentially competitive with conventional power sources for terrestrial applications. In the past great effort has been devoted toward reducing the cost and increasing the power conversion efficiency (PCE) of these cells. In the quest for reaching the Schokley-Queiser limit in PCE, a major hindrance in these solar cells has been the loss of photocurrent caused by parasitic light absorption in the planar CdS window layer. Planar CdS is responsible for absorption loss of 22-24%[33] and a photocurrent loss of approximately 7 mA/cm^2 [32-34] [2,17,18].

Several groups have worked on reducing the absorption loss in planar CdS window layer. One approach was to reduce the planar CdS thickness, for example, to 50nm[34,35][17,19]. This method demonstrated favorable spectral response at wavelengths longer than 500nm, but the parasitic absorption loss remained for wavelengths shorter

than 500nm. Furthermore, such planar window layer thinning presents significant challenges of its own. Substrate roughness and pinholes can exacerbate shunting and negatively influence open circuit voltage (V_{oc})[32,36] [2,20]. It necessitates an additional high resistivity buffer layer between the TCO and the CdS window layer. More recent approach is to widen the band gap of the CdS window layer by replacing CdS with the $Cd_{1-x}Zn_xS$ alloy through the high cost MOCVD method [19]. Quantum efficiency spectrum data appears that the gain in transmission over the 300-512 nm range was very modest and the transmission became detrimental in the 500-860nm range. Also, the quality of CdTe film deposited on top of the $Cd_{1-x}Zn_xS$ may be the cause of a relatively low open circuit voltage of 0.67 V-0.71 V.

A stable back-contact that is not significantly rectifying is essential for good performance and long-term stability of n-CdS/p-CdTe solar cells. Due to (5.9eV) sum of electron affinity (4.4eV) and bandgap(1.5eV) of p-CdTe, no metal with work function larger than 5.9eV to form ohmic contact. In practice, often the CdTe surface is chemically etched to create a Te-rich surface, and then Cu is incorporated as a key element to locally increase the effective doping level on the surface. However, Cu is known to be a fast diffuser in p-CdTe. The diffusion of Cu could be beneficial for the solar cell since it can dope CdTe p^+ giving a momentary increase in the efficiency but, in any case, at long run the efficiency decreases since Cu can diffuse along the CdTe grain boundary. In addition, due to polycrystalline CdS with pinholes and high defects, planar CdS can accelerate cell degradation because Cu diffuses from CdTe into planar CdS and further into SnO_2 through pinholes and defects of the planar CdS, forming deep penetration and introducing microshunts[37]. As a result, main junction and back ohmic contact behavior are

aggravated[37].

3.4 Device Design

we present an approach for overcoming these challenges through a stack nanowire solar cell structure with diffused p-n junction. The stack nanowire solar cell configuration is an array of CdS nanowires embedded in a transparent anodized aluminum oxide (AAO) matrix which replaces planar CdS as a nanowire window layer for tailoring optical properties, a CdTe absorber layer grown on the top of them; this nanowire CdS-CdTe device structure is illustrated in Figure. 11B, which is different with CdS nanopillar structure [38]. Carrier generation and transport of the stack nanowire and the conventional planar CdS-CdTe solar cells are shown in Figure 11C and 11D. The fine features of the CdS nanowires confined by nanopores in AAO matrix favorably increase the optical energy band gap and extend transmittance edge of CdS[39-41]. The length of CdS nanowires is 100 nm, which is significantly smaller than the wavelength of the incident. Hence, scattering induced absorption, as seen in long-length silicon nanostructures[15, 16] , is not a major factor here.

Under such circumstances, a part of incident light across the entire spectrum range can directly transmit through absorption-negligible AAO matrix (Figure 11C), and the other part of incident light transmitted through CdS nanowires (Figure 11C) can be enhanced due to their larger effective energy band gap[39-41]. Hence, much broader and stronger spectral range of incident light reaches the CdTe absorber layer where photons are absorbed and converted to carriers. Such configuration significantly suppresses parasitic absorption loss in the window layer, and extends the optical generation of carriers into the broad solar spectrum, resulting in enhanced light absorption and carrier generation and

collection. Further, this structure is particularly advantageous because junction interface area between the CdS nanowires and the polycrystalline CdTe is reduced (Fig. 1e) due to the CdS nanowires touching the CdTe at only a fraction of the planar interfacial area (Fig. 1e). Reduced interface area leads to reduced interface recombination and decreased effective reverse saturation current, which would, in turn, lead to a substantial increase in the V_{oc} of the solar cell. In addition, due to low defect density and the robustness of the CdS nanowires, the stack nanowire CdS-CdTe solar cells can prevent deep diffusion of Cu ion at back contact into the window layer. As a result, aging and reliability are strongly improved.

3.5 Experimental Procedures

To realize the above advantages offered by nanowire window layer solar cells, there is need for a relatively inexpensive process to economically fabricate large periodic arrays of semiconductor nanowires. To this purpose, we developed a lost-cost, template-assisted and metal catalysts-free electro-deposition process, to simply and efficiently grow 100 nm-CdS nanowires on transparent substrates. The key points are that due to fine geometric confinement of the AAO membrane, the CdS nanowires maintain their nanostructure characteristics during the various subsequent high temperature processes.

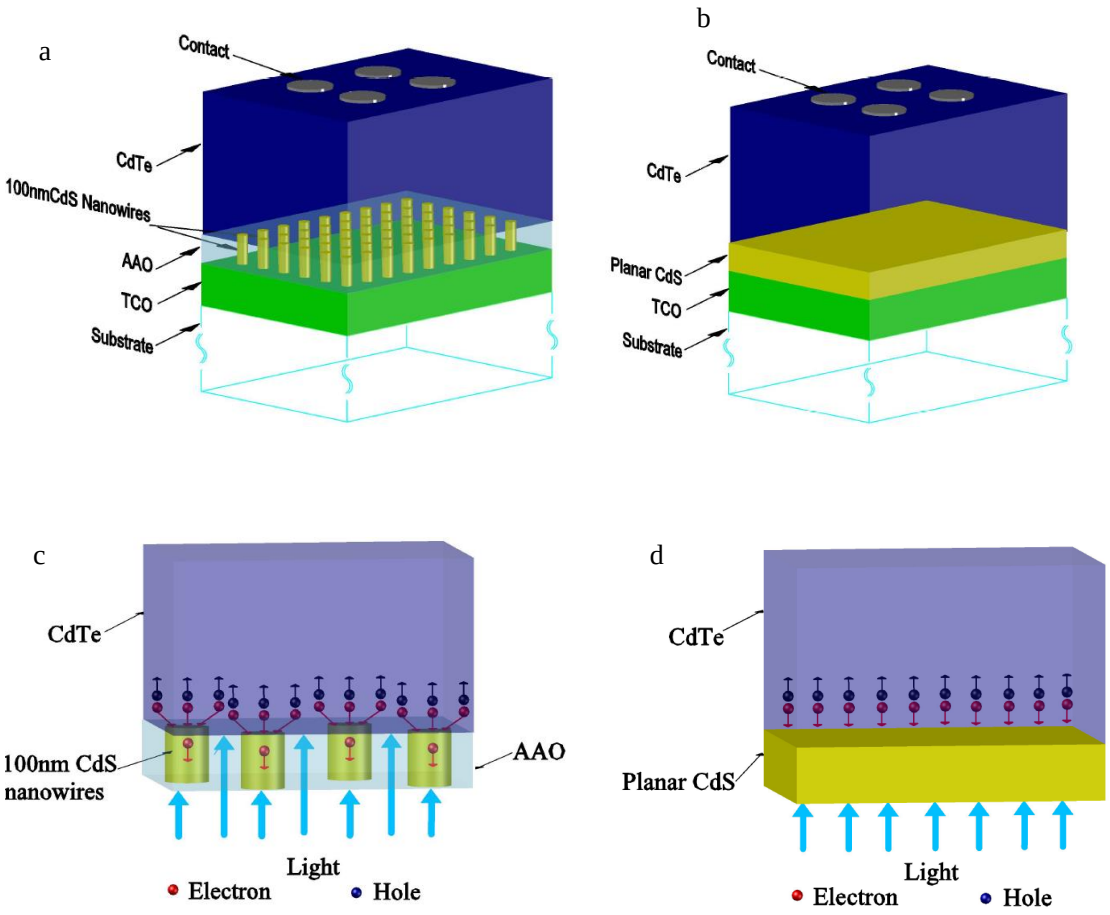


Figure 11, (a), Schematic structure of a planar CdS/CdTe solar cell. (b), Schematic structure of a vertical stack nanowire CdS/CdTe solar cell, where light blue color represents absorption- negligible AAO. (c), Electron and hole transport through reduced junction interface area in the nanowire CdS/CdTe solar cell. (d), for comparison, electron and hole transport through junction interface in a conventional planar CdS/CdTe solar cell.

3.5.1 AAO Membrane Fabrication

Commercially available ITO/ soda-lime glass substrates with sheet resistance of 23-28 Ω/square were cut into 1 inch by 1 inch pieces and cleaned in acetone, methanol, de-ionized water and dried in nitrogen flow. A 100 nm thick tin oxide (intrinsic SnO_2) layer and a 5 nm thick titanium layer were deposited on ITO by direct sputtering. The thickness of Ti layer has been optimized for standard membrane fabrication. When the Ti thickness less than 4nm, due to surface roughness of sputtered Ti layer, samples could crack at electrolyte–air interface during anodization. While the Ti thickness is more than 5.5nm,

anodization process may be extended to several hours, leading to incomplete anodization process.

Next, a 100nm thick aluminum (Al) layer is deposited on the top of Ti layer by electron beam evaporation. Anodized aluminum oxide (AAO) membrane is formed by the following steps. The Al film is anodized in a 0.3 M oxalic acid solution under a 50 V bias until Al is completely anodized where the electrolyte is maintain at a constant approximately 5 °C. Insertion of Ti is thought to improve adhesion and passivation, however, it will result in barrier layer. The formation of the barrier layer prevents growth of the nanowires. Only those nanopores of AAO membrane without the barrier layer can be fully filled with the nanowires. Therefore, introduction of a series of barrier layer removing processes is crucial to uniform nanowire growth. Firstly, the as-anodized samples are etched in 5% phosphoric acid (H_3PO_4) for 40minutes to partially remove the barrier layer. Reactive ion etch (RIE) is an important process to completely remove the barrier layer. The RIE process is set as an anisotropic etching with 90W of RF and 250W of ICP power, which etching rate of vertical dimension is faster than that of horizontal dimension. Then, the samples are etched in 5% phosphoric acid solution for 5minutes to dissolve removed barrier layer particles. Figure12 a and b show schematics of Al layer on ITO and formed AAO membrane. Figure 12c shows transmittance spectra of the as-anodized, H_3PO_4-etched, and RIE-etched AAO membrane for comparison.

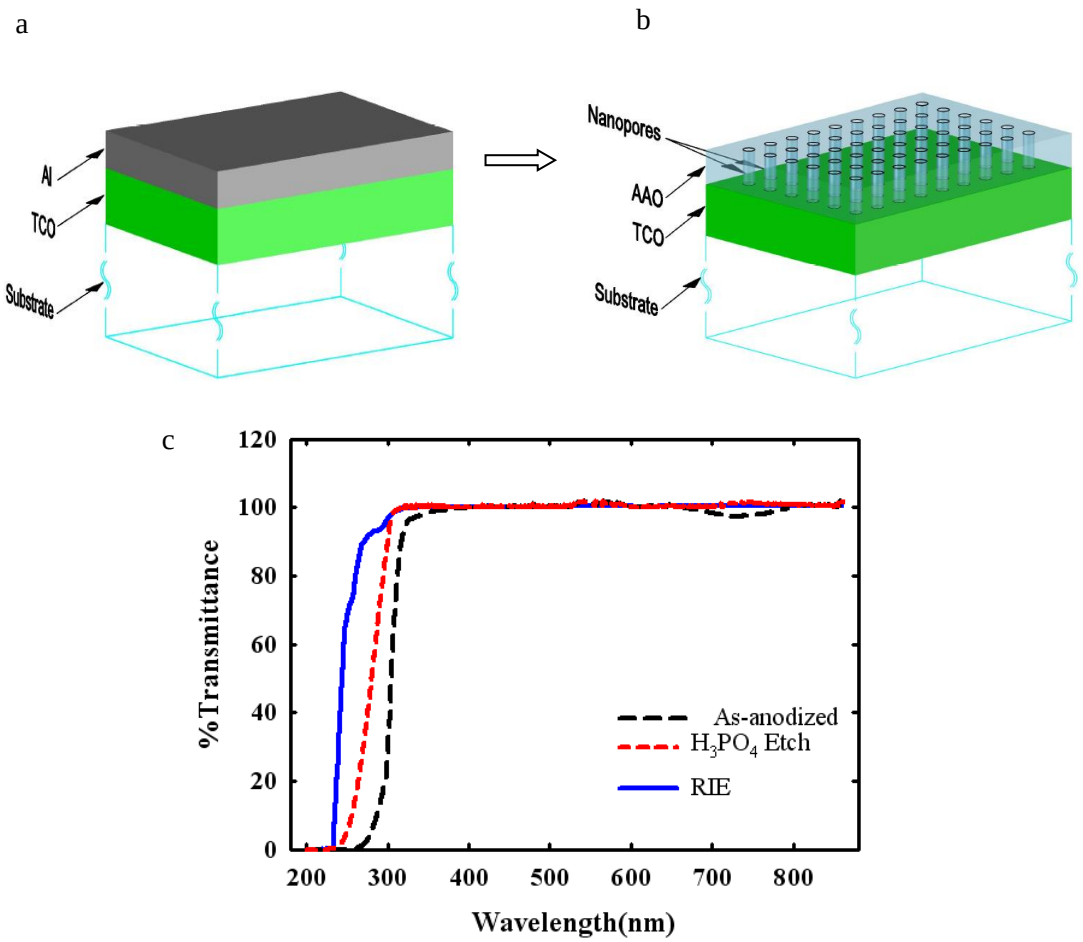


Figure 12, Schematics a) of Al layer on ITO and b) formed AAO membrane, and c) comparison of transmittances between as-anoidzed, H_3PO_4-etched and RIE-etched AAO membrane.

As shown in Figure 12c, the as-anoidzed AAO membrane exhibits approximately similar transmittance behavior with the H_3PO_4-etched and RIE-etched AAO membrane in the range of 343-860nm. However, existence of the barrier layer reduces transparence and causes that the transmittance of the as-anoidzed AAO membrane reduces from 0.98 at 343nm to 0.28 at 300nm. The barrier layer removing processes enhance transparence. H_3PO_4 etching widens pore dimension of nanopores and partially removes the barrier layer, hence the transmittance of the AAO membrane is enhanced, and corresponding transmittance is 0.98 at 306nm and 0.28 at 270nm. The transparence of the AAO

membrane is further improved by the RIE etching process, which demonstrates that the barrier layer has been totally removed through fully filled CdS nanowires. The resulted AAO membrane reveals completely negligible absorption and approximate 100% transparence across the studied wavelengths longer than 295 nm and the transmittance only reduced to 90% at 271nm. Negligible absorption property indicates that AAO membrane is ideal to support nanowire growth without introduction of another light absorption loss. Therefore, the AAO membrane provides an approach to grow nanostructures for solar cell applications.

3.5.2 CdS Nanowire Growth and Scanning Electron Microscope Characterization of CdS nanowires

Figure 13 shows schematics illustration of CdS nanowires embedded into nanopores of AAO membrane. The CdS naowires on transparent substrates are fabricated using electrodeposition. Electrolyte for the CdS nanowires deposition is a mixture of 0.5g cadmium chloride ($CdCl_2$) and 0.5g elemental sulfur in 50mL dimethyl-sulfoxide (DMSO) solution. The CdS nanowires are deposited under a high dc current density of 7mA/cm^2 and at a high deposition temperature of 160°C to form nanowires. Following high temperature and high dc current growth, the CdS nanowires are soaked in a 75%-saturated $CdCl_2$ for 15 minutes, and are annealed at 400℃ for 30 minutes with 100-sccm Argon purge.

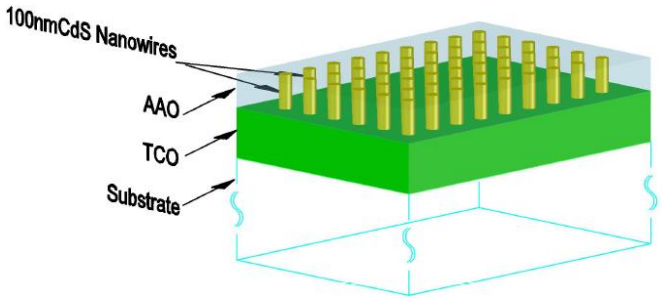


Figure 13, Schematics illustration of CdS nanowires embedded into nanopores of AAO membrane.

Material characterization of the CdS nanowires was conducted with a scanning electron microscope (Hitachi S-900 field emission SEM). Figure 14a and b show the top views of scanning electron microscopy (SEM) images of the nanoporous AAO membrane and the free-standing CdS nanowires, respectively, and figure 14c shows the cross-sectional view of CdS nanowires embedded in the AAO matrix. From figure 14c, nanopores are completely filled with CdS nanowires, which are highly ordered, vertically aligned and dense. Length, diameter and the average distance between the centers of neighboring nanowires were estimated at approximately 100 nm, 60 nm and 106 nm respectively. The porosity of the AAO membrane and the area density of CdS nanowires were calculated to be 32% and 1.14×10^{10} nanowires/cm^2 respectively. Such well-aligned nanowire arrays produced from the quasi-periodic arrangement of transparent AAO membranes are advantageous because they exhibit lower optical reflection than the arrays of random arrangements [42-44]. It should be noted that different forms-fully embedded and free standing nanowires can be readily grown, and various nanowire parameters including length, diameter and pitch could be varied controllably (see Experimental section). Furthermore, the AAO membranes and the nanowires can be grown on a large variety of rigid and flexible substrates, indeed all substrates, which allow for the deposition of

aluminum (Al) film and its anodization.

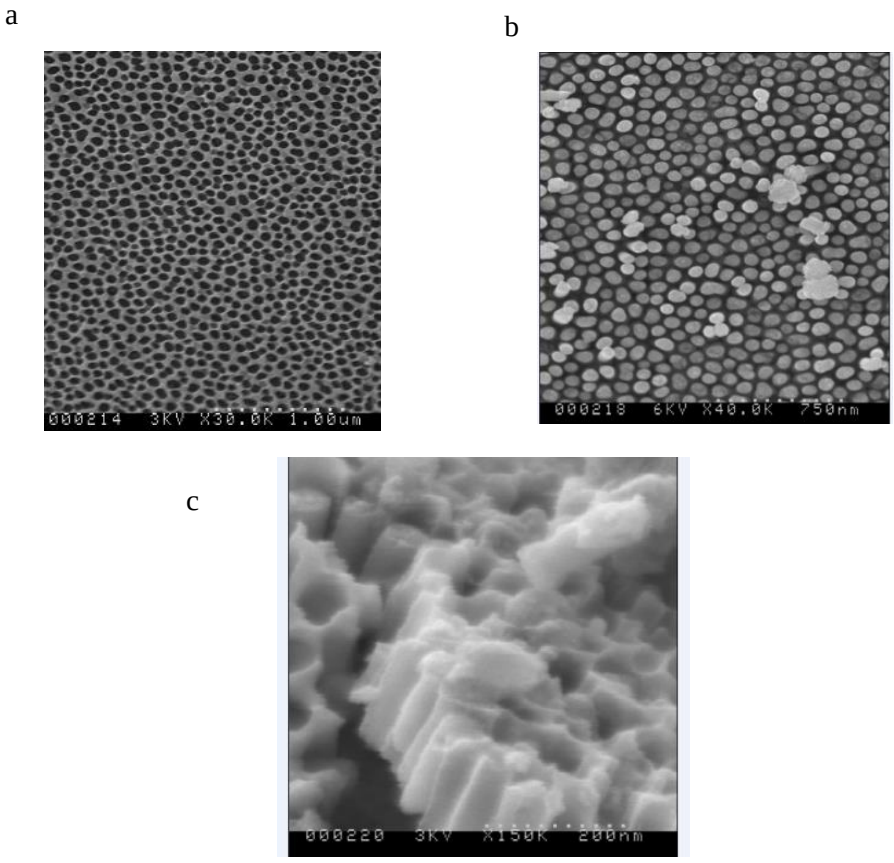


Figure 14, SEM images; (a), top view of a nanoporous membrane of anodized aluminum oxide (AAO); (b), top view of an array of 100 nm long free-standing CdS nanowires; (c), cross-sectional view of a 100 nm long CdS nanowire array embedded in the AAO membrane.

3.5.3 Fabrication of CdTe absorber layer

3.5.3.1 Close-spaced Sublimation

The CdTe is deposited by close-space sublimation (Figure 15) following the steps below. First, the CdTe source plate is made for the depositions. The source plate consisting of a piece molybdenum(Mo) substrate is loaded in the deposition chamber as shown in Figure 15. For source plate fabrication, CdTe is sublimated from a graphite boat packed with a chunk of CdTe powder (99.99% Alfa Aesar). Source plates are fabricated in 15-torr He, with a boat temperature of 600℃, a substrate susceptor temperature of 500℃, 2 mm

spacing, and a deposition time of 30 min. The resultant CdTe films are greater than 100 mm thick and have about 80% coverage of the glass substrate. After each use as a CdTe source, the CdTe source plate is blown with N_2 to remove any loosely adhered oxides or CdTe particles.

3.5.3.2 CdTe Layer by Close-spaced Sublimation and $CdCl_2$ Treament

Next, p-CdTe absorber layer was deposited in a closed-space sublimation system. Source for depositing CdTe was formed by the CSS system using a chunk of CdTe powder (99.99% Alfa Aesar) heated to a boat temperature of 625◦C, while the substrate temperature was set at 525◦C; deposition time was 20minutes. During CdTe deposition, the chamber was pumped down to a background pressure of approximately 0.25 torr; then He with 5% O_2 was introduced at a total pressure of 15 torr. The source and substrate were ramped together to 570◦C, then the source temperature was quickly increased to 630◦C. The source and substrate were maintained at 570 ◦C, and 630◦C for 2.3 minute deposition.

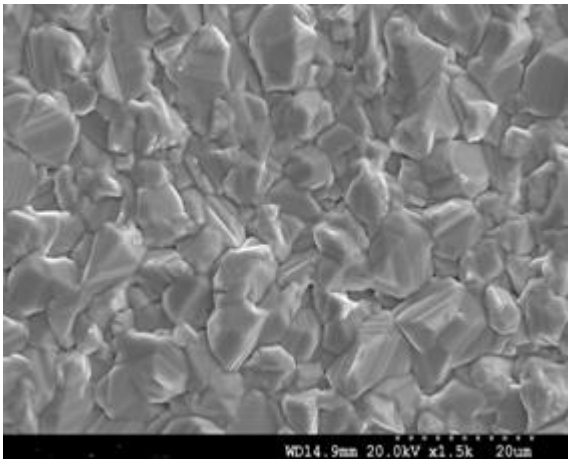
In-situ annealing and post $CdCl_2$ treatments will be important processes to improve the performance of CdTe films. In-situ annealing helps relax the stress and CdTe recrystallization. When the substrate is cooled to 400℃ in chamber of CSS, films are annealed in-situ for 10 minutes. Then, a $CdCl_2$ anneal is performed. The pieces are soaked in a 75%-saturated $CdCl_2$ in methanol solution. The substrates are dipped for 30 min at room tempearture. After that dip, the pieces are then placed on an aluminum plate in a tube furnace that is purged with Argon. The furnace is then set at 400℃ and left on for 30 min with a flow of 100-sccm Argon. After cooling to a maximum of 50℃, the pieces are rinsed in DI water to remove any excess $CdCl_2$.

Figure 15a and b show the surface morphologies of as-deposited CdS films. Figure 16c

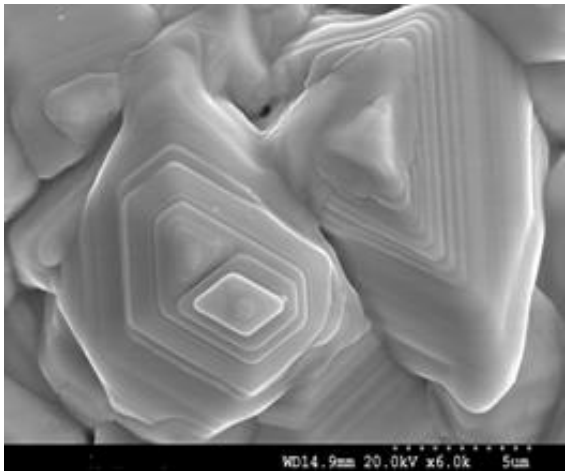
show the surface morphologies of CdTe films after the heat treatment with $CdCl_2$. It is obvious that as deposited CdTe films have a smooth and compact morphology, consisting of crystallites with grain size between average 5μm to 6μm. Films heat treated with $CdCl_2$ have a similar structure to as-deposited films. The anneal produces bulk recrystallization of the CSS-deposited CdTe films and slightly increase the grain size to 7μm to 9μm after $CdCl_2$ treatment (Figure 16c). It can be expected that the performance of solar cells with CdTe films annealed with $CdCl_2$. This is because that $CdCl_2$ treatment increases the grain size and eliminates fast-recombination centers in the CdTe film, eliminates small grains at the grain boundaries, and causes interdiffusion of CdS and CdTe at the interface and decreases the interface recombination.

Figure 15e and f show the cross section SEM images of CdTe film. At the deposition above, it is estimated that thickness of CdTe is the 10μm-15μm. The thickness is much higher than the 6-8μm, therefore thickness needs to be reduced to optimize the series resistance and Voc.

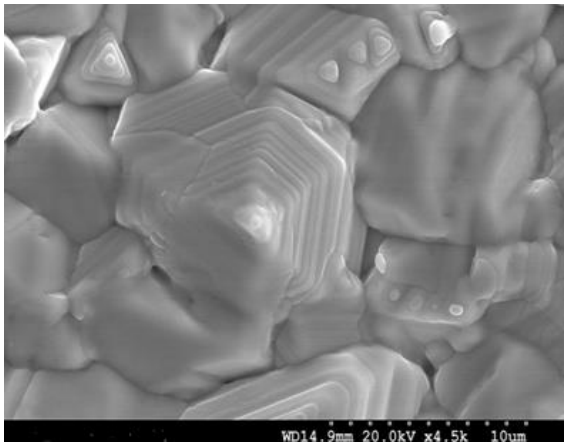
a



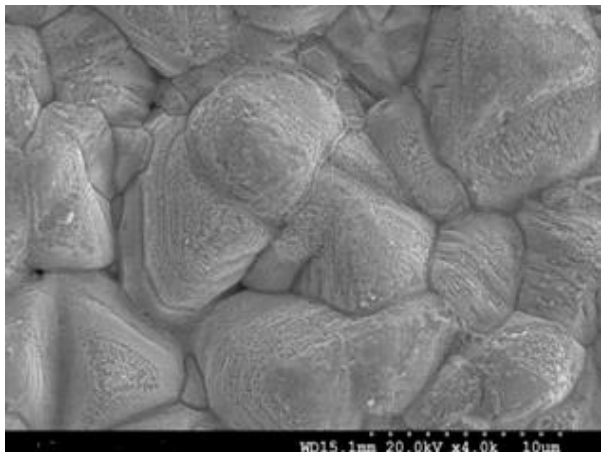
b


WD14.9mm 20.0kV x6.0k 5um

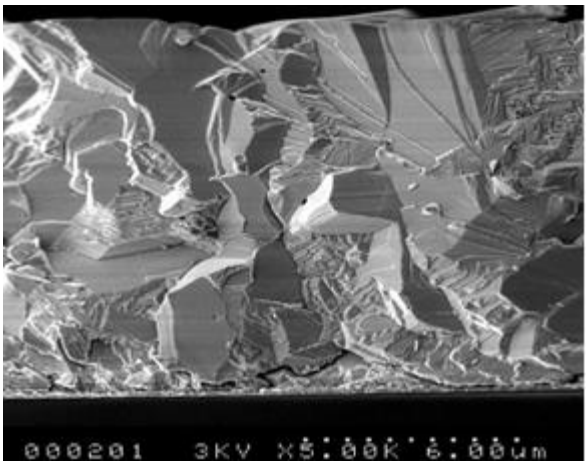
c


WD14.9mm 20.0kV x4.5k 10um

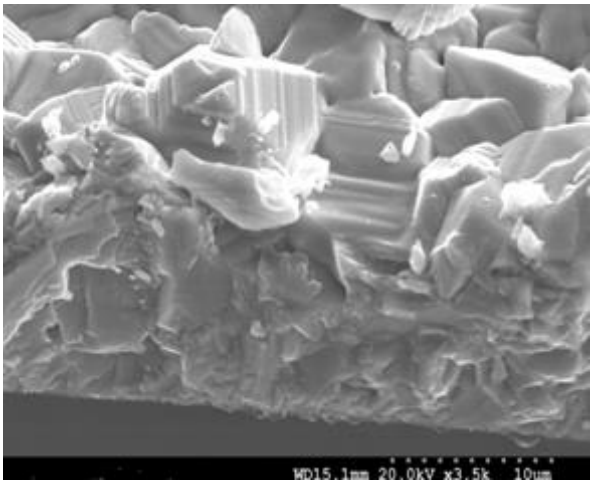
d


WD15.1mm 20.0kV x4.0k 10um

e


000201 3KV X5.00K 6.00um

f


WD15.1mm 20.0kV x3.5k 10um

g

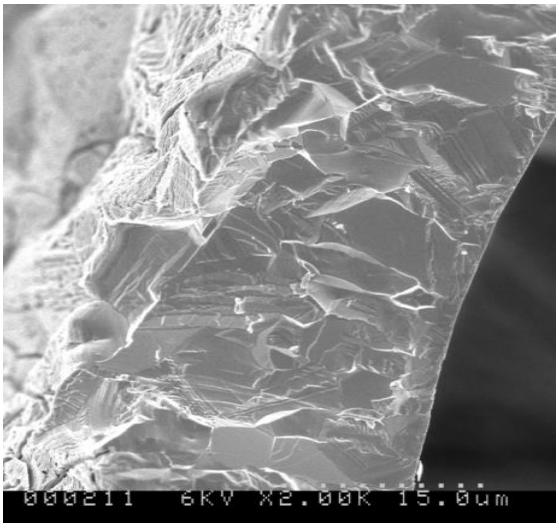

000211 6KV X2.00K 15.0um

Figure 15, The surface morphologies of as-deposited CdS films. (c) the surface morphologies of CdTe films after the heat treatment with $CdCl_2$. (d) the surface morphologies of CdTe films after NP etching. (e), (f) (g)the cross section SEM images of CdTe film**.**

3.5.4 Back Contact Formation

Before the deposition of contact electrode to CdTe, the cells were etched in a solution of nitric and phosphoric acid (NP) (1% HNO_3, 88% H_3PO_4, 35% DI-water) for 35seconds. Figure 16d show the surface morphologies of CdTe films after NP etching. This purpose was to clean up the surface of CdTe film and render it tellurium rich (Te+). The cells were then masked to define the back contact area. Next, 5 nm thick copper layer was deposited onto the back contact area by sputtering. Graphite paste (with 1200-2400 Ω/ml) and silver paste electrodes were painted on to the back contact area. The cells were then heated at 150 ◦C for 10 min to facilitate forming a Cu_2Te layer and for curing the graphite/silver paste electrode. To separate solar cell dots and to define the area of each cell, a cutter tool was used to cut through the p-CdTe and CdS layer. The area of a typical such cut/scratch was measured under an optical microscope. Schematic of the finished nanowire CdS-CdTe solar cells is showed in figure 16.

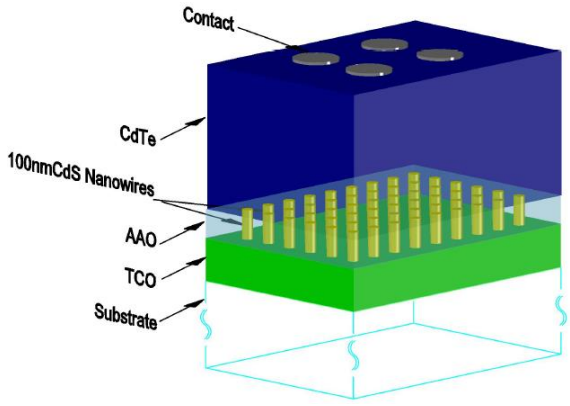


Figure 16, Schematic of the finished nanowire CdS-CdTe solar cells.

Chapter 4 Result and Discussion

4.1 Effect of Anodic Aluminum Oxide Membrane on Performance of Nanostructured Solar Cells

4.1.1. Introduction

Solar energy is one of the most promising renewable energy to meet increasing energy demands in the future. In the past years, tremendous efforts have been devoted in reducing cost and increasing efficiency of photovoltaics such that they can be potentially large-scale deployed[32,45-48]. Recently, particular interests of cost-effective solar cells are to utilize nanostructures or nanostructured materials to reduce volume of semiconductor materials, and enable beneficial optical management, novel conversion mechanism and improvement of carrier generation and collection [39,43,49] .

Anodic aluminum oxide (AAO) membrane has been widely applied into growth of nanostructures[50-53]. Due to it's highly regular and aligned nanoporous structures with high pore density in the range of 10^9-10^{11}cm^{-2} [50], AAO membrane becomes an ideal template for assisted growth of nanometer-scale structures. Most recent, several groups had grown CdS nanostructures through AAO membrane and have configured them intro nanostructured solar cells[38,39,41,54]. The grown nanostructured solar cells mainly focused on nanopillor CdS-[38] or nanowire CdS-CdTe solar cells[39,41,54] because CdTe solar cells have the shortest energy payback time[55] and superior tolerance to high energy irradiation for terrestrial and space applications[24]. These nanostructured CdS-CdTe solar cells have exhibited favorable optical, electrical and mechanical properties[38,39,54]. Specially, in nanowire CdS-CdTe solar cells, CdS nanowires as window layer have enabled light transmission gain in the window layer so that light absorption was enhanced in CdTe absorber[54]. The nanowire CdS-CdTe solar cells have further showed a nearly ideal spectral response of quantum efficiency and their reliability was improved by approximately 3 times. The nanowire CdS-CdTe solar cells grown through AAO membrane enhanced absorption and carrier generation abilities through tuning light transmission of the window layer and simultaneously obtained strong reliability benefits[54].

However, there are concerns for influence of AAO membrane on photovoltaic performance of the nanowire solar cells grown through AAO membrane. These concerns are concentrated on light transmission property of AAO membrane, the effect of AAO on light absorption property of the solar cells, and it's influence on carrier transport, and it's mechanical effect. Herein, we present three geometries of the nanowire CdS-CdTe solar cells to explore the effect of AAO membrane on photovoltaic performance of the

nanowire solar cells. We characterized and compared morpholotical features, spectral response characteristics, dark- light current-voltage (*I-V*), and carrier transport for the three geometries of the nanowire solar cells. We also demonstrate fabrication details in the nanowire growth processes, which can be adopted for other optoelectronic devices to tune light transmission through nanostructures. These results provide insight into absorption, charge transport and carrier collection properties in the nanowire solar cells through AAO membrane-assisted methods.

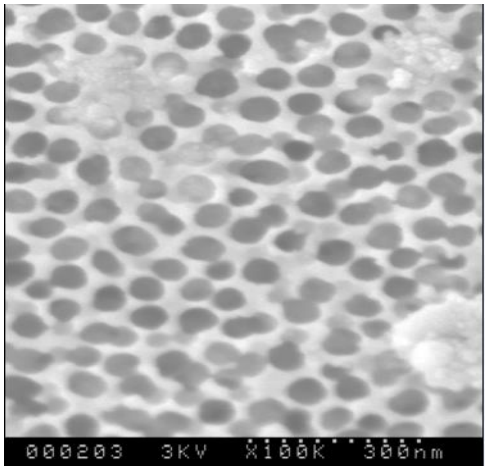
4.1.2 Results and Discussion

4.1.2.1 Nanowire Solar Cell Architecture Characteristics and Analysis

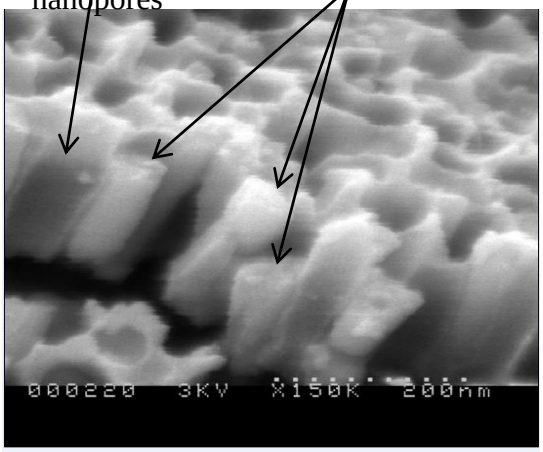
Top view and cross sectional SEM images of three geometry CdS nanowires are shown in Figure 18a, 18b, 18c, 18d and 18e respectively. Figure 18a and 18b show support and constrain of the AAO membrane on the CdS nanowires. As shown in Figure 18c and 18d, removing the AAO membrane forms free standing nanowires. The free standing nanowires can keep their vertical-standing structures on deposition of CdTe. Partially exposed CdS nanowires are revealed in Figure 18e. Long rang, well-aligned and dense rows and columns are characteristics of the three geometric CdS nanowires. Average length, average diameter and the average distance of between the centers of neighboring nanowires are estimated as100nm, 60nm and 106nm respectively. Thus, porosity and area density of CdS nanowires are calculated as approximately 32% and $1.14*10^{10}$ nanowires/cm^2. These nanowires can maintain their original nanowire structures even when they are treated with multiple high temperature annealing processes, which is obviously better than nanocrystalline reported in the literature[32]. In other words, CdS nanowires and AAO membrane typically take up only about 32% and 68% of physical area respectively. It is expected that when they function as the nanowire window

layer, they will exhibit unique optical and electrical properties different from those of planar CdS window layer.

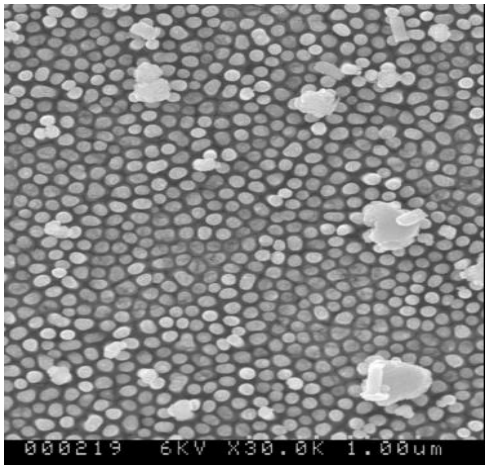
a



b

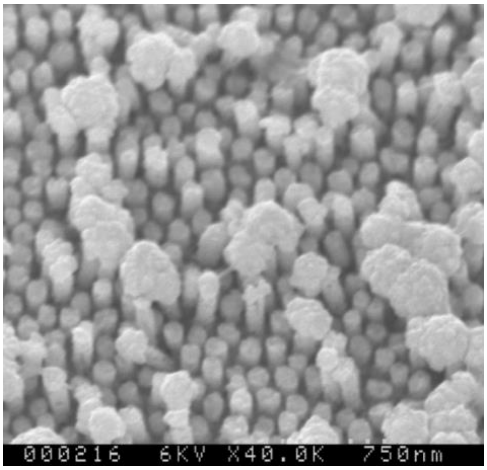


c



d

e



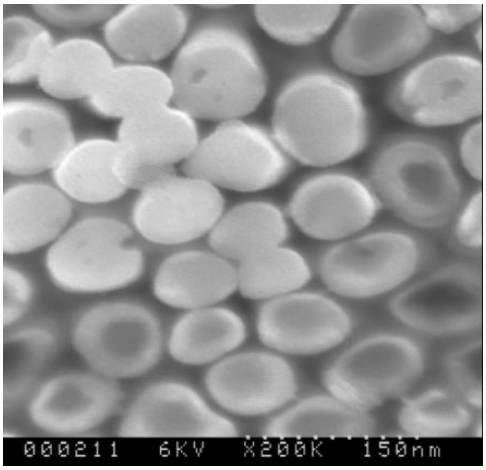


Figure 17, a) Top view and b) cross sectional SEM images of the CdS nanowires fully embedded in the AAO membrane. c) Top view and d) cross sectional SEM images of the free-standing CdS nanowires. e) Top view SEM images of the CdS nanowires partially embedded in the AAO membrane.

4.1.2.2. Optial Characteristics of Three Geometric CdS Nanowires

For CdS window layer-CdTe absorber layer solar cell architecture, high power conversion efficiency depends on solar spectrum range of photons transmitted through the window layer and further reached in the CdTe absorber. Hence, it is important to characterize transmission of the three geometric CdS nanowires over a broad range of wavelengths (300-860nm), covering a light spectra from very low wavelength to bandgap edge of CdTe absorber. Figure 19 summarizes transmittance spectra of the three geometric CdS nanowires. Compare with transmittance of the free standing CdS nanowires, the fully embedded and partially embedded CdS nanowires demonstrate similar and close transmittance behaviors at the wide wavelength range from 300nm-860nm. It further confirms that AAO membrane has a negligible absorption behavior. Observed from Figure 19, strong transmission of the three geometric CdS nanowires begin at approximately 350nm, which reveals higher bandgap of CdS nanowires arising from confinement of AAO nanopores[39,41,53]. SEM images of the CdS nanowires have shown that CdS nanowires and AAO membrane occupy 32% and 68% of physical area in

the window layer respectively. For CdS nanowires fully or partially embedded in AAO membrane as the nanowire window layer, a part of incident light across the entire spectrum range can directly transmit through absorption-negligible AAO membrane, and the other part of incident light is transmitted through CdS nanowires with high transmission due to their larger effective energy band gap[39,41,53]. For comparison, in free standing CdS nanowires, those incident lights transmitted through AAO membrane will directly reach the CdTe absorber through air ambient. As a result, much broader and stronger spectral range of incident light reaches the CdTe absorber layer where photons are absorbed. In addition, the front surface recombination loss which deteriorates device performance of the nanostructure silicon solar cells is effectively avoided because the photons of the wide wavelength are efficiently guided into CdTe absorber through the nanowire CdS window layer. In other words, AAO membrane-assisted grown CdS nanowires effectively increase light transmission in the window layer and thus improve the absorption of CdTe absorber.

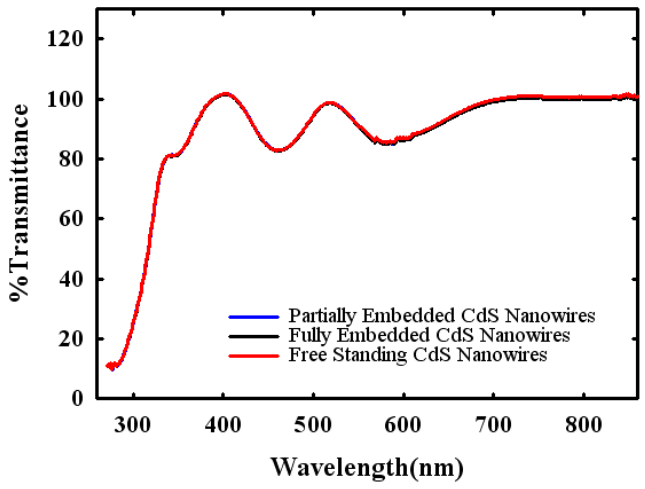


Figure 18, Transmittance spectra of fully embedded, partially embedded and free-standing CdS nanowires.

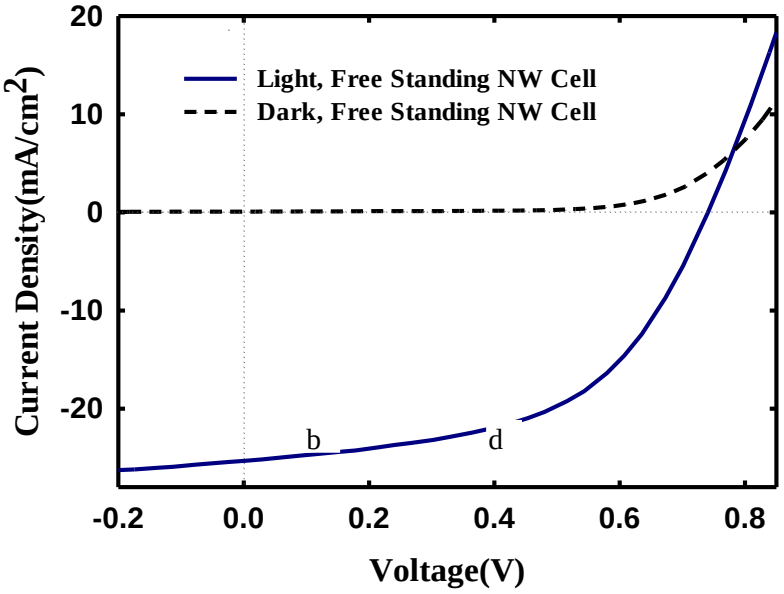
4.1.2.3 J-V Characteristics of Three Geometric Nanowire CdS-CdTe solar cells

AAO membrane can form interfaces with CdTe, and influence of these interfaces on the photovoltaic properties were characterized through studying the three geometric nanowire solar cells under dark and 100mW/cm^2 illumination. Figure 20a, 20b and 20c show the J-V characteristics of the three geometric nanowire solar cells, and Figure 20d illustrates comparison of their J-V data. Crossover between dark and illuminated J –V curves is observed in the three geometric nanowire solar cells, which is commonly related with photoconductivity of CdS nanowires and CdTe as well as the space charge variation under illumination.

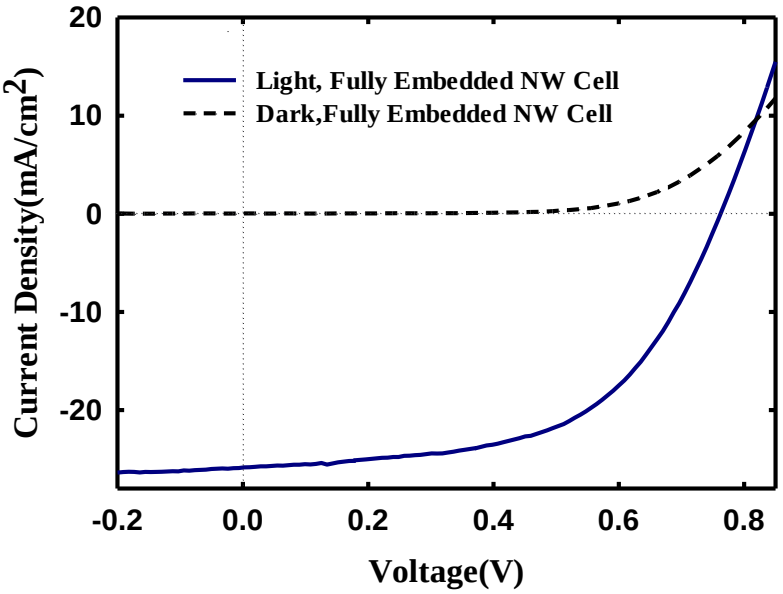
Two macroscopic parameters-diode quality factor (N) and reverse saturation current density (J_o) that describe the performance of the main junction are extracted from dark J-V curves. Extraction of N and J_o is taken from the slope and intercept of the dark ln(J)-V data in forward bias between 0.35 and 0.65V, which avoids influence of series and shunt resistances on collection of accurate value. N and J_o from dark J-V data are shown in Table 2. It is clearly demonstrated that the partially embedded nanowire solar cells (PENSC) have the N of 2.50 and J_o of $6.32*10^{-8}$ A/cm^2, which are obviously lower than corresponding value of 2.79, and $1.19*10^{-7}$ A/cm^2 of the free standing nanowire solar cells (FSNSC). In addition, the fully embedded nanowire solar cells (FENSC) shows the n of 2.53 and and J_o of $6.45*10^{-8}$ A/cm^2, slightly higher those of PENSC. N and J_o represent interface defects, traps and junction behavior. Higher N and and J_o indicate that there are a large amount of interface defects and traps, which induce interface recombination and tunneling currents in the free standing nanowire solar cells. Through maintaining CdS nanowires in AAO membrane for partially embedded and fully

embedded nanowire solar cells, interface defects, traps and junction behavior are noticeably improved. Given that Fill factor and V_{oc} are directly affected by the values of N and J_o, the lower *N* and J_o are desirable for the better device performance. Hence, AAO membrane has a mechanism to benefit interface and junction behaviors between CdS nanowire and CdTe film, which reduces the dark recombination current and improves device performance.

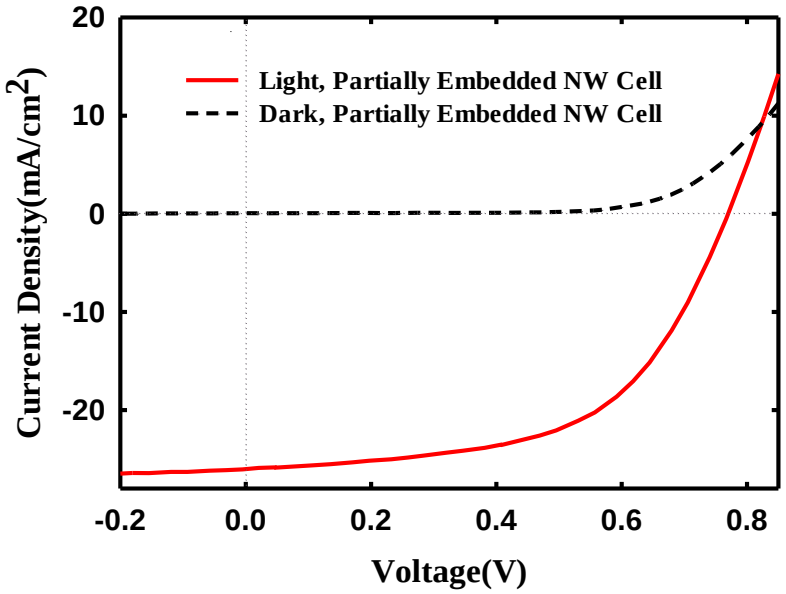
a



b


Light, Fully Embedded NW Cell
Dark,Fully Embedded NW Cell
Current Density(mA/cm2)
Voltage(V)
20
10
0
-10
-20
-0.2
0.0
0.2
0.4
0.6
0.8

c



d

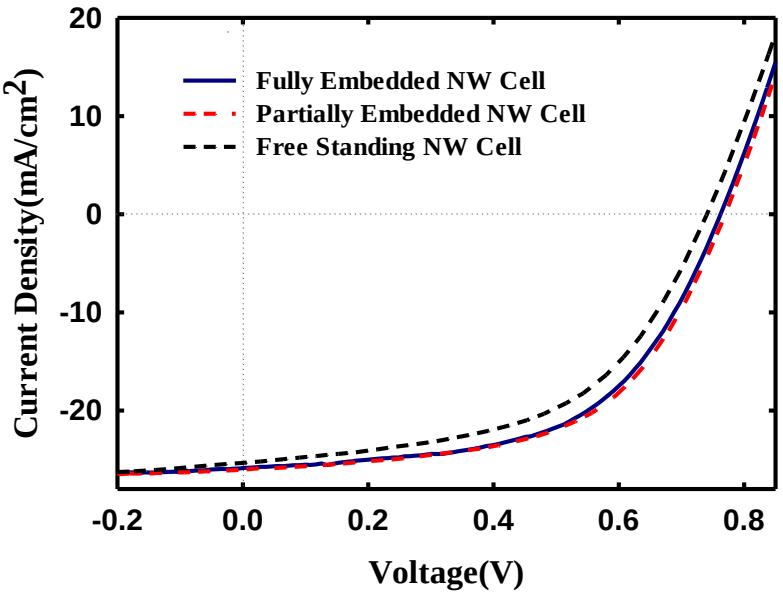


Figure 19, J-V characteristics of (a) free standing nanowire solar cells, (b) fully embedded nanowire solar cells, and (c) partially embedded nanowire solar cells respectively. (d) J-V comparision of the three geometric nanowire solar cells.

Under a full sun intensity of 100 mW/cm^2, the partially embedded nanowire solar cells exhibit short current density (J_{sc}) of 25.9mA/cm^2, open circuit voltage (V_{oc}) of 764mV and fill factor of 57.1%, which results in an overall power conversion efficiency of 11.29%. The fully embedded nanowire solar cells are characterized by J_{sc} of

25.85mA/cm^2, open circuit voltage (V_{oc}) of 762mV, fill factor of 56.5%, and power conversion efficiency of 11.09%. Compared to other two geometric cells, the power conversion efficiency in the free standing nanowire solar cells reduced to 9.9%, because the J_{sc} , V_{oc} and FF are respectively decresed to 25.3mA/cm^2, 738mV and 53%. The comparison illustrates the role of structure on device performance.

Table 2 Photovoltaic data of the three geometric nanowire solar cells.

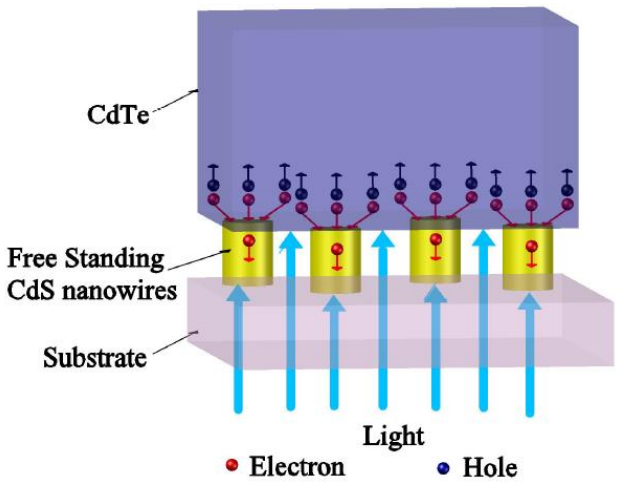
Structure	n	Jo(A/cm^2)	J_{sc}(mA/cm^2)	V_{oc} (mV)	FF(%)	Efficiency (%)	Rs(Ω /cm^2)	Shunt Resistance (Ω /cm^2)
PENSC	2.50	6.32*10^{-8}	25.9	764	57.1	11.29	4.46	286
FENSC	2.53	6.45*10^{-8}	25.85	762	56.5	11.09	4.47	272
FSNSC	2.79	1.19*10^{-7}	25.3	738	53	9.9	4.86	219

Figure 21a, 21b and 21c show schematics of light transmission of window layer, and electron-hole separation and transport in the three geometric nanowire solar cells. The three gemotric nanowire solar cells exhibit large short current density exceeding 25mA/cm^2. High J_{sc} is attributed to CdS nanowire window layer, which transmits wider spectrum through the CdS nanowires (occupy 32% of the window layer), and also transmits the whole spectrum through air or transparent AAO membrane (occupy 68% of the window layer). High transmission in the CdS nanowire window layer leads to more photons directed into the CdTe and improved absorption there. Hence, this result is in an agreement with the light transmittance spectra of the three geometric CdS nanowires in Figure 19.

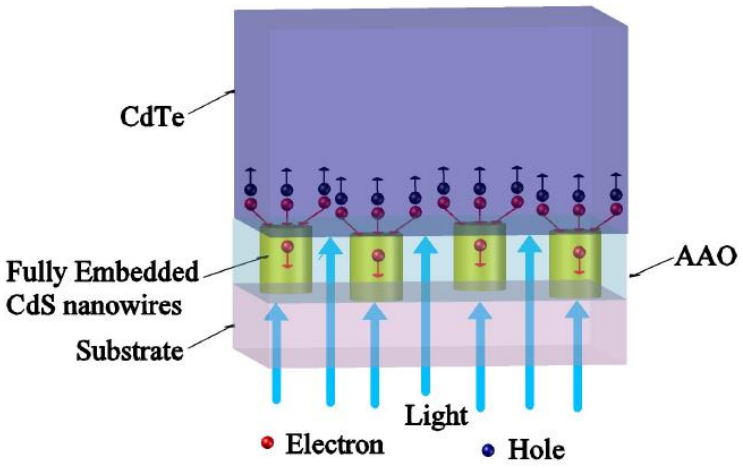
Similar transmission spectrum characteristics of the three geometric CdS nanowires

suggest that approximately equal photoexcited carriers are created in CdTe film. Then J_{sc} depends on effective carrier transport through interface and bulk. Observed from Figure 21a and 21b, CdS nanowires only form junction with CdTe on the top of the individual CdS nanowires, and CdTe forms interface with AAO membrane (Figure 21b, fully embedded nanowire) or CdTe forms interface with air (Figure 21a, free-standing nanowires) in the rest of area in the window layer. As shown in the Figure 21c, because CdS nanowires are exposed approximately 20nm, and CdTe crystals contact not only the top but also the lateral sides of the CdS nanowires, junction is formed on the top and lateral sides of the CdS nanowires. In addition, those CdTe crystal area contacting sides of the CdS nanowires is supported by 80nm-long AAO membrane and forms the interface with it.

a



b



c

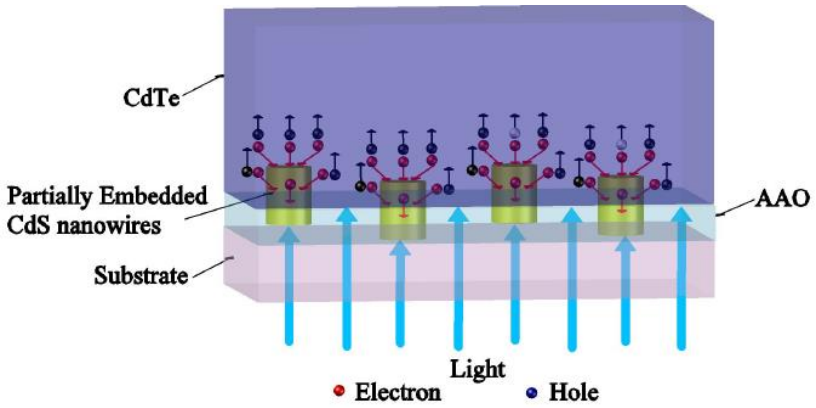


Figure 20, Schematics of carrier generation and transport in a) free standing nanowire solar cells, b) fully embedded nanowire solar cells and c) partially embedded nanowire solar cells respectively.

As shown in Figure 21a, in the free standing nanowire solar cells, CdTe above CdTe-air interface exposure to outer ambient exacerbates interface defects and traps. It is possible that humidity and oxygen can penetrate into interface of CdS nanowires and CdTe. As a result, oxygen migration forms an oxidation layer and leads the traps and interface defects, which block carrier transport. Hence, higher N and J_0, and lower J_{sc} and V_{oc} are observed. Further, CdTe-Air interface provides shunting paths such that CdTe tentacles can directly contact with SnO_2, and form microjunction. The free standing nanowire solar

cells exhibit low shunting resistance of 219Ω/cm^2 and low shunting resistance is responsible for low V_{oc}.

Through maintaining AAO membrane as the part of window layer, interface defects and traps due to humidity and oxygen are reduced. Further, due to insulting property of AAO membrane, it prevents the formation of CdTe-SnO_2 microjunction. Consequently, photovoltaic performance of the devices is obviously improved, and efficiency is enhanced to over 11%. As shown in the Figure 21d and table 2, the partially embedded nanowire solar cells show the efficiency slightly higher than the fully embedded nanowire solar cells. In the fully embedded nanowire solar cells, non-ideal and non-uniform nanowire growth makes a few nanometer growth discrepancies possible. Although CdTe has high possibility to contact individual CdS nanowires, existence of gaps inevitably increases interface roughness and introduce interface defects, which have been revealed by the slightly increased N and J_o and reduced fill factor. Partially removing AAO and exposing CdS nanowires with 20nm avoid nanometer level gaps between CdS nanowires and CdTe as well as CdTe exposure to ambience. Furthermore, because CdTe above AAO membrane laterally contacts the CdS nanowires, a most of electron-hole pairs are generated in axial direction and also a small quantity of electron-hole pairs are generated in lateral direction (Figure 21c). The carrier generation and collection are improved. Efficiency is increased to approximately 11.3%.

Figure 21 shows that photoexcited electrons above AAO and air travel an extra distance (approximately 50nm according to SEM images) to reach the CdS nanowires. The extra distance could incur additional resistance. It is concerned if such extra transport distance could result in large series resistance. It has been reported that light absorption

occurs in CdTe depletion region within a micrometer range[34]. In high electrical field depletion region of CdTe, carriers can be quickly drifted into opposite sides and are collected. Therefore 50nm extra distance much less than micrometers only causes a slight increase in series resistance. High series resistance in the three geometric nanowire solar cells is arising from CdTe film and back contacts, which graphite paste used in our laboratory to form back contacts has sheet resistance of 1200-2400Ω/sql. A detail analysis on the extra resistance will be in a future project.

In addition, we found that by including AAO membrane to embed the CdS nanowire, reliability of the nanowire solar cells is improved. Electrically insulating property of the AAO membrane and the low defect features in the CdS nanowires prevent the deep diffusion of Cu ions (Cu usually included in the back contacts to p-CdTe) into the CdS nanowires and then into SnO_2. The main CdS-CdTe junction and the Cu-induced conducting contact behavior are maintained. In other words, AAO membrane provides additional mechanical advantages expect its favorable optical-electrical properties.

4.1.2. 4. Conclusion

We grew 100nm long and well aligned CdS nanowires which are fully embedded and partially embedded in AAO membrane are as well as a free standing form to function as nanowire window layer. The nanowire window layers are configured into solar cells to investigate effect of AAO membrane on device performance. The three geometric CdS nanowires show similar transmittance spectra, indicating that AAO membrane has negligible-absorption property and the number of photons absorbed by CdTe absorber is approximately equal. Hence, power conversion efficiency is related with carrier transport and collection. Free standing nanowire solar cells have efficiency of 9.9%, and through inclusion of AAO in the solar cell structure, efficiency is improved to approximately

11.1%. Further structure optimization through partially exposed CdS nanowires yields efficiency of approximately 11.3%. Reasons are indentified that i) AAO membrane effectively reduces interface defects and traps caused by humidity and oxygen in the free standing devices; Further, ii) it prevents direct contact of CdTe tentacles with SnO_2 and formation of microjunction. Partially embedded nanowire solar cells further reduces influence of non-ideal and non-uniform nanowire growth and generates a most of carriers in axial direction and also a small quantity of carriers in lateral direction, thus becoming a promising solar cell structure. Including AAO membrane in solar cell structure can obtain favorable optical-electrical properties as well as mechanical advantages.

4.2 Embedded Nanowire Window Layers for the Enhancement of Quantum Efficiency in Window-Absorber Type Solar Cells

4.2.1 Spectral Transmittance of CdS Nanowire Window Layer

For gaining a quantitative understanding of the transmission advantage of the 100 nm long, embedded CdS nanowires layer over the 100 nm thick, traditional planar CdS film, we compared the spectral transmission of both in the wavelength range of 300-860 nm (Figure 22a). The substrate in both cases was a 100 nm thick tin oxide (SnO_2) layer sputtered on top of the ITO-coated-soda lime glass. The transmission spectrum of the 100nm thick AAO membrane (Figure 22b) exhibits practically complete transmission at wavelengths longer than 240nm. It is clear that absorption-negligible characteristics displayed by AAO membranes make them an ideal choice for the development of nanostructure designs for a host of applications in solar cells and other optoelectronic devices.

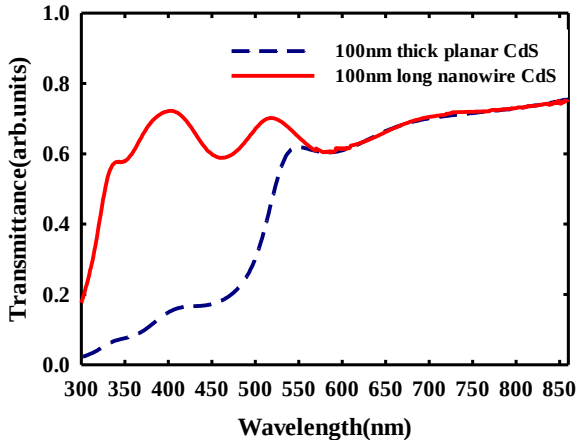
At wavelengths longer than 550 nm, where the photon energy is smaller than 2.4 eV

(the energy band gap of planar CdS), the two curves overlap each other. However, the CdS nanowire curve shows substantially higher transmission from 335 nm to 550 nm, while in this wavelength range, the spectral transmission of planar CdS is very poor. This difference could arise from, (i) the larger effective energy band gap of the nanowire CdS layer leading to higher optical transmission than that of the planar CdS layer[39-41]and/or, (ii) the nanowire CdS covering only a fraction (32%) of the substrate, the rest covered by the embedding AAO matrix.

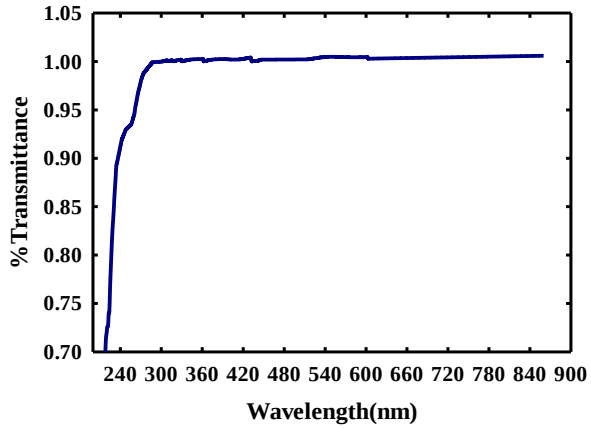
In the long wavelength range, for example at 860 nm, the transmission of the CdS-SnO_2-ITO-soda lime glass stack is about 70%. Thus, substantial optical losses are due to the intrinsic-SnO_2/ITO/the soda-lime glass. Higher transmission can be obtained by replacing the intrinsic-SnO_2/ ITO/the soda-lime glass with a higher transmission, higher quality substrate[32]. On the other hand, the higher transmission glass is more expensive and would add to the manufacturing costs.

It is clear that the CdS nanowires as the novel window layer suppresses the absorption loss at wavelengths below 550 nm and the spectral range of photons reaching the CdTe absorber is dramatically increased to 300-860 nm, compared to the 512 -860 nm range for the case of the planar CdS counterpart. In addition, because the photons of low wavelengths are efficiently guided into the absorber layer, the front surface recombination loss which often exists and deteriorates device performance in the silicon solar cells [43] is effectively avoided. Because of the fact that the photons are absorbed and converted to the photocurrent in the absorber layer, the two effects lead to enhanced carrier conversion for the nanowire solar cell configuration.

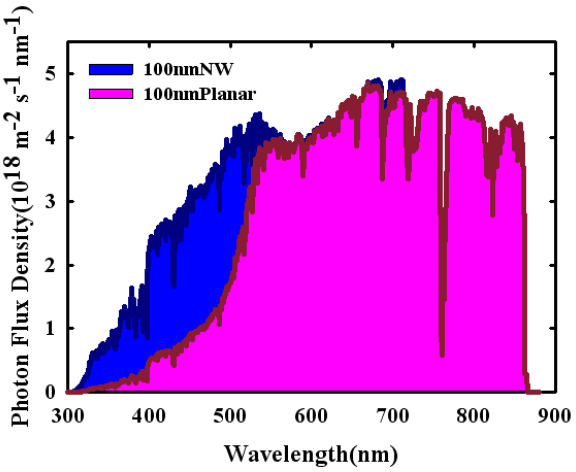
a


100nm thick planar CdS
100nm long nanowire CdS
Transmittance(arb.units)
Wavelength(nm)

b


%Transmittance
Wavelength(nm)

c


100nmNW
100nmPlanar
Photon Flux Density(10^18 m^-2 s^-1 nm^-1)
Wavelength(nm)

d

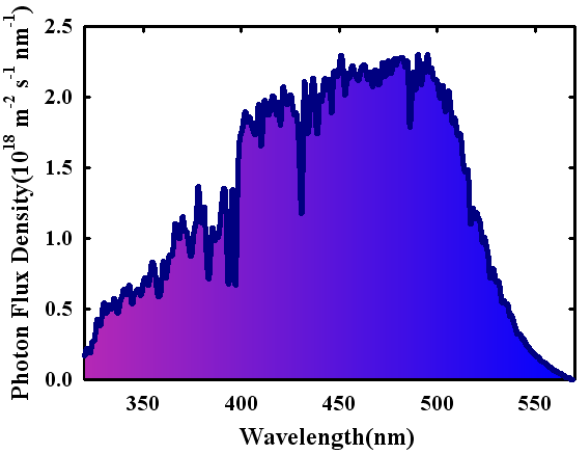


Figure 21 Transmission spectra of, (a), the 100 nm long embedded CdS nanowires and of 100 nm thick planar CdS film; (b),100 nm thick AAO membrane; (c), Photon flux density comparison of the CdS nanowire and planar solar cells; (d), Photon enhancement in the CdS nanowire solar cells; in all cases, the substrates is SnO_2/ITO/Soda-lime glass.

To gauge the effect of the transmission enhancement advantage of the CdS nanowires on the photocurrent (J_{sc}) of the nanowire solar cells, the overall photon flux (P) reaching the CdTe absorber was calculated. Figure 3C shows the photon flux $P_{nanowires}$ that can be converted to the photocurrent in the nanowire solar cells, and also shows the photon flux P_{planar} in the planar solar cells for comparison. The nanowire solar cells yield the photon flux which is higher than that of its planar counterpart in the wavelength range of 300 nm to 550 nm. The additional photon flux reaching the CdTe absorber layer because of the enhanced transmission of CdS nanowires window layer is plotted as a function of wavelength in Figure 3D.

The photon flux data of Figure 22 indicates that a solar cell employing a CdS nanowire window layer would yield a higher J_{sc} value than the cell with a planar CdS window layer. It is estimated that the total number of carriers and J_{sc} are $18.65*10^{16}/cm^2s$ and 29.84 mA/cm^2 for the nanowire solar cells. These numbers exceed the corresponding values of $15.64*10^{16}/cm^2s$ and 25.03 mA/cm^2 for the planar counterpart. The J_{sc}

increases by 4.81 mA/cm^2, which corresponds to a gain of 19.2% when the CdS nanowires window layer replaces the planar CdS window layer. In a hypothetical case where transmittance of a substrate is approximate 100%, J_{sc} values for the nanowire solar cells and counterpart planar solar cells were calculated to be 32.1 mA/cm^2 and 26.6 mA/cm^2 respectively, constituting an increase of 5.49 mA/cm^2 in J_{sc} and a gain of 20.6% over the base. Hence, one can expect even higher J_{sc} values in the future, when intrinsic SnO_2/ITO-soda lime glass substrates in the present device configuration are replaced by high quality transparent substrates.

Another advantage of the nanowire solar cells is that because CdS nanowires embedded in AAO templates typically take up only about 32% of the physical area, the interface area at the junction between CdS nanowires and CdTe is reduced approximately by a factor of 3. When interface recombination is the dominant electron transport mechanism across the heterojunction, which appears to be the case for these CdS-CdTe solar cells, then reduction in interface area would lead to an equivalent reduction in the effective reverse saturation current I_0. Since the open circuit voltage V_{oc} is dependent on I_0 and short current I_{sc}, both of these effects would result in gain of approximately 7.3% in V_{oc}. Overall, the J_{sc} gain of 19.2% and the V_{oc} gain of 7.3% would lead to a cumulative gain of 27.8% in the power conversion efficiency of the CdTe solar cell on intrinsic SnO_2/ITO-soda lime glass substrates. The corresponding gain in the power conversion efficiency of the CdTe solar cell on high quality transparent substrates would be 30%.

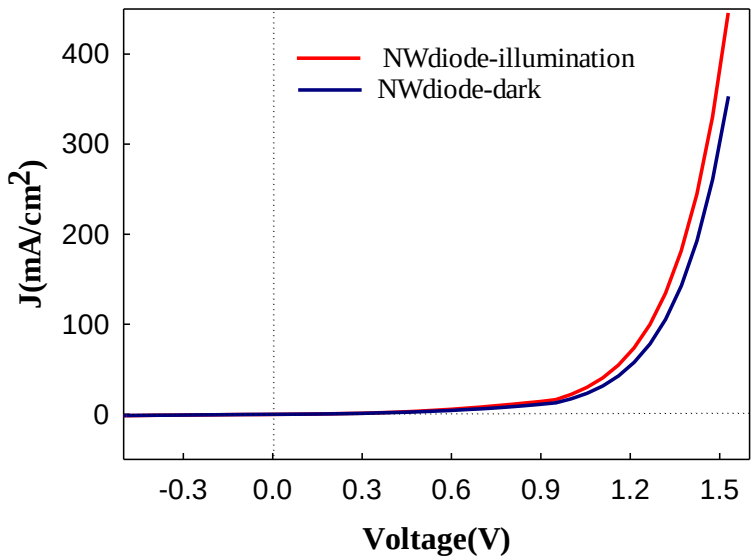
4.2.2 Current-Voltage Characteristics of Nanowire CdS/Au Schottky Diode

For a more detailed characterization of the CdS nanowire surfaces, and the electron

transport through the CdS nanowire arrays, Schottky diodes were produced by selectively etching AAO templates to partially expose the CdS nanowires, and then depositing Au contacts on the top of the CdS nanowires through a circular mask of 1/8 inch diameter, corresponding to an electrode area of 0.07 cm^2. For comparison, identical Au contacts were deposited on the planar CdS to form Au/CdS film Schottky diodes. Note that in the case of the nanowire CdS device, the actual CdS-Au junction area is only 0.022 cm^2, which is 32% of the electrode area of 0.07 cm^2. This is because the porosity is 32% and CdS nanowires occupy only that fraction of interface area; the rest is aluminum oxide. In case of planar CdS device, the electrode area and the CdS-Au junction area are the same.

Next, current-voltage characteristics of Au/CdS Schottky diodes were measured in dark and under "one sun" illumination; here, gold contact was biased positively with respect to the bottom ITO contact. The "nominal" current density versus voltage (J–V) characteristics of the Au/CdS nanowire Schottky diodes are shown in Fig. 23a. For comparison, J-V characteristics of Au/CdS film Schottky diodes are shown in Fig. 23b. In the current voltage characteristics of both CdS nanowire diodes and CdS thin film diodes, current increased slightly over its dark value, when sunlight was incident. This is thought to be due to additional light generated electron-hole pairs in CdS.

a



b

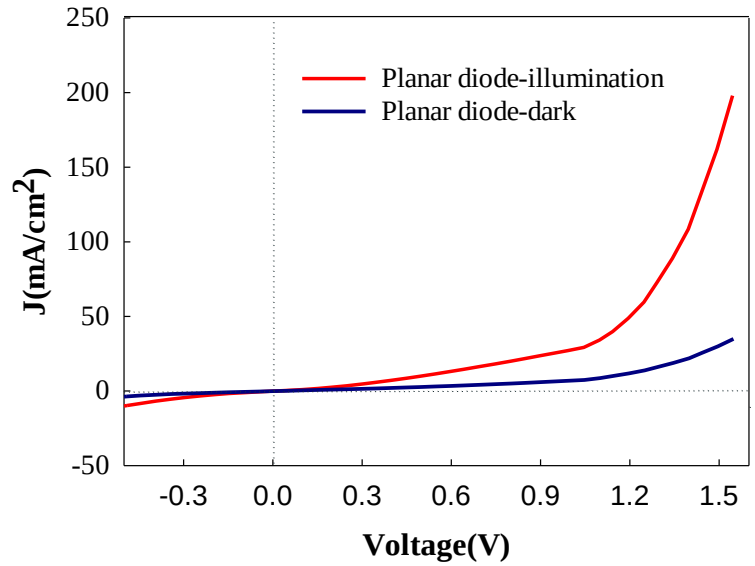


Figure 22, Current density versus voltage characteristics of Schottky diodes made of; (a): Au/CdS nanowire array; (b): Au/CdS planar thin film.

Analysis of J vs. V data of the Schottky diode on nanowire CdS layer of Fig. 23(a) yielded the effective reverse saturation current density (J_{01}) and diode ideality factor (A) values of $5.1*10^{-7}$ A/cm^2 and 3.67 in the dark and $6.7*10^{-7}$ A/cm^2 and 3.68 in light. These are "nominal" values in that the electrode area of 0.07 cm^2 was used for calculating

J_{01}. The "actual" effective reverse saturation current density (J_{02}) values *inside* the CdS nanowires are, J_{02} =1.6 x10^{-6} A/ cm^2 in dark and J_{02} =2.1x10^{-6} A/ cm^2 under one sun illumination. The CdS nanowire surface area of 0.022 cm^2 was used for calculating the "actual", J_{02}. Values of diode ideality factors (A), are not affected by the above change in area.

Similar analysis of J vs. V data of the Schottky diode on planar CdS film of Fig. 23(b) yielded the effective reverse saturation current density (J_o) and diode ideality factor (A) values of 8.5*10^{-6} A/cm^2 and 6.2 in the dark and 6.0*10^{-5} A/cm^2 and 6.6 in light.

In Fig.23, CdS nanowire diodes show higher current density in forward bias than the CdS film devices. This is thought to be related to a higher concentration of electrons in the CdS nanowire arrays. A super-stoichiometric content of Cd atoms in CdS crystals has been observed in the past by various researchers [18, 19]. Conductance measurements on the CdS nanowires yielded conductivity values of 355µScm^{-1} and 279 µScm^{-1} for nanowires under one sun illumination and in the dark respectively. The corresponding values for the CdS films were 43.6µScm^{-1} and 7.4 µScm^{-1}. Thus, under illumination, the conductivity of the nanowire arrays increased by 27.4%, while the conductivity of the film was enhanced by 491.7%. This widely different effect of sunlight radiation could be related to the fact that the effective energy band gap of CdS nanowires is substantially higher than that of CdS film and is therefore less responsive to the sunlight radiation, which is simply transmitted through.

4.2.3 C-V characteristics of nanowire CdS/Au Schottky diode

Capacitance-voltage measurements were conducted to study the behavior of depletion layer at the Au-CdS nanowire junction in the Schottky diode. The resulting plot of C^{-2}

versus V at a measurement frequency of 1MHz is shown in Fig.24. It is nonlinear. Therefore, equation (4) below was used for determining the variation in net space charge density, qN(x), near the junction interface [10].

$$N(x) = \frac{2}{qA^2\varepsilon_s}\left[-\frac{1}{d(1/(C_D^2))/dV}\right] \quad \text{.....(8)}$$

Here, qN (x) is the net space charge density; x is the depletion layer depth into CdS from the Au–CdS interface; q is the charge of one electron; A is junction area; C_D is the measured device capacitance in Farads. Capacitance-frequency measurements done earlier had revealed that at the relatively high measurement frequency of 1MHz, the deep defects and traps in CdS could not follow the measurement signal, and therefore, N(x) was a reasonably reliable measure of effective carrier concentration in CdS at the edge of depletion layer.

At zero bias, the junction capacitance per unit area was 1.88 $x10^{-7}$ F/cm^2, corresponding to a depletion layer width of 25.4 nm. For all calculations in this section, the surface area of CdS nanowires (0.022 cm^2) was used as the junction area.

From the slope of plot in Fig.24 in the lower amplitude reverse bias region, equation (4) yielded N(x)= $3.4x10^{17}$ cm^{-3} at x=29.7 nm, which corresponds to a plane at a distance of 29.7 nm from the Au/CdS interface. Similarly, a value of N(x) = $4.6x10^{16}$ cm^{-3}, was obtained in the higher amplitude reverse bias region, for x= 80.5 nm, a plane at a distance of 80.5 nm from the Au/CdS junction.

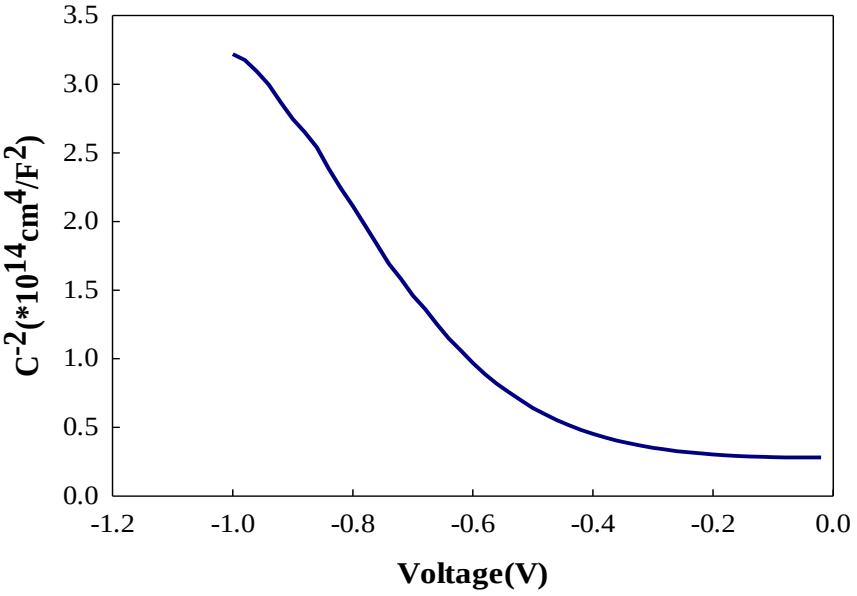


Figure 23, C^{-2} Vs. V Characteristic of a nanowire CdS/Au Schottky diode

This variation from $3.4x10^{17}$ cm^{-3} to $4.6x10^{16}$ cm^{-3} in effective carrier concentration along the length of CdS nanowire is thought to be related to $CdCl_2$ annealing treatment of the CdS layer prior to the deposition of Au contact. During the $CdCl_2$ heat treatment, chlorine accumulates at the surface of CdS nanowires. Chlorine is a known n-type dopant for CdS; it makes CdS nanowire highly conductive (n^+) at the top (near the Au-CdS junction). It has been reported in many earlier studies that $CdCl_2$ treatment is very effective in improving the structural and electro-optical characteristics of the CdS-based diodes and solar cells. We have found from our preliminary nanowire solar cell experiments that the efficiency of nanowire CdS/CdTe solar cells shows same value or improved value when subjected to multiple $CdCl_2$ treatments; however, the efficiency values of planar CdS/CdTe solar cells are greatly reduced with even one time over-treatment or after a second $CdCl_2$ treatment. This indicates that nanowire CdS/CdTe solar cells can avoid some of the negative effects found in their planar counterparts for $CdCl_2$ treatments, and

their performance can be repeatedly reactivated by $CdCl_2$ treatments. In any case, it is clear that $CdCl_2$ treatments affect the structural and electro-optical properties of nanowire CdS-based devices in a number of complex ways. These effects are currently under investigation in our laboratory.

Relatively high conductivity of CdS nanowires is a positive feature in terms of the performance of the CdS-CdTe solar cell. Similarly high carrier concentration values have been reported earlier by NREL group on the CdS side of their high efficiency CdS/CdTe solar cells [24]. Carrier concentration in their CdS film varied from 10^{18} cm^{-3} at the surface to 10^{14} cm^{-3} in the bulk. Using a CVD process, Ma et al. [25] produced indium-doped CdS nanowire with carrier concentration of $(2.7 \pm 0.2) \times 10^{17}$ cm^{-3}. However, their process required the use of a metal catalyst. For solar cell applications, such a catalyst can cause defects and recombination centers which are not desirable.

4.2.4 Quantum Efficiency of Nanowire CdS-CdTe Solar Cells

Figure 25a shows the normalized spectral response of the external quantum efficiency (EQE) of the (intrinsic soda-lime glass/ITO/ intrinsic SnO_2/NW-CdS/CdTe/graphite paste) solar cell device, which was measured by an independent group at the PV Measurements Inc.[56]. EQE value increases steadily from 40% at 335 nm to 80% at 380 nm, and 90% at 400 nm; it peaks at 535 nm, and then stays practically constant until reaching the energy band gap edge of the CdTe absorber layer. In the 300 nm to 550 nm wavelength range, the EQE response of the nanowire solar cells, shown in Figure 25a, is substantially higher than reported by other groups who have tried to enhance the quantum efficiency of CdS-CdTe solar cells by various other methods, which include reducing the thickness of the planar CdS window layer and increasing the optical

energy band gap by alloying[32,36,45-47,55,57-62]. Such strong EQE response at very wide spectral range proves that the CdS-CdTe solar cells including CdS nanowires as the window layer enhance light absorption and carrier generation and collection. It should be noted that the above device is built on the inexpensive and low transparent intrinsic SnO_2/ITO/soda lime glass substrate. Later, when such low transparent substrate is replaced by a higher transmission substrate, the EQE response of the nanowire window-absorber solar cells will be even further improved.

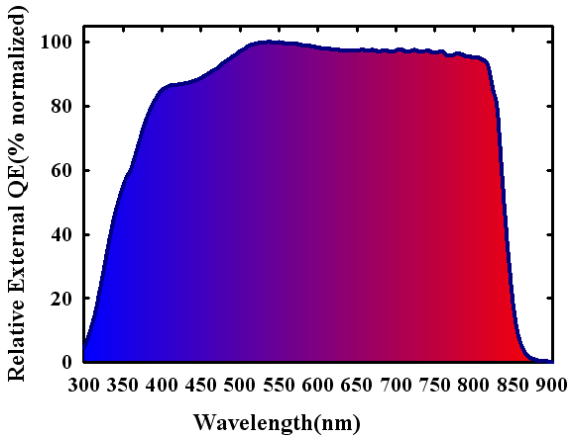
Wu et al used nanocrystalline CdS:O of 70-80 nm thickness for the window layer[32]. However EQE enhancement in their device was much smaller than seen in Figure 25a. In their case[32], EQE reached 90% of its maximum value at approximately 500 nm, while for our device, EQE reaches 90% at 400 nm. One possible reason is that our embedded CdS nanowires can maintain their fine nanostructured features even when exposed to subsequent high temperature CdTe deposition and $CdCl_2$ annealing treatments. On the other hand, Wu et al's nanocrystalline CdS film (nano-CdS: O) can lose its nanocrystalline structure feature due to the grain growth and recrystallization that happen during the high temperature treatments.

Energy band gap widening in CdS by alloying is another approach that has been investigated[36]. However, the EQE response seen in Figure 25a is higher than the EQE response of their device[36] not only in the (300-550) nm wavelength range, but also in the (550-850) nm range. A possible reason for this may be that alloying led to the creation of impurities and defects, which enhanced the optical scattering in CdS and possibly increased electron-hole recombination in CdTe near the CdS-CdTe heterojunction.

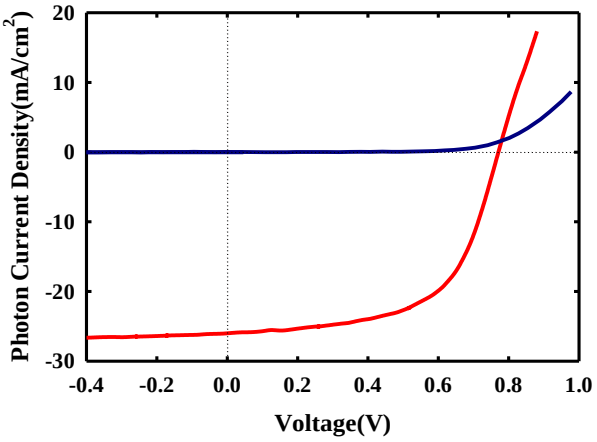
Also, comparing the EQE response of Figure 4A in the (300-550) nm range with those

of the CdS-CIGS [45,46,57,58,62] and CdS-CZTS cells [47,59-61,63] employing thin CdS layers, it becomes clear that the nanowire CdS approach is substantially superior to the "thinning CdS" approach, and performance of CdS-CIGS and CdS-CZTS cells would also be further improved if nanowire CdS were to be used as a window layer in that technology.

a



b



c

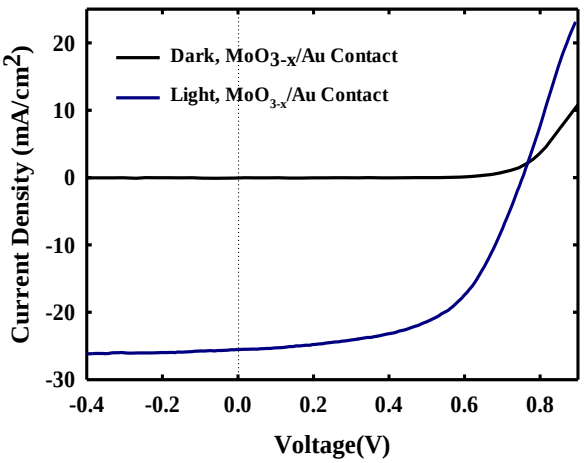


Figure 24 (a), Relative EQE of the nanowire CdS/CdTe solar cells without antireflection coating; (b), J-V characteristics of the nanowire CdS/CdTe/Cu/graphite/Silver paste solar cells, without antireflection coating under dark and 1-sun illumination. (c) J-V characteristics of the nanowire CdS/CdTe/MoO_{3-x}/Au solar cells, without antireflection coating under dark and 1-sun illumination.

4.2.5 J-V Characteristics of Nanowire CdS/CdTe Solar Cells

Figure 25b shows the J-V characteristics of one of our best nanowire CdS/CdTe solar cells, when tested under standard conditions of room temperature and 100 mW/cm^2 irradiation. The cell had an area of 0.018 cm^2, and yielded an open-circuit voltage V_{oc} of 770 mV, a short current density J_{sc} of 26 mA/cm^2, a fill factor, FF of 60%, and a power conversion efficiency (PCE) of 12%. It should be noted that the 12% efficiency value was achieved in our laboratory on an intrinsic SnO_2/ITO-soda-lime glass substrate and without antireflective coating. This is the first time that a nanowire CdS/CdTe solar cell has displayed an efficiency value higher than 10%.

The relatively high value of 26 mA/cm^2 for J_{sc} in the stack nanowire CdS-CdTe solar cell is significantly higher than J_{sc} of 21 mA/cm^2 in core-shell nanopillar CdS-CdTe solar cells [38]. Higher J_{sc} is attributed to the stack, diffused p-n nanowire solar cell configuration for transmission gain in the nanowire window layer and light absorption gain in the CdTe

absorber. It is higher than the J_{sc} of 25.88 mA/cm^2 reported in their high efficiency thin film CdS/CdTe solar cell, which employed a planar CdS with 70-80nm thickness for the window layer [32]. However, their solar cell device had two other extraneous advantages, (i) an antireflection coating and, (ii) a high quality, high cost CTO/ZTO/Corning 7059 glass substrate instead of the low cost, commercial, intrinsic SnO_2/ITO/soda lime glass substrate used in our device.

The cause of the relatively high short circuit current in our nanowire-CdS/CdTe solar cell is thought to be the enhanced optical transmission of the embedded CdS nanowire window layer and light absorption gain in the CdTe absorber, which, in turn, leads to the excellent external quantum efficiency (EQE) response of Figure 4A. Hence, our nanowire cell is not limited by the poor low wavelength response associated with the planar solar cell. Theoretical calculations show that if a high performance transparent substrate were to replace the low quality intrinsic SnO_2/ITO/soda lime glass substrates, then J_{sc} would increase by another 2.3 mA/cm^2. Thus, the photocurrent can be further enhanced readily in the future, based entirely on our current cell fabrication processes.

As of now, the 770 mV value for the V_{oc} of the nanowire solar cell device structure is notably higher than V_{oc} of 620mV in core-shell nanopillar CdS-CdTe solar cells [38]. In addition, it is higher than that of other cells (670mV-710mV) based on band gap widening in the window layer[36]. Higher V_{oc} is indeed expected because of the reduced saturation current density due to reduced interface area between CdS nanowires and CdTe as well as the higher photocurrent. Theoretical considerations indicate that these nanowire CdS/CdTe solar cells can achieve V_{oc} of about 912 mV and a resulting increase in PCE of 27.8%-30%. Currently, the V_{oc} of 770 mV in our nanowire CdS/CdTe solar

cells is only 84% of the maximum theoretical value. It is thought that the low vacuum (0.35 torr, higher than 0.02 torr used in CdS/CdTe solar cells[64]) and low deposition temperature limitations in our current fabrication facilities are responsible for introduction of a large number of defects and traps. In addition, high resistive graphite paste with 1200-2400 Ω/sql applied in back contacts negatively impacts V_{oc}, where V_{oc} was observed as 818mV before coating back contacts. The identification of the mechanisms which limit the V_{oc} of the nanowire CdS-CdTe solar cells and the finding of the pathways to further improvements will be discussed in more detail in following sections.

When MoO_3(10nm)/Au(15nm) as back contact to CdTe, the nanowire solar cells yielded V_{oc} of 753 mV, J_{sc} of 25.5 mA/cm^2, a fill factor, FF of 57.1%, series resistance of 7.72 Ω/cm^2, and a power conversion efficiency of 11%, shown in Figure 25c. Our nanowire CdS-CdTe cell design with MoO_{3-x} /Au back contacts has demonstrated the performance comparable to efficiency of 12.2%-14.1% in planar cells with MoO_{3-x} /metal back contacts[65-67].

It should be noted that the power conversion efficiency of our nanowire CdS/CdTe solar cell is the highest efficiency achieved among the nanostructured device designs in the CdS-CdTe solar cell technology(with efficiency 5.6%-6.5%). Although using nonoptimal Cu/graphite/silver pastes as back contacts, our nanowire solar cells exhibited efficiency lower than best planar CdS-CdTe solar cells reported in the literature[32], efficiency of our nanowire CdS-CdTe cell design with MoO_{3-x} /Au back contacts is comparable to efficiency of planar counterparts [65-67]. We project that the efficiency of the nanowire solar cell can be significantly enhanced in the future through further

optimization of CdS nanowire layer and the CdTe absorber layer, avoidance of high resistivity buffer layer of intrinsic SnO_2, and integration with the several conventional approaches, such as utilizing high conductivity and transparent substrates and applying low resistance back contacts.

We assess stabilization of nanowire CdS/CdTe solar cells at 120 °C thermal tests under air ambient for 240 hours. Degradation of power conversion efficiency is alleviated by approximately 3 times through inclusion of CdS nanowires as window layer (supplement information). The improvement in reliability is thought to be due to the electrically insulating property of AAO membrane and the fact that the low density of defect features of the CdS nanowires prevents deep diffusion of Cu ion into CdS nanowires and SnO_2. Recombination centers and micro shunts are significantly reduced. The nanowire CdS/CdTe structure relieves the main cell junction degradation and maintains the Cu-induced ohmic contact behavior. However, in planar CdS-CdTe solar cells, due to polycrystalline CdS with pinholes and high defects, Cu diffuses farther into SnO_2 through pinholes and defects of the planar CdS, forming deep penetration and introducing microshunts. As a result, main junction and back ohmic contact behaviour are aggravated.

4.2.6 Carrier Concentration Distribution and Interface characteristics in Nanowire CdS/CdTe Solar Cells

Carrier concentration distribution and interface characteristics are critical parameters for identifying the pathways to further enhancement in the performance of nanowire solar cells. They were measured by performing the capacitance-voltage (C-V) measurements, at the fixed, high frequency of 1MHz over a set of temperatures, 300, 275, 250, 225, 200 and 175 ^{o}k. The depletion layer width and the net space charge density profile N(x) was calculated. Figure 26a shows the C^{-2} versus voltage characteristics of the nanowire

CdS/CdTe solar cell at 300 ^{o}K and 250 ^{o}K in the dark and under sunlight illumination. These curves are not linear but can be represented approximately by two straight line tangents, one at zero bias and the other at the "strong" bias of -2.5V. Slopes of these two tangents yield the space charge density values, N_1 and N_2. Table 3 summarizes extracted net space charge density N_1 and N_2 and depletion layer widths at a set of temperatures in the 300 ^{o}K to 175 ^{o}K range.

From Figure 26a and Table 3, we observe that net space charge density is higher at large reverse bias (-2.5V) than at zero bias. N_1 and N_2 encompass the hole carrier density arising from the shallow acceptor traps near the valance band of the p-type CdTe layer, as well as the "deep" mid gap traps. Depending on the type of impurity or defect, mid gap traps can manifest as donor type trap states or as acceptor type trap states. Reduced value of N_1 in the region nearer to the heterojunction interface in the dark indicates a higher density of donor type traps and/or a lower density of acceptor type traps near the nanowire CdS/CdTe junction [68].

Also, in the dark, both N_1 and N_2 increase as the device temperature is decreased from 300 ^{o}K to 175 ^{o}K (Table 3). This is understandable because at lower temperature, less energy is available for the "deep" traps to donate and/or accept an electron; hence their effectiveness is reduced. On the other hand, even at the low temperature of 175 ^{o}K, there is enough thermal energy available for the shallow acceptor levels to accept an electron from the valance band of CdTe.

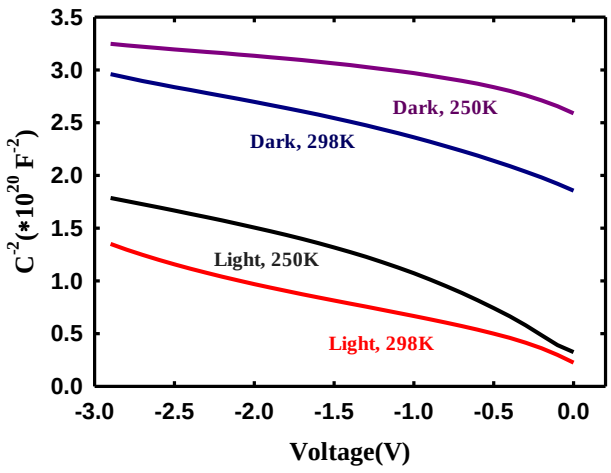
Under one-sun illumination, values of both N_1 and N_2 are smaller than their dark values. This indicates that the active deep mid gap trap in CdTe is the donor type and not the acceptor type. Under illumination, more donor type traps are able to donate electrons to

the conduction band of CdTe. This results in additional positive space charge in the midgap traps, which opposes the negative space charge in the shallow acceptor traps. The net value of space charge density (N_1 as well as N_2) is thus reduced.

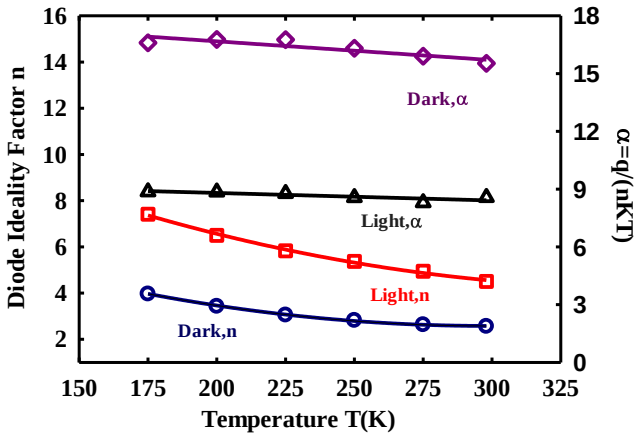
The shallow acceptor trap level in CdTe is thought to be due to ionized cadmium vacancy, VCd^- acceptor defect and chlorine center VCd^{2-}-Cl_{Te}^+ acceptor defect [69]. The deep donor type trap level, on the other hand, may be related to the doubly ionized interstitial Cu^{++}ion [68]. If this is the case for the nanowire CdS/CdTe solar cells, then the inclusion of Cu in the back contact to CdTe may be responsible for this deep trap and the $CdCl_2$ annealing treatment may be partially responsible for the shallow acceptor levels. In addition, the inter-diffusion of sulfur and tellurium across the CdS-CdTe junction is likely to be playing a role as well.

Considering that the deep donor trap is an effective recombination center, further optimization of Cu concentration at the back contact to CdTe and interface passivation to suppress donor trap density will effectively reduce J_o and enhance V_{oc} for these nanowire CdS/CdTe solar cells. This investigation, including the detailed characterization of mid gap traps is planned in our laboratory in the near future.

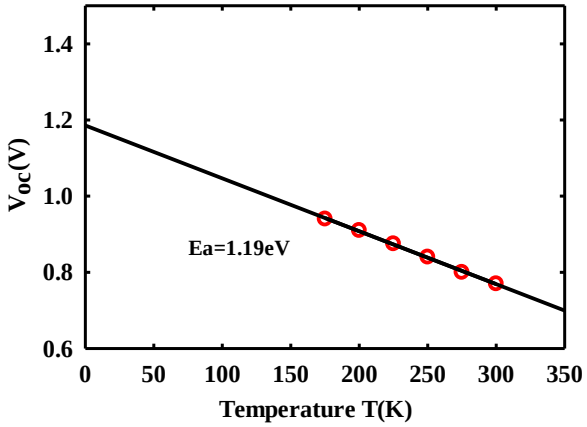
a



b



c



d

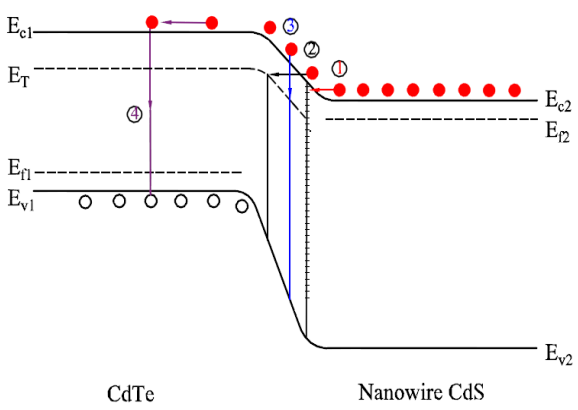


Figure 25 (a), C^{-2} versus voltage curves of the nanowire CdS/CdTe solar cell at 300 ºK and 250 ºK in dark and light; (b), Diode ideality factor (n) and α as functions of temperature in dark and under illumination; (c), Open circuit voltage as a function of temperature under one-sun illumination; (d), Four mechanisms for electron transport across the nanowire CdS-CdTe heterojunction.

Table 3 Depletion Layer Widths and Space Charge Densities of the nanowire CdS/CdTe solar cell at various temperature.

T(K)	Dark				Light			
	W_0 (μm)	$N_1(W(0))$ $*10^{15}cm^{3-3}$	$W_{-2.5V}$ (μm)	$N_2(0.8\mu m)$ $*10^{15}cm^{-3}$	W_0 (μm)	$N_1(W(0))$ $*10^{15}cm^{-3}$	$W_{-2.5V}$ (μm)	$N_2(0.8\mu m)$ $*10^{15}cm^{-3}$
300	0.69	8.54	0.85	15.3	0.24	10.1	0.54	10.33
275	0.70	8.54	0.83	23.7	0.26	7.89	0.60	12.3
250	0.81	11.2	0.90	36.0	0.29	5.17	0.65	14.3
225	0.82	11.9	0.91	36.1	0.31	4.96	0.66	15.7
200	0.83	13.3	0.92	36.8	0.35	4.51	0.69	13.6
175	0.87	15.7	0.94	42.3	0.39	5.29	0.70	12.7

4.2.7 Current Transport Processes in Nanowire CdS/CdTe Solar Cells

To gain deeper insight into the nature of electron transport across the nanowire CdS-CdTe heterojunction, and to identify the processes which limit device performance in these solar cells, I-V characteristics of a typical nanowire device were measured at different temperatures in the 300 ºK -175 ºK range. Figure 27b shows variations with temperature in the values of diode ideality factor, A and α (= q/AkT). It is interesting to note that the value of A is greater than 2, and increases from 2.56 to 3.98 and from 4.5 to 7.4 in the dark and in light, respectively, as the device temperature is reduced from 300 ºK to 175 ºK . The slope α (α= q/AkT) varies slightly with temperature, between 15.4 and 16.7 in the dark, and between 8.3 and 8.87 in the light. According to the theoretical models developed earlier[70], it is the sequence of tunneling current and the interface recombination current, which can lead to the α being independent of temperature and the

diode ideality factor (A) being in excess of 2.

Figure 26d illustrates schematically the two electron transport processes at the nanowire CdS-CdTe heterojunction. These are, (i) tunneling of electrons from n-CdS nanowires, across the narrow CdS depletion layer region to the interface states, followed by trickling down the interface states until they reach the top of the CdTe valance band and recombine with holes; and, (ii) tunneling of electrons from n-CdS nanowires, across the narrow CdS depletion layer region to the mid-gap trap levels in CdTe, followed by recombination with holes in the valance band of CdTe[54]. For illustration, the other two less dominant processes involving the diffusion of electrons from CdS followed by recombination in CdTe are also shown in Figure 26d. The latter two are less dominant because they are associated with A being less than 2. Thus, it appears that the densities of interface states and traps enable the tunneling-recombination processes over the electron transport processes of diffusion followed by bulk or space charge layer (SCL) recombination.

Temperature dependence of V_{oc} provides another valuable tool for determining the performance limit of solar cells, whereby the activation energy, E_a of the dominant recombination mechanism can be extracted through the literature[71]. Figure 26c shows a plot of V_{oc} versus T, which, when extrapolated to T=0, yields a value of 1.19 eV for E_a. The fact that this number is smaller than 1.45 eV, the energy band gap of CdTe, is another indication that, because of the non-ideal electron transport processes such as tunneling and interface recombination at the junction, the V_{oc} of nanowire CdS-CdTe solar cell remains smaller than what it can be.

Table 4 Jo and Voc of a nanowire CdS/CdTe solar cell at various temperatures.

T(K)	J_o (A/cm^2)	V_{oc} (mV)
300	$5.5*10^{-8}$	770
275	$3.8*10^{-8}$	800
250	$1.6*10^{-8}$	840
225	$3.3*10^{-9}$	875
200	$6.1*10^{-10}$	910
175	$1.3*10^{-10}$	940

Table 4 shows the variations in J_o and V_{oc} of the nanowire CdS/CdTe solar cell with decreasing temperature. When J_o decreases from $5.5*10^{-8}$A/cm^2 at 300 ^oK to $3.3*10^{-9}$A/cm^2 at 225 ^oK, the corresponding V_{oc} increases from 770 mV to 875 mV. This suggests a pathway to improve the V_{oc} in the future. Traps and interface state density needs to be reduced so that the value of J_o at room temperature can be brought down to 10^{-9}A/cm^2, and the value of V_{oc} increased to 875 mV. This can be accomplished by optimization of CdS nanowire layer and the CdTe absorber layer(high vacuum of 0.02torr), avoidance of high resistivity buffer layer of intrinsic SnO_2, and integration with the several conventional approaches, such as utilizing high conductivity and transparent substrates and applying low resistance back contacts.

4.2.8. Conclusions

In summary, we have demonstrated a stack nanowire window-absorber type solar cell structure with diffused p-n junction for overcoming low efficiency in nanostructured CdS-based solar cells, and light transmission loss and low reliability of conventional planar CdS-based solar cells. CdS nanowires embedded in AAO membrane with

occupancy rate of 32% tailor optical properties and enable light transmission gain especially from 300nm to 550nm in the window layer. Light spectrum directed into absorber layer is hence extended and light absorption loss at short wavelength is improved. A nearly ideal spectral response of quantum efficiency from 300 nm to 860 nm, the bandgap edge of CdTe, provided the evidence for improving light transmission in the window layer and enhancing carrier generation and collection in absorber. A nanowire CdS/CdTe solar cell with Cu/graphite/Silver paste as back contact, on SnO_2/ITO-soda lime glass substrates, with no additional antireflection coating, yielded power conversion efficiency of 12% under 1sun illumination, which is currently the highest efficiency in nanostructured CdS-CdTe solar cells. In addition, with MoO_{3-x} /Au back contacts, the nanowire CdS-CdTe solar cells exhibited efficiency comparable to efficiency of planar counterparts. The observed photocurrent value of 26 mA/cm^2 is substantially higher than that of core-shell nanopillar CdS-CdTe solar cells and exceeds that of reported high efficiency thin film CdS/CdTe solar cell. V_{oc} of 770 mV value is significantly higher than V_{oc} (620mV) of core-shell nanopillar CdS-CdTe solar cells, and window layer band gap widening cells (670mV-710mV). We further showed that reliability is improved by approximately 3 times through the use of embedded CdS nanowires as window layer. Interface states, deep traps and current transport are identified for further improvement in V_{oc} and efficiency. This could be done with the optimization of CdS nanowires and CdTe characteristics and interface passivation and reducing series resistance in back contacts. This nanowire window layer design offers an opportunity for other optoelectronic devices to enhance light transmission through nanostructures. The nanowire CdS-CdTe solar cell configuration can be applied for other window-absorber solar cells like CdS-CIGS and

CdS-CZTSSe solar cells to enhance their absorption and carrier generation abilities through tuning light transmission of the window layer and simultaneously obtain strong reliability benefits.

4.3 Nanowire CdS-CdTe Solar Cells with Molybdenum Oxide as Contact

4.3.1 Introduction

CdTe[32], $Cu(In,Ga)Se_2$ [45], $Cu_2ZnSn(S,Se)_4$ [13], silicon[72], and perovskites[73] are among the leading photovoltaic technologies being developed to generate low-cost solar electricity. In particular, CdTe photovoltaics have energy return investment exceeding that of traditional fossil fuels and provide the shortest energy payback time among all photovoltaic technologies for terrestrial applications[55]. In addition, CdTe photovoltaics have superior tolerance to high energy irradiation and are more suitable for space applications[24].

Development of a transparent and stable contact to the CdTe absorber layer has remained challenging and is of great interest because it can further advance the technology where CdTe solar cells are fabricated on flexible foils of metals in a superstrate device structure. The metal foil-based CdTe solar cells can be implemented by a high-throughput roll-to-roll manufacturing process, resulting in significant cost reduction, high material utilization and fabrication scalability[24]. Traditionally, CdTe solar cells on metal foils are configured with an inverted substrate structure[24,55]. However, CdTe solar cells using the substrate structure yield lower efficiency values than their superstrate counterparts[24]. The substrate structure imposes many restriction on process optimization, for example, the rather difficult etching process on the CdTe layer prior to contact formation, diffusion of impurities to the contact of CdTe, and $CdCl_2$ treatment

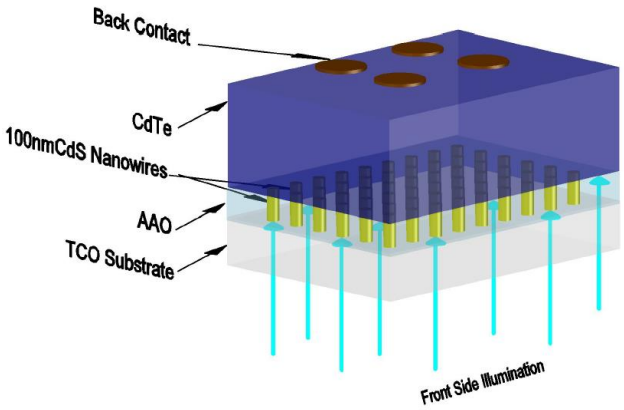
effect on CdS and CdTe layer[24,55]. Hence, formation of superstrate structured CdTe solar cells on metal foils is one of the most promising options for low cost and high efficiency photovoltaic technologies.

Recently, we have developed nanowire CdS-CdTe solar cells to address light absorption loss and reliability issues, where CdS nanowires embedded in a transparent anodic aluminum oxide (AAO) membrane replace planar CdS as the window layer and CdTe is deposited on the top of the CdS nanowires (Figure 27a)[74]. Such nanowire CdS-CdTe solar cells reduced light absorption loss in the low wavelength region, exhibited a nearly ideal spectral response of quantum efficiency from 335nm to bandgap of CdTe absorber, and simultaneously had strong reliability. By exploring a transparent back contact for CdTe film, the nanowire CdS-CdTe solar cells could allow the shining of sunlight through the back contact and thus realize the superstrate configuration (Figure27b). Because AAO is formed by anodizing aluminum, the nanowire CdS-CdTe solar cells can be grown on aluminum foil; this makes the roll-to-roll manufacturing process feasible and greatly reduces the complexity of fabrication (Figure27c).

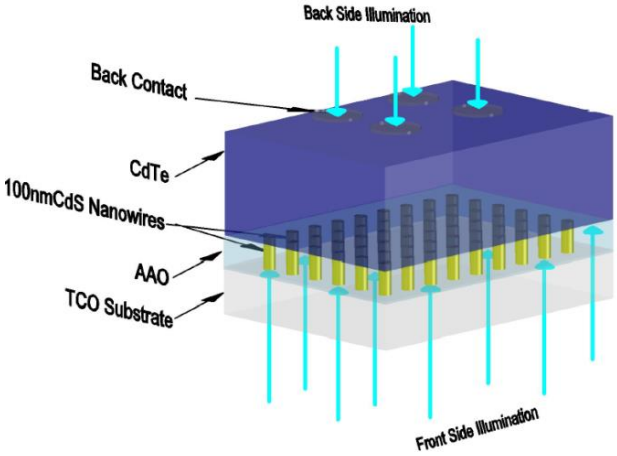
In this work, molybdenum oxide (MoO_3) is studied as a transparent back contact to the CdTe absorber layer, due to its high transparency (higher than 80%) in the visible and near IR range and its behavior like that of a high work function metal[75-77]. In addition, its electrical and optical properties can be tuned by controlling the oxygen stoichiometry during processing. Several groups have applied MoO_3/Ni and MoO_3/Au back contacts into CdS/CdTe solar cells and reported 12.2%-14.1% values for power conversion efficiency[65-67]. Here, we investigate the effects of a thin MoO_3/Au layer as the transparent back contact on the nanowire solar cells through front and back side illuminations. We

further investigate possibility of reducing resistance of MoO_3 back contacts due to its insulation property by post-processing annealing. In the following sections, the effects of the MoO_3/Au back contact layer on the structural and device properties of the nanowire CdS-CdTe solar cells are demonstrated and their loss mechanism and further improvement are discussed.

a



b



c

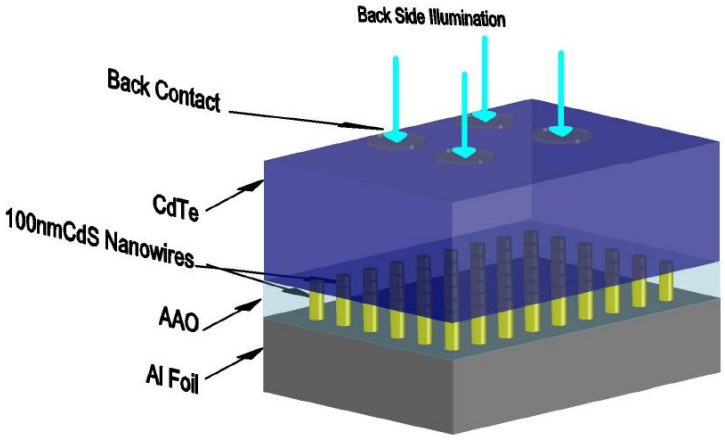


Figure 26, (a), Schematic of a CdS nanowire window layer-CdTe absorber solar cell on TCO substrate illuminated from front side. (b), Schematic of a CdS nanowire window layer-CdTe absorber solar cell on TCO substrate with almost transparent back contacts which can be illuminated from front and back side. (c), Schematic of a CdS nanowire window layer-CdTe absorber solar cell on Al foil with almost transparent back contacts which can be illuminated from back side.

4.3.2 Experimental procedures

The nanowire CdS/CdTe solar cells are prepared by our previously established methods[74]. The solar cells were fabricated on ITO coated soda-lime glass substrates with sheet resistance of 23-28Ω/square. The fabrication processes include formation of AAO membrane by anodizing aluminum film, electro-deposition of CdS nanowires with 100nm height , close-space sublimation of CdTe to a thickness of 10μm , and $CdCl_2$ treatments at 400◦C. Without NP etch, MoO_3 thin films with a thickness of 10 nm were thermally evaporated on clean CdTe surfaces from stoichiometric MoO_3 powder (Alfa Aesar, 99.9%), where the pressure was less than $1*10^{-5}$ Torr and the deposition rate was maintained as 0.5 Å/s. Samples were masked and then annealed at 200◦C in N_2 for 10 mins. In the last step, 15nm Au was deposited by sputtering process. For a comparative study, after thermal evaporation of molybdenum oxide, samples were directly coated with 15nm of Au without the intervening annealing step. After depositing Au layer, all of the

samples were annealed at 200◦C in Argon for 10mins. Structures of CdS nanowires embedded in AAO templates were characterized via scanning electron microscopy (S-900-SEM). Current–voltage (I –V) was measured by a solar simulator set at 100mW/cm^2, calibrated by a power meter.

4.3.3 Results and Discussion

4.3.3.1 SEM Characterization

CdS nanwires are characterized by scanning electron microscopy (SEM). Figure 28a shows free standing CdS nanowires where AAO membrane has been completely removed by a highly selective NaOH solution. Figure 2b shows cross-sectional view of CdS nanowires. As seen in Figure28b, CdS nanowires are embedded in AAO nanopores; some nanopores are missing their CdS nanowires; it is likely that many nanowires are knocked off from the nanopores during device fabrication and/or measurement sample preparation steps. Overall, CdS nanowires form uniform and dense arrays; values of the average length of nanowires, the average diameter and the average distance between the centers of neighboring nanowires are 100nm, 60nm and 106nm respectively. Based on the CdS nanowires features, porosity is approximately 32% and area density of CdS nanowires is calculated as approximately $1.14*10^{10}$ nanowires/cm^2. This high density CdS nanowire array was grown perpendicular to the glass-ITO substrate, but can also be directly grown on aluminum foil and other flexible substrates. These embedded CdS nanowires function as the window layer and are configured into the CdS nanowire window layer-CdTe absorber layer solar cells.

a b

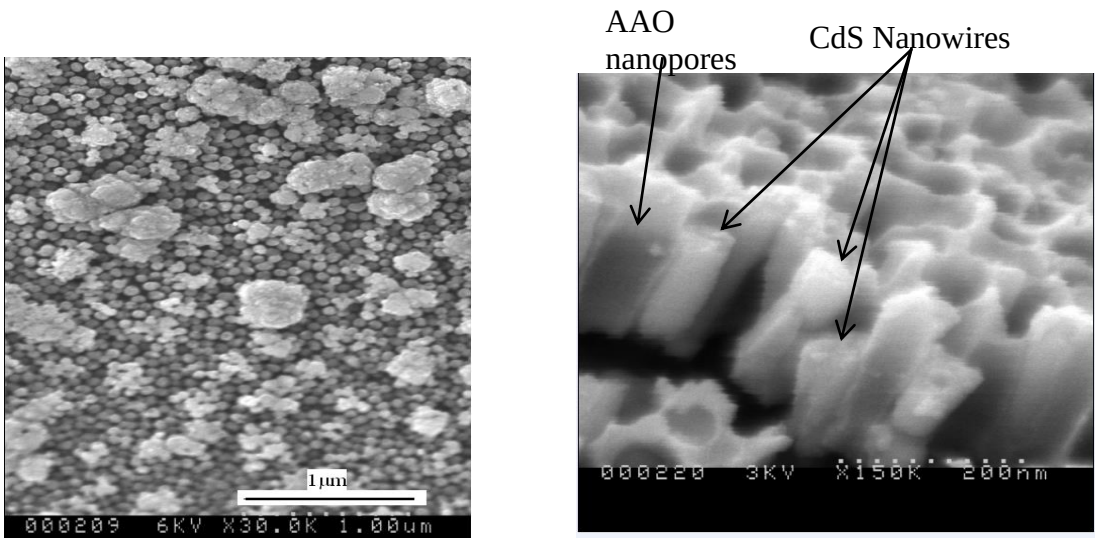


Figure 27, (a), Top view SEM image of free-standing CdS nanowires, and (b), Cross-sectional view SEM images of CdS nanowires embedded in AAO membrane.

4.3.3.2 Quantum Efficiency of the Nanowire CdS-CdTe Solar Cells

Quantum efficiency characterization is especially interesting in exploring how the CdS nanowires embedded in the AAO membrane as the window layer effectively improve light transmission and how the nanowire CdS-CdTe solar cells effectively absorb light and generate and collect carriers. The normalized external quantum efficiency (EQE) of a typical nanowire solar cell is shown in Figure29. These nanowire solar cells were fabricated on intrinsic SnO_2/commercially available ITO-soda lime glass substrate with low transparency and high resistivity.

As shown in Figure29, the nanowire CdS-CdTe solar cells exhibit relatively strong quantum efficiency response from 345nm to 845nm, which is the bandgap edge of CdTe absorber. Such EQE response indicates that a very wide spectral range of incident photons is almost completely absorbed and photogenerated carriers are effectively collected. It is clear that CdS nanowires embedded in transparent AAO membrane

effectively enhance transmission of the window layer. As a result, the wide spectrum of sunlight above 345nm can be directed into the CdTe absorber where photons are absorbed and converted into charge carriers. Thus by using the embedded CdS nanowires as the window layer, abilities of carrier generation and collection in the CdS-CdTe solar cells are effectively enhanced.

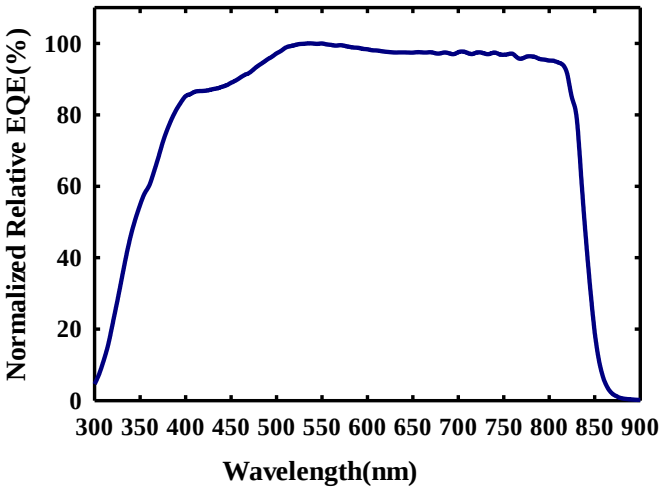


Figure 28, Normalized relative EQE of the nanowire CdS/CdTe solar cells on intrinsic SnO_2/ITO/Soda-lime glass substrate.

4.3.3.3 Photovoltaic Characteristics of Nanowire CdS-CdTe-MoO_{3-x}-Au solar cells

The performance of the nanowire CdS-CdTe solar cells with MoO3/Au back contacts was characterized. Figure 4 shows the J-V characteristics of the nanowire solar cells with MoO3/Au contacts with N2 annealing under dark, 1-Sun front side illumination and 1-Sun back side illumination, as well as the cells with MoO3/Au contacts without N2 annealing under 1-Sun front side illumination. There is no roll-over effect observed in any of the light J-V curves. Hence, incorporation of MoO3/Au as a back contact to CdTe film eliminates the commonly observed blockage to the to hole transport across the interface between the CdTe layer and the "traditional" back contact. It has been reported that MoO3 has high work function of 5.5 eV-6.86eV and has a behavior like that of a

metal[76,77]. This high work function of MoO_3 is thought to form a well-aligned buffer layer and to reduce the effective barrier height, thus facilitating the formation of quasi-ohmic back contacts to CdTe.

The optimal thickness of the MoO_3 layer is observed to be approximately 5nm-10nm, while the thickness of CdTe by closed-space sublimation is about 10μm-12 μm. Thinner MoO_3 layer, less than 5nm, is not enough to guarantee a continuous coverage and efficient contacts for hole transport due to surface roughness of CdTe. Thicker MoO_3 layer, more than 10nm, leads to decrease of short current density (J_{sc}) and fill factor (FF) due to high resistivity of the MoO_3 layer. To reduce resistance and guarantee a continuous layer, we deposited the 10nm MoO_3 layer as the buffer layer of back contacts for CdTe absorber in this work. Table 5 summarizes cell performance parameters.

The reported cell performance was achieved on intrinsic SnO_2/ITO-soda-lime glass substrates and without antireflective coating. The nanowire CdS-CdTe solar cell made without annealing MoO_3 in N_2 prior to coating with the Au back contact, yielded an open-circuit voltage, V_{oc} of 756 mV, a short current density J_{sc} of 25.1 mA/cm^2, a fill factor FF of 52.2%, and a power conversion efficiency (PCE) of 9.9%. The series resistance and shunt resistance were estimated as 9.98 Ω/cm^2 and 303.1 Ω/cm^2. As comparison, these values of V_{oc}, J_{sc} and fill factor are lower than the V_{oc} of 770mV, J_{sc} of 26 mA/cm^2 and fill factor of 60% seen in the best nanowire CdS-CdTe solar cell with Cu/graphite back contacts. Hence there is room for further optimization and performance improvement. Low shunt resistance might have been caused by contribution from the incomplete isolation of cells and less than satisfactory scribing of intrinsic SnO_2. Lower fill factor and J_{sc} are attributed to high series resistance, which is higher than the series

resistance of planar CdS-CdTe solar cells. Fully stoichiometric MoO_3 with only Mo^{6+} is insulating and has a rather high resistivity of 10^3–10^4 Ωcm [65,66]. Although J-V curves show that the incorporation of thin MoO_3 layer does not lead to the roll-over behavior , still, high resistivity attribute of MoO_3 may lead to some blockage of hole transport. This would show up as a high effective series resistance, leading to lower values fill factor and J_{sc}.

When MoO_3 is exposed to N_2 annealing before depositing Au as back contact, the performance of the nanowire solar cells is improved. The J_{sc} and fill factor are improved to 25.5 mA/cm^2 and 57.1% respectively, and the series resistance is reduced from 9.98 Ω/cm^2 to 7.72 Ω/cm^2, and shunt resistance is increased to 333.3 Ω/cm^2, leading to power conversion efficiency of approximately 11%. It has been reported earlier that after annealing in N_2, a small amount of MoO_2 as well as Mo^{4+} ions are present in the MoO_3 film, and MoO_2 is metallic[76,77]. Consequently, it is thought that after annealing at 200°C in N_2 for 10 minutes, evaporated MoO_3 film has in it the mixed oxidation states of Mo, mainly attributed to MoO_3 and MoO_2 phases[75-77]. These mixed oxidation states of Mo (MoO_{3-x}) can sustain the dominant high work function behavior arising from MoO_3 and also reduce resistivity due to metallic behavior of MoO_2 phase. Hence, series resistance of the nanowire solar cells is significantly reduced, and fill factor and power conversion efficiency are improved. An increase in J_{sc} for the annealing MoO_3 (MoO_{3-x}) back contact case is attributed to reduced barrier height due to lower resistivity of MoO_{3-x}/Au back contacts.

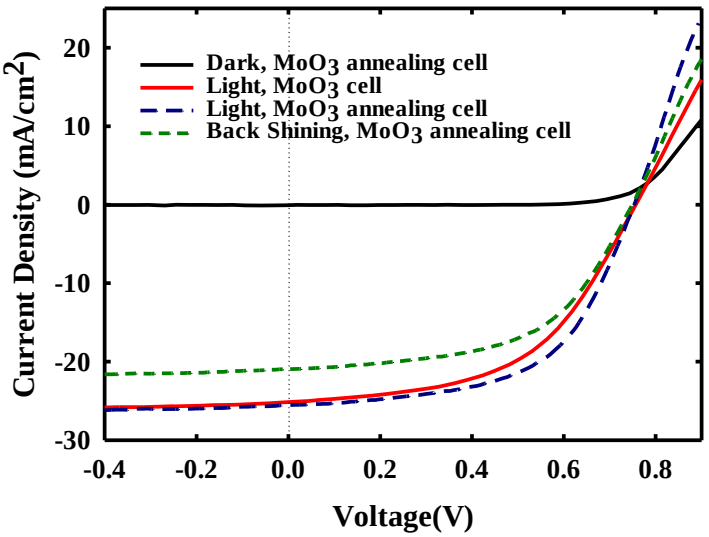


Figure 29, J-V curves of nanowire CdS-CdTe solar cells with as deposited MoO_3/Au back contacts under front side illumination, annealing MoO_3/Au back contacts under dark, front side and back side illuminations.

To illustrate the feasibility of a relatively transparent MoO_{3-x}/Au hole selective contact to p-CdTe, we illuminated the nanowire solar cells from back-contact side (MoO_{3-x}/Au side rather than SnO_2/ITO/Soda-lime glass side). The resulting J-V characteristics and the photovoltaic performance are shown in Figure 30 and Table 5. Under back side illumination, the nanowire CdS-CdTe solar cell with MoO_{3-x}/Au back contact exhibits J_{sc} of 20.9 mA/cm^2, V_{oc} of 749mV, fill factor of 55.2%, corresponding to a power conversion efficiency of 8.6%. Comparing with [15], our cells demonstrate J_{sc} comparable with J_{sc} of 21 mA/cm^2 ; however, in our case, efficiency is much higher than the 5.8% value reported for the nanopillor CdS-CdTe solar cells with Cu/Au (1 nm/13 nm) back contacts from back side illumination[38].

When comparing with front-side illumination, thicker MoO_{3-x} (10nm) and Au (15nm) are responsible for low optical transmission. Although MoO_{3-x} has bandgap of 3.0-3.8eV and high transparency of more than 80% from 400nm to near IR range, still, Au of 15nm

thickness could cause relatively strong transmission losses. Hence, obvious decrease in efficiency is on account of lower J_{sc} based on low transmission from back side illumination. By further exploring transparent back contacts of CdTe, for example, transparent metal at nanoscale in the future, the superstrate structured nanowire CdS-CdTe solar cells on Al substrate can become a low complexity and high efficiency solar technique.

Table 5 Photovoltaic properties of nanowire CdS-CdTe solar cells with MoO3/Au as back contacts.

Back Contacts	**Illumination Conditions**	**J_{sc}(mA/cm^2)**	**V_{oc} (mV)**	**FF(%)**	**Efficiency (%)**	**Rs(Ω /cm^2)**	**Rsh(Ω /cm^2)**
MoO_3/Au	Front-Side	25.1	756	52.2	9.9	9.98	303.1
MoO_3/Au annealing	Front-Side	25.5	753	57.1	10.97	7.72	333.3
MoO_3/Au annealing	Back-Side	20.9	749	55.2	8.64	10.21	346.3

Considering that MoO_{3-x} behaves like a high work function metal with a low density of states at the Fermi level and has transparent properties in the visible and near IR range[75,76], it is chosen as a transparent back contact candidate for nanowire CdS-CdTe solar cells. For a better understanding of the MoO_{3-x} back contacts, the energy band

diagram of the junction between CdTe and MoO_{3-x}/Au is illustrated in Fig. 31 below. A work function of 5.7eV and energy bandgap of 3.2eV are assumed for MoO_{3-x}, and the electron affinity of 4.4eV and energy band of 1.5 eV are assumed for CdTe[75]. Figure 31 illustrates the energy band discontinuities between CdTe and MoO_{3-x}/Au . It is noted that Au, when placed directly next to p-CdTe, would form a blocking, Schottky diode contact with a barrier height of 0.8eV. This would prevent hole transport from CdTe to Au contact and reduce cell performance. Introducing the thin MoO_{3-x} interlayer between CdTe and Au removes the Schottky diode problem. Now, a valance band offset of approximately 0.2eV occurs between the CdTe and the MoO_{3-x} layers. Thus , MoO_{3-x} layer functions as a well-aligned buffer layer to reduce barrier height relative to CdTe. Hence it plays an important role to ensure hole extraction and transport to the electrode. As a result, the nanowire CdS-CdTe solar cells yield enhanced performance. In addition, due to its transparent properties, MoO_{3-x} layer, as a back contact to CdTe provides a potency to achieve superstrate structured nanowire solar cells on flexible metal foil substrate.

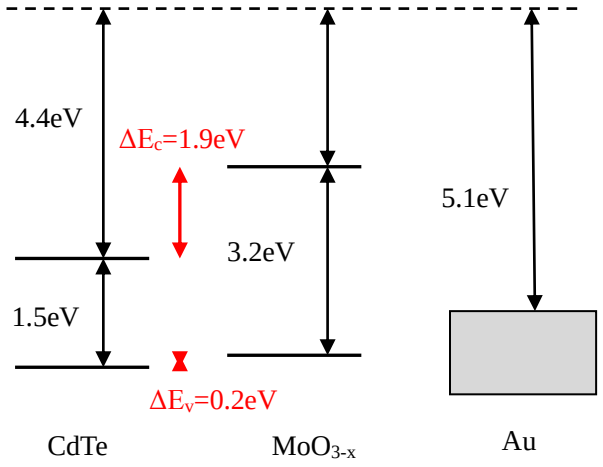


Figure 30, Band discontinuities between CdTe and MoO_{3-x}/Au back contacts.

Our nanowire CdS-CdTe cell design with MoO_{3-x} /Au back contacts has demonstrated the performance comparable to that of planar counterpart with MoO_{3-x} /metal back contacts under front side illumination[65-67]. For back side illumination, it has exhibited performance much better than that of nanopillar CdS-CdTe solar cells with Cu/Au contact[38], and its performance is comparable to that of planar CdS-CdTe solar cells with substrate structure[24,78]. It clearly illustrates the concept of MoO_{3-x} as a transparent hole selective contact to p-CdTe due to its well-aligned band structure.

Various potential improvements of our nanowire solar cell design with MoO_{3-x}/metal back contacts can be envisioned including optimization of MoO_{3-x} layer to further reduce resistance, and optimization of CdS nanowires and CdTe layer to further improve V_{oc} and J_{sc}. The FF could be improved by replacement or ideal scribing of intrinsic SnO_2 to increase shunt resistance and optimization of MoO_{3-x} layer for low series resistance. Development of a transparent metal layer on the MoO_{3-x} will improve light transmission loss and significantly enhance J_{sc} under back-side illumination. Furthermore, MoO_{3-x} with the transparent metal as the back contacts of CdTe could make the nanowire solar cells on Al foil with superstrate structure promising and facilitate a roll-to-roll fabrication process application on such solar cells, thus providing a route toward a scalable, low-cost solar cell architecture.

4.3.4 Conclusion

We have fabricated nanowire CdS-CdTe solar cells and introduced MoO_{3-x} as a transparent, low barrier back contact. The MoO_3 layer reduces the valence band offset relative to the CdTe, and creates improved cell performance. Annealing as-deposited MoO_3 in N_2 reduces series resistance from 9.98 Ω/cm^2 to 7.72 Ω/cm^2, and hence

efficiency of the nanowire solar cell is improved from 9.9% to 11%. When the nanowire solar cell is illuminated from MoO_{3-x} /Au side, it yields an efficiency of 8.7%. This reduction in efficiency is attributed to decrease in J_{sc} from 25.5mA/cm^2 to 21mA/cm^2 due to light transmission loss in the MoO_{3-x} /Au electrode. Even though these nanowire solar cells, when illuminated from back side exhibit better performance than that of nanopillar CdS-CdTe solar cells [15], further development of transparent back contacts of CdTe could enable a low-cost roll-to-roll fabrication process for the superstrate structure-nanowire solar cells on Al foil substrate.

4.4 Ambient Air-Stable Nanostructured Window Layer Solar Cells

4.4.1 Introduction

Thin film photovoltaic (PV) devices including CdS/CdTe solar cells have become promising low-cost technologies[32,79] and have reached power conversion efficiency (PCE) values higher than 20% in recent years[32,72]. It is well established that the wide terrestrial applications reinforce the need for these PV devices to deliver reliable and competitive power output over long-time in harsh environment conditions[80]. These PV devices, for example CdS/CdTe solar cells, have exhibited good reliability when they are properly encapsulated[55,81-83]; however, in general, unencapsulated cells exhibit degradation when tested under accelerated tests conditions[80,84]. It has been found that, especially for high efficiency, unencapsulated cells, device characteristics are maintained temporarily and then their performance deteriorates in humid ambient at room temperature[37,84,85]. For CdS/CdTe solar cells, one of the factors for degradation is related with back-contact reliability [37,86-89]. General approach to form back-contact of CdTe cells involves including metal, for example Cu, as a key element in the contacting process[32,80]. During the

operating life of the cell, the Cu migrates and diffuses along the grain boundary toward the main CdTe/CdS heterojunction[37,80,89]. Fill factor and efficiency or power output of the cells degrade dramatically due to deteriorating back contact and main junction[80,84]. Another factor is oxidation under ambient atmosphere condition, which hinders carrier collection due to carriers getting trapped in the oxidized sites [84].

Recently, nanostructured devices and materials have created great interest because they enable tailoring and tuning of optical and electrical properties at nanoscale[39,54,90,91]. We have developed nanowire CdS/CdTe solar cells where CdS nanowire array replaces planar CdS film as a window layer and CdTe maintains its polycrystalline structure on the top of the window layer[92]. Figure 32a and 32b illustrate the nanowire and conventional planar solar cell structures respectively. We have demonstrated that such nanowire CdS/CdTe solar cells show a nearly ideal spectral response of quantum efficiency from 335nm to 850nm. Electrical robustness of the nanowire CdS/CdTe solar cells was first noticed when these cells did not show performance reduction even after multiple annealing treatments in highly concentrated $CdCl_2$ during processing. On the other hand, the performance of the planar CdS–CdTe counterpart was significantly lower, when during processing, it was subjected to highly concentrated $CdCl_2$.annealing treatments, probably because of structural deterioration at the CdS/CdTe(S) interface during subsequent $CdCl_2$ treatments[32,93,94]. When nanowire CdS-CdTe heterojunction was stored in air for long time, without the protection of the top graphite paste electrode, their open circuit voltage showed some reduction due to surface oxidation of CdTe. However, this loss was reversible; cells could be revived by simply performing another annealing treatments in highly concentrated $CdCl_2$ ambient. This revival option was not available

in the case of the planar CdS-CdTe cells.

Further, when the NW-CdS/CdTe cells, with back contacts in place but no encapsulation, were stored in humid, room temperature conditions for one year, their performance was not noticeably decreased. However, the planar solar cells, tested under same conditions, exhibited large degradation. It appears that the nanowire solar cells have a better interface at the CdS/CdTe junction, which is more robust against environment driven degradation.

Following through on above observations, we conducted thermal tests at 120 °C ambient air for 120 and 240 hours on the nanowire CdS/CdTe solar cells coated with Cu/graphite contacts. For comparison, the same thermal tests and characterizations were performed on planar CdS/CdTe solar cells with same Cu/graphite contacts. In the following paragraphs, we present and compare stability and degradation mechanisms of these nanowire and planar CdS-CdTe solar cells. We expect through this work that such nanowire solar cell structure can be applied into other photovoltaic devices which need to provide not only good efficiency but also long-time reliability. And also it provides a design basis that traditional high resistivity buffer layer between ITO and CdS is unnecessary and a nanowire CdS-CdTe solar cell without high resistivity buffer layer is possible in order to reduce manufacturing cost.

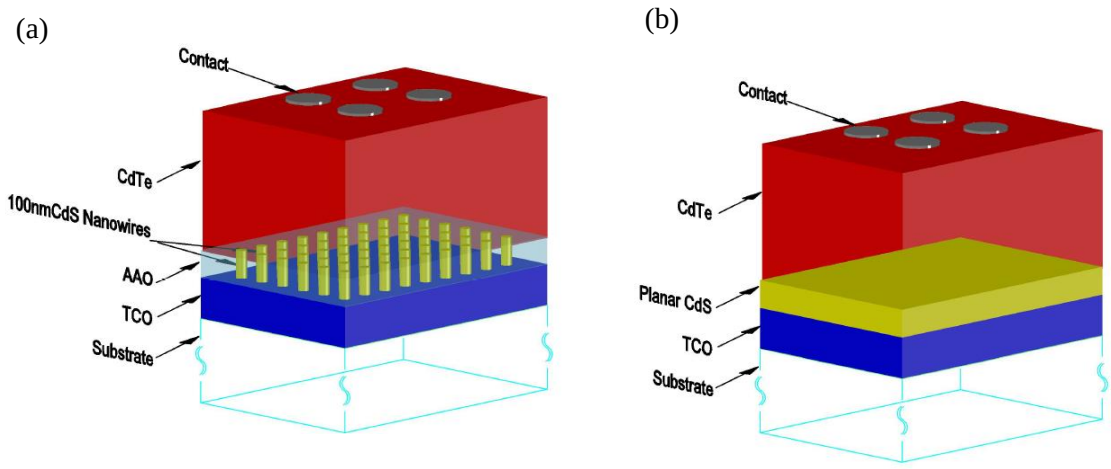


Figure 31, (a), Schematic of nanowire CdS-CdTe solar cell device structure where 100nm CdS nanowires (yellow color) embedded in absorption-negilible AAO membrane (shallow blue color) function as a nanowire window layer, and CdTe absorber is deposited on the top of the nanowire window layer. (b), Schematic of conventional planar CdS-CdTe solar cell device structure where planar CdS functions as a planar window layer and CdTe absorber is deposited on the top of the planar CdS.

4.4.2. Experiemental Details

The nanowire CdS/CdTe solar cells were prepared by the well established methods in our group[41,54]. The back-contact was formed by processes where 10nm copper was sputtered onto the back contact area and was followed by graphite paste (1200-2400 ohms/sq, PELCO Conductive Graphite, No.16058) and silver paste. Planar CdS/CdTe solar cells were prepared in same experimental conditions except that planar CdS was grown to 100nm thickness by chemical bath deposition. Substrate for both of type solar cells is intrinsic tin oxide (SnO_2) layer/ITO-coated soda-lime glass.

Reliability tests were conducted on elevated thermal tests. The thermal tests for both types of solar cells were carried out in annealing furnace where the non-encapsulated cells were kept at 120°C for 240 hours in ambient air. Current–voltage (I –V) characteristics were measured in dark and one-sun illumination, on all cells at the beginning (t=0), after 120 hours of thermal cycle and after 240 hours of thermal cycle.

4.4.3. Results and Discussion

Stabilization of the nanowire CdS/CdTe solar cells is reflected by external quantum efficiency (EQE). The cells was stored under room and humid ambient for eight and a half of (8.5) months before EQE tests. Figure 2a shows the normalized spectral response of the external quantum efficiency (EQE) of the nanowire CdS/CdTe solar cells after 8.5 months storage, which was measured by an independent group at the PV Measurements Inc.[56].

After 8.5 month storage under ambient air, EQE exhibits a nearly ideal spectral response from very low wavelength at 335nm to near bandgap of CdTe absorber at 850nm. Even though, we do not have the initial EQE, the fact that, the EQE at 8.5 months is "nearly ideal", the degradation over 8.5 months must have been rather minimal. This indicates that the nanowire solar cells have enough robustness to withstand the effects of humidity and oxidization on cell performance over a long period of time.

The maximum power conversion efficiency of the nanowire CdS/CdTe solar cells made in our group was 12% with open circuit voltage (V_{oc}) of 770mV and photocurrent density of 26mA/cm^2 at 1sun illumination. There is a room to improve the efficiency. Deposition of CdTe under 0.35 torr vacuum, high resistive graphite paste (1200-2400 ohms/sq) as back contact and inscribed SnO_2 layer negatively impact efficiency of both of the nanowire and planar solar cells. Three representative nanowire cells with initial average initial efficiency of 10.3% and three representative planar cells with average initial efficiencies of 9.75% were selected as samples for thermal tests under ambient air, where planar solar cells with lower efficiency are due to lower photocurrent. J-V data at baseline and after thermal cycle for a representative nanowire device with Cu/graphite contacts are shown in figure 33d and 33e respectively. Figure 33b and 33c show J-V data

at baseline and after thermal cycle for a representative planar device with Cu/graphite contacts for comparative illustration. Average photovoltaic values of three nanowire cells and three planar cells are extracted for performance comparison. Table 6 shows extracted average photovoltaic data of nanowire and planar solar cells under dark and 1-sun illumation after fabrication (t=0), 120 hours (t=120hrs) and 240 hours (t=240hrs) of 120°C thermal cycle.

4.4.3.1 Comparision of dark J-V characteristics of nanowire and planar Solar Cells under Thermal Cycle

As shown in Figure 33b and 33c, the planar solar cells exhibited substantial degradation in 120 hour 120°C-thermal cycle, and such degradation becomes severer in 240 hour thermal cycle. The noted feature of degradation is indicated by roll-over of the J-V curves of the planar solar cells in thermal cycle. A stronger roll-over appears in J-V curves under 240 hour thermal cycle, suggesting that long-time thermal cycle under air has dual effects on accelerated degradation of the planar solar cells. The roll-over in J-V characteristic is associated with the interface between the CdTe absorber layer and the back contact. Oxidation and moisture can degrade this interface to the extent that the contact junction takes on the characteristics of an M-I-S device and is no longer a straightforward conducting contact[95].

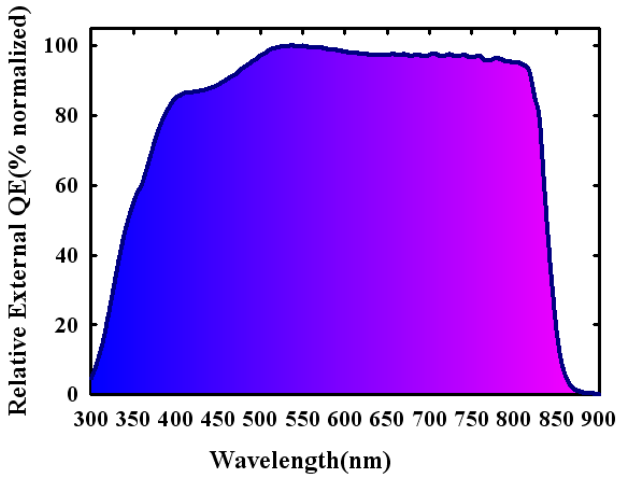
As for the CdS-CdTe junction, we observe, from Table 6, that the extracted average diode ideality factor (A) is 2.43 after fabrication, and its value is increased to 2.99 and 4.15 at 120 and 240 hour thermal cycle respectively. The degradation is estimated as 23% at 120 hour thermal cycle and 70.8% at 240 hour thermal cycle. The average reverse saturation current density (J_o) increases from $5.35*10^{-8}A/cm^2$ at t=0 (baseline) to

$5.99*10^{-7}$ A/cm^2 at 120 hour thermal cycle, and further deteriorates to $1.97*10^{-6}$ A/cm^2 at 240 hour thermal cycle. The thermal cycle in air atmosphere causes degradation of reverse saturation current density J_o by 10.2 times and 35.8 times for 120 and 240 hours respectively. The J_o and A represent junction performance; hence increased value of J_o and A indicate junction deterioration of the planar solar cells during long time thermal cycle. It is noted that degradation under air occurs nonlinearly, revealing that the planar solar cells can provide a substantial reliability, for example 120 hours, to suppress detrimental effects of heat and air (H_2/O_2), and the longer time thermal cycle causes accelerated deterioration.

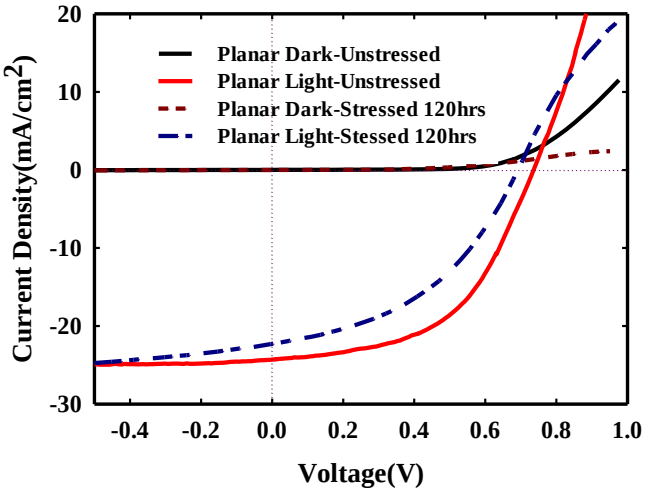
As shown in Figure 33d and 33e, there is no roll-over occurring in the J-V curve of the nanowire solar cells at 120 and 240 hour thermal cycle, suggesting less degradation and no apparent barrier to carrier transport at the interface between CdTe and the back contact. The thermal cycle causes diode ideality factor (A) to be degraded only 5.8% and 13.7%, and average value of A varies from 2.41 at baseline to 2.55 after 120 hour cycle and to 2.74 after 240 hour cycle. Corresponding reverse saturation current density (J_o) degraded by 0.27 and 0.89 times, and its average value increases from $5.15*10^{-8}$A/cm^2 at baseline to $6.56*10^{-8}$ A/cm^2 at 120 hour cycle and to $9.72*10^{-8}$ A/cm^2 at 240 hour cycle. Compared with degradation of A and J_o of the planar solar cells, A is improved by approximately 3.9 times and 5.1 times, and J_o is significantly improved at 120 and 240 hour cycle. The nanowire solar cells show a relatively slow degradation and favorable junction stabilization against heat and H_2/O_2. These better diode ideality factors illustrate that although the nanowire solar cells is coated with Cu/graphite as back contacts, its device configuration has features, which retard the degradation of main CdS-CdTe

junction and back electrode-CdTe contact junction.

(a)

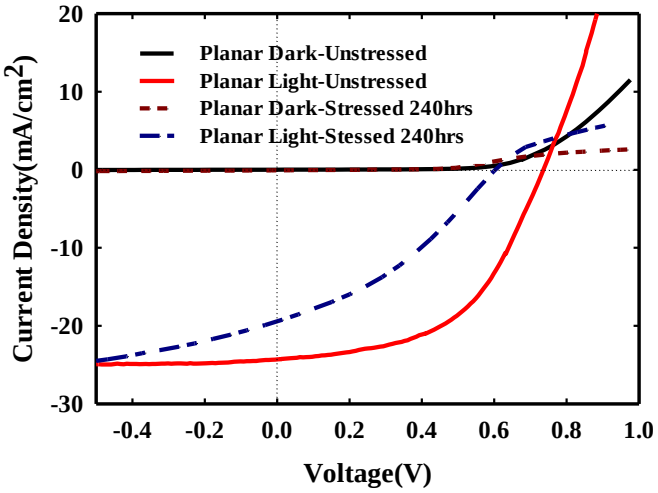


(b)

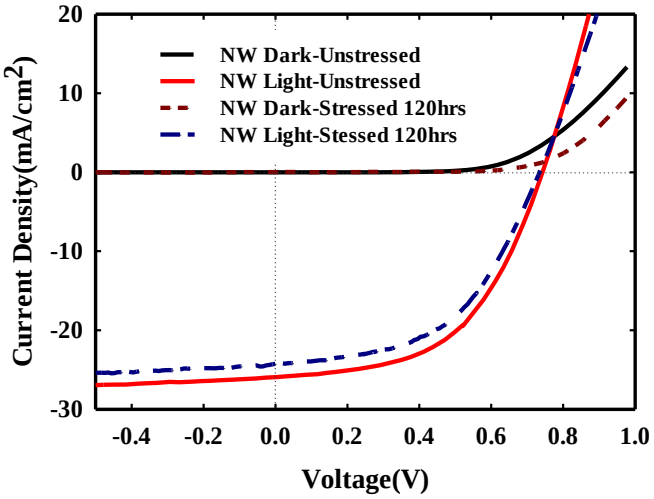


(c)

(b)


Planar Dark-Unstressed
Planar Light-Unstressed
Planar Dark-Stressed 240hrs
Planar Light-Stessed 240hrs
Current Density(mA/cm2)
Voltage(V)
20
10
0
-10
-20
-30
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
1.0

(d)


NW Dark-Unstressed
NW Light-Unstressed
NW Dark-Stressed 120hrs
NW Light-Stessed 120hrs
Current Density(mA/cm2)
Voltage(V)
20
10
0
-10
-20
-30
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
1.0

(e)

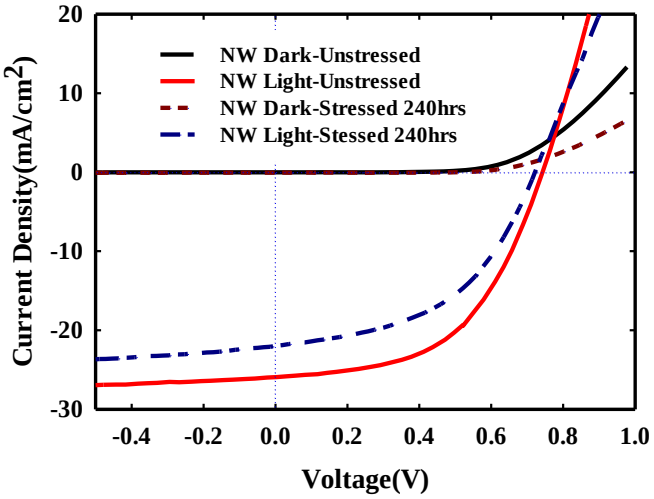


Figure 32 (a), Relative EQE of the nanowire CdS/CdTe solar cell with intrinsic SnO_2/ITO/soda lime glass substrate; (b) Dark and light J-V curves of planar solar cells with Cu/graphite back contacts after fabrication and b)120 hour thermal cycle, and (c) 240 hour thermal cycle; Dark and light J-V curves of nanowire solar cells with Cu/graphite back contacts after fabrication and (d) 120 hour thermal cycle, and (e) 240 hour thermal cycle.

4.4.3.2 Comparision of light J-V characteristics of nanowire and planar solar cells

As shown in table 6 and light J-V curves, degradation of the planar solar cells appears in large reductions in V_{oc}, J_{sc} and shunt resistance and increase in series resistance. It is observed that series resistance drastically increases from 6.47Ω/cm^2 to 24.35 Ω/cm^2 (120 hour cycle) and then to 97.15 Ω/cm^2 (240 hour cycle); thus it increased by 2.7 time and 14 times respectively. Significant degradation also occurs in shunt resistance. It value is estimated as 272.5Ω/cm^2 after fabrication to 161 Ω/cm^2 (120 hour thermal cycle) and then to 73.5 Ω/cm^2 (240 hour thermal cycle), resulting in degradation of 41% (120 hour thermal cycle) and 73% (240 hour thermal cycle). It is considered that drastic increase in series resistance is indicative of back contact degradation [1,20] and is responsible for decrease of J_{sc} from 24.46mA/cm^2 at baseline to 22.2 mA/cm^2 (decreased by 9%) at 120 hour thermal cycle and then to 18.9mA/cm^2 (decreased by 22.7%) at 240 hour thermal cycle. Shunt resistance reduction is a characteristic of the main junction degradation,

which causes drop of V_{oc} by 6.9% (from 741.5mV to 690mV) and by 19% (from 741.5mV to 600mV) at 120 and 240 hour thermal cycle respectively. For the planar solar cells, it is the back contact and main junction degradation that causes efficiency drop by 27.15% and 54.15% respectively during 120 and 240 hour accelerated thermal cycling testing.

Replacing planar CdS with CdS nanowires as the window layer, the solar cells exhibited improved reliability performance against thermal cycle and humidity. After 120 and 240 hour thermal cycle, V_{oc} is slightly decreased by 1.2% (from 743mV to 734mV) and 2.7% (from 743mV to 723mV), J_{sc} yields 6.4% (from 25.7mA/cm^2 to 24.05mA/cm^2) and 14.4% (from 25.7mA/cm^2 to 22mA/cm^2) drops; and efficiency is decreased by 8.75% and 24.3%. Compared with degradation of the planar solar cells, after 120 and 240 hour thermal cycle, the nanowire solar cells improve reliability of V_{oc} by approximately 5.7 times and 7 times; J_{sc} by approximately 1.4 times and 1.6 times; and efficiency by approximately 3.1 times and 2.2 times. Stabilized V_{oc} is an evidence of good junction behavior under thermal cycle and humidity. Decrease of fill factor and efficiency is primarily caused by drop in J_{sc}. Hence, it is thought that there is a barrier for carrier transport at back contact interface under thermal cycle. It is the back contact degradation rather than the main junction degradation that mainly impacts the reliability of the nanowire solar cells. Thus, the nanowire solar cells have a mechanism to protect the main junction from detrimental effects of humidity and thermal cycle.

These observations are in agreement with our finding that after cells are stored in room ambient for one year, the planar solar cells exhibited the strongest reduction in V_{oc}, J_{sc}, FF and the increase in series resistance. However, there is little deterioration in the J-V

characteristics of the nanowire solar cells after one year storage. The nanowire solar cells can withstand high concentration $CdCl_2$ annealing treatments for multiple times and exhibit good photovoltaic performance. However, after a strong $CdCl_2$ treatment, the performance of the planar solar cells demonstrated irreversible deterioration effect. These agree well the results of the thermal cycle test that the nanowire solar cells have a solid and robust junction and interface to prevent degradation.

It should be noted that our results regarding the improvement in aging by a factor of 3 are applicable only to those planar CdS-CdTe devices, which use copper in the back electrode and are not encapsulated. Also, when using Cu:ZnTe as back contact and applying thermal cycle to the encapsulated cells, degradation of cell performance in planar CdS devices is expected to be lesser than seen in our unencapsulated devices. Still, due to the nanostructure features of the AAO and the CdS, the nanowire CdS-CdTe devices are, overall, more robust and alleviate thermal and humidity detrimental effects.

Table 6 Comparison of average photovoltaic properties in nanowire and planar CdS /CdTe solar cells under thermal thermal cycle.

Device	A	J_0(A/cm^2)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF(%)	Efficiency (%)	Rs (Ω /cm^2)	Shunt Resistance (Ω /cm^2)	Efficiency Degradation (%)
Planar graphite/ Baseline	2.43±0.04	$5.35*10^{-8}$±$0.55*10^{-8}$	24.46±2.4	741.5±3.5	53.8±1.1	9.75±0.35	6.47±0.16	272.5±3.5	
Planar graphite/ thermal cycle (120hrs)	2.99±0.1	$5.99*10^{-7}$±$1.77*10^{-7}$	22.2±0.2	690±5	46.3±1.9	7.1±0.4	24.35±0.75	161±11	27.15±1.45
Planar graphite/ thermal test (240hrs)	4.15±0.26	$1.97*10^{-6}$±$0.96*10^{-6}$	18.9±0.4	600±10	39.4±1.4	4.45±0.35	97.15±5.45	73.5±9.5	54.15±1.65

NWgraphite/ baseline	2.41±0.03	$5.15*10^{-8}\pm0.45*10^{-8}$	25.7±0.1	743±5	53.9±1.2	10.3±0.3	6.22±0.35	274±9	
NWgraphite/ thermal cycle (120hrs)	2.55±0.06	$6.56*10^{-8}\pm0.34*10^{-8}$	24.05±0.15	734±5	53.1±1.3	9.4±0.3	7.94±0.5	248±12.4	8.75±0.25
NWgraphite/ thermal cycle (240hrs)	2.74±0.09	$9.72*10^{-8}\pm1.78*10^{-8}$	22.0±0.6	723±5	48.55±0.45	7.8±0.3	10.73±0.55	211.5±8.5	24.3±0.7

4.4.3.3 Stablization mechanics of nanowire solar cells

Cu is a common element among the back contact technologies for making conducting contact to p-CdTe absorber layer. These technologies include, HgTe:CuTe-doped graphite paste, Cu-doped ZnTe,Cu_xTe and Au/Cu. Copper is known to improve contact properties and carrier concentration at the back surface of CdTe. In our work, back contact is achieved by vapor deposition of 10nm thickness Cu on approximately 10μm thick CdTe layer and subsequent graphite past brushing and annealing at 150°C. Analysis of J-V characteristics in the planar solar cells demonstrates that there are at least two mechanisms responsible for severe degradation under thermal cycle. The formation of J-V rollover and significant increase of series resistance is the result of back contact degradation. At 120°C air thermal cycle, oxygen can migrate through the back contact and form oxidation on the CdTe surface. The oxidation layer traps carriers and decreases hole transport from CdTe to electrode, resulting in a back-contact Schottky barrier[95]. Depletion of Cu at the back contact/CdTe interface is another major factor, which is responsible for back contact degradation. Cu is considered as a fast diffuser[89]. For 120 hour thermal cycle at 120°C air atmosphere, obvious increase of series resistance and moderate degradation of shunt resistance suggest that thermal cycle for 120 hours has facilitated Cu in the back contact to diffuse into the polycrystalline CdTe film along grain boundaries[87], and accumulate in the CdS. When Cu is diffused into the CdTe, hole density and carrier lifetime in CdTe are decreased because Cu occupies the interstitial positions and forms compensating donor defects[37,89]. After Cu diffuses away from the back contact, the back contact becomes a Cu-depleted rectifying contacts[89]. This rectifying back contact is thought to be the cause of observed rollover in the J-V characteristics of the planar solar cell after the 120 hour thermal cycle. Accumulation of

Cu in the CdS can create acceptor states[84], however at initial 120 hour thermal cycle, such Cu acceptor concentration is much less than electron concentration of approximately $10^{18}/cm^3$ in n-CdS, thus Cu accumulation in CdS could not lead to detrimental effects on junction stability. As a result, series resistance and J_{sc} are obviously degraded, however V_{oc} and shunt resistance are maintained relatively stable. Longer thermal cycle leads to excessive Cu quantities in CdS. Excessive Cu doping of CdS could create acceptor states and recombination centers which are compared with effective donor concentration of CdS. Furthermore, because the planar CdS is composed of polycrystalline CdS with pinholes, Cu accumulated in CdS film diffuses farther into SnO_2 through pinholes of the planar CdS, forming deep penetration and introducing microshunts. As a result, main junction is aggravated. Because of this degradation, all photovoltaic parameters, A, J_o, V_{oc}, J_{sc}, FF, and efficiency are negatively affected.

Unlike the case of the planar solar cells, the nanowire solar cells do not exhibit the roll-over in their J-V characteristics even after the 240 hour thermal cycle. Similarly, in the nanowire solar cells, it is relatively easy that Cu diffuses from the back contact into CdTe film along CdTe grain boundaries under thermal thermal cycle. However, continuous diffusion of Cu is dramatically impeded due to structure and features of the nanowire window layer. The nanowire window layer is formed by CdS nanowires embedded in AAO membrane. The AAO membrane is typically crystalline, insulating and thermodynamically stable, and occupies 68% area of the SnO_2/ITO substrate[54]. Cu ions seek low resistive locations to migrate to; hence it is unlikely that Cu would find its way to the surface of the AAO membrane, for the purpose of diffusing. Thus, continuous diffusion of Cu is prevented by AAO/CdTe interface. Moreover, CdS nanowires are

ordered-aligned crystalline structures with low defects, dramatically avoiding pinhole defects, which exist in the planar CdS[32]. Such low defect and ordered structure of the CdS nanowires effectively suppress diffusion of Cu into CdS nanowires, and there is very low probability that Cu ion can further migrate into SnO_2 through the CdS nanowires. Consequently, recombination centers in CdS and microshunts are significantly reduced. The nanowire CdS/CdTe structure alleviates degradation of the main cell junction, which agrees well with stabilized value of V_{oc} and shunt resistance after 240 hour thermal cycle. The nanowire window layer prevents deep diffusion of copper. In other words, it maintains the Cu-induced conducting contact between CdTe and graphite, and greatly reduces the back contact barrier and roll-over characteristics of the J-V curve.

Note that the diffusion of Cu in CdTe film over long time or under thermal cycle conditions leads to more compensating donor defects and reduced hole density, which cause a reduction in $J_{sc.}$ of the nanowire solar cells. Another factor that can degrade I-V characteristics is the oxidation caused by the thermal cycle of high temperature in the air ambient. This oxidation layer is commonly the dominant factor in the increase of series resistance and back contact degradation. Degradation of series resistance and J_{sc} is responsible for drops in fill factor and efficiency for the nanowire solar cells.

Generally, a planar window layer thinning approach is used to reduce the absorption loss in the planar CdS window layer. Pinholes in the planar CdS and substrate roughness exacerbate shunting and negatively influence open circuit voltage. It is necessary that an additional high resistivity buffer layer is deposited between the TCO and the CdS window layer[32] in order to reduce shunting issues due to pinholes of the planar CdS. Earlier, we demonstrated that the nanowire CdS/CdTe solar cells reduced absorption loss

in the window layer and enable a nearly ideal spectral response of quantum efficiency, indicating effective light absorption and carrier collection. In this work, we further revealed the nanowire solar cells enable long-term performance to be effectively improved and can potentially deliver reliable power output against harsh operation environment. Hence the traditional high resistivity buffer layer between ITO and CdS is likely to be unnecessary. This would lead to reduced manufacturing costs as well as reduced series resistance for the solar cell. The reliability investigation provides a basis to design a nanowire CdS/CdTe solar cell without high resistivity buffer layer.

The nanowire solar cell structure offers an opportunity to not only yield high efficiency but also deliver reliable power. It is expected that such nanowire solar cell structure can be applied into other type of solar cells, including organic-inorganic mixed solar cells, which need to improve carrier generation and collection, and simultaneously address reliability issues.

4.4.3.4. CONCLUSION

Thermal cycle induced degradation of nanowire solar cells and planar cells kept at 120 °C ambient air for 120 and 240 hours was measured, compared and analyzed. Power conversion efficiency of the planar solar cells decreased by 27.15% and 54.15% respectively. Corresponding efficiency of the nanowire solar cells is reduced by 8.75% and 24.3% respectively after 120 and 240 hour thermal cycle. It was demonstrated that the nanowire solar cells exhibit degradation of power conversion efficiency, which is approximately 3 times smaller than the degradation in the planar solar cells. The enhanced performance in nanowire solar cells is thought to be due to the electrically insulating property of the AAO membrane and the low defect features in the CdS

nanowires; these prevent the deep diffusion of Cu ions into the CdS nanowires and then into SnO_2. Further, because of reduced copper diffusion, recombination centers and microshunts are significantly reduced. Thus, nanowire CdS/CdTe structure reduces the degradation of the main CdS/CdTe junction and also maintains the Cu-induced conducting contact behavior at the back contact between the Cu-graphite electrode and the CdTe absorber layer. High reliability of the nanowire solar cells suggests that traditional high resistivity buffer layer between ITO and CdS is unnecessary and a nanowire CdS-CdTe solar cell without high resistivity buffer layer is possible in order to reduce manufacturing cost. The nanowire solar cell structure offers an opportunity to achieve effective carrier generation and collection and hence high quantum efficiency, but also simultaneously address reliability issues. These concepts for improving efficiency and reducing degradation with time are applicable to other types of solar cells, including organic semiconductors cells and mixed inorganic-organic solar cells.

4.5 Nanotube Photovoltaic Configuration for Enhancement of Carrier Generation and Collection

4.5.1 Introduction

The increasing demand for energy and its environmental impact led to renewed efforts and novel approaches to develop cost-effective photovoltaics. Recently, development of nanostructured devices and materials has created a new paradigm for reducing cost and improving power conversion efficiency of photovoltaic device.[43,96,97] Solar cells have been benefited from structures in multiple dimensions on nanoscale.[43,96-101] Nanowires, nanorods and nanoparticles have been extensively used to reduce volume of semiconductor materials, enable beneficial optical management and novel conversion

mechanisms in polymer-based and silicon solar cells.[43,96-107] A few was concentrated on CdS nanopillar- and CdS nanowire-based photovoltaics,[38,39,108] and power conversion efficiency are lower than 10%, which is difficult to compared with corresponding planar solar cells.

Power conversion efficiency depends on effective light absorption and efficient photo-carrier generation and collection. In this regard, we designed a three-dimensional (3D) nanotube solar cell structure where a n- or p-type semiconductor material (semiconductor-1 or S-1) is formed in the shape of nanotubes (yellow color in Figure 1A), and a second, p- or n-type semiconductor material (semiconductor-2 or S-2) is deposited inside the inner walls of nanotubes and is also made to wrap around the outer wall of the nanotubes (purple color in Figure 1A). The S-2 can be continuously deposited on the top of S-1. We developed a low-cost, anodic aluminum oxide (AAO) membrane-assisted method to efficiently grow geometric feature tuned nanotubes. Utilization of AAO membrane-assisted methods is because AAO membrane possesses highly ordered and controlled nanoporous structure, and absorption-negligible, electrical insulating and thermodynamically stable properties.[50,109,110] In addition, we have found in our group that the nanostructures embedded in AAO membrane exhibited strong reliability to restrain performance degradation in harsh environment. Therefore, it becomes a low cost and reliable method for growing nanostructures for photovoltaic applications. AAO membrane has been widely applied into growth of nanostructures, usually nanowires since 1990s.[38,39,50-52,54,90,110,111] Development of nanopillar–array photovoltaics promoted application of the AAO membrane-assisted vapour–liquid–solid growth method into CdS nanowires.[38] However, growth of nanotubes through AAO membrane-assisted methods

was primarily focused on carbon nanotubes,[112-114] and few reports were concentrated on growth of CdS nanotubes.[115] Previous studies have not yet applied these nanotubes for 3D solar cell structure.

In this work, we report on 3D nanotube solar cells for enhancing carrier generation and collection, and make nanotube CdS-CdTe solar cell as an example. Figure 34c shows visual images of the fabrication process flow of the nanotube CdS/CdTe solar cells. The CdS nanotubes are grown by electrodeposition inside the ordered nanopores of AAO membrane. After removing AAO membrane and forming free-standing CdS nanotubes, the CdTe absorber is not only grown in the inner core of nanotubes but also replaces the membrane and is filled in the intertube space, which surrounds the outer walls of nanotubes (Figure 34a and 34c). Such 3D nanotube solar cell configuration can improve photocarrier generation and collection by generating and separating photocarriers in 3D directions. Specifically, photocarriers can be generated and transported in the inner core space of nanotubes and in the intertube space between nanotubes along radial direction, and also be generated and transported above the nanotubes along the axial direction (Figure 34b). This type of structure is particularly advantageous for those absorbers or sensitizers with short minority carrier lifetime. Because nanotubes with inner diameter and intertube space at nanometer scale can facilitate carrier to be effectively collected before recombination, the 3D nanotube solar cells can relax the long minority carrier collection length required by conventional absorbers.

For CdS-CdTe solar cells, because CdS functions as a window layer and CdTe functions as an ideal absorber material, we develop 200nm-long CdS nanotubes to reduce light absorption loss in the CdS window layer. It should be noted that length of nanotubes

can be readily varied (see Methods section) for various types of solar cell applications. In the following paragraphs, we present materials and electro-optical characterizations and the charge transport processes in the nanotube CdS-CdTe solar cells. By investigation of photovoltaic performance of the nanotube CdS-CdTe solar cells in this work, we expect that such nanotube solar cell structure will be applied into organic-inorganic solar cells, for example, CdS-CuPC solar cells and those solar cells with short minority carrier lifetime.

4.5.2 Experimental Section

Formation of AAO membrane. Nanotube-CdS/CdTe solar cells were prepared on ITO/soda-lime glass substrates through process steps: AAO membrane formation, CdS nanotube growth, CdTe deposition, and back contact formation. First, a 100nm thick intrinsic tin oxide (SnO_2) layer and a 5nm thick titanium layer were RF sputtered onto cleaned ITO-coated glass substrates with sheet resistance of 23-28 Ω/square. A 200nm thick aluminum (Al) layer was then deposited by electron beam evaporation. The Al film was anodized in a 0.3 M oxalic acid solution under 60 V bias and at approximately 5 □C until Al was completely anodized into anodized aluminum oxide (AAO). The as-anodized AAO membrane was etched with a 5% phosphoric acid solution for 40minutes and then subjected to a reactive ion etch (RIE) treatment for 2minutes, resulting in an absorption-negligible AAO membrane. These solar cells can thus be illuminated through transparent AAO/SnO_2/ITO glass substrates, greatly reducing light transmission loss.

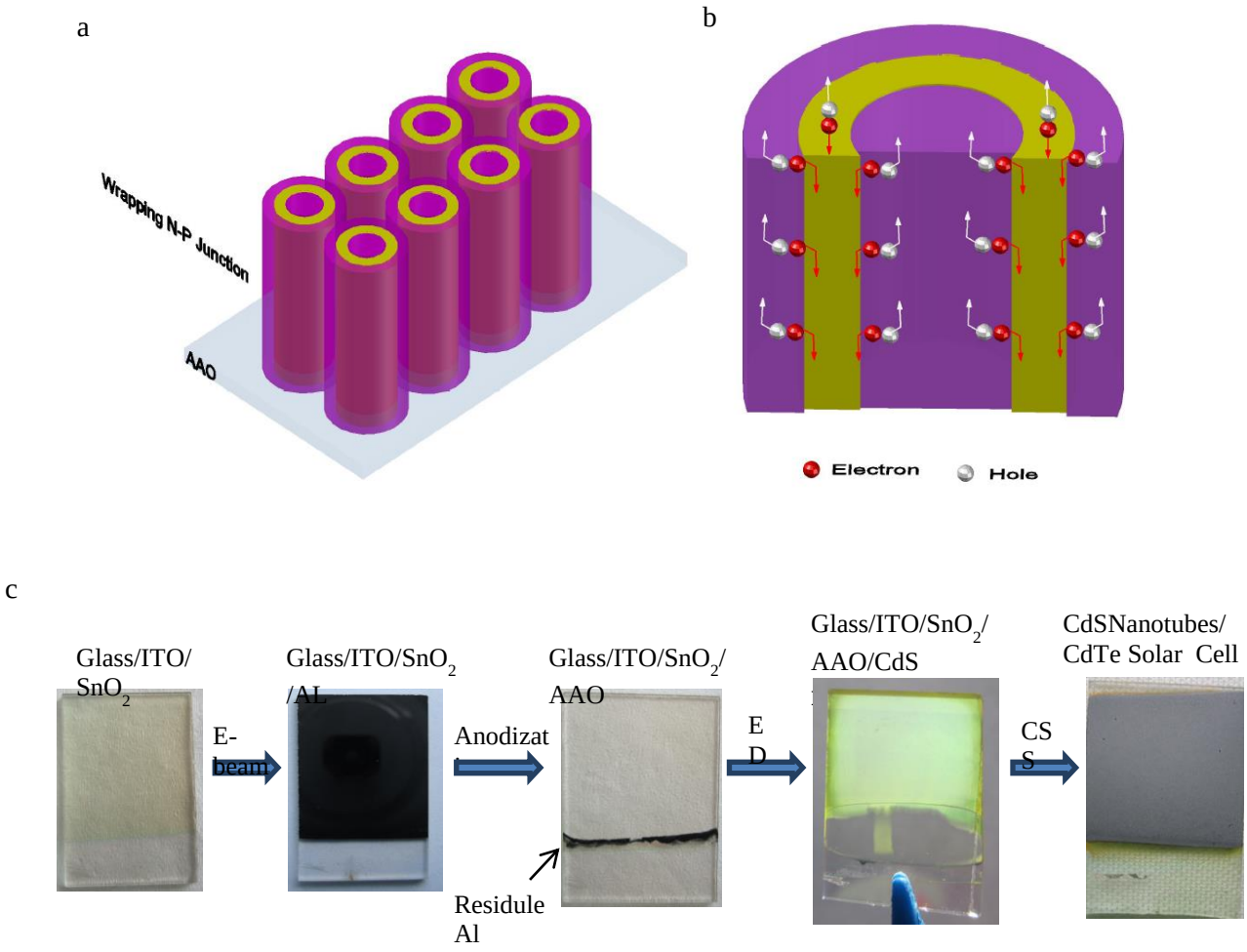


Figure 33, (a), Schematic of three-dimensional nanotube solar cell device structure where a n-or p--type semiconductor material (S-1) is formed as nanotubes (yellow color), and absorbers or sensitizers is deposited inside the nanotubes (purple color) and are wrapped around the outer wall of nanotubes (purple color). (b), Photocarriers are generated and transported in the inner core and in the intertube space between nanotubes along radial direction, and above the nanotubes along axial direction. (c) Visual images of fabrication steps for a 3D nanotube CdS-CdTe solar cell, including aluminum deposited on the top of a substrate; formation of absorption-negligible nanoporous AAO membrane; CdS nanotubes filled in the nanopores of AAO membrane by electro-deposition; partially exposed CdS nanotubes and CdTe absorber deposited in the inside of the CdS nanotubes, in the intertube space between CdS nanotubes and on the top of embedded CdS nanotubes.

Growth of CdS Nanotubes. For growth of the CdS nanotubes, 0.042M cadmium chloride ($CdCl_2$) and 0.2M elemental sulfur solution in 50mL dimethyl-sulfoxide (DMSO)

were used as precursors. The growth of the CdS nanotubes depends on concentration of $CdCl_2$, dc current density and deposition temperature. We found that the CdS nanotubes can be optimally formed at lower concentration of $CdCl_2$, lower dc current density of $2mA/cm^2$ and deposition temperature of 100°C, with the growth time maintained at 20s. The growth mechanism of the CdS nanotubes will be discussed in the following paragraphs. After the formation of CdS nanotubes , the samples were soaked in a 75% $CdCl_2$ solution for 15 minutes, and were subjected to an annealing treatment for 30 minutes at 400℃ under 100-sccm Argon flow.

Fabrication of CdTe Absorber.The samples were then placed in a 0.1M NaOH solution for 10mins to partially remove AAO membrane and expose 170nm height of CdS nanotubes, while the rest of the CdS nanotubes (30nm) remained embedded in the AAO membrane. Next, before the deposition of CdTe, the CdS nanotubes were dipped in a 0.1M HCl solution for 5s to clean the surface. CdTe was deposited in a closed-space sublimation system, where the CdTe source and the nanotube CdS substrate substrate were first heated to the relatively low temperatures of 470◦C and 100 ◦C respectively. They were kept at those temperatures for 1 minute. Then, source and substrate were ramped together to a common temperature of 575 ◦C. Next, source temperature alone was increased to 635◦C and maintained there for 30 seconds under the flow of 15 torr He (with 5% O_2 background gas). Thus CdTe got deposited in the inner cores of CdS nanotubes, in the intertube space between the CdS nanotubes and on top of the nanotube CdS substrate. After CdTe deposition, the nanotube solar cells were immersed in a 75% $CdCl_2$ methanol solution for 30 minutes and then annealed at 400 ◦C for 30minutes under the flow of 100-sccm Argon.

Formation of Back Contact. The solar cells were then etched in a mixture solution (1:88:35) of nitric and phosphoric acid for 35s. This etch is known to make the CdTe surface rich in tellurium (Te+), which in turn facilitates the formation of a a pseudo-ohmic contact between the graphite paste and the p-CdTe. Next, to further facilitate the pseudo-ohmic contact formation, a 5 nm thick copper layer was sputtered onto the back contact areas. Then contact layers of graphite paste (PELCO Colloidal Graphite, 16051, TED PELLA, INC.) and silver paste were applied with a brush. Finally, cells were annealed at 150 ◦C for 10 minutes to cure the graphite/silver paste. Thus finished 3D nanotube CdS-CdTe solar cells were obtained.

Materials and device characterization. Material characterization of the CdS nanotubes was conducted with a scanning electron microscope (Hitachi S-900 field emission SEM). Optical transmittance spectra were measured with a Cary, Model 50 Probe UV-Visible Spectrophotometer. Quantum efficiency data was extracted from measurements made by an independent PV measurements company.[56] Electrical properties of the nanotube CdS-CdTe solar cells were characterized by current–voltage (I–V) as functions of light intensity and temperature in the 175 ºK -300 ºK range. A standard ScienceTech SS150 solar simulator was used for device illumination, the solar simulator was calibrated with a standard light meter. For low temperature measurement, nanotub solar cells were mounted inside an Oxford's vacuum cryostat with a helium refrigerator unit (Sumitomo Heavy Industries Ltd).

4.5.3 Results and Discussion

4.5.3.1 Scanning Electronic Micoscope

The AAO membrane-assisted electrodeposition, described above, can form CdS nanotubes or CdS nanowires, depending on growth conditions. CdS nanotubes are

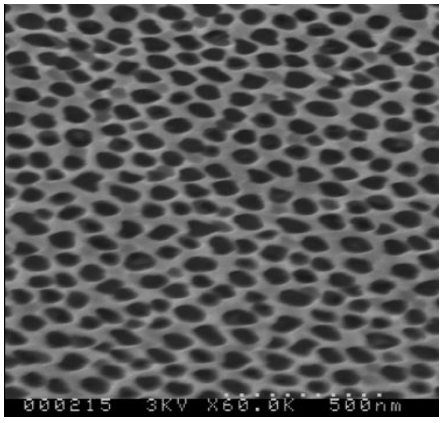
formed only at lower concentration of $CdCl_2$, lower dc current density, and lower deposition temperature. At higher concentration of $CdCl_2$, higher than $7mA/cm^2$ of dc current density and higher than 160°C deposition temperature, CdS nanowires instead of CdS nanotubes are formed. [54] The possible growth mechanism of CdS nanotubes can be explained as follows. Elemental sulfur diffused to the AAO template was subjected to reduction reaction to s^{-2} ions at nanopores. Cd^{+2} was attracted to nanopores in action of electrical field. Inside the nanopores, s^{-2} immediately reacts with Cd^{+2} , forming CdS crystalline. Under lower concentrations of $CdCl_2$, lower current density and temperature, the CdS preferentially nucleates and grows onto the nanopore walls of the AAO template due to lower Gibbs free energy at nanopore walls. At the bottom of the nanopores, low current density and temperature cannot provide sufficiently high energy because the the Gibbs free energy at the nanopore bottom is high. Therefore, CdS nucleation at nanopore bottom is suppressed. The precipitation of CdS takes place on nanopore walls of the AAO templates. When the concentration of $CdCl_2$ is reduced, precipitation rate of CdS is correspondingly decreased. Therefore, in a short growth time, the CdS nanotubes are formed. High current density and high temperature provide energy higher than Gibbs free energy at bottom of nanopores, therefore, CdS can nucleate and quickly grow along walls and bottom of the nanopores, resulting in CdS nanowires. Observing from appearance, the CdS nanotubes exhibit a color, which is lighter yellow than that of the CdS nanowires.

AAO membrane and CdS nanotubes were characterized by scanning electron microscopy (SEM). Figure 35a shows a SEM image of the top surface of AAO membrane, which possesses well-ordered nanopore features with diameter of approximate 80nm. Figure 35b shows top surface view SEM image of CdS nanotubes

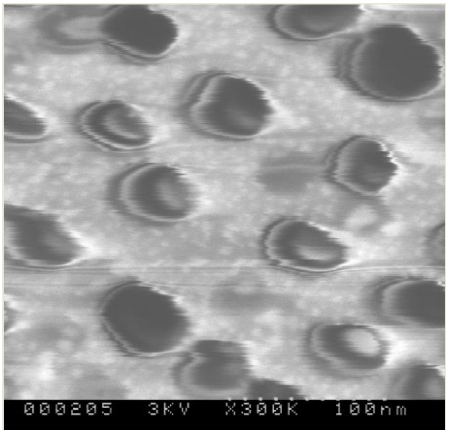
embedded in AAO membrane. Figure 35c, 2d and 2e show top view and side view SEM images of free-standing CdS nanotubes respectively, where AAO membrane has been removed. The CdS nanotubes are ordered structures with an average length, inner diameter and wall thickness of approximately 200nm, 35nm and 20nm respectively. From examination of SEM images, average center-to-center distance between CdS nanotubes is 110nm and thus the average intertube spacing is 35nm. Based on the CdS nanotube feature parameters, a porosity and CdS nanotube density are determined as 36.5% and 2.26×10^{10} nanotubes /cm^2 respectively.

Through SEM images, we anticipate that these high density CdS nanotube arrays provide novel ways to manipulate light absorption, and carrier generation and collection. As observed from SEM images, the nanotubes with 35nm inner diameter and 35nm intertube space will enable carriers to be effectively collected before they are lost by recombination, and hence will significantly improve carrier collection for those absorbers (for example, CuPC) with short minority carrier diffusion length, for example less than 100nm.

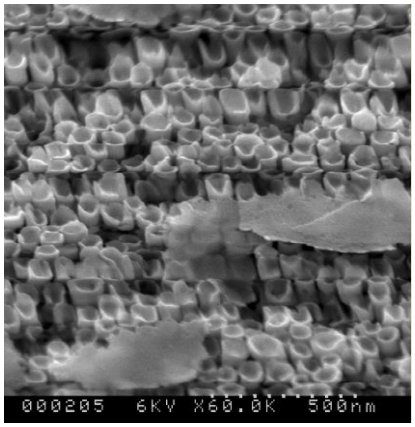
a



b



c



d

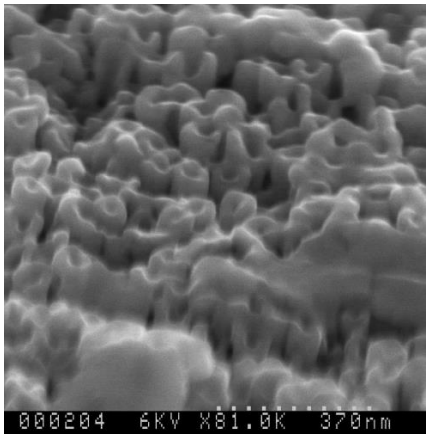


Figure 34, (a) Top view SEM image of AAO membrane. (b) Surface top view SEM image of CdS nanotubes embedded in AAO membrane. (c) Side view of free-standing CdS nanotubes. (d) Side view of free-standing CdS nanotubes.

4.5.3.2 Absorption and Transmittance of CdS nanotubes

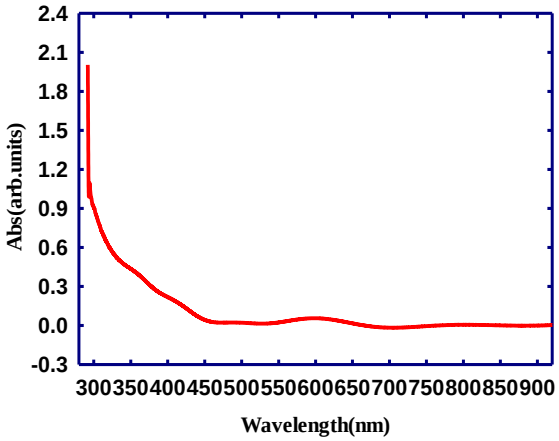
The fundamental absorption and transmittance of CdS nanotubes are especially interesting to understand their unique characteristics of light manipulation. UV-visible spectroscopy measurement was conducted over spectrum wavelengths from 300nm to 900nm, which cover most of sunlight photons of energy higher than the band gap of the CdTe absorber. Figure 36a and 36b show absorption and corresponding transmittance spectra of CdS nanotubes embedded in the AAO template. The CdS nanotubes exhibit nearly zero absorption and strong transmission from 450nm to 900nm. Only a weak absorption peak is observed at 600 nm and the corresponding transmittance is decreased to 0.88. A long absorption tail extends from 450nm to 296nm, and the corresponding transmittance is reduced from 0.925 to 0.10 between 450nm and 296nm, where the transmittance of the CdS nanotubes is reduced to 0.8 at 430nm. It is considered that such unique optical absorption and transmittance properties are related to transparent AAO membrane and geometry of CdS nanotubes. First, the absorption-negligible AAO membrane facilitates the transmission of sunlight through the substrate.. The length of the

CdS nanotubes is about 200nm, which is significantly smaller than the wavelength of incident light, thus making light scattering negligible. This phenomenon is different from the enhanced light scattering in long silicon nanowire structures.[43,100]

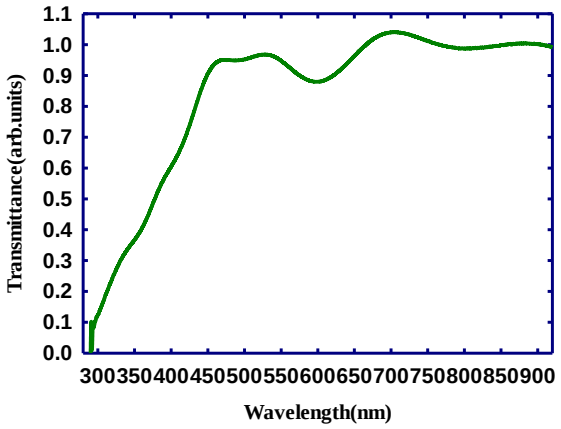
It should be noted that when the size of the nanotubes, for example length, exceeds the wavelength of the incident light, the nanotubes provide enhanced light scattering and light trapping, which increase the effective light path and light absorption.[43,100] Such long nanotubes can be favorably utilized for absorber materials. In the CdS-CdTe solar cell application, the CdS nanotubes were grown with 200nm length in order to function as a window layer, and benefit light absorption and carrier generation and collection in the CdTe absorber.

This unique light absorption behavior exemplifies beneficial properties of 200nm-long CdS nanotube geometry, which, here, is designed to enhance light absorption and carrier conversion in the CdTe absorber layer. This beneficial effect is further elucidated through the use of AM 1.5D spectrum and measured absorption spectrum of CdS nanotubes to simulate photon flux (P), which can be converted to carriers through the nanotube solar cells.

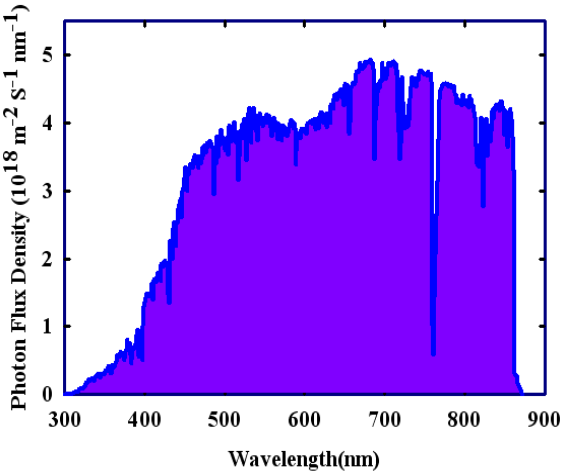
a



b



c



d

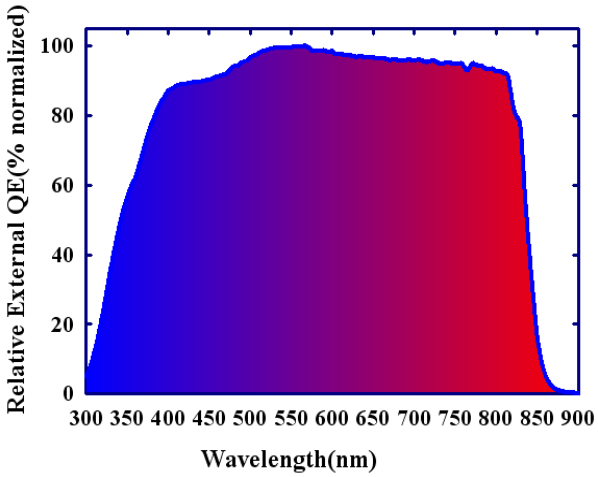


Figure 35, (a) Absorption spectra of CdS nanotubes embedded in the AAO membrane. (b) Corresponding transmittance of CdS nanotubes. (c) Simulated photon flux that is absorbed by the nanotube CdS-CdTe solar cell. (d) Relative EQE of the 3D nanostructured CdS-CdTe solar cells.

Figure 36c shows that the simulated photon flux $P_{nanotubes}$ that can be absorbed and be effective converted into photocurrent in nanotube CdS-CdTe solar cells. Photon flux $P_{nanotubes}$ was simulated on the basis of the measured transmittance spectrum of CdS nanotubes and absorption coefficient of CdTe at AM 1.5D spectrum. As shown in Figure 36c, simulation demonstrates that unique optical behavior of the CdS nanotubes yields a greater overall photon absorption enhancement for the nanotube CdS-CdTe solar cells. Integrating the photon flux shown in Figure 36c and assuming that each photon generates one electron-hole pair (EHP), the 3D nanotube CdS-CdTe solar cells create the total electron-hole pairs of $18.23*10^{16}/cm^2s$ and photocurrent density of $29.18mA/cm^2$. These data suggest that CdS nanobute array geometry, through tailoring optical properties at nanoscale, potentially enhances photon current density.

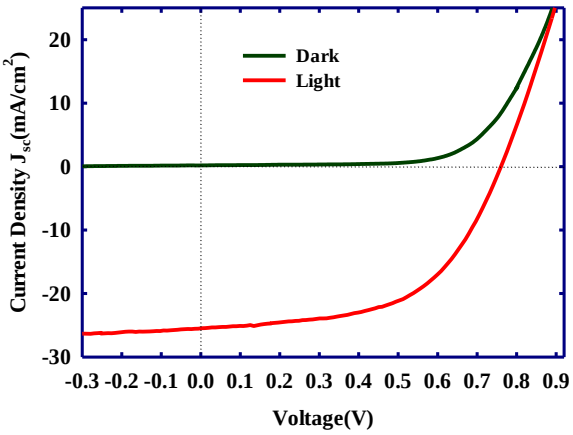
Figure 36d shows the normalized spectral response of the external quantum efficiency (EQE) of a nanotube CdS-CdTe solar cell on intrinsic SnO_2/ITO/soda-lime glass, which was measured by an independent group at the PV Measurements Inc.[56] EQE value increases steadily from 80% at 385 nm to 90% at 445 nm; it peaks at 565nm, and then stays strong until reaching 825nm which corresponds approximately to the energy band gap of the CdTe absorber layer. Integrating the spectral response of EQE and assuming 100% of maximum response and no transmittance loss in the substrate, photocurrent density is calculated to be $28.05\ mA/cm^2$. The photocurrent density calculated from EQE response is in agreement with the photon flux simulation. Strong EQE response from a broad spectral range indicates that the nanotube solar cell structure configuration can benefit photocarrier generation and collection. It should be noted that the above device is fabricated on the inexpensive and low transparent intrinsic SnO_2/ITO/soda-lime glass

substrate. Later, when the low transparent substrate is replaced by a higher transmission substrate, spectral response of the nanotube solar cells will be further improved.

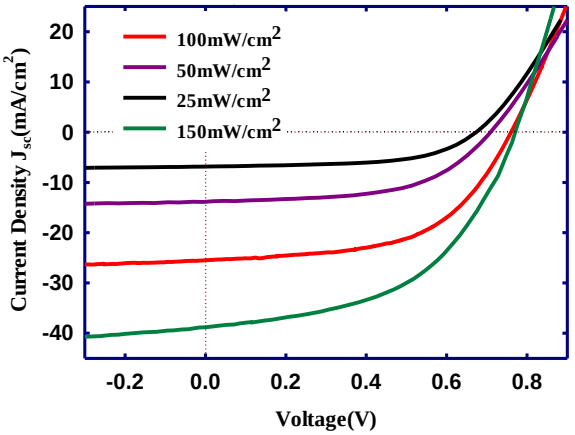
4.5.3.3 Photovoltaic Performance of nanotube CdS-CdTe Solar Cells

Characteristics of the photovoltaic performance of the nanotube CdS-CdTe solar cells were studied under dark and 1Sun irradiation using a solar simulator, which was calibrated through a standard light meter. Figure 37a shows the current density–voltage (J-V) characteristics of the nanotube solar cells under dark and standard 1-sun illumination conditions. Extracted J-V data of the CdS-CdTe nanotube solar cells yields short current density (J_{sc}) of 25.5 mA/cm^2, open circuit voltage (V_{oc}) of 750mV and fill factor of 55.9%, resulting in an overall power conversion efficiency of 10.7%.

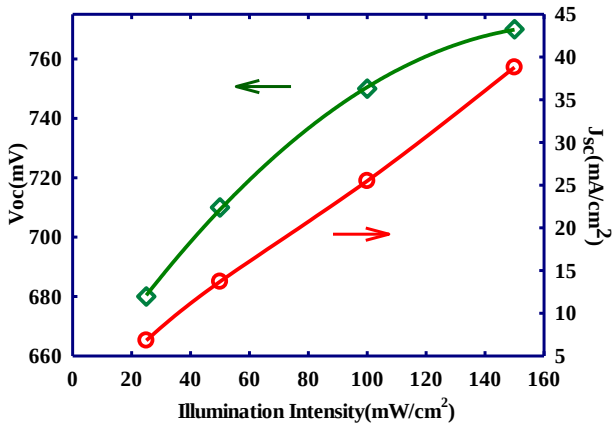
a



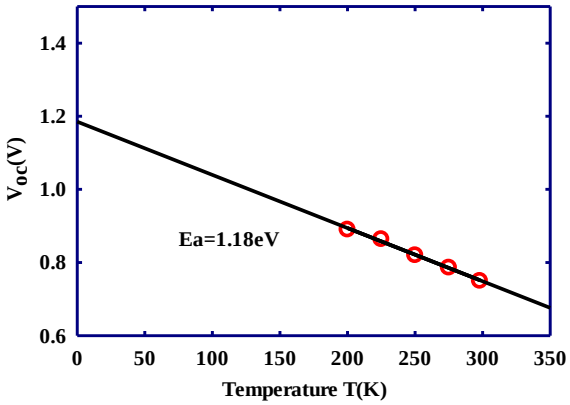
b



c



d



e

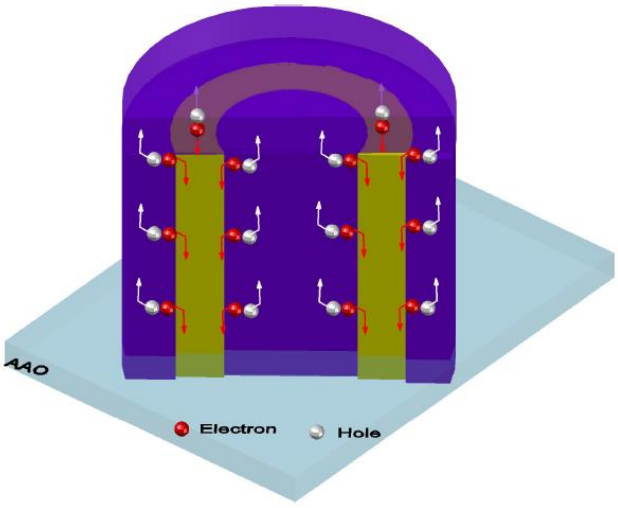


Figure 36, (a) J-V curves of the nanotube CdS-CdTe solar cells under dark and 1Sun illumination. (b) J-V curves of the nanotube CdS-CdTe solar cells as a function of illumination intensity. (c) V_{oc} and J_{sc} of the nanotube CdS-CdTe solar cells as a function of illumination intensity. (d) V_{oc} of the nanotube CdS-CdTe solar cells as a function of temperature under one-sun illumination. (e), Carrier transport along inner core and

intertube space of nanotubes in radial direction, and above the nanotube in axial direction, where yellow color represents CdS nanotubes, purple color represents absorber.

Measurement of photovoltaic properties as a function of illumination intensity (Figure 37b and table 7) shows that the efficiency is varied by 8%, indicating stability of the nanobute solar cells under light intensity. Efficiency is substantially higher and reaches 10.9% at 0.5 Sun illumination. Hence it is possible to improve efficiency exceeding 10.7% in the future. Dependence of J_{sc} and V_{oc} on the light intensity is shown in Figure 37c and table6. The J_{sc} increases from 6.81 mA/cm^2 to 38.8 mA/cm^2 and V_{oc} increases from 675mV to 770mV with light intensity, suggesting that photo-generated carriers are dominated and photon flux intensity doesn't cause obvious increase of reverse saturation current, which reveals a well junction at CdS nanotubes and CdTe absorber.

Table 7 Photovoltaic property of the nanotube CdS-CdTe solar cells as a function of illuminations intensity.

Sun Intensity	**J_{sc}(mA/cm^2)**	**V_{oc} (mV)**	**FF(%)**	**Efficiency (%)**	**Rs(Ω /cm^2)**	**Shunt Resistance (Ω /cm^2)**
0.25SUN	6.81	675	57.6	10.6	7.75	935.7
0.5SUN	13.7	710	56	10.9	7.47	431.6
1SUN	25.5	750	55.9	10.7	4.92	228.6
1.5SUN	38.8	770	50.6	10.08	3.95	128.2

The intrinsic SnO_2/ITO-soda-lime glass substrate used here has relatively low transmittance and hence negatively impacts photocurrent. Still, nanotube solar cells exhibit relatively high short current density of 25.5 mA/cm^2 under 1-Sun illumination without antireflective coating. High J_{sc} depends on effective light absorption, and efficient carrier generation and collection. In the 3D nanotube solar cell structure, CdTe forms junctions with CdS nanotubes in radial and axial dimensions (Figure 37e) because CdTe contacts inner core and intertube space of the CdS nanotubes, and the space above the nanotubes (Figure 37e). When light illuminates from transparent side, incident light transmits through the CdS nantubes and the transparent AAO membrane into the CdTe absorber where most of photons are absorbed and generate carriers (Figure 37e). Hence, the light absorption behavior is improved. Carrier transport behavior is another factor for high J_{sc}. Photo-generated electrons in CdTe layer above the plane of CdS nanotubes drift readily into the CdS nanotubes along the axial direction and are then collected by the front contact. In addition, because the CdTe laterally contacts CdS nanotubes from their inner core space and outer wall space, those photo-generated electrons drift into CdS along the radial direction (Figure 37e). Thus, more direct paths are provided along three dimensions for carrier generation and transport. In other words, carrier generation and transport occur in three dimensions which include the axial direction above wall of CdS nanotubes, and the radial direction along inner core and intertube space of CdS nanotubes (Figure 37e). It is in this manner that the unique 3D nanotube photovoltaic structure facilitates carriers to be effectively generated and collected.

The fill factor is attributed to series and shunt resistances. The series resistance is estimated to be 4.92Ω/cm^2. This series resistance is arising from bulk and contact

resistances. One reason is that the graphite paste we used for back-contacts had a sheet resistance of 1200-2400Ω/sq. Low shunt resistance might have been caused by contribution from the incomplete isolation caused by less than satisfactory scribing of intrinsic SnO_2. Another reason for the low shunt resistance is related to non-optimal growth of CdS nanotubes. In short, the fill factor and efficiency can be substantially improved in future by optimizing the growth of CdS nanotubes, developing a low-resistance back-contact to CdTe, and replacing intrinsic SnO_2 with high transparent TCO.

Diode ideality factor (A), reverse saturation current density (J_o), and shunt conductance for the junction performance are extracted from dark J-V curve. Fits to ln(J)–V data in forward bias between 0.5V and 0.8V are approximately linear and yield diode ideality factor, A of 2.49 and J_o of 1.2×10^{-7}A/cm^2. From the slope of the J–V characteristic at zero bias, the shunt conductance is estimated to be 2.39×10^{-4}(S/cm^2), which corresponds to a shunt resistance of 4184Ω/cm^2. A value of A higher than 2 and a relatively high J_o indicate that tunneling and interface recombination are participating in the electron and hole transport processes across the p-n junction.[70] In the dark, the shunt conductance is close to the lower end of shunt conductance values reported in the literature of planar CdS-CdTe solar cells.[116] This suggests that the interface structure is not a significant factor for the shunting effect. Thus I-V analysis indicates that the nanotube solar cells have those fundamental diode characteristics which are essential for making solar cell devices with power conversion efficiency higher than 10%. However, the diode behavior could be further improved for enhancement of power conversion efficiency.

The V_{oc} value of 750 mV in these nanotube solar cells is higher than the value of 620mV for the CdS nanopillar solar cells reported earlier.[38] However it is lower than

845mV, which is the V_{oc} of the one of the best planar solar cells.[32] It is a factor that limits the efficiency and needs to be improved in the future. To identify the processes which limit device performance in these nanotube solar cells, we conducted I-V characteristics at different temperatures in the 300 ºK -200 ºK range. Figure 37d shows V_{oc} as a function of temperature. As expected, V_{oc} increases with decreasing temperature due to reduction in temperature dependent losses associated with the reverse saturation current of the CdS-CdTe heterojunction. V_{oc} approaching the value of Eg/q=1.45 volts (band gap of CdTe absorber) as T approaches zero indicates an ideal p-n junction.[71] For our device, V_{oc} in Figure 4D extrapolates to a value of 1.18 volts as T approaches 0 K. This is lower than the value of 1.45 volts for CdTe and is an indication of the presence of non-ideal current transport mechanisms involving tunneling and interface recombination at the CdS-CdTe interface.[71] We are in the process of devising strategies for reducing the tunneling and interface recombination currents at the junction interface in these nanotube solar cells.

For the first time, we have fabricated nanotube CdS-CdTe solar cells with power conversion efficiency (PCE) of over 10 %. The efficiency could be further improved through improvement of V_{oc} and fill factor, by means of follows: reducing the densities of traps and interface states through optimizing growth of CdS nanotubes and CdTe, developing low-resistance back contacts, and better understanding of nanotube junctions and interfaces.

4.5.3.4 Conclusion

In summary, we first time fabricated and characterized the nanotube CdS-CdTe solar cells where CdTe absorber is filled in the inner core space and intertube space of the CdS nanotubes. We grown CdS nanotubes with inner diameter, wall thickness and intertube

spacing of 35nm, 20nm and 35nm respectively; and a porosity and CdS nanotube density are 36.5% and $2.26x10^{10}$ nanotubes /cm^2 respectively. Such fine features of CdS nanotubes enable more efficient carrier collection because of reduced recombination, especially in those cases where the minority carrier lifetime is short resulting in a diffusion length less than 100 nm. In such nanotube solar cells, carrier generation and collection occur in three dimensions which include inner core and intertube space along the radial direction, and above the nanotubes along the axial direction. We have demonstrated through a very wide and strong quantum efficiency spectra that the configured nanotube solar cells can effectively enhance carrier generation and collection. In preliminary experiments, the nanotube CdS-CdTe solar cells, with no additional antireflection coating, exhibited short current density of 25.5 mA/cm^2, open circuit voltage of 750mV, and power conversion efficiency of 10.7% under 1Sun illumination. Analysis of the junction characteristics of the nanotube CdS-CdTe solar cells indicated well-defined diode junction and interface, with various optimizations, a far higher PCE value is reachable. By enhancing generation and collection of carriers in 3D directions, such nanotube solar cell configuration will find a general application especially for solar cells whose absorbers have short minority carrier lifetime.

Chapter 5 Summary and Future Work

5.1 Design of Nanowire CdS-CdTe Solar Cells Without High Resistivity Buffer Layer

This work has demonstrated that CdTe solar cells including CdS nanowires as window layer can enhance spectral response of quantum efficiency at a wide spectrum range and strongly improve reliability. Generally, in planar CdS-CdTe solar cells, to reduce the absorption loss in planar CdS window layer, one approach was to reduce the planar CdS thickness to 50nm. Such planar window layer thinning presents significant challenges i) substrate roughness and pinholes can exacerbate shunting and negatively influence open circuit voltage (V_{oc}); ii) it necessitates an additional high resistivity buffer layer between the TCO and the CdS window layer. The high resistivity buffer layer could increase series resistance and manufacturing costs.

This work has shown that when embedded CdS nanowires are used for the window layer instead of the traditional planar CdS film, reliability of power conversion efficiency is increased by a factor of approximately 3, and light absorption loss in the window layer is strongly suppressed. This is because that the CdS nanowires are embedded in the absorption-negligible anodized aluminum oxide (AAO) membrane, and the junction surface area between nanowire CdS and CdTe is reduced substantially by 68%; and also, CdS nanowires in the pores of AAO membrane are crystalline in nature and have low density of defect features. Therefore, in the nanowire CdS-CdTe solar cells, it is unnecessary to include the traditional high resistivity buffer layer between ITO and nanowire CdS. This would lead to reduced manufacturing costs as well as reduced series resistance for the solar cells.

Therefore, the nanowire CdS-CdTe solar cells can be configured into glass/ITO/CdS nanowires embedded in AAO/ CdTe/ back contact structure. In addition, the nanowire CdS-CdTe solar cells can be additionally configured into aluminum foil/CdS nanowires embedded in AAO/ CdTe/ back contact structure.

5.2 Route of Improvement Power Conversion Efficiency of Nanowire CdS-CdTe Solar Cells

We have demonstrated that the nanowire solar cells yielded an open-circuit voltage V_{oc} of 770 mV, a short current density J_{sc} of 26 mA/cm^2, a fill factor, FF of 60%, and a power conversion efficiency (PCE) of 12%. However, according to theoretical simulation, nanowire solar cells can yield 29.84 mA/cm^2, V_{oc} of 912mV, the J_{sc} gain of 19.2%, V_{oc} gain of 7.3%, and a cumulative gain of 27.8% in the power conversion efficiency on intrinsic SnO_2/ITO-soda lime glass substrates. The corresponding gain in the power conversion efficiency of the CdTe solar cells on high quality transparent substrates would be 30%, where J_{sc} value is calculated to be 32.1 mA/cm^2.

Hence, there is a lot of room to improve efficiency of nanowire CdS-CdTe solar cells. Low V_{oc} and fill factor are mainly responsible for low efficiency. The low V_{oc} is related with interface states and deep traps. High series resistance and low shunt resistance are responsible for low fill factor.

V_{oc} and shunt resistance can be improved by optimizing growth of CdS nanowires, reducing low vacuum from 0.25 torr to 0.02 torr, increasing deposition temperature of CdTe film, and optimizing the $CdCl_2$ heat treatment. These steps can significantly reduce interface states and deep straps, hence increasing V_{oc} and shunt resistance.

Series resistance can be obviously decreased by reducing the thickness of bulk CdTe

film, and replacing high resistive graphite paste with 1200-2400 Ω/sql with low resistance of Cu doped graphite paste. When series resistance is reduced, the power conversion efficiency will be significantly improved.

References

1 Musselman, K. P. & Schmidt-Mende, L. Nanostructured inorganic solar cells. *Green* **1**, 7-27 (2011).
2 Petroleum, B. Statistical review of world energy June 2014. (2014).
3 Agency, I. E. world energy outlook 2012 (2012).
4 Lewis, N. S. Chemical Challenges in Renewable Energy. (2005).
5 Agency, I. E. Technology Roadmap Solar Photovoltaic Energy (2014).
6 Association, E. P. I. Global Market Outlook for photovoltaics 2014-2018 (2014).
7 Agency, I. E. Key World Energy Statistics (2014).
8 Department, E. *http://energy.gov/articles/us-utility-scale-solar-60-percent-towards-cost-competition-goal* (2014).
9 Department, E. *http://energy.gov/articles/energy-department-announces-more-59-million-investment-solar* (2015).
10 Razykov, T. *et al.* Solar photovoltaic electricity: Current status and future prospects. *Solar Energy* **85**, 1580-1608 (2011).
11 Green, M. A., Emery, K., Hishikawa, Y., Warta, W. & Dunlop, E. D. Solar cell efficiency tables (Version 45). *Progress in photovoltaics: research and applications* **23**, 1-9 (2015).
12 Wolden, C. A. *et al.* Photovoltaic manufacturing: Present status, future prospects, and research needs. *Journal of Vacuum Science & Technology A* **29**, 030801 (2011).
13 Wang, W. *et al.* Device Characteristics of CZTSSe Thin-Film Solar Cells with 12.6% Efficiency. *Advanced Energy Materials* **4**, n/a-n/a, doi:10.1002/aenm.201301465 (2014).
14 Boix, P. P., Nonomura, K., Mathews, N. & Mhaisalkar, S. G. Current progress and future perspectives for organic/inorganic perovskite solar cells. *Materials Today* **17**, 16-23 (2014).
15 Laboratory, N. R. E. *http://www.nrel.gov/ncpv/* (2015).
16 Energy, S. U. S. D. o. Photovoltaic System Pricing Trends 2014
17 First Solar, *www.firstsolar.com*
18 ISE, F. Fraunhofer institute for solar enenrgy systems ISE (2014).
19 Adolf Goetzberger, J. L., Gerhard Willeke. Solar cells: past, present, future. *Solar Energy Materials & Solar Cells* **74**, 1-11 (2002).
20 S.M.SZE, K. K. N. Physics of Semiconductor Devices. (2006).
21 Wurfel, P. Physics of Solar Cells from principles to new concepts. (2005).
22 Fonash, S. Solar Cell Device Physics *Academic Press* (2010).

23 AlRashidi, M., El-Naggar, K. & AlHajri, M. Parameters estimation of double diode solar cell model. *World Academy of Science, Engineering and Technologoy* **74** (2013).
24 Aliyu, M. *et al.* Recent developments of flexible CdTe solar cells on metallic substrates: issues and prospects. *International Journal of Photoenergy* **2012** (2012).
25 Reynolds, D. & Czyzak, S. Mechanism for photovoltaic and photoconductivity effects in activated CdS crystals. *Physical Review* **96**, 1705 (1954).
26 Woodbury, H. & Aven, M. Some diffusion and solubility measurements of Cu in CdTe. *Journal of Applied Physics* **39**, 5485-5488 (1968).
27 Bonnet D., R. H. New results on the development of a thin film p-CdTe–n-CdS heterojunction solar cell. *Proceedings of the 9th Photovoltaic Specialists Conference*, 129-131 (1972).
28 Basol, B. M. Electrodeposited CdTe and HgCdTe solar cells. *Solar Cells* **23**, 69-88 (1988).
29 Tyan, Y. S., Perez-Albuerne, E.A. Efficient thin film CdS/CdTe solar cells. *IEEE Publishing, IEEE Publishing*, 794 (1982).
30 al., T. L. C. e. *IEEE Electron. Dev. Lett.* **13**, 303 (1992).
31 Britt, J. & Ferekides, C. Thin-film CdS/CdTe solar cell with 15.8% efficiency. *Applied Physics Letters* **62**, 2851-2852 (1993).
32 Wu, X. High-efficiency polycrystalline CdTe thin-film solar cells. *Solar energy* **77**, 803-814 (2004).
33 Kosyachenko, L., Grushko, E. & Mathew, X. Quantitative assessment of optical losses in thin-film CdS/CdTe solar cells. *Solar Energy Materials and Solar Cells* **96**, 231-237 (2012).
34 Ferekides, C. *et al.* CdTe thin film solar cells: device and technology issues. *solar Energy* **77**, 823-830 (2004).
35 Han, J. *et al.* Optimized chemical bath deposited CdS layers for the improvement of CdTe solar cells. *Solar Energy Materials and Solar Cells* **95**, 816-820 (2011).
36 Kartopu, G. *et al.* Effect of window layer composition in Cd1− xZnxS/CdTe solar cells. *Progress in Photovoltaics: Research and Applications* **22**, 18-23 (2014).
37 Dobson, K. D., Visoly-Fisher, I., Hodes, G. & Cahen, D. Stabilizing CdTe/CdS Solar Cells with Cu-Containing Contacts to p-CdTe. *Advanced Materials* **13**, 1495-1499 (2001).
38 Fan, Z. *et al.* Three-dimensional nanopillar-array photovoltaics on low-cost and flexible substrates. *Nature materials* **8**, 648-653 (2009).
39 Liu, P., Singh, V. P., Jarro, C. A. & Rajaputra, S. Cadmium sulfide nanowires for the window semiconductor layer in thin film CdS–CdTe solar cells. *Nanotechnology* **22**, 145304 (2011).
40 Suh, J. S. & Lee, J. S. Surface enhanced Raman scattering for CdS nanowires deposited in anodic aluminum oxide nanotemplate. *Chemical Physics Letters* **281**, 384-388 (1997).
41 Dang, H. *et al.* in *Photovoltaic Specialists Conference (PVSC), 2012 38th IEEE.* 002697-002701 (IEEE).

42 Lee, Y.-J., Ruby, D. S., Peters, D. W., McKenzie, B. B. & Hsu, J. W. ZnO nanostructures as efficient antireflection layers in solar cells. *Nano letters* **8**, 1501-1505 (2008).
43 Oh, J., Yuan, H.-C. & Branz, H. M. An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures. *Nature nanotechnology* **7**, 743-748 (2012).
44 Huang, M.-J., Yang, C.-R., Chiou, Y.-C. & Lee, R.-T. Fabrication of nanoporous antireflection surfaces on silicon. *Solar Energy Materials and Solar Cells* **92**, 1352-1357 (2008).
45 Jackson, P. *et al.* New world record efficiency for Cu (In, Ga) Se2 thin-film solar cells beyond 20%. *Progress in Photovoltaics: Research and Applications* **19**, 894-897 (2011).
46 Repins, I. *et al.* 19· 9%-efficient ZnO/CdS/CuInGaSe2 solar cell with 81· 2% fill factor. *Progress in Photovoltaics: Research and applications* **16**, 235-239 (2008).
47 Todorov, T. K. *et al.* Beyond 11% Efficiency: Characteristics of State-of-the-Art Cu2ZnSn (S, Se) 4 Solar Cells. *Advanced Energy Materials* **3**, 34-38 (2013).
48 Burschka, J. *et al.* Sequential deposition as a route to high-performance perovskite-sensitized solar cells. *Nature* **499**, 316-319 (2013).
49 Lee, M. M., Teuscher, J., Miyasaka, T., Murakami, T. N. & Snaith, H. J. Efficient hybrid solar cells based on meso-superstructured organometal halide perovskites. *Science* **338**, 643-647 (2012).
50 Routkevitch, D., Bigioni, T., Moskovits, M. & Xu, J. M. Electrochemical fabrication of CdS nanowire arrays in porous anodic aluminum oxide templates. *The Journal of Physical Chemistry* **100**, 14037-14047 (1996).
51 Al-Mawlawi, D., Liu, C. & Moskovits, M. Nanowires formed in anodic oxide nanotemplates. *Journal of materials research* **9**, 1014-1018 (1994).
52 Shimizu, T. *et al.* Synthesis of Vertical High-Density Epitaxial Si (100) Nanowire Arrays on a Si (100) Substrate Using an Anodic Aluminum Oxide Template. *Advanced Materials* **19**, 917-920 (2007).
53 Mondal, S., Das, K., Dhar, A. & Ray, S. Characteristics of CdS nanowires grown in a porous alumina template using a two-cell method. *Nanotechnology* **18**, 095606 (2007).
54 Dang, H. *et al.* Cadmium sulfide nanowire arrays for window layer applications in solar cells. *Solar Energy Materials and Solar Cells* **126**, 184-191 (2014).
55 Kranz, L. *et al.* Doping of polycrystalline CdTe for high-efficiency solar cells on flexible metal foil. *Nature communications* **4** (2013).
56 PV Measurements, I.
57 Nakada, T. & Mizutani, M. 18% efficiency Cd-free Cu (In, Ga) Se2 thin-film solar cells fabricated using chemical bath deposition (CBD)-ZnS buffer layers. *Japanese Journal of Applied Physics* **41**, L165 (2002).
58 Ramanathan, K. *et al.* Properties of 19.2% efficiency ZnO/CdS/CuInGaSe2 thin-film solar cells. *Progress in Photovoltaics: Research and Applications* **11**, 225-230 (2003).
59 Barkhouse, D. A. R., Gunawan, O., Gokmen, T., Todorov, T. K. & Mitzi, D. B. Device characteristics of a 10.1% hydrazine-processed Cu2ZnSn (Se, S) 4 solar cell. *Progress in Photovoltaics: Research and Applications* **20**, 6-11 (2012).

60 Ahmed, S. *et al.* A high efficiency electrodeposited Cu2ZnSnS4 solar cell. *Advanced Energy Materials* **2**, 253-259 (2012).
61 Todorov, T. K., Reuter, K. B. & Mitzi, D. B. High-Efficiency Solar Cell with Earth-Abundant Liquid-Processed Absorber. *Advanced materials* **22**, E156-E159 (2010).
62 Chirilă, A. *et al.* Highly efficient Cu (In, Ga) Se2 solar cells grown on flexible polymer films. *Nature materials* **10**, 857-861 (2011).
63 Yang, W. *et al.* Novel Solution Processing of High-Efficiency Earth-Abundant Cu2ZnSn (S, Se) 4 Solar Cells. *Advanced Materials* **24**, 6323-6329 (2012).
64 Rose, D. H. *et al.* Fabrication procedures and process sensitivities for CdS/CdTe solar cells. *Progress in Photovoltaics Research and Applications* **7**, 331-340 (1999).
65 Paudel, N. R., Compaan, A. D. & Yan, Y. Ultrathin CdTe Solar Cells with MoO3− x/Au Back Contacts. *Journal of Electronic Materials*, 1-5 (2014).
66 Paudel, N., Compaan, A. & Yan, Y. Sputtered CdS/CdTe solar cells with MoO< sub> 3− x</sub>/Au back contacts. *Solar Energy Materials and Solar Cells* **113**, 26-30 (2013).
67 Lin, H., Xia, W., Wu, H. N. & Tang, C. CdS/CdTe solar cells with MoO x as back contact buffers. *Applied Physics Letters* **97**, 123504-123504-123503 (2010).
68 Balcioglu, A., Ahrenkiel, R. & Hasoon, F. Deep-level impurities in CdTe/CdS thin-film solar cells. *Journal of Applied Physics* **88**, 7175-7178 (2000).
69 Seymour, F. H., Kaydanov, V., Ohno, T. R. & Albin, D. Cu and CdCl2 influence on defects detected in CdTe solar cells with admittance spectroscopy. *Applied Physics Letters* **87**, 153507 (2005).
70 Singh, V. P., Linam, D. L., Dils, D., McClure, J. C. & Lush, G. Electro-optical characterization and modeling of thin film CdS–CdTe heterojunction solar cells. *Solar energy materials and solar cells* **63**, 445-466 (2000).
71 Hegedus, S. S. & Shafarman, W. N. Thin-film solar cells: device measurements and analysis. *Progress in Photovoltaics: Research and Applications* **12**, 155-176 (2004).
72 Green, M. A., Emery, K., Hishikawa, Y., Warta, W. & Dunlop, E. D. Solar cell efficiency tables (version 39). *Progress in photovoltaics: research and applications* **20**, 12-20 (2012).
73 Liu, M., Johnston, M. B. & Snaith, H. J. Efficient planar heterojunction perovskite solar cells by vapour deposition. *Nature* **501**, 395-398 (2013).
74 Dang, H., Rajaputra, S., guduru, s. & Singh, V. Cadmium Sulfide Nanowire Arrays for Window Layer Applications in Solar Cells. *Solar Energy Materials and Solar Cells* (2014).
75 Simchi, H., McCandless, B. E., Meng, T. & Shafarman, W. N. Structure and interface chemistry of MoO3 back contacts in Cu (In, Ga) Se2 thin film solar cells. *Journal of Applied Physics* **115**, 033514 (2014).
76 Battaglia, C. *et al.* Silicon heterojunction solar cell with passivated hole selective MoOx contact. *Applied Physics Letters* **104**, 113902 (2014).
77 Battaglia, C. *et al.* Hole Selective MoO x Contact for Silicon Solar Cells. *Nano letters* **14**, 967-971 (2014).

78 Romeo, A. *et al.* Development of thin-film Cu (In, Ga) Se2 and CdTe solar cells. *Progress in Photovoltaics: Research and Applications* **12**, 93-111 (2004).
79 Rios-Flores, A., Arés, O., Camacho, J. M., Rejon, V. & Peña, J. Procedure to obtain higher than 14% efficient thin film CdS/CdTe solar cells activated with HCF 2 Cl gas. *Solar Energy* **86**, 780-785 (2012).
80 Strevel, N., Trippel, L., Kotarba, C. & Khan, I. Improvements in CdTe module reliability and long-term degradation through advances in construction and device innovation. . *Photovoltaics International* **22**, 1-8 (2012).
81 Morales-Acevedo, A. Thin film CdS/CdTe solar cells: research perspectives. *Solar Energy* **80**, 675-681 (2006).
82 Chopra, K., Paulson, P. & Dutta, V. Thin-film solar cells: an overview. *Progress in Photovoltaics: Research and Applications* **12**, 69-92 (2004).
83 Hegedus, S. Thin film solar modules: the low cost, high throughput and versatile alternative to Si wafers. *Progress in photovoltaics: research and applications* **14**, 393-411 (2006).
84 Visoly-Fisher, I. *et al.* Factors affecting the stability of CdTe/CdS solar cells deduced from stress tests at elevated temperature. *Advanced Functional Materials* **13**, 289-299 (2003).
85 Ulbrich, C., Jordan, D. C., Kurtz, S. R., Gerber, A. & Rau, U. Direct analysis of the current density vs. voltage curves of a CdTe module during outdoor exposure. *Solar Energy* **113**, 88-100 (2015).
86 Moutinho, H. *et al.* Role of Cu on the electrical properties of CdTe⁄CdS solar cells: A cross-sectional conductive atomic force microscopy study. *Journal of Vacuum Science & Technology B* **25**, 361-367 (2007).
87 Roehl, J. & Khare, S. Diffusion of Cd vacancy and interstitials of Cd, Cu, Ag, Au and Mo in CdTe: A first principles investigation. *Solar Energy* **101**, 245-253 (2014).
88 Li, J. V. *et al.* in *Photovoltaic Specialists Conference (PVSC), Volume 2, 2012 IEEE 38th.* 1-5.
89 Corwine, C., Pudov, A., Gloeckler, M., Demtsu, S. & Sites, J. Copper inclusion and migration from the back contact in CdTe solar cells. *Solar Energy Materials and Solar Cells* **82**, 481-489 (2004).
90 Xu, D. *et al.* Preparation and characterization of CdS nanowire arrays by dc electrodeposit in porous anodic aluminum oxide templates. *Chemical Physics Letters* **325**, 340-344 (2000).
91 Badawi, A., Al-Hosiny, N., Abdallah, S., Negm, S. & Talaat, H. Tuning photocurrent response through size control of CdTe quantum dots sensitized solar cells. *Solar Energy* **88**, 137-143 (2013).
92 Dang, H., Singh, V. P., Guduru, S., Bowie, J. & Cambron, D. in *Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th.* 1601-1606 (IEEE).
93 Nakamura, K., Fujihara, T., Toyama, T. & Okamoto, H. Influence of CdCl2 Treatment on Structural and Electrical Properties of Highly Efficient 2-μm-Thick CdS/CdTe Thin Film Solar Cells. *Japanese journal of applied physics* **41**, 4474 (2002).
94 Mathew, X. *et al.* CdS thin film post-annealing and Te–S interdiffusion in a CdTe/CdS solar cell. *Solar Energy* **86**, 1023-1028 (2012).

95 Singh, V., Erickson, O. & Chao, J. Analysis of contact degradation at the CdTe-electrode interface in thin film CdTe-CdS solar cells. *Journal of applied physics* **78**, 4538-4542 (1995).
96 Yu, P. *et al.* 13% Efficiency Hybrid Organic/Silicon-Nanowire Heterojunction Solar Cell via Interface Engineering. *ACS nano* **7**, 10780-10787 (2013).
97 Huynh, W. U., Dittmer, J. J. & Alivisatos, A. P. Hybrid nanorod-polymer solar cells. *science* **295**, 2425-2427 (2002).
98 Law, M., Greene, L. E., Johnson, J. C., Saykally, R. & Yang, P. Nanowire dye-sensitized solar cells. *Nature materials* **4**, 455-459 (2005).
99 Lee, S.-M. *et al.* Printable Nanostructured Silicon Solar Cells for High-Performance, Large-Area Flexible Photovoltaics. *ACS nano* **8**, 10507-10516 (2014).
100 Tian, B. *et al.* Coaxial silicon nanowires as solar cells and nanoelectronic power sources. *Nature* **449**, 885-889 (2007).
101 Baxter, J. B. & Aydil, E. S. Nanowire-based dye-sensitized solar cells. *Applied Physics Letters* **86**, -, doi:doi:http://dx.doi.org/10.1063/1.1861510 (2005).
102 Tétreault, N. *et al.* High-efficiency solid-state dye-sensitized solar cells: fast charge extraction through self-assembled 3D fibrous network of crystalline TiO2 nanowires. *ACS nano* **4**, 7644-7650 (2010).
103 Chang, J. A. *et al.* High-performance nanostructured inorganic− organic heterojunction solar cells. *Nano letters* **10**, 2609-2612 (2010).
104 Kim, C.-H. *et al.* Silver nanowire embedded in P3HT: PCBM for high-efficiency hybrid photovoltaic device applications. *ACS nano* **5**, 3319-3325 (2011).
105 Shankar, K., Feng, X. & Grimes, C. A. Enhanced harvesting of red photons in nanowire solar cells: Evidence of resonance energy transfer. *Acs Nano* **3**, 788-794 (2009).
106 Zhang, J. *et al.* A 12%-Efficient Upgraded Metallurgical Grade Silicon-Organic Heterojuction Solar Cell Achieved by Self-Purifying Process. *ACS nano* (2014).
107 Kelzenberg, M. D. *et al.* Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications. *Nature materials* **9**, 239-244 (2010).
108 Fan, Z. *et al.* Challenges and prospects of nanopillar-based solar cells. *Nano Research* **2**, 829-843 (2009).
109 Diggle, J. W., Downie, T. C. & Goulding, C. Anodic oxide films on aluminum. *Chemical Reviews* **69**, 365-405 (1969).
110 Piao, Y., Lim, H., Chang, J. Y., Lee, W.-Y. & Kim, H. Nanostructured materials prepared by use of ordered porous alumina membranes. *Electrochimica Acta* **50**, 2997-3013 (2005).
111 Li, Y. *et al.* Preparation of cadmium sulfide nanowire arrays in anodic aluminum oxide templates. *Chemistry of materials* **11**, 3433-3435 (1999).
112 Kyotani, T., Tsai, L.-f. & Tomita, A. Formation of ultrafine carbon tubes by using an anodic aluminum oxide film as a template. *Chemistry of materials* **7**, 1427-1428 (1995).
113 Lee, J. S. *et al.* Growth of carbon nanotubes on anodic aluminum oxide templates: fabrication of a tube-in-tube and linearly joined tube. *Chemistry of Materials* **13**, 2387-2391 (2001).

114 Bae, E. J. *et al.* Selective growth of carbon nanotubes on pre-patterned porous anodic aluminum oxide. *Advanced Materials* **14**, 277 (2002).
115 Peng, T., Yang, H., Dai, K., Pu, X. & Hirao, K. Fabrication and characterization of CdS nanotube arrays in porous anodic aluminum oxide templates. *Chemical physics letters* **379**, 432-436 (2003).
116 del Cueto, J., Pruett, J. & Cunningham, D. Stabilization of High Efficiency CdTe Photovoltaic Modules in Controlled Indoor Light Soaking. (National Renewable Energy Laboratory (NREL), Golden, CO., 2003).

Vita

The author received her Bachelor's degree in Materials Science and Engineering at University of Science and Techonlogy of Beijing, and her Master degree in Physics at Tsinghua University and Master's degree in the department of Chemical and Materials Engineering, University of Kentucky. She defened her PhD dissertation at April 13, 2015, Department of Electrical and Computer Engineering, University of Kentucky.