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Stargrazer One: A New Architecture for Distributed Maximum Power Point Tracking of Solar Photovoltaic Sources

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Edgard Munoz-Coreas, Student

Dr. Lawrence E. Holloway, Major Professor

Dr. Cai-Cheng Lu, Director of Graduate Studies

Stargrazer One:
A New Architecture for Distributed Maximum Power Point Tracking of Solar Photovoltaic Sources

THESIS

A Thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering in the College of Engineering at the University of Kentucky

By
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ABSTRACT OF THESIS

Stargrazer One:
A New Architecture for Distributed Maximum Power Point Tracking of Solar Photovoltaic Sources

The yield from a solar photovoltaic (PV) source is dependent on factors such as light and temperature. A control system called a maximum power point tracker (MPPT) ensures that the yield from a solar PV source is maximized in spite of these factors.

This thesis presents a novel implementation of a perturb and observe (PO) MPPT. The implementation uses a switched capacitor step down converter and a custom digital circuit implementation of the PO algorithm. Working in tandem, the switched capacitor step down converter and the custom digital circuit implementation were able to successfully track the maximum power point of a simulated solar PV source. This implementation is free of the overhead encountered with general purpose processor based MPPT implementations. This makes this MPPT system a valid candidate for applications where general purpose processors are undesirable.

This document will begin by discussing the current state of MPPT research. Afterward, this thesis will present studies done to be able to use the chosen switched capacitor step down converter. Then the digital circuit PO implementation will be discussed in detail. Simulations of the architecture will be presented. Finally, experimental validation using a hardware prototype will be shown.

KEYWORDS: solar energy, maximum power point tracker, computer architecture, switched capacitor, power electronics, renewable energy

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Date: July 3, 2015

Stargrazer One:
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Mr. Richard Anderson also must be thanked. Without his assistance, the design and testing of the hardware prototype would not have taken place. He provided me a place to work and made sure that I was able to get the needed assistance and materials so that this system could be instantiated and tested.

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Chapter 1 Introduction

1.1 Introduction

This chapter will explain the purpose of this research and discuss how the thesis will be organized. Discussion will begin by describing the problem to be addressed then focus in on the particular implementation and conclude with discussing the order of the thesis

1.2 Project Motivation

Currently the overwhelming majority of our electric power comes from fossil fuels such as coal, natural gas, or oils. Figure 1.1 shows this is the case for the United States.

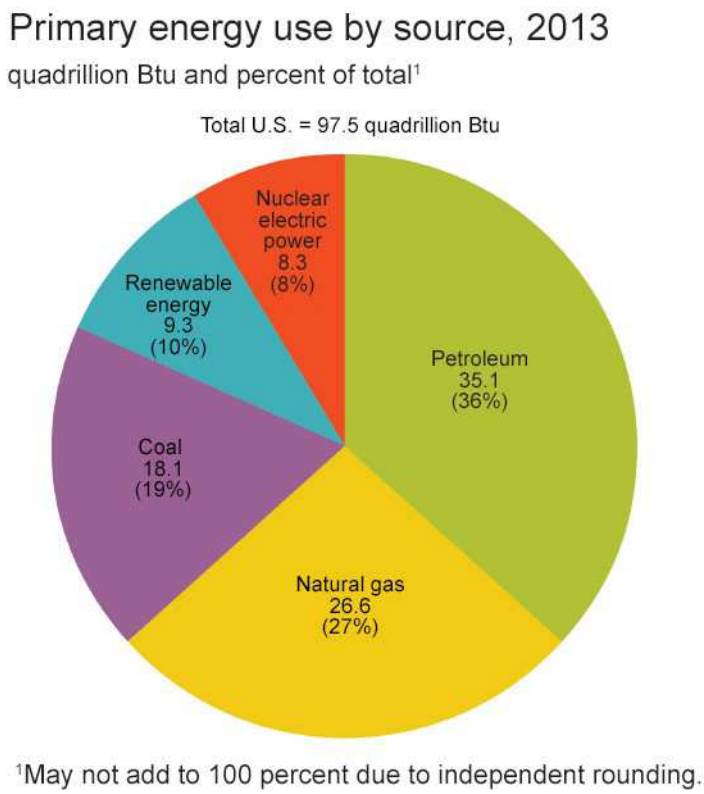

Figure 1.1: A recent graphic showing energy use by fuel source for the United States. Source [1].

It is well known that the combustion of these fuels produces pollutants. Notable examples include sulfur and nitrogen dioxides, and heavy metals such as mercury. A waste product that has been getting considerable attention lately is carbon dioxide.

This gas is one of the major products that results from the combustion of these fuels. The reason for this attention is that carbon dioxide is a greenhouse gas. Recent scientific evidence suggests that the emissions of this gas may be a key player in observed changes in the global climate. In addition to changes in climate, notable phenomenon such as receding glaciers and unusually violent storm systems have been recorded in recent years. Many scientists claim that the continued emission of carbon dioxide is a major motivator behind these events. The fossil fuels themselves are the results of a million year natural process making them non-renewable resources. Different estimates are offered as to the remaining reserves but it is safe to assert that eventually extraction may become too complicated and/or costly. These reasons suggest that it would be prudent to find means to conserve these resources. One mean is by exploring alternative forms of electrical power generation.

There are numerous available alternatives of which solar energy is an option. The basic premise of solar energy is to capture some of the radiation which travels from the Sun and convert it into electricity. The fuel source is free and readily available. The Sun is available constantly and it's radiation and will continue to be available for a considerably long time (some scientists estimate a remaining solar lifespan on the order of billions of years). Therefore, concerns about running out of solar fuel are far from paramount. Generating electrical energy from solar energy whether by photovoltaic cells or through heat engines do not result in the emission of greenhouse gases.

The abundance of solar energy makes it a very appealing choice for electrical power generation. The potential benefits not only to us but to the environment make pursuing a design problem in solar energy a worthwhile task. As will be discussed in the following section, current techniques for taking advantage of the Sun's power are far from perfect with plenty of room for scientists and engineers to suggest improvements.

1.3 Design Problem and Background

This thesis presents a possible alternative solution to an issue encountered when using photovoltaic cells to produce electricity from the Sun. This section will discuss the problem that this thesis will address.

A photovoltaic cell is a semiconductor device which produces current when struck by sunlight. The architecture of the photovoltaic cell resembles a diode. The voltage current relationship for a solar cell has been defined by others and is repeated below in its simplest form.

$$I = I_{short} - I_{dark} * \left(e^{\left(\frac{V}{V_{thermal}}\right)} - 1 \right) \tag{1.1}$$

Where I_{short} is the current seen when there is no potential difference across the cell, I_{dark} is the observed current even the solar cell is in total darkness, and $V_{thermal}$ is a constant called the thermal voltage.

The specifics on the derivation of equation 1.1 is beyond the scope of this thesis. The value of I_{short} depends on the solar radiation which strikes the cell. Scientists have determined a quantitative relationship between the short circuit current and the solar radiation striking the cell. The equation is now presented:

$$I_{sc} = I_{sc0} * \frac{L}{1000} \tag{1.2}$$

where I_{sc} is the short circuit current actually produced, I_{sc0} is the short circuit current produced when the solar radiation is 1000 $\frac{W}{m^2}$ and L is the solar radiation in $\frac{W}{m^2}$.

The temperature also will affect the yield from the photovoltaic cell. In this model, this is accounted for with the thermal voltage quantity. The thermal voltage in 1.1 is defined as:

$$V_{thermal} = \frac{kT}{q} \tag{1.3}$$

Where k is Boltzmann's constant, T is the temperature in degrees Kelvin and q is the charge of an electron.

Scientists have developed mathematical constructs which more accurately describe the temperature effects. For the purposes of this thesis, usage of the simplified ideal model will be sufficient.

A graphical visual obtained from the literature displays how temperature and radiation can impact solar cell performance is available in figure 1.2.

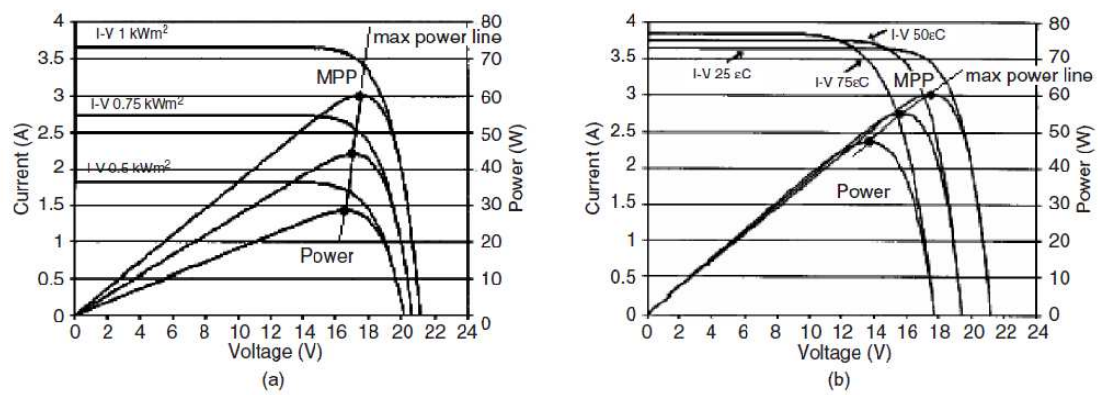

Figure 1.2: Several representative plots for a solar source showing temperature and radiation effects. Left hand image shows the effect of radiation and the right hand image shows the temperature impact. Power and current as a function of voltage are presented. Source: [2].

The point of this discussion and figure 1.2 is to emphasize the fact that a photovoltaic cell is not a constant source of electrical power. Several factors will affect the yield from the cell. Several of these, most notably radiation level and temperature, will fluctuate in actual use of the solar cell. Common occurrences such as passing

clouds or dust collection on the surface of the photovoltaic cell can affect the power yield.

It is preferable to have a source which produces a constant, expected power value. By itself, a photovoltaic power source does not meet this preference.

It was discovered that placing a power electronics circuit (specifically a DC to DC converter) between the solar cell source and a load can make using a solar source more viable. By varying the switching pattern in the power electronic circuit, the load seen by the solar cell can change. In paper [10], the authors present observed impedance relationships for common DC to DC converters.

For the buck converter as stated in paper [10]:

$$R_{eff} = \frac{R_{load}}{D^2} \tag{1.4}$$

For the boost converter as stated in paper [10]:

$$R_{eff} = (1 - D)^2 * R_{load} \tag{1.5}$$

For the buck-boost converter as stated in paper [10]:

$$R_{eff} = \left(\frac{1 - D}{D}\right)^2 * R_{load} \tag{1.6}$$

In equations 1.4, 1.5 and 1.6, D is the current duty cycle and R_{load} is a resistive load. Paper [10] models assume resistive loads.

Being able to adjust the effective load observed by the solar cell permits one to adjust the operating point of the solar cell. This can improve the yield from the solar cell by having the operation move towards the maximum power point. The maximum power point refers to an operating voltage and current which produces the highest power possible from the cell (please see figure 1.2 for visual examples of this behavior). Every photovoltaic solar source has this behavior and as the solar cell behavior is affected by external factors, the required operating voltage and current to operate at the maximum power point changes as well.

Directing the power electronics circuit to present an effective load to the solar cell which forces it to perform at the maximum power point is the duty of what is called a *maximum power point tracker*. At the basic level, a maximum power point tracker is simply a switch controller. It typically requires one or more feedback variables in order to adjust the switches to reach the maximum power point. The performance benefits of using this converter controller arrangement have been demonstrated numerous times in the literature. Several control algorithms have also been developed and demonstrated in the literature. Despite this, there are still plenty of avenues for new research.

1.4 Stargrazer One

This thesis proposes a maximum power point tracking control for a switched capacitor power electronics circuit for the scientific community. This system is built with

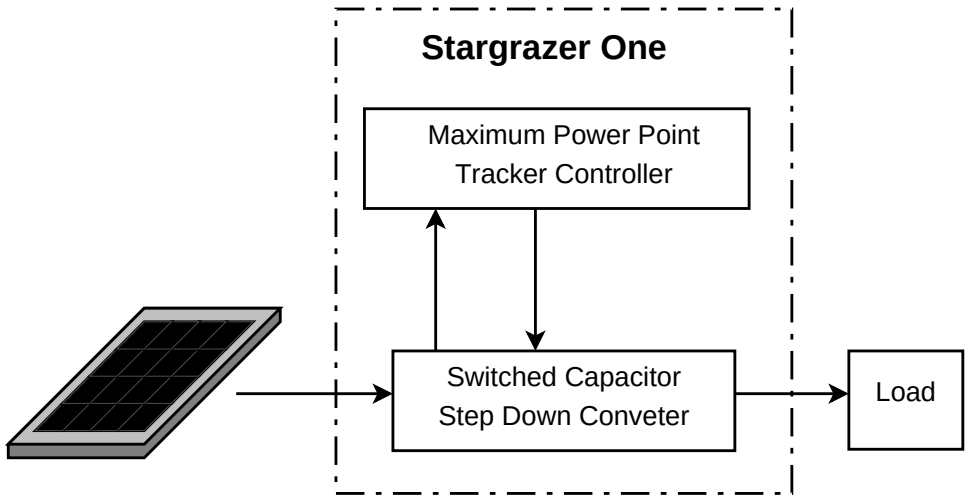

Figure 1.3: A visual, high level representation of the complete Stargrazer One maximum power point tracking system. The components enclosed in the dotted line box are designed and tested in this thesis.

emphasis on power consumption, simplicity and size. This proposed system is called "Stargrazer One". A visual presentation of this proposed system is in figure 1.3. These listed motivators were behind these design goals:

- For solar panels, more notably large arrays of solar panels, it is possible to have conditions where a portion of the solar cells sees diminished solar radiation. This can present difficulties in maximum power point tracking. There are several proposed solutions ranging from elaborate software programs which permit a single tracker to handle this situation to placing multiple trackers across the solar cell source for more localized control. Stargrazer One is an implementation for the latter solution. Stargrazer One was designed with the intention that it could be instantiated multiple times inside a solar array. Stargrazer One was built with the intention of not only serving an entire solar panel but possibly working with an individual or a small string of solar cells. At this localized level, the likelihood of encountering a drop of the solar radiation across a part of the solar source being serviced is greatly reduced. This facilitates the simplification of the control mechanism.

- The maximum power point tracker requires electricity in order to operate. This will likely be from the solar cell source. Therefore, power is being lost in the power point tracking circuits. It is best to minimize this as much as possible. Therefore, Stargrazer One is a specialized system. Only the circuits required to execute the control of the power electronic circuits are present. This arrangement will go far to minimize the required energy that this circuit will require to perform its tracking duties.

These motivations were taken into consideration in choosing the particular algorithm to track the maximum power point and the selection of the power electronic

device amongst other key decisions. The following presents what Stargrazer One is. Please note that this listing will present potentially unfamiliar terms, these will be explained in detail in the appropriate thesis section:

- Stargrazer One refers to the control architecture and power electronic circuit used to implement the maximum power point tracking for a solar source (see figure 1.3).
- The control architecture is a customized digital architecture specialized for the duty of maximum power point tracking. The architecture shall:
  - Implement a form of the perturb and observe maximum power point tracking algorithm. The algorithm has been tuned with the intention of simplifying the architecture
  - Accept voltage readings from the power electronic circuit and adjust the time the transistors are on (or "on times"). Voltage and transistor on times will be the feedback variables.
- The power electronic circuit chosen is a step down switched capacitor converter. This architecture was selected due to the ability to miniaturize this type of converter using modern fabrication methods.

It is the intention and desire of this author that this proposed design be adapted for more uses and even improved upon. Possible directions for new research will be presented at the end of this document.

1.5 Thesis Content

The purpose of this final section is to inform the reader the contents of the thesis. This thesis will be divided into parts with each one deals with an important aspect of the design of Stargrazer One. The following listing presents in brief what each chapter will contain:

- Part I : This chapter presents the results of the major literature surveys conducted over the course of preparing this document. The objectives of the literature surveys were twofold. They are to determine the uniqueness of this idea and to make informed decisions regarding how Stargrazer One should be designed. The chapter is divided into sections each of which addresses a particular question posed for literature study.
- Part II: This part analyzes the power electronic converter used in Stargrazer One. The design is unique and a firm understanding is essential in order to successfully design Stargrazer One. Voltage models are developed for the power electronic converter. Also, its performance is examined. This part presents suggestions for a designer to use this type of power electronic converter.

- Part III: This part presents the control architecture for Stargrazer One. After introducing the entire circuit, the part will discuss the topology piece by piece. The architecture is discussed and simulated validation is presented.
- Part IV: This part presents a physical implementation of Stargrazer One. This implementation is described and experimental results presented.

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Part I

Survey of the Literature

Chapter 2 Introduction and Purpose

Introduction

As stated in chapter 1, other scientists have explored the maximum power point tracking problem. Other scientists have proposed control algorithms and even presented possible systems. Several of the scientists have published their work in the various journals and conferences for the electrical engineering profession. The available literature presents an excellent opportunity to gain an in-depth understanding of the problem that this thesis is to address. Perhaps more significantly, the literature was an invaluable source for inspiration and suggestion to further enhance the uniqueness and viability of Stargrazer One. Strategic consultation of the literature provided the information needed to address important questions on how Stargrazer One is to be designed. The purpose of this chapter is to present the findings of the most significant literature surveys done for this thesis. Also included will be a description of the procedure used to filter through the vast quantity of available information.

In creating the Stargrazer One system, the literature was consulted for two general purposes which are now listed below:

- During the development of Stargrazer One, several important decisions needed to be made. In order to choose the appropriate pathway to satisfy the design goals of Stargrazer One an informed decision was prudent and essential. The purpose of the subsequent literature surveys was to obtain information on possible options for the design choice in question. Armed with this information, it was possible to select an appropriate choice for Stargrazer One for each question.

- In order to have a Stargrazer One be a contribution to the scientific community, it must be determined if the proposed design is unique. As the literature includes proposed maximum power point tracking devices created by other scientists, answering this question is best done by an appropriately planned literature survey. This is what was done in this thesis.

Chapter Contents

This chapter will present the most significant questions which required an aggressive examination of the available scientific literature to answer. Each section will address an individual question. Each section will state the literature sources explored, present notable findings from the literature and present the answers found for the particular question under examination. The following list presents the contents for this chapter:

- Section 3 will address the questions: What is the current state of the technology? Are their other implementations like Stargrazer One?

- Section 4 will address the question: are switched capacitor solar cell maximum Power point trackers are commonplace?
- Section 5 will address the question: which maximum power point tracking algorithm should Stargrazer One use.
- Section 6 is related to the previous section (section 5). However, the question posed merits its own section. The question is: How to tailor the chosen tracking algorithm for Stargrazer One. The objectives are balancing performance with the goals of Stargrazer One.

Chapter 3 Current Maximum Power Point Tracking Technologies

Introduction

As stated in chapter 1, Stargrazer One is to be a maximum power point tracking system which executes the perturb and observe algorithm using a special purpose digital architecture. The plant for this control system will be a switched capacitor power electronic converter. In order for Stargrazer One to be acceptable as a contribution to the scientific community, it must be determined if this system has been produced elsewhere. Therefore, before Stargrazer One was designed, an extensive survey of the scientific literature was taken. The objective was to validate the uniqueness of the Stargrazer One design concept. This section will present the results of this survey. It will begin by setting the scope of material covered, notable observations in the literature will be reported, and this section will conclude by presenting conclusions.

Scope of Survey

This survey was confined to examining conference papers, journal articles and patents. The time frame of the survey is from 1980 to the present. It was possible to access the computer databases of the IEEE and those of the Thompson Routers "Web of Knowledge". Patent searches were facilitated with the SumoBrain Solutions Company's patent search data base known as FreePatentsOnline.com. The time frame of this survey was from 1981 to 2011. Details on the procedure used to execute this survey are available in appendix 15.3.

Notable Findings

In examining the body of literature collected, a notable observation was made. There were what appeared to be two general directions of hardware implementations for solar cell maximum power point trackers. A majority of papers presented power point trackers which were either custom analog circuits, or a digital solution using a programmable general purpose processor. Due to the extensive results obtained, an exhaustive listing of the power point trackers built in these manners will not be included. However, an illustrative sampling of documents will be presented. Each paper will be discussed individually. Complete title information is available in the bibliography section.

Examples of Programmable General Purpose Processor Implementations

- In paper [11] (Optimized Digital Maximum Power Point Tracker Implementation for Satellites by A. Ramamurthy et al), the authors develop a maximum power point tracker for use in satellites. The specific algorithm selected is perturb and observe (same as the choice for Stargrazer One). The tracking algorithm is physically implemented using a commercially available programmable

processor [11]. The authors specify the processor type as a Texas Instruments TMS320F2808 [11].

- In paper [12] (Adaptive digital MPPT control for photovoltaic applications by Cabal C. Alonso et al), the authors present a digital implementation for a maximum power point tracking technique called extremun seeking control. What is of relevance to this discussion is the fact that this algorithm is ultimately implemented into a commercially available processor [12]. The authors specify the type which is a PIC18F1220 [12].

- In paper [13] (Study of Different Implementation Approaches for a Maximum Power Point Tracker by Boico, F et al), the authors present a study on different implementations of the perturb and observed algorithm [13]. In all cases the algorithm is implemented inside a programmable processor [13]. The authors specify the processor as a PIC18F452 [13]. The different implementation approaches summarize as modifications to the control variable to be adjusted [13]. One approach uses the duty cycle as a control variable [13]. This technique was ultimately selected for Stargrazer One [13]. The other two approaches use the operating voltage of the solar panel [13]. The differences in the implementations for these two are that one case requires analog components while the other uses more processor resources [13].

- Paper [14] (Combined Low-Cost , High-Efficient Inverter, Peak Power Tracker and Regulator for PV Applications by Enslin, J.H.R. et al) presents an early proposal for a complete solar energy system [14]. The selected algorithm for maximum power point tracking is perturb and observe [14]. The specific variant is called hill climbing [14]. Again the hardware is a programmable processor specified by the authors as an 8031 microprocessor [14].

- What makes this paper interesting is that the authors present a solar power system that serves a single cell [15] (A Single Cell Maximum Power Point Tracking Converter without a Current Sensor for High Performance Vehicle Solar Arrays by L.Tang et al). Stargrazer One is designed with the intention of possibly being utilized in this manner [15]. The algorithm selected by the authors is a variant of perturb and observe [15]. The control algorithm is physically implemented in a commercially available processor [15]. The authors specify the processor as a MSP340 [15].

Examples of Analog Implementations

- Paper [16] (Dynamic Maximum Power Point Tracker for Photovoltaic Applications by Midya P. Krein et al) is an early implementation of a maximum power point tracking technique called ripple correlation control. The implementation is bulky involving several commercially available multipliers, operational amplifiers and a pulse width modulator IC [16].

- In paper [17] (Single-loop maximum power point tracker with fast settling time by il-Song, Kim et al), the maximum power point tracking method proposed by the authors involves the conductance. The resulting hardware consists of a specialized analog circuit [17]. What was notable is that they presented a customized solution for the drive signals for the converter switches [17]. The implementation was accomplished with a digital gate and a D flip flop [17]. Produced control signals were converted into digital forms using comparators [17]. Such arrangements where computation is done in analog and the switch output signals are generated with digital gates was encountered several times in the course of this survey.

- Paper [18] (Design of a Solar-Harvesting Circuit for Batteryless Embedded Systems by Davide Brunelli et al) is an example of the potential simplicity analog systems offer. The authors implement a version of the fractional open circuit voltage method [18]. The control mechanism consists of a single analog comparator [18]. The inputs are the panel voltage and a properly scaled voltage from a pilot cell [18].

- In paper [19] (Stand-Alone Photovoltaic Energy Storage System With Maximum Power Point Tracking by V. M. Pacheco), the authors proposed a maximum power point tracking technique which uses the voltage and power derivatives [19]. Of relevance to this discussion is that the resulting circuitry is a similar flavor to paper [17]. Driving the power electronic circuit switches required digital gates [19].

- In paper [20] (A simplified analog control circuit of a maximum power point tracker by Kung-Yen Lee et al), the authors present a version of the perturb and observe power point tracking technique implemented in analog circuitry [20]. All computation is executed in the analogue domain [20]. Driving the switches in the power electronic circuit is accomplished with a JK flip flop where the J and K inputs are controlled by appropriate signals [20]. The selected control variable is the duty cycle [20].

As stated before, in the area of solar cell power point tracking, these two implementations styles were prominent. There are scientists whose work was of particular interest for this thesis. The most significant literature found is now summarized. Each paper will be discussed individually. Complete title information is available in the bibliography section.

Relevant Literature

- In paper [21] (A Novel Digital MPPT Control Architecture Renewable System Integration by Muhtaroglu, A), the author presents an alternative to Stargrazer One. It is a digital implementation of the perturb and observe algorithm using only digital functional blocks [21]. The functional blocks include a subtractor, several counters and a custom multiplier [21]. The author placed emphasis on

this multiplier and, admittedly, the role the other functional blacks played was not readily clear [21]. However the circuit is supposed to perform the version of perturb and observe which uses the duty cycle as the control variable [21]. The author also stated that the system will require the voltage and current measured from the solar cell [21]. A physical prototype was implemented in a field programmable gate array [21]. As is demonstrated in this thesis, Stargrazer one is significantly different then this architecture.

- Paper [22] (A new Maximum Power Point Tracking system by W.J.A. Teulings et al) is an older article that presents a perturb and observe maximum power point tracking system for solar cells in space [22]. What made this article of extreme relevance is the implementation of the maximum power point tracking algorithm [22]. The power comparison along with a portion of the control variable adjustments is in the digital domain [22]. These digital tasks are carried out with only simple functional blocks [22]. The power comparison uses a digital comparison unit for the operation and a register to hold the previous power value [22]. The result of this comparison is fed into a JK flip flop which directs a counter in which direction to increment [22]. This comparison architecture is perfectly suited for the needs of Stargrazer One [22]. This architecture is adopted by Stargrazer one to execute the power comparison. Like this article, to implement the control variable adjustments, a counter and a T flip flop will be required. Unlike this article, the entire system will be digital.

- What made paper [23] (Switched Capacitor DC-DC Converter Based Maximum Power Point Tracking of A PV Source for Nano Satellite Applications by Agarwal V. et al) qualify for this classification is the authors' use of a switched capacitor power electronic converter [23]. This was not considered for the developed Stargrazer One system in this thesis until this paper was encountered. Such a converter presents a means to miniaturize Stargrazer One further. The step down switched capacitor converter used by these authors will be investigated and adopted for use in Stargrazer One.

- Paper [24] (V2-based power tracking for nonlinear PV sources by Veerachery M. et al) presents a method of power point tracking which uses voltage and duty cycle [24]. The discussion is very detailed. Incoming power is computed by applying the Watt's law variant which is: [24]

$$P = \frac{V^2}{R} \tag{3.1}$$

  Where R is a function of the converter duty cycle and output resistances [24]. As presented in this thesis, an alternative power computation method which only requires voltage is used in Stargrazer One. This article is in this listing because it is a precedent and was highly useful in developing the chosen method for Stargrazer One. The technique proposed in this thesis is acceptable for the type of switched capacitor power electronic circuit used. It may also be

possible to adapt the same procedure for other types of switched capacitor power converter with or without modification. Papers like this one can help facilitate this adaptation.

Implications for the Developed Stargrazer One System

As of writing this section, Stargrazer One remains a valid contribution to the scientific knowledge in the area of maximum power point tracking for solar cells. The survey clearly demonstrates that the proposed design of the Stargrazer One power point tracker is unconventional. Only a few authors have put forward similar designs.

It is important to emphasize that this assertion of uniqueness applies to solar cell maximum power point trackers only. Designers of power systems for thermoelectric or piezoelectric systems, which also require maximum power point trackers, have presented solutions consisting of digital functional blocks. Paper [25] is one such example. In this article the authors present a perturb and observe algorithm which is implemented with just digital and analog functional blocks [25]. The scheme requires a current sensor and drives a conventional power electronic converter [25]. Other examples probably exist. The emphasis was on solar cell maximum power point trackers as this is the intended application for Stargrazer One.

The discovered relevant articles, besides being helpful to determining the present state of affairs, presented further means to make Stargrazer One more distinct. Very few solar cell maximum power point trackers use switched capacitor converters. As will be demonstrated later, there are performance limits to these converters which may have driven many scientists from considering them. Despite this, there are still useful applications for these converters. Therefore, Stargrazer One presents an additional option to scientists who decide to use switched capacitor converters. The literature also presented other innovations which would benefit Stargrazer One, for instance, the concept of dispensing with the current sensor as presented in paper [24].

Chapter 4 Survey of Uses of Switched Capacitor Power Electronics In Photovoltaic Maximum Power Point Tracking

Introduction

Stargrazer One uses a switched capacitor architecture for the power electronics. The use of a switched capacitor power electronic converter for Stargrazer One was not originally planned. During the course of determining the uniqueness of the Stargrazer One control circuit concept, paper [23] was encountered. This paper describes a maximum power point tracker for a satellite solar system [23]. The tracker is implemented with the satellite's central computer and involves numerous input variables [23]. What is of note is the use of a step down switched capacitor power electronic converter. The authors claim that this is the first instance of the use of this type of power electronic device for this application.

The purpose of this paper is to present the findings of a survey to see if other instances of solar cell maximum power point trackers have been developed which use a switched capacitor converter for the power electronics.

Procedure

The procedure for this survey is similar to the procedure outlined in section 3 but only the time from year 2000 to present was performed. Patents were not included in the analysis. Dates before year 2000 were found to yield no relevant results.

Results

Only a few relevant papers were found. Some examples are now presented:

- Paper [26] presents a solar power system which uses a type of switched capacitor converter known as a charge pump. Different conversion ratios are obtained by selective switching of the transistors in this device [26].

- A recent paper presents a maximum power point tracker which uses a step up switched capacitor power converter [27]. The authors use a sampling capacitor to obtain the necessary data, which is voltage [27]. This presents a possible starting point for adapting Stargrazer One to other types of switch capacitor converters. The authors also seem to use a very similar technique to determine the power [27]. The procedure was not explicitly defined in the article. However, it was noted that they do use the voltage oscillation within the converter to determine the energy passing through the system [27]. This same approach is used in Stargrazer One. Despite this, the algorithm implemented is very different from Stargrazer One [27]. The authors do not explain the algorithm in great detail. The technique appears to adjust several different items [27]. Stargrazer One simply adjusts the duty cycle of one of the converter transistors in accord with the perturb and observe algorithm. This paper presents an

algorithm which adjusts the converter's step down ratio, switching transistor sizes, gate voltages and the switching frequency [27]. How it is determined what to adjust and when is not specified [27]. The authors mention the need of a look up table [27]. The majority of the system appears to be in the analogue domain [27]. Stargrazer One shall be mostly in the digital domain. Therefore, it can be said that Stargrazer One will still be a unique contribution to the body of knowledge.

Implications for Stargrazer One

Clearly, other scientists have designed maximum power point trackers for solar cells using switched cpacitor power electronics. The developed systems different from the developed Stargrazer One maximum power point tracker. It is safe to assert that Stargrazer One will offer an alternative design for those wishing to use switched capacitor power electronics in solar cell applications.

Chapter 5 Survey of Maximum Power Point Tracking Algorithms

Introduction

One important design choice for Stargrazer One is which maximum power point tracking algorithm the hardware should execute. Should an already defined solution be used or does a new one need to be developed? This section addresses this very important question. The section opens with a summary of findings obtained during a survey of the technical literature. Then the discussion will present the algorithm chosen for Stargrazer One with justification.

Literature Survey Results

The purpose of this investigation was to see which solutions to the maximum power point tracking problem have been presented by other scientists. Considerable time could be saved by using an already tried and proven method. The focus of this study was on simple methods that could be accomplished without the resources on a general purpose programmable processor. This section will present the findings of this investigation.

Candidate Solutions

During the survey, it was found that several studies have been done across multiple algorithms. These documents facilitated the learning process. Some works even offered side by side comparisons in performance which was very helpful. Thanks to the survey, it was possible to narrow the scope of study to a few algorithms. They are now presented in list format

- **Fractional Open Circuit Voltage**

  This method is an approximation technique of maximum power point tracking [28]. It takes advantage of a discovered property that open circuit and maximum power point voltage maintain a directly proportional relationship [28]. This constant of proportionality is dependent on the solar cell used [28]. The estimation of the maximum power point voltage is found by using the following [28].

  $$V = K * V_{open} \tag{5.1}$$

  Paper [28] also presented another version of this technique which used the short circuit current.

- **Perturb and Observe**

  This technique appears as a systematic method of guess and check. A control variable is incrementally adjusted according to the present power conditions of the solar source [28]. If the algorithm sees improving results, the control variable will be incremented in the same direction [28]. If the power drops the direction of control variable adjustment switches [28]. Paper [28] cites two examples of valid control variables which are the duty cycle and operating voltage of the solar panel.

  Paper [3] suggests that this algorithm is relatively low cost. Paper [3] defines cost as the monetary costs of the controller and sensors. The authors assume a physical implementation for this algorithm using a programmable general purpose processor [3].

  Paper [28] presents the major disadvantages of this algorithm. This algorithm continuously adjusts the control variable[28]. Therefore once the algorithm has found the maximum power point it will continue to execute and perform adjustments [28]. Therefore, the system will dither around the maximum power point resulting in some loss [28]. Paper [28] also discussed another issue. This algorithm may be temporarily fooled into adjusting away from the maximum power point during rapid radiation changes [28].

Paper [28] and other similar documents presented other algorithms. Examples include incremental conductance, fuzzy logic control, ripple correlation control, etc. These techniques require significant amounts of computation and / or computer resources. For example, fuzzy logic requires a look up table (sometimes called the "rule table") and appropriate hardware to implement the fuzzification and defuzzification processes [28]. Therefore these algorithms are not ideal for Stargrazer One and were not studied any further.

Stargrazer One Power Point Tracking Algorithm

It was decided to use an existing algorithm. Of the viable choices, the perturb and observe technique was selected. This decision was not taken lightly and is the result of literature investigations. Relevant findings are now presented.

Paper [3] presents a strong case in favor of using this algorithm. The authors created a series of input vectors representing solar illumination and computed the ideal energy yield of for each test vector [3]. Each algorithm the authors decided to examine was then subjected to these input vectors and the energy yield reported [3]. The results were presented in a table repeated in figure 5.1 [3].

The authors examined three variants of the perturb and observe method [3]. The variant labeled "P&Oa" is the simplest with constant adjustments to the control variable. The authors build upon this model with modifications to the basic algorithm in "P&Oa" to create "P&Ob" and "P&Oc". For the experiment in [3], all techniques of perturb and observe achieved an energy yield of over 85 percent, with the simplest approach achieving almost 99 percent yield [3]. The other methods of perturb and

observe presented, with the exception of one, performed very well [3]. Other authors performed similar examinations. One example is paper [29] where a procedure similar to paper [3] is applied to a perturb and observe implementation and three other algorithms. The perturb and observe algorithm achieved an efficiency rating of above 95 percent [29]. The authors use a fix control variable adjustment technique [29].

Closing Remarks

This evaluation of the literature suggests that using perturb and observe is a good choice to meet the requirements of Stargrazer One. The exploration revealed several other interesting algorithms each with their own merits. The fractional approximation methods, while simple, do not actively track the maximum power. The perturb and observe method does this active tracking without adding significant complexity. The alternative methods require much more computation and were therefore dismissed as too complicated for Stargrazer One. However, developing a compact solution for these other algorithms could permit their use in a Stargrazer One system. This is a topic best left for future research.

TABLE IV

ENERGY GENERATED AS FUNCTION OF MPPT TECHNIQUE AND IRRADIANCE INPUT

Input	IDEAL [J]	CV [J]	SC [J]	OV [J]	P&Oa [J]	P&Ob [J]	P&Oc [J]	ICa [J]	ICb [J]	TG [J]	TP [J]
(a)	1711	1359	1539	1627	1695	1707	1490	**1708**	**1708**	1562	1681
(b)	1785	1410	1687	1700	1774	1781	1558	**1782**	**1782**	1643	1761
(c)	1481	1192	1337	1403	1465	1476	1301	**1478**	**1478**	1311	1424
(d)	1633	1290	1492	1552	1625	**1628**	1416	**1628**	**1628**	1476	1589
(e)	1785	1403	1659	1699	1769	1780	1543	**1782**	**1782**	1643	1762
(f)	1711	1363	1636	1630	1692	1697	1508	**1709**	**1709**	1563	1683
(g)	1633	1298	1351	1552	1617	1627	1432	**1630**	**1630**	1477	1593
(h)	1482	1204	1397	1409	1441	1431	1311	**1479**	**1479**	1314	1429
(i)	1711	1360	1519	1630	1701	**1708**	1491	**1708**	**1708**	1563	1682
(j)	540	459	427	479	524	**525**	515	469	503	397	444
(k)	1160	888	893	872	1126	**1150**	986	1116	1126	1078	1146
(l)	1558	1248	1388	1478	1542	1553	1370	**1555**	**1555**	1395	1510
Total	18189	14465	16324	17031	17971	18063	15921	18044	18088	16422	17704
%	100	79.5	89.7	93.6	98.8	99.3	87.5	99.2	99.4	90.3	97.3
Classification		10	8	6	4	2	9	3	1	7	5

Figure 5.1: Comparitive study results from paper [3].

Chapter 6 Survey of Perturb and Observe Approaches

Introduction

As discussed in section 5, the perturb and observe method of maximum power point tracking was selected for Stargrazer One. Its minimal computation demands and simplicity made this a wise choice. However, the algorithm is far from perfect. This literature survey revealed that several scientists have attempted to address the shortcomings of this algorithm. They present a myriad of viable options ranging from selecting an optimal step size to executing an algorithm which dynamically adjusts the step size. It would be prudent to examine the work of these scientists with the intention of applying the appropriate improvements to Stargrazer One. Of course, it is important not to forget the goal of simplicity in the design of Stargrazer One. Some solutions, while effective, may be unsuitable for Stargrazer One because they have too much hardware cost. In selecting the optimal version of the perturb and observe algorithm for Stargrazer One, the following was investigated:

- What should the control variable be?
- How should data be sampled?
- What should be perturbation size be?
- Can a dynamic algorithm be used?

Each of these is significant decisions will impact how Stargrazer One is built. In this section, each one will be discussed individually.

Control Variable Choice

During the examination the literature, two choices for the control variable appeared predominantly. They were the duty cycle or solar source operating voltage. Paper [4] presents a comparison study between the two particular control variable choices. The authors develop a simulation model for an entire solar cell power system [4]. The authors carefully designed the two candidate algorithms so that they behave similarly [4]. While not explicitly stated, the authors do note that they designed the step sizes so that in steady state the oscillations would be identical for both algorithms [4] . This resulting model was subjected to changes in sunlight [4]. The sunlight changes were modeled as abrupt step changes [4]. Figures 6.1 and 6.2 presents the results of this study.

The results clearly demonstrate that with voltage as the control variable, the tracker has a faster response with fewer voltage transients as opposed to the design with duty cycle as the variable [4]. The authors attribute the lack of voltage swing to the proportional integral (PI) control element in the implementation that uses voltage as the control variable [4].

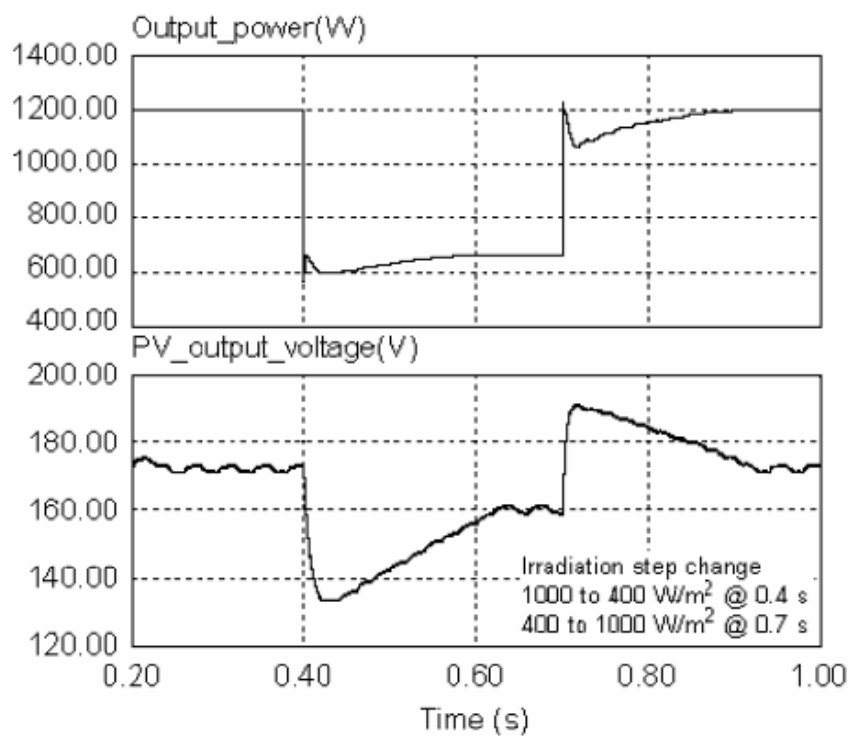

Figure 6.1: Study results of paper [4] for the case of perturb and observe with duty cycle as the control variable. Note the use of step transitions in the test.

Decision for Stargrazer One

Given this rather convincing argument in favor of using voltage as the control variable, it was decided to instead use the duty cycle as a control variable. Two major factors contributed to this selection.

The first item is simplicity. The duty cycle approach does not require the insertion of a PI element in order to function [4]. This means that if voltage were to be used, additional hardware would have to be added to the Stargrazer One implementation. Admittedly, a PI element could be integrated into the design of the Stargrazer One digital hardware. However, additional complexity would still be introduced.

In this study the authors use a step model for the illumination on the solar cell [4]. In reality changes can be very fast but cannot be instantaneous. This study still is very valid because it is known that under rapid sunlight changes the perturb and observe algorithm can be fooled into incorrect operation. The solution these authors present is to use the more complex voltage control variable design they present [4]. However, it was found that through careful selection of design choices it may be possible to make Stargrazer One resistant to a large range of possible solar radiation change rates. Other papers encountered during this survey presented recommendations for these design choices.

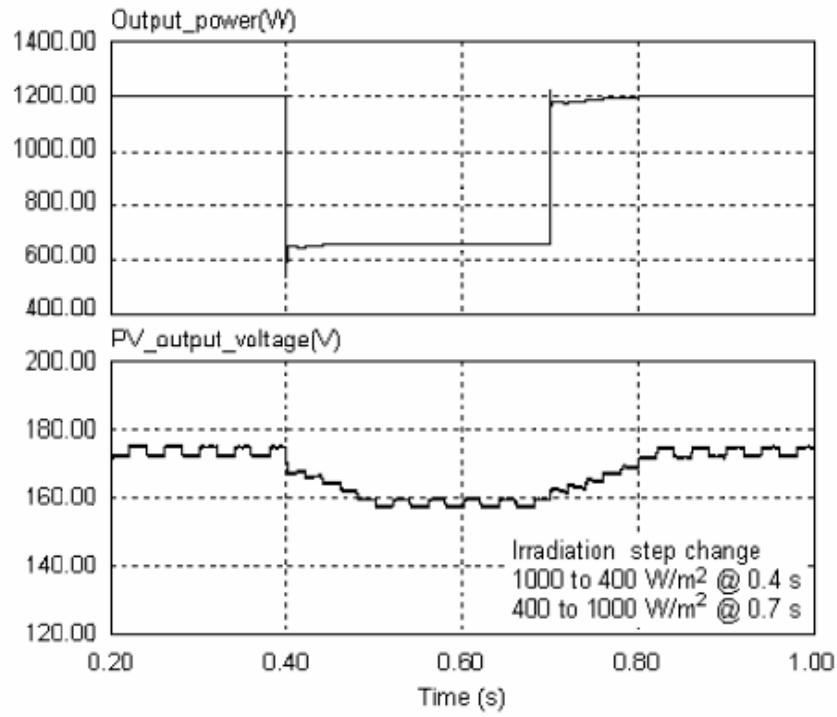

Figure 6.2: Study results of paper [4] for the case of perturb and observe with voltage as the control variable. Note the use of step transitions in the test.

Data Acquisition Method

In paper [5], the authors present a perturb and observe method which uses the current as the control variable. This paper is very relevant to this study because the scientists present several design suggestions which may simplify Stargrazer One considerably. The first notable suggestion is to take a single instantaneous data sample for a computation [5]. The authors claim that the majority of implementations use averages of the data values [5]. The authors state that the main disadvantage of this is slow action [5]. The authors suggest that taking one instantaneous sample per computation of power is sufficient[5]. They go on to assert that two instantaneous power readings from two consecutive converter cycles should be sufficient to determine the direction of adjustment for the next cycle [5].

It is important to note that the authors also suggested when samples should take place [5]. However, this applies to only a conventional power electronic boost converter with a selected control variable of current [5]. Therefore these suggestions while noteworthy are of no help to designing Stargrazer One.

The authors also presented recommendations as to the speed of samples [5]. The authors do not specify a specific recommendation but the logic behind their choices has value [5]. The authors adopt a rapid adjustment speed [5]. Essentially, the rapid sampling frequency is to contend with the issue of this particular algorithm becoming confused under conditions of rapid change [5]. The authors justified the validity of this recommendation using the case of the increasing sunlight [5]. Under this case,

the yield from the solar source will increase for all operating points [5]. What can occur is that the next power computation made will appear to be an improvement over the previous result due to this increase [5]. Depending on the direction of the perturbation this could cause the tracker to drift away from the maximum power point [5]. If one samples quickly, the effects from increasing sunlight will be reduced perhaps sufficiently to safeguard the power point tracker from incorrect operation [5]. This is visually displayed in figure 6.3.

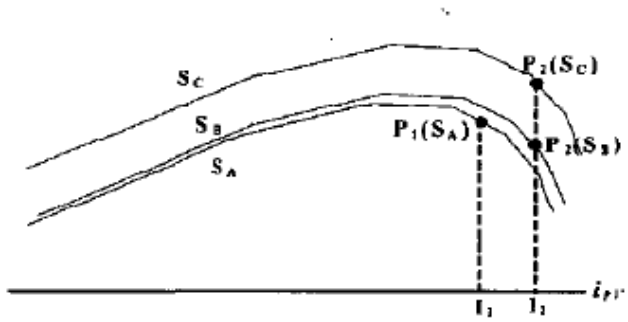

Figure 6.3: A visual demonstration showing how perturb and observe could become confused under rapid changes. A transition from S_a to S_c will result in drift away from maximum power operation. However a transition from S_a to S_b will see a change in direction which will keep operation near maximum power operation. Source: [5].

The authors executed a simulation and experimental validation of the proposed design [5]. It is important to note that the power point tracker was implemented in a digital signal processor [5].

Perturbation Size

Another important factor to consider is the size of the control variable adjustment. Scientists have taken the time to examine the costs and benefits associated with the selection of the control variable adjustment size. The notable example of paper [6] will be used as the perturb and observe implementation will use duty cycle as the control variable [6].

The authors took the time to discuss the tradeoffs that must be made when selecting the control variable size [6]. They determined that a larger size will facilitate rapid response to environmental change but the cost is increased loss under steady state conditions due to the increased amplitude of the steady state oscillations about the maximum power point [6]. The smaller size sees the reverse [6]. The steady state loss is reduced but response to environmental change is increased [6]. The authors do propose a variable step solution which attempts to reap only advantages but, for the purposes of this section, analysis will focus on their studies with fixed duration systems [6].

For the study the authors select steps sizes of .008, .001, and .00001 [6]. It is important to note that the authors do not specify the units for these step size

values[6]. The experiment is conducted using a conventional boost power electronic converter [6]. Converter current and voltage are measured to determine power [6]. The authors subjected the system to a simulated test vector which presents changes in solar radiation [6]. The changes are instantaneous in duration [6].

The authors note that the larger steps size saw increased steady state oscillation [6]. As expected the largest response time to the radiation change was from the smallest step size case [6]. The intermediate condition presented a compromise, the response was reasonable and the steady state oscillation considerably reduced [6]. To explore the ideal step size further, the authors perform an efficiency study [6]. The efficiency metric is defined as [6]:

$$\eta = \frac{P_{pv}}{P_{MPP}} * 100 \tag{6.1}$$

Where P_{pv} is the power from the solar source under test and P_{MPP} is the power at the maximum power point.

Table 6.1: Results of the efficiency study in [6].

Results	
step size	η [in %]
.008	18.8
.001	86.3
.0001	95.3

The authors noted that the efficiency appear to vary as the experiment was performed [6]. Therefore, they reported the worst case results which is reiterated in table 6.1 [6]. This table reveals that the smallest step size achieves the best results [6]. This suggests that Stargrazer One should have a similarly small adjustment [6]. However, since the authors did not designate the units of the step size selected the appropriate small size will have to be experimentally determined. Therefore, Stargrazer One should be designed so that the step size can be adjusted with ease. This is tended to in the appropriate chapter.

Dynamic Perturb and Observe Implementations

The main sale point for this approach is to attempt to dispense with the transient and steady state losses that occur with a fixed adjustment perturb and observe approach. During the course of the literature survey, several authors presented interesting work. However, it was decided to not try an adaptive implementation for Stargrazer One. The obvious reason is to avoid any undue complexity. These adaptive solutions add extra layers of computation and require retention of additional data. Furthermore, the literature suggests that the performance benefits may be mostly gained with a fixed step solution. For instance, operating a small adjustment step solution at a sufficiently rapid speed should give a competitive response.

Impact of Findings on Stargrazer One

As expected, taking the time to explore the literature has provided excellent beginning points for the development of Stargrazer One. The study permitted the selection of the appropriate algorithm control variable, a significant decision that must be made before development can begin. The study offered an opportunity to explore possible options. This permitted a more detailed definition of the particular solution to the implemented. As such, it was determined that a fixed duration perturb and observe method which uses duty cycle would be used in Stargrazer One. With the intent of increasing performance, this algorithm will be run at a fairly rapid pace. To ease complexity, data sampling will be instantaneous with only a single round of the sampling per computation required.

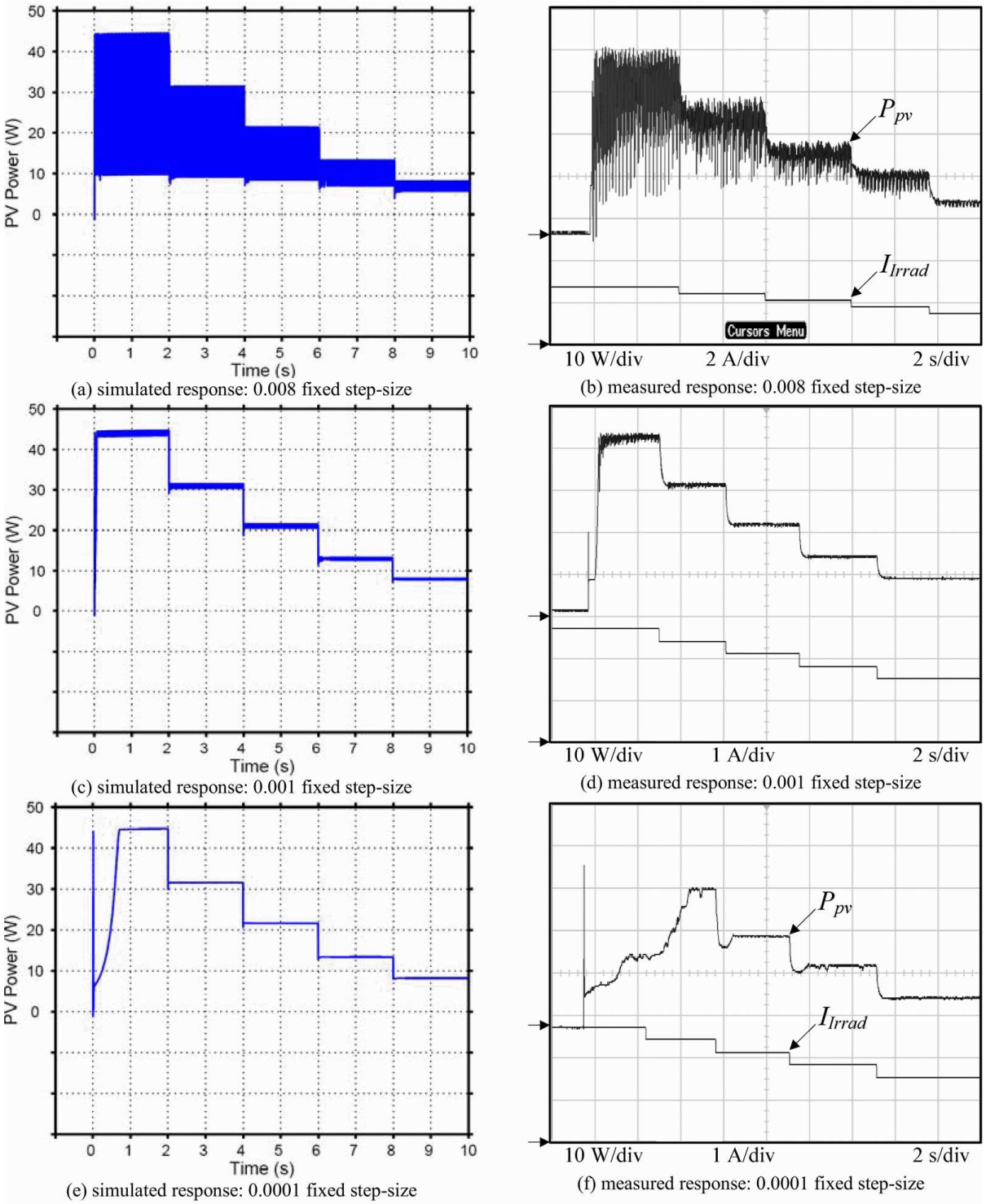

Figure 6.4: Efficiency simulation traces from paper [6]. Plots on the left are simulation results while those on the right are from a physical model.

Part II

Switched Capacitor Step Down Converter For Stargrazer One

Chapter 7 Introduction

7.1 Introduction

An overwhelming majority of the maximum power point trackers proposed in the literature feature power electronics circuits which include inductors. These along with capacitors are needed to filter the voltage and current spikes that take place when the switches change state. Inductors, while useful, are bulky circuit elements. To be able to have a small maximum power point tracker system, the design must be as compact as possible. An option for the power electronics is to use a switched capacitor power converter. These dispense with inductors entirely. The energy storage and filtering is accomplished with capacitors alone. This chapter will present the switched capacitor power converter which will be used in Stargrazer One.

7.2 Converter Description

There are several varieties of switched capacitor power converter in the literature. The selected converter for Stargrazer One was first proposed by paper [30]. A motivation for this choice is the converter's apparent simplicity. Alternatives found in the literature were considerably more complex. The converter proposed in paper [30] is a step down converter. This means that the output will see a value less than or equal to the input voltage. An important note is that paper [30] uses MOSFETs for the switches. The implementation in this thesis will also use MOSFETs for the physical implementation of the switches.

What also made this converter stand out is that one of the circuit topologies (or states) the converter assumes features capacitor C1 open circuited. This presents a very simple way to obtain voltage readings for the maximum power point tracker.

Figure 7.1 presents the states the converter assumes as the switches operate. During State One, capacitor C1 is being charged by the solar source. State two is an intermediate state where capacitor C1 is open circuited. During State Three, capacitor C1 delivers charge to the load. Then the process repeats again starting from State One after passing again through State Two. The period of time that it takes for the converter to complete a single iteration of this described process is a converter cycle.

Figure 7.2 presents an example switching pattern for the converter. At no time are both transistors on simultaneously. The duty cycles for the transistor gate signals can be adjusted as needed. A detailed discussion on the best switching arrangements for Stargrazer One is discussed in section 9.2 and section 13.3.

7.3 Part Contents

The aim of this chapter is to provide analysis of the switched capacitor DC to DC power converter to facilitate the design of Stargrazer One. The work presented in

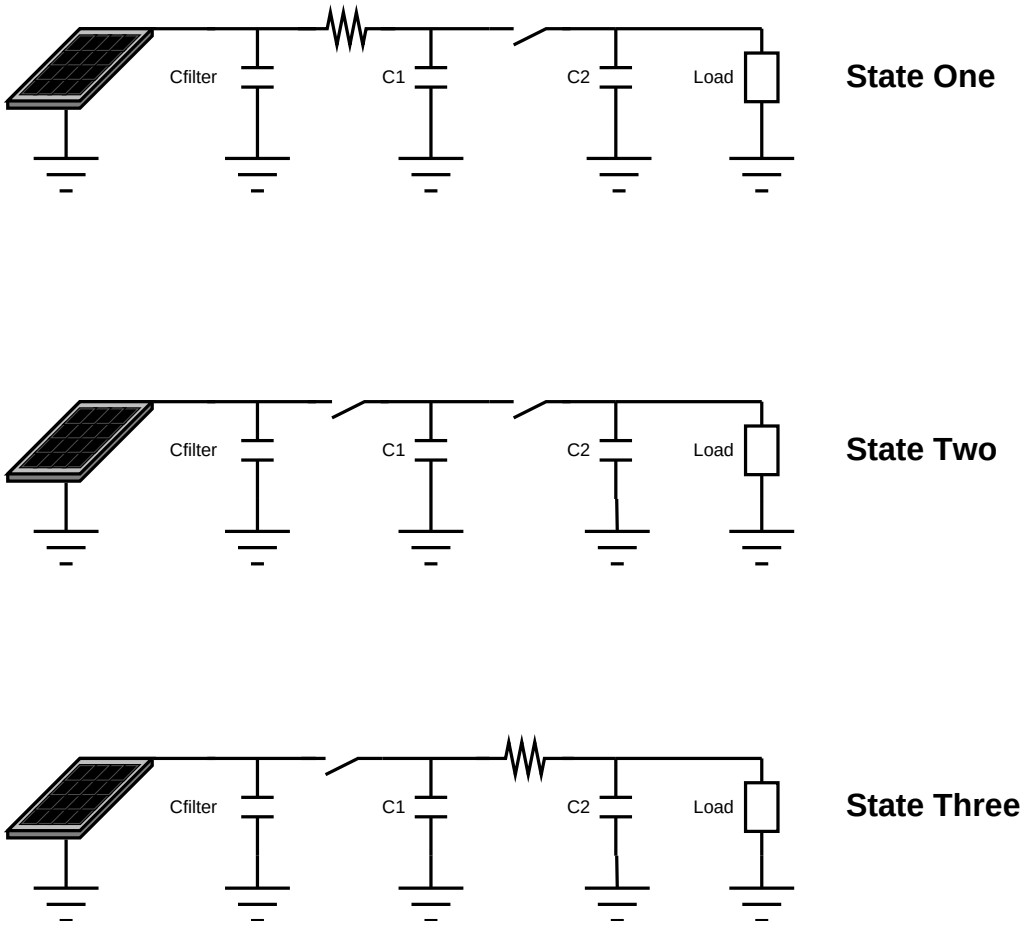

Figure 7.1: The converter states. Capacitors are labeled. Note the use of a switch resistor model for the power transistors.

paper [30], does not cover all that was required to effectively use this converter in this proposed system. Paper [23] uses this converter in a maximum power point tracking application but said little on how this converter was configured. This chapter fills this void by performing an analysis of this converter. As of writing this chapter, the author has found no other examples of this converter used in solar cell maximum power point tracking in the literature. The objective was to apply this DC to DC converter to Stargrazer One. However, it may be possible to use the methods proposed in this chapter to prepare this converter for use in another system. The objectives of the studies in this chapter are now listed:

- Obtain a quantitative and qualitative understanding of this converter in both steady state and changing conditions.
- Assess the performance of the switched capacitor DC to DC converter.
- Determine a systematic means to select appropriate devices so that an appropriate implementation of this DC to DC converter can be instantiated.

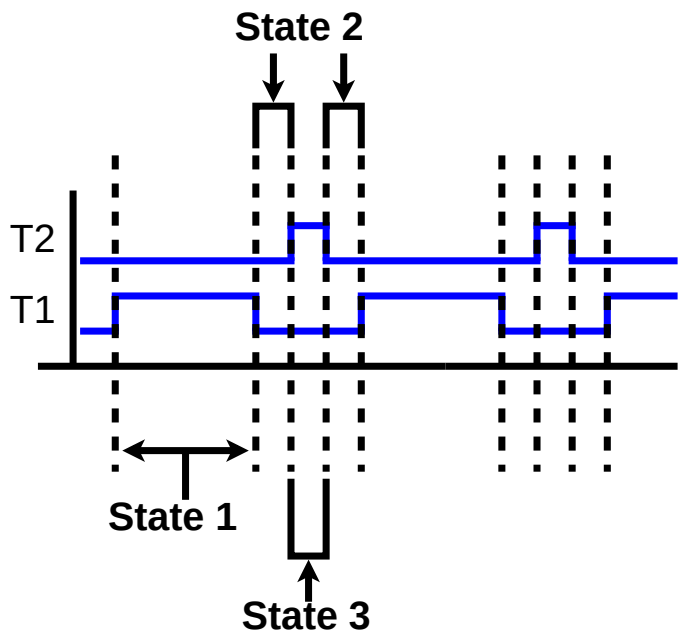

Figure 7.2: An example switching sequence for the transistors in the described step down converter. The converter state assumed during each portion of the switching sequence is labeled.

- Optimize the performance of the switched capacitor DC to DC converter to improve Stargrazer One's viability.
- Determine how to design Stargrazer One so that the negative impacts, if any, from the converter behavior are minimized.

These objectives are handled in the sections of this part which are now presented in list format:

- Chapter 8
  - Section 8.1: This section presents a voltage model which uses the switch resistor transistor model. The determination of several design choices, such as how to turn on and off the transistors, required a quantitative model for charge movement inside the converter. This model presents a tradeoff between increased accuracy and added model complexity that was sufficient for this thesis. The voltage model addresses each state the DC to DC converter assumes.
  - Section 8.2: This section presents an ideal switch voltage model for the switched capacitor DC to DC converter. This simplified model is used throughout this thesis for analysis where fine detail on how charge moves

between the capacitors is not required. The ideal voltage model addresses each state the DC to DC converter assumes.

- Chapter 9
  - Section 9.1: This section defines a method to assess the performance of the switched capacitor step down converter. All performance metrics and the procedure will be defined. This procedure will then be used on an instance of this converter.
  - Section 9.2: This section poses the question "Can this converter's efficiency be improved while preserving its simplicity?". This section shows how optimizing the State Two and Three durations offers a valid answer via experimentation.
- Chapter 10
  - Section 10.1: This section explores how the converter reacts when presented with change. A qualitative explanation is presented. The section then explores if this behavior interferes with the duties of the proposed maximum power point tracking system. The section will conclude by presenting design tools to be used in the design of Stargrazer One to minimize negative impacts from the converter's response to changes.

Chapter 8 Modeling of the Step Down Converter

8.1 Voltage Model Using Switch-Resistor Model for Transistors

Introduction and Purpose

This model provides insight into the behavior of this switched capacitor converter which greatly aided the design of Stargrazer One. This discussion will proceed to describe the model state by state.

When entering States One and Three this circuit is a violation of Kirchhoffs rule of voltage [31]. Wires and transistors present a finite (albeit small) resistance in this converter [31]. Therefore what will occur is that the discrepancy in voltage will be dropped across these resistances. There will be a limit to the maximum amount of current that will move in accord with Ohm's Law. Since these resistance values are small the charge movement will be rather large once these capacitors are connected. As time advances, the current flow between the capacitors will diminish as charge redistributes. To reflect this, a switch resistor model is used for the power MOSFETs. To facilitate ease of analysis, remaining components are assumed ideal. The solar cell source is to be defined by the following relationship:

$$I(t) = I_{sc} - I_o \cdot \left(e^{\left(\frac{V(t)}{V_{th}}\right)} - 1 \right) \tag{8.1}$$

Where I_{sc} is the short circuit current of the source, V_{th} is the thermal voltage and I_o is the reverse bias current. Taken from [2].

For reference, figure 7.1 presents the circuit topology for each state that will be discussed.

State One

In this state, capacitors C1 and Cfilter form a source fed RC circuit. The resulting topology is visually presented in figure 7.1. To define quantitatively the voltages observed in this state, Kirchhoff current law was applied to the two nodes in this topology. The results are presented in the following set of equations:

$$\frac{dV_{Cfilter}}{dt} = \frac{I_{sc} - I_o \cdot \left(e^{\left(\frac{V_{Cfilter}(t)}{V_{th}}\right)} - 1 \right)}{Cfilter} - \frac{V_{Cfilter}(t)}{R_{switch} \cdot Cfilter} + \frac{V_{C1}(t)}{R_{switch} \cdot Cfilter} \tag{8.2}$$

$$\frac{dV_{C1}}{dt} = \frac{V_{Cfilter}(t)}{R_{switch} \cdot C1} - \frac{V_{C1}(t)}{R_{switch} \cdot C1} \tag{8.3}$$

As can be observed, equations 8.2 and 8.3 form a cross coupled pair of differential equations. The presence of the solar source in equation 8.2 makes this pair nonlinear. In this thesis, numerical means are used to evaluate this equation set.

A source-less RC loop is formed with capacitor C2 and the resistive load. The voltage on capacitor C2 is determined with equation 8.4:

$$V_{C2}(t) = V_i \cdot e^{\left(\frac{-t}{R_{load} \cdot C2}\right)} \tag{8.4}$$

V_i is the initial voltage of capacitor C2. This value is equal to the voltage on this capacitor at the end of State Three.

State Two

Capacitor C1 is open circuited during this state. The switch resistances have no effect. Since the components are ideal, the voltage of capacitor C1 is constant.

Capacitor C2 is still involved with the source-less RC loop. The voltage is still determined by 8.4.

Capacitor Cfilter is still connected to the solar cell source. The equation which describes the voltage is presented below:

$$\frac{dV_{Cfilter}}{dt} = \frac{I_{sc} - I_o \cdot \left(e^{\left(\frac{V_{Cfilter}(t)}{V_{th}}\right)} - 1\right)}{Cfilter} \tag{8.5}$$

This is a nonlinear differential equation and will be numerically evaluated in this thesis.

State Three

Capacitors C1 and C2 are in a second order RC circuit with no source. This can be viewed in figure 7.1. Executing Kirchhoff's current law on the high potential nodes of capacitors C1 and C2 produced the following differential equations describing the circuit's behavior.

$$\frac{dV_{C1}}{dt} = \frac{V_{C2}(t)}{C1 \cdot R_{switch}} - \frac{V_{C1}(t)}{C1 \cdot R_{switch}} \tag{8.6}$$

$$\frac{dV_{C2}}{dt} = \frac{V_{C1}(t)}{C2 \cdot R_{switch}} - \frac{V_{C2}(t) \cdot (R_{load} + R_{switch})}{C2 \cdot R_{switch} \cdot R_{load}} \tag{8.7}$$

Where R_{switch} is the parasitic switch resistance and R_{load} is the load resistance. This analysis assumes that both transistors have the same on resistance.

These equations present a complete description for the converter in this state. The challenge is taking these equations and converting them into a convenient form for analysis. Equations 8.6 and 8.7 are cross coupled and linear. The equations have two unknown variables which are the capacitor voltages. This means that these can be algebraically solved. The following approach was used. First, the two expressions were converted into a vector matrix form.

$$\dot{V} = \begin{bmatrix} -\frac{1}{C1 \cdot R_{switch}} & \frac{1}{C1 \cdot R_{switch}} \\ \\ \frac{1}{C2 \cdot R_{switch}} & -\frac{R_{load} + R_{switch}}{C2 \cdot R_{load} \cdot R_{switch}} \end{bmatrix} \cdot V \tag{8.8}$$

Where V is a vector containing the capacitor voltages and $\dot{V}$ is the vector containing the derivatives of the capacitor voltages. The vector V is defined as:

$$V = \begin{bmatrix} V_{C1}(t) \\ V_{C2}(t) \end{bmatrix} \tag{8.9}$$

and the vector $\dot{V}$ is defined as:

$$\dot{V} = \begin{bmatrix} \frac{dV_{C1}(t)}{dt} \\ \frac{dV_{C2}(t)}{dt} \end{bmatrix} \tag{8.10}$$

The first task was to find the general solution for this equation set. The task required finding the eigenvalues for the matrix in equation 8.8.

The type of homogeneous solution will depend on the result. For the capacitor values examined, two distinct real eigenvalues were found. This means the equation will be in the form of a double exponential. The possibility of obtaining imaginary solutions or equal values using realistic device values was not explored. This had no impact on developing Stargrazer One. Therefore the discussion will conclude assuming the case of two real and distinct eigenvalues. What remains is to find constants using the initial conditions. Determining this entails solving the following initial value problem:

$$\begin{bmatrix} V_{C1}(0) \\ V_{C2}(0) \end{bmatrix} = K_1 \cdot \vec{u_1} \cdot e^0 + K_2 \cdot \vec{u_2} \cdot e^0 \tag{8.11}$$

$V_{C1}(0)$ and $V_{C2}(0)$ are the voltages on capacitors C1 and C2 respectively upon entering State Three. $\vec{u_1}$ and $\vec{u_2}$ are eigenvectors for the eigenvalues λ_1 and λ_2 respectively. K_1 and K_2 are constants and can be algebraically determined by using the two equations.

The complete description for both capacitor voltages is in this operating state is given in equation 8.12:

$$\begin{bmatrix} V_{C1}(t) \\ V_{C2}(t) \end{bmatrix} = K_1 \cdot \vec{u_1} \cdot e^{\lambda_1 \cdot t} + K_2 \cdot \vec{u_2} \cdot e^{\lambda_2 \cdot t} \tag{8.12}$$

As with state 2, capacitor Cfilter is being charged by the source. Its voltage is modeled with equation 8.5.

Example

To observe how this converter behaves (as per the model), a simulation model was developed using the equations discussed in this section. This example was prepared in the MATLAB environment. Table 8.1 includes the values used in this example.

Replacing the appropriate variables with their respective chosen values, the following linear equation system was determined for capacitors C1 and C2 in State Three:

Table 8.1: Converter values chosen for the presented example.

Parameter	Value	Units
C1	17	μF
C2	20	μF
R_{load}	3	Ω
R_{switch}	15	mΩ
T	5	μs

$$\dot{V} = \begin{bmatrix} 3.922 \cdot 10^6 & -3.922 \cdot 10^6 \\ -3.350 \cdot 10^6 & 3.333 \cdot 10^6 \end{bmatrix} \cdot V \tag{8.13}$$

Where V is a vector containing the capacitor C1 and C2 voltages. The obtained eigenvalues are $\lambda_1 = -8.999 \cdot 10^3$ and $\lambda_2 = -7.262 \cdot 10^6$. As the values are real, the behavior will be modeled as two decaying exponential equations. The two resulting eigenvectors are presented below:

$$\begin{bmatrix} 0.718 \\ 0.706 \end{bmatrix} \tag{8.14}$$

for λ_1 and

$$\begin{bmatrix} 0.761 \\ -0.649 \end{bmatrix} \tag{8.15}$$

for λ_2. To determine the specific solution, the initial value problem for this specific case was determined to be the following:

$$\begin{aligned} K1 &= 0.650 \cdot V_{C1}(0) + 0.764 \cdot V_{C2}(0) \\ K2 &= 0.709 \cdot V_{C1}(0) + -0.710 \cdot V_{C2}(0) \end{aligned} \tag{8.16}$$

Due to the nonlinear differential equations governing State One and the behavior of capacitor Cfilter, the MATLAB simulation proceeded toward steady state in an iterative manner. The initial voltages V_{C1} and V_{C2} were the observed result for the particular converter cycle. For the purposes of this section, steady state behavior is of interest. The definition of steady state is the same as for section 8.2, namely the voltage oscillation boundaries for all devices are constant. The particular steady state values obtained for the converter whose components are defined in table 8.1 are given in table 8.2.

Table 8.2: Observed limits of voltage oscillations assumed by capacitors C1 and C2.

Limits of Oscillation		
$V_{C1}(min)$	=	0.12
$V_{C1}(max)$	=	0.17
$V_{C2}(min)$	=	0.10
$V_{C2}(max)$	=	0.12

Where all values in 8.11 are reported in volts. For completeness, the solution for 8.16 for this particular converter is presented in equation 8.17.

$$\begin{aligned} V_{C2}(t) &= 0.13 \cdot e^{-8999.499 \cdot t} - .033 \cdot e^{-7.262569e6 \cdot t} \\ V_{C1}(t) &= 0.13 \cdot e^{-8999.499 \cdot t} + .038 \cdot e^{-7.262569e6 \cdot t} \end{aligned} \tag{8.17}$$

Behavioral plots for capacitor C1 and C2 are presented individually in figures 8.1 and 8.2. Figure 8.3, presents the voltage observed on the high potential node for all capacitors.

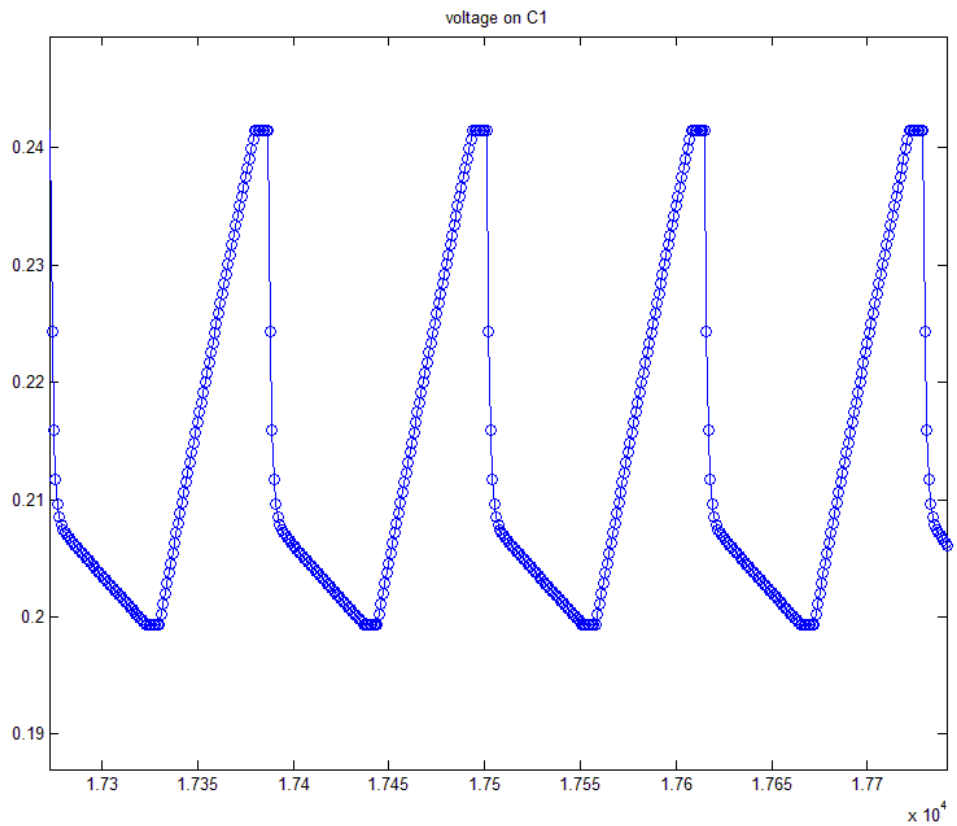

Figure 8.1: This presents the voltage seen on the capacitor C1 under steady state conditions. The observed rings on the plots indicate actual data points. Note that the plots are on different timescales. Note that the simulator is designed so that he point corresponding to a state transition is repeated twice. Simulation accuracy is not affected by this design choice. Y axis is voltage in V. X axis is in data point number.

Conclusions

Figure **??** presents the behavior of both capacitors C1 and C2 individually while figure 8.3 presents them together along with Cfilter. As can be seen in figure 8.3

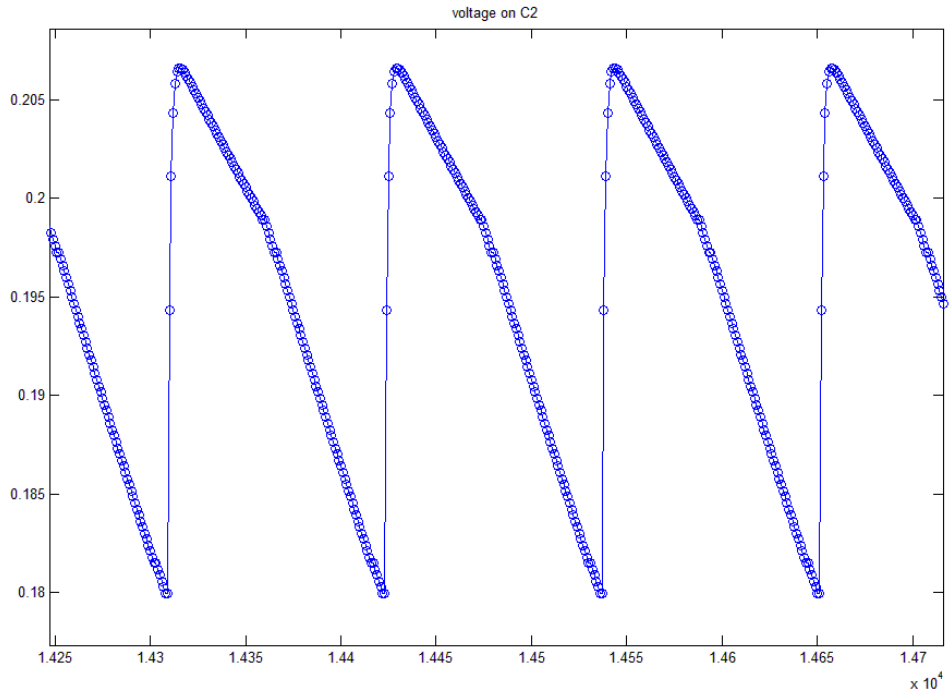

Figure 8.2: This presents the voltage seen on the capacitor C2 under steady state conditions. The observed rings on the plots indicate actual data points. Note that the plots are on different timescales. Note that the simulator is designed so that he point corresponding to a state transition is repeated twice. Simulation accuracy is not affected by this design choice. Y axis is voltage in V. X axis is in data point number.

There seems to be a brief transient during State Three operation. This is because the two capacitors must assume an equal voltage. The duration of this adjustment is a result of the switch resistances. Since the value of the resistance is finite, Ohms law dictates that the current movement will also be finite. As charge redistributes on the capacitors, this current will gradually reduce to a final very small but non zero value. This naturally implies that a final [albeit small] voltage difference will remain between the capacitors. This can be verified by subtracting the equation for capacitor C1 from the equation for capacitor C2. A similar observation can be made for the observed behavior of capacitors C1 and Cfilter during State One.

As the capacitors readjust their voltage, a portion of the energy delivered from capacitor C1 is being dissipated by the resistance. A way to fully remove this loss source is to reduce the voltage difference between capacitors C1 and C2 to zero. This condition is achievable if both devices are at the same voltage. Obviously there would be no charge movements making this arrangement useless for Stargrazer One. It was found that appropriate adjustments can be made to how this converter operates to reduce this observed loss. This is handled in section 9.2.

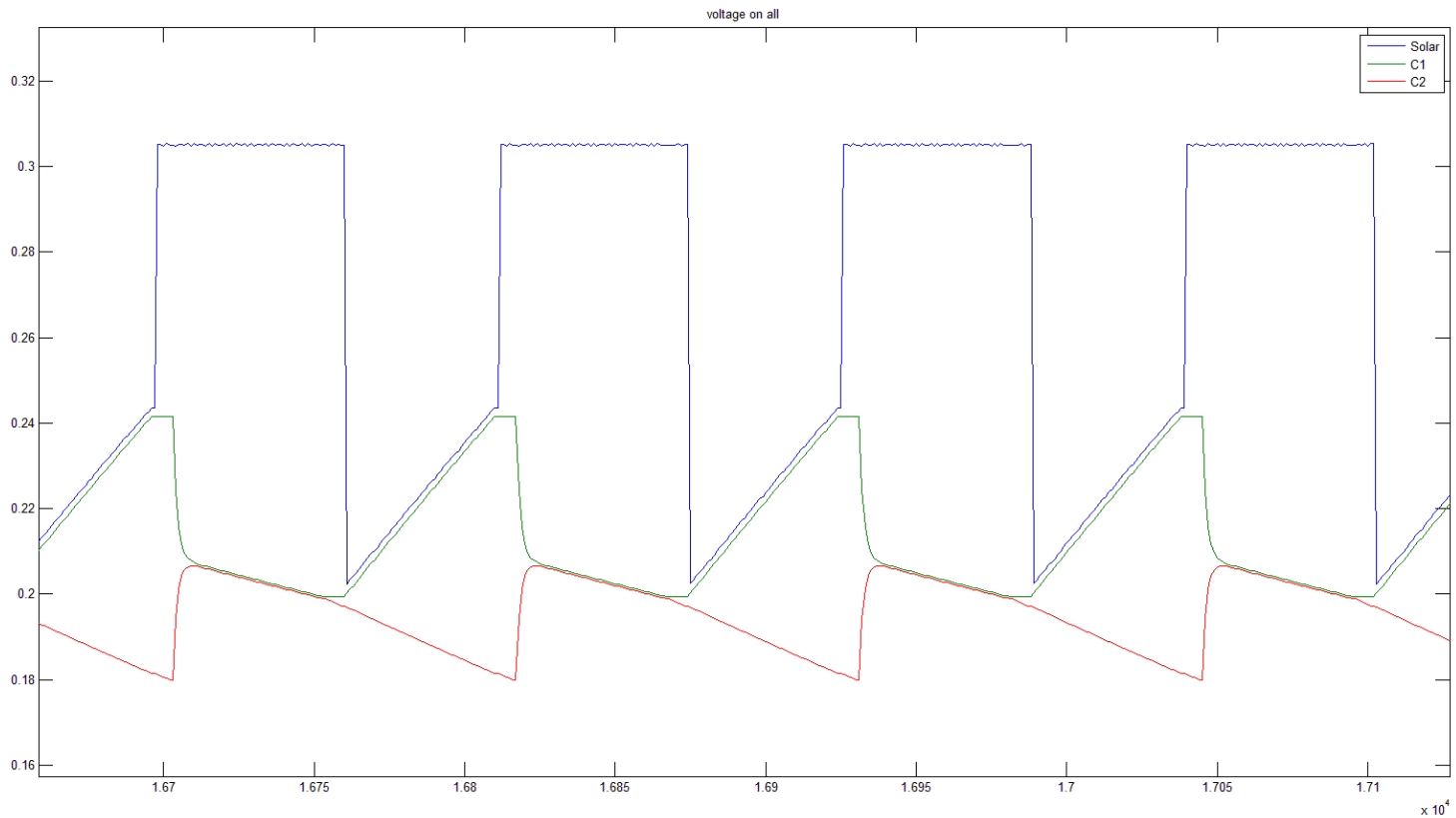

Figure 8.3: All capacitor high potential nodes are presented simultaneously. The top trace is for capacitor Cfilter, the middle trace is for capacitor C1 and the bottom plot is capacitor C2. Note that the simulator is designed so that he point corresponding to a state transition is repeated twice. Simulation accuracy is not affected by this design choice. Y axis is voltage in V. X axis is in data point number.

8.2 Voltage Model Using Perfect Switch Model for Transistors

Introduction

Certain analyses required the use of a perfect switch model for the transistors. This model assumes the following conditions:

- All circuit components free of any parasitic affects.
- All sources free of parasitic affects.
- Instantaneous switching of transistors.
- The solar cell source will be defined using equation 8.1 presented in section 8.1.

The equations will be derived for each operating state of the converter circuit. Figure 7.1 visually shows the states the converter assumes as it operates. For the purposes of the model, the switch resistances are assumed zero.

State One

Capacitors C1 and Cfilter are being charged by solar cell source. Upon entering State One, capacitors C1 and Cfilter will be at different initial voltages. This is a violation of Kirchhoff's voltage law [31]. This situation is temporary and charge will redistribute between these two capacitors to equalize the voltage across the high potential mode of the circuit. Since the circuit is ideal, this transition can be assumed immediate. The final resulting voltage is determined with the following equation:

$$V_{i1} = \frac{V_{C1}(0) \cdot C1 + V_{Cfilter}(0) \cdot Cfilter}{C1 + Cfilter} \tag{8.18}$$

Where $V_{C1}(0)$ and $V_{Cfilter}(0)$ are the voltages on capacitors C1 and Cfilter respectively when entering State One and $C1$ and $Cfilter$ are the values for capacitors C1 and Cfilter. V_{i1} is the final resulting voltage.

The results of equation 8.18 becomes the initial condition to the differential equations which describes how the voltage will change for both capacitors C1 and Cfilter. This equation is presented below:

$$I = (C1 + Cfilter) \cdot \frac{dV}{dt} \tag{8.19}$$

Where $C1$ and $Cfilter$ are the values for capacitors C1 and Cfilter, I is the current through the device and V is the voltage seen by capacitors C1 and Cfilter.

The current entering the capacitors is from the solar cell. So to reflect this equation 8.19 is changed to:

$$(Isc - Io \cdot \left(e^{\left(\frac{V(t)}{Vth}\right)} - 1\right) = (C1 + Cfilter) \cdot \frac{dV}{dt} \tag{8.20}$$

Where I_{sc}, I_o, Vth are specific to the solar source selected for use. V is the voltage seen by capacitors C1 and Cfilter. This is a nonlinear differential equation. For this thesis, this differential equation will be evaluated using numerical methods.

While capacitors C1 and Cfilter are being charged, capacitor C2 is acting as a charge reserve. It forms a source-less capacitor impedance loop. In this analysis, the load is modeled as a resistance. Therefore, the voltage of capacitor C2 is determined by finding the value of the high potential node of the RC loop. Finding this relationship is a simple exercise of the basic circuit theory. Applying Kirchhoffs current law gives the basic form of the voltage equation

$$0 = C2 \cdot \frac{dV_{C2}(t)}{dt} + \frac{V_{C2}(t)}{R} \tag{8.21}$$

Solving the differential equation in 8.21 gives the final result

$$V_{C2}(t) = V_{i2} \cdot e^{\left(\frac{-t}{R \cdot C2}\right)} \tag{8.22}$$

Where V_{i2} is the initial voltage of capacitor C2. The initial value is determined from the voltage on capacitor C2 at the end of the time spent in State Three.

State Two

Capacitor C1 sees no changes since it is open circuited. Capacitor C2 continues to be governed by equation 8.22.

Capacitor Cfilter continues to be charged by the solar source. The following equation determines the voltage seen on capacitor Cfilter:

$$\frac{dV_{Cfilter}}{dt} = \frac{I_{sc} - I_o \cdot \left(e^{\left(\frac{V_{Cfilter}(t)}{V_{th}}\right)} - 1\right)}{C_{filter}} \tag{8.23}$$

This is a nonlinear first order differential equation. In this thesis, this equation is evaluated using numerical methods.

State Three

Capacitor Cfilter continues to be charged by the solar cell. The voltage change is governed by equation 8.23.

Capacitors C1 and C2 see the same behavior. This is because both are involved in a RC source-less loop. Applying Kirchhoff's current law at the high potential node gives:

$$0 = C1 \cdot \left(\frac{dV_{C1}(t)}{dt}\right) + C2 \cdot \left(\frac{dV_{C2}(t)}{dt}\right) + \frac{V_{C2}(t)}{R} \tag{8.24}$$

As $V_{C1} = V_{C2}$, this can be written as:

$$0 = (C1 + C2) \cdot \left(\frac{dV_{C1,C2}(t)}{dt}\right) + \frac{V_{C1,C2}(t)}{R} \tag{8.25}$$

Where $V_{C1,C2}$ indicates the voltage seen by both capacitors C1 and C2. Solving the differential equation gives the desired relationship:

$$V_{C1,C2}(t) = V_{i3} \cdot e^{\left(\frac{-t}{R \cdot (C1+C2)}\right)} \tag{8.26}$$

The V_{i3} value in equation 8.26 is a voltage constant. The value of this constant is determined from:

$$V_{i3} = \frac{(C1 \cdot V_{C1}(0) + C2 \cdot V_{C2}(0)}{(C1 + C2)} \tag{8.27}$$

Equation 8.27 presents the final result after the capacitors C1 and C2 pass charge between themselves. Immediately upon entering State Three, capacitors C1 and C2 are at different voltages (denoted as $V_{C1}(0)$ for capacitor C1 and $V_{C2}(0)$ for capacitor C2). Just like State One, State Three violates Kirchhoffs voltage law because two unequal voltage sources (the capacitors) are being connected together [31]. As with State One, this situation is temporary as charge passes between the devices to equalize the voltage. Since the model is ideal, this exchange can be assumed instantaneous.

Important Comments

Using the derived equations, it is possible to visualize the ideal voltage behavior for this DC to DC converter. Figure **??** presents a steady state voltage view for capacitors C1 and C2 under regular switching. For the purposes of this section, steady state means that the observed oscillations have settled within a voltage band that is constant (no upward or downward trending). A MATLAB script was prepared to generate these images.

Table 8.3: Design choices for the converter used to produce the plots in figures 8.4 and 8.5.

design values		
$C1$	17	μF
$C2$	20	μF
R_{load}	3	Ω
$V_{thermal}$	.0256	V
I_{short}	.15	A
I_o	1	μA

Conclusion

In this section, a idealized model for the switched capacitor step down converter is presented. This model is appropriate for high level analysis where the details of how charge moves within the converter can be ignored.

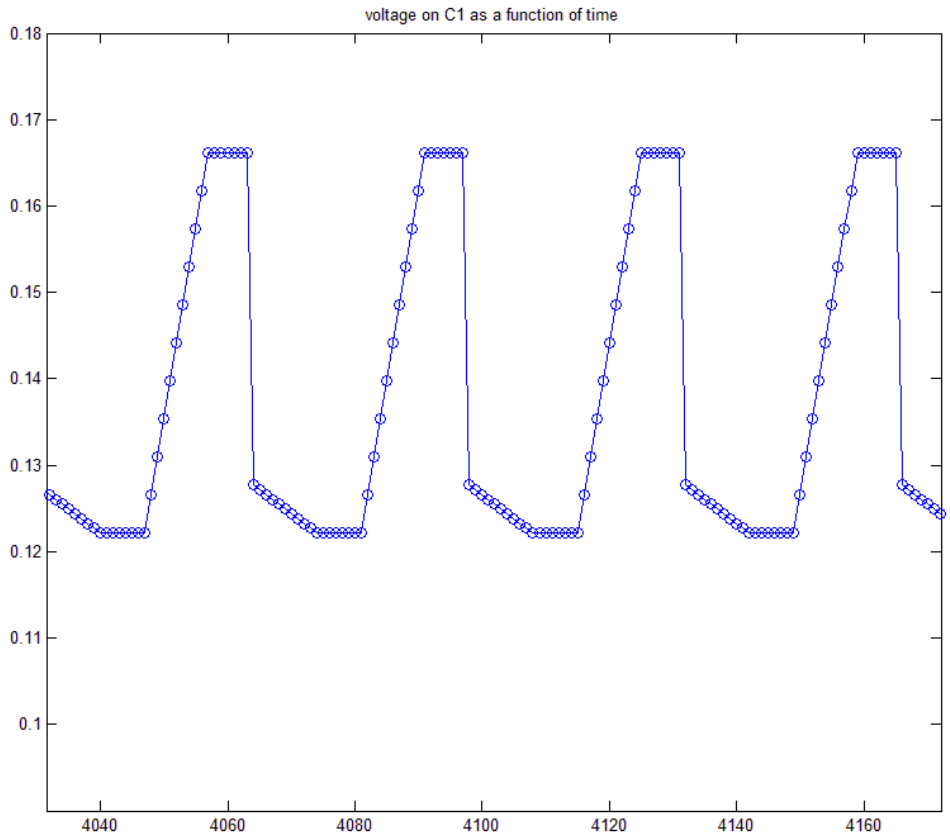

Figure 8.4: The voltage oscillation seen on capacitor C1. The observed "choppiness" is due to the way the simulation is designed. The point corresponding to a state transition is repeated twice. Simulation accuracy is not affected by this design choice. Y axis is voltage in V. X axis is in data point number.

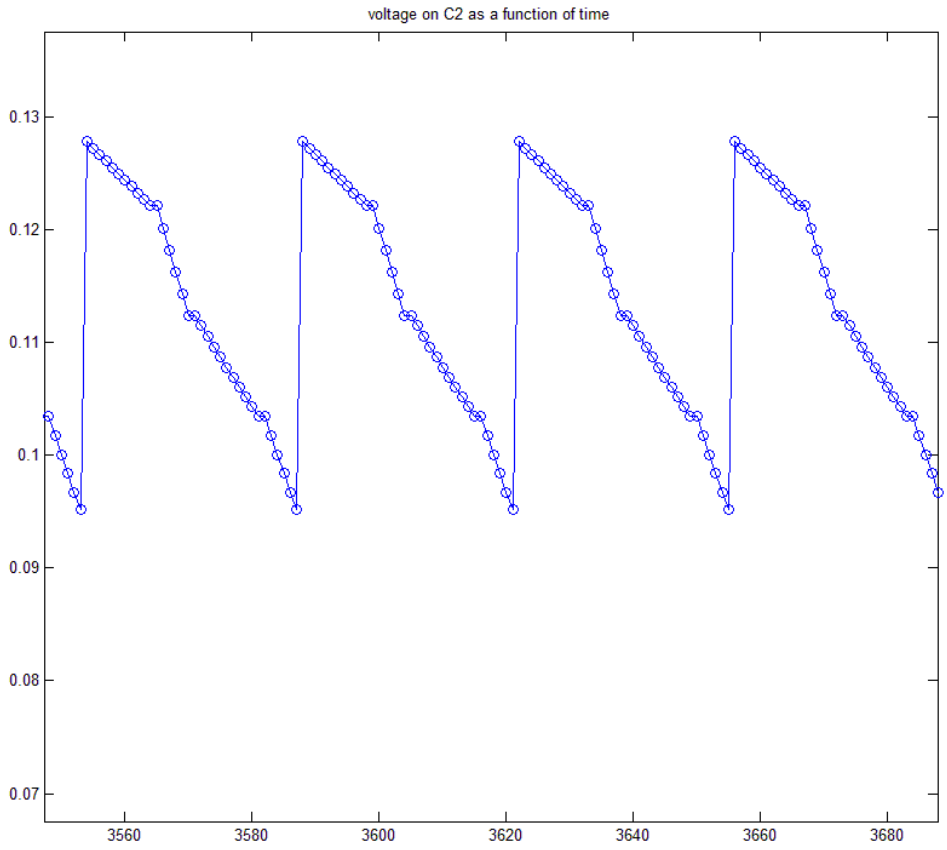

Figure 8.5: The voltage oscillation seen on capacitor C2. The observed "choppiness" is due to the way the simulation is designed. The point corresponding to a state transition is repeated twice. Simulation accuracy is not affected by this design choice. Y axis is voltage in V. X axis is in data point number.

Chapter 9 Performance Assessment of Step Down Converter

9.1 Developed Method To Assess Efficiency of the Step Down Converter

Introduction

When this system is in use, it is preferable to not have a large amount of the supplied energy be wasted. The following discussion presents an exploration of the efficiency of this power converter. The original designers for this converter did not include this analysis [30]. Emphasis was on proof of concept in paper [30]. Article [23] presents only the results of an efficiency study. No discussion of how these values were determined was included. Therefore, this paper will present a method to determine the performance of this switched capacitor power electronic converter. The intent is to provide an efficiency performance reference point using a switching pattern similar to the one presented in paper [30]. This discussion will begin by explaining the efficiency metrics to be used followed by an outline of the procedure. Then the procedure will be applied to the switched capacitor converter using the model presented in section 8.1. The discussion will conclude with a presentation of the obtained results.

Basic Definitions

Before proceeding the following must be properly defined:

- The efficiency examined will be the ratio of power that enters the converter and what exits to the load. The capacitor Cfilter is considered as outside of the converter and its effect is not examined. This is permissible due to the definition of efficiency to be studied. Loss sources before the converter (such as from the capacitor Cfilter or the solar source itself) are outside of the scope of this evaluation.

- Power is defined as follows

$$Power = \frac{\Delta Energy}{\Delta Time} \tag{9.1}$$

  The time in question is an entire converter switching cycle. The definition of a converter cycle is defined in chapter 7. It takes an entire converter cycle for energy to propagate across the converter. Each cycle sees new energy from the solar cell. Since we are interested in the power entering and exiting the converter, using the converter switching cycle as the time unit is a prudent choice.

- Expanding upon the basic definition of power in equation 9.1 the following definitions for the power entering the converter P_{in} and exiting P_{out} are defined as follows.

$$
\begin{aligned}
P_{in} &= \frac{\Delta E_{in}}{T_{cycle}} \\
P_{out} &= \frac{\Delta E_{out}}{T_{cycle}}
\end{aligned}
\tag{9.2}
$$

P_{in} is the power that enters the converter from the solar source. P_{out} is the power that leaves the converter to the load. T_{cycle} is the time duration of a converter cycle. E_{in} and E_{out} are the observed energy values for the energy that enters and leaves the converter respectively.

- To assess efficiency the following equation will be used:

$$
\eta = \frac{P_{out}}{P_{in}} \tag{9.3}
$$

Procedure

The following approach was used. First the power that comes into the converter was determined. Then the power that makes it into the load is determined. Once these values are found, the efficiency is evaluated using equation 9.3. The incoming and outgoing powers were determined by computing equation 9.1 for each case. All analysis is done under "steady state conditions". "steady state" is defined as repeated cyclic behavior where the converter capacitors assumes a fixed range of voltages.

Determining Energy Entering Converter

Energy comes into the converter only during State One operation. Energy only enters the converter via capacitor C1. When energy enters the converter, it must first pass through the switch resistance. To quantitatively determine what portion of energy enters the converter, the energy entering capacitor C1 and the energy consumed by the resistance were first determined. The desired value will be the sum of these two. The lost energy corresponds to the value for the resistance.

The energy entering capacitor C1 can be quantitatively defined by first determining the maximum and minimum voltages the device will assume under normal operation. Once these values are known, finding the energy entering capacitor C1 becomes an application of the following equation:

$$
\Delta E_{in} = \frac{1}{2} \cdot C1 \cdot (V_{max(C1)}^2 - V_{min(C1)}^2) \tag{9.4}
$$

Where $C1$ is the size of capacitor C1 and $V_{max(C1)}$ and $V_{min(C1)}$ are the observed minimum and maximum voltages respectively.

Translating this into the desired power value is accomplished by applying equation 9.1 with ΔE_{in} as the result from equation 9.4

Finding the energy consumed by the switch resistance entails the following procedure. Resistors do not store energy, so the following equation must be used to determine the energy consumed:

$$\int_0^{T_{State\,One}} P_r(t)\,dt \tag{9.5}$$

Where $P_r(t)$ is the power consumed by the loss resistance as a function of time and $T_{State\,One}$ is the duration of State One. Given the fact that behavioral models defined in this chapter find voltages on the converter capacitors, the most convenient method to determine power is using this variation of Watt's law:

$$P_r(t) = \frac{(V_{Cfilter}(t) - V_{C1}(t)^2}{R_{switch}} \tag{9.6}$$

As discussed in section 8.2, determining the required voltages ($V_{Cfilter}(t)$ and $V_{C1}(t)$) involves solving a nonlinear differential equations system. Because this equation system is evaluated using numerical methods, the energy consumed by the switch resistance is an estimated value. To obtain a reasonable estimate, a large amount of time points should be selected and the resulting voltages recorded on capacitors Cfilter and C1 for each time point. For this analysis, the duration of State One was divided into 1,000 equal time segments. For each segment, the resulting voltages for capacitor Cfilter and C1 were recorded. For each time point, the instantaneous power was computed using equation 9.6. The decision to use equal time segments was made to facilitate use of the trapezoidal approximation method for the integral needed to evaluate energy (as shown in equation 9.5). As a result, equation 9.5 becomes:

$$\sum_{i=0}^{999} \frac{1}{2} \cdot \frac{T_{State\,One}}{1000} \cdot (P_r(i) + P_r(i+1)) \tag{9.7}$$

Where $T_{State\,One}$ is the duration of State One and $P_r(i)$ and $P_r(i+1)$ are the instantaneous power values for time points i and $i+1$ respectively. The solution of equation 9.7 will give the energy lost in the switch resistor.

Determining the energy which enters the converter involves adding the results of equation 9.4 and equation 9.7.

Determining Energy Exiting Converter

Energy departs the converter to the load during all converter states. There are two capacitors supplying energy during State Three. During the other two operating points, capacitor C2 supplies energy alone.

For States One and Two the energy leaving the system is defined as:

$$\Delta E = \frac{1}{2} \cdot C2 \cdot (V_{max(C2)}^2 - V_{min(C2)}^2) \tag{9.8}$$

$V_{max(C2)}$ is the Voltage seen on capacitor C2 (labeled $C2$ in equation 9.8) at the end of State Three operation and $V_{min}(C2)$ is the voltage just before the converter assumes State Three.

Evaluating the energy that moves during State Three was handled in the following manner. The contributions from capacitor C1 and capacitor C2 were separately

determined. The energy which leaves to the load during this state is the sum of these energies.

The energy which leaves capacitor C1 was determined by applying equation 9.8 after replacing $V_{max}(C2)$ with $V_{max}(C1)$ and $V_{min}(C2)$ with $V_{min}(C1)$. $V_{max}(C1)$ and $V_{min}(C1)$ are equal to the maximum and minimum voltages the capacitor can assume. As shown in section 8.1, capacitor C1 sees a decreasing voltage across the entire period of State Three. Since energy is proportional to the square of the voltage, the available energy in the device will decrease across the state. It was observed that a portion of this energy will be used to replenish capacitor C2 and be lost in the parasitic switch resistance. These values must be determined in order to find the contribution from capacitor C1. Determining what value of energy reenergizes capacitor C2 requires the voltage equation for the capacitor determined in section 8.1:

$$V_{C2}(t) = K1 \cdot \vec{u_1} \cdot e^{\lambda_1 \cdot t} + K2 \cdot \vec{u_2} \cdot e^{\lambda_2 \cdot t} \tag{9.9}$$

In section 8.1, equation 9.9 when applied with real values had an exponential decay term and an inverted exponential decay term. This means that at some point a voltage maximum will be reached. Given the charge exchange between the capacitors that occurs in this state, it is safe to assert that equation 9.9 will behave similarly with reasonable, alternate values. This was indeed the case for all values examined in this thesis. Proceeding, the precise time location of this maximum can be readily found by differentiating equation 9.9 and solving for zero. Placing the solution into equation 9.9 will give the maximum voltage capacitor C2 will assume. The energy used to replenish capacitor C2 can now be found using equation 9.4 where $V_{max}(C2)$ is now the energy value corresponding to the maximum voltage for capacitor C2 just determined and $V_{min}(C2)$ is the voltage seen on capacitor 2 upon entering State Three.

To determine the energy consumed by the parasitic switch resistance the following was done. A resistor does not store energy. The energy contribution will be determined from the power. The most convenient method to determine power in this case is with the following Watt's Law variant:

$$P_r(t) = \frac{V_r(t)^2}{R} \tag{9.10}$$

Where V_r is defined as:

$$\begin{aligned} V_r(t) &= V_{C1}(t) - V_{C2}(t) \\ V_r(t) &= (K1 \cdot e^{\lambda_1 \cdot t} + K2 \cdot e^{\lambda_2 \cdot t}) - (K3 \cdot e^{\lambda_1 \cdot t} + K4 \cdot e^{\lambda_2 \cdot t}) \end{aligned} \tag{9.11}$$

Where $K1, K2, K3, K4$ consist of the determined constant and the appropriate eigenvector element. The energy can now be determined with equation 9.12 listed below:

$$E_r = \int_0^{T_{State\,Three}} P_r(t)\, dt \tag{9.12}$$

Where P_r is the power consumed in the resistance and $T_{State\,Three}$ is the duration of State Three. Once equation 9.12 has been evaluated, the energy from capacitor C1 to the load can be determined by:

$$E_l = \Delta E - E_{C2} - E_r \tag{9.13}$$

Where E_r is the energy consumed by the switch resistance, E_{C2} is the energy sent to capacitor C2, E_l the energy consumed by the load and ΔE is the energy from capacitor C1.

The contribution from capacitor C2 to the load during State Three is found with equation 9.4. Here $V_{max}(C2)$ is the peak voltage assumed by capacitor 2 and $V_{min}(C2)$ is the voltage of the capacitor at the conclusion of State Three. No charge from capacitor C2 will pass through the loss resistance as capacitor C1 is at a higher potential than capacitor C2.

Determining the Powers and Efficiency

The incoming average power was computed with the following expression

$$P_{in} = \left(\frac{E_{in}}{T_{State\,One}}\right) \cdot \left(\frac{T_{State\,One}}{T_{cycle}}\right) \tag{9.14}$$

Where $T_{State\,One}$ is the length of time in operating State One, T_{cycle} is the total switching cycle, and E_{in} is the computed energy. An important observation is that this is an average power. In reality the power entering capacitor C1 is not constant. Since the total amount of energy has been computed and the time that this energy was able to move is known, an accurate average can be determined. This is far more convenient then using the real power relationships. The first part of equation 9.14 defines the average power during State One operation. The second part weighs the average across the entire converter switching period.

The departing power was computed with the following:

$$\begin{aligned} P_{out} = \; & \left(\frac{E_{out}(State\,Three)}{T_{State\,Three}}\right) \cdot \left(\frac{T_{State\,Three}}{T_{cycle}}\right) + \\ & \left(\frac{E_{out}(State\,One, State\,Two)}{(T_{State\,One} + 2 \cdot T_{State\,Two})}\right) \cdot \left(\frac{(T_{State\,One} + 2 \cdot T_{State\,Two})}{T_{cycle}}\right) \end{aligned} \tag{9.15}$$

$E_{out}(State\,Three)$ is the result from equation 9.13 and equation 9.8. $E_{out}(State\,One, State\,Two)$ is the result from equation 9.8. Furthermore $T_{State\,One}, T_{State\,Two}, T_{State\,Three}$ are the time durations of States One, Two and Three respectively. Again this is a weighted average power. The scaling is the same as for equation 9.14. The efficiency is determined with equation 9.3.

Physical Example

The values used in this example are in table 9.1.

Determining the energy entering the converter requires evaluating equation 9.4 and 9.7. Applying equation 9.4 determined the energy which enters capacitor C1. Applying equation 9.4 with the appropriate values for the variables, the energy coming

Table 9.1: Design choices for the presented example.

converter values

device	value	unit
C2	20	mu F
C1	17	mu F
Load	3	Ω
switch loss	.015	Ω

solar cell

I_{short}	.15	A
Io	1e-7	A
Vth	.025	V
M	1000	partitions
$T_{State\,One}$	5	μs
$T_{State\,Two}$	10	μs
$T_{State\,Three}$	5	μs

in was determined. Using equation 9.14, the weighted average power incoming was determined. The results are in table 9.2.

Table 9.2: Test results showing incoming power and energy lost in switch resistances.

computed incoming values

Energy from source	1.2e-7	J
Energy into C1	1.1e-7	J
Energy lost from T1 resistance	1.1e-8	J
Energy lost from T2 resistance	2.4e-8	J

average per converter cycle

Power into converter	6.0	mW

Finding the weighted average power which reaches the load was determined as follows. Applying equation 9.8 with appropriate values gives the energy leaving capacitor C2 during states one and two. State three was handled as follows. It was observed that the time spent in State Three was sufficiently long that the capacitor C2 energy peaks before the end of the time. Capacitor C2 obtains the maximum energy at $.73\mu s$. The voltage on capacitor C2 at this time is $.13V$. Equation 9.8 with V_{max} set to $.13mV$ and E_{min} set to the initial energy on C2 will give the energy from C1 that resupplies C2. Finding the amount of energy from C2 that leaves the converter during this state was also found using equation 9.8 with the maximum voltage as $.13mV$ and the minimum as the final energy value of C2 in this operating state. To find the contribution from capacitor C1 during this operating state all that remains is finding the amount of energy consumed by the switch resistance. For this particular case, the voltage seen across the parasitic switch resistance was found to

be:

$$V_{loss} = (2.9414 \cdot 10^{-4}) \cdot e^{-8999.5 \cdot t} + (7.1036 \cdot 10^{-2}) \cdot e^{-7.2626 \cdot 10^{6} \cdot t} \tag{9.16}$$

Using equation 9.10 and equation 9.12 the energy consumed by the switch resistance is determined. The value is in table 9.3. Equation 9.13 it gives the energy that reaches the load. The obtained result is available in table 9.3.

The average power was determined using equation 9.15. The results were then used along with the average incoming power to determine the converter efficiency. These results are also in table 9.3.

Table 9.3: Test result for outgoing power and transfer efficiency.

outgoing energies and powers		
E_{out}^{load}	$8.5 \cdot 10^{-8}$	J
P exiting converter	4.2	mW
η	70.8	%

Conclusion

In this paper a methodology to determine transfer efficiency for the switched capacitor power electronic converter is presented. An investigation using real values reveals the disadvantage of this particular choice of converter. The energy losses qualitatively observed in section 8.1 are now quantitatively reflected in the efficiency values obtained for the particular converter instance examined. Compared with conventional power electronic converters (which can approach almost 100% efficiency depending on the design), this efficiency results in table 9.3 is very unimpressive. However bear in mind that this paper merely presents a technique to determine efficiency. This converter is operating under conditions similar to those presented in paper [30]. The behavioral model in section 8.1 ignores many non-ideal parasitic elements that could, in practice, impact the observed efficiency.

9.2 Proposal and Evaluation of Two Methods to Improve Efficiency of the Step Down Switched Capacitor Converter

Introduction

For Stargrazer One to the practical, it is preferable to make the system as lossless as possible. As discussed in section 9.1, the switched capacitor step down power converter will present a loss. This is due to the behavior of the converter. Using the switching pattern presented in paper [30], the efficiency was found to be 70.8%. During the course of these studies several observations were made which suggests possibilities to optimize performance. These optimizations mainly entail simple modifications to the switching scheme proposed in article [30]. This paper presents the proposed switching pattern modifications. The adjustments are presented in this list:

- The time that the switched capacitor converter remains in State Two will only be sufficiently long enough for the sample and hold circuitry to successfully collect the voltage value on capacitor C1.
- State three will be held until capacitor C1 has completed replenishing charge in capacitor C2.

State one will need to be free to adjust as the converter is interacting with the solar cell source during this time. This is not the case in State Two or State Three. This paper will discuss each presented modification individually. First, the modification will be explained in detail with emphasis on why the listed adjustment is considered an optimization of converter performance. Then, the discussion will present experimental studies validating the proposed improvements.

State Three Time Adjustment

Discussion

When capacitor C1 is connected to capacitor C2, there will be a period of time where charge moves between the devices. The quantitative relationship governing this exchange was determined in section 8.1. The relevant equation is presented for reference:

$$\begin{bmatrix} V_{C1}(t) \\ V_{C2}(t) \end{bmatrix} = K_1 * \vec{u_1} * e^{\lambda_1 * t} + K_2 * \vec{u_2} * e^{\lambda_2 * t} \tag{9.17}$$

Where λ_1,λ_2 are eigenvalues, $\vec{u_1}$, $\vec{u_2}$ eigenvectors and K_1 and K_2 are constants. The discussion on how to determine these values is available in section 8.1.

The increase observed in the voltage of capacitor C2 is from new charge from capacitor C1. Eventually a maximum is reached and then the observed voltage starts to decay. The remaining time after this maximum sees an insignificant amount of charge movement. The observed current approaches a very small value after the voltage on capacitor C2 completes its increase. Upon reaching this peak voltage, capacitor C1

has finished delivering the overwhelming majority of the harvested energy to capacitor C2. Therefore, all that is being accomplished by remaining in State Three is to further deplete the charge on both devices. Remaining in State Three will also contribute to increasing the initial voltage difference observed between capacitors C1 and C2. This has been found to increase the amount of charge lost in the switch resistances. Therefore, remaining in State Three for only as long as necessary will help minimize loss.

"As long as necessary" should be defined as the time needed to reenergize capacitor C2. How to determine this point is discussed in section 9.1. How to optimize a fixed State Three duration to remain in this state for as long as necessary is available in appendix 15.3.

Procedure

This section will investigate any efficiency gains by applying the recommended adjustment to State Three time on a physical example. This was examined in the Maple and MATLAB environments. The following tables present design choices and parameter values for the converter. Table 9.4 presents the values for the converter devices and for the solar source used in the test. Table 9.4 also presents design choices (namely the lengths of the other two states and the total number of equal partitions of State One chosen to estimate incoming energy).

Table 9.4: Test conditions for adjusting State Three duration experiment.

design choices

converter

Capacitor 1	17	μF
Capacitor 2	20	μF
Load	3	Ω
switch resistance	.015	Ω

solar cell

short circuit current	.15	A
reverse bias current	1e-7	A
thermal voltage	.025	V

testing parameters

$T_{State\,Two}$	10	μs
$T_{State\,One}$	5	μs
M	1000	partitions

Additional relevant testing parameters are presented below:

- State Three durations of 5 and 1 μs will be examined and compared. The 5 μs case results in a switching pattern similar to the case study in section **??**.

The $1\mu s$ case represents a plausible optimization of State Three based on the observed behavior of this instance of the switched capacitor converter.

- Durations for States One and Two are the same for both studies.
- The solar cell is characterized by the basic model given as:

$$I(t) = I_{short} - I_o * \left(e^{\left(\frac{V(t)}{V_{thermal}}\right)} - 1 \right) \tag{9.18}$$

- The only significant non-ideality is the on resistance of the switches. All other non-idealities are assumed negligible.
- The switching of the transistors is ideal.

For each selected case study, the first task was to determine the steady state voltage values. Using the voltage model defined in section 8.1, a MATLAB script was prepared to estimate the steady state voltages. Once these voltage estimates are found, the efficiency was then determined. This was done in the Maple environment. The definition of efficiency used is the same as for section 9.1. They are repeated below for reference:

$$\begin{aligned} \eta &= \frac{P_{out}}{P_{in}} \\ \eta &= \frac{\frac{E_{out\,to\,load}}{t_{cycle}}}{\frac{E_{from\,solar\,source}}{t_{cycle}}} \end{aligned} \tag{9.19}$$

For each selected time value, the power entering and exiting the system was determined. The procedure to determine these values is the same as the one used in section 9.1. Once the appropriate values are known equation 9.19 is applied to obtain the efficiency

Results

Table 9.6 shows there is an improvement in efficiency. This supports the argument for performing this adjustment. The efficiency gain is modest (only ≈ 2.8 percent). Note that the average power values and steady state voltage values for the $1\mu s$ State Three length case are notably higher. It is known that the converter will adjust the charge held in capacitors C1 and C2 in order to operate under conditions where charge entering equals charge departing. The observed voltage increase suggests that the converter needed to collect charge in order to reach the operating condition discussed in the previous sentence. The observed power increase suggests that this new operating point is likely closer to the maximum power point then the $5\mu s$ case.

Table 9.5: Resultant steady state voltage values obtained from adjusting State Three time. The minimum and maximum voltage values for capacitors C1 and C2 are presented.

tested intervals		
5	1	μs

capacitor C1		
.12	.16	V
.17	.20	V

capacitor C2		
.09	.12	V
.12	.16	V

Table 9.6: Resultant power and efficiency values from adjusting State Three time.

tested intervals		
5	1	μs

entering system		
6.0	8.9	mW

exiting system		
4.2	6.5	mW

efficiencies		
70.6	73.5	%

Minimize State Two Time

Discussion

During this state, capacitor C1 is not performing any useful function. The relevant purpose of this state is just to facilitate voltage sampling on capacitor C1. Therefore, minimizing this time will help reduce the amount of charge lost in the switch resistances.

Procedure

The procedure is identical to the previous case study for State Three. Table 9.7 outlines selected converter and source values along with relevant test choices. Unlike the case study for State Three, four different candidate State Two lengths will be examined.

Table 9.7: Parameters for the adjusting State Two duration experiment.

design choices

converter

Capacitor 1	17	μF
Capacitor 2	20	μF
Load	3	Ω
Switch loss	.015	Ω

solar cell

short circuit current	.15	A
reverse bias current	1e-7	A
thermal voltage	.025	V

testing parameters

$T_{State\,Three}$	5	μs
$T_{State\,One}$	5	μs
M	1000	partitions

Results

Table 9.8: Resultant steady state voltage values from adjusting State Two time.

tested intervals

10	5	1	.5	μs

capacitor C1

.12	.16	.21	.21	V
.17	.20	.25	.26	V

capacitor C2

.09	.13	.19	.19	V
.12	.16	.21	.21	V

The result is comparable to the previous investigation. Reducing the time spent in State Two results in an improvement in performance. The observed improvements are nontrivial. Halving the State Two duration increases the efficiency by over 7%. Table 9.9 presents the results from this case study. It was observed that the capacitors stabilize at higher operating voltages as State Two's duration is reduced. Also it was observed that the average power increased as the State Two's time was reduced. Operation within closer proximity to the maximum power point and the reduced converter cycle time are players in these observed effects.

Table 9.9: Resultant power values from adjusting State Two time.

tested intervals				
10	5	1	.5	μs

power entering system				
6.0	9.5	15.9	17.1	mW

power exiting system				
4.2	7.4	13.6	14.8	mW

efficiency				
70.6	78.5	85.7	86.7	%

Optimized DC/DC Converter for Stargarzer One

This section has demonstrated that the optimization of States Two and Three does have a positive impact on the performance of this type of converter. A valid question is how much gain can be achieved by optimizing both states simultaneously. This section presents an example. The times for State Two and Three will be adjusted to optimal values that could be used in a real Stargrazer One design. The efficiency value obtained will be compared to the baseline results presented in section 9.1.

Design choices and converter parameters are as presented in table 9.10. States two and three time values are in table 9.11.

Using the procedure outlined in section 9.1, the final results were obtained. The operating voltage results are in table 9.12. The power and efficiency results are in table 9.13.

Conclusion

While less efficient than more common power electronic converters, using this step down switched capacitor converter permits a compact Stargrazer One design. Despite the apparent shortcomings with this particular converter, a competitive efficiency value can be obtained with the optimizations proposed in this section. A keen observer may note that a sufficiently long State One duration will diminish the performance gains obtained by this optimization. Appendix 9.2 presents an example using the optimized time settings for States Two and Three proposed in this section. With prudent design, a competitive efficiency can be achieved for all possible State One values.

The development of a better performing converter is beyond the scope of this thesis. Such a project is a worthwhile direction for future research.

Table 9.10: Device values for optimized converter test.

design choices

converter		
Capacitor 1	17	μF
Capacitor 2	20	μF
Load	3	Ω
Switch loss	.015	Ω
$T_{State\,One}$	5	μs

solar cell		
short circuit current	.15	A
reverse bias current	1e-7	A
thermal voltage	.025	V

testing parameters		
M	1000	partitions

Table 9.11: State time values for optimized converter test. Both cases see the same duration of State One. A 1 μs total State Two duration correspond to two time periods in the state each lasting 500 ns. There are sample and hold circuits which can work inside this timeframe.

test choices		
basal	optimal	
State Two time		
10	1	μs
State Three time		
5	1	μs

Table 9.12: Resultant steady state voltage values from optimal converter test.

capacitor C1		
basal	optimal	
.12	.29	V
.17	.33	V

capacitor C2		
basal	optimal	
.10	.26	V
.12	.29	V

Table 9.13: Resultant power values from optimal converter test.

power entering system		
basal	optimal	
6.0	28.7	mW

power exiting system		
basal	optimal	
4.2	25.4	mW

efficiencies		
basal	optimal	
70.8	88.6	%

Chapter 10 Adapting the Step Down Converter For Stargrazer One

10.1 Analysis of this Converter's Response to Changes and the Impact on the Design of Stargrazer One

Introduction

For this type of DC/DC power converter, the input, output and internal node voltages are maintained by storing charge inside the capacitors of the converter. Adjusting the charge to respond to voltage changes will not be instant. This characteristic must be examined because the performance of Stargrazer One may be affected. The aims of this section are to ascertain the impact of this behavior on Stargrazer One and provide a procedure that will allow one to estimate when it is safe to perform a power computation. This section presents a series of experiments performed to address these issues.

The section will begin by explaining, at a high level, the behavior observed as the converter responds to change. Then the paper will evaluate the impact towards Stargrazer One performance.

Behavior

In chapter 8, the voltages seen in the converter are functions of the voltages on the capacitors. In chapter 8, the capacitor voltage was seen to oscillate within a fixed band. These voltage values observed are a function of the charge in the capacitors of the converter. Changes in light, temperature and the switching action of the transistors will alter the charge flowing through the converter. The converter's operating voltages will readjust as a result. To accomplish this, the total charge in the capacitors will increase or decrease. Due to the fact that the converter must still deliver charge to the load, this transition will be gradual. If a change causes excess charge to enter, some charge will accumulate on the capacitors. The band of voltages the capacitors assume will increase. When a change causes a deficiency of incoming charge, the deficit is compensated by the charge stored in the capacitors. The band of voltages the capacitors assume will decrease. Once charge entering and exiting the converter has been equalized, the operating voltages will cease to change and stabilize within a constant voltage band resembling the behavior observed in chapter 8. The converter will have reached a new steady state.

Impact on Stargrazer One

The purpose of this study is to determine if the transition delay for this switched capacitor converter can cause Stargrazer One to function improperly. As demonstrated in chapter 8, the converter voltage behavior is cyclical in nature. Therefore, the operating point shift can be tracked by simply following the voltage oscillations seen on the capacitors. The studies presented in this section was performed in the MATLAB

environment. In the script, a working model of the switch capacitor converter was created. The converter is modeled using the equations developed in section 8.1. A basic solar cell model was used for the source. A more detailed source model is not necessary for this experiment. The solar cell model is defined as:

$$I(t) = I_{short} - I_o * \left(e^{\left(\frac{V(t)}{Vth}\right)} - 1\right); \tag{10.1}$$

Where I_{short} is the solar source short circuit current, I_o is the reverse bias current and Vth is the thermal voltage.

An equation level implementation of the perturb and observe power point tracking algorithm is included. These pieces (the solar cell, the power converter, the tracker) are able to interact. The interaction resembles actual operation. Two test cases will be studied:

- The tracker will collect voltage data for the next adjustment immediately after the previous adjustment ignoring the behavior of the switched capacitor converter.
- The tracker will collect voltage data for the next adjustment after a fixed delay from the previous adjustment.

Both cases will be examined under the same procedure which is outlined in the following section. Results and conclusions will come afterward.

Procedure

For both cases will be examined:

- Initialize the system to a predefined starting point. This reflects the fact that Stargrazer One will begin tracking at an intermediate value of State One.
- For a fixed number of iterations, allow the tracker to perform calculations and adjustments to the duty cycle in response to simulated environmental change. In this experiment: both test cases will see a total of three environmental states. For the case of immediate recalculation, 50 adjustments will occur per state. For the case of a delay between calculations, 35 adjustments will occur per state. The difference in adjustments is to avoid excessive simulation times.
- Record the capacitor C1 voltage, computed powers, and State One duration for each adjustment.

Results With Conclusions

For this experiment, table 10.1 presents used design choices and initial values.

Figure 10.1 presents the simulation test waveform used for the test cases. Performing the discussed procedure using the values in tables 10.1 and gave the following results. Figure 10.2 presents transistor duty cycle adjustments for the case of no pause

Table 10.1: Design choices for the experiment. T_2, T_3 are the lengths of States Two and Three which remain fixed throughout the test. $T_1(0)$ is the initial duration for state 1. State One will vary throughout the test. ΔT is the perturbation step size for adjusting State One.

device values:		
C1	17	μF
C2	20	μF
R	.015	Ω
L	3	Ω

solar source parameters:		
I_{short}	.15	A
$V_{thermal}$	25	mV
I_o	1e-7	A

test parameters :		
$T_1(0)$	2	μs
T_3	1	μs
T_2	1	μs
ΔT	.5	μs
T_{wait}	20	cycles

between adjustments. Figure 10.3 presents transistor duty cycle for the case where a wait is included. Also included is the observed capacitor C1 voltage. The case of no delay between computations is given in figure 10.2 and the case of a delay is given in figure 10.3. Relevant observations will be presented for each case studied.

- No delay between computations: The case of immediate adjustment shows undesirable system performance. Figure 10.2 shows the system reacting to the voltage adjustments inside the converter. This is most apparent during the response to the second environmental condition (see figure 10.2). The voltage on capacitor C1 falls while the tracker is oscillating. This decay is from the charge re-balancing in the switched capacitor converter. Ideally, the tracker should only oscillate at the maximum power point. The tracker appears to be confused by the charge redistribution in the converter. The other two transitions show sensitivity to the capacitor charge in the converter. Figure 10.2 shows the tracker overshooting the maximum power point for two of the environmental conditions. The tracker did eventually reach and oscillate about the maximum power point.

- Fixed wait between computations: Figure 10.3 shows a contrasting behavior than for the case of no delay depicted in figure 10.2. Figure 10.3, shows the system promptly seeking and remaining at the maximum power point for all three environmental states (Note that for the second environmental state, the tracker

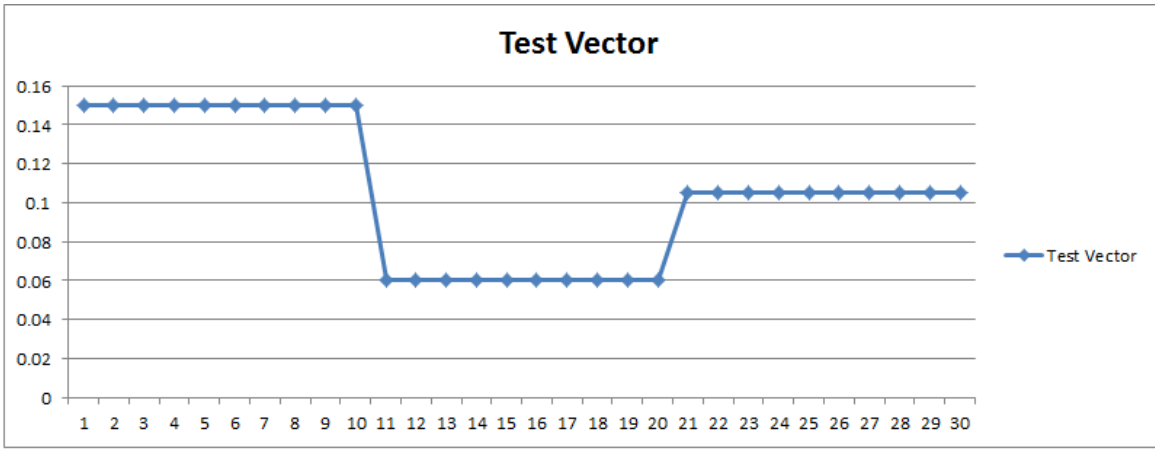

Figure 10.1: Example test vector for the experiment. The X axis is the number of adjustments. The Y axis is the short circuit current of the solar source. A reduced total number of adjustments is used to present a clear illustration of the test vector.

failed to reach the maximum power point within the 35 adjustments allowed per environmental state). Given the observed behavior for the other two states, it is safe to assert that the tracker would have reached and maintained operation at the maximum power point. The response in figure 10.3 shows the tracker only reacting to the changes in the environment. The charge adjustments in the converter has no effect.

These simulation data demonstrates that immediate computation of powers will cause Stargrazer One to be sensitive to the converter. It is preferred to have Stargrazer One react solely to changes from the solar cell source. Sensitivity to the power converter clearly interferes with the maximum power point trackers ability to seek and operate the solar source at its maximum power point.

The idea of simply waiting between computations of power presents a very simple solution to this problem. As is observed (see figure 10.2), applying a 20 converter cycle delay between computations resulted in the tracker being insensitive to the voltage adjustments in the switched capacitor converter.

Placing a delay between computations comes at the expense of response time. Too long a wait will result in delayed response to changes. This means that rapid environmental changes may be missed resulting in power loss. Too brief a wait may introduce sensitivity to the converter. In this thesis, a constant delay was used in the implementation of Stargrazer One. Developing a more systematic method of determining this delay is a topic for future research.

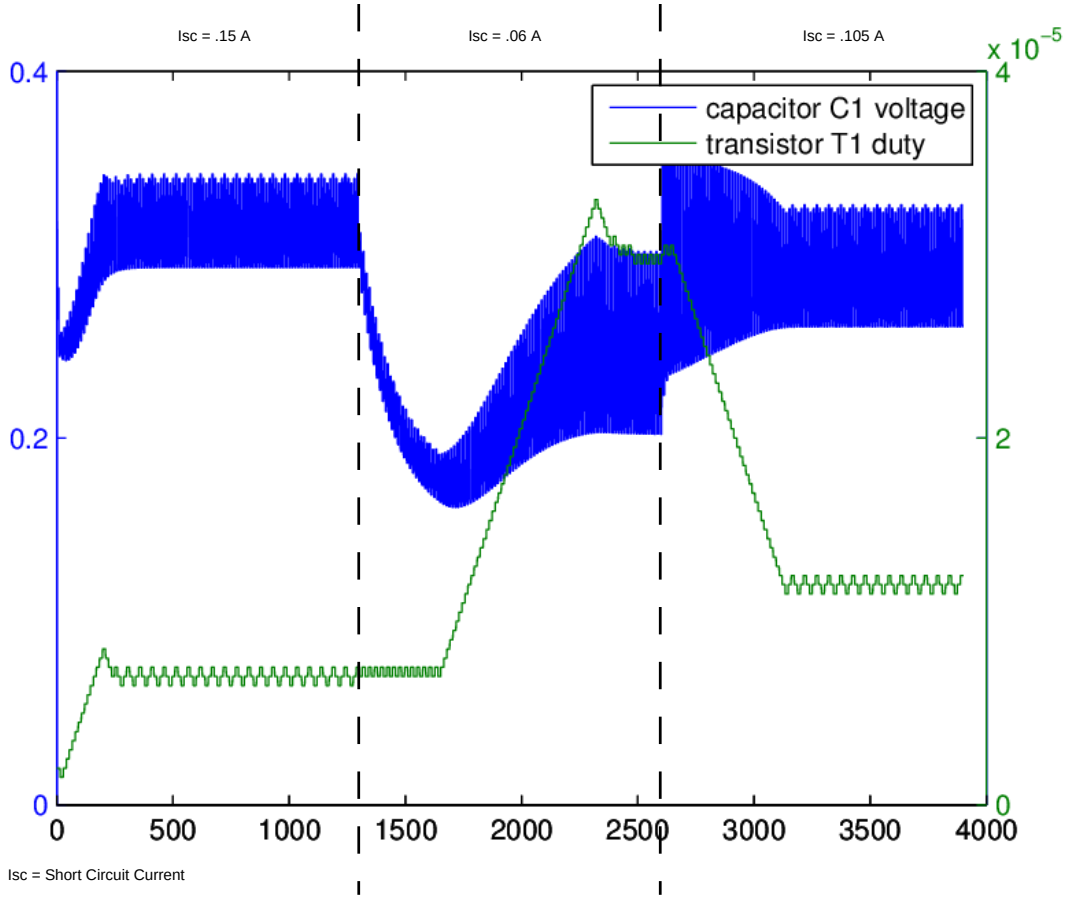

Figure 10.2: The observed capacitor C1 voltage and transistor T1 on times for the case of no wait between computations using the test vector in figure 10.1. The output corresponding to each environmental condition is labeled. The transistor T1 on time appears as a stepwise linear function. This is to accommodate the simultaneous viewing of both capacitor C1 voltage and transistor T1 on time as time progresses. X axis is the number of data points from time t = 0. The Y axes is voltage in V for capacitor C1 and time in s for the transistor T1 on time.

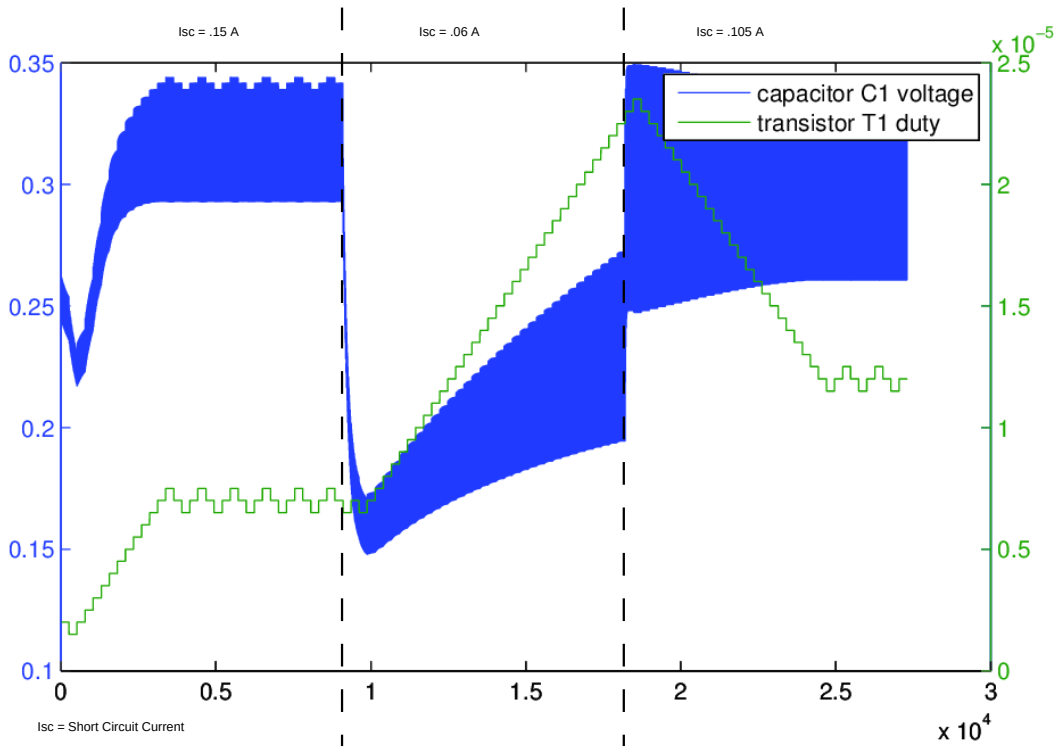

Figure 10.3: The observed capacitor C1 voltage and transistor T1 on times for the case of a wait between computations using the test vector in figure 10.1. The output corresponding to each environmental condition is labeled. The rather dense plot for the capacitor C1 voltages is due to the several iterations that occur between adjustments. The transistor T1 on time appears as a stepwise linear function. This is to accommodate the simultaneous viewing of the capacitor C1 voltage and the on time. X axis is the number of data points from time t = 0. The Y axes is voltage in V for capacitor C1 and time in s for the transistor T1 on time.

Part III

The Stargrazer One Control Architecture

Chapter 11 Introduction

11.1 Introduction

The major contribution of the Stargrazer One concept is a digital architecture for use in solar cell maximum power point tracking applications. The major design objectives favor simple and low hardware solutions. The best choice to meet these objectives is a specialized digital circuit. The general purpose processors while capable of operating with notably small power needs do contain far more hardware then will ever be used by Stargrazer One. Additional savings in power and in size would be achieved if this extraneous hardware was not present. Furthermore, use of a custom solution will permit the designer to further optimize the design. This chapter will present the first generation digital architecture to be used in the maximum power point tracker.

11.2 Architectural Overview

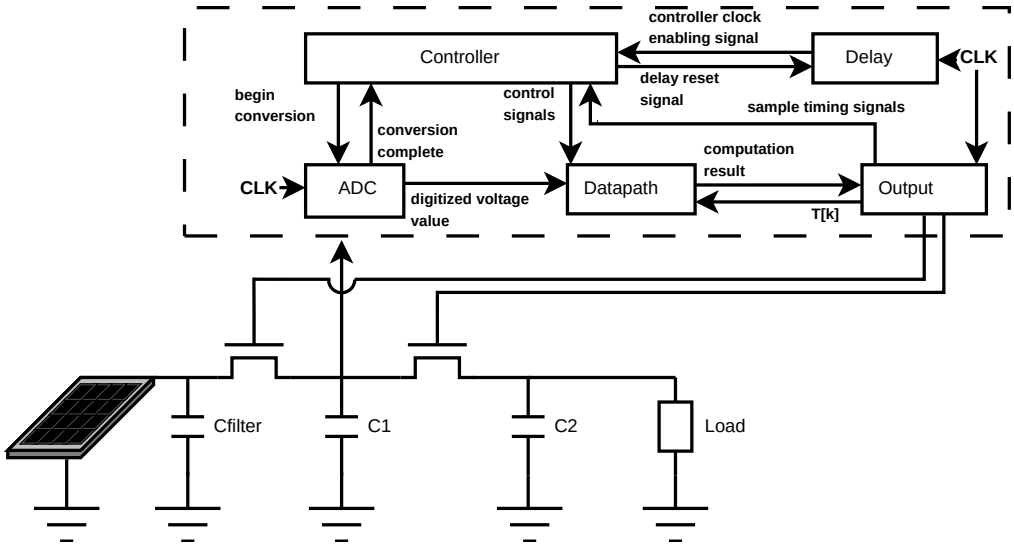

Figure 11.1: Top level view which visually depicts how data moves inside the Stargrazer One system. Details on the exchanged information are discussed throughout this chapter and summarized in list format in this introduction.

Figure 11.1 presents a top level view of the proposed maximum power point tracker. Figure 11.1 also presents how information moves in the proposed system. A keen observer will note that the data path and control circuits when viewed together behave like a special purpose processor. Extending this analogy will permit an introductory explanation to the function of these two important blocks. The control circuitry contains the program to execute the perturb and observe maximum power point tracking algorithm. The data path circuit contains the required tools for the program to complete its function. The function of the program is to determine how

the transistors of the power electronic circuit should be adjusted. Specifically the current power $P[k]$ and previous powers $P[k-1]$ are determined. Then, the following is evaluated:

$$P_[k] \leq P_[k-1] \tag{11.1}$$

Where $P[k-1]$ is the previous computed power and $P[k]$ is the current computed power.

The result of equation 11.1 determines how the transistors should be adjusted. The output circuit executes this adjustment. The output circuit drives the transistors in the switched capacitor power converter. To execute the duty cycle adjustments needed for power point tracking, the unit must interact with the other circuits. This unit must know when capacitor C1 is open circuited. This information is sent to the control circuit so that the control circuit will know when to instruct the analog to digital (ADC) circuit to begin work. The delay circuit interacts solely with the control circuitry. Its purpose, as elaborated in section 13.4 is to create the needed pauses between power computations. How these pieces interact is graphically shown in figure 11.1and discussed in detail throughout this chapter.

Figure 11.1 presents how the major pieces of the Stargrazer One architecture communicate with each other as they perform their duties. The information communicated along with the direction of transmission is presented in figure 11.1. A brief explanation of the each signal is now presented:

- *begin conversion*: This signal notifies the analog to digital converter to begin work preparing a voltage value from capacitor C1.
- *conversion complete*: This signal will be sent to the control circuit once the appropriate sampled voltage value has been digitized and ready for use. the control circuit is designed to pause at predetermined states until this signal is received.
- *digitized voltage*: This is the conversion results from the analog to digital converter.
- *control signals*: This single line represents multiple signals which all perform the same general function. These signals instruct how the data path executes a particular instruction.
- *computation result*: This signal returns a binary one if the inequality 11.1 evaluates false, the signal is binary zero otherwise.
- *controller clock enabling signal*: In order to insure the system waits for the appropriate amount of time between samples, the control circuit employs clock enabling. When this signal is binary zero, the control circuit cannot advance effectively freezing it.

- *delay reset signal*: This signal resets the delay circuit so that the system will continue to wait for the appropriate amount of time between adjustments. This signal is necessary due to the architecture used to create the delay circuit.

- *sample timing signals*: This single arrow represents two signals. Whenever capacitor C1 is open circuited one of these represented signals is binary one. Only one of the signals will be binary one during this time. the purpose is to be able to notify the control circuits when capacitor C1 is at a maximum or minimum voltage. Both these values are required to evaluate the inequality 11.1.

- $T[k]$: This is defined as a complete converter cycle duration. This value is computed inside the output circuit block and is sent to the data path circuits. this value is needed to successfully compute the power values for evaluating inequality 11.1.

- CLK: The clock for the system

When the tracker is to be first used, it should be initialized. Each functional element has the appropriate hardware necessary to handle initialization. The entire system will be cleared when the initialization signal is binary one. The physical production of this initialization pulse can be very simple. Tying this port to a debounced switch or button is sufficient. Once initialized, the tracker can work independently.

What is not included in this proposed design is the clock generation and analog digital conversion circuits. These circuits were considered outside of the scope of this project which is to present a unique architecture which performs maximum power point tracking. However, putting this circuit to work will require these elements. There already exist numerous implementations of these circuits in the literature. This includes efficient, compact solutions ideal for Stargrazer One. An appropriate clock generator can be implemented to service Stargrazer One with no modifications to the Stargrazer architecture. The architecture only requires the output from the clock generator to function. The analog to digital converter may require additional hardware between Stargrazer One and the converter to properly function.

The entire Stargrazer One power point tracking system is customized. Therefore, this article will proceed by discussing each major component individually. The major components to be discussed are the output circuit, the data path, the control circuit and the delay circuit. Each of these functional units will be discussed individually. For each section, this document will begin by discussing the architecture developed and then proceed to present simulated performance results.

11.3 Simulation Procedure

Before proceeding into the discussions on the circuitry, it is important to outline how they will be tested. Where possible circuits were verified correct. Depending on the circuit, the goal will be to either validate or verify correct performance. Complex

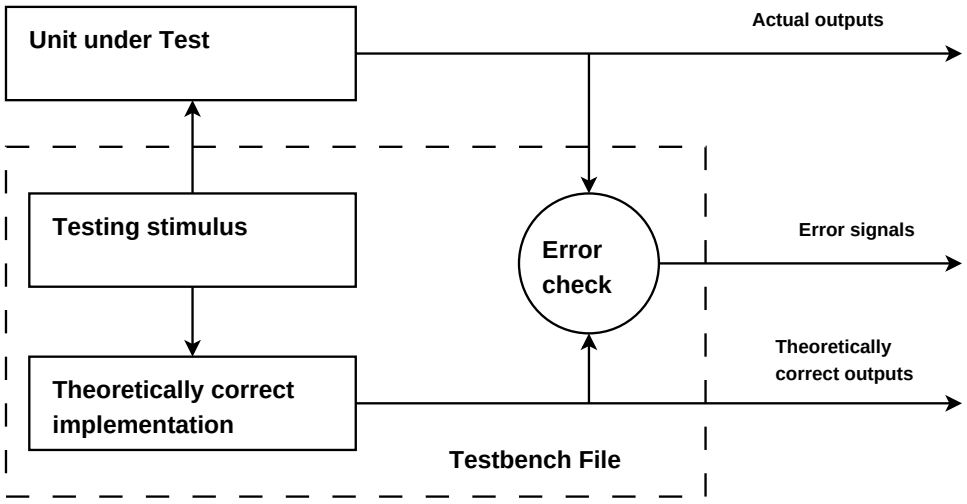

Figure 11.2: Flowchart showing how testing will be implemented. The same format will be used for both behavioral and post place and route testing.

systems are sometimes too difficult to verify. The words "verify" and "validate" are now defined for this context :

- verify : The circuit under test is proven to work under all possible input combinations.
- validate : The circuit under test is demonstrated to work according to the design specifications.

All these circuits were designed using what is known as a structural approach. Simple basic blocks were defined then used to build larger modules. Finally these modules were combined to form the circuits presented. Testing occured at each level of design. It was possible to verify these smaller pieces and some of the larger modules. However, as will be demonstrated in this chapter, the final circuits could only be validated. This is due to the complexity of the circuits under test.

Each circuit developed underwent two rounds of testing. They are described in the following list:

- behavioral : The circuits to be tested are studied under ideal conditions. The intention is to make sure that the circuit functions as expected to input stimuli.
- post place and route : Timing delays associated with the target hardware [in this case a field programmable gate array (FPGA)] are included inside the circuit to be tested. The intention is to make sure that the circuit will function as expected in the presence of these non-ideal effects.

Figure 11.2 shows how the testing will be performed for both rounds of study. Note that the test bench file presents stimuli to the circuit to be studied along with providing a theoretically correct implementation. These stimuli will resemble what

the tested circuit will see in actual use. The theoretically correct implementation is another instance of the circuit to be tested. The implementation style differs from the actual unit to be tested and this implementation is rigorously examined for correctness. For ease of testing, the error checking block compares the outputs from both circuits. This block is designed to output 1 bit signals which return binary 1 when a particular signal set does not match. For ease of troubleshooting , the output signals from both implementations and the error signals are presented as output.

This chapter will present representative trace images from this testing to demonstrate that the particular circuit module under discussion functions as expected. Wave traces showing posts place and route and behavioral results will be included. For reference, the content of this section will be briefly recapped during each simulation section.

11.4 Chapter Contents

The sections in this chapter will discuss the circuit modules in the following order. All discussions will include details on the architecture and simulated results.

- Chapter 12 presents a validation of the whole Stargrazer One architecture.
- Chapter 13
  - Section 13.1 will discuss the data path circuit.
  - Section 13.2 will discuss the control circuit.
  - Section 13.3 will discuss the output circuit.
  - Section 13.4 will discuss the delay circuit.

Chapter 12 Proposed Architecture Validation

12.1 Introduction

The purpose of this section is to present a validation of the proposed architecture discussed in chapter 11. The entire system was subjected to testing. This section will begin by briefly reviewing how the completed architecture will appear. Then the section will proceed to discuss the tests performed and present results. As seen in chapter 11, the Stargrazer One system is composed of several major functional unit. For details on each functional unit, please refer to chapter 13.

12.2 Test Description

A Verilog hardware description language module was defined. The coding style of this developed module is structural. A test bench was created presenting input vectors and a theoretically correct implementation of the entire Stargrazer One system. Both implementations will see the same input test vectors. Testing will be done at the behavioral and post place and route levels.

To determine if the system is functioning properly, the proposed architecture was selected to test cases. Two will be presented in this chapter:

- Case One: The capacitor C1 minimum and maximum voltage will be increasing at a rate of 1 unit per $6ms$. If functioning properly, Stargrazer one should proceed towards the smallest available State One duration. In the case of an increasing voltage, the tracker should eventually see that smaller transistor T1 on times gives an increased power value.

- Case 2: The capacitor C1 maximum and minimum voltage will be decreasing at a rate of 7 units per $2.5ms$. Stargrazer One should again proceed towards the smallest available State One duration. The tracker should again see that the smaller duty times give better power results.

12.3 Test Results With Conclusions

Case One

Figures 12.1 and 12.2 present representative samples from a behavioral validation simulation run. The figures present all stimuli and relevant test outputs. For each output, the result from the actual architecture and the theoretically correct test vector are presented. They are labeled “actual” and “expected” respectively. The result from the comparison of these signals is labeled “discrepancy”. The “discrepancy” signal is binary zero if the signals match and becomes binary one otherwise. The signal labeled “testing complete” is a signal which turns binary one when the test is

concluded. Observed "spikes" in the "discrepancy" signals for test outputs are due to instantaneous propagation delays (an artifact of the simulator).

In both figures 12.1 and 12.2 show that the proposed architecture matches the theoretically correct output. Figure 12.1 demonstrates that both implementations not only match but perform as expected . The signal labeled "State 1 duration" is clearly observed decreasing toward the minimum values possible. Once there, the system remains at that value. This is in accord with the expected performance for this test case. Once at the minimum value, the system was found to remain at this value. Figure 12.2 provides additional support for this observation. Figure 12.2 presents how the architecture behaves when presented with a voltage change. Figure 12.2 shows the architecture operating at the minimum State One times possible. As the voltage change is an increase, there is an observed increase in the State One duration but this is temporary. The proposed architecture quickly returns to minimum value operation. This reflects expected operation. Post place and route level testing produced similar results.

Case Two

As with case one, figures 12.3 and 12.4 present representative samples from a behavioral validation simulation run. As with case one, the figures present all stimuli and relevant test outputs. For each output, the result from the actual architecture and the theoretically correct test vector are presented. They are labeled "actual" and "expected" respectively. The result from the comparison of these signals is labeled "discrepancy". The "discrepancy" signal is binary zero if the signals match and becomes binary one otherwise. Observed "spikes" in the "discrepancy" signals for test outputs are due to instantaneous propagation delays (an artifact of the simulator).

Figures 12.3 and 12.4 demonstrate that the proposed architecture preform as expected. Figure 12.3 shows how the system behaves after it has been initialized. Note that the State One duration proceeds to the minimum values possible. This matches expected behavior for this case. Figure 12.4, shows an example of how this system responds to a voltage change. The voltage is diminishing in magnitude. The proposed architecture remains at minimum State One duration values as expected. Post place and route level testing produced similar results.

12.4 Conclusion

In this section the entire Stargrazer One maximum power point tracking architecture has demonstrated that it functions as expected under the tests described. The proposed architecture matches the performance of the theoretically correct system in both cases. This suggests that the Stargrazer One components correctly interact with each other. This also provides support in favor of the validity of the proposed Stargrazer One architecture as a hardware implementation for maximum power point tracking.

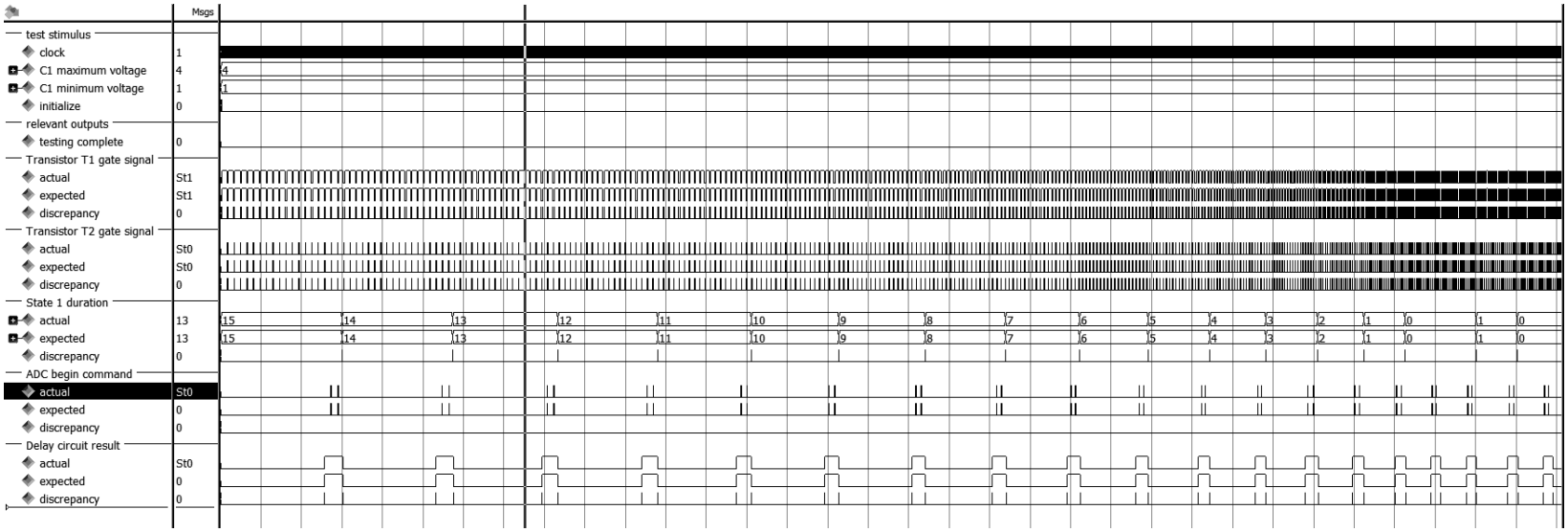

Figure 12.1: A long range view of the behavioral simulation for Case One. This trace begins from initialization. Note how the time of State One reduces to the minimum size possible as expected.

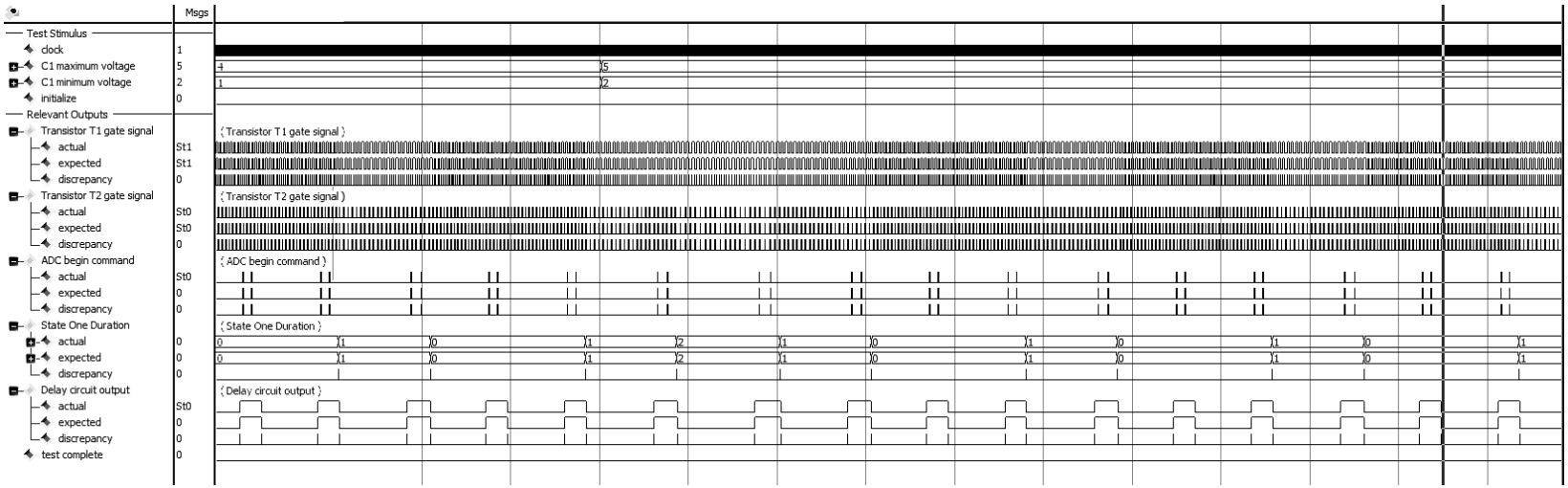

Figure 12.2: A sample of the behavioral simulation for Case One. This trace begins after the system is operating at minimum State One duration. Note the system response to the change in voltage. The system remains at the minimum designed State One durations.

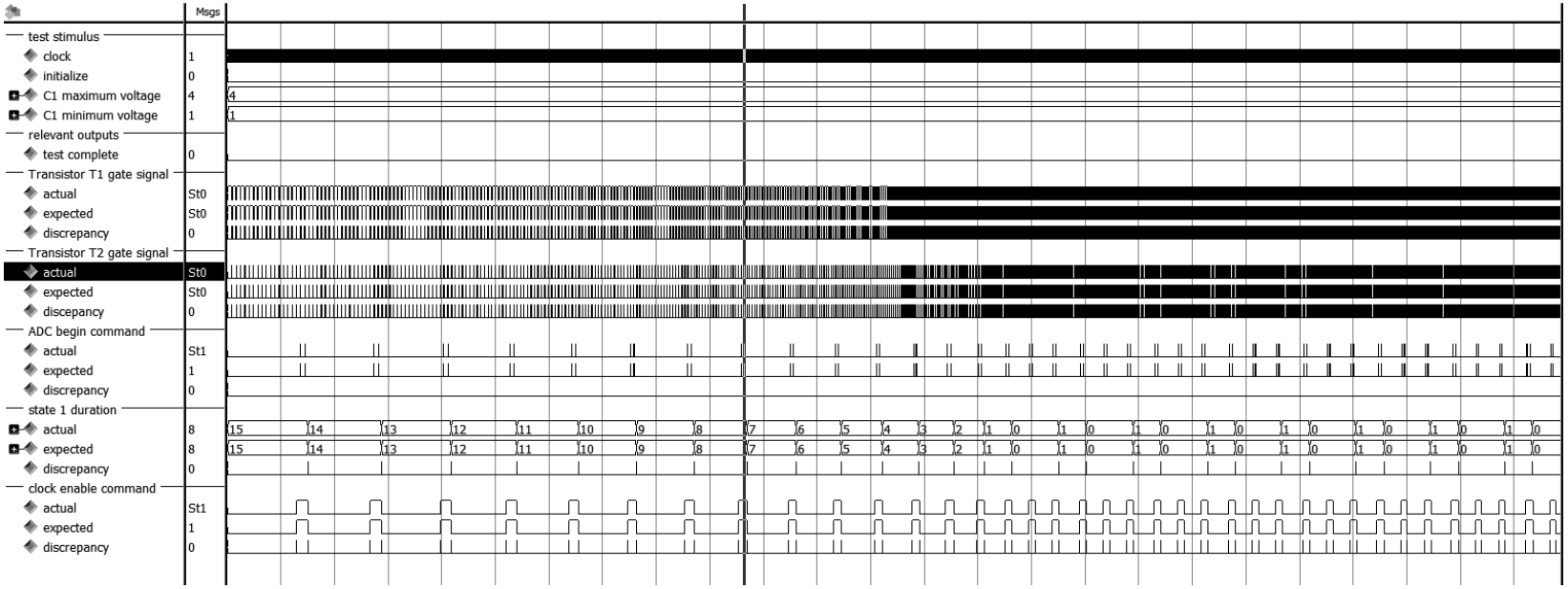

Figure 12.3: A long range shot of the behavioral simulation for Case Two. This trace begins from initialization. The primary takeaway is that the time of State One reduces to the minimum size possible as expected.

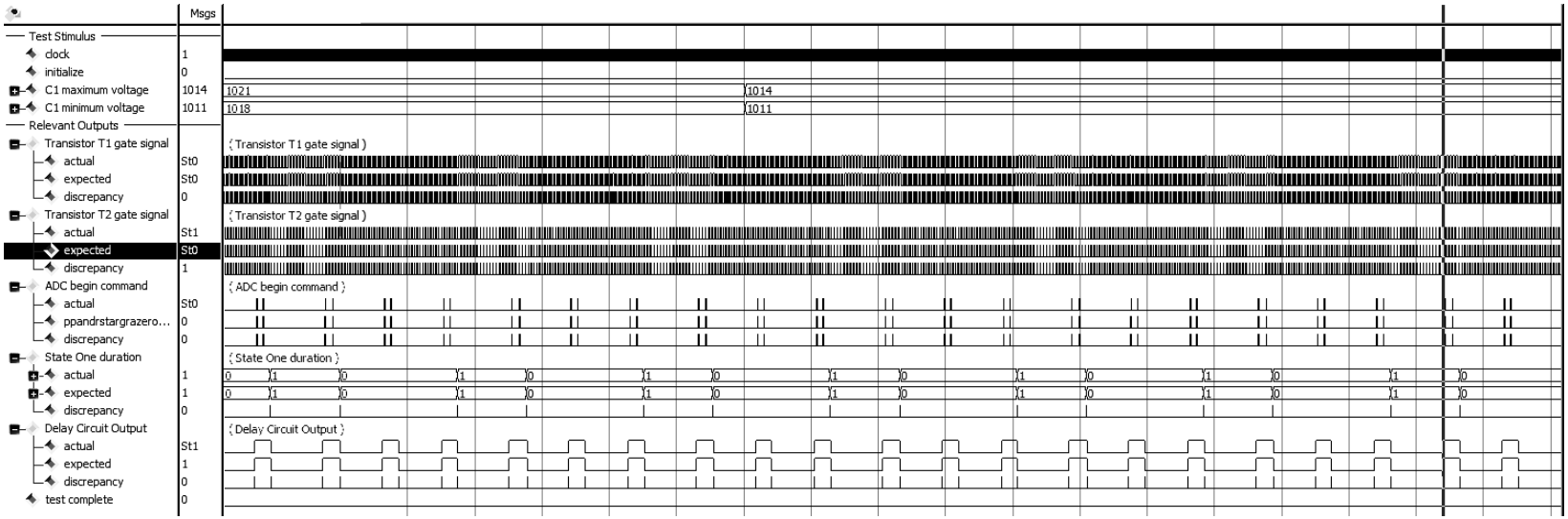

Figure 12.4: A sample of the behavioral simulation for Case Two. This trace begins after the system is operating at minimum State One duration. Note the system response to the change in voltage. The system remains at the minimum designed State One durations.

Chapter 13 Description of Architecture by Functional Block

13.1 Data Path Circuit

Introduction

This article will focus on the components of the data path circuit. This circuit interacts with the voltage data sampled from capacitor C1. This circuit computes power values and determines which direction to adjust the duty cycle of transistor T1. This circuit performs these duties under the guidance of the control circuit (this circuit will be discussed in section 13.2).

The discussion will begin with details on the architecture. Then the discussion will present simulation validation. In simulation the data path circuit will see stimuli identical to what will be encountered in actual use.

Data Path

In appendix 15.3, a technique to determine power using the chosen step down switched capacitor converter was proposed. The developed data path hardware executes the proposed method.

Figure 13.1 presents a functional block level schematic view of the proposed data path circuit. The power was computed using the following equation:

$$P = \frac{\Delta Energy}{\Delta Time} \tag{13.1}$$

As discussed in appendix 15.3, computing power in this technique requires a division operation. Division is still today a complex operation to perform with digital computers [32]. Therefore the following workaround was developed.

This system is to perform the perturb and observe method of power point tracking. This means that the system will be preparing the appropriate values to determine if the following relationship is true.

$$P_[k-1] \leq P_[k] \tag{13.2}$$

Applying the definition of power expressed in equation 13.1 followed by algebraic manipulation of 13.2 produces the following:

$$\Delta E[k-1] * T_{cycle}[k] \leq \Delta E[k] * T_{cycle}[k-1] \tag{13.3}$$

This suggests an alternative means to evaluate equation 13.2. Since time and energy for all relevant normal operating conditions remain either zero or positive the direction of comparison will not need to be switched. Equation 13.3 was validated with computer simulation. The complete discussion is in appendix 15.3.

Applying equation 13.3 means all computation involves either multiplication or subtraction. The following presentation contains the functions the datapath must perform. They are in no specific order:

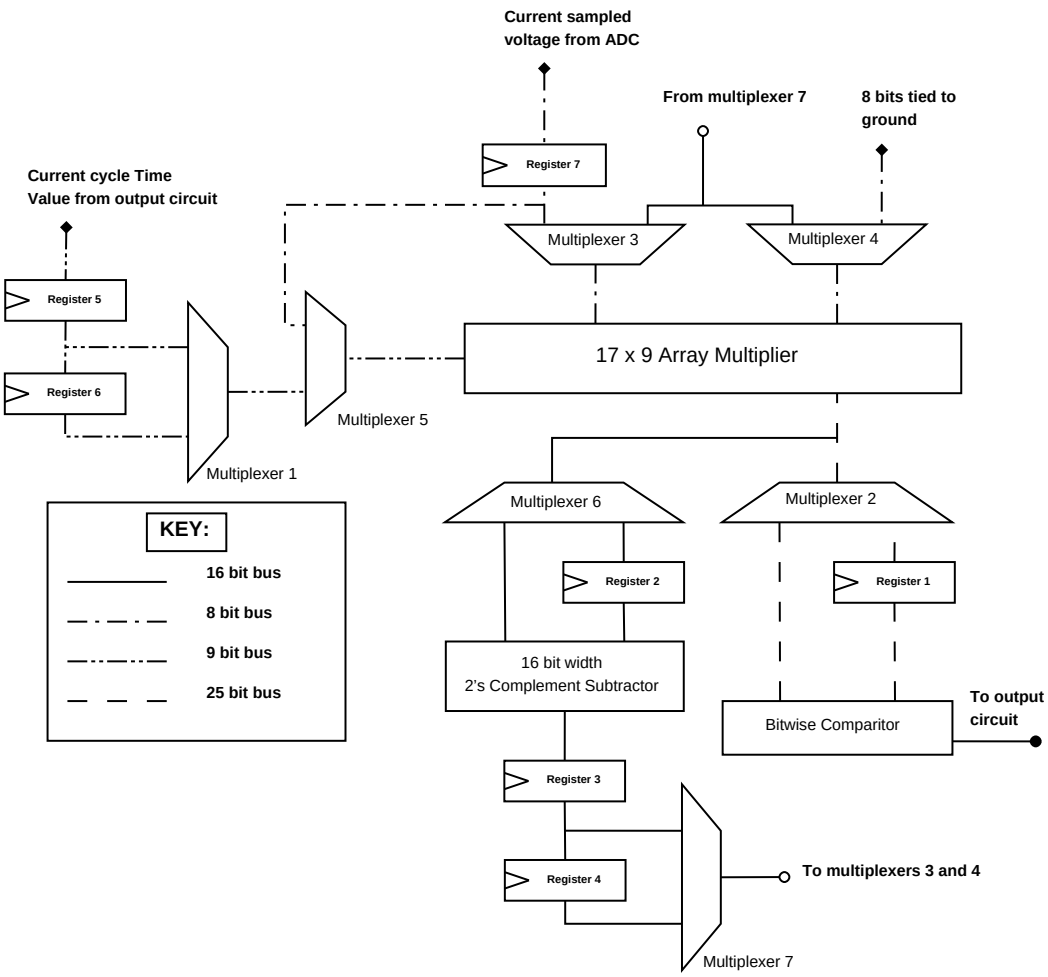

Figure 13.1: Block diagram of the proposed data path architecture.

$$Calculate : \Delta E[k-1] * T_{cycle}[k] \tag{13.4}$$

$$Calculate : (V_{C1}^{max})^2, (V_{C1}^{min})^2 \tag{13.5}$$

$$Calculate : \Delta E[k] = (V_{C1}^{max})^2 - (V_{C1}^{min})^2 \tag{13.6}$$

$$Calculate : \Delta E[k] * T_{cycle}[k-1] \tag{13.7}$$

$$Evaluate : \Delta E[k-1] * T_{cycle}[k] \leq \Delta E[k] * T_{cycle}[k-1] \tag{13.8}$$

Where $\Delta E[k]$ is the current energy leaving capacitor C1, $\Delta E[k-1]$ is this energy from the previous adjustment, $T_{cycle}[k-1]$ is the previous converter cycle length, $T_{cycle}[k]$ is the current converter cycle length, V_{C1}^{max} is the maximum capacitor C1 voltage and V_{C1}^{min} is the minimum capacitor C1 voltage.

If equation 13.8 evaluates true, this means Stargrazer One should continue to adjust T_{cycle} in the current direction. If equation 13.8 is false, the tracker must reverse the direction of adjustment for T_{cycle}.

A keen observer will note that that the equations for energy lack the constant multiplier consisting of the size of the capacitor and $\frac{1}{2}$. To reduce operations this constant term is removed from the actual energy computation. Since the constant appears in both energy terms of expression 13.6, this constant can be safely factored out. The energy values will no longer be accurate but the energy versus T_{cycle} relationship should be preserved. As long as this relationship is preserved, the power point tracker will not require accurate values. This was found to be true. The investigation is presented in appendix 15.3.

Crucial to successful operation is the need to update the stored energy and time values. These duties are accomplished with the appriopiate exchange of values in the registers of the datapath. The multiplexers and de-multiplexers insure the correct information arrives at the appropriate time to the functional blocks. Stargrazer One will perform all required computations with a subtractor and a multiplier. Details on the specific implementations of these functional blocks are in appendix 15.3.

In order to carry out the comparison in equation 13.3, the data path circuitry must perform the calculations 13.4, 13.5, 13.6, 13.7 and 13.8 first.

Functional blocks are reused. For instance, the array multiplier executes all multiplication and squaring functions. Reducing the circuit area comes at the cost of more control steps and increased execution time. This is readily observable by noting the amount of multiplexing and storage elements in the data path.

Simulation

This section will only present the validation work for the entire data path system. Simulated validation showing in detail that the proposed architecture successfully executes equations 13.4, 13.5, 13.6, 13.7, and 13.8 is available an appendix 15.3.

Procedure

In order to execute the testing, a Verilog description of the discussed architecture was created and tested in the Xilinx FPGA design environment. The design, as discussed in the previous paragraph, is composed of many pieces. The coding style at the top level is structural.

The data path circuit was validated in the behavioral and post place and route levels. To facilitate testing, test-bench files were created. These provide inputs for the system and generate expected results to validate correct operation. The stimuli is designed to resemble what will be seen in practice.

Results

Figures 13.2 and 13.3 present the error signals from one of the validation tests performed on the proposed circuit. In figure 13.2 the error signals reported compares

the values stored in the registers of the proposed and functionally correct versions of this architecture.

Table 13.1: Values stored in data path registers. Note that the energy values store the observed change in energy across capacitor C1 for the time unit k. It was not possible to include the "Δ" symbol on the waveform tracings.

register #	value
R_1:	$E[k-1] * T_{cycle}[k]$
R_2:	E_{C1}^{max}
R_3:	$E[k]$
R_4:	$E[k-1]$
R_5:	$T_{cycle}[k]$
R_6:	$T_{cycle}[k-1]$
R_7:	V_{C1}

The register values are results from computations by the data path or operands needed for computations. As is seen for the entire test shown in figure 13.2 the register values do match. The spikes seen in figure 13.2 are due to propagation delays in the proposed architecture. This shows that the proposed architecture is functioning properly.

Figure 13.3 demonstrates the success of the proposed architecture's execution of equation 13.8. Inside the selected areas on the trace equation 13.8 is being executed. When equation 13.8 is performed the actual results matches the expected comparison value.

In figure 13.3, note the one cycle delay of the functionally correct system to respond to the comparison. This is a reflection of the fact that the output circuit will be instructed to accept the comparison results after multiplexers 3, 4 and 5 (please consult figure 13.1 for the location of these multiplexers) have been properly controlled for one clock cycle. This was done to avoid timing issues. The expected circuit response is designed to present the correct comparison value at this time.

In figure 13.3, note that the value of the wave trace labeled $E[k] * T_{cycle}[k-1]$ changes value multiple times. The data line corresponding to this wave trace is not buffered by a register in the proposed architecture. This means that results from intermediate computations executed by the array multiplier will appear on this line. However with appropriate use of control signals, the system will react to the appropriate value.

Conclusion

A custom data path for implementing a novel implementation of the perturb and observe method of maximum power point tracking has been described and successfully validated. The system is comprised of simple functional blocks. However, the compact circuit size comes with the price tag of increased operation time and logistical overhead. These trade offs were found to not hamper the viability of Stargrazer One as a maximum power point control architecture.

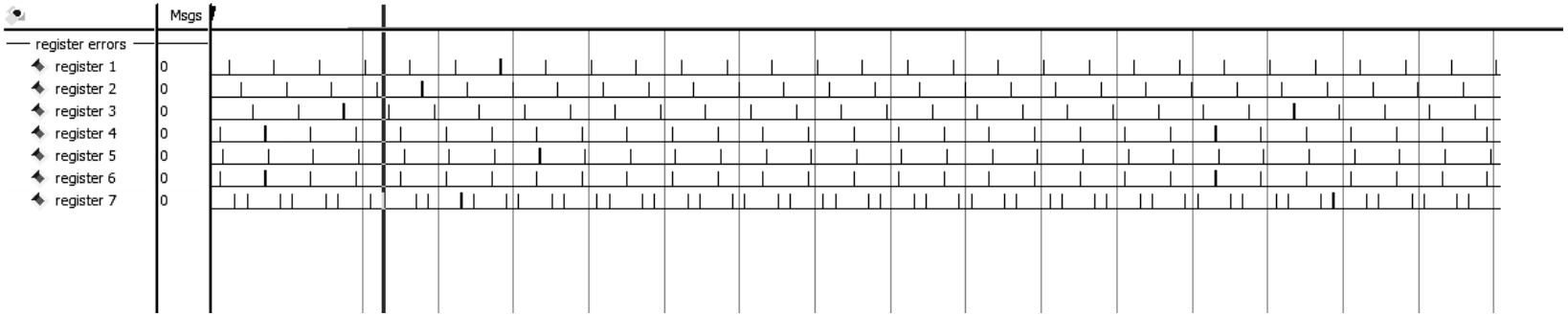

Figure 13.2: Test wide view or error signals which monitor the values stored in the data path registers. These error signals compare the values stored in both the proposed and theoretically correct architectures for each register. A value of zero indicate the values match.

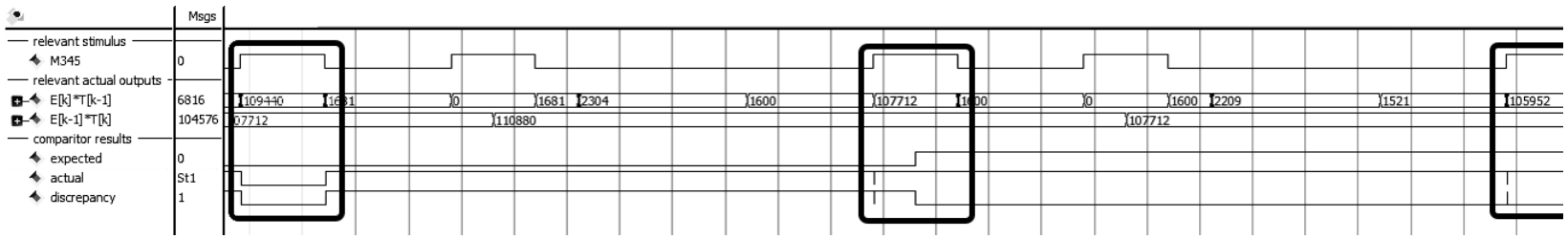

Figure 13.3: Sample view of the simulation results for the final power comparison. The signals labeled "expected" is from the theoretically correct implementation, "actual" is from the proposed architecture and "discrepancy" compares the two signals. The way the system is designed the $E[k] * T_{cycle}[k-1]$ input is sourced from a data line whose value changes as the data path works. The times where this data line represents $E[k] * T_{cycle}[k-1]$ and where computation 13.8 is done are clearly surrounded by boxes.

13.2 Control Circuit

introduction

The purpose of the control circuit is to coordinate the flow of data in Stargrazer One. This circuit interacts with each of the other functional units. The amount of interaction varies. The data path functional block is most dependent on this functional block for valid operation. This section will discuss the control algorithm, the circuit architecture and conclude with simulated validation of the proposed system.

Algorithm

Figure 13.4 presents the algorithm this circuitry is to perform. For completeness, the following signals presented in figure 13.4 are defined:

- $ADCstart$: This signal is sent by the control circuit. Its purpose is to notify one to begin an analog to digital conversion.
- $ADCdone$: This signal is received by the controls circuit. This signal notifies the circuitry that a valid digital representation for the voltage on capacitor C1 is ready.
- $t1$: This signal is received by the control circuit. This signal notifies the circuitry when the step down converter is about to enter State Two and capacitor C1 is holding the maximum voltage for the converter cycle. This voltage is reached after capacitor C1 has been charged by the solar source. Recall that capacitor C1 is briefly opened circuited as the switched capacitor step down converter operates (this occurs during State Two).
- $t2$: This signal is received by the control circuit. This signal notifies the circuitry when the step down converter is about to enter State Two and capacitor C1 is holding the minimum voltage for the converter cycle. This voltage is reached after capacitor C1 has been discharged into capacitor C2 and the load. Recall that the step down converter enters State Two twice during each converter cycle.

For each equation that the data path must execute the corresponding control states are presented in figure 13.4. The algorithm takes into account the wait from the analog to digital conversion process in the states labeled J and E in 13.4. Voltage sampling must occur at specific times. States P and G (see figure 13.4) accomplish this duty.

The control circuitry interacts with the delay circuit. The control circuit sends signals to reset and hold the initialize state of the delay circuitry. This ensures that the control circuitry is disabled for the appropriate time. The control circuit also sends signals to the output circuitry to orchestrate the communication between the output circuitry and the data path circuit.

Architecture

Table 13.2: The state encoding for the developed finite state machine.

A	=	0000000000000001
B	=	0000000000000010
C	=	0000000000000100
D	=	0000000000001000
E	=	0000000000010000
F	=	0000000000100000
G	=	0000000001000000
H	=	0000000010000000
I	=	0000000100000000
J	=	0000001000000000
K	=	0000010000000000
L	=	0000100000000000
M	=	0001000000000000
N	=	0010000000000000
O	=	0100000000000000
P	=	1000000000000000

The implementation of the control circuit is a state machine. The machine is built using the "one hot encoding"' scheme. This results in a wide state register but the tradeoff is simplified transition and output logic. Several of the outputs require no additional logic before being routed to the required control point on the data path. The finite state machine moves on the rising edge of the system clock. The state register has clock enable capability. The clock enable port receives a signal from the delay circuit. When this signal is binary one the state machine can progress through the algorithm in figure 13.4. When binary zero, the state machine remains inactive.

Section 13.1 explains that the data path simplification comes with the cost of increased control steps. It was possible to reduce the total number of states by applying the principles of parallelism found in today's programmable processors [32]. It was found that some tasks could be performed while the state machine waits for data from the analog to digital converter. Figure 13.4 show the final optimized instruction flow. There was limited leeway to move instructions due to the read after write [RAW] dependencies of several of them. Examples are the instructions which executes the computation of the current energy $E[k]$ and the equation $P = E[k] * T[k-1]$. These instructions must proceed in a sequential manner as they depend on data from the previous ones. Moving these dependent instructions out of sequence will result in incorrect operation [32]. The instructions that produce $P = E[k-1]*T[k]$ were movable. These instructions are executed while the analog and digital converter obtains the maximum voltage on capacitor C1. Further reductions in state count were possible by taking full advantage of the available hardware. As seen in figure 13.4 several actions are being accomplished during one state in numerous

cases. There were limits to how often this could occur due to structural hazards from the data path [32].

Simulation

The discussed design was implemented in Verilog and tested in the Xilinx field programmable gate array (FPGA) design environment. A behavioral level coding style was used. Testing was performed at the behavioral and post place and route levels. The state machine was tested with the use of test bench file. The file presented the proposed architecture with stimulus similar to what would be encountered in practice. Also, a functionally correct implementation written in a different coding style is subjected to the same stimuli. The results are then compared presenting a reference point for performance validation.

Results

Figures 13.5, 13.6 and 13.7 present an illustrative snapshot of the behavioral level simulations performed on the proposed control circuits. Enclosed within the solid vertical lines for each figure is a complete iteration of the algorithm in figure 13.4. All command signals are presented (figure 13.5 presents the register command signals, figure 13.6 presents the signals for the ADC controller and the multiplexers. Remaining signals are in figure 13.7). For each command signal, the results from the proposed architecture (labeled "actual" in all figures) and the functionally correct reference (labeled "expected" in all figures) are presented. These are compared by the testbench. The result signal for each pair is labeled "discrepancy" in all figures. A value of zero on these signals indicates both signals match.

Figures 13.5, 13.6 and 13.7 shows that for each command signal the proposed architecture matches the functionally correct model. The brief spikes on the discrepancy signals are due to instantaneous glitches (an artifact of the simulator).

Figure 13.8 demonstrates the response of the control circuit to the clock enabling signal from the delay circuit. As expected, the circuit operates only when this signal is binary one. When binary zero, the state machine stops at the current state.

For both functional and post place and route testing all discrepancy signals remained binary zero (With only brief spikes when the signals examined changed state due to propagation delays). Since Stargrazer One will be operated at fairly slow clocking speeds, these propagation delays should not be an issue.

Conclusion

This chapter presents and validates the proposed design of the control circuit The proposed architecture has been validated in the Xilinx FPGA design environment.

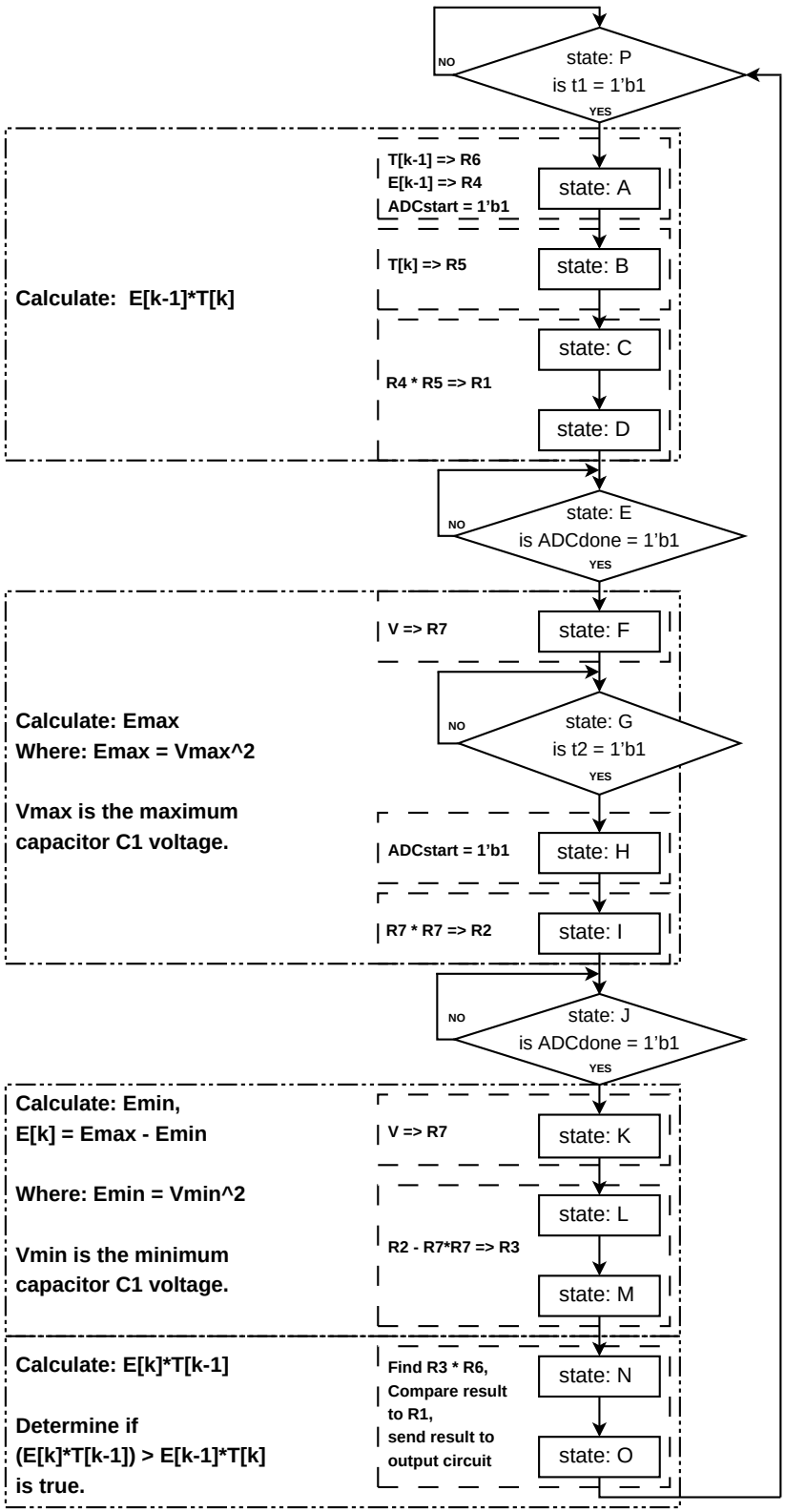

Figure 13.4: This graphic presents the state flow diagram for the finite state machine implemented for the control circuit. The expressions in the dashed boxes surrounding the states, describe what is occurring in the data path circuit at the register transfer level. The dot dash boxes describe what data path expression is being calculated. Operation begins in state "P".

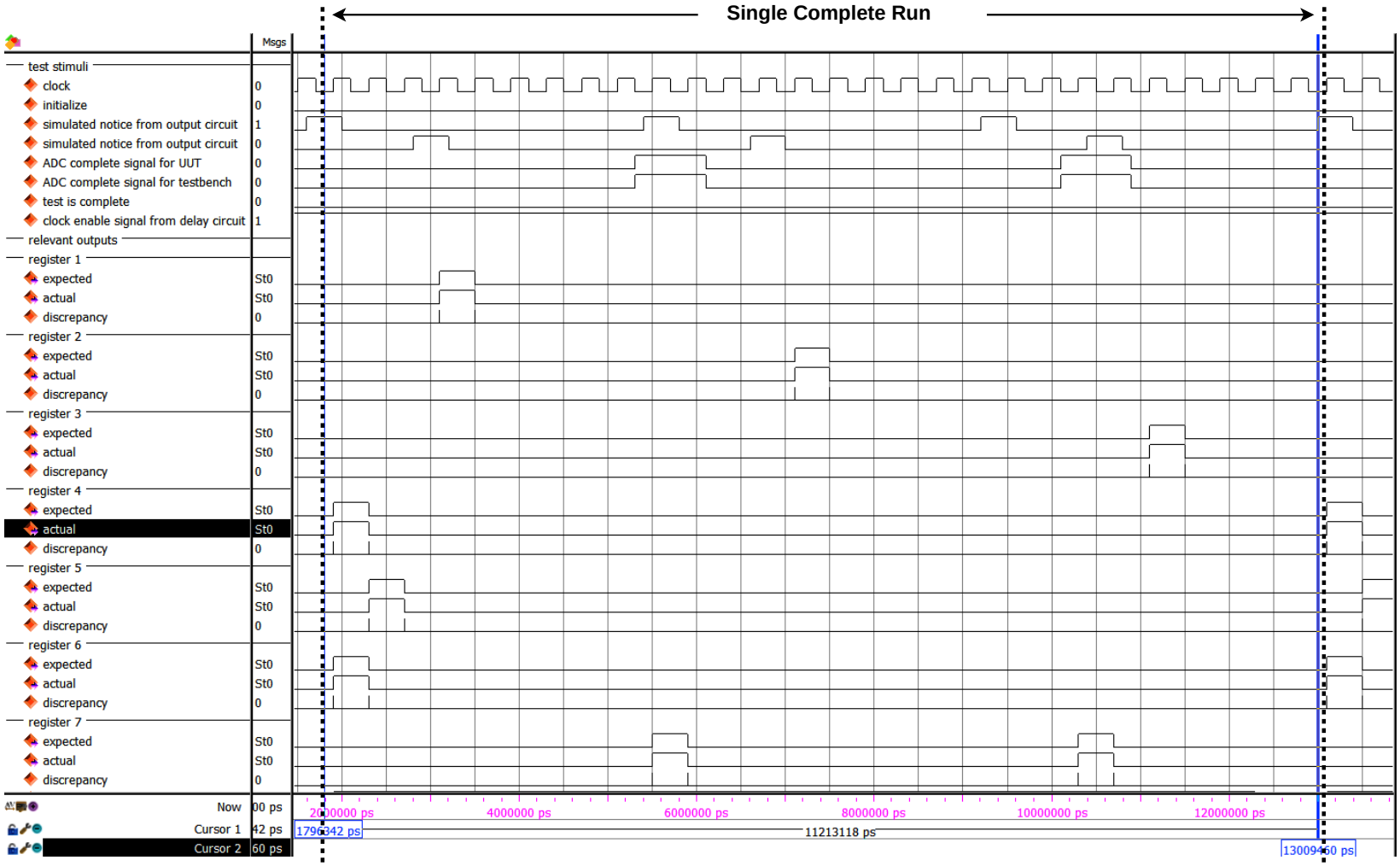

Figure 13.5: A complete run of the state machine through all states. Latching signals for the data path registers are presented. Signals labeled "expected" are from the theoretically correct implementation in the test bench, "actual" is from the proposed system and "discrepancy" is the comparison of the two.

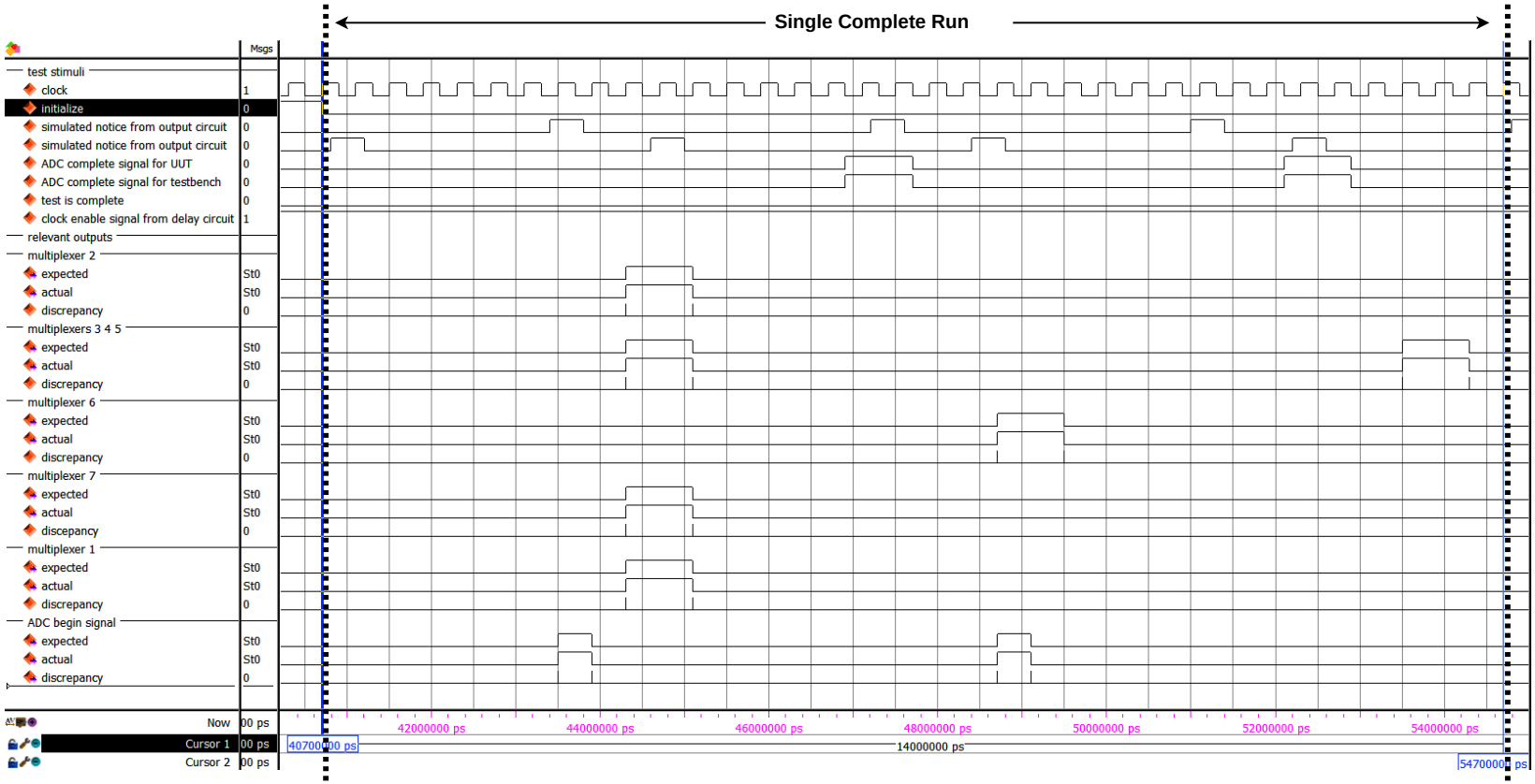

Figure 13.6: A single complete run of the state machine through all states. The run is within the two vertical cursor lines on the figure. Signals for the data path multiplexers and the signal to notify the ADC to begin work are presented. Signals labeled "expected" are from the theoretically correct implementation in the test bench, "actual" is from the proposed system and "discrepancy" is the comparison of the two.

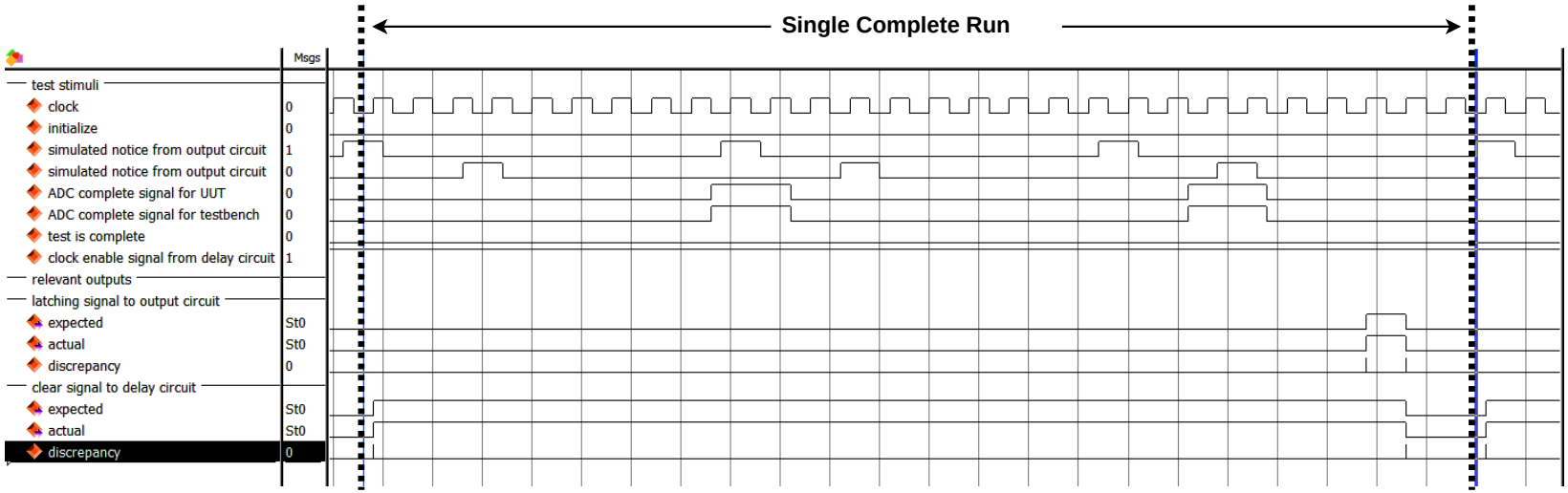

Figure 13.7: A complete run of the state machine through all states. The run is within the two vertical cursor lines on the figure. Signals that interface with the delay and output circuits are presented. Signals labeled "expected" are from the theoretically correct implementation in the test bench, "actual" is from the proposed system and "discrepancy" is the comparison of the two.

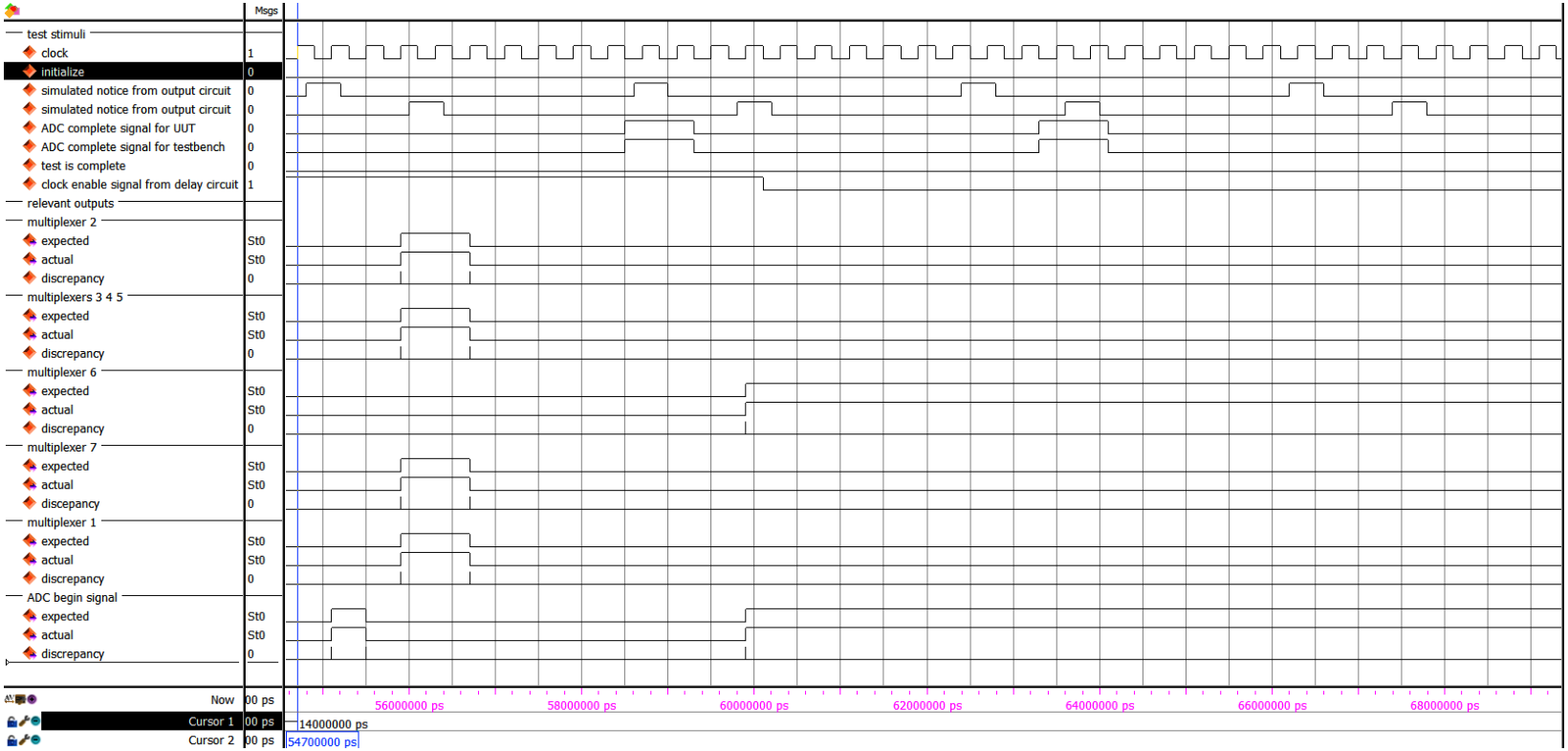

Figure 13.8: A demonstration showing the successful action of the clock enable signal. Under normal operation this signal will remain active until the state machine has completed a run of the algorithm in figure 13.4. Signals labeled "expected" are from the theoretically correct implementation in the test bench, "actual" is from the proposed system and "discrepancy" is the comparison of the two.

13.3 Output Circuit

Introduction

The output circuit takes the result of the maximum power point tracking (MPPT) algorithm and generates a repeating voltage waveform for the actuation of these transistors. The MPPT algorithms's results becomes a continually adjusting switching waveform.

A modified switching pattern based on pulse width modulation (PWM) is developed. To create the pattern, a custom digital architecture was developed. This paper will begin with a discussion of the developed switching pattern followed by a discussion of the digital architecture. This paper will conclude by validating the proposed architecture via simulation.

Switching Pattern For Stargrazer One

Figure 13.9 shows the developed switching pattern.

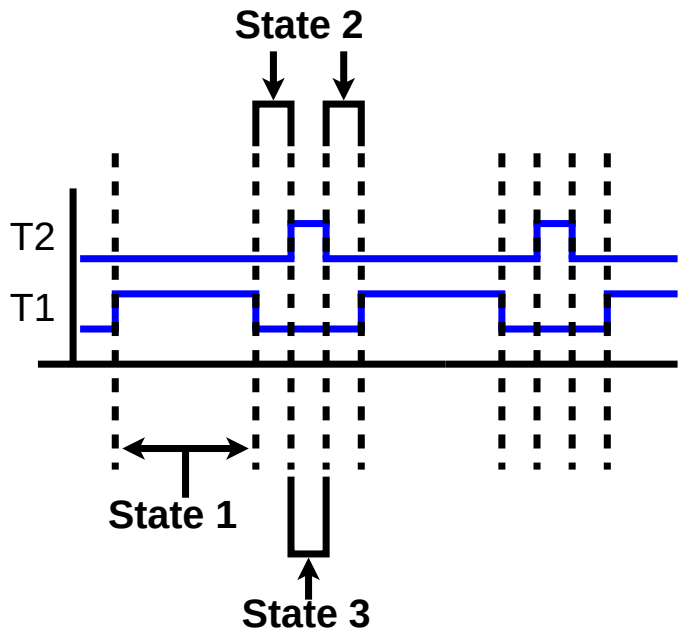

Figure 13.9: A visual showing the gate voltage patterns for each transistors in the switched capacitor converter.

What is immediately observable in figure 13.9 is that the transistors see two different waveforms. Transistor T1 connects the solar cell source to the converter. Transistor T2 connects the captured solar cell energy to the load. It was found in section 9.2 of chapter 9 that improved performance could be obtained if these switch differently. For transistor T2, an optimal fixed duty cycle length was found.

Transistor T1 has a variable duty cycle. This is a required to facilitate the power point tracking. The duty cycle adjustments on T1 are essential to create the varying impedance seen by the solar cell.

Figure 13.9 shows that both transistors are off simultaneously for two time periods. This is to take advantage of a property of this switched capacitor circuit. As discussed in chapter 8 when both transistors are off, capacitor C1 is open circuited. This was found to be an excellent time to obtain required voltage readings. These periods are a sufficient length to permit sampling of capacitor C1's voltage.

The duration of an entire switching cycle is not fixed. Longer on-time of transistor T1 will result in an increased total cycle length. Conversely, a shorter T1 on-time will reduce the total length.

Output Circuit Architecture

Figure 13.11 presents the overview of the architecture (to ensure image clarity, figure 13.11 is on its own page at the end of this section). The actual signals used for the power electronic circuit transistors are generated by the finite state machine (see figure 13.11). The purpose of the additional circuitry is to assist the state machine in creating the appropriate output waveforms. Besides creating the transistor gate signals, the output circuitry is also charged with additional important tasks. They are as follows:

- Send timing signals to the control circuitry to insure correct sampling of the capacitor C1 voltage.
- Provide the current length of a converter cycle to the data path circuitry

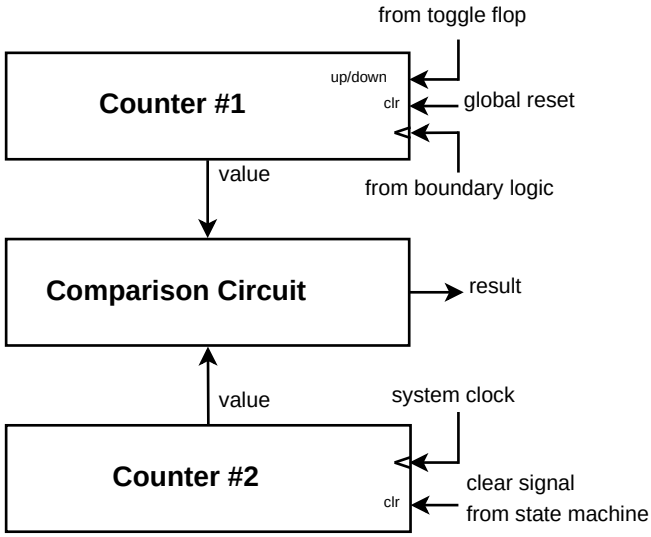

Figure 13.10: Functional block view of the digital architecture which helps dictate how long transistor T1 is on.

Figure 13.10 shows a high level schematic view of the circuits which assist the state machine. The purpose of this circuitry is to insure the proper execution of the duty cycle adjustment for transistor one. Appendix 15.3 discuss the functional blocks in figure 13.10 in greater detail.

It is important to note that the finite state machine design used in this thesis is not portable. The state machine design presented may not be valid for other switch capacitor converters. It is plausible that this example state machine could be adapted for other power electronic converters. This is a valid topic for future research. Figure 21 presents the state flow diagram for the example state machine.

Simulation

To demonstrate the functionality of the proposed architecture a Verilog description was created. This system is composed of multiple functional blocks, each one individually designed and tested. Therefore the top level description uses a structural coding style.

The proposed architecture was tested at the behavioral and post place and route levels. To conduct the testing, test benches were developed. These subjected the system to a controlled set of inputs and provided sets of expected results to facilitate comparison.

Results With Conclusions

Figure 13.12 shows an illustrative segment of a post place and route validation run. The output of counter one (see figure 13.10) is chosen for testing. Figure 13.12 only presents this output. The image shows the proposed output circuit successfully responding to the command to change direction. The The direction change occurs when a value of binary one on the signal labeled "comparison result" is seen on the rising edge of the "counter one update" signal (please see figure 13.12). As expected, when the "comparison result" line is zero the output circuit continues to adjust the time transistor TA stays on the current direction. The signal labeled "discrepancy" is binary one only when the theoretically correct output (label beginning with "expected") and the proposed architecture output (label beginning with "actual") are dissimilar. This signal remains at binary zero confirming that the proposed output circuit architecture is performing as expected. The small spikes observed on the discrepancy signal were determined to be due to propagation delays.

Figure 13.13 provides further support by presenting the "discrepancy" signal for an entire simulation run (labeled "error" in the figure). The fact that it remains binary zero (with the exception of brief spikes due to delays) suggests correct operation. Provided the Stargrazer system operates with a sufficiently slow clock, the propogation delays will present no problems.

Figure 13.14 presents an example of how the proposed architecture performs when the output circuit reaches the minimum or maximum possible on time for the transistor T1 gate signal. This situation may be encountered in actual operation so it must be handled. The proposed architecture is designed to remain at either zero

or the maximum possible duty value until instructed to change direction from the "comparison result" signal when this occurs. In the case presented in figure 13.14, the output circuit architecture is allowed to continue to increase transistor T1 on time until it reaches the maximum possible size (which corresponds to a count value of 255). Notice that the architecture remains at this value. This corresponds to the expected behavior.

In all examined test cases, the proposed architecture performed as expected. This architecture was subjected to additional testing at both the behavioral and post place and route levels. It was also found to operate as expected. The section has presented and shown evidence supporting the validity of an architecture that successfully translates the results of the power point tracking algorithm executed by Stargrazer One into a switching pattern for the transistors in the step down switched capacitor converter.

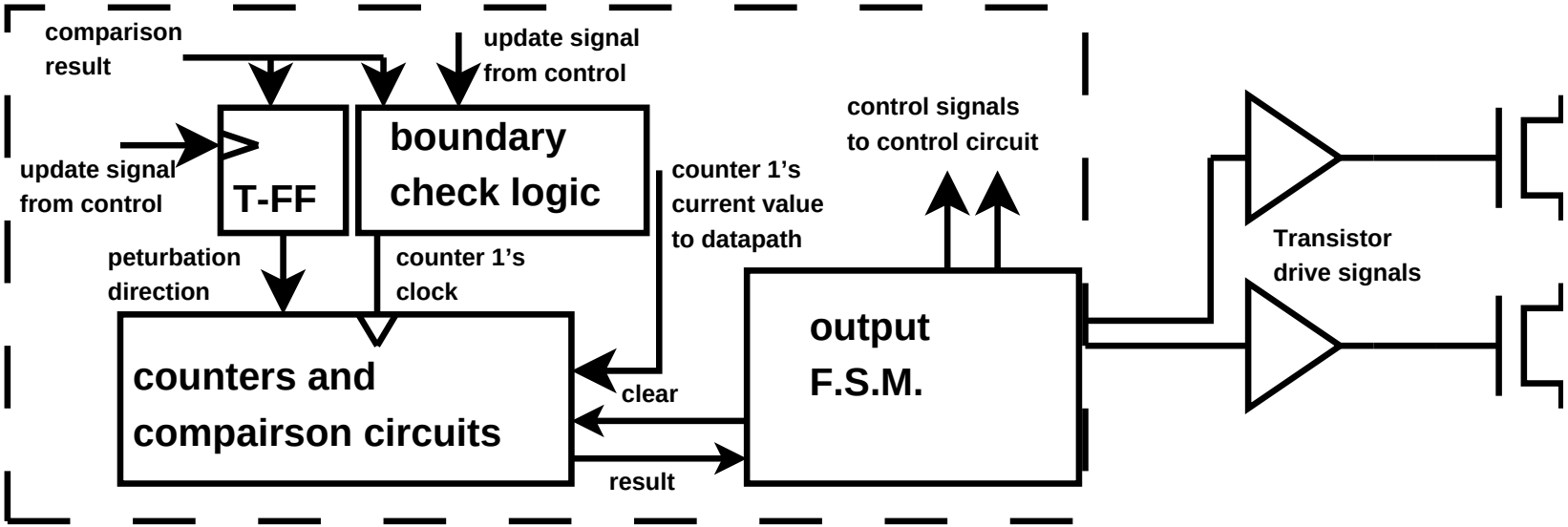

Figure 13.11: Top level schematic for the output circuit. The system clock [not shown] goes into the output finite state machine and counter two.

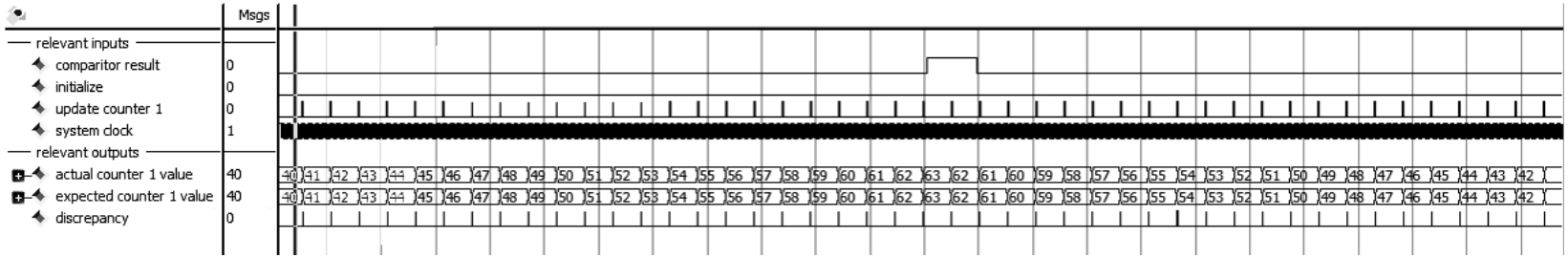

Figure 13.12: An illustrative trace for the output circuit system. The output of counter one is selected as the test node. The value of the counter containing the on time for transistor T1 is the test output being compared. Note the direction change at the center of the trace. The circuit performs as expected.

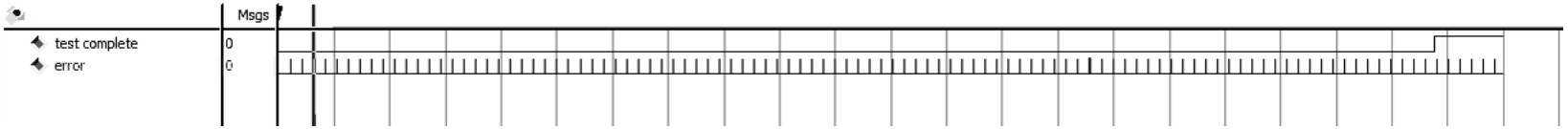

Figure 13.13: An entire test run. The signal labeled "error" compares the value or the counter with contains the transistor T1 on time for the theoretically correct and proposed implementations. The test complete signal turns binary one when the simulation is concluded. The spikes observed in "error" are due to propagation delays. A value of binary zero for "error" indicates that the implementations match.

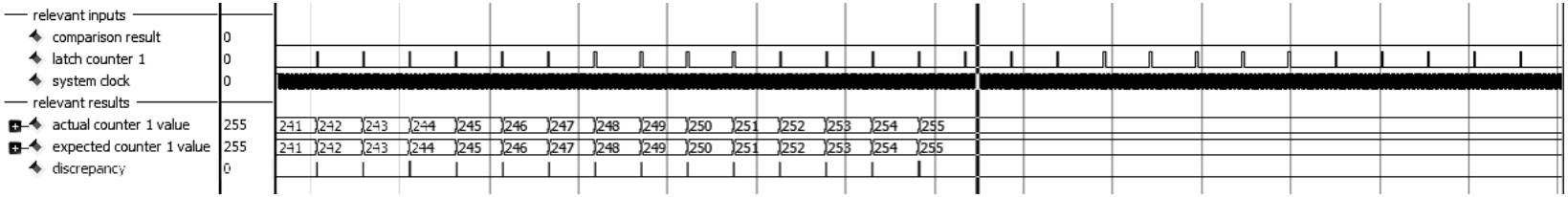

Figure 13.14: An illustrative tracing validating correct response to an end value condition. The system is directed to continue increasing and remains at the maximum value as expected.

13.4 Delay Circuit

Introduction

As determined in chapter 10, Stargrazer One should be instructed to wait a certain amount of converter cycles before executing another round of power computation. This section will present the digital architecture used to execute this required delay. The proposed architecture will be presented and discussed. Then testing results using the Xilinx field programmable gate array (FPGA) design environment will be presented. Behavioral and post place and route simulations were performed on the proposed architecture.

Proposed Architecture

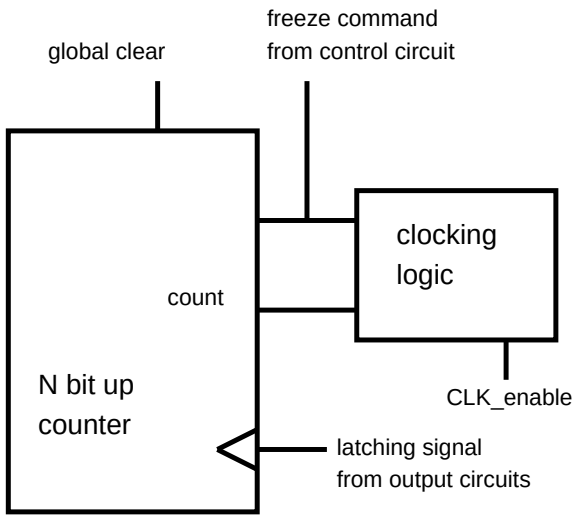

Figure 13.15: Second level schematic of developed system.

Figure 13.15 show a top level view of the proposed architecture. In order for this proposed system to do its job, it must be able to shut down the control circuit for a designated amount of time. The architecture accomplishes this task by disabling the clock entering the control circuit. Without a clock, the control circuit cannot advance. This circuit has logic to determine when to enable the clock and shut it off.

Implementing the delay between calculations is accomplished with a counter (as shown in figure 13.15). The counter clocked using a signal from the output circuitry. This signal will deliver a rising edge once every converter cycle. The counter is designed to reset to all zeros when presented with a global reset signal or a command from the control circuit.

Figure 13.16 presents the architecture used to determine when to send in the clock enable signal to the control circuitry in more detail. The appropriate task can be accomplished with a few logical gates . The gates pass a binary one when a desired count value is reached and maintain binary one while the control circuit is performing its duties . The equation selected that performs these tasks is below:

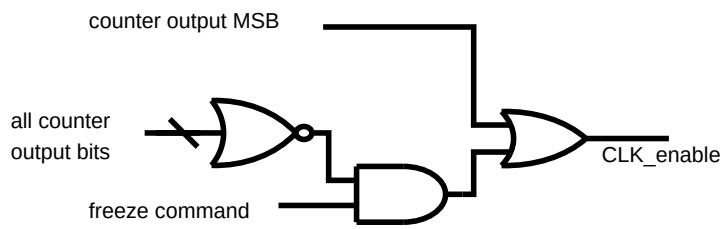

Figure 13.16: Example gate level schematic of the logic used to enable and disable the clock.

$$CLK\_enable = (c[4]) + (freeze * -c[4] * -c[3] * -c[2] * -c[1] * -c[0]) \qquad (13.9)$$

Where $c[1], c[2], c[3], c[4], c[0]$ are the counter bits. $c[0]$ is the least significant bit and $c[4]$ is the most significant bit. $freeze$ is the holding signal sent by the control circuit. Multiplication denotes logical AND and addition logical OR.

The expression in the first parenthesis in equation 13.9 tells when to enable the control clock. The expression in the second parenthesis of equation 13.9 insures that the control clock remains enabled until the control circuit has completed its duties.

As indicated, equation 13.9 is an example of how the clock enabling function is accomplished. This particular expression will not be valid for all switched capacitor converter types. However, it may be possible to produce a valid delay circuitry by resizing the counter size and/or adjusting the logic equation to check for another value. This can be explored in future research.

Simulation

To examine this architecture, a Verilog description was prepared. Then the proposed architecture was simulated in the Xilinx FPGA computer aided design environment at both behavioral and post place and route levels. To evaluate the performance a test bench containing a theoretically correct implementation of the delay circuit was developed and presented with the same inputs seen by the proposed architecture. The generated inputs mimic actual operation.

Results With Conclusions

Figure 13.17 presents an example of the validation simulations performed on the proposed delay architecture. As expected, the generated clock enable signal remains binary zero until a desired counter value is reached (see figure 13.17). Once this value is reached the clock enable signal should remain binary one for as long as equation 13.9 remains true. As figure 13.17 shows this is indeed what occurs.

Figure 13.18 presents a closer view of when the delay system enables the clock. Observe that when the counter becomes binary sixteen the clock enable signal becomes binary one (see figure 13.18). This is in accord with the first term of equation

13.9. Figure 13.18 shows the counter remaining zero and the clock enable signal remaining binary one for the duration of time that the simulated freeze signal remains binary one (see figure 13.18). This is in accord to the second term of equation 13.9. Once the freeze signal becomes binary zero, the counter resumes incrementation.

This article presents the successful operation of an proposed implementation for the simple solution to the operating point transition delay problem posed by the choice of power converter for Stargrazer One as outlined in chapter 10.

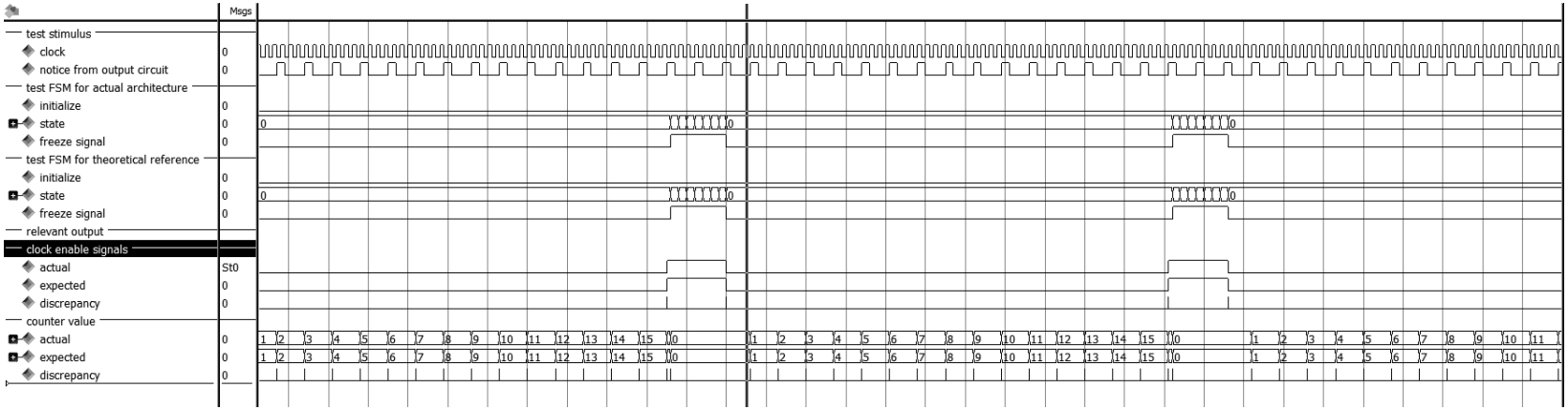

Figure 13.17: Representative simulation trace at the post place and route level. Several iterations of the delay circuit's operation are presented. For each output, signals labeled "expected" come from the theoretically correct implementation in the test bench, "actual" is from the proposed architecture and "discrepancy" compares the two signals. A result of zero on "discrepancy" indicates a match.

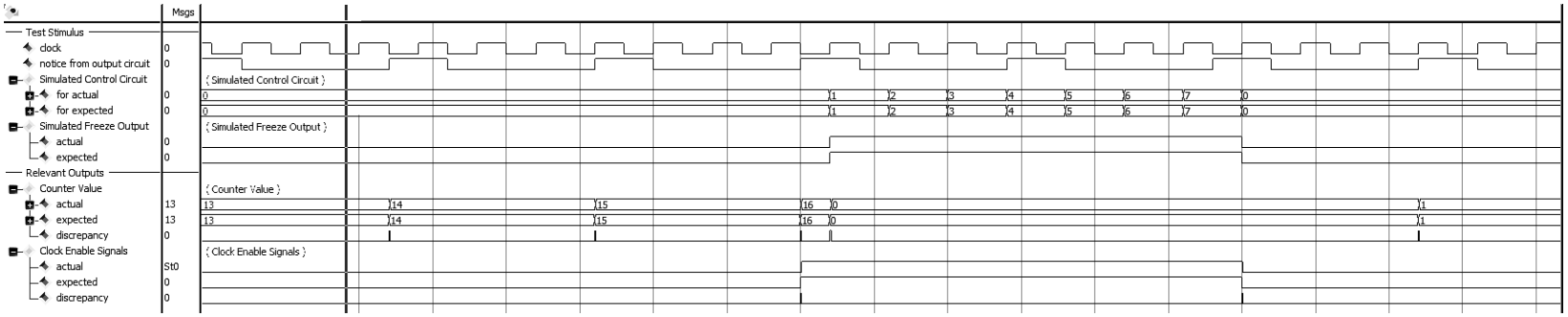

Figure 13.18: A closer view showing a successful execution of equation 13.9. For each output, signals labeled "expected" come from the theoretically correct implementation in the test bench, "actual" is from the proposed architecture and "discrepancy" compares the two signals. A result of zero on "discrepancy" indicates a match.

Part IV

Stargrazer One System-Wide Experimental Validation

Chapter 14 Introduction and Chapter Contents

Introduction

In part II, a novel switched capacitor step down converter was defined. Continuous time models were developed and performance optimizations were proposed. Part III presented the special purpose digital architecture to execute a novel implementation of the perturb and observe maximum power point tracking algorithm. This design was captured via the Verilog hardware description language and tested in the digital domain using the Xilinx ISE computer aided design environment. In both of these parts, arguments as to the viability and correct operation of the various featured components were presented. However, these pieces were tested in isolation. A simulated representation in continuous time of the maximum power point tracker was used to test the step down converter. The digital architecture was presented with a binary representation of voltage values that could be seen from the step down converter. These tests while insightful were limited.

The purpose of this chapter is to test the entire Stargrazer One system together. The intent is to have the proposed digital architecture interact with the developed switched capacitor step down converter. The tests use a physical prototype of the Stargrazer One system. Besides facilitating a system-wide validation, a physical prototype will permit an exploration of practical issues a designer may encounter should they choose to implement the Stargrazer One system. In the development of the physical prototype, such issues were encountered. These required some fine tuning and development of additional hardware. The additional hardware came in the form of interface circuitry so that Stargrazer One could successfully execute its duties. The Stargrazer One architecture as proposed in part III did not require any revisions. Information concerning details of the interfacing circuits is referred to in the appendices. These are referenced where appropriate.

The contents of this part are as follows:

- Chapter 15
  - Section 15.1: The physical prototype of Stargrazer One is developed. The prototype is validated via experimentation.
  - Section 15.2: The design goals of Stargrazer One are revisited and the final architecture is checked against them.
  - Section 15.3: This section presents next steps worthy of future research effort.

Chapter 15 System-Wide Validation

15.1 Experimental Validation

Introduction

In this section, a physical implementation of the Stargrazer One maximum power point tracker is developed and tested. The purpose is to validate the design's ability to operate in a physcial instance. This also permits testing of the system under more realistic stimuli then what was possible in the previous chapters.

The discussion in this section will begin by first describing and presenting the physical testbed. Then the discussion will proceed to the experiments. The experiments executed were as follows:

- Experiment 1: Validation of Stargrazer One performance under steady state conditions
- Experiment 2: Validation of Stargrazer One performance under simulated environmental changes

Each experiment will be discussed in its own section

Experimental Setup

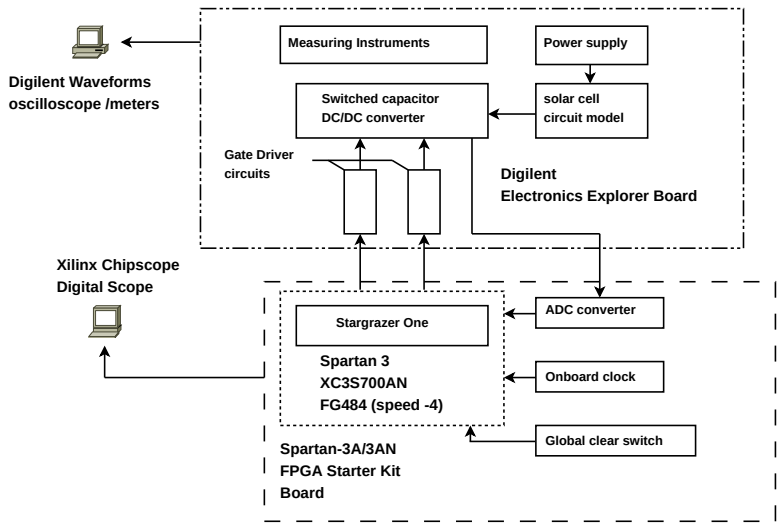

Figure 15.1: Block diagram presenting the experimental setup used in this section. Relevant hardware is labeled and routing presented.

Referring to figure 15.1, The proposed Stargrazer One architecture developed in part III is implemented inside the Spartan 3AN prototyping board. The interactions with the other blocks are through the transistor drive signals and the voltage on

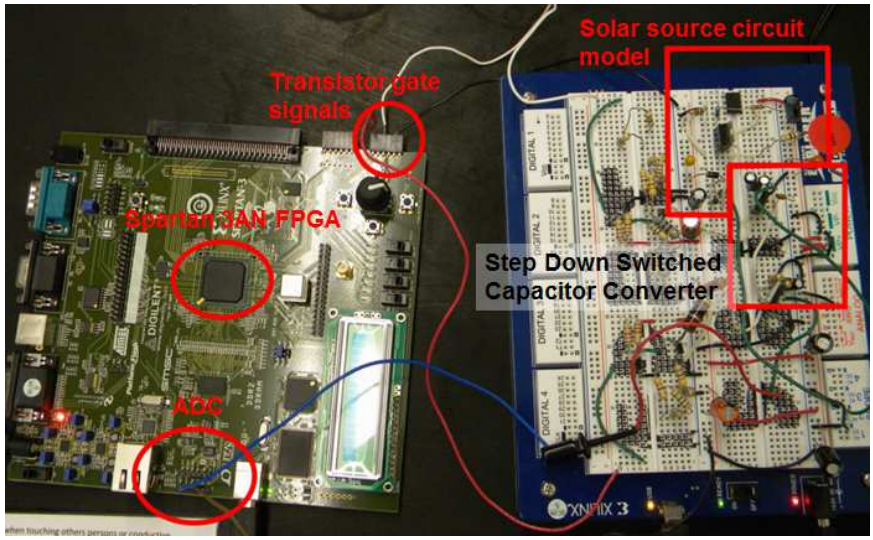

Figure 15.2: Photograph presenting the hardware used for this section. Relevant components are labeled.

Table 15.1: Switched capacitor step down converter device values used for the physical experiment. Note that the values for C1, C2, and R_{load} are composite were created from parallel combinations of capacitors and resistors.

DC to DC converter part list		
T1	NXP PSMN2R0-30PL N channel MOSFET	
T2	NXP PSMN2R0-30PL N channel MOSFET	
C1	5.7	μF
C2	20	μF
R_{load}	5.5	Ω
C_{filter}	2	nF

capacitor C1. The Spartan 3AN prototyping board has its own analog to digital converter. This was used to capture the voltage on capacitor C1 and convert this information into a usable form. In order to take advantage of this feature, special interfacing hardware needed to be defined in the FPGA. The architecture is described in detail in appendix 15.3. The gate drive signals for transistors T1 and T2 are issued from two pins on one of the Spartan 3AN board's accessory headers. The clock for Stargrazer One is provided from an internal oscillator in the Spartan 3AN prototyping board. The clock has a frequency of 50 MHz, too fast for Stargrazer One. A digital clock divider needed to be defined and is discussed in appendix 15.3. To initialize Stargrazer One, it was decided to use one of the switches available on the development board. The switches do not have de-bouncing circuits. To avoid false resets, an appropriate circuit is defined. This circuit is described in appendix 15.3.

In figure 15.1, the analog elements are also included. Table 15.1 defines the components used in the step down switched capacitor converter implemented in this experiment. In developing this system, there was a need to include additional analog

circuitry to effectively drive the gates of the power transistors in the converter. For additional information on these gate driver circuits, please refer to appendix 15.3. To simulate a solar cell power source, a circuit model was developed and characterized. For more details on the implementation of the circuit model and/or its characterization, the reader is encouraged to consult appendix 15.3. Figure 15.1 shows that the analog components have been developed on a Digilent Electronic Explorer Board. This is a prototyping and testing module featuring a solder-less circuit board and several power supply and measurement features. The on board power supply was used exclusively to power the analog circuit components. The measurement features include an on board oscilloscope and on board volt meters. Both capabilities were used to obtain information both in this section and the various appendices following it.

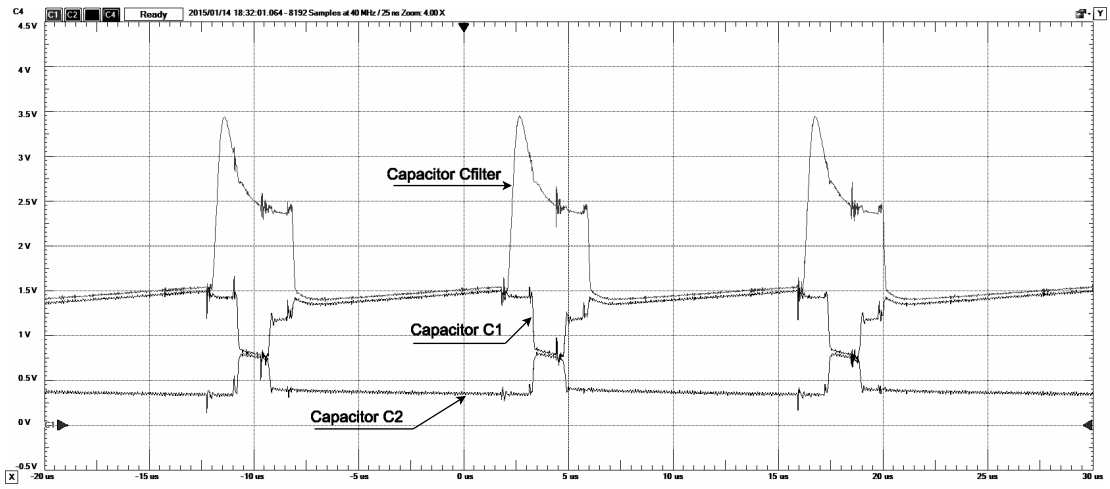

Figure 15.3: Oscilloscope capture showing the observed signals for the voltages on capacitor C1, C2 and Cfilter. The appropriate signal is labeled in the figure. Operating states of the converter is also labeled.

The implementation of the switched capacitor step down power electronic converter on the Explorer Board manifested some unexpected behavior. This is visually shown in figure 15.3. The observed behavior is in stark contradiction to the computed waveforms in part II which defined the converter. Investigation revealed that parasitic affects are responsible for the observed behavior. The observed ringing in the waveforms indicates that parasitic inductance is manifesting itself. The most striking deviation from expected behavior is in the transition from operating State Three to State Two. Investigation strongly suggests that the cause is from parasitic inductance. Scope observations support this conclusion (such as the one in figure 15.3). Additionally, the capacitors used to create capacitor C1 and capacitor C2 are electrolytic units. The switches are working at frequencies up to the hundreds of kilohertz. As frequency increases, electrolytic capacitors begin to adopt resistive and inductive characteristics from the parasitic elements in the devices. The frequencies that the step down converter operates are sufficient for electrolytic capacitors to exhibit inductive behavior. The fact that operating the switches at lower frequen-

cies significantly reduced the observed non-ideal behavior validates this reasoning. The non-ideal characteristics of the solder-less circuit board and the wiring no doubt added to the observed non-ideal behavior.

It was decided that the most convenient solution was to do nothing. This behavior does not prohibit a valid validation of the proposed Stargrazer One system. As discussed in the previous paragraph, reducing frequency did reduce the observed non-ideal behavior. An instance of Stargrazer One could simply be operated at a slower clock to reduce this effect. Additionally, use of capacitors more tolerant of high frequencies and an implementation more optimized for high frequency testing can also assist in producing behavior which better resembles the ideal characteristics modeled in part II.

Figure 15.1 also includes a personal computer. Measurements information from the on board instruments in the Explorer Board appear on the computer. Also, the power supply is controlled from the computer. In addition, the digital scope feature of the Xilinx ISE design tools (called Chip Scope) is used to capture information from the hardware implementation inside the Spartan 3AN prototyping board. The information is sent to the computer where it is presented in a visual form.

For completeness, figure 15.4 presents a photograph of the hardware implementation.

Experiment One

Introduction

The purpose of this experiment is to validate the ability for Stargrazer One to detect and remain at the maximum power point under steady state conditions. This would be consistent with a situation where the system is operating in a sunny day.

An important element of this experiment is to determine what State One values correspond to maximum power operation. As the solar system is modeled by a circuit, it was possible to design a circuit which simulates a fixed number of illumination changes. For details, please consult appendix 15.3. For each designed illumination value, the State One values corresponding to maximum power operation were determined. The developed procedure, experiments and results can be viewed in finer detail in appendix 15.3. Table 15.2 below presents the results for each simulated illumination value of the circuit.

Table 15.2: State One values corresponding to maximum power operation for each simulated illumination value from the source circuit. The integer values presented correspond to multiples of the Stargrazer One system clock. Short circuit current I_{short} is reported in milliamperes and $t_{State\ One}$ is in number of clock cycles.

Best State One Values	
I_{short}	$t_{State\ One}$
108	5
70	10
34	30

The procedure used in this experiment and the results are in the sections that follow.

Procedure

The procedure to be used will be defined as follows:

- Prepare the correct solar source setting by adjusting the short circuit current.
- Configure the digital scope to log samples of data from the Stargrazer One architecture in the Spartan 3AN board. The probe of the digital scope will be applied to the databus which holds the result of counter one in the output circuit. Please refer to the appriopiate section in part III for the location of this bus within the output circuitry.
- Reset the Stargrazer One Prototype.
- Permit the system to operate for a minimum of 1 minute. This allows ample time for settling.
- Record the observed range of State One values seen on the digital scope.
- Repeat previous three steps to ensure robust data. (These steps were repeated five times when this experiment was conducted. Number of times need not be five.).
- Repeat entire procedure for remaining simulated radiation values from the solar cell circuit model

Results

Table 15.3: Results for the case of $I_{short} = 108$ mA. The State One value corresponding to maximum power operation is presented in table 15.2. The observed range of values that the Stargrazer One prototype assumes is reported for each experimental run. Results are reported as multiples of the Stargrazer One system clock.

Experimental Results
Maximum Power when $I_{short} = 108$ mA

run:	Range of State One Durations
1	{4, 5, 6, 7}
2	{4, 5, 6, 7}
3	{4, 5, 6, 7}
4	{4, 5, 6, 7}
5	{4, 5, 6, 7}

The developed solar cell circuit model is designed to simulate three different illumination levels. The reader can consult appendix 15.3 for details on the implementation. Tables 15.3, 15.4 and 15.5 presents the results for each of the three different

Table 15.4: Results for the case of $I_{short} = 70$ mA. The State One value corresponding to maximum power operation is presented in table 15.2. The observed range of values that the Stargrazer One prototyped assumes is reported for each experimental run. Results are reported as multiples of the Stargrazer One system clock.

Experimental Results Maximum Power when $I_{short} = 70$ mA	
run:	Range of State One Durations
1	{8, 9, 10, 11}
2	{9, 10, 11}
3	{9, 10, 11}
4	{9, 10, 11}
5	{9, 10, 11}

Table 15.5: Results for the case of $I_{short} = 34$ mA. The State One value corresponding to maximum power operation is presented in table 15.2. The observed range of values that the Stargrazer One prototyped assumes is reported for each experimental run. Results are reported as multiples of the Stargrazer One system clock.

Experimental Results Maximum Power when $I_{short} = 34$ mA	
run:	Range of State One Durations
1	{34, 35, 36, 37}
2	{23, 24, 25, 26}
3	{24, 25, 26, 27}
4	{33, 34, 35, 36, 37}
5	{33, 34, 35}

illumination levels. The tables present the range of values that the Stargrazer One prototype assumes in steady state operation. Table 15.2 lists the State One value that corresponds to maximum power point operation for each simulated illumination.

Conclusions

The experimental results are very encouraging. For the simulated radiation levels reported in tables 15.3 and table 15.4, the observed range of State One values that Stargrazer One operated in included the State One value corresponding to maximum power operation. This indicates that, in these two cases, Stargrazer One is successfully seeking and remaining at the maximum power point. The fact that this result is consistent across the five experiments further reinforces these conclusions.

For the experiment performed at the solar radiation level reported in table 15.5, the proposed architecture seemed to settle within two ranges of values. Both value ranges are near to the determined State One value corresponding to maximum power operation. To rule out the possibility of error, this experiment was re-executed. The same ranges were obtained and are the values seen in the table 15.5. The

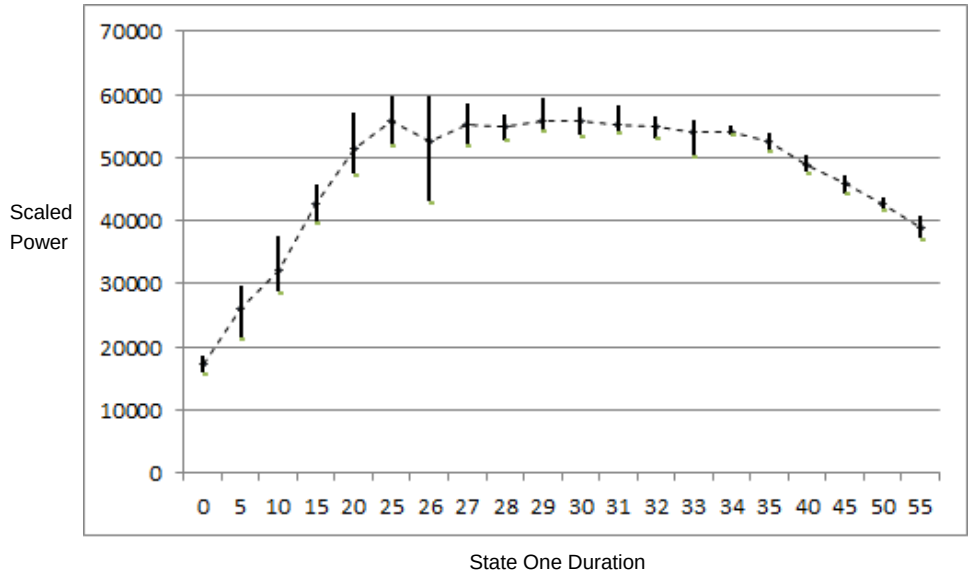

Figure 15.4: Power vs. State One value for $I_{short} = 34$ mA. The horizontal axis is the length of State One (reported in multiples of the Stargrazer One system clock) and the vertical axis is the scaled power value. Power was determined using $P = \frac{\Delta Energy}{\Delta Time}$. This tracing is repeated from appendix 15.3. The dashed line passes through the average of the collected data values for each State One value. The vertical bars on each data point correspond to the variation observed in the data collection. For details on how this data was obtained, please refer to appendix 15.3.

results are not unexpected. Figure 15.4 presents the observed power vs. State One characteristic for $I_{short} = 34$ mA. The characteristic between State One equal to 25 and 35 system clock cycles is notably flat. Furthermore, the presence of vertical bars at every point (some quite large such as the one at when State One is 26 clock cycles) indicates a large variance of values that the power can assume for State One. Given this uncertainty, the prototype settling at different ranges of State One values is unsurprising. The ranges of values that the hardware prototype settles do fall within the observed plateau in figure 15.4. Given the variations observed in figure 15.4 (pursuant to the vertical bars) it is plausible that the system has indeed found the maximum power for that particular experimental instance. The vertical bars seen in figure 15.4 indicate significant noise. This is further reflected in the wide ranges of State One values that Stargrazer One settles to in table 15.5 and table 15.3. Given the demonstrated performance in the cases presented in tables 15.3 and 15.4 along with the consistency noted in the ranges assumed for the case of $I_{short} = 34$ mA, it is valid to conclude that system noise is playing a significant role in causing the observed behavior in this case.

Experiment Two

The purpose of this experiment is to demonstrate that the proposed Stargrazer One power point tracking system properly responds when presented with changes to the

solar source output. This occurs regularly in practice as solar photo-voltaic sources are sensitive to temperature and light intensity. If operating correctly, the power point tracking system should seek the new maximum power point. Once there, the tracking system hold operation around this new maximum power point until the next environmental change.

To assess whether or not Stargrazer One responds appropriately, environmental changes will be emulated on the physical prototyping developed. The design of the current source lends itself well to simulate changes in light. It is known that changes in the observed short circuit current is proportional to the light intensity striking the solar source. Therefore, illumination changes will be simulated by changing the current produced by the source. Details on the construction of the solar source model are available in appendix 15.3. In this experiment, Stargrazer One was subjected to two separate test vectors. These vectors are presented in figure's 15.5 and 15.6.

The experimental setup is the same as the previous experiments in this section. All measurements will be done using the Xilinx Chip Scope digital scope.

The procedure used, the results and conclusions are the following sections.

Procedure

The procedure used is presented is the following list:

- Set current source to starting value for the chosen test vector. This was accomplished by adjusting a resistance in the current source circuit developed. Please consult appendix 15.3 for specifics.
- Initialize the Stargrazer One system
- Start the digital scope. If possible, set for repeated sampling with export of the data.
- After six samples from the scope, adjust the current source to the second value in the test vector.
- After six samples from the scope, adjust the current source to the final value in the test vector.
- After six samples, stop data collection.

optional Repeat above procedure multiple times to obtain more robust results.

- Repeat this procedure with the second test vector.

Results With Conclusions

Tables 15.6 and 15.7 presents the results of the experiment. The solar cell source circuit used in this experiment has a differing current voltage relationship than the one used in the previous experiment. The current voltage relationship was not characterized for the source as the purpose of this experiment is to demonstrate that

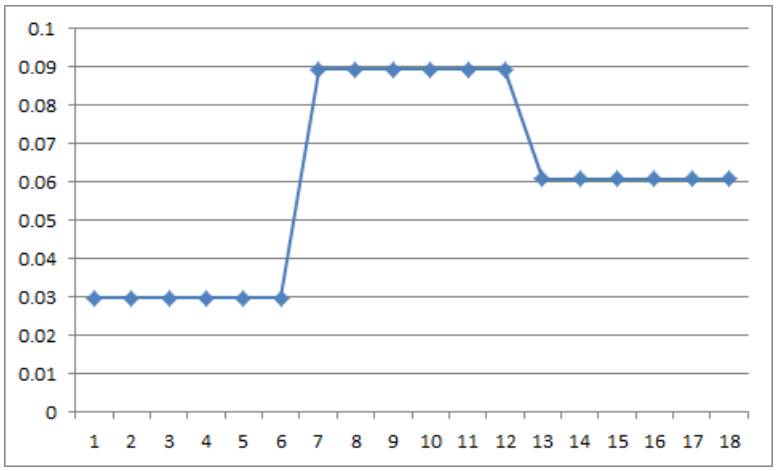

Figure 15.5: Waveform showing an example of the first test vector presented to Stargrazer One. The X axis is the number of data acquisitions done by the digital scope and the Y axis is the resistance used to produce the short circuit current value. For details on how this resistance is translated into a current please consult appendix 15.3. This appendix discuss is the architecture used to model the solar power source.

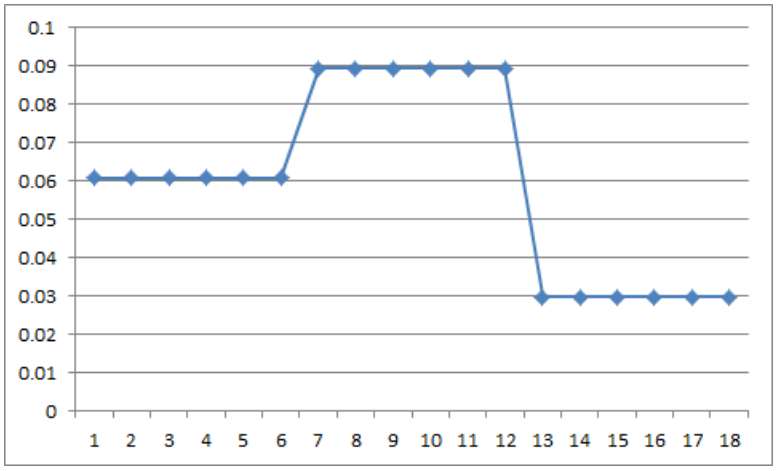

Figure 15.6: Waveform showing an example of the second test vector presented to Stargrazer One. The X axis is the number of data acquisitions done by the digital scope and the Y axis is the resistance used to produce the short circuit current value. For details on how this resistance is translated into a current please consult appendix 15.3. This appendix discuss is the architecture used to model the solar power source.

Stargrazer One properly responds when the environment changes. Stargrazer One has already demonstrated that it assumes steady state at the maximum power point in the previous experiment.

Both figures show the Stargrazer One power point tracking system either actively seeking or remaining at a range of State One values. This is consistent with expected behavior. When presented with changing environmental conditions, a maximum power point tracker should adjust the operating conditions until a new maximum

Table 15.6: Observed range of values assumed by the Stargrazer One hardware prototype for each data acquisition by the digital scope. Stargrazer One is responding to the test vector presented in figure 15.5. For the columns that list only two numbers with the word "through" between them: the digital scope was able to capture a portion of Stargrazer One's transition to the new maximum power point. To keep the table at a manageable number of columns, only the absolute lowest and highest State One values are presented for these data captures. All State One values are reported as multiples of the Stargrazer One system clock period.

Data Capture Number	Observed Range of State One Values
1	{60, ... 43}
2	{48, 47, 46, 45, 44, 43}
3	{48, 47, 46, 45, 44, 43}
4	{45, 44, 43, 42}
5	{45, 44, 43, 42}
6	{45, 44, 43, 42}
7	{45, 44, 43, 42}
8	{44, 43, 42, 41}
9	{15, ... 3}
10	{6, 5, 4, 3}
11	{9, 8, 7, 6}
12	{11, 10, 9}
13	{12, 11, 10, 9, 8, 7}
14	{12, 11, 10, 9, 8, 7}
15	{12, 11, 10, 9, 8, 7}
16	{12, 11, 10, 9, 8, 7}
17	{12, 11, 10, 9, 8, 7}
18	{12, 11, 10, 9, 8, 7}
19	{22, ... 7}
20	{20, 19, 18, 17}
21	{18, 17, 16, 15, 14}
22	{18, 17, 16, 15, 14}
23	{18, 17, 16, 15, 14}
24	{18, 17, 16, 15, 14}
25	{18, 17, 16, 15, 14}
26	{18, 17, 16, 15, 14}
27	{19, 18, 17, 16, 15}
28	{19, 18, 17}

power point has been found.

Due to the limitations of the digital scope use to obtain this data, it was not possible to obtain complete transitions between the observed steady state oscillations presented in tables 15.6 and 15.7. In the tables, the larger ranges reported for particular data samples by the scope are due to the capture of a portion of the response of

Table 15.7: Observed range of values assumed by the Stargrazer One hardware prototype for each data acquisition by the digital scope. Stargrazer One is responding to the test vector presented in figure 15.6. For the columns that list only two numbers with the word "through" between them: the digital scope was able to capture a portion of Stargrazer One's transition to the new maximum power point. To keep the table at a manageable number of columns, only the absolute lowest and highest State One values are presented for these data captures. All State One values are reported as multiples of the Stargrazer One system clock period.

Data Capture Number	Observed Range of State One Values
1	{62, ... 15}
2	{20, 19, 18, 17, 16, 15}
3	{20, 19, 18, 17, 16, 15}
4	{20, 19, 18, 17, 16, 15}
5	{20, 19, 18, 17, 16, 15}
6	{20, ... 14}
7	{18, 17, 16, 15, 14}
8	{9, 8, 7, 6}
9	{10, 9, 8}
10	{10, 9, 8}
11	{10, 9, 8, 7}
12	{10, 9, 8, 7}
13	{10, 9, 8, 7}
14	{10, 9, 8, 7}
15	{28, ... 17}
16	{41, ... 33}
17	{40, 39, 38}
18	{52, ... 41}
19	{54, ... 47}
20	{52, ... 44}
21	{52, 51, 50, 49, 48, 47}
22	{51, 50, 49, 48, 47}
23	{51, 50, 49, 48, 47}
24	{51, 50, 49, 48, 47}

Stargrazer One to the simulated change in the environment. A resistance substituter are was used to facilitate the change in the short circuit current. Changes in the resistance was done manually. Due to this, a transition was sufficiently slow so that the digital scope could capture a portion of the transition. The observed transitions were all either monotonically increasing or decreasing. This demonstrates that imposing a constant delay between calculations will benefit performance. Stargrazer One was able to actively seek the maximum power point despite the transitions in the converter and the noise evident in the step down power electronic converter.

For each test vector, the experiment was repeated multiple times. The architecture

was found to assume the same range of values when in steady state operation. This can be seen in tables 15.6 and 15.7. The tables present a variation in the size of the steady state of oscillation but the same State One values consistently appear. This further validates the correct operation of the Stargrazer One architecture.

Validation Conclusions

In this section, a physical implementation of Stargrazer One has been described and tested. The previous chapters defined and validated this proposed system only at theoretical or simulation levels. Furthermore, the developed models were either strictly analog (the study of the switched capacitor step down converter) or strictly digital (the testing of the Stargrazer One power point tracking architecture). The developed hardware prototype brings the switched capacitor step down converter and the Stargrazer One power point tracking architecture together. This has not been done at any point in this thesis prior to this section.

An important validation benchmark is whether the system can successfully seek and remain at the maximum power point. In spite of non-ideal effects (such as signal noise), Stargrazer One has demonstrated the ability to seek and maintain operation at the maximum power point. This demonstrates that the architecture defined in part III can properly interact with a switched capacitor step down converter to optimize power leaving a solar cell source.

Further evidence in favor of this architecture is demonstrated by the second experiment presented in this section. Stargrazer One when presented with simulated environmental changes was observed to transition to the new maximum power point. Stargrazer One consistently arrived at the appropriate range of transistor T1 on times for each transition in the two test vectors presented. The observable transitions between maximum power points suggest that the power point tracker is robust to the charge redistribution that occurs inside the switched capacitor step down converter after environmental changes. This experimentally supports the observations made in part II and the proposed remedy of imposing a fixed delay in the Stargrazer One architecture.

In this section, an experimental prototype of a Stargrazer One was presented. This prototype interacted with a physical implementation of the switched capacitor step down converter. This converter was placed between a circuit model for a solar cell source and a load. The experiments demonstrate that the proposed Stargrazer One architecture is able to recognize where the maximum power point is from a solar source. The experiments demonstrate that Stargrazer One is capable of responding to environmental changes properly. These experiments demonstrate that Stargrazer One is a valid maximum power point tracker for solar photo-voltaic applications.

15.2 Discussion of the Developed Architecture

Introduction

The previous section demonstrated successful operation of the Stargrazer One maximum power point tracking architecture. A motivation of this design is to present a low power, compact and simple maximum power point tracking architecture. The purpose of this section is to see if Stargrazer One satisfies these design objectives. Each one will be discussed individually in its own section.

Power Consumption

A direct measurement of power consumption by the Stargrazer One maximum power point tracking architecture was not possible. Measuring dynamic power consumption directly with the built in Xilinx power measurement tools was not possible due to the use of secondary clocks and clock gating in the Stargrazer One architecture.

However, it is possible to indirectly assess system power. Power consumption is a function of the number of resources. More gates in an architecture means more switching and more transistors leaking. While a quantitative power value may not be possible, the area of the architecture could offer qualitatively insights into the power consumption of the system. The area of Stargrazer One is discussed in the next section.

Area

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	235	11,776	1%	
Number of 4 input LUTs	759	11,776	6%	
Number of occupied Slices	442	5,888	7%	
Number of Slices containing only related logic	442	442	100%	
Number of Slices containing unrelated logic	0	442	0%	
Total Number of 4 input LUTs	759	11,776	6%	
Number of bonded IOBs	10	372	2%	
Number of BUFGMUXs	6	24	25%	
Average Fanout of Non-Clock Nets	3.69			

Figure 15.7: Resource usage information from the Xilinx ISE design tool. This presents how much of the field programmable gate array is being used by the implementation of Stargrazer One. The field programmable gate array used is a Xilinx Spartan 3 XC3S700AN -4 FGG484.

Figure 15.7 presents the resource usage in the Spartan 3AN by the implementation of Stargrazer One. The resource usage is separated by item type. It is important to note that the logical elements inside the field programmable gate array chip consist

of look up tables (LUTs), D flip flops and multiplexers [33]. This is reflected in the resource utilization table presented in figure 15.7. The table in figure 15.7 permits an estimation of area based on resources used.

According to figure 15.7, 7% of the available slices are occupied. A slice is the smallest functional block in a Xilinx FPGA [33]. For completeness, for this family of devices a slice contains two look up tables and two flip flops [33]. For the particular FPGA used for the hardware prototype (XC3S700AN -4 FGG484), the total number of gates inside this device is 700,000 [33]. Assuming that the FPGA consists entirely of configurable slices, 7% slice utilization means Stargrazer One uses roughly 49,000 gates. This value includes the interfacing circuitry to talk to relevant components on the Spartan 3AN development board and oversized components in the data path.

As stated earlier, a slice consists of two look up tables (small memories) and two D flip flops [33]. Schematics of the slice can be viewed by consulting reference [33]. IN a slice, there are additional logical resources used to program the lookup tables and route signals. An application specific integrated circuits (ASIC) implementation could be made more compact then the implementation of Stargrazer One presented on FPGA technology in this thesis. The result would be a solution requiring fewer gates than the 49,000 currently estimated.

Considering the results presented, Stargrazer One has satisfied the desire for a small area implementation. Despite the shortcomings of FPGA technology in terms of minimizing gate count, Stargrazer One was shown to use a small fraction of the available resources in the chosen FPGA device.

Simplicity

It was necessary to translate this desired system characteristic into requirements that can be engineered. The resulting translation of simplicity used for Stargrazer One is listed below:

1. The design shall not use current sensing to compute power.
2. The design shall not use a micro-controller.
3. The design shall not use division
4. The design shall be able to generate the signals to drive the power transistors in the switched capacitor step down converter.
5. The architecture should use minimal hardware.

This definition of simplicity was adopted and applied in the development of Stargrazer One. The execution of these requirements is reflected in the design of the architecture presented in part III. The first four requirements were met and can be verified by examining the architecture presented in part III. The fifth requirement is admittedly optional as there were cases where minimum hardware would come at too much of a cost. For example, the array multiplier used in the architecture of Stargrazer One could have been replaced by a serial multiplication architecture. The

hardware requirements of a serial multiplier are significantly less than the multiplier used but the cost is a significant loss of speed. Methods to compensate for the speed (such as a custom clocking circuit) could introduce unnecessary complexity.

Conclusions

In this thesis, the design and test of an alternative architecture for maximum power point tracking applications is presented. Goals in the design of this architecture involve its size, the power used and if it is "simple"(as defined by the requirements listed in the previous section). While some metrics could be directly measured some could not, the architecture succeeds in meeting the design goals set.

15.3 Directions For Future Research

Introduction

This document has presented a unique approach to maximum power point tracking of solar photo-voltaic sources. In part II, it was decided to use a switched capacitor power electronic circuit to interface between the solar source and the load. Part III presented the architecture of the power point tracker. This part shows the developed systems are valid by demonstrating its ability to function via experimental study.

The purpose of this concluding section is to bring light on observations made as this system was being developed. The items discussed are valid directions for subsequent work to improve the candidacy and viability of Stargrazer One in a power point tracking application. This discussion will only be confined to the most notable observations made as Stargrazer One was developed. They are listed as follows:

- Revising the synchronous design of the digital architecture in Stargrazer One.
- Revising the functional unit to drive the power transistors of the switched capacitor step down converter
- Making Stargrazer One compatible with other kinds of power electronic circuits.
- Addressing how the step down converter in State One (where the solar source is charging capacitor C1) traverses a large range of voltage values.

Each of these points will be discussed in their own section.

Synchronous Design of the Digital Architecture

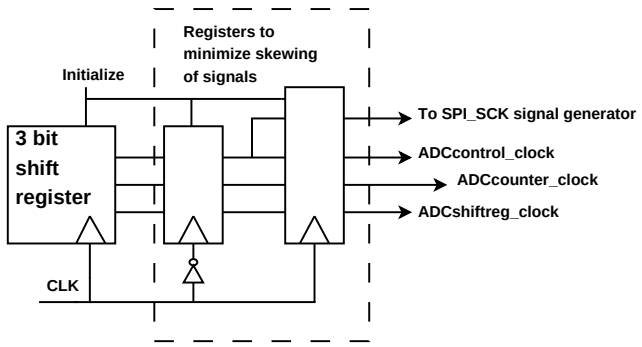

Figure 15.8: Illustrative graphic presenting the clocking pattern presented to the synchronous circuit elements in the ADC unit interface circuitry discussed in appendix 15.3. This image is repeated from that appendix.

In order to function correctly, Stargrazer One uses several synchronous elements serviced by a global clock. Every functional block (excluding the data path circuits) require the use of this clock. The need to implement a multi stage algorithm made selecting a sequential type circuit a natural choice. As discussed in part III, several

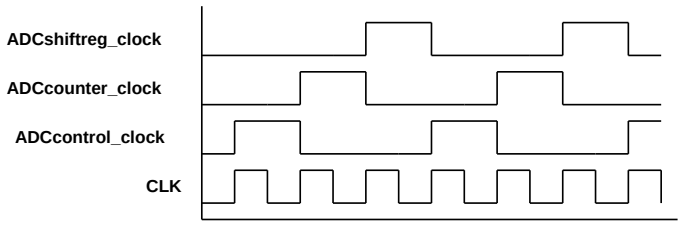

Figure 15.9: Example architecture that could be used to generate the clocking waveforms presented in figure 15.8. This architecture was implemented for the ADC unit interface circuitry presented in appendix 15.3.

functional blocks depend on a single clocking signal. Unfortunately, making sure that these functional blocks successfully talk to each other within the constraints of a single clock signal presented some challenges in the development of Stargrazer One. In order to avoid timing issues, additional modules needed to be added to several of the functional units. While sufficient and permissible for a demonstration prototype, it would be meritorious to find improvements.

A simple improvement would be to apply the clocking scheme developed in appendix 15.3 to operate the analog to digital converter (ADC) unit interface circuits. The developed and validated architecture is repeated in figure 15.8. The generated clocking pattern for the functional units is presented in figure 15.9. The reader is encouraged to read appendix 15.3 for details on the development and validation of this clocking circuitry. This scheme could be easily adapted for the next iteration of Stargrazer One. Using the scheme proposed in figure 15.8, the extraneous modules created to preserve timing integrity could be removed. Validating this hypothesis along with a study of how much hardware can be removed can be done with subsequent research.

A more ambitious project could entail replacing the logic family that is used to build Stargrazer One. There exist logic families that are asynchronous. The potential benefits are the removal of a clocking network altogether. This can translate into significant simplification in the implementation of the Stargrazer One system. A benefit would be the elimination of the clock tree. Research on this matter may yield additional benefits or complexities.

Simplification of the Output Circuitry

Figure 15.11 presents the circuitry used to drive the gates of the switched capacitor power electronic circuitry. This is referred to as the output circuit in part III. While able to properly perform its duties, it is observed that this circuitry may not be the most compact solution possible. A valid avenue for subsequent work is to devise a more compact output circuitry. A solution that can properly respond to power comparisons and interact with the step down power electronic circuit with fewer functional units can only help to further reduce Stargrazer One's footprint and power consumption.

Making Stargrazer One Compatible With Other DC to DC Converters

Part II discusses the trade off of transfer efficiency that come as a consequence of choosing the particular switched capacitor step down converter design. A survey of literature revealed documents which compared different types of power electronic circuits. For example, document [10] compares the range of impedances that a power electronic converter can present. The paper examines several types of converter (buck, boost, buck-boost and buck-boost variants) [10]. The most relevant finding is that the buck-boost power electronic converters can present the largest range of impedances to a solar cell. The converter used in this thesis is a step down converter. The buck converter (a type of step down converter) discussed in paper [10] was not able to present as many impedances to the solar cell as the buck-boost power electronic devices studied. It is important to recognize that the switched capacitor step down converter architecture is radically different than the buck converter discussed in paper [10]. That said, the major point is still valid. It would be ideal to have the Stargrazer One architecture be able to function correctly with a range of power electronic circuits as they display differing performance characteristics. Switched capacitor converters may not be desirable for all applications. Limitations of the chosen step down switched capacitor converter has already been demonstrated in this thesis. For example, in applications where high frequency switching is desired, the converter exhibits inductive behavior. Energy is being lost in energizing the parasitic inductors' magnetic field. A Stargrazer One design compatible with multiple converters will permit designers to take advantage of this innovative design in more applications.

It has been demonstrated that the output of circuitry is not transferable. It has been designed to specifically interact with the particular type of power electronic device discussed in part II. However, the same should not hold true for the remaining circuit elements. Part III, describes how Stargrazer One computes power using the following basic relationship:

$$P = \frac{\Delta E}{\Delta t} \tag{15.1}$$

Where P is power, ΔE is a change in energy and Δt is a change in time.

A valid hypothesis is: if it is possible to measure the movement of energy from the solar cell source to a load by measuring voltage changes with a chosen power electronic circuit, Stargrazer One should be able to function with that power electronic circuit (ignoring the required revisions to the output circuitry). Determining what power electronic circuits can be used with Stargrazer One is an excellent topic for more research. Devising revisions to permit Stargrazer One to operate with more types of power electronic circuits is just as also a valid direction for more research. The end result would be a specialized maximum power point tracking architecture that could be used in even more applications.

Capacitor C1 Voltage Swing

In part II, emphasis was placed on attempting to improve the transfer efficiency of the switched capacitor step down converter. These activities, while successful in

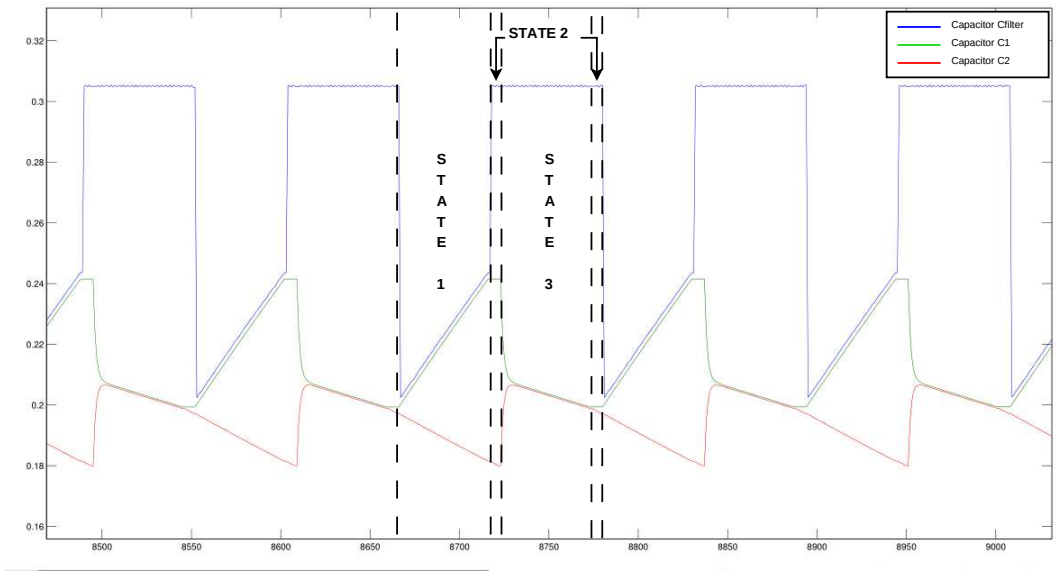

Figure 15.10: Theoretically generated waveforms of capacitors C1, C2 and Cfilter as a function of time. Operating state of the converter is clearly labeled. Each capacitor voltage being traced is labeled. This is a plot created from the theoretical models developed in part II.

improving the efficiency, exposed an interesting area for improvement. Figure 15.10 presents a wave trace of the voltages of the capacitors in the converter. In particular, please note the behavior during State One for capacitor C1. To repeat, State One is when the solar cell source is charging capacitor C1. During this state, capacitor C1 traverses a very large range of voltages. This means that the solar source is not operating at or near the maximum power point voltage for the entire time that the system is in State One. It would be preferable to have the voltage on capacitor C1 remain at or near the maximum power point voltage for the entire time the system is in State One. The maximum power point tracking system as it is ensures that the range of voltages assumed by capacitor C1 includes the maximum power point voltage. However, if the switch capacitor power electronic converter was further enhanced so that operation remains near the maximum power point voltage during State One, the power movement through the converter may be enhanced. The validation of this hypothesis and modifications to the step down switched capacitor power electronic circuit present a valid avenue for further research.

Final Comments

This thesis presented a novel implementation for the perturb and observe maximum power point tracking algorithm. This brief section has described several directions for improvement of this design. This is by no means an exhaustive list. The development of compact customizable solutions like Stargrazer One for power point tracking application presents another tool for designers interested in renewable energy systems. Stargrazer One presents another option for designers who need or want maximum

power point tracking without the extra overhead presented by general purpose processors.

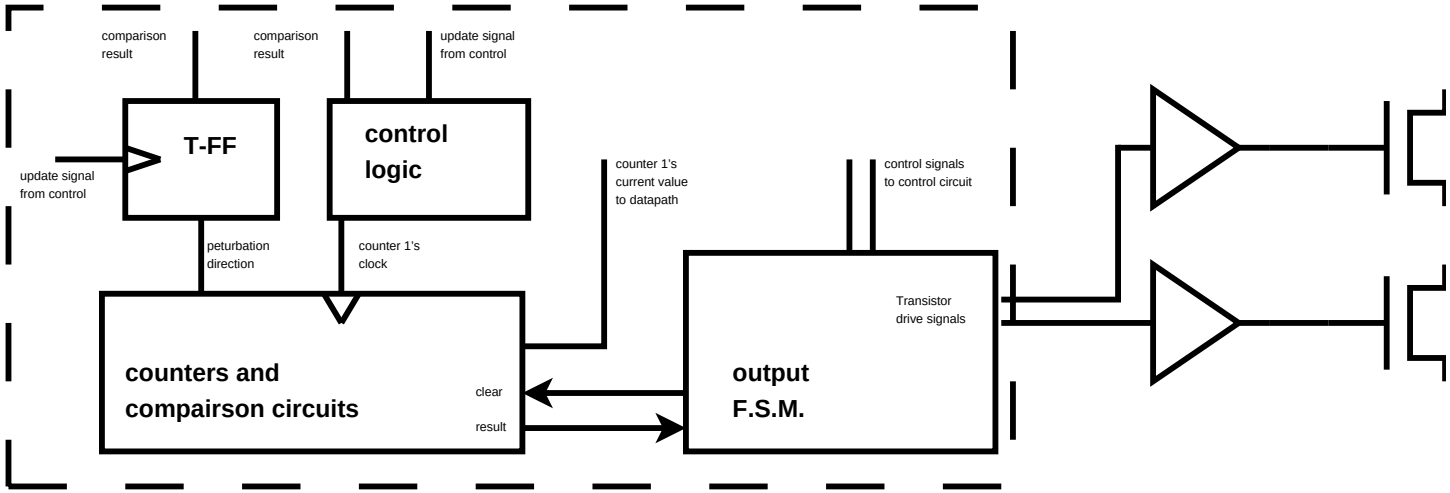

Figure 15.11: Second level schematic view of the output circuitry used in Stargrazer One. This is repeated from part III.

Appendices for Part I

Procedure Used In Literature Surveys

Introduction

The purpose of this appendix is to discuss in detail how the literature was examined in chapter 3. The time frame chosen for the survey is quite large and the resulting body of work is equally copious. In order to conduct this survey in a timely manner, it was necessary to develop a means to rapidly sift through the work. However, the increase in speed must not result in loss of thoroughness. A satisfactory balance was made between these two needs.

Procedure

Given the objectives involved (which is to try to find examples of solar cell maximum power point trackers like Stargrazer One), the search used terms which were generally broad in nature. The search terms are listed below.

- Maximum Power Point Tracker
- Micro Power Point Tracker
- Digital Power Point tracker
- Simple Power Point Tracker

The procedure is fairly straightforward. For each keyword, results were examined. Notable records were noted and retained for future reference and study. The results were continuously examined until either complete or the overwhelming majority of result content was not related to maximum power point trackers for solar cells.

Each data base used permitted a certain degree of control over the search. With the intention of reducing irrelevant results the following search setups were used for the databases:

- **IEEE Data Base**

  For all search terms, the IEEE data base was searched for them through both the full text and metadata of the files. To increase the relevant results, the search for the key words included the titles, abstracts, and index terms of the files in the database. Only content available for complete examination was searched. All IEEE affiliate publishers were included in the survey. It was possible to select the type of documents to be examined. The documents chosen were conference papers, journal articles, books and standards. To remove irrelevant results, appropriate subject headers were selected. The fields designated "computing and processing hardware/software", "components, circuits, devices

and systems" were selected. These were chosen as the interest is to find hardware implementation of solar cell maximum power point trackers. The field "power, energy and industry applications" was selected as maximum power point tracking falls within this category. It may be possible that very relevant literature may be classified under this area and not appear in the results of a search solely using circuits or hardware subject headers. The same logic applies to the selection of the fields "signal processing and analysis" and "robotics and control". Due to the extensiveness of this database, the search was performed in decade increments.

- **ISI Web of Knowledge**

  The search for the keywords included subjects or titles. The resources available in the database were found to be divided into three general citation data bases. The citation database most relevant to the search was the "science citation index expanded". Therefore, all searches were done only using this data base alone. Due to the extensive volume of contents, all searches were performed in decade increments. It was possible to designate the language of the items retrieved. For ease of reading, all results that have been written in English were considered. The search scanned all available document types in the data base.

- **Patent Survey**

  The scope of the search included United States payments and United States patent applications. Also for completeness, the survey included available information from the World Intellectual Property Organization (WIPO). To improve result yield, the search included the titles, abstracts, and in the content of the files. Since the volume of results was large the search was confined to decade increments. Also to save time results were sorted by relevancy.

Appendix for Part II

Investigation Into the Sensitivity of the Charge Redistribution In State Three Between Capacitors C1 and C2 to Environmental Change and State One Duration

Introduction

The time optimizations for States Two and Three presented in section 9.2, are to be implemented as fixed values. The motivator behind this decision is the simplicity of the solution. It is possible to achieve additional performance improvement by adjusting the State Two and State Three durations in response to the operating conditions. However, any performance gain will come at the expense of increased computing hardware.

Before designating the fixed times for States Two and Three, it was necessary to determine if the duration for the energy transfer between capacitors C1 and C2, if any, is sensitive to environmental and State One duration effects. This has bearing on whether or not a fixed duration solution is possible for State Three. State Two can be fixed as no energy exchange occurs. The purpose of this appendix is to present how this investigation was performed and the results.

Procedure

Using the MATLAB environment, a script was developed to carry out this study. Using the step down converter equation model defined in section 8.1, a converter model was instantiated. This model was subjected to changing temperature, light and State One duration. The assumptions that this experiment was performed under and the specific tests performed are enumerated below. Experimental assumptions are listed first:

- Converter components are highly resistant or immune to temperature and light variation
- All parasitic effects besides switch on resistance assumed negligible
- Solar cell power source is ideal
- The converter is in "steady state" (no net change in the average charge in capacitors C1 and C2 as time advances)
- Ideal switching on both transistors

The following lists the tests performed:

- System subjected to a temperature range of 255 to 394 degrees Kelvin [or 0 to 250 degrees Fahrenheit]. This range is based off of operating temperature ranges reported in several commercially available solar panel technical specifications.

- System presented with a range of illuminations from 100 to 1000 $\frac{W}{m^2}$.
- Time spent in State One is varied from 1 to 164 μs. State Two time will be held constant at 1 μs.

Results With Conclusions

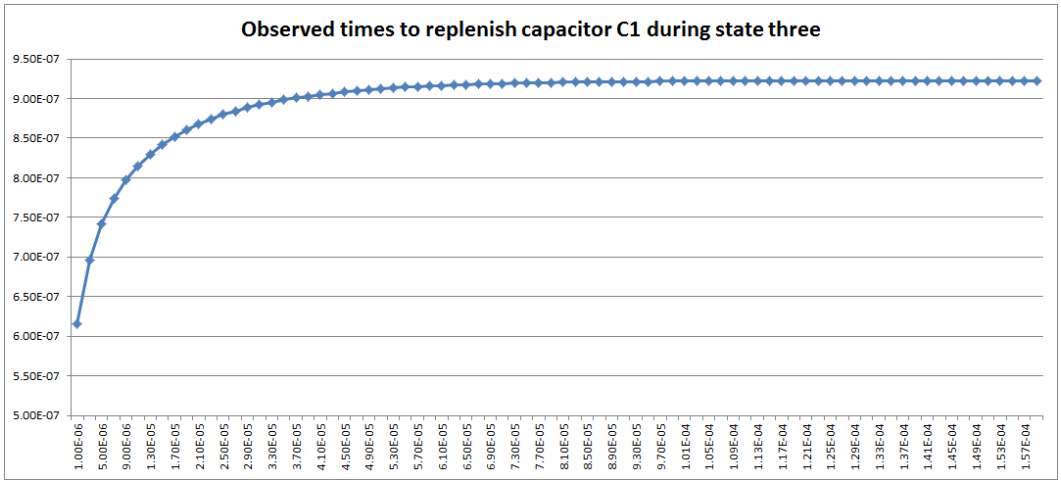

Figure 1: Study results. X axis is the length of time spent in State One. Unit is in s. Y axis is the length of time needed to replenish capacitor C2. Unit is in s.

Table 1: Experimental results for varying light intensity. All times are reported in seconds. Note the modest changes between the values.

	Results for these State One values		
light in $\frac{W}{m^2}$	1 μs	10 μs	100 μs
100	$6.15631105 * 10^{-7}$	$8.06699340 * 10^{-7}$	$9.21878128 * 10^{-7}$
200	$6.15632065 * 10^{-7}$	$8.06699048 * 10^{-7}$	$9.21874734 * 10^{-7}$
300	$6.15632265 * 10^{-7}$	$8.06698240 * 10^{-7}$	$9.21874866 * 10^{-7}$
400	$6.15632292 * 10^{-7}$	$8.06696375 * 10^{-7}$	$9.21874128 * 10^{-7}$
500	$6.15632228 * 10^{-7}$	$8.06692101 * 10^{-7}$	$9.21877424 * 10^{-7}$
600	$6.15632119 * 10^{-7}$	$8.06682291 * 10^{-7}$	$9.21877188 * 10^{-7}$
700	$6.15631947 * 10^{-7}$	$8.06659868 * 10^{-7}$	$9.21877177 * 10^{-7}$
800	$6.15631723 * 10^{-7}$	$8.06609950 * 10^{-7}$	$9.21877177 * 10^{-7}$
900	$6.15631422 * 10^{-7}$	$8.06506629 * 10^{-7}$	$9.21877177 * 10^{-7}$
1000	$6.15631048 * 10^{-7}$	$8.06592628 * 10^{-7}$	$9.21877177 * 10^{-7}$

It was found that the time needed to re-energize capacitor C2 was effectively insensitive to heat and light. The term "effectively" is used as there were observed variations but the changes took place after a minimum of four significant figures for the case of varying light and three for the case of varying temperature. Do to this small variation, the effects from these two factors can be assumed negligible. The

Table 2: Experimental results for varying temperature. All times are reported in seconds. Note the modest changes between the values.

	Results for these State One values		
temperature ^oK	1 μs	10 μs	100 μs
255	$6.1562961 * 10^{-7}$	$8.0665406 * 10^{-7}$	$9.2187718 * 10^{-7}$
269	$6.1563018 * 10^{-7}$	$8.0654738 * 10^{-7}$	$9.2187718 * 10^{-7}$
282	$6.1563065 * 10^{-7}$	$8.0678234 * 10^{-7}$	$9.2187718 * 10^{-7}$
296	$6.1563102 * 10^{-7}$	$8.0659447 * 10^{-7}$	$9.2187718 * 10^{-7}$
310	$6.1563134 * 10^{-7}$	$8.0671397 * 10^{-7}$	$9.2187718 * 10^{-7}$
324	$6.1563159 * 10^{-7}$	$8.0650156 * 10^{-7}$	$9.2187718 * 10^{-7}$
338	$6.1563179 * 10^{-7}$	$8.0655502 * 10^{-7}$	$9.2187718 * 10^{-7}$
352	$6.1563198 * 10^{-7}$	$8.0659290 * 10^{-7}$	$9.2187718 * 10^{-7}$
366	$6.1563213 * 10^{-7}$	$8.0661631 * 10^{-7}$	$9.2187718 * 10^{-7}$
380	$6.1563227 * 10^{-7}$	$8.0663511 * 10^{-7}$	$9.2187718 * 10^{-7}$
394	$6.1563239 * 10^{-7}$	$8.0664859 * 10^{-7}$	$9.2187718 * 10^{-7}$

observed results can be viewed in table 1 (for the case of varying light) and table 2 (for varying temperature). The small variations observed reflects the fact that the components in the converter were assumed unaffected by the environment. In practice, there are no circuit elements that are fully unaffected by the environment but it is possible to obtain highly resistant pieces. With such devices the above results can be assumed correct.

The length of time that the converter stays in the other states proved to have a more significant impact. Figure 1 shows this graphically. The length of time needed for capacitor C1 to replenish capacitor C2 increases as the length of time spent in the other states increases.

Final Comments

Assuming environmentally resistant converter components, the optimal State Three duration will change as a function of the time spent in State One. Since a fixed duration for State Three is to be used, it is best to select a fixed duration which can accommodate the observed charge exchange from the longest possible State One duration for the particular design.

Experimental Investigation Into the Effect of Increasing State One Duration On Gains Obtained From the Proposed Adjustments in Section 9.2

Introduction

The proposed optimizations for States Two and Three will result in diminishing gains in performance as the duration of State One is increased. The purpose of this appendix is to support this with experimental data. The discussion will begin with the experimental procedure, present results then offer conclusions.

Procedure

To assess the impact of State One length on converter performance, an experiment in the MATLAB environment was prepared. Table 3 presents the design choices for the study.

Table 3: Design choices for the test in this section.

converter		
Capacitor 1	17	μF
Capacitor 2	20	μF
Load	3	Ω
Switch loss	.015	Ω
T_{state1}	5	μs

solar cell		
short circuit current	.15	A
reverse bias current	1e-7	A
thermal voltage	.0256	V

The experiment was conducted under the following conditions:

- The ideal model for the solar cell source is to be used. The model is below:

$$I(t) = I_{short} - I_o * \left(e^{\left(\frac{V(t)}{Vth}\right)} - 1\right); \tag{2}$$

  Where I_{short} is the solar source short circuit current, I_o is the reverse bias current and Vth is the thermal voltage.

- The voltage model presented in section 8.1 will be used to define the converter.
- Pursuant to the previous point, switch on resistances will be the only non-ideal effect considered. All other parasitic effects will be assumed negligible
- States two and three will both last 1 μs.
- Switching is assumed ideal.

A large range of possible State One values will be used. The selected range is from 1 to 160 μs. This range will be crossed in 5 μs increments starting at 1 μs. For each State One value, the resulting efficiency will be calculated and recorded. The procedure outlined in section 9.1 is used to compute the efficiency.

Results with Conclusions

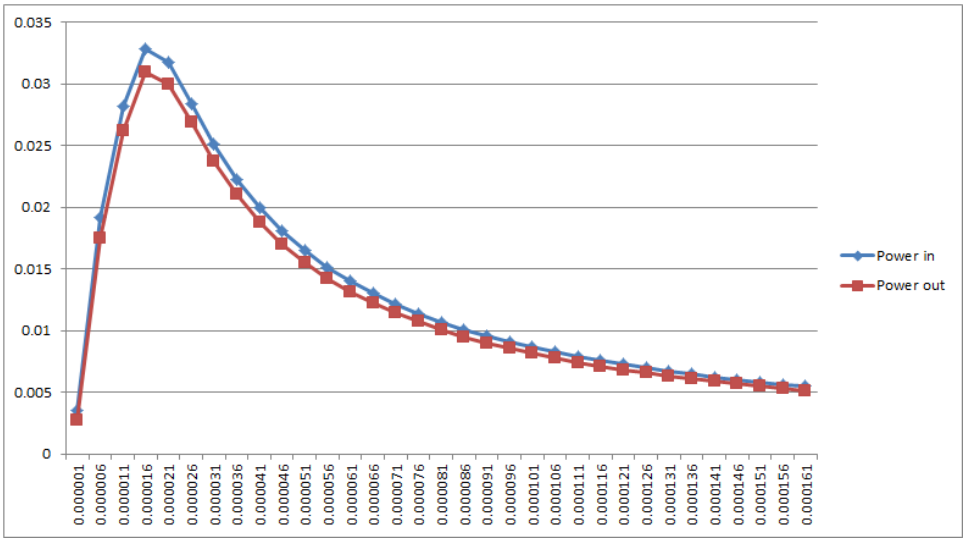

Figure 2: Computed average incoming and outgoing powers as a function of State One time. The observed "dots" are actual data points. Note that the observed maximum power corresponds to one of the highest observed efficiency values in table 4.

Figure 2 and table 4 presents graphically the results of this study. Table 4 shows the observed efficiencies as a function of the appropriate State One time. Note that the efficiency rapidly approaches a peak value then gradually begin to diminish. The observed diminishment is rather subtle.

Figure 2 shows the observed exiting and entering powers. The main purpose of including this figure is to note that the highest observed efficiency values appear to correspond to the maximum computed average power. This suggests that when operating at the maximum power point the converter should operate at or near peak performance.

Final Conclusions

As expected, increasing State One duration will diminish the gains from optimizing States Two and Three. The observed fall of was not very extreme but does lend empirical support for the assertion made in this appendix. An unexpected observation is that the converter's performance is maximized when the power flow through the circuit is greatest. Since, the maximum power point tracker will try to operate the converter in this condition at all times, this further bolsters the candidacy of this converter in designs.

Table 4: Calculated efficiency values for the state one durations tested reported to three significant figures.

Experimental Data	
State One Length	Computed Efficiency
1.00E-06	0.785
6.00E-06	0.911
1.10E-05	0.932
1.60E-05	0.942
2.10E-05	0.945
2.60E-05	0.945
3.10E-05	0.945
3.60E-05	0.944
4.10E-05	0.944
4.60E-05	0.943
5.10E-05	0.943
5.60E-05	0.943
6.10E-05	0.943
6.60E-05	0.942
7.10E-05	0.942
7.60E-05	0.942
8.10E-05	0.942
8.60E-05	0.942
9.10E-05	0.942
9.60E-05	0.941
1.01E-04	0.941
1.06E-04	0.941
1.11E-04	0.941
1.16E-04	0.941
1.21E-04	0.941
1.26E-04	0.941
1.31E-04	0.941
1.36E-04	0.941
1.41E-04	0.940
1.46E-04	0.940
1.51E-04	0.940
1.56E-04	0.940
1.61E-04	0.940

Appendices for Part III

Equation by Equation Validation of Data Path Circuit

Introduction

As discussed in section 13.1, the Stargrazer One data path circuit executes a series of computations to produce the required power comparison. The required computations are now repeated for reference:

$$Calculate : \Delta E[k-1] * T_{cycle}[k] \tag{3}$$

$$Calculate : (V_{C1}^{max})^2, (V_{C1}^{min})^2 \tag{4}$$

$$Calculate : \Delta E[k] = (V_{C1}^{max})^2 - (V_{C1}^{min})^2 \tag{5}$$

$$Calculate : \Delta E[k] * T_{cycle}[k-1] \tag{6}$$

$$Evaluate : \Delta E[k-1] * T_{cycle}[k] \leq \Delta E[k] * T_{cycle}[k-1] \tag{7}$$

In all equations $\Delta E[k]$ is the current energy leaving capacitor C1, $\Delta E[k-1]$ is this energy for the previous adjustment, $T[k-1]$ is the previous converter cycle length, $T[k]$ is the current converter cycle length, V_{c1}^{max} is the maximum capacitor C1 voltage and V_{c1}^{min} is the minimum capacitor C1 voltage.

The purpose of this appendix is to demonstrate that the proposed data path circuit executes these equations properly. The architecture has been shown to function correctly in section 13.1. The purpose of this appendix is to demonstrate that the data path architecture functions correctly for each specific equation.

For each equation, the movement of information through the data path circuit will be described and validated by simulation. For all simulation wave traces: signals labeled "actual" come from the proposed architecture, signals labeled "expected" come from a theoretically correct implementation created in the test bench used to validate the architecture and "discrepancy" compares these two signals.

Equations 4 and 5

Figure 3 presents the required movement of data to execute equation 4. The figure clearly presents how data is to move. To make sure the appropriate hardware is available, the control circuit will deliver the appropriate commands to the multiplexer circuits. Operation begins with register seven which contains the required voltage value from capacitor C1. As shown in figure 3, the array multiplication unit is used to execute the squaring. Both inputs are the value in register seven, therefore, the result is this value taken to the second power. As the minimum capacitor C1 voltage

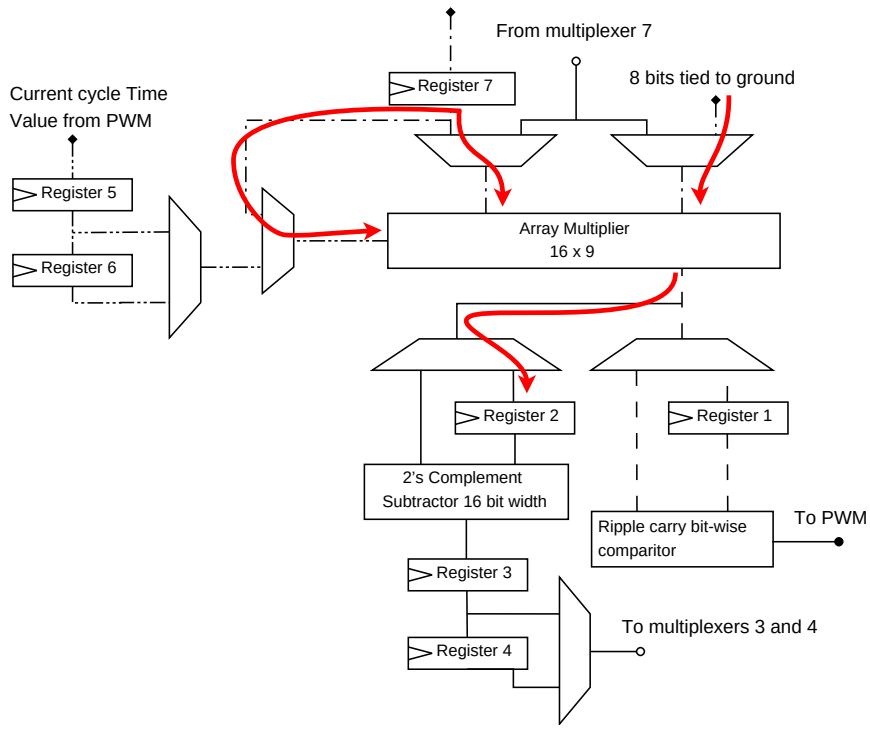

Figure 3: This is how the data path executes equation 4. The arrows indicate the direction data moves through the circuit.

is not yet known, the result must be stored in one of the data path registers. Note the need to zero pad one of the operands into the array multiplier. This is to accommodate the size of the array multiplication unit.

Figure 4 presents the required movements of data to evaluate equation 5. The movement of data is clearly presented. Register seven is again required. This time it contains the minimum capacitor C1 value. Note that the array multiplication unit is again configured to square these voltage values. Notice that now the results of the subtraction unit is of interest. The resulting difference now contains the present energy value $\Delta E[k]$. This value will be required for future use. Therefore (as shown in figure 4) the result is stored in register three.

Simulated Results With Conclusions

Figure 7 presents an illustrative simulation trace comparing the architecture to a theoretically correct reference implementation.

As relevant values are stored in registers, the simulation checks the values of all appropriate registers. For ease of reading, the data lines on the figure 7 are grouped by the physical data quantity as opposed to register numbers. This is done for all subsequent simulation traces presented.

Since equations 5 and 4 are sequential they are presented on the same figure. Note that the "discrepancy" signals remain binary zero with only brief periods in binary one. These brief binary one moments were determined to be propagation delays. This

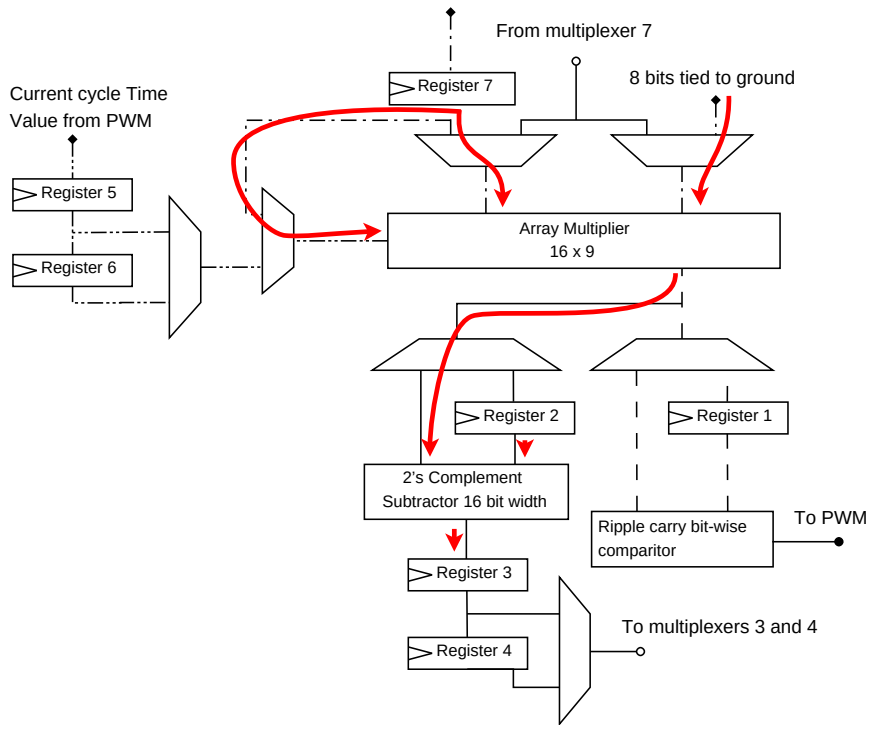

Figure 4: This is how the data path executed equation 5. The arrows indicate the direction data moves through the circuits. Note that hardware is reused.

suggests that these equations are being correctly evaluated.

Equation 3

Figure 5 shows how data moves inside the data path to evaluate equation 3. As can be seen this is a register transfer operation. The required operands are stored in registers. The current time $t[k]$ is retained in register five and the past energy $\Delta E[k-1]$ is in register four. As figure 5 shows, these register values enter the array multiplication unit as operands. The results is the solution to equation 3. The result is crucial to evaluate equation 7 and is retained for future use in register one.

Simulation Results With Conclusions

Figure 8 shows an illustrative sample of the simulated results. The test conditions are the same as for the previous subsection. Figure 8 shows the solution to equation 3 along with the required operands. Note that across the trace the physical values match and the "discrepancy" signals remain at binary zero. This suggests that the data path is correctly evaluating the equation.

Equation 6

Figure 6 presents how the data path executes equation 6. Like with the evaluation of equation 3, the action is essentially a register transfer operation. Register five contains

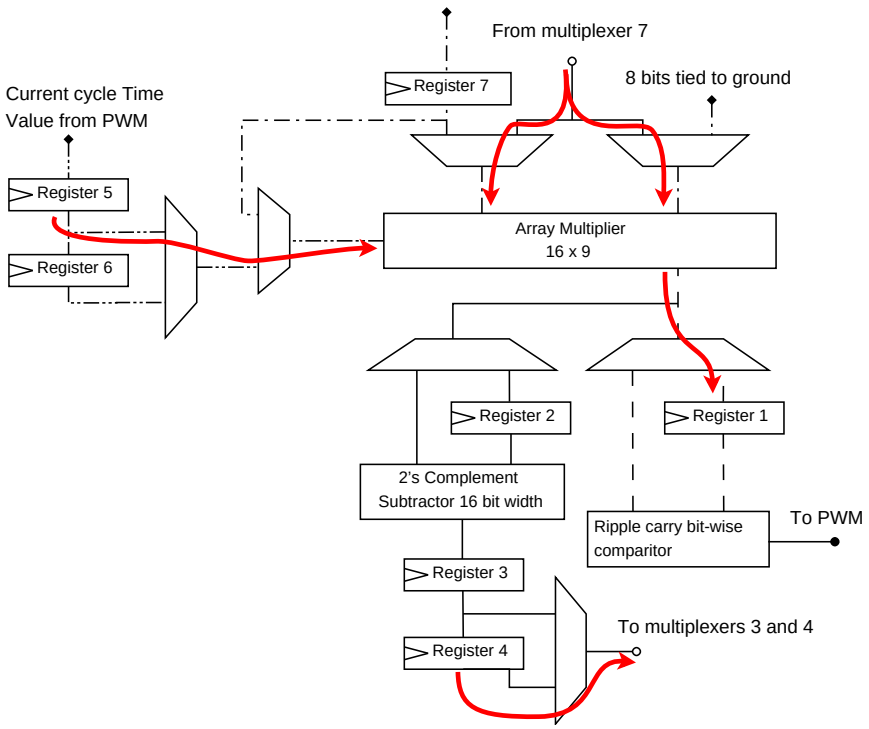

Figure 5: This is how the data path executed equation 3. The arrows indicate the direction data moves through the circuits.

the $t[k-1]$ value and register three contains the current energy value $\Delta E[k]$. The data path is configured to allow these two values to reach the multiplication unit. The solution is then sent to the comparison circuits. Since equation 7 will be promptly performed once equation 6 is evaluated, there is no register for the solution. The data path maintains this configuration to insure the correct comparison value is stored in the output circuit.

Simulation Results With Conclusions

Figure 9 presents an illustrative sample of the simulated validation for this equation. An important observation is that the "actual" result appears to change frequently. This is because the output is from a data bus as opposed to a register output. The solution to equation 6 is presented. The value of the data bus (labeled "actual" in the group "E[k]*T[k-1]" in figure 9) has the result of the evaluation of equation 7. As indicated by the "discrepancy" signals, valid operands are being supplied for this evaluation.

Final Comments

The purpose of this appendix is to provide the reader with detailed evidence to support the functionality of the developed Stargrazer One data path architecture. This expands upon section 13.1 by presenting a equation by equation analysis. The

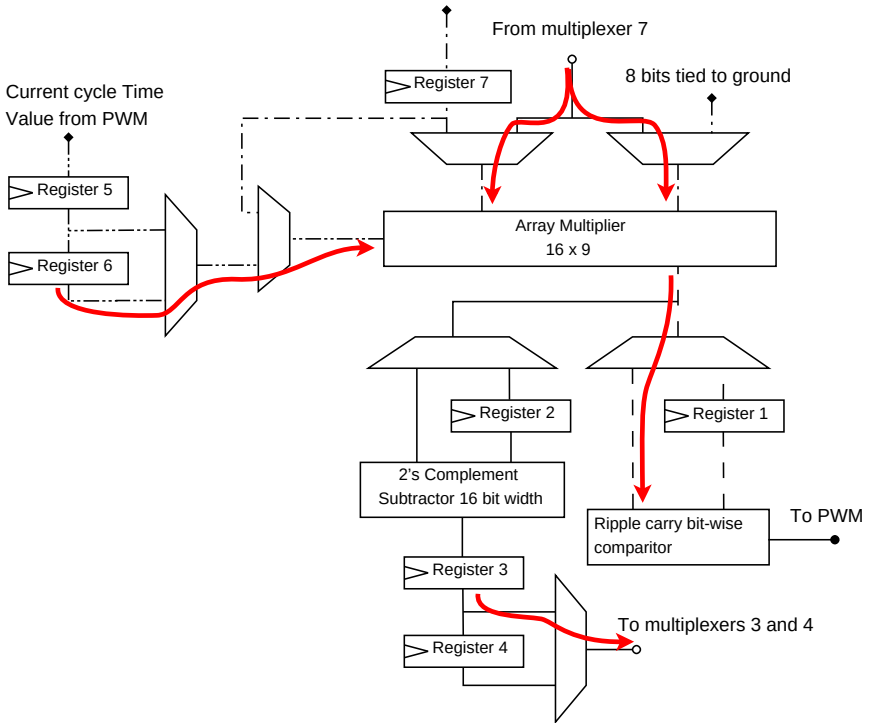

Figure 6: This is how the data path executed equation 6. The curving arrows indicate the direction data moves through the circuits.

expected operation of the data path is presented and discussed. With simulated evidence, the architecture is shown to be performing its expected duties properly.

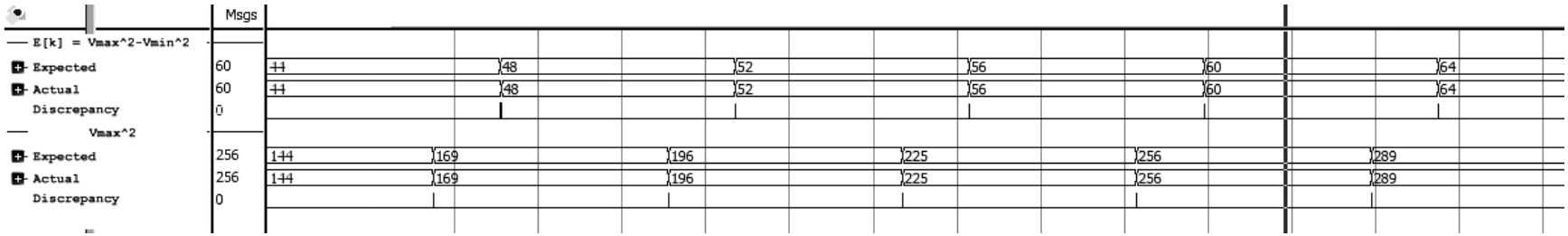

Figure 7: Illustrative sample of the validation simulation demonstrating correct implementation of the data flow shown in figures 3 and 4. Both equations covered by the figure. Note that the energy values stored are the observed change in energy across capacitor C1 for the time unit k. It was not possible to include the "Δ" symbol on the waveform tracings.

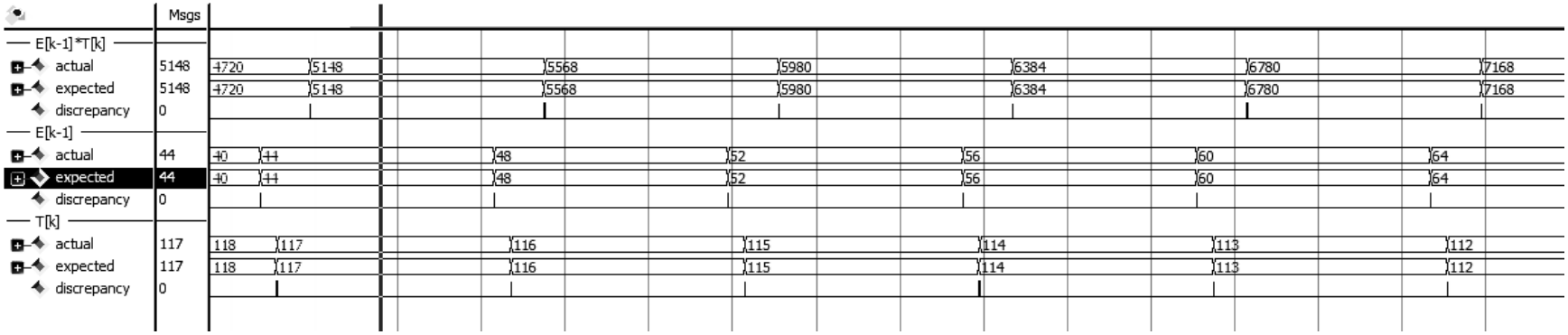

Figure 8: Illustrative sample of the validation simulation demonstrating correct implementation of the data flow shown in figure 5 and the successful evaluation of equation 3.

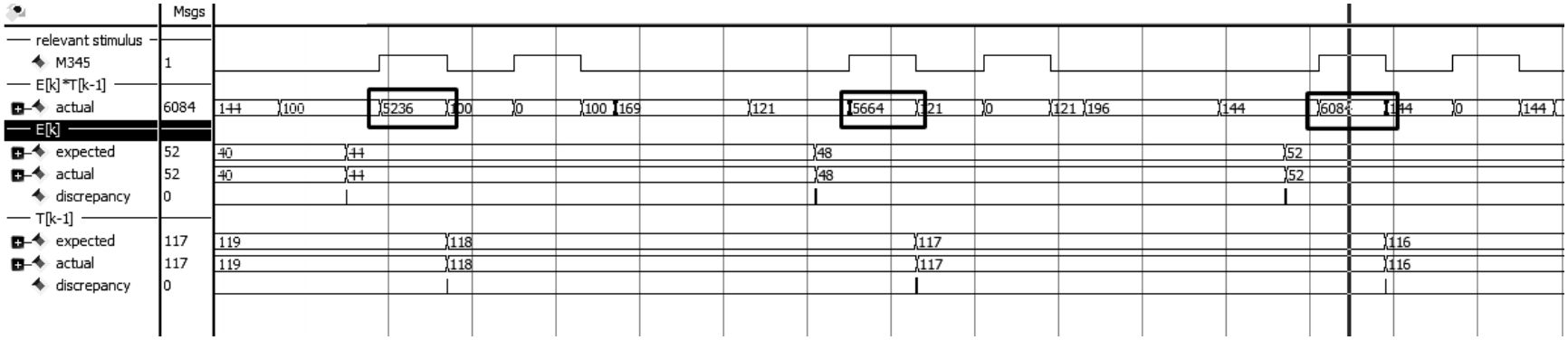

Figure 9: Illustrative sample of the validation simulation demonstrating correct implementation of the data flow shown in figure 6 and the successful evaluation of equation 6.

Validation of Design Choices to Simplify Data Path Circuits

Introduction

This appendix will present a simulated validation of the method used to evaluate equation 8 proposed in section 13.1. Equation 8 is presented below:

$$P[k-1] \leq P[k] \tag{8}$$

A simplification used in the data path circuits for the computation of energy will be discussed and validated.

Proposed Method to Evaluate Equation 8

In section 13.1, the power comparison to the executed given in euqation 8 was algebraically modified to this form:

$$\Delta E[k-1] * t[k] \leq \Delta E[k] * t[k-1] \tag{9}$$

Where $t[k-1]$, $\Delta E[k-1]$, $P[k-1]$ are the converter cycle length, computed energy and power respectively for the previous adjustment. $t[k]$ $\Delta E[k]$, $P[k]$ are the converter cycle length, computed energy and power respectively for the current adjustment.

To validate the correctness of this technique, an investigation in the MATLAB environment was prepared. In the experiment, a solar cell and switched capacitor step down power converter was defined. Two maximum power point trackers were prepared. Both used the same model for DC to DC converter and solar cell. They both implement the perturb and observe algorithm. The difference is in how they evaluate equation 8. One design will evaluate equation 8 using the proposed modification presented in equation 9. The other will evaluate equation 8 using the following equation to find $P[k]$:

$$P[k] = \frac{\Delta E[k]}{t[k]} \tag{10}$$

Where $\Delta E[k]$ is the change in energy on capacitor C1 and $t[k]$ is the converter cycle length for the current adjustment

Procedure

This experiment was performed under the following constraints:

- ideal solar cell
- switch resistor model for the transistors
- ideal converter components
- instantaneous radiation changes

- maximum power point tracker computation in the analog domain

The test presented in this document will present a case of varying solar radiation. The test vector is presented here:

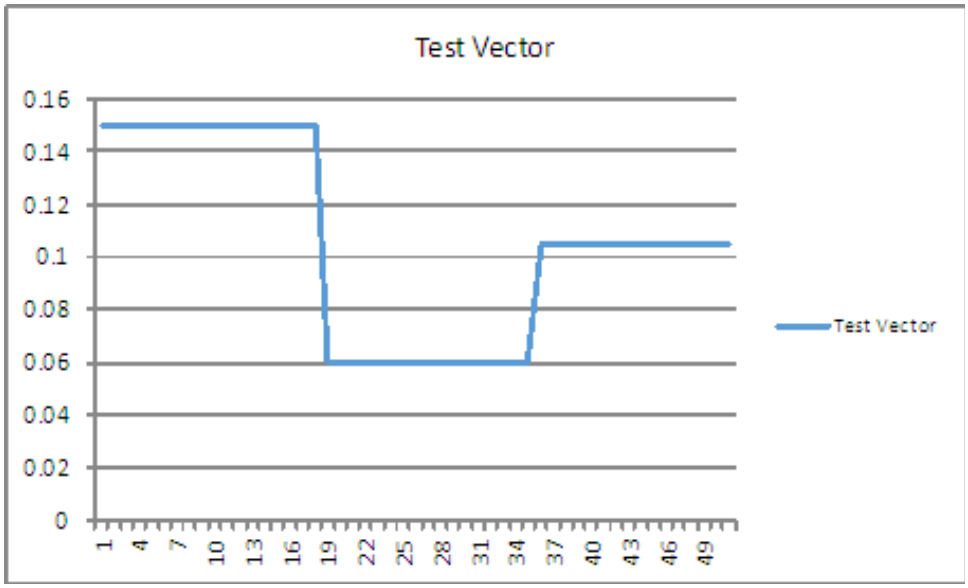

Figure 10: Irradiation test vector that will be used for the test. Y axis indicates the short circuit current in Amperes and the X axis indicates the number of power comparisons that have occurred. The short circuit current changes values during adjustment 20 and 40.

Both implementations will be subjected to the same test vector. Computed powers and duty cycle adjustments will be logged. The step adjustment size is $2\mu s$. Once both implementations have been tested, the results will be compared.

Results with Conclusions

Figure 11 presents the observed State One durations for each tracker when presented with the test vector in figure 10. Figure 12 presents the difference between the two responses.

Figure 12 does show discrepancy. However, observe that the values tend to remain between $4\mu s$ and 0. There is a period where the discrepancy is at $8\mu s$ but this is temporary. Examining 11 reveals that the periods where 12 appears to oscillate between 0 and $4\mu s$ corresponds to operation at the maximum power point. The implementations are merely dithering out of phase. The observed differences, as seen in figure 11 appear to be a one adjustment delay between both implementations. As both systems find the maximum power point, this out of phase behavior is not of concern. As both implementations exhibit arrive at the maximum power point, this test asserts that this simplification is valid. A system using the proposed method of evaluating equation 8 will function properly.

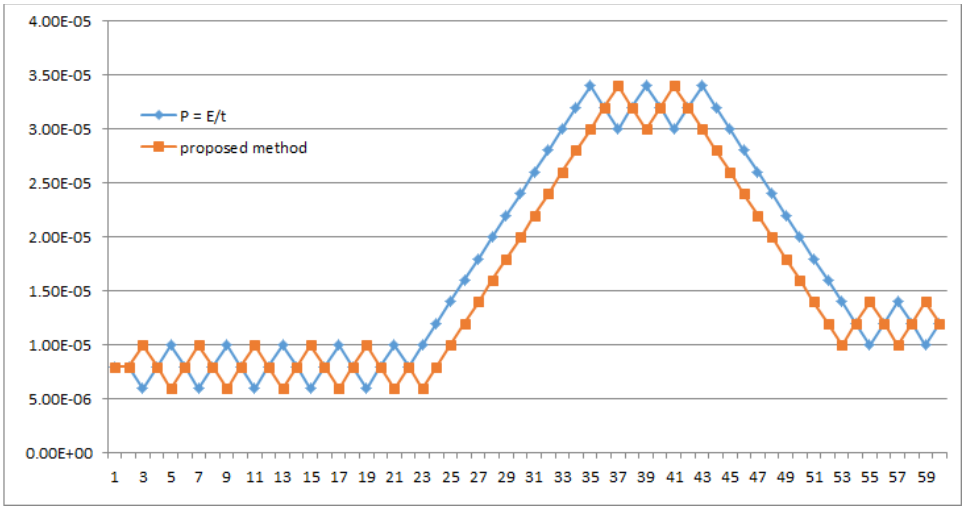

Figure 11: Resultant State One duration for both test cases. Note that both cases find the maximum power point. The trackers were designed to adjust the length of State One by $2\mu s$. This was done to ensure a timely arrival to the maximum power point. The short circuit current changes values during adjustment 20 and 40.

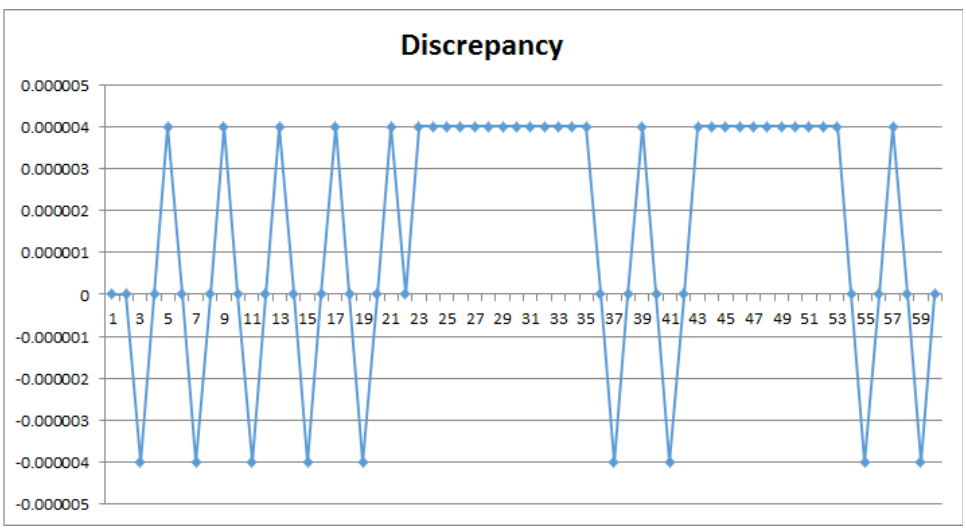

Figure 12: This figure presents the results from subtracting the data shown in figures 11. The trackers were designed to adjust the length of State One by $4\mu s$ for the generation of this plot. This was done to ensure a timely arrival to the maximum power point. The short circuit current changes values during adjustment 20 and 40.

Simplifying Computation of Energy

For a capacitor energy is given as:

$$E = \frac{1}{2} * C * V^2 \tag{11}$$

Where C is the capacitance of the particular device and V is the voltage across

the terminals. Computing an energy change across a capacitor C is given as:

$$\Delta E = \frac{1}{2} * C * V_a^2 - \frac{1}{2} * C * V_b^2 \tag{12}$$

Where V_a, V_b are the beginning and ending points of a voltage change. Notice that the capacitance along with the constant $\frac{1}{2}$ appear before each energy term. Assuming a fixed capacitance, the following manipulation can be executed on equation 12

$$\Delta E = \frac{1}{2} * C * (V_a^2 - V_b^2) \tag{13}$$

Stargrazer One does not require an accurate value of power to operate. As long as the slope of the power curve is preserved, any simplifying operation is acceptable. Removing the constant term in equation 13 is a desirable simplification. The elimination of these constants reduces the number of operations to be done. Without these constants, a designer will not need to measure a capacitor C1 value to use Stargrazer One.

The constant terms effects the magnitude of the dependent variable in the relationship in equation 13. It should follow then that the behavior of the power curve should be preserved if the constants are removed from equation 13.

An analytical argument in favor of the proposed simplification is offered by examining the tasks Stargrazer One performs. The Stargarzer One power point tracker executes the following power comparison:

$$P[k-1] \leq P[k] \tag{14}$$

Expanding equation 14 using the power relationship in equation 10 and energy equation 13 gives:

$$\frac{\frac{1}{2} * C1 * ((V_{max}[k-1])^2 - (V_{min}[k-1])^2}{T[k-1]} \leq \frac{\frac{1}{2} * C1 * ((V_{max}[k])^2 - (V_{min}[k])^2}{T[k]} \tag{15}$$

The constant terms $(C1, \frac{1}{2})$ can be canceled out producing the proposed simplification. To further validate the correctness of this simplification, an investigation in the MATLAB environment was prepared. In the experiment, a solar cell and switched capacitor step down power converter was defined. Two maximum power point trackers were prepared. Both used the same model for DC to DC converter and solar cell. They both implement the perturb and observe algorithm. Power is computed using equation 10. The difference is in how ΔE is evaluated. One design will find ΔE using equation 12. The other will use equation 13 with the constant terms ignored.

Procedure

This experiment was performed under the following constraints:

- ideal solar cell

- switch resistor model for the transistors
- ideal converter components
- instantaneous radiation changes
- maximum power point tracker computation in the analog domain

The test presented in this document will present a case of varying solar radiation. The test vector is presented in figure 10. Both implementations will be subjected to the same test vector. Computed powers and duty cycle adjustments will be logged. Once both implementations have been tested, the results will be compared.

Results with Conclusions

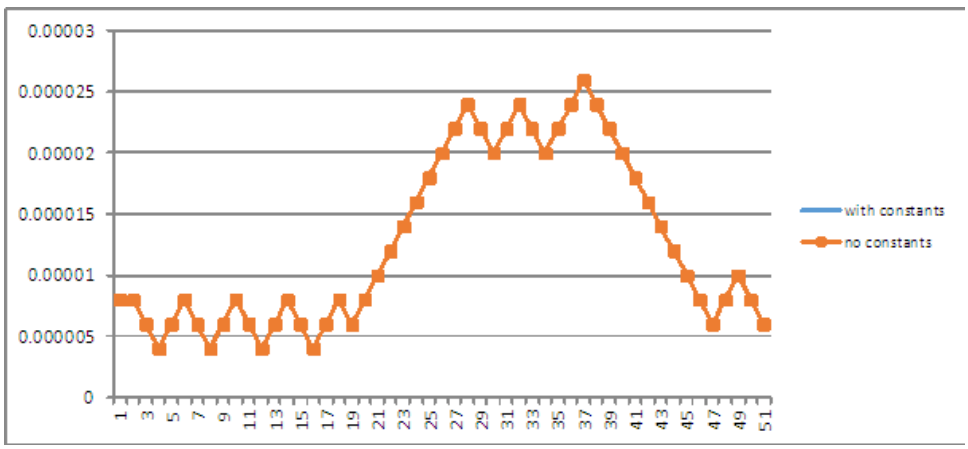

Figure 13: Resultant on time for State One for both implementations for the test. Y axis is time in μS and the X axis indicates the number of power comparisons that have occurred. The trackers were designed to adjust the length of State One by $2\mu s$ for the generation of this plot. This was done to ensure a timely arrival to the maximum power point. The short circuit current changes values during adjustment 20 and 40.

Figure 13 presents the duty cycles the tracking system assumes under both test cases. Figure 14 presents the difference between these two plots.

Observe that figure 14 is zero for the whole test. Figure 13 presents both plots superimposed. As can be observed both cases reach the maximum power point. Figure 13 shows that the two systems exhibit identical behavior. This suggests no significant loss in tracking accuracy by applying this simplification. This validates the use of this simplification.

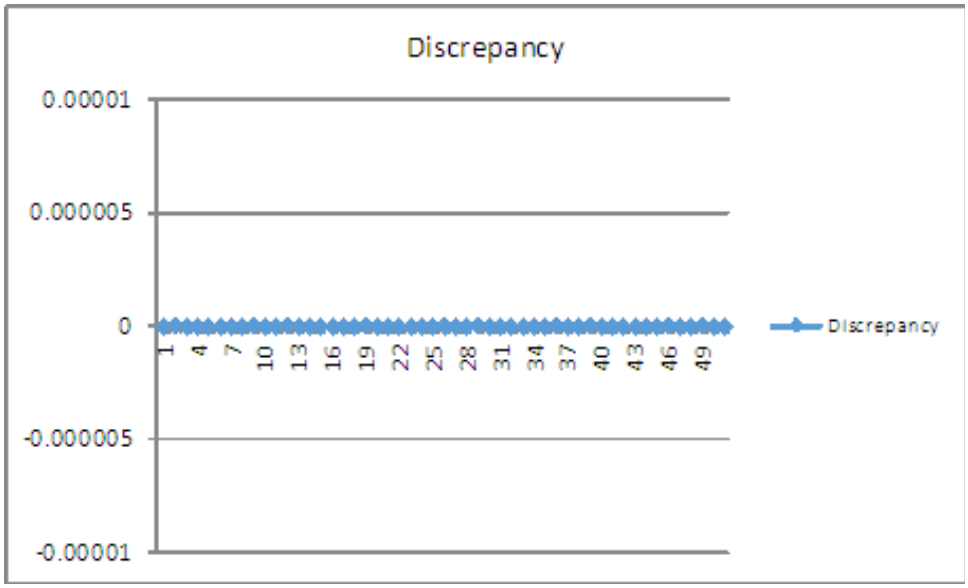

Figure 14: Difference between the transistor on times presented in 13. Y axis is time in μs and the X axis indicates the number of power comparisons that have occurred. The trackers were designed to adjust the length of State One by $2\mu s$ for the generation of this plot. This was done to ensure a timely arrival to the maximum power point. The short circuit current changes values during adjustment 20 and 40.

Discussion of Relevant Submodules Used to Construct the Data Path Circuit

Introduction

There are several sub-components in the data path architecture that merit individual discussion. This appendix will present these pieces along with providing verification of their functionality where appropriate.

Digital Comparison Circuit

Figure 15 presents a gate level view of the each bit comparison and how each of these bit comparison circuits are wired together to produce an accurate comparison of a multi-bit value.

Simulation Results with Conclusion

A Verilog description of this architecture was created and subjected to exhaustive testing at the behavioral and post place and route levels. For convenience, a four bit wide version of the comparator was used for the testing. Since a generic and structural coding style was used to describe the unit, resizing entails simply changing the generic variable.

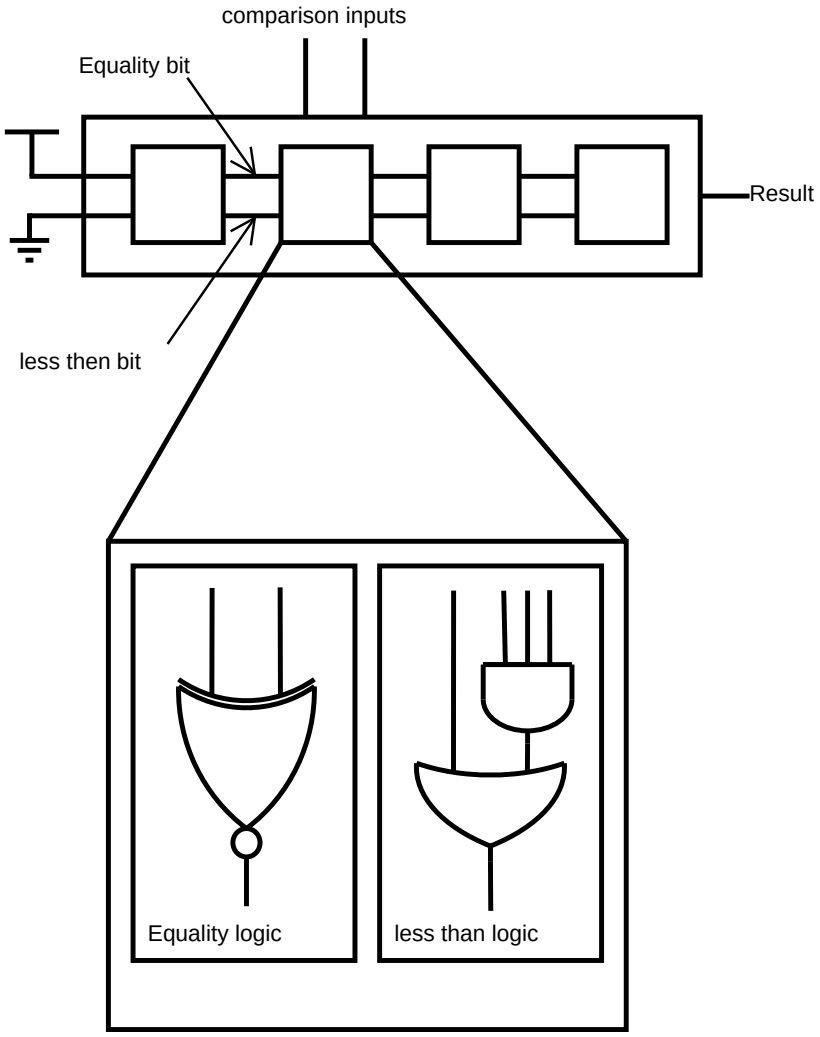

Figure 15: A module level view of the comparison circuit with a gate level description of the bit wise comparison.

Figure 18 is a snapshot of the verification tests performed. The relevant inputs are the two values to be compared. The physical quantity that each input value represents is clearly labeled. The comparison circuit is used to evaluate the following:

$$E[k] * T[k-1] < E[k-1] * T[k] \tag{16}$$

During this test the comparison circuitry performed as expected. In figure 18, the output trace labeled "expected" is produced from a theoretically correct output in the test bench. The output labeled "actual" is from the proposed architecture. The behavior of both output traces are almost a perfect match. The discrepancies are delays and glitches in the actual output trace. Since the circuit will operate at a slow clocking speed, these delays should not be an issue.

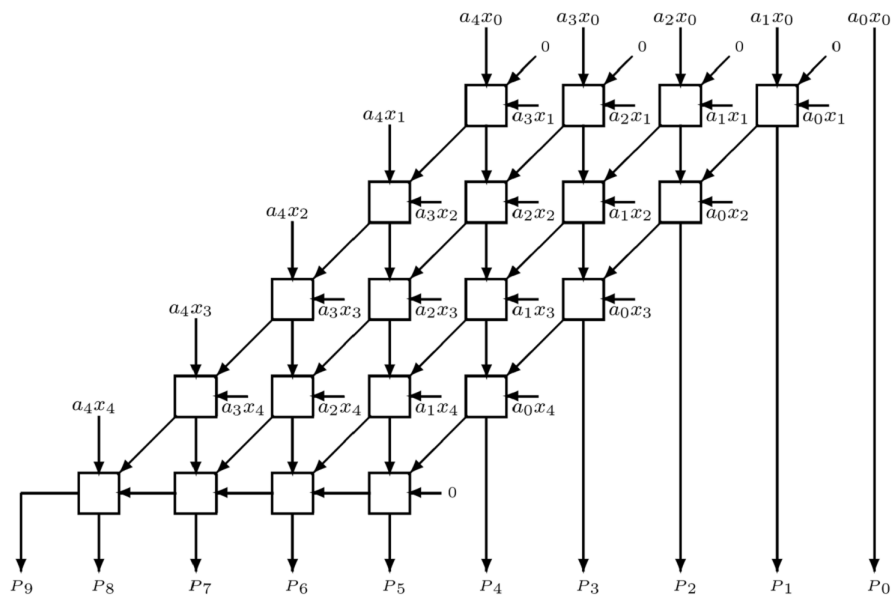

Figure 16: Representative schematic of the array multiplier. Source [7].

Multiplication Circuit

Figure 16 is a representative image of the array multiplier used in the data path architecture. All partial products are achieved with logical AND gates. All addition units are full adders. Each level of addition uses the ripple carry design principle. Since speed is not paramount, the delay should not be an issue.

The widest bit line computations will involve a multiplication between a 16 and 9 bit values. Having a square array multiplier (like in figure 16) would introduce unnecessary hardware. A rectangular version of the multiplier in figure 16 is used. The unit will have sufficient hardware to execute a 9 by 17 bit multiply. The extra bit was needed to ensure correct operation.

Simulation Results with Conclusion

The multiplication circuit was implemented using the Verilog hardware description language. The proposed architecture was subjected to exhaustive testing at the behavioral and post place and route levels.

Figure 19 presents an illustrative snapshot of the array multiplier verification testing at the post place and route level. A clear observation is the notable delay to respond to the change in test stimulus. This source of the delay is in the fact that the correct solution must work its way through several levels of ripple carry addition units. The test stimuli were programmed to change every $100ns$. It takes roughly a fifth of the time ($\approx 20ns$) for the correct output to appear (see figure 19). As Stargrazer One is to be clocked at speeds under 10 MHZ, the array multiplier will have sufficient time to present correct results despite the propagation delay. Despite this delay, the proposed architecture successfully obtains correct responses in the test.

Additional testing yielded similar results.

Subtraction Circuit

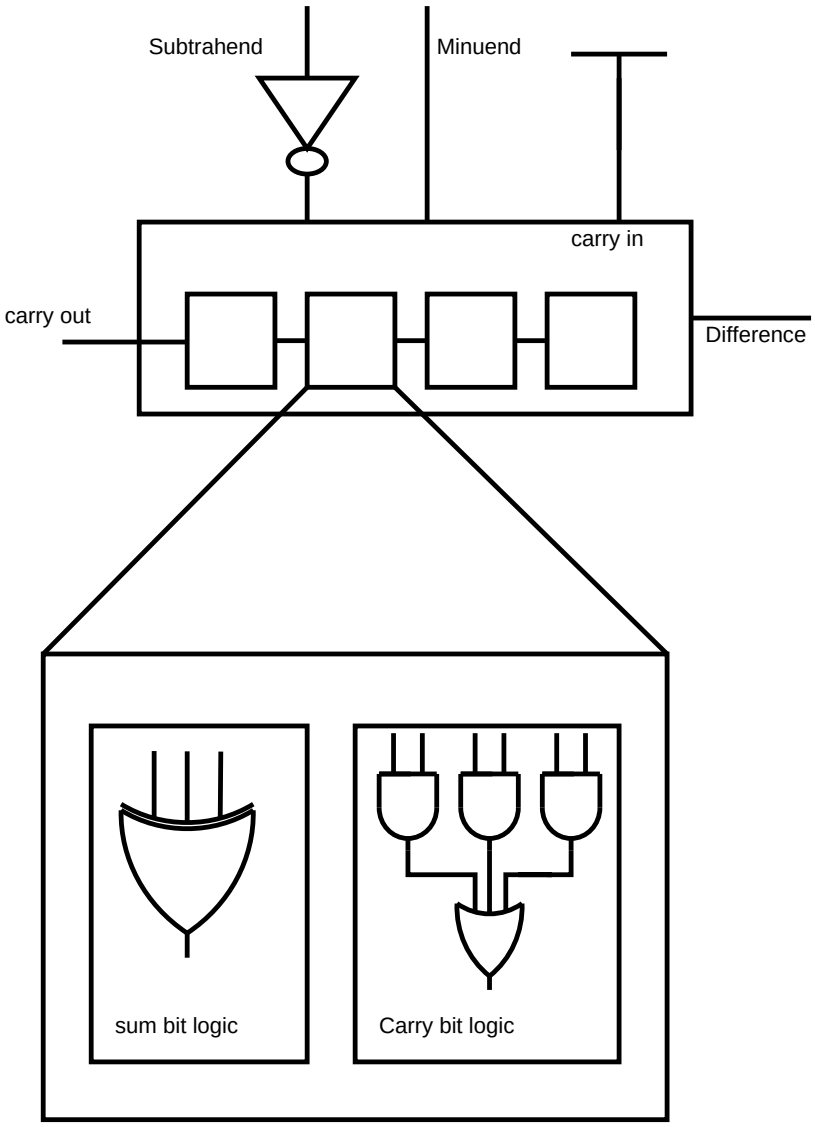

Figure 17: Module level view of the subtraction unit, with the gate level description of the individual bit full adders used. Subtraction is achieved by converting one of the operands into its 2's complement inverse.

Figure 17 presents the gate level implementation of the one bit subtraction circuits used. Figure 17includes a schematic view of the entire functional unit as well.

The subtraction circuitry is a chain of binary one bit adders. The unit is designed to perform 2's complement subtraction. The input corresponding to the lowest voltage capacitor C1 assumes is negated. The maximum voltage value is left positive. Under normal conditions, neither value will be negative. Also, the result from the unit will be greater then or equal to zero. This removes the need for overflow inspection.

Simulation Results with Conclusion

It was possible to exhaustively test this circuit. This circuit was implemented in the Verilog hardware description language and tested at the behavioral and post place and route levels. The size of the unit tested is sixteen bits.

Figure 20 presents a representative segment of the test results. The "subtrahend" and "minuend" signals are the input into the system. The signal named "actualout" is the difference produced by the proposed circuit. The signal "expectedout" is produced by a theoretically correct implementation in the test bench. The signal labeled "error" presents the discrepancy, if any, between the "expected" and "actual" results. This signal remains at binary zero. The brief pulses seen at each change of input value are due to gate delays. This suggests correct operation. Further testing yielded similar results.

Remaining Elements

The functional blocks presented were composed from simpler blocks. Due to the rudimentary nature of these pieces, they will not be separately discussed. For state devices such as registers, Stargrazer One uses D flip flops exclusively. Additional elements such as multiplexers were created using appropriate combinational logic. These pieces once designed, were implemented using the Verilog hardware description language. The circuits were then exhaustively tested at the behavioral and post place and route levels. The designs for these basic functional blocks were verified for correctness before being used.

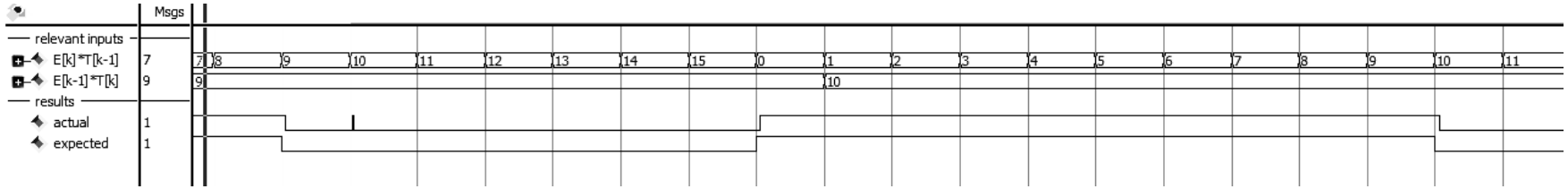

Figure 18: An illustrative sample of the testing performed on the comparison unit. The spikes seen in the architecture output (labeled "actual") are due to propagation delays.

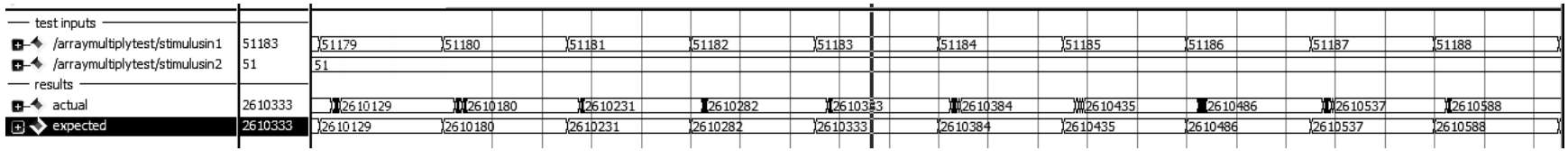

Figure 19: An illustrative example trace taken at the post place and route level of the multiplier. The signal labeled "actual" is the result from the architecture and the signal labeled "expected" is the theoretically correct reference from the test bench. Note the propagation delays of the architecture.

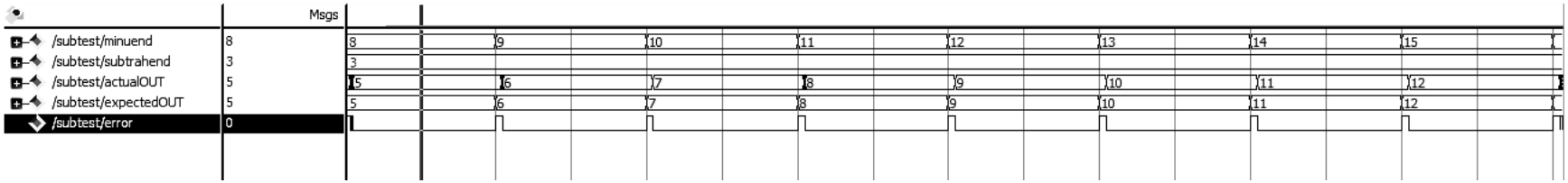

Figure 20: An illustrative portion of the subtractor validation trace taken at the post place and route level.

Discussion of Relevant Functional Blocks Used to Construct the Output Circuit

Each component used to create the output circuit was subjected to be same testing procedure as the whole system. This appendix will discuss the larger functional blocks developed. Each of the functional units will be reported as follows. The discussion will open with a description of the architecture then the functional performance will be reported.

Counter One

Both counting circuits consist of a register of D flip flops with an increment circuit. The Counter One increment circuit is capable of incrementing by positive or negative one. Additional logic is included to avoid wraparound by checking for all zeros or all ones in the output. The result of this check, with the count direction signal, serve as inputs to a clock gate between Counter One's clock port and the system clock. When these signals are active the clock is disabled freezing the counter. When the entire Stargrazer One system is first activated, Counter One is set to an initial value. The register is designed to start at an intermediate value. The value stored in the register will be updated according to the results of the evaluation of $P[k-1] \leq P[k]$. Based on the results, the counter will change the output value by ± 1. For every power comparison, the value inside the register of Counter One will change.

This circuit was defined in the Verilog hardware description language and tested in the Xilinx ISE design environment. Testing was done at the behavioral and post place and rout levels. To assist in validation, a functionally correct counter is implemented in the test bench file used to test the architecture. Its output is compared to the actual device. For ease of testing the bit length of the counter was set to four bits. Since a structural and generic coding style was used, the unit can be expanded by merely changing the generic variable. The counter was found to perform as expected. The unit counts down and counts up as expected. The counter architecture did not wraparound.

Counter Two

The function of Counter Two is similar to the saw tooth wave generator used in some PWM circuits. It is built similarly to Counter One. The increment circuit is only able to increment by positive one. The counter can be cleared. Counter Two along with the comparison circuit (discussed in section **??**), determine how long transistor T1 should remain active.

This circuit was defined in the Verilog hardware description language and tested in the Xilinx ISE design environment. Testing was done at the behavioral and post place and route levels. To assist in validation, a functionally correct counter is implemented in the test bench file used to test the architecture. Its output is compared to the actual device. For convenience the counter is sized to four bits. Since a structural and generic coding style was used, the unit can be expanded by merely changing the

generic variable. This counter will need to be able to tolerate being repeatedly set to zero while counting. The testing file subjects the counter to such situations. The proposed architecture was found to perform as expected.

Finite State Machine

The chosen way to generate the transistor switching waveforms is with a special finite state machine. Figure 21 and table 5 presents the state transition and output diagrams for this machine:

Table 5: Outputs for the finite state machine. "T1" and "T2" are the gate signals for transistors T1 and T2 respectively. "flag1" and "flag2" are notices sent to the control circuit. These tell when to execute voltage sampling on capacitor C1. "clear" sets Counter Two to zero.

finite state machine outputs

state	T1	T2	flag1	flag2	clear
A	1	0	0	0	0
B	1	0	1	0	0
C	0	0	0	0	0
D	0	1	0	0	0
E	0	1	0	1	1
F	0	0	0	0	1

To implement the state machine, a "one hot encoding" scheme is used. The inconvenience of a larger state register is offset by simple implementation of the state transition and output logic. Almost all outputs are simply tied to the appropriate Q output from the state register. The signals that communicate with the control circuitry are delayed by half a clock cycle. This is accomplished by running these signals thorough a falling edge triggered register. The purpose of this is to minimize the possibility of timing errors.

The input for state A insures that transistor T1 sees the desired on signal length. Since the other states can be operated for fixed durations, the state machine automatically generates these signals once transistor T1 can be turned off. The state machine is charged with other important tasks. The machine clears Counter Two so that it starts from zero when transistor T1 is to be turned on. The machine also generates signals which let the control circuit know that it is time to sample the voltage on capacitor C1.

Simulation Results With Conclusions

The finite state machine was implemented in the Verilog hardware description language and subjected to testing at the behavioral and post place and route levels. To assist in validation of the architecture, a test bench containing a functionally correct model of the state machine was developed. This along with the proposed architecture was subjected to appriopiate stimulus.

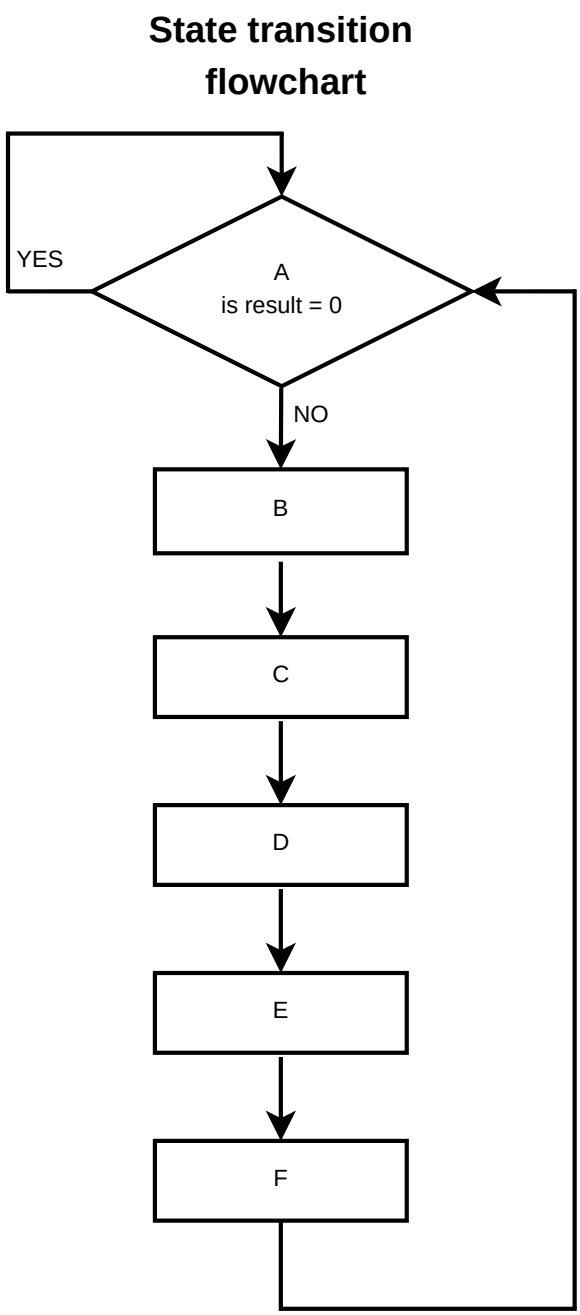

Figure 21: State transition flow chart of the output circuit finite state machine.

Figure 22 presents an illustrative sample of the validation simulation for this finite state machine. The testing is done at the post place and route level. For each state machine output the theoretically correct output (named "expected" in figure 22) and proposed architecture output (named "actual" in figure 22) results are presented. For each output the signals were compared (labeled "error" in figure 22). A value fo zero indicates a match. Notice that for all output signals, the discrepancy signal remain binary zero. This suggests correct operation.

Figure 23 presents further support by presenting all "error" signals for an entire

simulation run. Note that they remain binary zero indicating proper operation. The brief spikes were determined to be from propagation delays in the proposed architecture.

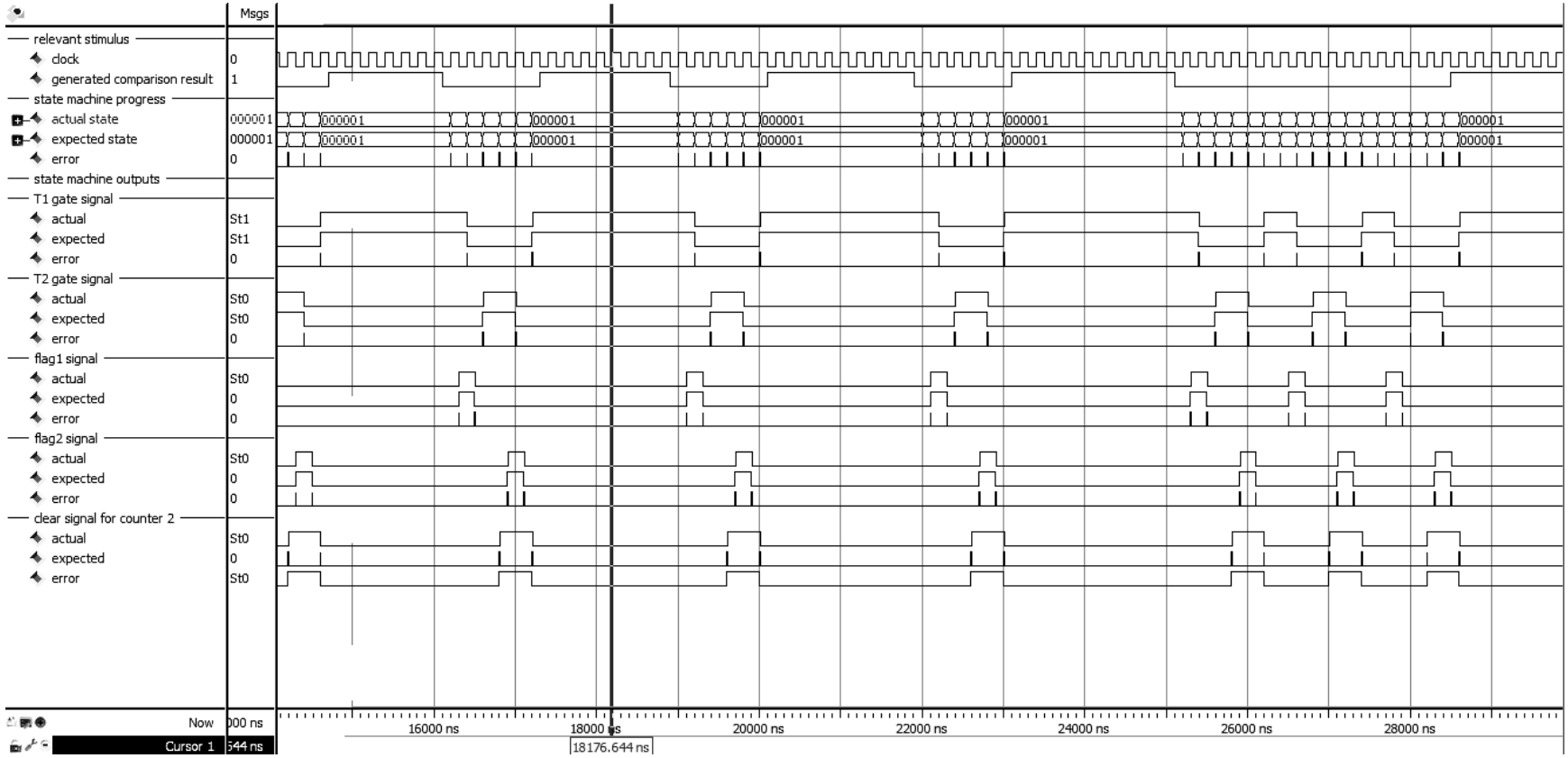

Figure 22: An illustrative view of the post place and route validation of the finite state machine. All outputs are included in this validation. For each output, signals labeled "expected" come from the proposed architecture, "actual" come from the proposed architecture and "discrepancy" compares the two.

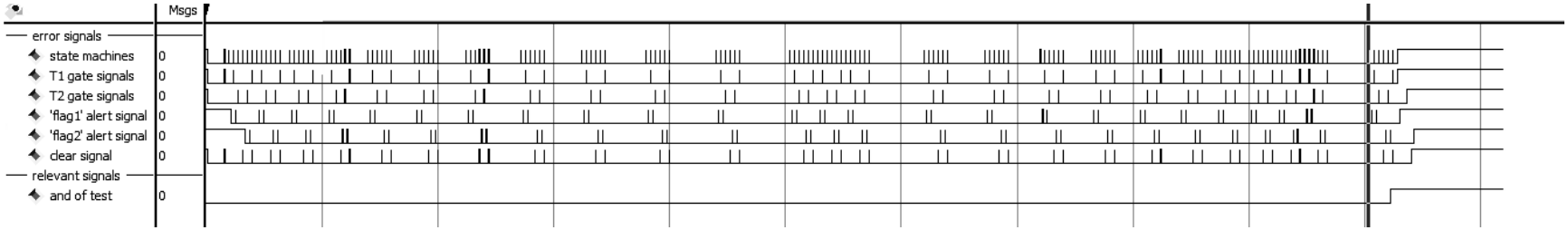

Figure 23: All error signals for an entire validation test run. The simulation was taken at the post place and route level.

Appendices for Part IV

Solar Cell Circuit Model Used for the Validation In Chapter 15

Introduction

To simplify analysis and maintain focus on the maximum power point tracking system, equation 17 was used to define a solar cell source.

$$I(t) = Isc - Io * \left(e^{\left(\frac{V(t)}{Vth}\right)} - 1\right) \tag{17}$$

Where Isc is the short circuit current, Io is the reverse bias current and Vth is the thermal voltage.

In the computer studies done in this thesis, it was possible to use equation 17 directly in scripts. For the testing done in this part, it was necessary to translate equation 17 into a physical circuit. The purpose of this appendix is to present how this basic circuit is implemented in the testbed for Stargrazer One. The appendix will open by discussing the architecture then will present the voltage current and voltage power characteristic of the developed circuit.

Architecture

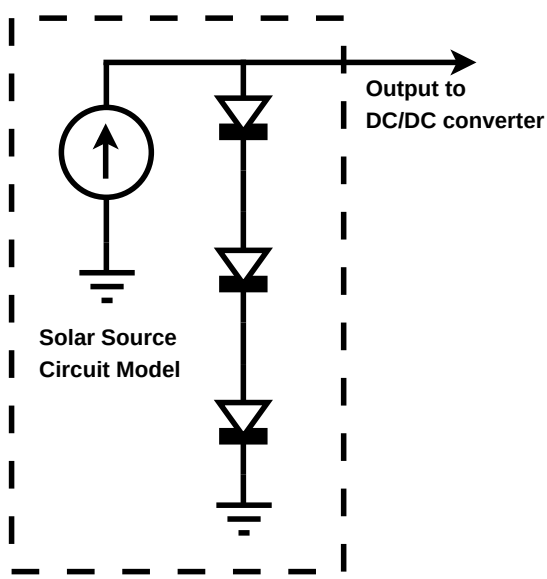

Figure 24: Circuit model for a photovoltaic source to be used in the hardware prototype of Stargrazer One. The diodes in cascade imitate the effect of placing solar cells in series.

Figure 24 shows the entire schematic for the solar cell source. Note the use of a cascaded string of diodes. The purpose for this design choice is to ensure that a

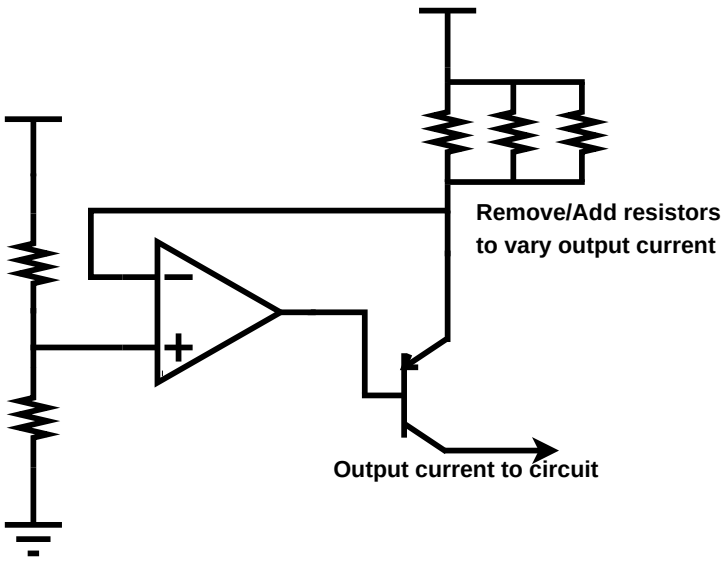

Figure 25: Schematic view of the current source that is used in figure 24.

majority of the possible operating voltages assumed by the circuit remain within the acceptable input range of the analog to digital converter of the Spartan 3AN field programmable gate array development board. This board will be used for a physical implementation of the Stargrazer One architecture. The analog to digital converter is range limited. It can only process inputs between 0.4 and 2.9 volts [8].

Figure 25 presents the circuit used to produce the current source. The current value is set by the parallel resistor network between the PNP bipolar junction transistor (BJT) and the positive power supply rail (see figure 25). Simulating variations in solar radiation is achieved by removing or adding parallel resistors to this network.

The purpose of the operational amplifier seen in figure 25 is to ensure that a constant current is produced. The property of operational amplifiers where the voltage on both input ports are nearly equal is exploited to fix the voltage drop across the parallel resistors. The voltage to be imposed is presented by the voltage divider acting on the positive input of the amplifier. The negative amplifier input is connected between the parallel resistor network and the emitter of the bipolar junction transistor. The output current from the amplifier into the base of the BJT will adjust to satisfy the requirement that the amplifier input voltages be equal.

A PNP BJT is chosen as it will remain in the "forward active" region during normal operation of this circuit. The transistor interfaces between the parallel resistor network and the circuit's output.

Characterization of the Solar Source Circuit Model

This proposed circuit was implemented in a Digilent Analog Explorer solder-less circuit board for testing. Current vs. voltage and power vs. voltage relationships were determined experimentally for the developed circuit. Figure 26 presents a diagram showing the experimental setup. The following sections will presents the procedure and results.

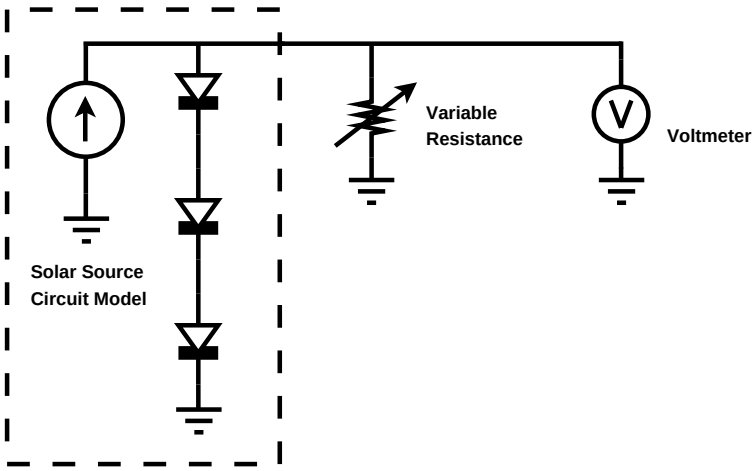

Figure 26: Experimental setup. Please refer to table 6 for actual devices used in the experiment.

Procedure

The procedure used to determine the voltage current and voltage power relationships is now presented:

- Measure the voltage observed between the diode chain and the collector of the bipolar junction transistor. This value will give the open circuit voltage.
- Set a resistance between the collector of the bipolar junction transistor and ground. Make sure the resistors used are rated to sink the power that will be presented from the current source.
- Using a volt meter, record the observed voltage value.
- Compute the current using Ohm's law. For completeness, the equation used is $I = \frac{V}{R}$.
- Compute the power using Watt's law. For completeness, the equation used is $P = I * V$.
- Adjust the resistance and repeat this procedure. Once the observed current flowing through the resistor falls below a certain minimum value threshold cease experimentation.
- Repeat this experiment for each short circuit current value to be used.

Results With Conclusions

All devices used in the experimental circuit are listed in table 6. Figures 27, 28 and 29 show the observed current voltage relationship for each of three short circuit current values. Figures 30, 31 and 32 present the power vs voltage relationships. Using the experimental data, it is possible to estimate the voltage of the maximum power point.

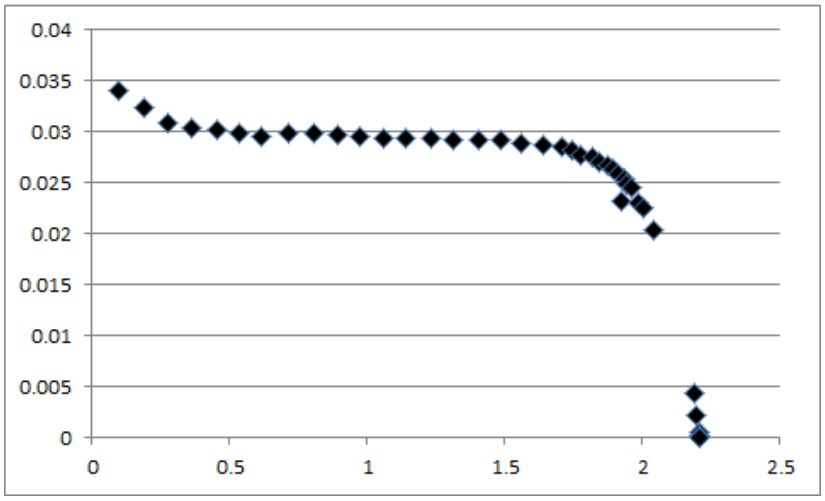

Figure 27: Observed current vs voltage relationship. In this case the observed short circuit current was equal to $34mA$. This current value is achieved by having one 51Ω resistor between the positive power supply and the emitter of the bipolar junction transistor. The vertical axis is current in A and the horizontal axis is voltage in V.

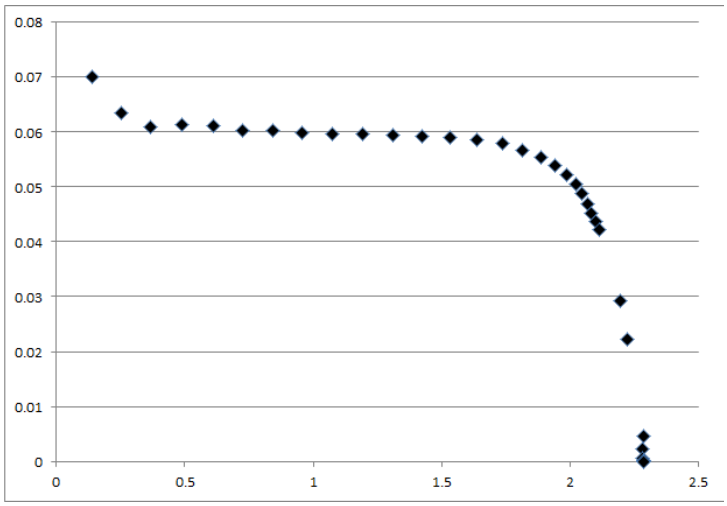

Figure 28: Observed current vs voltage relationship. In this case the observed short circuit current was equal to $70mA$. This current value is achieved by having two 51Ω resistors in parallel between the positive power supply and the emitter of the bipolar junction transistor. The vertical axis is current in A and the horizontal axis is voltage in V.

The estimated maximum power voltage for the 3 current values tested are presented in table 7.

In figures 27, 28 and 29, the curves traced resemble the voltage current characteristic seen from solar photovoltaic cells. This suggests that the implementation described in this appendix acceptably emulates a solar cell source.

Figures 30, 31 and 32 show power curves which resemble the characteristic seen

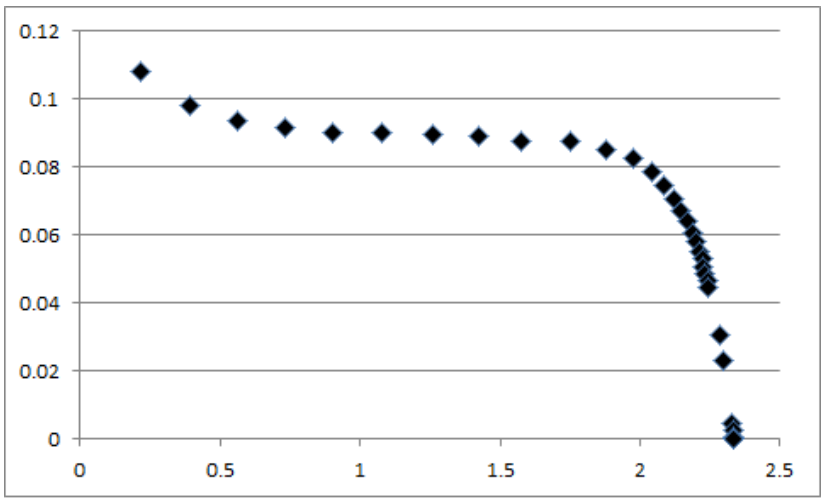

Figure 29: Observed current vs voltage relationship. In this case the observed short circuit current was equal to $108mA$. This current value is achieved by having three 51Ω resistors in parallel between the positive power supply and the emitter of the bipolar junction transistor. The vertical axis is current in A and the horizontal axis is voltage in V.

Table 6: Nominal device values and/or part names used in the implementation of the current source and the validation experiment defined in this appendix. Resistances assumed by the RS 200 unit are enumerated in table 8.

Devices used in Current Source

Type	part number	amount used
Diode	1n4001	3
OpAmp	uA741	1
BJT [PNP]	TIP32	1
Resistor	51 Ω	3
Resistor	20 $k\Omega$	1
Resistor	5.1 $k\Omega$	2

Testing devices

Type	part	amount used
Variable resistance	RS 200	1
volt meter		1

for a solar source for each simulated illumination. Figures 30, 31 and 32 show a characteristic which increases from zero Watts to a particular value. Then the observed power drops off to zero. Just like a solar photovoltaic source, this circuit produces a power characteristic which features a maximum power point.

Table 7: Estimated maximum power voltages for each short circuit current value of the solar source circuit model.

Estimated Maximum Power Voltages V_{MMP}	
I_{short}	V_{MMP}
$108mA$	$1.978V$
$70mA$	$1.942V$
$34mA$	$1.874V$

Closing Remarks

In this section, a circuit based model for a solar cell is developed and experimentally validated. The experimental results showed a behavior sufficiently close to that of a real solar source to permit use of this model. The current voltage relationship and the power voltage relationship was studied. Both relationships emulate those of a solar source further confirming the validity of this circuit model for a solar photovoltaic unit.

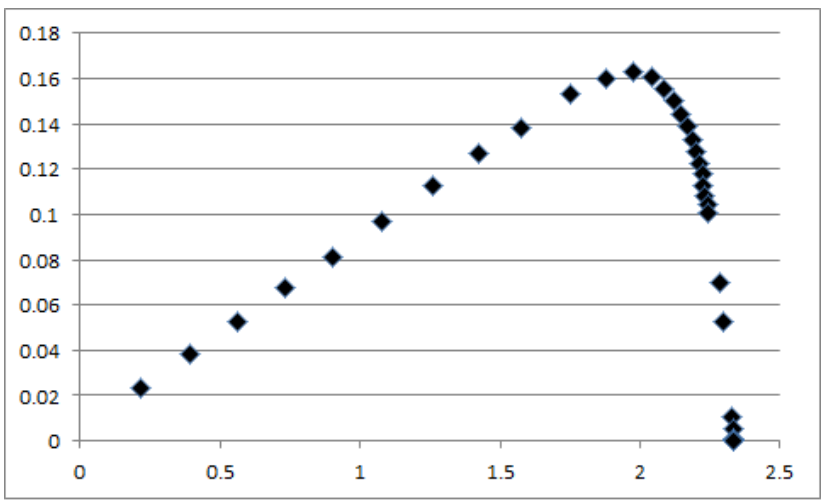

Figure 30: Power vs. voltage for the case of short circuit current equal to $108mA$. This current value is achieved by having three 51Ω resistors in parallel between the positive power supply and the emitter of the bipolar junction transistor. The vertical axis is power in W and the horizontal axis is voltage in V.

Table 8: Resistor values used for the characterization of the solar source model in appendix 15.3.

Resistor values	
3	Ω
6	Ω
9	Ω
12	Ω
15	Ω
18	Ω
21	Ω
24	Ω
27	Ω
30	Ω
33	Ω
36	Ω
39	Ω
42	Ω
45	Ω
48	Ω
51	Ω
54	Ω
57	Ω
60	Ω
62	Ω
64	Ω
66	Ω
68	Ω
70	Ω
72	Ω
74	Ω
76	Ω
78	Ω
80	Ω
83	Ω
86	Ω
89	Ω
100	Ω
500	Ω
1	$k\Omega$
5	$k\Omega$
10	$k\Omega$
50	$k\Omega$
100	$k\Omega$
∞	

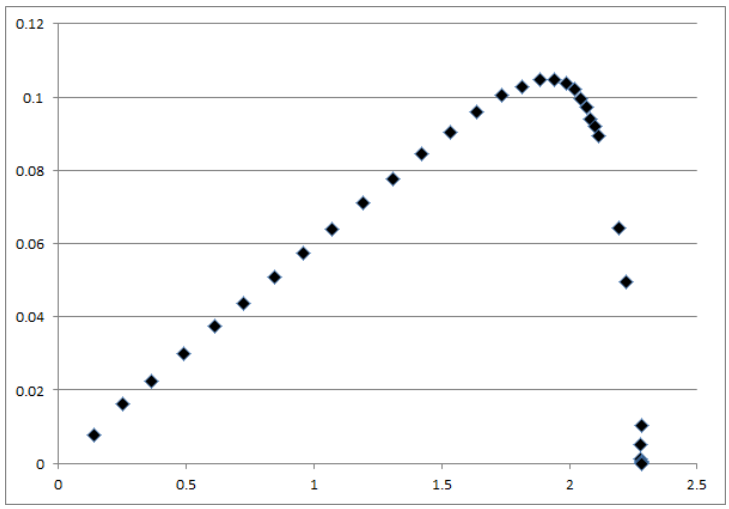

Figure 31: Power vs. voltage for the case of short circuit current equal to $70mA$. This current value is achieved by having two 51Ω resistors in parallel between the positive power supply and the emitter of the bipolar junction transistor. The vertical axis is power in W and the horizontal axis is voltage in V.

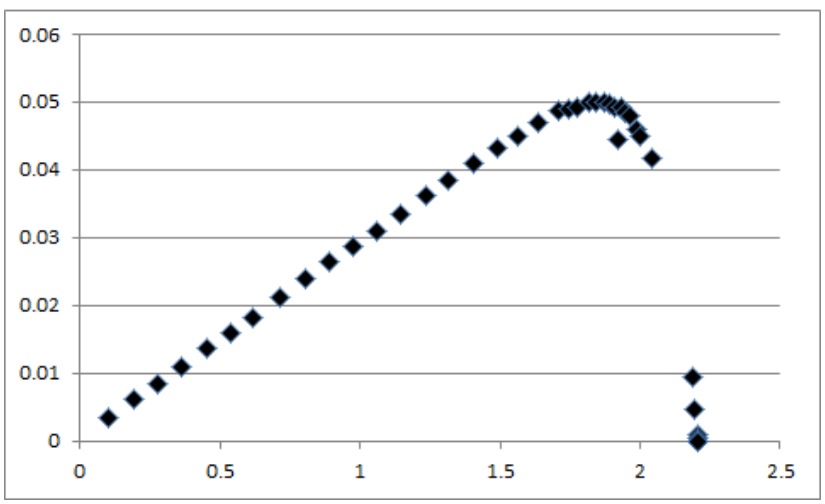

Figure 32: Power vs. voltage for the case of short circuit current equal to $34mA$. This current value is achieved by placing a single 51Ω resistor between the positive power supply and the emitter of the bipolar junction transistor. The vertical axis is power in W and the horizontal axis is voltage in V.

Determination of the Expected State One Durations Used In Chapter 15

Introduction

In section 15.1, Stargrazer One's performance was validated by comparing to known State One durations corresponding to maximum power point operation. The purpose of this appendix is to present the methodology used to determine these values. The appendix will open by describing the experimental setup and procedure. Finally

results will be presented and conclusions will be drawn.

Experimental Setup

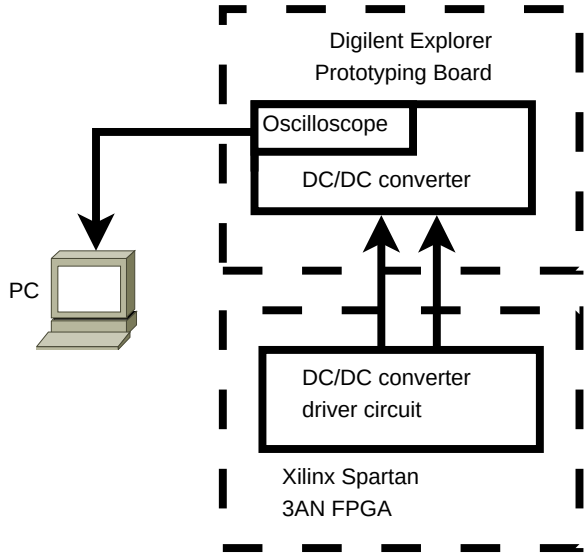

Figure 33: Block diagram view of circuitry implemented in the Spartan 3AN field programmable gate array for this experiment.

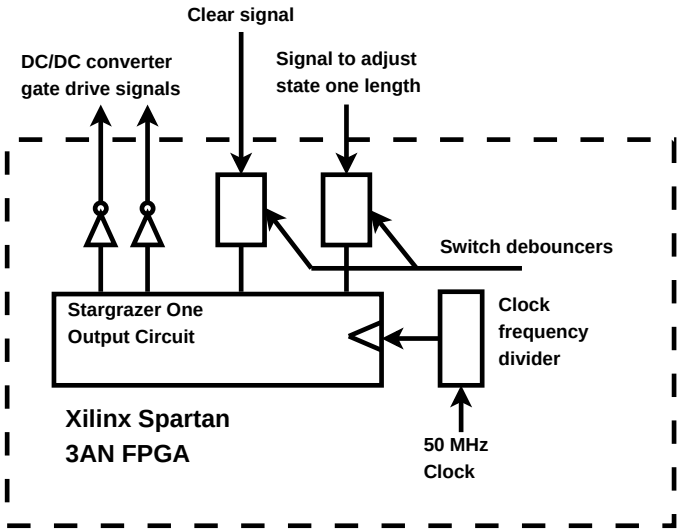

Figure 34: Diagram presenting the experimental setup used.

Figure 33 presents a schematic of the experimental setup. The Spartan 3AN FPGA contains a circuit which presents a switching pattern equivalent to the one presented by Stargarzer One to the power electronic circuits. The detailed schematic of this circuit is presented in figure 34. The circuit is designed so that the duration of State One can be controlled manually. The FPGA gate drive signals interact with

an instance of the power electronic circuit on a Digilent Analog Explorer Board. The circuit itself is implemented using discrete circuit elements. The Explorer Board has built in power supply and oscilloscope features. These will be used for power and to collect data.

As stated before, figure 34 presents a schematic block diagram for the circuit implemented in the Spartan 3AN FPGA. In the FPGA, the core circuit is the output circuit developed for Stargrazer One with minor adjustments. Details of the schematic of the Stargrazer One output circuit is available in section 13.3 of chapter 13. As shown in figure 34 the circuits can be cleared and adjusted by hand.

When the step down switched capacitor converter is interacting with the solar source a range of voltage values is traversed as capacitor C1 charges. Stargrazer One computes the average energy entering the converter by computing the maximum and minimum voltage on capacitor C1. Therefore in effect Stargrazer One is trying to determine the maximum average power as it adjusts.

As the duration of State One varies, the observed voltage range covered and the total time of a converter cycle changes. Power is computed as the ratio of energy and time. A solar cell source has a fixed voltage range. This means that a finite amount of energy can be delivered from the solar cell source to capacitor C1 for any State One duration. This suggests that there will be an optimal duration of State One that presents the highest average power to the load.

This experiment will determine what this optimal duration is and verify that the maximum power point is included in the observed voltage range. The developed circuit model for the solar source is set to present three possible short circuit current values. This experiment will be conducted for each value.

Procedure

The procedure to be used is as follows

- Prepare oscilloscope probes and initialize the circuit in the Spartan 3AN FPGA. The probe for the oscilloscope is to be placed on the high potential node of capacitor C1 and ground.
- Enable all circuits and record the highest and lowest observed voltage for capacitor C1.
- Adjust the length of State One to the next desired point of study and repeat the previous list point
- Once all State One lengths to be studied have been examined, compute the average powers by applying the equation:

$$P = \frac{\Delta E}{\Delta t} \tag{18}$$

- Determine the State One length which gives the highest average power value (Should Stargrazer One be functioning properly, the system will operate at or very near this point).

- Repeat this procedure to obtain a more robust result. For the execution presented in this appendix, this procedure will be repeated five times for each short circuit current value.
- Repeat this procedure for each short circuit current (I_{short}) from the solar cell source that will be encountered in testing.

Results with Conclusions

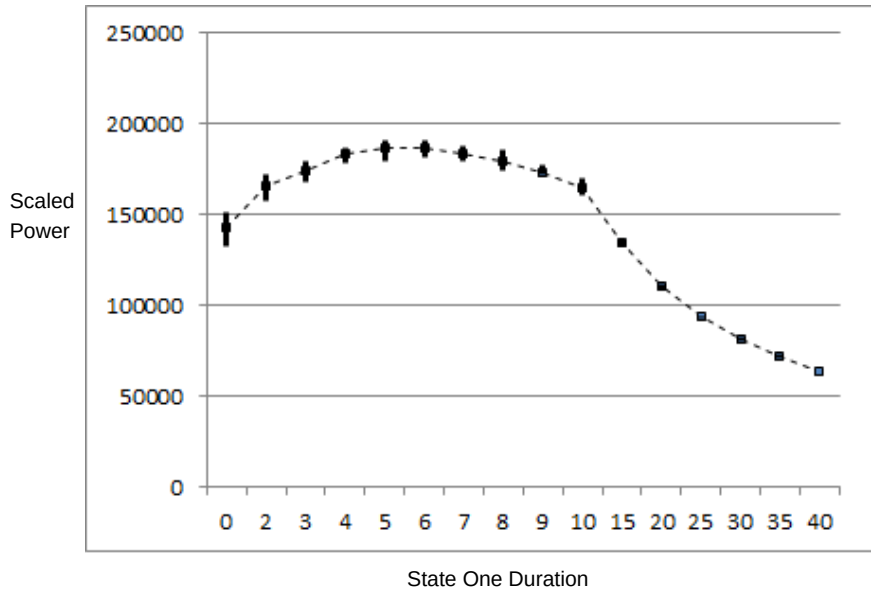

Figure 35: Results from five iterations of the procedure outlined in the section 15.3 for $I_{short} \approx 108$ mA. The horizontal axis is the length of State One in clock cycles. The vertical axis presents the computed values for power.

Figures 35, 36 and 37 presents results from on execution of the experimental procedure outlined in section 15.3. Each of the figures presented show that a particular value or values of State One will yield maximum power. For the purpose of this analysis, the average values for the experimental data will be used. The average values were used to generate the line connecting each vertical segment observed in each figure. The vertical segments themselves present the variation in collected data values for the five total experimental runs. The segments span from the smallest to the largest observed data value. As evidenced in the figures, certain data points show greater variance than others. A keen observer will note that in all figures the spacing between values in the horizontal axis (corresponding to State One durations) is not constant. This was done deliberately. Near where the maximum power point value is located the resolution is fine so that a precise determination of the State One value corresponding to maximum power point operation can be determined. For State One values located further away, the spacing is increased. This was done to convince the reader that the global maximum was captured in the figures. A table presenting the averaged powers computed for all State One durations tested is presented in table 10.

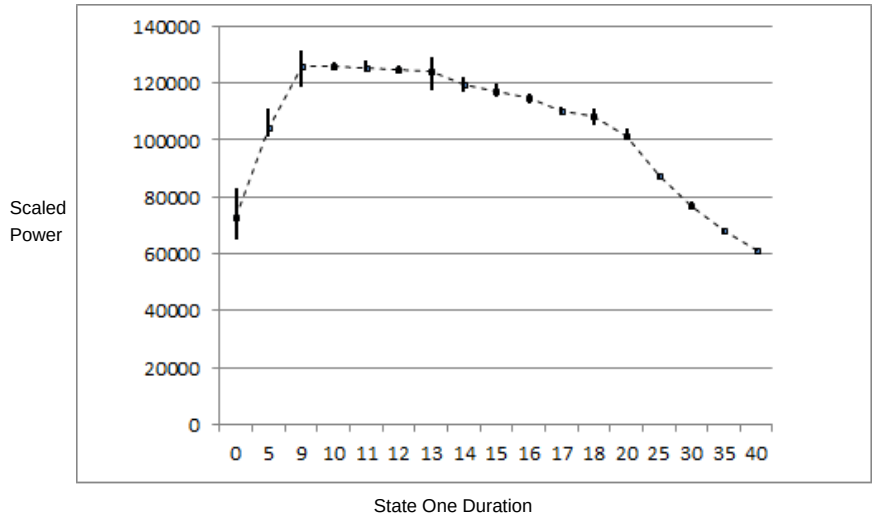

Figure 36: Results from five iterations of the procedure outlined in the section 15.3 for $I_{short} \approx 70$ mA. The horizontal axis is the length of State One in clock cycles. The vertical axis presents the computed values for power.

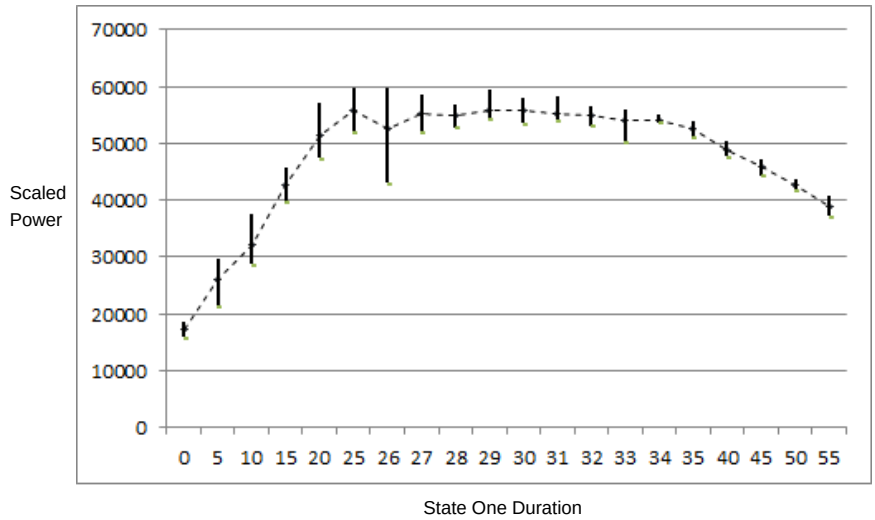

Figure 37: Results from five iterations of the procedure outlined in the section 15.3 for $I_{short} \approx 34$ mA. The horizontal axis is the length of State One in clock cycles. The vertical axis presents the computed values for power.

Examining the location of the average value for each State One value, it was possible to determine what State One duration Stargrazer One should assume. The State One value corresponding to the maximum power point is presented in table 9. Because of the relatively flat nature of the power curves presented in figures 36 and 37, it is very likely that Stargrazer One may end up operating within a range of values for State One adjacent to be presented values in table 9. Considering the variation in measured data observed in executing this test, such an outcome would come as no surprise. As presented in figure 36 and 37, there appears to be a plateau around the

reported state one value corresponding to maximum power point operation. Should Stargrazer One be operating within this plateau, it will be safe to assert that the system is operating correctly.

Table 9: Observed State One duration values which correspond to operating at the maximum power point. State one duration values are reported in clock cycles. The numbers mean that the system must remain in State One for the listed multiple of Stargrazer One system clock period to operate at the maximum power point.

	State One Length Values		
I_{short}	≈ 108 mA	≈ 70 mA	≈ 34 mA
Time (in T_{CLK})	5	10	30

Final Comments

This appendix presents how the references used to determine if Stargrazer One is functioning correctly were determined. Using the procedure outlined and the experimental setup discussed, the power vs State One curves were defined for each of three short circuit current values. Using these, it was possible to define the state one value corresponding to maximum power point operation for each short circuit current tested. These values now present a reference to measure the observed performance of Stargrazer One. Should Stargrazer One seek and maintain values of State One that include or are adjacent to the values reported in table 9, it will be safe to assert that the system is seeking the maximum power. =

Table 10: Average power values computed for all State One durations tested (denoted as T_{conv}). Reported values in Watts. The notably large values are a result of dividing the observed energy transfer on capacitor C1 by the duration of a converter cycle. The time duration of a converter cycle ranges from several microseconds to under a millisecond.

Computed Average Powers [in W] For All Three Short Circuit Current Values					
T_{conv}	$I_{short} \approx 108$ mA	T_{conv}	$I_{short} \approx 70$ mA	T_{conv}	$I_{short} \approx 34$ mA
0	142999.5703	0	72674.53125	0	17105.85938
2	166114.5833	5	104614.0799	5	25867.84722
3	174087.5893	9	125809.6635	10	32126.88616
4	183292.7148	10	125815.2567	15	42538.48684
5	186336.3368	11	125418.7917	20	51329.58333
6	186284.3906	12	124946.6016	25	55682.88254
7	183663.9773	13	124133.8327	26	52594.22917
8	179230.0911	14	119826.1198	27	55059.80343
9	173526.6827	15	117039.7368	28	54790.40527
10	165196.3393	16	115008.3047	29	55857.89299
15	135000.1316	17	110388.3929	30	55927.97794
20	110198.1771	18	108586.6548	31	55244.94196
25	93555.25862	20	101400.1367	32	54830.85069
30	81603.92004	25	87436.875	33	53971.43159
35	71866.02163	30	76756.18107	34	54175.60033
40	63736.88565	35	68085.67308	35	52482.28766
0	0	40	61176.7223	40	48892.06676
0	0	0	0	45	45735.58673
0	0	0	0	50	42637.66493
0	0	0	0	55	38883.89831

Discussion of Additional Circuits Designed To Interact With the Spartan 3AN Development Board's On Board Analog to Digital Converter

Introduction

As discussed in section 15.1, the Stargrazer One system is to be validated using a Xilinx Spartan 3AN field programmable gate array (FPGA) prototyping board. This testing platform was selected for many reasons. Most relevant for this discussion is the presence of an analog to digital converter.

In order to take advantage of this hardware, it was necessary to design additional circuitry inside the field programmable gate array to properly interface with the conversion hardware. The purpose of this appendix is to present the additional circuits developed for testing Stargrazer One in the Spartan 3AN FPGA. Discussion will cover the interface circuitry for the analog to digital converter. In the Spartan 3AN FPGA testing platform, the analog to digital converter (ADC unit) has two distinct pieces. The conversion hardware has a preamplifier module as well as a converter. Each of

these modules require an individual interface. The Spartan 3AN test platform uses a LTC6912 unit for the amplifier and the ADC unit is a LTC1407 unit [8]. As each device requires its own interface, they will be discussed separately.

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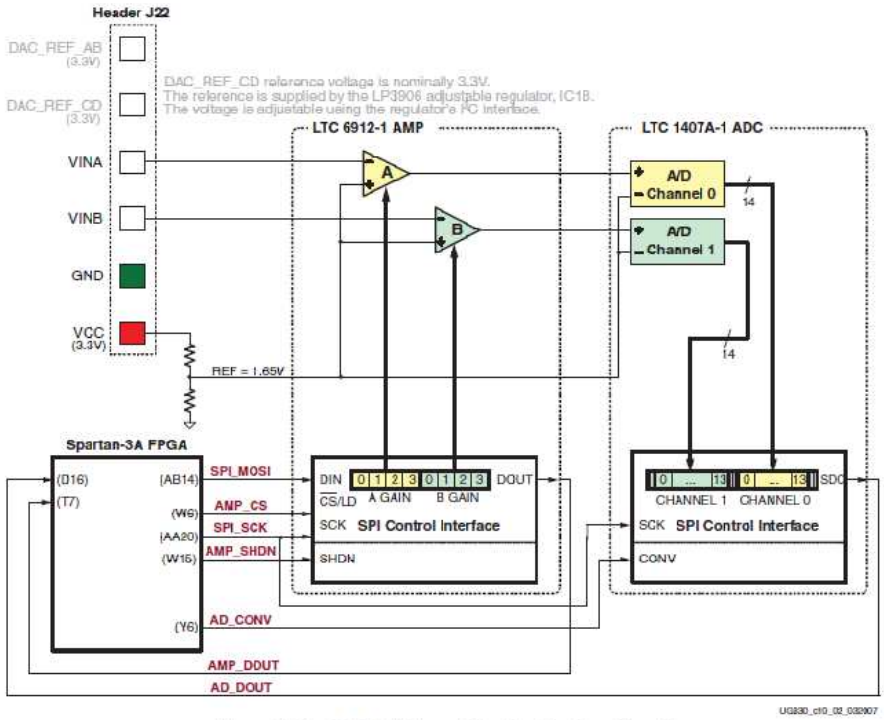


Figure 38: Complete schematic view of the analog capture circuit used in the Spartan 3AN test board. Source: [8].

Figure 38 visually presents the analog conversion system in the Spartan 3AN test platform. Each developed interfacing circuit will be covered individually. For each section, discussion will begin with an examination of the architecture then, where appropriate, proceed to discuss validation results.

LTC6912 Dual Programmable Gain Amplifiers with Serial Digital Interface

There are two amplifiers inside this unit. Only one amplifier is required to successfully convert an analog signal as presented in figure 38. Before this amplifier can be used, the gain must be set [8]. For this particular amplifier, the gain is programmed by providing a four bit serial input into the appropriate port [8]. There are several possible gain options each tied to a particular four digit binary number [8]. The table of possible choices is presented in figure 39.

For Stargrazer One, it made the most sense to use the -1 gain setting. This gain has the largest possible voltage swing for the input voltage. This will permit the largest amount of flexibility in the validation of Stargrazer One. For example, a large

Table 10-2: **Programmable Gain Settings for Pre-Amplifier**

Gain	A3	A2	A1	A0	Input Voltage Range	
	B3	B2	B1	B0	Minimum	Maximum
0	0	0	0	0		
-1	0	0	0	1	0.4	2.9
-2	0	0	1	0	1.025	2.275
-5	0	0	1	1	1.4	1.9
-10	0	1	0	0	1.525	1.775
-20	0	1	0	1	1.5875	1.7125
-50	0	1	1	0	1.625	1.675
-100	0	1	1	1	1.6375	1.6625

Figure 39: Possible gain values for the LTC6912 amplifier with the corresponding digital four bit values. Source: [8].

input swing will permit testing the response of the proposed architecture to different simulated levels of solar radiation. Additionally, the architecture requires the actual voltage values observed on capacitor C1 for computation. Amplification could add unnecessary complexity.

Table 10-1: **AMP Interface Signals**

Signal	FPGA Pin	Direction	Description
SPI_MOSI	AB14	FPGA→AMP	Serial data: Master Output, Slave Input. Presents eight-bit programmable gain settings, as defined in Table 10-2.
AMP_CS	W6	FPGA→AMP	Active-Low chip-select. The amplifier gain is set when the signal returns High.
SPI_SCK	AA20	FPGA→AMP	Clock
AMP_SHDN	W15	FPGA→AMP	Active-High shutdown, reset
AMP_DOUT	T7	FPGA←AMP	Serial data. Echoes previous amplifier gain settings. Can be ignored in most applications.

Figure 40: Interface port listing of the LTC6912 amplifiers. Source: [8].

In order to successfully program the correct gain into the LTC6912 amplifier, appropriate signals must be fed into the unit in a predetermined manner. Furthermore, timing constraints for these signals must be met. Figure 40 presents the signals that must be presented to the amplifier circuit in tabular form. Figure 40 defines the signal as well as explains its purpose. Figure 41 presents the timing constraints that must be followed in delivering the signals. In addition to providing timing information, figure 41 presents the sequence that must be presented to properly program the amplifier circuit.

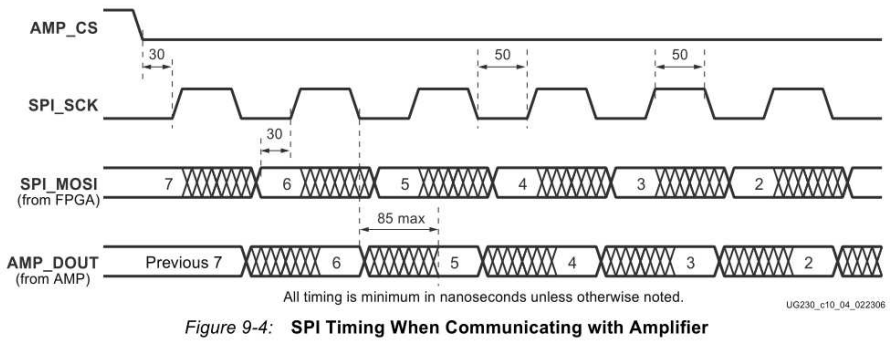


Figure 41: Timing limits for interface signals to the LTC6912 amplifier. The timing constraints are presented in graphical form. Source: [8].

Architecture

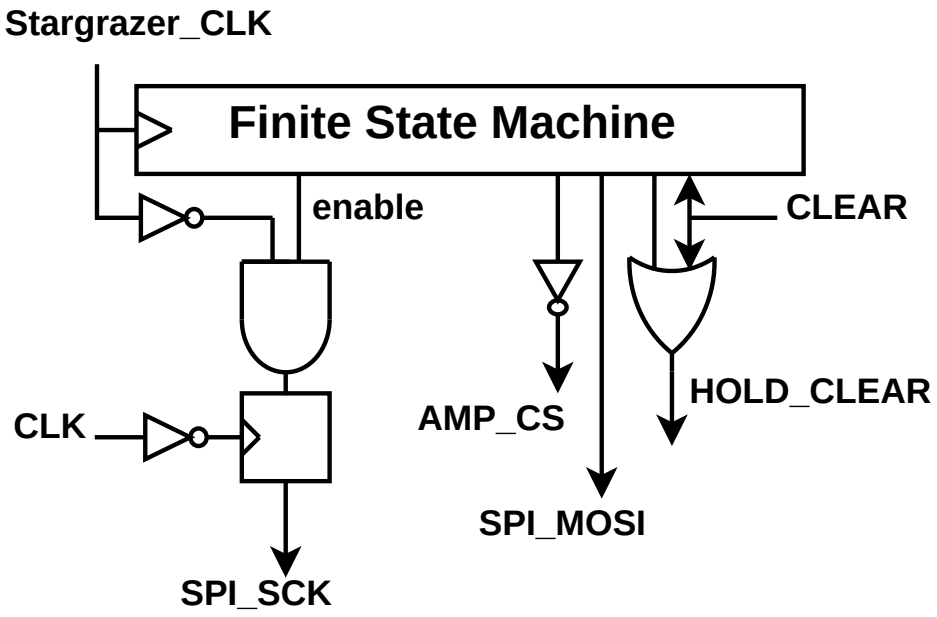


Figure 42: Schematic showing the unit used to program the gain of the LTC6912 amplifier. The signal "Stargrazer_ CLK" is a scaled down clocks signal produced for the Stargrazer One system. The amplifier can only receive information at a speed in the tens of megahertz [8]. It was decided to just use the clock signal that will be used in Stargrazer One. The signal labeled "CLEAR" will be from an external switch. The signal "HOLD_CLEAR" maintains Stargrazer One in a initial state. The signal labeled "CLK" is a 50 MHz onboard FPGA clock.

The chosen solution to generate the required signals shown in figure 40. The major functional block is a finite state machine. Figure 42 shows a diagram of the developed circuit. Figure 50 presents the state transition flowchart and table 11 lists the outputs for this state machine. Note that the state machine remains in the final

Table 11: State machine outputs, "AMP_CS" and "SPI_MOSI" serve the purposes of the "SPI_MOSI" and "AMP_CS" signals defined in figure 40. "HOLD_CLEAR" applies an initialize signal to Stargrazer One, blocking the system from working until the amplifier has been programmed. "enable" activates the "SPI_SCK" signal to program the amplifier.

Output signals from circuit				
state	AMP_CS	enable	SPI_MOSI	HOLD_CLEAR
A	0	0	0	1
B	1	0	0	1
C	1	1	0	1
D	1	1	0	1
E	1	1	0	1
F	1	1	0	1
G	1	1	0	1
H	1	1	0	1
I	1	1	0	1
J	1	1	1	1
K	1	0	0	1
L	0	0	0	0

state. The amplifier only need be programmed once. Note that the state machine is designed to output an additional signal to the entire Stargrazer One system. As shown in figure 42, this signal is needed to maintain a global reset signal while the amplifier is being programmed. When Stargrazer One is first initialized, the first task is to program the LTC6912 amplifier to the appropriate gain setting. The reason for maintaining a global reset (labeled "HOLD_CLEAR" in figures 42 and 50) signal to the rest of the system is to prevent Stargrazer One from operating before the amplifier is ready. Once the amplifier has been properly programmed, the system can begin work.

The state machine is created using the one hot encoding method. The disadvantage of a wider state register is offset by very simple logic for state transition and outputs. As seen in figure 42, the output labeled "SPI_MOSI" directly leaves the finite state machine to the programmable amplifier. The remaining output signals pass through very simple logic before exiting to the amplifier with the exception of the signal labeled "enable". The purpose of this signal is to enable the generation of the "SPI_SCK" signal for the amplifier. The "enable" signal enters into a port of a logical AND gate with the inverted form of the Stargrazer One system clock (labeled "Stargrazer_CLK" in figure 40). The output passes through a falling edge triggered flip flop clocked at 50 megahertz (the on board clock of the Spartan 3AN development board) [8]. The flip flop is falling edge triggered in order to avoid timing issues.

Simulation

A Verilog description of this architecture was created for validation. It was validated using a test bench file under behavioral and post place and route conditions. The purpose of the testing is to validate that the design functions as expected and satisfies the requirements specified in figure 41.

Results and Conclusions

Figure 51 presents a example validation trace (at the behavioral level) of the Verilog description used to implement the architecture described in the previous sections. Relevant input and output signals are presented. As described in the caption, signals labeled "actual" come from the architecture while signals labeled "expected" come from a theoretically correct implementation created in the test bench used to generate the tracing seen in figure 51. The signals labeled "discrepancy" compare signals from the architecture and the theoretically correct implementation during the test. The fact that for each output the corresponding discrepancy signal remains at binary zero suggests that the system is functioning correctly. The proposed architecture was tested at the post place and route level and similar results were obtained. This suggests that the architecture will fulfill its duties properly.

As stated in the previous section and visually presented in figure 41, there are timing constraints that must be obeyed. As the architecture developed in operates at the same clock frequency as Stargrazer One ($781.25kHz$ for the system implemented in this thesis), the transitions are sufficiently slow to mitigate any timing issues. This was found to be the case during validation of the hardware prototype.

LTC1407 Serial 14-Bit 3Msps Simultaneous Sampling ADCs with Shutdown

Table 10-3: **ADC Interface Signals**

Signal	FPGA Pin	Direction	Description
SPI_SCK	AA20	FPGA→ADC	Clock
AD_CONV	Y6	FPGA→ADC	Active-High, initiates conversion process.
ADC_OUT	D16	FPGA←ADC	Serial data. Presents the digital representation of the sample analog values as two 14-bit two's complement binary values.

Figure 43: Input and output signals of the analog to digital converter. Source: [8].

This unit consists of two analog to digital converters [34]. Only one unit will be required for Stargrazer One. Specifics on the type of analog to digital converter was not presented [34]. Regardless, in order for the ADC unit to execute its function, it must be presented with specific signals in an appropriate sequence. Figure 43 presents a table listing the required signals for the ADC unit. Figure 44 graphically presents

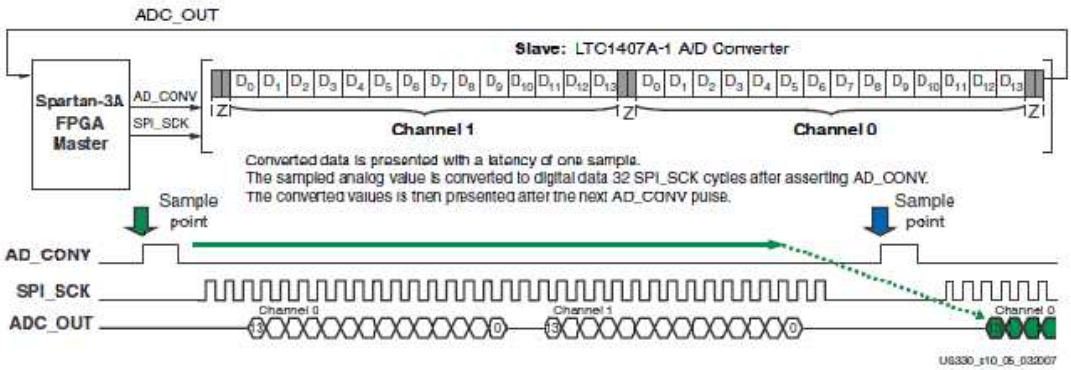


Figure 10-6: **Analog-to-Digital Conversion Interface**

Figure 44: This figure presents the signal interaction between the field programmable gate array and the analog to digital converter unit. Note that the analog to digital converter unit is pipelined. Source: [8].

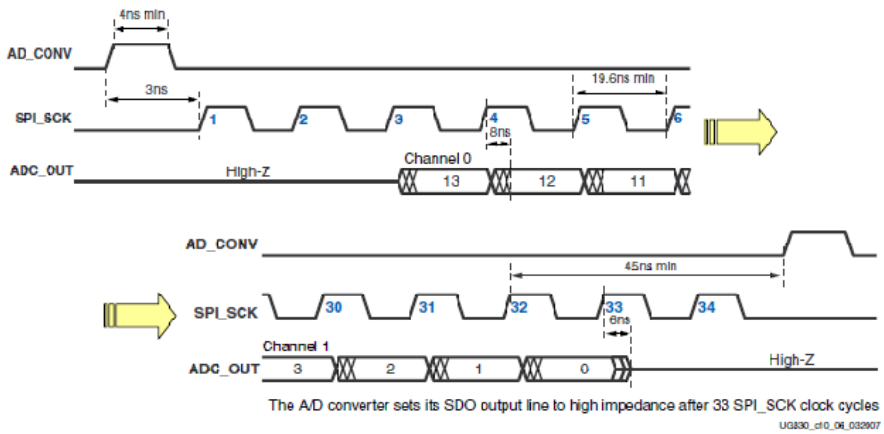


Figure 10-7: **Detailed SPI Timing to ADC**

Figure 45: Timing restrictions for the signals entering and exiting the analog to digital conversion unit. Source: [8].

how the required signals must be presented to the ADC unit. Figure 45 presents graphically timing constraints on the input signals.

Like the amplifier presented earlier, an interface architecture must be developed to present the appropriate input signal sequence to the ADC unit. However, in addition to this task, the architecture must also retrieve the digital representation for the sampled analog signals fed into the ADC unit. The digital representation is designated as a special signal as noted in figure 43. The digital representation is presented as a serial feed. The order that the bits exit the ADC unit via this feed is presented in figure 44. This output signal also has timing constraints reflected in figure 45.

Several observations can be made from these figures. Figure 44 shows that the ADC unit is pipelined with the signal labeled "AD_CONV" appearing to act as the

clocking signal for the pipe. Therefore, the ADC unit captures desired data on the first "AD_CONV" signal. This signal must be cycled again in order to extract the desired digital data. As shown in figure 44, the results from both ADC unit channels exit through the same output port. This architecture will need to only collect information for one of the channels and ignore the rest. The manual specifies that all digitized results should be fed out of the ADC unit before executing another conversion [8]. The architecture developed must make sure that this task has been accomplished.

Architecture

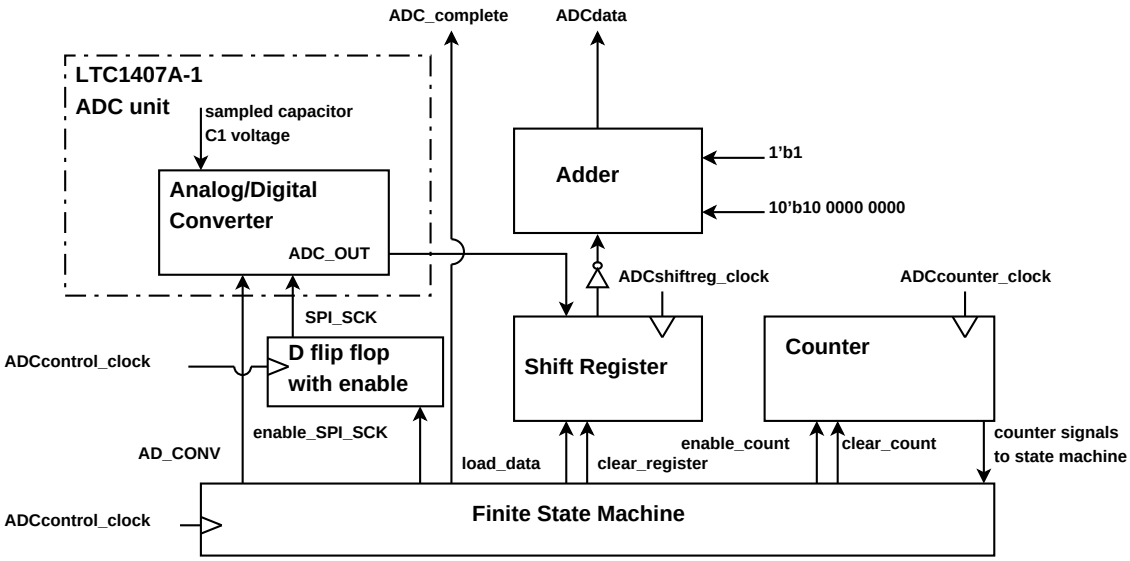


Figure 46: A top level schematic of the analog to digital converter interface circuit. All functional blocks along with signals are included. Directional arrows are used in the signals to indicate direction of data movement.

The following list adds to figure 46 by a describing the functions of the signals connecting the blocks.

- AD_CONV : This signal notifies the ADC unit to capture the analog voltage input and execute a conversion.
- ADC_OUT : This signal contains the digitized voltage values. It is a one bit wide signal as data is fed serially.
- SPI_SCK : Clocking signal for the ADC unit output
- initialize : The system-wide signal to initialize the interface circuit
- ADCdata : The final unsigned digital voltage value that will be presented to Stargrazer One
- enable_count : This signal permits the counter to begin incrementing

- load_data : This signal permits the shift register to begin to collect data from the ADC unit serial output
- ADC_complete : This signal becomes binary one once the correct digitized voltage value is ready for Stargrazer One. This signal is held for the equivalent of several cycles of the clock used by Stargrazer One. This is to insure that Stargrazer One receives this signal.
- clear_count, clear_register : These signals reset the contents of the counter and shift registers respectively to all zeroes.
- counter signals to state machine : presented as a single line for clarity in figure 46. Several counter values are checked for in order to ensure correct operation they are presented in the following list
  - begincollecting : This value of corresponds to a result of the binary two in the counter. This notifies the finite state machine to enable the shift register to start collecting data from the analog to digital converter.
  - endcollecting : This value of corresponds to a result of binary twelve in the counter. This notifies the finite state machine to disable the shift register.
  - count_done : This corresponds to a value of binary 34 in the counter. This notifies the finite state machine that all data from the ADC unit output feed has been removed
  - hold_ADCcomplete : This corresponds to a value of binary 60 in the counter. This signal imposes a delay on the movement of the finite state machine and ensure that this signal holds for several Stargrazer One clock cycles
- clock signals: Each of the individual generated clocking signals from the clocking circuit are now presented:
  - ADCcontrol_clock : This signal clocks the finite state machine. This same clocking signal is also fed into the circuit which controls the "SPI_SCK" signal.
  - ADCcounter_clock : This signal clocks the counter
  - ADCshiftreg_clock : This signal clocks the shift register

Figure 46 presents a "second level" block diagram description of the developed architecture to interact with ADC unit. The ADC unit is included in the figure to assist in visualizing where the appropriate input and output signals of the ADC unit go into the developed architecture. To facilitate adequate discussion, relevant functional blocks will be discussed in individual sections. Not shown in figure 46 is the clocking circuit developed for this proposed architecture. This will be discussed after the aforementioned discussion.

- Finite State Machine:
  - Architecture: Figure 52 presents a flowchart that shows state machine operation on a clock cycle by clock cycle basis. Certain states correspond to particular actions. Figure 52 includes this information. Table 14 presents the outputs generated by the state machine in a concise format. Note that the machine directs the analog to digital converter to sample and empties information from the serial output feed twice. This is due to the pipeline design of the ADC unit. This state machine is clocked by a custom generated clocking signal. The developed clocking circuitry is presented later in this appendix.

    The state machine is implemented using the one hot encoding method. The motivation for selecting this encoding method of is to take advantage of the simplicity in the state transfer and output logic.
  - Simulated Validation:

    The developed architecture was implemented using the Verilog hardware description language and tested in the Xilinx field programmable gate array design environment. To validate the proposed architecture, a test bench was developed. The test bench provided inputs similar to what will be seen in actual use and provided a theoretically correct implementation to compare the proposed architecture against.

    Figure 53 presents a illustrative sample of the results of a behavioral validation for the finite state machine. A single execution of the state machine flow chart presented in figure 52 is shown. Figure 53 presents relevant test inputs and appropriate outputs. The input signals presented are now defined:

    * clock [50 MHz]: This is a simulated rendering of the onboard clock for the Spartan 3AN development board.
    * state machine clock: This is the clocking signal that is fed into the state machine register.
    * ADC begin: When binary one, this signal notifies the state machine to begin the collection of information from the ADC unit.
    * sample again: This signal is included due to the pipelined nature of the LTC1407 ADC unit. When binary one, this signal tells the state machine to issue another command to the ADC unit to sample. This moves the appropriate output to the serial feed port.
    * clear: When binary one, the finite state machine is set to a default state.

    To assess performance, several outputs produced from both the proposed architecture and theoretically correct implementation are compared. This is shown in figure 53. Each grouping of output signals is together. For each output signal to be compared, the signal labeled "actual" comes from the proposed architecture, the signal labeled "expected" comes from the

theoretically correct implementation and the signal labeled "discrepancy" compares the two. When the signal labeled "discrepancy" is binary zero, the signals from both sources are matching. In addition to testing output signals directly from the state machine, the test bench contains two counter units to interact with each implementation. These counters have been verified functionally correct. The results from these counters are compared. The presented counter output in figure 53 labeled "for actual" is from the counter interacting with the proposed architecture. The counter output labeled "for expected" is from the counter interacting with the theoretical correct implementation and the signal labeled "discrepancy" compares these two signals. When binary zero, the signals from both sources match.

  - Conclusion:

    Figure 53 shows that across the presented instance, all discrepancies signals remain at binary zero. This suggests correct functional operation of the proposed architecture. The proposed architecture was subjected to additional testing both at the behavioral and post place and route levels. During the tests, the discrepancy signals remained binaries zero. This further supports the observed behavior in figure 53 and further justifies the conclusion that the proposed architecture will properly perform this function.

- N bit wide counter:

  The purpose of the counter is to assist in the preparation of the appropriate signals to the ADC unit. In addition, the counter assists in determining when the digitized results have been cleared from the serial output feed. In figure 46 (which presents the state machine flowchart), signals "count_done", "begincollecting", "endcollecting", "hold_ADCcomplete" are generated from the counter. As indicated in figure 46, these signals assist the state machine in knowing when to conduct certain operations. For example the signals "begincollecting" and "endcollecting" notify the state machine when relevant data is coming from the serial output of the ADC unit.

  The architecture itself is a typical counter architecture consisting of a register and a addition unit. The counter increases its value by one every clock cycle. The counter can only increase its value and it is designed to wrap around. The unit can also be set to all zeros. The counter also has a clock enable feature. When this signal is binary one, the counter operates normally. When the signal is binary zero, the counter holds its value. The signals to the state machine are made by tying the appropriate counter output bits together with logical gates.

  The described architecture was implemented using the Verilog hardware description language and tested in the Xilinx ISE design environments using an appropriate test bench. It was possible to verify the system at both behavioral and post place and route levels. The proposed architecture was determined to function correctly.

- Shift Register:

  The need for a shift register is twofold. The register is used to capture the digital representation of the analog voltage sampled at capacitor C1 by the ADC unit. The register also converts this digital representation from a serial feed into a N bit wide digital representation. The shift register is rising edge triggered and will shift once per clock cycle. Like the counter circuits, the shift register can be cleared and also possesses an enabled function.

  The described architecture was implemented using the Verilog hardware description language. It was tested in the Xilinx ISE design environment. The circuit was validated using an appropriately designed test bench at the behavioral and post place and route levels. The proposed architecture was determined to function correctly.

- Adder Circuit:

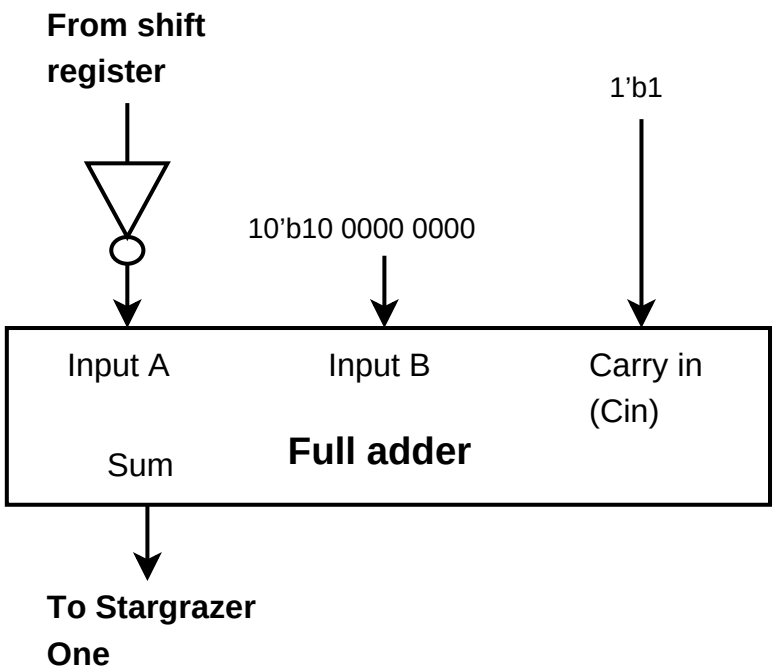


Figure 47: Second level schematic view of the final architecture used in the system. The logical gates and additional inputs presented to the adder are required to convert the digital voltage value from the ADC unit into a form Stargrazer One can use.

The need for this circuit is to convert the digital output from the ADC unit into an unsigned binary representation. Stargrazer One requires unsigned binary representations for the sample voltages in order to function correctly. It was experimentally determined that the ADC unit does not produce its output according to this requirement. This was done by recording the digital representations produced by the ADC unit for a series of predetermined analog input voltages. The observed output corresponds to a 2's complement representation.

The most significant positive value (the binary representation of $2^{N-1}-1$) corresponds to the minimum analog voltage the ADC unit can receive (0.4 volts) [8]. The most significant negative value (the binary representation of 2^{N-1}) corresponds to the maximum voltage the ADC unit can receive (2.9 volts) [8]. A digital output of all zeros was found to represent a value between 1.6 and 1.7 volts in the analog domain. A representative table taken from data in this experiment is available for viewing in table 12 at the end of this appendix chapter.

In order to ensure that Stargrazer One operates correctly, this 2's complement representation must be converted into an unsigned representation. Furthermore, the digital representation of all zeros should correspond to 0.4 volts or lower in the analog domain. The digital representations should increase with the analog domain voltages in a monotonic manner. The highest possible binary value (corresponding to a decimal value of $2^n - 1$) should correspond to the maximum voltage the ADC unit can receive.

Figure 47 presents the final architecture used to execute the required conversion of the ADC unit output. The architecture inverts the 2's complement values. Now the digital representations have been flipped, lower analog domain voltages are now being presented by negative binary representations and higher analog voltages are being represented by positive binary representations. This is still a 2's complement presentation.

By including the binary value of 2^{n-1} as one of the adder inputs, the digital representations originally represented by a binary value of M are now represented by $M + 2^{n-1}$. When combined with the inversion operation , the result is a representation compatible with the needs of Stargrazer One. This was verified experimentally using the same procedure described earlier. A representative table taken from data collected in this experiment is available in table 13.

The adder architecture itself is a ripple carry design consisting of a chain of appropriately connected addition circuits.

The complete architecture was implemented using the Verilog hardware description language. Performance of the circuit was verified using an appropriately constructed test bench in the Xilinx ISE design environment. The architecture of the adder circuit performed appropriately at both the behavioral and post place and route levels. Validation that an appropriate binary representation was being presented to Stargrazer One from the output of this architecture was validated by experimentation.

Clock Circuit

The need for a clock generation circuit is a direct result of the design. The circuit elements discussed are all clocked sequential circuits that interact with each other. This type of situation inevitably opens the door to timing issues such as race conditions. The chosen solution has each relevant sequential element (the finite state

Table 12: An illustrative sampling of data presenting the digital representations for analog values experimentally collected from the ADC unit. Only the most significant first 10 bits are collected. Stargrazer One does not use the entire 14 bit digital output from the ADC unit. The binary values are read from left to right with the most significant bit at the left. All voltage values are reported in Volts. Possible input voltages from the solar source circuit do not exceed 2.4 volts.

binary representation of analog voltages from ADC unit

	digital representation captured [2's complement]										
analog voltage	binary value										decimal value
0.4	0	1	1	1	1	1	1	1	1	1	511
0.7	0	1	1	0	0	0	0	0	1	0	386
1	0	1	0	0	0	0	0	1	0	0	260
1.3	0	0	1	0	0	0	1	0	1	0	138
1.6	0	0	0	0	0	0	1	1	1	0	14
1.9	1	1	1	0	0	1	0	1	0	0	-108
2.2	1	1	0	0	0	1	0	1	1	0	-234
2.4	1	0	1	1	0	0	0	1	1	0	-314

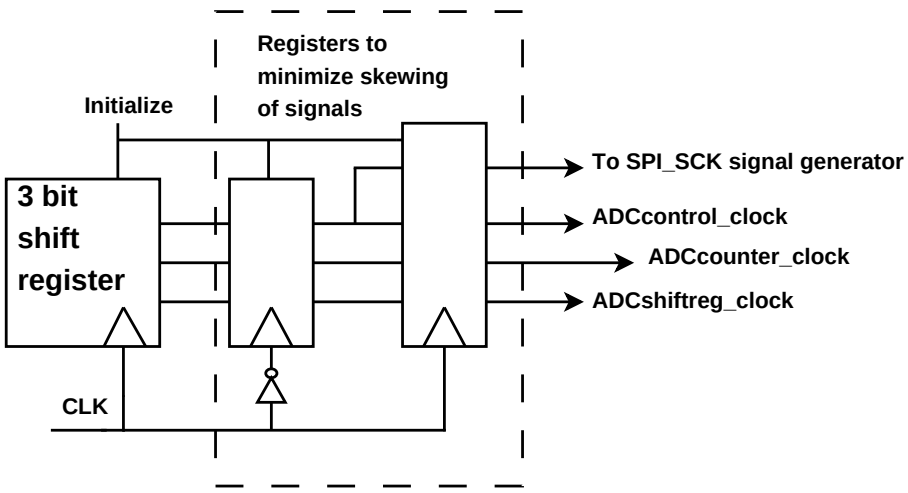


Figure 48: "Second level" block diagram view of the architecture developed to deliver the clocking signals to the various circuit elements in the ADC unit interface circuit.

machine, the counter, and the shift register) on their own independent clock signal. The clocking signals were designed so that no more than one element received a rising clock edge at any given time. Furthermore, the signals were designed so that within a given clock period, each functional unit will only be clocked once. The resulting designed clocking pattern is visually presented in figure 49. "CLK" is the 50 MHz on board system clock generated by the Spartan 3AN prototyping board. The other three signals are the generated clocking signals for the finite state machine, counter and shift register. Please refer to the caption in figure 49 for a key defining which

Table 13: An illustrative sampling of digital representations of analog voltages experimentally obtained from the proposed architecture. Only the most significant 10 bits of the ADC unit were used. Stargrazer One does not use the entire 14 bit digital representations that the ADC unit outputs. The binary representations are read left to right with the most significant bit on the left. Note that a monotonically increasing relationship between digital representation and analog voltage has been obtained. Possible input voltages from the solar source circuit do not exceed 2.4 volts.

binary representation of analog signals from proposed architecture

	digital representation captured [unsigned]										
analog voltage	binary value										decimal value
0.4	0	0	0	0	0	0	0	1	0	0	4
0.7	0	0	0	1	1	1	1	1	1	1	127
1	0	0	1	1	1	1	1	1	0	1	253
1.3	0	1	0	1	1	1	0	1	1	0	374
1.6	0	1	1	1	1	1	0	1	0	0	500
1.9	1	0	0	1	1	0	1	1	0	1	621
2.2	1	0	1	1	1	0	1	0	0	1	745
2.4	1	1	0	0	1	1	1	0	1	0	826

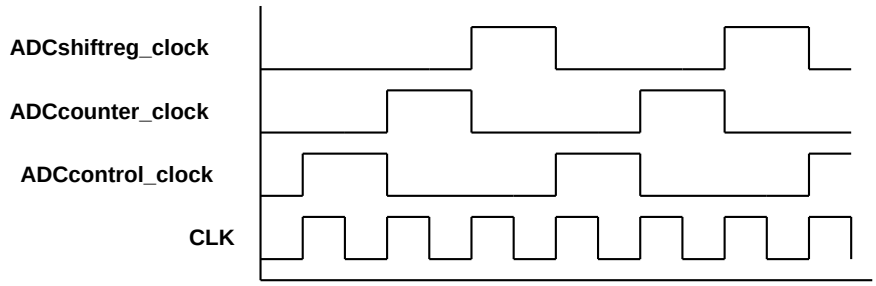


Figure 49: Graphical representation of the output produced from the circuit presented in figure 48. "ADCshiftreg_clock" goes to the clock port of the shift register, "ADCcounter_clock" goes to the clock port of the counter and "ADCcontrol_clock" goes to the clock port of the finite state machine.

signal goes where.

Figure 48 presents the architecture developed to execute the clock pattern presented in figure 49. The alternating signals are generated by the three bit shift register. It is clocked by the 50 MHz Spartan 3AN on-board clock. This circuit can also be cleared (labeled as "initialize" in figure 48). When cleared, the flip flop at the least significant bit position is designed to initialize to a value of binary one. Once the "initialize" signal falls to binary zero, the circuit left shifts. It is designed to wrap around. The additional registers were required to avoid issues as the Xilinx software programs the Spartan 3AN field programmable gate array.

The proposed architecture was implemented in the Verilog hardware description language and tested in the Xilinx ISE design environment. The circuit defined in

figure 48 was validated at both the behavioral and post place and route levels. The circuit was found to perform as expected. To validate whether or not this design averts timing issues, the implementation of this circuit was included in the complete design test of the ADC unit interfacing circuits. As the entire system performed successfully in simulation and the physical tests, this circuit is successful in its task.

System-wide Simulation

The complete architecture presented in figure 46 was implemented using the Verilog hardware description language. This script and was then tested using the Xilinx field programmable gate array design tools. Testing at the behavioral and post place and route level was performed.

Results With Conclusions

Figures 54 and 55 presents representative samples from behavioral level simulation to validate the developed architecture to interact with the LTC1407 ADC unit. To assist the reader in interpreting the visuals, presented signals are now defined:

- *ADCbegin* : This signal notifies the ADC unit interface circuitry to begin a conversion operation. When this signal becomes binary one, the unit begins work. The ADC unit interface circuitry will not respond to this signal again until the current conversion operation is completed.
- *sampleagain* : This signal notifies the ADC unit interface circuitry to execute another sampling action. The need for this signal is due to the fact that the LTC1407 ADC unit is pipelined. It takes two sampling commands to obtain desired digital information.
- $clock[50MHz]$: This is a simulated replica of the Spartan 3AN on board clock which is used by the ADC unit interface circuitry.
- *simulatedADCoutput* : These are values representing the captured and converted analog signals. These are presented in bus format for reference while testing. The signals will be presented as a serial feed to properly emulate the action of the LTC1407 ADC unit.
  - *desireddata* : This represents the desired information captured by the ADC unit.
  - *irrelevantdata* : This represents what could appear while the ADC unit interface circuitry clears the output of the ADC unit before issuing another sample command to obtain the desired information.
- *serialoutputs* : The simulated replication of the serial output that would be encountered in practice. The signal labeled "for actual" presents the simulated replication of the feed that goes into the proposed architecture. The signal labeled "for expected" presents the simulated output feed that goes into the

theoretically correct implementation. The circuitry developed to produce these serial outputs has been validated to produce the serial output in a manner equivalent to the LTC1407 ADC unit.

- *clear* : When binary one, both architectures (proposed and theoretically correct) are set to an initial state.
- *ADCcomplete* : This signal becomes binary one when the ADC unit interface circuitry has completed producing a properly adjusted 10 bit digital representation of the capacitor C1 voltage for Stargrazer One
- *converterresult* : This bus contains the prepared digital representation of the capacitor C1 voltage.
- *SPI_SCK* : This is a clocking signal for the LTC1407 ADC unit. This signal must be generated in order to empty the outputs of the unit via the serial feed.
- *AD_CONV* : This signal when binary one notifies the ADC unit to sample the analog signal at its input. In addition, it advances the two stage pipeline of the LTC1407 ADC unit.

Figure 54 presents the proposed architecture and the theoretically correct implementation (developed inside the test bench) executing a conversion. That trace begins from the prompt to begin conversion until the signal "ADC complete" turns binary one.

Figure 55 presents the proposed architecture completing several conversion actions.

In figures 54 and 55, the proposed architecture is found to successfully function. This is indicated by the fact that the "discrepancy" signals remain binary zero. In figure 55, the observed spikes in the discrepancy signal for "SPI_SCK" were determined to be instantaneous glitches (artifacts of the simulator). The proposed architecture was also subjected to additional testing at both the behavioral and post place and route levels. In all cases, the proposed architecture was found to function properly.

Closing Remarks

This appendix presented the architecture developed to successfully interact with the on board analog capture and conversion hardware available in the Spartan 3AN development board. Being able to correctly use these instruments is essential to being able to produce a meaningful hardware based validation of the proposed Stargrazer One power point tracking architecture. This appendix described the architecture and provided samples of simulated validations. The testing demonstrates that a valid architecture has been developed to directing the available hardware in the capturing of information from capacitor C1 into a form usable by Stargrazer One.

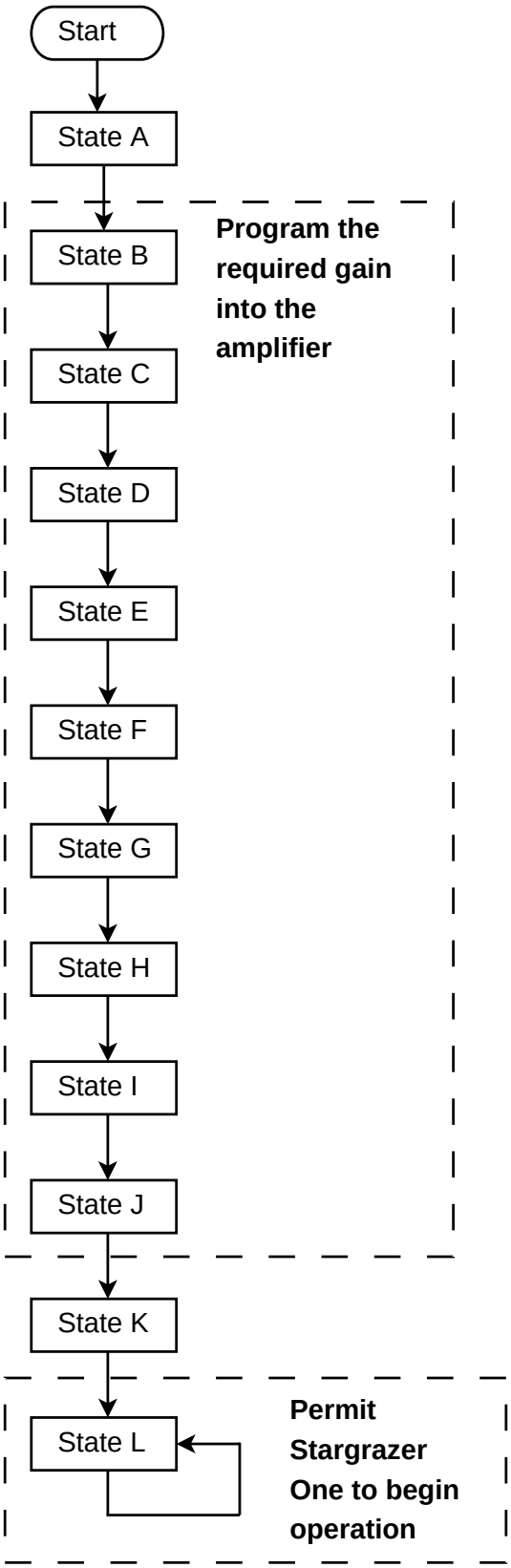


Figure 50: State Flow diagram for the state machine used to program the amplifier unit.

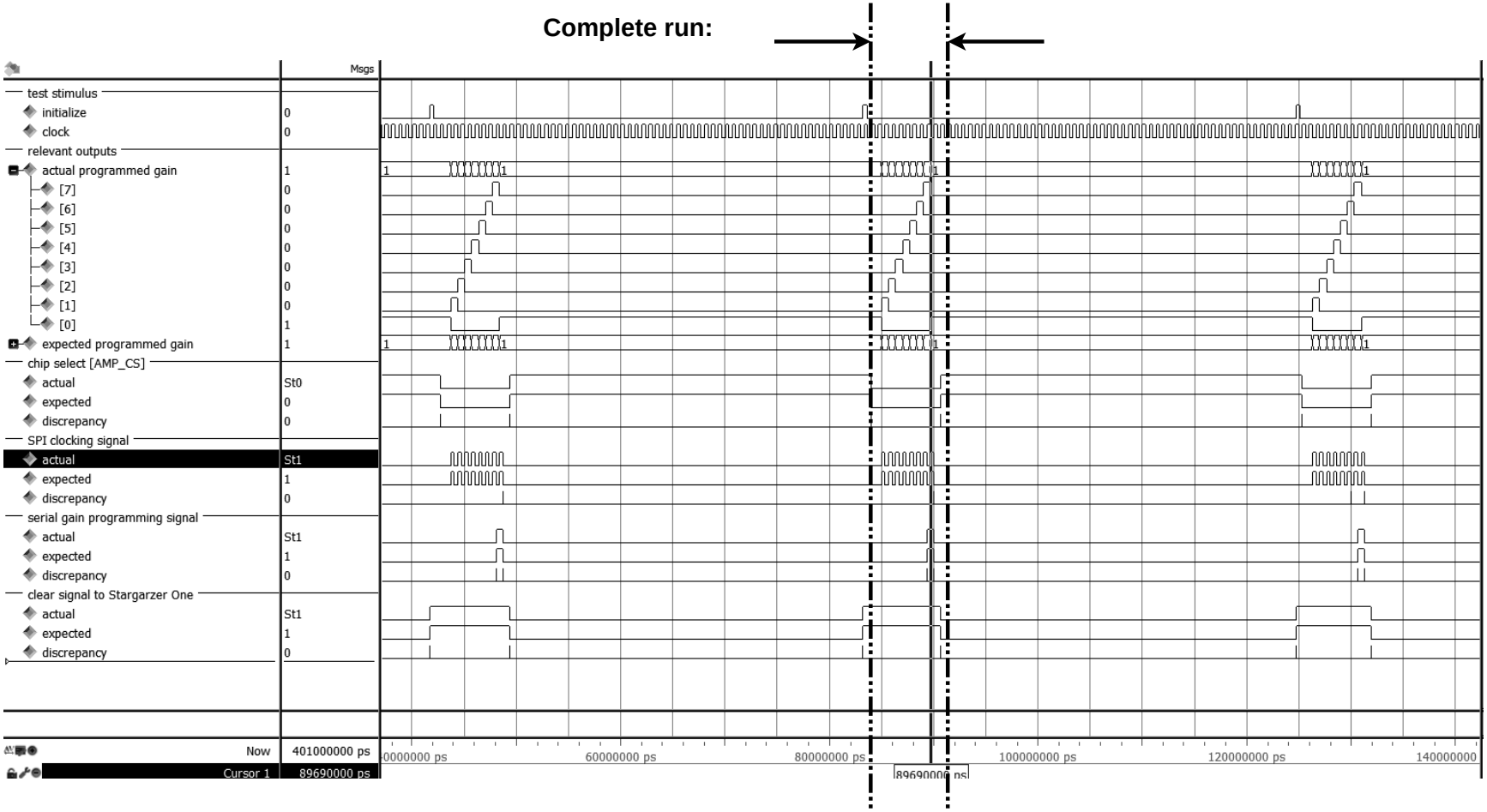


Figure 51: Behavioral level simulation showing several successful runs of the proposed amplifier programming circuit. All relevant signals are labeled in the figure. Signals labeled "actual" come from the proposed architecture. Signals labeled "expected" come from a theoretically correct reimplementation of the programming architecture. The signal labeled "discrepancy" is a comparison between the actual and expected signals. A value of zero indicates that the values match. The spikes observed were instantaneous glitches, an artifact of the simulation.

Table 14: State output table, the purpose of each signal is indicated in section 15.3.

State	Outputs					
	AD_CONV	enable_count	load_data	ADC_complete	clear_count	clear_register
A	0	0	0	0	0	0
B	0	0	0	0	1	0
C	0	1	0	0	0	0
D	1	0	0	0	1	1
E	0	0	0	0	0	0
F	0	1	0	0	0	0
G	0	0	0	0	1	0
H	0	0	0	0	0	0
I	1	0	0	0	0	0
J	0	0	0	0	0	0
K	0	1	0	0	0	0
L	0	1	1	0	0	0
M	0	1	0	0	0	0
N	0	0	0	1	1	0
O	0	1	0	1	0	0
P	0	0	0	1	1	0
Q	0	1	0	1	0	0

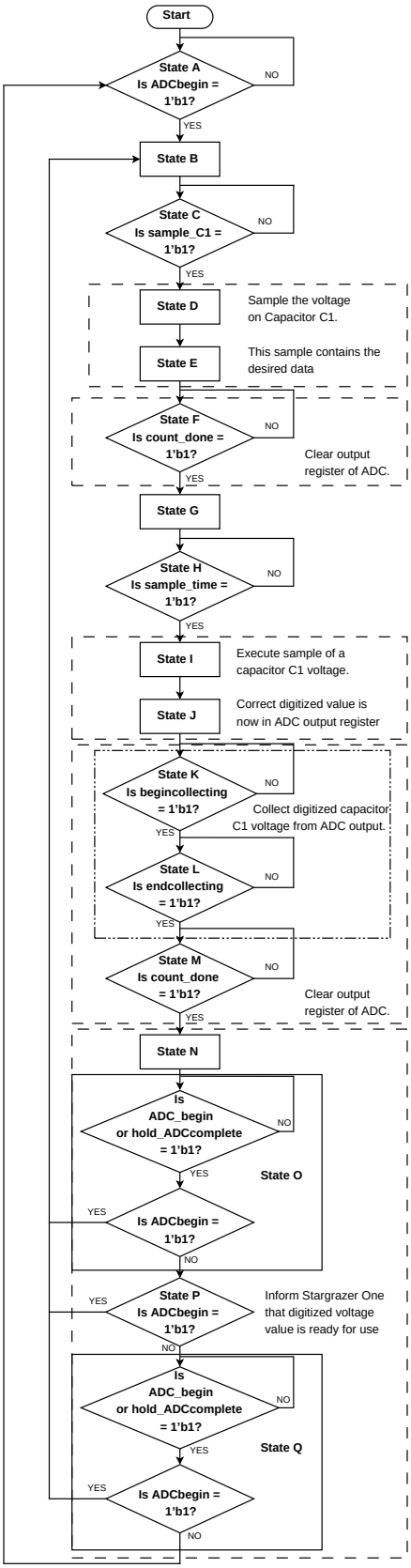


Figure 52: State flow diagram for the state machine shown in figure 46.

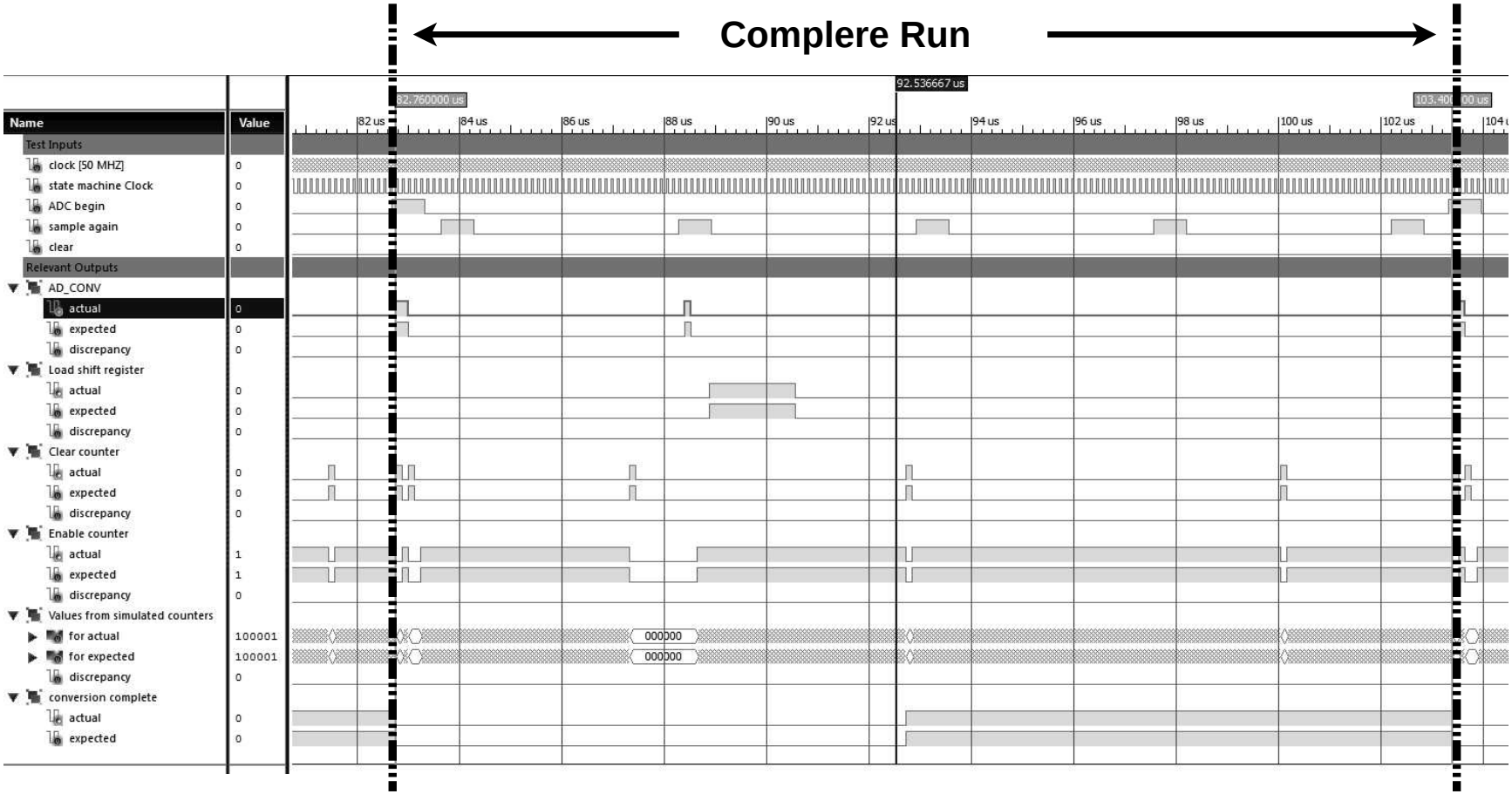


Figure 53: Validation trace of the finite state machine of the ADC unit interfacing circuit. Trace names are explained in section 15.3.

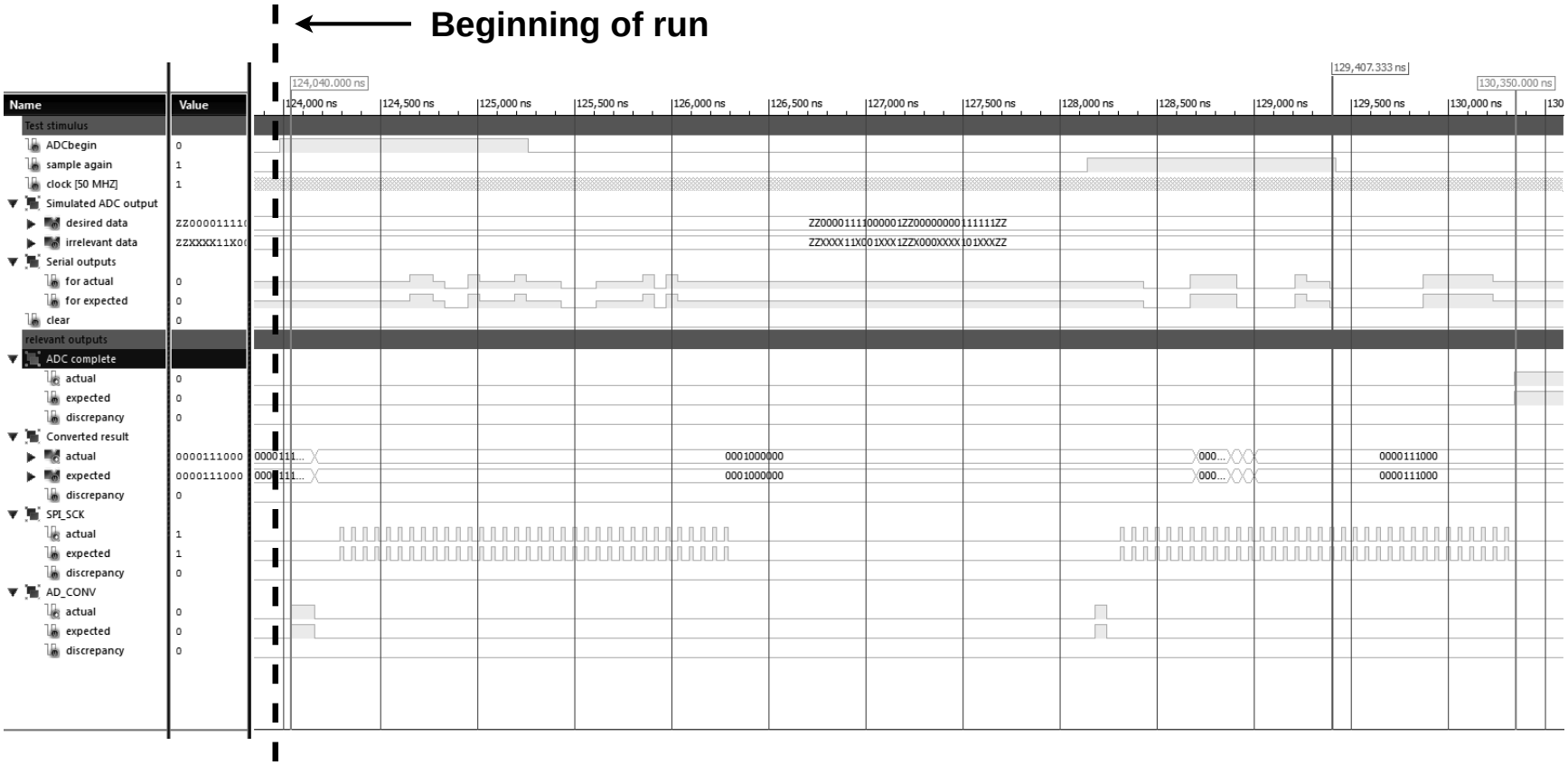


Figure 54: Behavioral level simulation wave trace showing a successful execution of a single analog to digital conversion. Relevant test stimuli and outputs are reported in the figure. For each output, the signal labeled "actual" comes from the proposed architecture. The signal labeled "expected" comes from a theoretically correct implementation in the test bench and "discrepancy" compares these two signals.

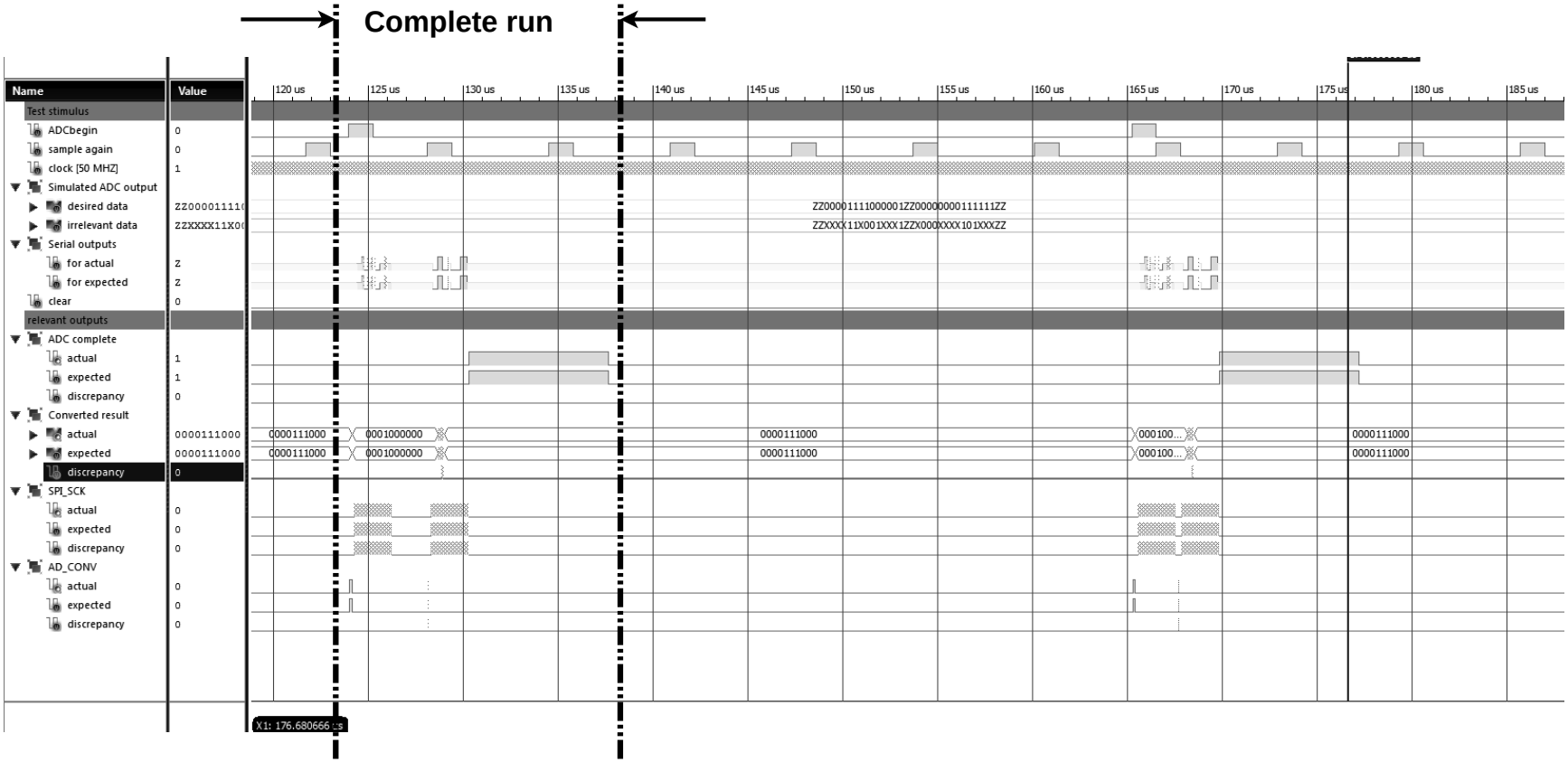


Figure 55: Behavioral level simulation trace showing successful conversion actions done by the proposed architecture. Relevant test stimuli and outputs are reported in the figure. For each examined output, the signal labeled "actual" comes from the proposed architecture. The signal labeled "expected" comes from a theoretically correct implementation in the test bench used to examine the proposed architecture. The signal labeled "discrepancy" compares these two results.

Discussion of Additional Circuits Designed To Interact Additional Components of the Spartan 3AN Development Boards

Introduction

The developed Stargrazer One architecture did not include a means to generate the required system clock signal or the global reset signal. For the hardware prototype to be useful for testing, a means to produce these two required signals must be created. The Spartan 3AN prototyping board does possess its own clock. In addition, the prototyping board features many buttons and switches presenting a convenient means to apply a global reset signal. However, in order to ensure proper functioning of Stargrazer One, it was required to develop interface circuits to use the switches and the onboard clock. The purpose of this appendix is to present the developed circuits. Each circuit will be discussed individually.

Switch De-bouncing Circuitry

The Spartan 3AN FPGA test board has several mechanical switches and buttons to permit interaction with prototyped systems. For the purposes of this testing, Stargrazer One will make use of one of these switches. The switch, when active high, is to return the entire system to an initial state.

According to the manual, these switches will have roughly two milliseconds of mechanical bounce [8]. The switches do not have internal switch de-bouncing circuits [8]. Switch bounce is a form of noise which can result in the system behaving in an unexpected or undesired manner. The need for an interface circuit is to mitigate the risk of improper functioning posed by this noise.

Architecture

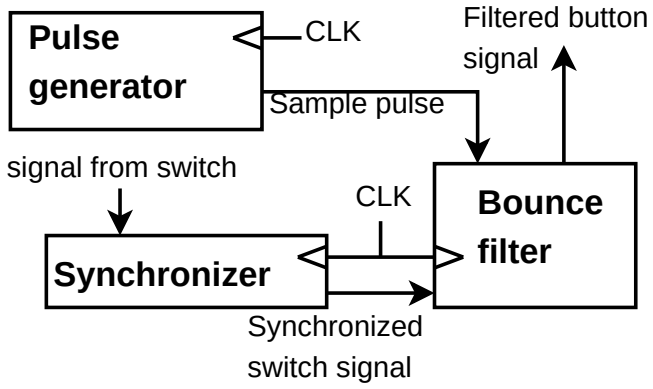


Figure 56: A top level block schematic showing the components used in the switch de-bouncing circuitry. Components are labeled along with the signals that move between the components. Signal direction is indicated by the arrowheads.

Figure 56 presents the architecture to be implemented for this switch de-bouncing circuit. As can be observed, this system can be divided into three blocks. They will now be discussed individually

- Synchronizer: The architecture itself is two cascaded D flip flops. The purpose of this arrangement is to synchronize the random input from the switch into a waveform which transitions in accord with the system clock. Two flip flops were selected as it was found to minimize the possibility of metastability.

- Pulse Generation Circuit: The purpose of this circuit is to determine when the sampling of the switch input is to take place. The core functional block is a counter. An appropriate output value is checked for by logic. Care must be taken in the choice of what output value to use. A large count value may cause additional delay in filtering the input signal. A smaller count value may require more samples in order to effectively filter noise from the switch. It was decided to have the pulse spaced 500 μs apart. The counter is composed of a register of D flip flops with half adders to execute the incrementing.

- Bounce Filter Circuit: This component is more complex than the two prior blocks. A visual representation of this circuit is presented in figure 57.

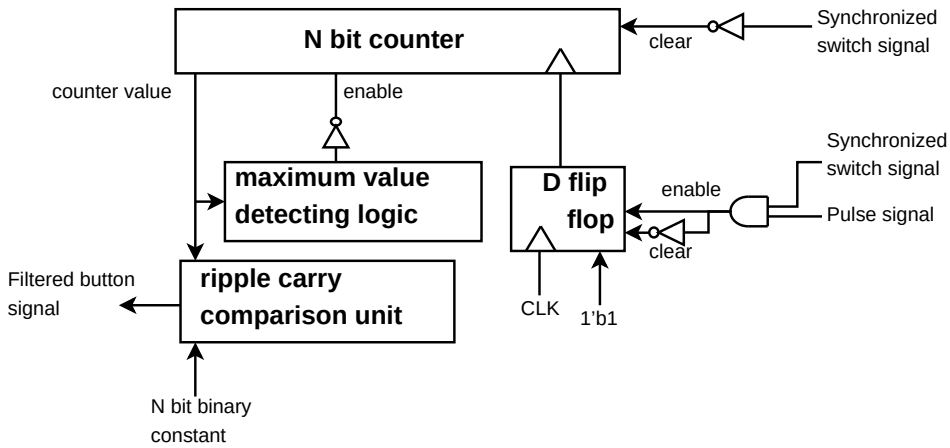


Figure 57: System level view of the de-bouncing circuit. Components and signals have been labeled. Signal direction is indicated by arrowheads on the appropriate signals.

As seen in figure 57, this circuit consists of a saturating counter configured to increment by binary one and a digital comparison unit. The circuit is designed to check for when the switch is closed (an input value of binary one). When the input signal from the mechanical switch is binary one, the counter is allowed to increment. The counter is clocked by the pulses from the Pulse Generation Circuit. Should the switch input fall to binary zero, the saturating counter is reset to zero. The comparator compares the results from the saturating counter to a fixed value. Once the counter value exceeds this fixed value the switch is

assumed on. Care should be exercised in the selection. Too large a value may result in missing legitimate but fast switching. Too small reduces the robustness of the system to the noise of the mechanical or electrical switches. In this design a value of 20 was used for the fixed value. This was computed to filter out switch on times of less than 10 milliseconds. It was deemed safe to assert that if the input signal remains binary one for longer than 10 milliseconds, the switch is physically on.

The counter used has the same architecture as the unit used in the Pulse Generator Circuit. The comparison circuit is the same architecture as the comparison units presented in appendix 15.3. This design will not be run at high speeds permitting the use of this architecture.

Simulation

Each functional block was evaluated using the procedure presented in part III. This section will only present the simulated validation of the top level circuit. The circuit was evaluated at both of the behavioral and the post place and route levels.

Results With Conclusions

Figures 59 and 60 were taken from a behavioral level validation of the proposed architecture. The figures present an example of the observed system response to the switch transitioning from the off to on position and vice versa. To simulate switch bounce, the stimulus representing the input from the switch (labeled "signal from button") in the figures is designed to rapidly alternate from binary zero to binary one for a time.

For all output signals presented in the figure 60 and 59: Signals labeled "actual" come from the proposed architecture. Signals labeled "expected" come from a theoretically correct implementation in the test bench. The signals labeled "discrepancy" compare the differences between the "actual" and "expected" signals.

Figure 59 shows the proposed architecture successfully reacting to when the switch is moved to the off position. As can be seen, the filtered switch signal seen by Stargrazer One promptly falls to binary zero when the switch input falls to binary zero. There is simulated noise on the switch input but the signal to Stargrazer One remains binary zero. This means the noise is being filtered. The architecture is performing consistent with expected behavior.

In the case of figure 60, the system successfully filters out the simulated noise. The filtered switch signal seen by Stargrazer One does not change to binary one until the actual switch input remains at binary one for the designed predetermined time. This is consistent with expected behavior as presented in figure 60.

Clock Preparation Circuit

The Spartan 3AN FPGA developments board only has a $50MHZ$ clock generator. The 50 MHz clock is too fast for Stargrazer One. To bring the clock frequency down

to a more acceptable level, it was necessary to design a frequency dividing circuit.

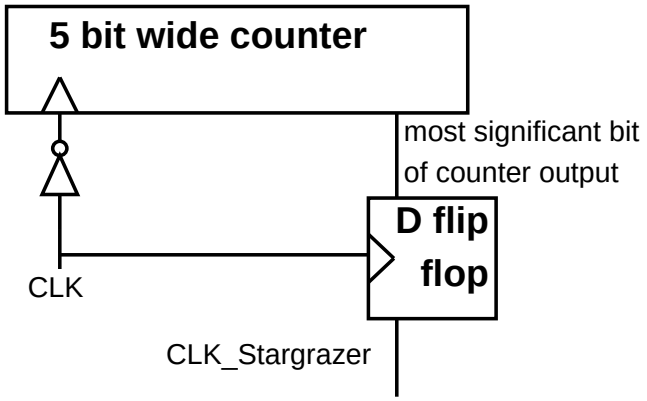


Figure 58: Schematic showing the implementation of the clock scale down circuitry. The signal labeled "CLK" is the $50MHz$ clock from the development board. "CLK_Stargrazer" is the slowed down clock to be used by the Stargrazer One architecture.

Figure 58 presents a top level view of the circuit to be used. The scale down of the 50 MHZ clock signal is accomplished with a counter. The counter is a register and an incrementing circuit. The most significant bit of the counter output is used for the clocking signal.

An observer will note that figure 58 shows the counter advancing on the falling edge of the system clock and the flip-flop is rising edge triggered. This was done to have the "CLK" and "CLK_Stargrazer" signals transition in sync. "CLK_Stargrazer" is a clocking signal with a frequency of $781.25kHz$. This frequency is slow enough to ensure that Stargrazer One correctly functions while significantly faster than many environmental changes.

Each level of the circuit was a tested in simulation to validate functional correctness. Testing was done in the post place and route and behavioral levels. The proposed architecture was found to operate correctly.

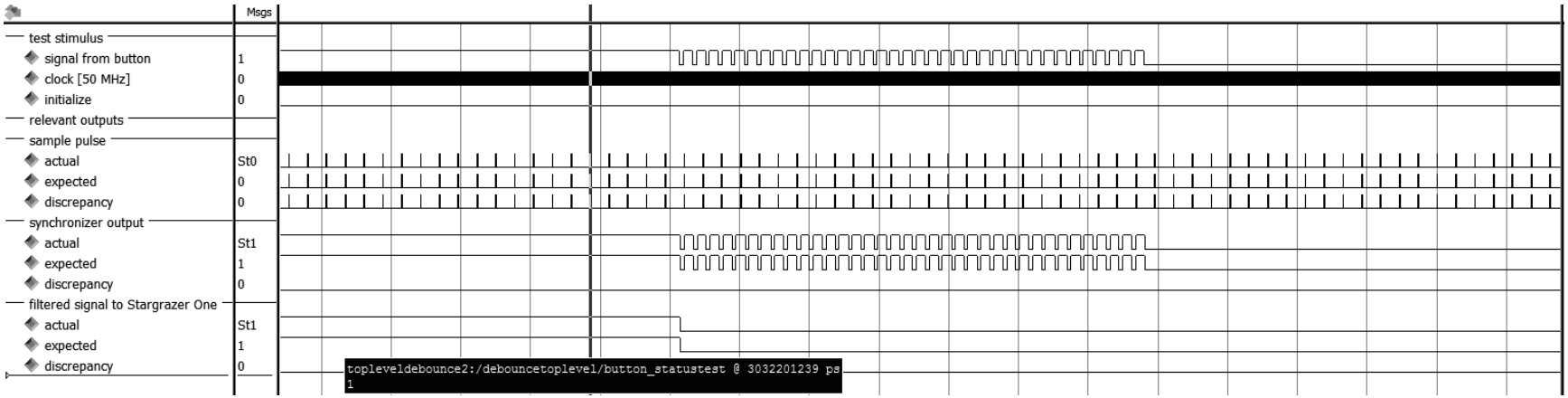


Figure 59: Illustrative sample from a behavioral level validation of the complete switch de-bouncing circuitry. Depicted is a response to the switch transitioning to the off position from on.

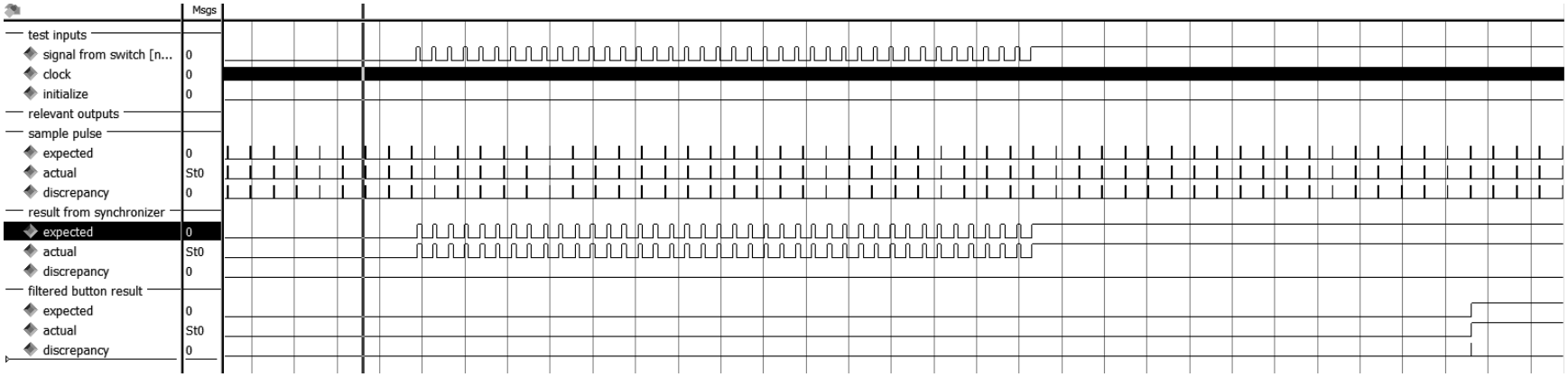


Figure 60: Illustrative sample from a behavioral level validation of the complete switch de-bouncing circuitry. Depicted is a response to the switch transitioning to the on position from off.

Discussion of Circuits Developed To Drive the Transistors In the Step Down Switched Capacitor Converter

Introduction

Directly connecting the gates of transistors T1 and T2 to the appropriate output pins of the Spartan 3AN FPGA development board was insufficient to turn on the transistors in a timely manner. It was found that the NXP PSMN2R0-30PL N channel power MOSFETs used for transistors T1 and T2 have a large gate capacitance. In order to be able to validate the proposed Stargrazer One architecture, it was necessary to develop interfacing circuits between the Spartan 3AN FPGA and the power transistors to enable them to be turned off and on in a desired manner. This appendix will proceed as follows:

- The need for an interfacing circuit
- The developed architecture and its observed performance
- Relevant concluding remarks

Need For An Interfacing Circuit

The need for this circuit is due to the fact that transistors T1 and T2 have large capacitances on their gates. The gate terminal in these MOSFETs is isolated from the rest of the device by an insulating material. This structure is an instance of a capacitor. Therefore, if one desires to have a particular voltage on the gate of a MOSFET, the source must be able to deliver the appropriate charge needed to this capacitor.

It was possible to estimate the gate to source capacitance using the provided specifications for the chosen transistor. The equation used is presented:

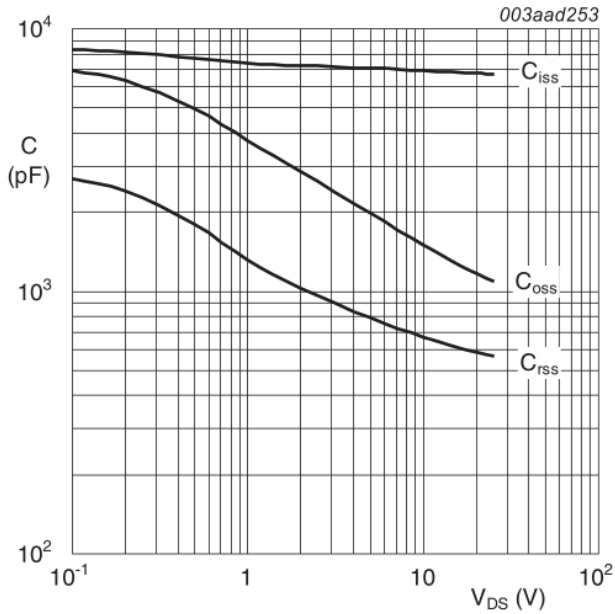
$$C_{GS} = C_{ISS} - C_{RSS} \tag{19}$$

Where C_{ISS} and C_{RSS} are defined as the input capacitance and reverse transfer capacitance respectively. C_{GS} is the gate source capacitance.

These were graphically presented in the datasheet for the PSMN2R0-30PL power mosfets (presented in figure 61). To estimate the actual value it was deemed prudent to design for the worst case capacitance value. For this particular device, the value of C_{GS} increases as a function of increasing Vds (drain source voltage).

For each transistor, the estimations are as follows:

- Transistor T1: For this device, the largest value of drain source voltage is observed immediately upon entering State One. At this point, capacitor C1 is at its lowest operating voltage and the solar cell source is at open circuit voltage. For the purposes of estimating, a Vds value corresponding to the open circuit voltage was used for the computation. This is likely larger then what could be encountered in practice, but a conservative estimate was desired. Measured and computed values are now presented:



$$V_{GS} = 0V; f = 1MHz$$

Figure 61: Gate capacitance graphic from the transistor data sheet used for the estimates conducted in this section. Source: [9].

- C_{iss} = 70 nF
- C_{rss} = 9nF
- C_{GS} = 61 nF

- Transistor T2: For this device, the largest value of drain source voltage is observed immediately before entering State Three. It is plausible to find in practice situations where capacitor C1 assumes a value very near the open circuit voltage and where capacitor C2 is approaching ground. It was decided to adopt the same estimate used for transistor T1 for the worst case gate source capacitance for this device. Thus, the capacitance results will be the same.

These are rather large values (C_{GS} = 61 nF). This means transistors T1 and T2 will require rather large current draws to rapidly activate them. The gate voltage as a function of time can be modeled as follows:

$$V(t) = \int_{t_o}^{t} \frac{I(t)}{C} dt \tag{20}$$

Assuming a constant current source I for $I(t)$, replacing C with C_{GS} and starting from $t_o = 0$ gives the following change to equation 20:

$$V(t) = \frac{I}{C_{GS}} * t + V_o \tag{21}$$

With the capacitance of the gate estimated, it is possible to determine if there is a need for a gate driver circuit. The Stargrazer One prototype presented in chapter 15 uses a clock frequency of $781.25kHz$. This corresponds to a period of $1.28\mu s$. The output pins for the Xilinx Spartan 3AN FPGA board were found to provide a maximum voltage of $3.3V$ and a current drive of $25mA$ [35]. In order to turn on transistor T2 or transistor T1, the gate voltage must exceed the source voltage by at least the threshold voltage. It will be necessary to turn on and turn off these transistors within one clock cycle. To determine if the Spartan 3AN output pin drive strength is sufficient, equation 21 is reworked with new values. Values and results are in table name here 15.

Table 15: Table showing if transistors T1 and T2 can be directly driven by the FPGA output pins.

values for equation 21		
V_o	0	V
t	1.28	μs
I	25	mA
C_{GS}	61	nF

results		
$V(t)$	.5246	V

Table 15 shows the most the voltage will change on the gate of either transistor T1 or T2 by just over 0.5 volts. These transistors have a rated minimum threshold voltage of 1.3 volts [9]. The result presented in table 15 is insufficient to drive these transistors at the required speed. Given the results, there is a need to develop a gate driver circuit for each transistor.

Another reason for developing a gate driver circuit was noted during this experiment. The Spartan 3AN field programmable gate array output pin voltage is 3.3 volts. This may be sufficient to drive transistor T2. As demonstrated in appendix 15.3, the open circuit voltage of the developed solar source circuit model is 2.3 volts. As capacitor C1 charges during State One, the source voltage will approach this value. The difference between the Spartan 3AN FPGA output pin voltage and this open circuit voltage is rougly one volt. This is less than the minimum threshold voltage of transistor T1 [9]. This means that transistor T1 would turn off prematurely as capacitor C1 charges. These transistors should switch on and off pursuant to the switching pattern from Stargrazer One. A solution is to present a sufficiently high gate voltage so that the transistor remains on when capacitor C1 is charged to open circuit voltage. Creating this voltage will require some form of interfacing circuitry.

Architecture and Performance Validation

To meet the need outlined in the previous section, the following circuitry was developed. The circuit takes the appropriate output from the Spartan 3AN FPGA and

produces an appropriate signal to drive the power transistors. The circuit topology and experimental performance traces will be presented.

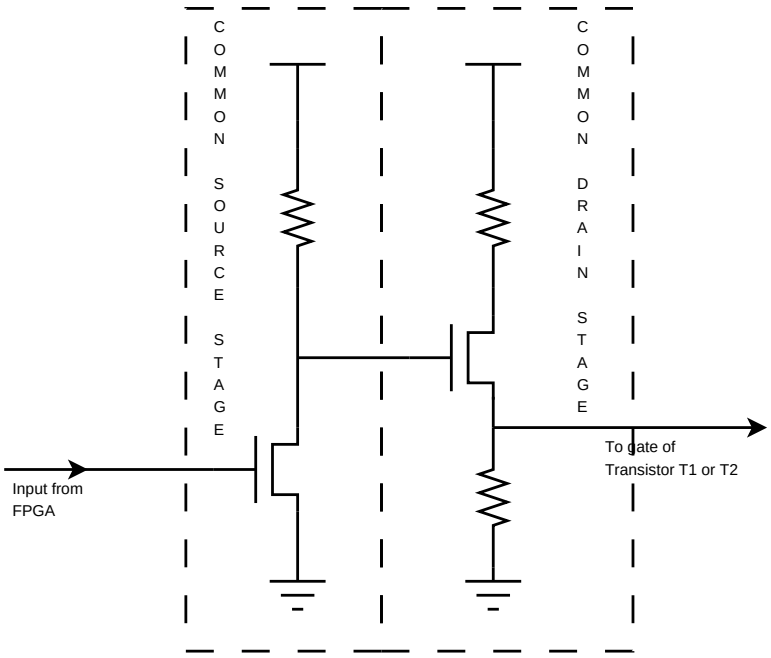


Figure 62: Circuit diagram for the developed gate driver circuits. The depicted circuit is used twice (each instance drives one of the power transistors). Each sub circuit is labeled in the image. Details for each sub circuit is discussed in the appropriate section.

Figure 62 presents a schematic showing the drive circuit to be used. Two instances of this circuit will be used. Each one will drive one of the transistors. As shown in figure 62, the circuit is two cascaded amplifiers. Each one is now individually discussed.

- Common Source Amplifier: This is the circuit in figure 62 labeled as "common source stage". The intent of this circuit is to increase the amplitude of the voltage waveform from the FPGA to one sufficient to keep the transistors on for as long as desired. The amplifier was designed with the intention to produce an output signal that saturates at both power supply values (0 and 9 volts on the prototype). Table 16 presents the designed gain for the common source stage for each transistor of the step down converter.

  Figures 63 and 64 present oscilloscope captures from the esperimental validation of the common source circuit. All relevant signals are labeled. As seen in figures 63 and 64, the observed output voltage is sufficiently high. The observed oscillation of the output voltage signal goes from the positive power supply voltage to nearly ground. It was found by experimentation that this stage alone could not drive the gates of the power transistors. An additional stage (which will be discussed next) produces a signal with sufficient current to turn

Table 16: Computed values for the common source amplifier. Gm is the transcondutance. This value is estimated using data from the specification sheets for the transistors. R_d is the resistance placed between the drain of the MOSFET and the positive power supply rail.

Transistor Two		
Gm	.0667	S
R_d	310	Ω
Av	-20.667	V

Transistor One		
Gm	.0667	S
R_d	310	Ω
Av	-20.667	V

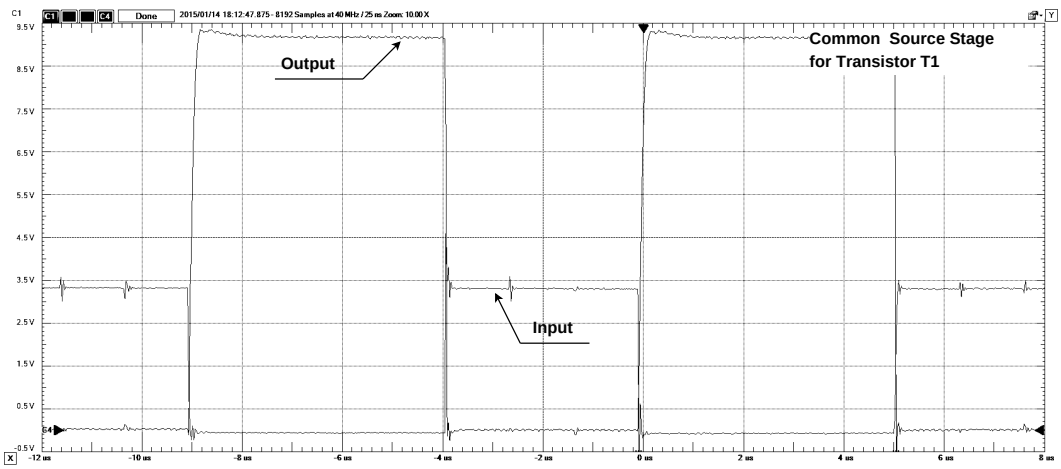


Figure 63: Experimentally observed input and output waveforms for the common source stage for transistor T1. Signals are appropriately labeled. Time is on the horizontal axis and voltage is on the vertical axis.

on the power transistors. Figures 63 and 64 shows the output and input signals inverted. This is an artifact of the particular amplifier chosen. When the input voltage is zero, the transistor is off. The output is at the positive Power Supply voltage. Conversely when the input voltage is 3.3 volts, the transistor is on and the output drops to near ground. To make sure that the appropriate signal is presented to the gates of the power transistors, the transistor T1 and T2 gate signals pass through inverters inside the field programmable gate array before arriving at the transistor.

- Common Drain Amplifier: The schematic is presented in figure 62 labeled as "common drain stage". The circuit design is also called a source follower. When the input to the gate is high, the transistor will be turned on. A large gate

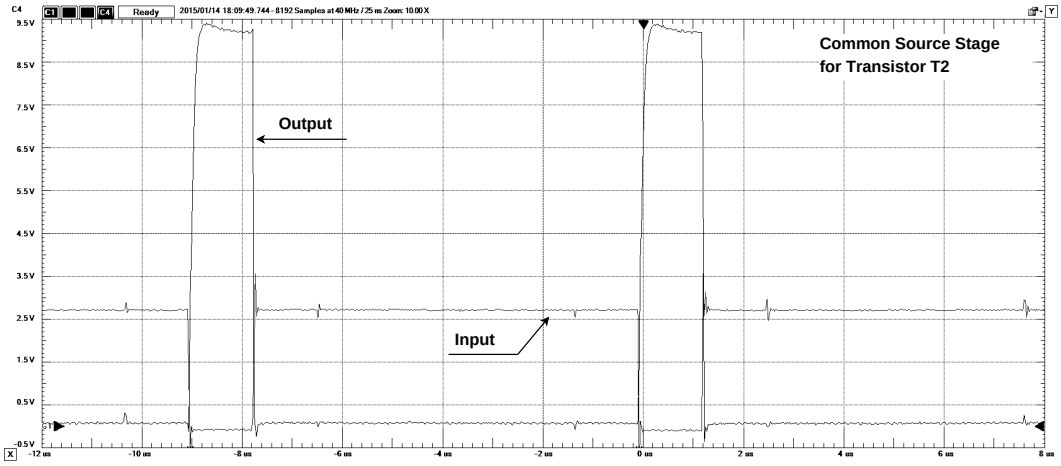


Figure 64: Experimentally observed input and output waveforms for the common source stage for transistor T2. Signals are appropriately labeled. Time is on the horizontal axis and voltage is on the vertical axis.

source voltage will be presented. The transistor will be biased to sink a significant amount of current. To avoid destroying the device, a safety resistor is placed between the positive power supply voltage and the drain terminal of the transistor (see figure 62). Figure 62 shows the output between the source of the transistor and a resistance to ground. When the transistor is active, the resulting current will be split between this resistance and the output. The resistor is sized so that a majority of the current goes to the output. When the transistor is off, the source to ground resistance presents a conductive path to ground.

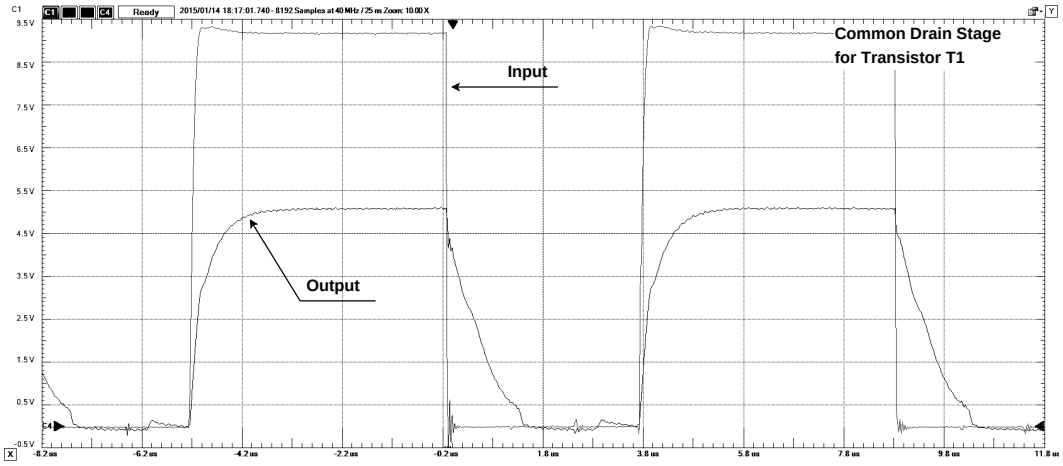


Figure 65: Observed experimental wave traces for the common drain circuit stage serving transistor T1. Output and input signals are presented and appropriately labeled. The circuit is connected to the appropriate transistor on the power electronic circuit. Time is on the horizontal axis and voltage is on the vertical axis.

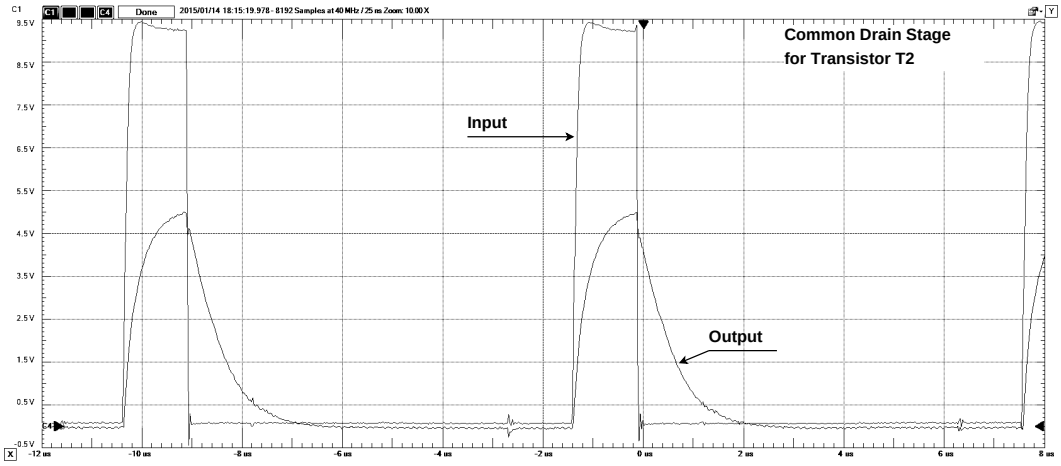


Figure 66: Observed experimental wave traces for the common drain circuit stage serving transistor T2. Output and input signals are presented and appropriately labeled. Circuit is connected to the appropriate transistor on the power electronic circuit. Time is on the horizontal axis and voltage is on the vertical axis.

As is observed in figures 65 and 66, the proposed circuit (when in cascade with the common source amplifier stage discussed) presents a strong signal to the gate of the power transistors. As shown in figures 65 and 66, the PSMN2R0-30PL transistor gate capacitance charges and discharges in a timely manner assuming values from ground to $\approx$ 5V. The final value is sufficient to ensure that the power transistors remain on when they are supposed to. Figures 65 and 66 do show a curved rise and fall of this signal. This is due to the equivalent resistor capacitor circuits formed from the common drain circuit and the gate capacitances of the power transistors in the step down converter. Figures 65 and 66 shows a final value of output voltage less than the positive power supply voltage. This is an artifact of the design of the common drain circuit. The voltage seen from the gate capacitance is lower due to the fact that a voltage divider is created from the resistances in the circuit.

Complete Circuit Validation With Conclusions

Figure 67 shows the gate voltages seen by both the transistors of the switched capacitor power electronics converter from the developed circuit. The figure shows both devices receiving signals of sufficient drive strength to affectively charge and discharge the gate capacitance in a timely manner. The final value achieved is $\approx$ 5 volts. This value is sufficiently high to ensure that the transistors in the converter remain on when they are supposed to. This confirms that a suitable system has been developed to drive these transistors.

It is important to note that the developed gate driver circuits are suitable for the purposes of developing and testing a hardware prototype of Stargrazer One. The developed design is not appropriate for power sensitive applications. It was found that significant currents were required to drive the power transistors. For these

Table 17: Devices used to design the gate drive circuits for transistor T2. Resistor values reported are produced from series and parallel combinations of resistors. This was necessary to meet power dissipation and design requirements.

Transistor Two Gate Drive Circuit

Common Source Amplifier

Device	value	unit
FET	n-MOSFET	zvn2210a
R_d	310	Ω

Common Drain Amplifier

Device	value	unit
R_{safety}	47	Ω
FET	n-MOSFET	zvn2110a
R_s	67	Ω

Table 18: Devices used to design the gate drive circuits for transistor T1. Resistor values reported are produced from series and parallel combinations of resistors. This was necessary to meet power dissipation and design requirements.

Transistor One Gate Drive Circuits

Common Source Amplifier

Device	value	unit
FET	n-MOSFET	zvn2110a
R_d	310	Ω

Common Drain Amplifier

Device	value	unit
R_{safety}	50.495	Ω
FET	n-MOSFET	zvn2110a
R_s	67	Ω

applications, it will be necessary to redesign these gate driving circuits and possibly even change the transistors used in the switched capacitor converter. A recommended implementation is an excellent topic for future research.

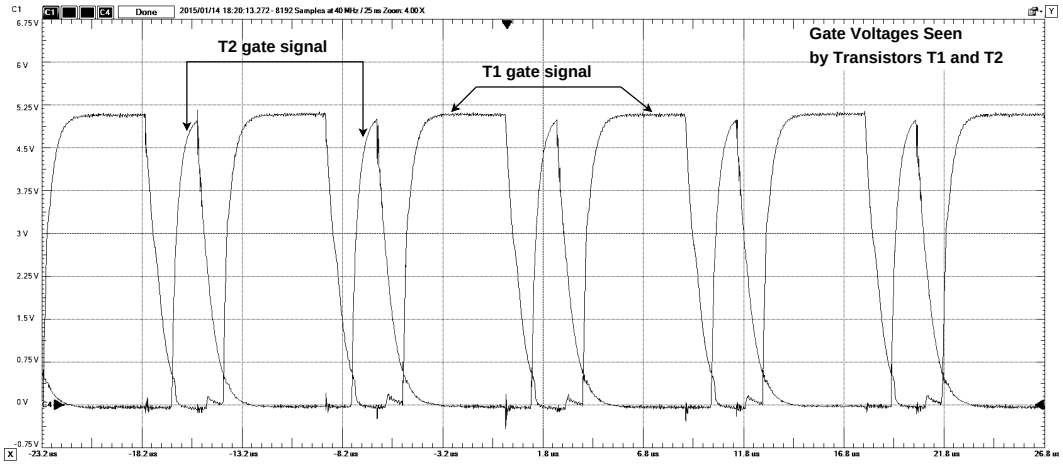


Figure 67: Scope capture presenting the gate voltages seen for both transistors T1 and T2. Each gate driver circuit is connected to the appropriate transistor on the power electronic circuit. Time is on the horizontal axis and voltage is on the vertical axis.

Bibliography

[1] "Primary energy use by source, 2013," in *Monthly Energy Review May 2014*, US Energy Information Administration, 2014.

[2] L. Chaar, "Solar power conversion," in *Power Electronics Handbook* (M. H. Rashid, ed.), 2007.

[3] R. Faranda, S. Leva, and V. Maugeri, "Mppt techniques for pv systems: Energetic and cost comparison," in *Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, 2008 IEEE*, pp. 1–6, July 2008.

[4] F. Liu, Y. Kang, Y. Zhang, and S. Duan, "Comparison of p and o and hill climbing mppt methods for grid-connected pv converter," in *Industrial Electronics and Applications, 2008. ICIEA 2008. 3rd IEEE Conference on*, pp. 804–807, June 2008.

[5] X. Liu and L. Lopes, "An improved perturbation and observation maximum power point tracking algorithm for pv arrays," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 3, pp. 2005–2010 Vol.3, June 2004.

[6] C. W. Tan, T. Green, and C. Hernandez-Aramburo, "Analysis of perturb and observe maximum power point tracking algorithm for photovoltaic applications," in *Power and Energy Conference, 2008. PECon 2008. IEEE 2nd International*, pp. 237–242, Dec 2008.

[7] I. Koren, "Part 6c high-speed multiplication - iii," in *Digital Computer Arithmetic ECE 666*, Retrieved from: http://www.ecs.umass.edu/ece/koren/.

[8] Xilinx, *Spartan-3A/3AN FPGA Starter Kit Board User Guide*, 2008. v1.1.

[9] NXP, *N-channel 30 V 2.1 m logic level MOSFET Product Data Sheet*, 2009. Rev. 01.

[10] R. Coelho, F. Concer, and D. Martins, "A study of the basic dc-dc converters applied in maximum power point tracking," in *Power Electronics Conference, 2009. COBEP '09. Brazilian*, pp. 673–678, Sept 2009.

[11] A. Ramamurthy and S. Bhattacharya, "Optimized digital maximum power point tracker implementation for satellites," in *Telecommunications Energy Conference, 2008. INTELEC 2008. IEEE 30th International*, pp. 1–5, Sept 2008.

[12] C. Cabal, C. Alonso, A. Cid-Pastor, B. Estibals, L. Seguier, R. Leyva, G. Schweitz, and J. Alzieu, "Adaptive digital mppt control for photovoltaic applications," in *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, pp. 2414–2419, June 2007.

[13] F. Boico and B. Lehman, "Study of different implementation approaches for a maximum power point tracker," in *Computers in Power Electronics, 2006. COMPEL '06. IEEE Workshops on*, pp. 15–21, July 2006.

[14] D. Snyman and J. Enslin, "Combined low-cost, high-efficient inverter, peak power tracker and regulator for pv applications," in *Power Electronics Specialists Conference, 1989. PESC '89 Record., 20th Annual IEEE*, pp. 67–74 vol.1, Jun 1989.

[15] P. Wolfs and L. Tang, "A single cell maximum power point tracking converter without a current sensor for high performance vehicle solar arrays," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, pp. 165–171, June 2005.

[16] P. Midya, P. Krein, R. Turnbull, R. Reppa, and J. Kimball, "Dynamic maximum power point tracker for photovoltaic applications," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, vol. 2, pp. 1710–1716 vol.2, Jun 1996.

[17] I.-S. Kim and M.-J. Youn, "Single-loop maximum power point tracker with fast settling time," in *Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of IEEE*, vol. 1, pp. 862–866 Vol. 1, Nov 2004.

[18] D. Brunelli, C. Moser, L. Thiele, and L. Benini, "Design of a solar-harvesting circuit for batteryless embedded systems," vol. 56, pp. 2519–2528, Nov 2009.

[19] V. Pacheco, L. Freitas, J. Vieira, E. Coelho, and V. Farias, "Stand-alone photovoltaic energy storage system with maximum power point tracking," in *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, vol. 1, pp. 97–102 vol.1, Feb 2003.

[20] K.-Y. Lee, J.-H. Niu, and G.-W. Lin, "A simplified analog control circuit of a maximum power point tracker," in *Photovoltaic Specialists Conference, 2008. PVSC '08. 33rd IEEE*, pp. 1–3, May 2008.

[21] A. Muhtaroglu, "A novel digital mppt control architecture for renewable system integration," in *Sustainable Energy Technologies (ICSET), 2010 IEEE International Conference on*, pp. 1–4, Dec 2010.

[22] W. Teulings, J. Marpinard, A. Capel, and D. O'Sullivan, "A new maximum power point tracking system," in *Power Electronics Specialists Conference, 1993. PESC '93 Record., 24th Annual IEEE*, pp. 833–838, Jun 1993.

[23] P. Peter and V. Agarwal, "Switched capacitor dc-dc converter based maximum power point tracking of a pv source for nano satellite application," in *Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE*, pp. 002604–002609, June 2010.

[24] M. Veerachary and K. Shinoy, "V2-based power tracking for nonlinear pv sources," vol. 152, pp. 1263–1270, Sept 2005.

[25] R. Pilawa-Podgurski, W. Li, I. Celanovic, and D. Perreault, "Integrated cmos dc-dc converter with digital maximum power point tracking for a portable thermophotovoltaic power generator," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, pp. 197–204, Sept 2011.

[26] J. Cooley and S. Leeb, "Per panel photovoltaic energy extraction with multilevel output dc-dc switched capacitor converters," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, pp. 419–428, March 2011.

[27] I. Lee, S. Bang, D. Yoon, M. Choi, S. Jeong, D. Sylvester, and D. Blaauw, "A ripple voltage sensing mppt circuit for ultra-low power microsystems," in *VLSI Circuits (VLSIC), 2013 Symposium on*, pp. C228–C229, June 2013.

[28] T. Esram and P. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," vol. 22, pp. 439–449, June 2007.

[29] D. Hohm and M. Ropp, "Comparative study of maximum power point tracking algorithms using an experimental, programmable, maximum power point tracking test bed," in *Photovoltaic Specialists Conference, 2000. Conference Record of the Twenty-Eighth IEEE*, pp. 1699–1702, 2000.

[30] V. A. Pradeep K. Peter, "Design and analysis of a buck switched capacitor dc-dc converter." Unpublished: obtained via personal correspondence, 2011.

[31] P. T. Krein, *Elements of Power Electronics*. Oxford University Pres, 1 ed., 1997.

[32] D. A. Patterson and J. L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*. Morgan Kaufmann, 4 ed., 2011.

[33] Xilinx, "Spartan-3an fpga family: functional description," in *Spartan-3AN FPGA Family Data Sheet*, 2014. Version 4.2.

[34] Linear Technology Corporation, *LTC1407-1/LTC1407A-1 Serial 12-Bit/14-Bit, 3Msps Simultaneous Sampling ADCs with Shutdown*. Revision: B (12/09).

[35] Digilent, *Digilent Pmod Interface Specification*, 2011. Revision: November 20, 2011.

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