2008

PROPORTIONAL FEEDBACK CONTROL OF DUTY CYCLE FOR DC HYBRID ACTIVE POWER FILTER

Govind N. Malleichervu
University of Kentucky, govindma@gmail.com

ABSTRACT OF THE THESIS

PROPORTIONAL FEEDBACK CONTROL OF DUTY CYCLE FOR DC HYBRID ACTIVE POWER FILTER

This thesis deals with the design and implementation of a feedback control scheme for a DC Hybrid Active Power Filter used to filter harmonics from a Switched Reluctance Motor (SRM) Drive load. Power electronic systems are non-linear & dynamic [1,3,5]. Power electronic systems employ switching circuits to maximize their efficiency at the penalty that switching circuits generate electrical noise called ripple current and voltage or conducted electromagnetic interference (EMI). The ripple current drawn by the power electronic systems needs to be attenuated to an acceptable level. Filters attenuate this to an acceptable level. Traditionally filters with passive inductors and capacitors are used. Active filters contain switching elements in addition to passive inductors and capacitors which reduce overall size of passive components used.

Two control approaches, full-state state space, and plain proportional feedback, are evaluated for this filter. Circuit models are simulated in SPICE and mathematical models are simulated in Matlab/Simulink for evaluating these control approaches. Proportional feedback control was chosen for implementation and the reason for this is provided in the thesis. The active filter was tested with chosen feedback control and experimental results were compared with simulation results. Inferences and scope for further work are finally presented.

Keywords: Hybrid active power filter (HAPF), Switched Reluctance Motor (SRM), harmonics, feedback control, pulse width modulation (PWM).

GOVIND N. MALLEICHERVU

August 29, 2008

PROPORTIONAL FEEDBACK CONTROL OF DUTY CYCLE FOR DC HYBRID ACTIVE POWER FILTER

By
Govind N. Malleichervu
Lexington, Kentucky

Dr. Lawrence E. Holloway
Director of Thesis

Dr. Yu Ming Zhang
Director of Graduate Studies

August 29, 2008

RULES FOR THE USE OF THESIS

Unpublished theses submitted for the Master's degree and deposited in the University of Kentucky Library are as a rule open for inspection, but are to be used only with due regard to the rights of the authors. Bibliographical references may be noted, but quotations or summaries of parts may be published only with the usual scholarly acknowledgements.

Extensive copying or publication of the dissertation in whole or in part also requires the consent of the Dean of the Graduate School of the University of Kentucky.

A library that borrows this project for use by its patrons is expected to secure the signature of each user.

Name Date

_____

_____

_____

_____

_____

_____

_____

_____

THESIS

Govind N. Malleichervu

The Graduate School

University of Kentucky

2008

PROPORTIONAL FEEDBACK CONTROL OF DUTY CYCLE FOR DC HYBRID ACTIVE POWER FILTER

THESIS

A thesis submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering in the
College of Engineering at the University of Kentucky

By
Govind N. Malleichervu

Director: Dr. Lawrence E. Holloway, Associate Professor of Electrical Engineering
Lexington, Kentucky
2008

ACKNOWLEDGEMENTS

I am very thankful to my advisor, Dr. Arthur V. Radun, for his continuous support and guidance in my thesis work. I am also grateful for his professional guidance and for giving me an opportunity to work as a graduate Research Assistant. I am in awe of his acumen in the field of my thesis research and his technical aptitude with laboratory test work. Lastly, I appreciate his assistance in summarizing and shaping this thesis.

I am also thankful to Dr. Bruce L. Walcott for his perennial and generous assistance in my thesis work and for his willingness to serve on my thesis committee. In addition, I thank Dr. Lawrence E. Holloway for his willingness to serve on my thesis committee. I also thank him for aiding me with setting up a shipping account for obtaining parts for my thesis testing.

I am grateful to Dr. YuMing Zhang and the staff of the Department of Electrical and Computer Engineering at the University of Kentucky for their assistance throughout my stay as a graduate student.

I would like to thank Xiaohu Feng for his help during the initial stages of this project. Finally, I would like to thank my friend Weston Johnson for helping me throughout my master's program and for providing valuable tips towards completing my thesis.

I would like to specially thank Ilka Balk for aiding me in my summer internship search which led me to an internship in Germany with Robert Bosch GmbH.

I would like to thank my family and friends for their unrelenting support throughout my master's program. Last but not the least; I would like to thank the Almighty for giving me courage and helping me complete my master's program.

Table of Contents

List of Tables

List of Figures

List of Files

1. MalleichervuGovind_MSThesis.pdf

1 Introduction

This thesis deals with the design and implementation of a feedback control scheme for a DC Active Power Filter used to filter out harmonics from a Switched Reluctance Motor (SRM) Drive load. References [1], [3] & [5] highlight that any power electronic system is a non-linear dynamic system. In addition, power electronic systems employ switching circuits to maximize their efficiency at the penalty that the switching circuits generate electrical noise called ripple current and voltage or conducted electromagnetic interference (EMI). The ripple current drawn by the power electronic systems needs to be attenuated to an acceptable level.

Filters are used to attenuate the power electronic input ripple current to an acceptable level. Traditionally passive low-pass filters using power inductors and capacitors are used. These filters can be large in switched reluctance motor drives when the filter must filter low frequency components caused by the rotation of the machine. An active filter containing switching elements in addition to passive inductors and capacitors can be used to reduce the overall size of passive components used.

These active filter switching elements can be power MOSFETs, insulated gate bipolar transistors (IGBTs) or any other kind of switch. Because the switching elements switch at a frequency with a period that is short compared to the time constants of the power electronics system they can be replaced with an equivalent circuit model [10, 11] for control analysis. The equivalent circuit model is called an average model of the original non-linear power electronic system and the added active filter. This average model is still nonlinear and thus it must be linearized around a steady-state DC operating point for small signals [1, 11] so that the resultant small signal system is linear. Now, linear control theory can be applied to obtain a desired system response.

In this thesis the following two control approaches, full-state state space feedback, and plain proportional feedback, are evaluated for the active filter. Circuit based models are simulated in SPICE and mathematical based models are simulated in Matlab/Simulink to evaluate the control approaches. Based on the results from these simulations, proportional

feedback control was chosen for implementation. The reason for this selection is provided in the thesis. The active filter with proportional feedback control is tested and the experimental results are compared with simulation results. Inferences and scope for further work are finally presented.

1.1 Background

According to Reference [4] a filter is "*a device that passes electric signals at certain frequencies or frequency ranges while preventing the passage of others*". Reference [7] says that a filter is an electric circuit system which alters the amplitude and/or phase characteristics of a signal with respect to frequency. Reference [7] classifies filters broadly into passive, active and switched capacitor filters. References [4] and [7] state that an active filter includes components such as switching elements, i.e. active elements in addition to traditional passive elements such as capacitors, inductors and resistors. The latter three form the building blocks of passive filters. Reference [7] lists the benefits of passive filters in terms of simple transfer function implementation, absence of external bias sources for switching elements in active filters and low noise generation. Conversely, the drawbacks of passive filters are the absence of signal gain (amplification) and the cost of precision made passive elements. However, precision in passive power filter elements is rarely a concern due to the bigger size of inductances and capacitances used owing to the requirement of low frequency attenuation. Passive power filters can cause resonance, need large components if the frequencies being filtered are low, which can be impractical. Due to these drawbacks passive power filters may not be able to meet the stringent regulatory requirements [24]. Active filters benefit from the use of amplifying elements such as power switching elements. The biggest advantage of using such amplifying elements is the reduction in the size of the passive elements used, such as capacitors and inductors. This helps in reducing the size, weight, and cost of power filters. A common approach used to make an active power low pass filter is to generate the required current or voltage to cancel the harmonic current or voltage generated by a non-linear load [24].

All of the above mentioned filters can be further classified based on the frequency of signal attenuation as low pass, high pass, all pass and band pass filters among numerous others. A number of books are available to cater to most filter design applications and we avoid digressing.

Advances in semiconductor technology have been the fuel for revolutions in power electronic circuits also called switching circuits. References [1, 8, 24, 25] indicate that power electronics based systems are ubiquitous and their use will only increase in the coming years because of their high efficiency compared to other power control methods. Commonly used power electronic systems include ac and dc motor drives, uninterruptible power supplies (UPSs), ac to dc converters among others. References [1, 3, 24] highlight that such power electronic systems are non-linear dynamic systems. A motor drive, which incorporates switching elements like bipolar transistors, MOSFETs, IGBTs, diodes in addition to transformers, capacitors and inductors, is a perfect example of a non-linear system. In an ideal case there would be no resistances in a power electronic system enabling it to be 100% efficient. However, resistances creep into the system as equivalent series and parallel resistances for capacitors and inductors, junction resistances for semiconductor switches and resistances in connecting wires. These lead to voltage drops and eventually reduce the power electronic system's power transfer efficiency. Though power-electronic systems offer various benefits in terms of efficiency, lower cost of operation and more control options, they add noise into the electric system they are connected to. This is due the presence of their switching elements. The result of using these power electronic systems is the generation of ripple currents and voltages. Observation of the power electronic circuit voltage and current switching waveforms reveals they are made up of an infinite number of harmonic components of the fundamental switching frequency often called ripple or conducted electromagnetic interference (EMI) [9]. In power electronic systems powered from a DC source the power transferred contains the DC or power frequency component, plus the harmonics generated by the switching of the power semiconductors. The other harmonics are considered as conducted EMI, which must be prevented from entering the DC power supply [9].

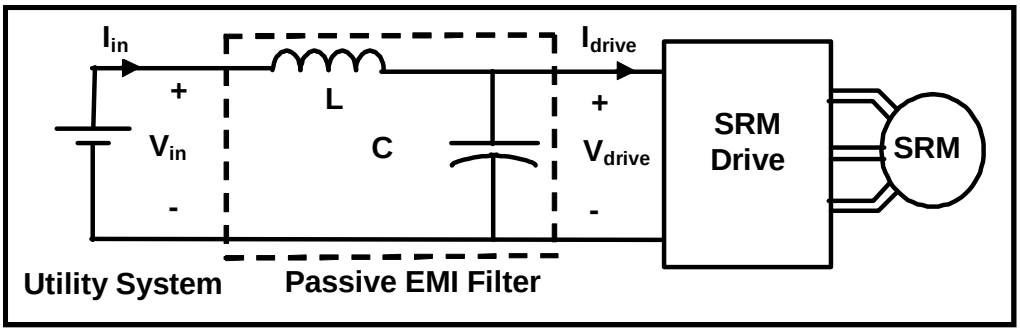


Figure 1.1 A typical SRM motor drive system

Current related interferences entering the input side and voltage related interference entering the output side of the power electronic system are common characteristics of DC-DC converters [8]. The switched reluctance motor (SRM) and motor drive system operating from a DC source such as in an automobile or future aircraft that is the subject of this thesis is shown in Figure 1.1. However, these can be replaced by any other motor and drive. The goal of thesis is to design a DC active power filter for SRM Drive to replace and reduce the size of the conventional passive EMI filter.

1.1.1 A SRM Motor and Drive System

A SRM is a novel synchronous machine [13]. It is referred to as a *doubly salient machine* as both the stator and rotor have salient poles. The stator contains winding similar in construction to the field windings of a DC motor. The windings are concentrated around the stator poles. The rotor has no coils or magnets.

A SRM with 8 stator poles and 6 rotor poles, also called a four phase SRM, is shown in Figure 1.2. The sequential turn-on and turn-off of the current in the windings around the stator pole pairs result in the production of torque to move the rotor. The blue and green dots beside the stator pole pair in Figure 1.2 indicate that this stator pole pair must be energized or turned on in order to produce torque or rotation of the rotor poles towards the energized stator poles in the counter-clockwise direction.

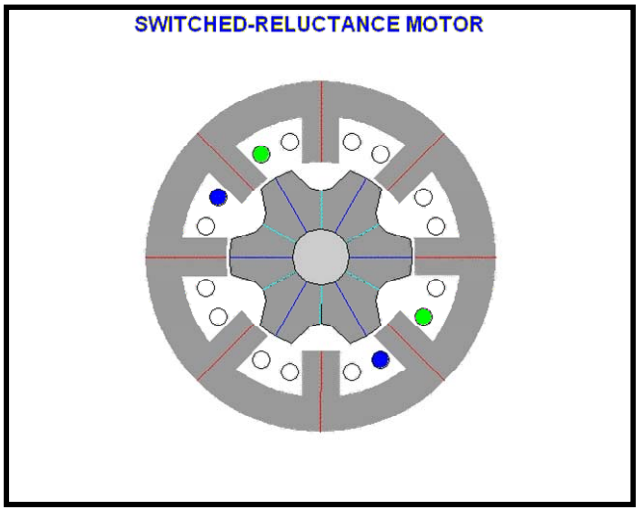


Figure 1.2 An 8/6 SRM Configuration (Source, http://www.ece.umn.edu/users/riaz/animations/switchrel.html)

A SRM thus requires a high frequency dc switching input power supply. However, the power available in Figure 1.1 is a constant DC power supply. A system known as an inverter or motor drive and specifically in this case, a SRM drive, converts the input DC into the pulsating current in the various SRM windings as the SRM rotates. The SRM inverter is a switching circuit and thus it is a nonlinear system. The SRM is also a non-linear system as the result of its salient poles and due to the significant saturation of the magnetic iron that is characteristic of SRMs. Thus both the SRM and the SRM inverter introduce harmonics into the DC utility system. These harmonics can be multiples of the switching frequency of any of the switching elements and of the motor speed.

Figure 1.1 shows the utility system being a dc source. If the SRM drive system can be thought of as emulating a resistor (ideally) to this DC source, the current drawn by the drive would be a perfect dc current. However, the harmonics generated by the drive and motor constitute a significant amount of input current noise. The deviation of the input current from dc, is called ripple current. Another way to visualize this effect is through the Fourier transform of the input current. A dc current would give a fundamental component (zeroth harmonic) without any additional components. However, in reality, there will be a number of additional harmonics produced that are multiples of the fundamental frequency that constitutes the input ripple current.

To reduce the SRM motor drive input harmonics drawn from the DC power supply, filters are incorporated. A traditional filter is constructed using a capacitor and an inductor as shown in Figure 1.1. The filter attenuates the noise generated by the load (input current ripple or conducted EMI) and drawn from the power supply. This thesis develops an active dc power filter to replace this passive filter to obtain a filter with smaller size and weight.

1.2 Literature Review

The active input DC filter for a SRM drive that is the subject of this thesis is for an aerospace application. Reliable and precise filtering of dc supplies in aerospace applications (aircraft or spacecraft) is an important consideration in establishing the overall integrity of the power system.

Switching power inverters and converters (in this case a SRM drive) generate ripple. They typically require input and output filtration to meet ripple and electromagnetic interference (EMI) specifications. In addition, the temperature and high reliability demands (aerospace applications) of filter capacitors present tough design constraints. Use of active filters [15 – 22, 24] ensures that these constraints are met with relative ease.

The conventional filter in Figure 1.1 using a capacitor and inductor is termed an L-section filter [14]. An L-section filter is a passive filter. The main benefit of such a passive filter is the simplicity of its circuitry. An active filter on the other hand will use more components and is a more complex circuit, but offers the benefit of a reduction in the size of passive components used and thus a reduction in the size of the overall filter. In addition, an active filter has better attenuation and a wider bandwidth, which are useful when used with converters having a wide range of switching frequencies. References [1], [15 – 22, 24, 25] encompass the progress of active power filter implementation techniques over the last 20 years.

Integration of a base passive filter with an active section leads to greater benefits in terms of signal attenuation [15, 16]. Such an integrated filter is termed a hybrid active power filter [17 – 19, 21 – 22]. Hybrid active power filters (HAPFs) use transistors, IGBTs or

MOSFETs for the active section of the hybrid filter. Op-amps are not used due to efficiency, amplitude, and power limitations. Operational amplifier based active power filters have low efficiency because the op-amps are in the linear region all the time. Therefore the power loss in such circuits is much greater than that of circuits with switching elements such as IGBTs or MOSFETs [17]. Of all switching elements available, for low voltage applications (less than 1000V), MOSFETs are the fastest switch in terms of switching speed. The switching times are in the order of a few tens of nanoseconds to a few hundred nanoseconds [1]. A comparison chart of the various available switching elements is shown in Table 1.1 [1]. Active power filters can be classified based on their configuration and this classification is shown in Figure 1.3.

Table 1.1 Relative properties of controllable switches

Device	Power Capability	Switching Speed
MOSFET	Low	Fast
IGBT	Medium	Medium
BJT/MD	Medium	Medium

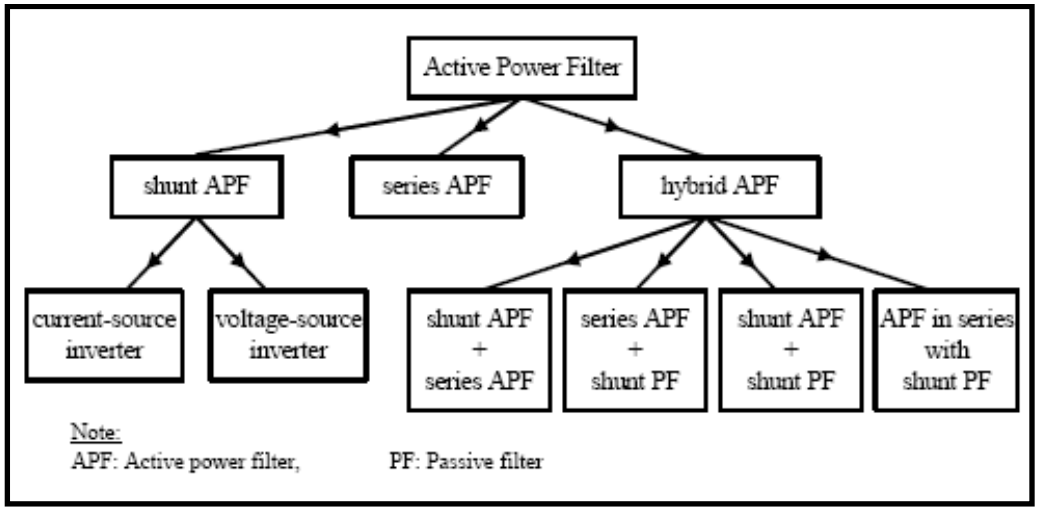
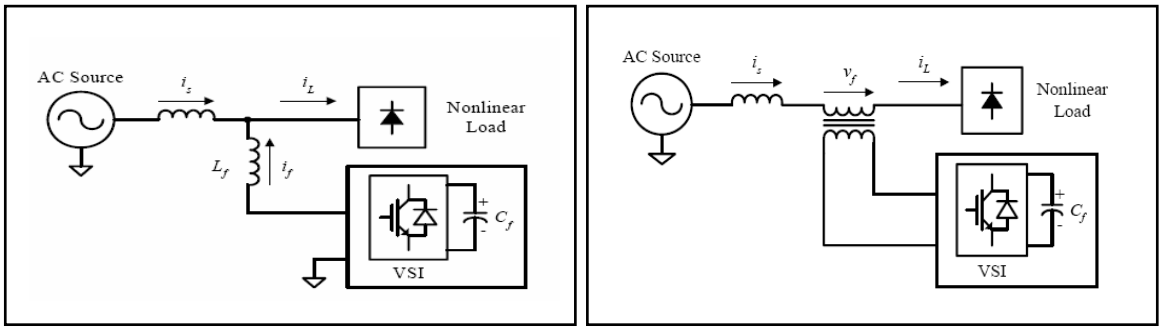


Figure 1.3 Active Power Filter Classification (Source, Reference [24])

A shunt active power filter uses an active section in parallel with the non-linear load and a series active power filters uses an active section is series with the non-linear load. Figure 1.4 shows shunt and series filter topologies as (a) and (b) respectively. Of the two, the shunt APF topology is preferred over the series APF. This is due to the power loss in the series APF [17 – 18]. However, both these configurations introduce switching frequency noise into the utility systems due to the switching elements in their active section and need additional filtering to prevent interference.



(a) Shunt APF **(b) Series APF**

Figure 1.4 Shunt and Series APFs (Source, Reference [24])

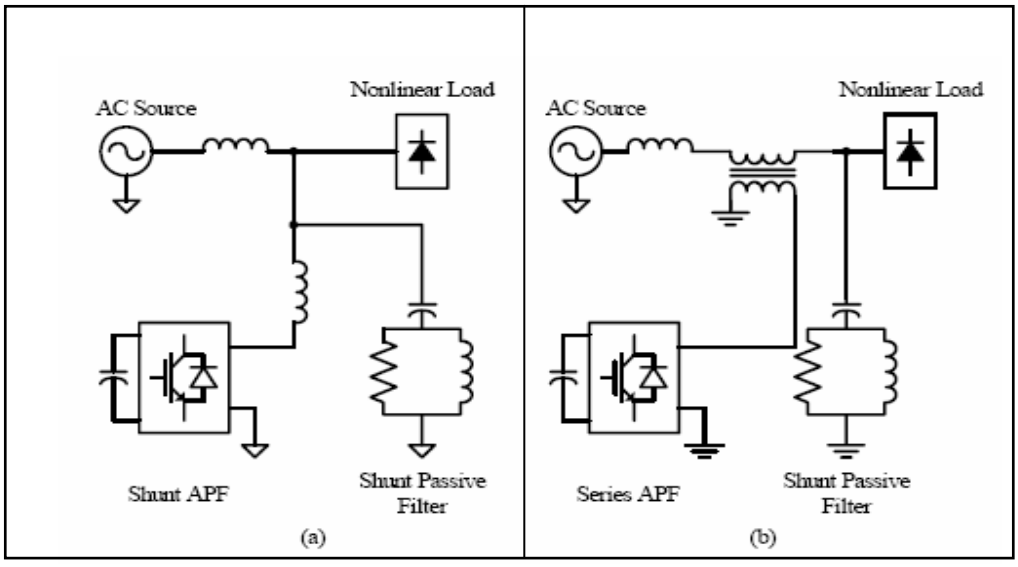


Figure 1.5 Hybrid APF Topologies (Source, Reference [24])

Therefore the hybrid active filter is used. Also Figure 1.5 shows shunt and series connected hybrid APF topologies as (a) and (b) respectively.

In a hybrid active power filter, a passive filter is coupled with an active filter section (high frequency switching circuit) for ripple attenuation in addition to mitigating interference.

"The passive filter limits the ripple to a level that is manageable by the active circuit and to attenuate ripple components that fall beyond the bandwidth of the active circuit. The active filter circuit cancels or suppresses the low-frequency ripple components that are most difficult to attenuate with a passive low-pass filter. This approach permits a substantial reduction in the passive filter size, with potential benefits in converter size, weight, and cost" [21].

The most commonly used forms of hybrid active power filters are the last two configurations in Figure 1.3 (also shown in Figure 1.5). DC active power filter employed on the DC side is one of the best effective techniques to eliminate current ripple when compared to DC passive filters [17]. The active control of this ripple voltage (series active) or current (shunt active) can be done using feed-forward [6, 21] or feedback [1, 2, 15, 17 – 20, 22] control loops. A combination of both can also be done. A feed-forward filter creates an exact (or almost) copy of the ripple voltage or current of magnitude opposite to the actual ripple. Theoretically these two ripples would cancel out and ensure that the input is pure dc. Due to inaccuracies in the components and minute losses there would still be some ripple in the final system.

However, the magnitude of this is much lower than that without a filter. On the other hand feedback filters use high gain error feedback [21]. Novel control schemes with high efficiency in attenuation have been proposed for specialized applications [17 – 18]. Further information on the classification of active power filters and proposed control schemes can be found in [24 – 28], especially [26].

1.3 Proposed Active Filter

The proposed active power filter that is the subject of this thesis is as shown in Figure 1.6.

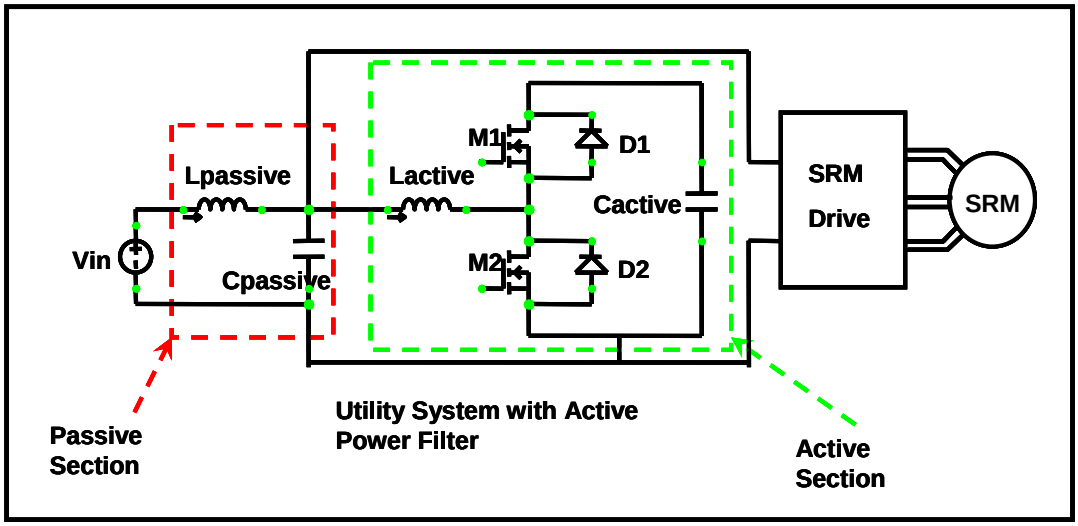


Figure 1.6 Power EMI filter with active power filter

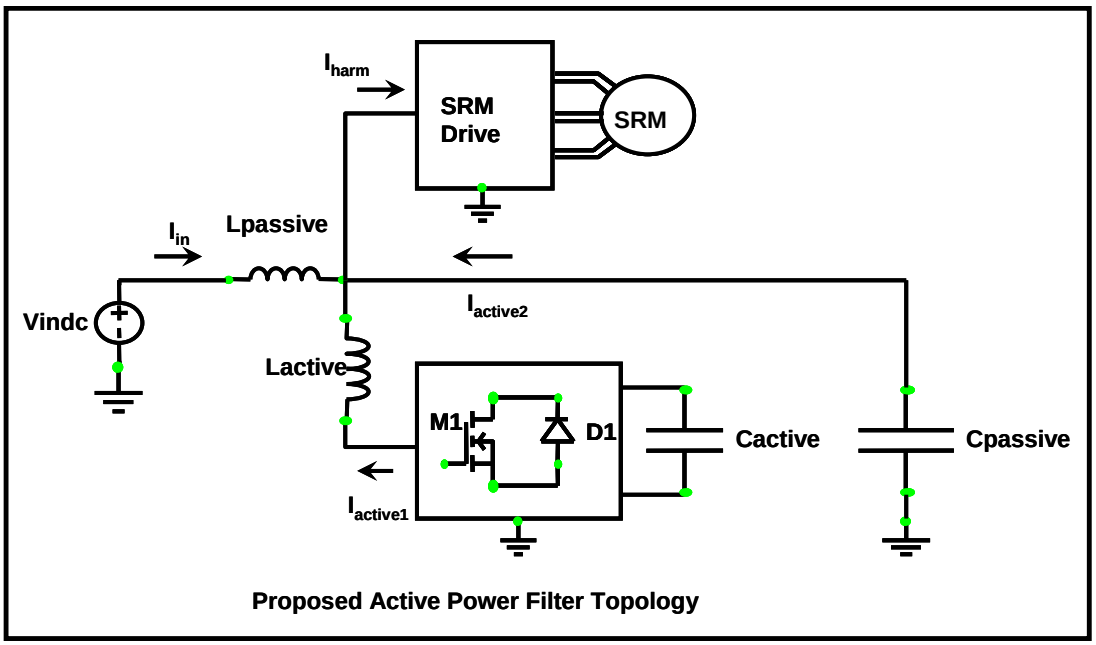


Figure 1.7 Proposed Active Power Filter Topology

The active and passive sections in Figure 1.6 are marked off using green and red outlines respectively. It is a slightly different form of shunt novel hybrid filter since two different filter systems are integrated. A DC passive capacitor is used in place of the LRC passive circuit as shown in Figure 1.5. And a DC voltage source is used in the place of an AC source. The proposed topology is shown in Figure 1.7.

Upon comparison to the topologies shown in Figure 1.5, this hybrid filter utilizes the combination of a capacitor (*Cpassive*) and inductors (*Lpassive*) and (*Lactive*) to ensure that the high frequency ripple doesn't enter the power supply. No additional passive elements (combination of resistance, capacitance and inductance) are utilized. This makes modeling of the filter for linear control design a lot easier. The current equation at the only node is given by equation 1.1.

$$I_{harm} = I_{in} + I_{active1} + I_{active2} \quad \textbf{1.1}$$

The goal of the thesis is to design an active filter so that the currents generated by the active section would cancel out the harmonics generated by the harmonic load and to ensure that the current drawn from the input is dc (or almost dc).

The SRM drive is connected in between the hybrid filter and the SRM. Such a topology is termed as shunt connected hybrid active filter as the active filter section is connected in parallel to the passive filter capacitor. Again, this topology is chosen as it has very low losses when compared to series connected active filters [17 – 18]. Shunt connected filters are good for ripple current compensation and series connected filters for ripple voltage compensation [19].

This proposed active power filter is for an aerospace application (actuator motor drive system). Therefore, the demands for components are very high in terms of reliability, temperature of operation and weight. Using complex switching circuitry to reduce bulky capacitors is often used and is the main idea behind this filter design [14]. High frequency inductors and the switching elements are relatively small in size. Research from [2] shows that FPE (Fluorinated Polyethylene) plastic film capacitors are very light, have the highest current carrying capability and meet high operating temperature requirements.

Table 1.2 Comparison of different capacitor topologies (Source, Reference [2])

	X7R	COG (NPO)	FPE	PPS	Al
Tmax °C	200	200	300	150	100
μF / in^3	20	2.86	6.3	2.74	164
μF / lb	66	9.4	80	54.8	1,680
Arms / μF	5.4	70	10	1.01	3.55e-3
Arms / in^3	108	200	40	2.77	0.582
Arms / lb	356	658	800	55.4	5.95

Operating voltages in aerospace application is 270V for capacitors [2]. Due to this voltage rating, capacitors tend to be relatively larger in size. This adds significant weight. Therefore size reduction is emphasized. Table 1.2 shows a comparison of current high temperature capacitor technologies at a 270V rating.

Even though FPE plastic film capacitors are the capacitors of choice for implementing the active filter, polypropylene plastic film capacitors are used in the experimental implementation of this active filter. This is done because FPE plastic film capacitors are still in development and thus expensive while polypropylene plastic film capacitors are mature and inexpensive. Polypropylene plastic film capacitors are electrically similar to FPE plastic film capacitors though their maximum operating temperature is much lower, about 105°C. In addition, the active filter is designed for a 42V DC voltage rating to eliminate experimental safety issues. This voltage level is under consideration as a new standard for automotive DC voltage to replace the present 12V DC. It should be noted that the design issues and challenges do not depend on this input voltage and the results obtained can be generalized to systems that have similar current levels.

The reduction in the value of the DC capacitance [Appendix A] that is possible using the proposed active filter circuit without feedback control is given in equation 1.2.

$$C_{passive} = \frac{C_{active}}{D^2} \qquad \textbf{1.2}$$

Here, D is the constant duty cycle of the switching elements, MOSFETs. The size of a capacitor is better explained using the energy equation for a capacitor. This is given for the passive filter as

$$E_{passive} = \frac{1}{2} \cdot C_{passive} \cdot V_{passive}^{\ 2} \quad \textbf{1.3}$$

Using the average switching circuit analysis technique [10 – 12], the following relations are used [23].

$$V_{passive} = D \cdot V_{active} \quad \textbf{1.4}$$

$$E_{active} = \frac{1}{2} \cdot C_{active} \cdot V_{active}^{\ 2} \quad \textbf{1.5}$$

$$E_{active} = \frac{1}{2} \cdot \left(D^2 \cdot C_{passive}\right) \cdot \left(\frac{V_{passive}}{D}\right)^2 = \frac{1}{2} \cdot C_{passive} \cdot V_{passive}^{\ 2} = E_{passive} \quad \textbf{1.6}$$

This shows that the size benefit of using an active filter is defeated when constant duty cycle control is used even though equation 1.2 shows that the capacitor C_{active} looks effectively larger because of its higher voltage rating. Therefore, variable duty cycle control with feedback is proposed.

This brings the question of a benchmark filter against which the proposed active filter can be compared with. A passive filter implemented for an automotive electronic brake system operating at 42V was used as the benchmark [2]. The proposed design in [2] is presented below in Table 1.3 for comparison with the currently proposed filter.

Results from [2] show that the implemented active filter successfully worked in attenuating noise generated by the harmonic source. From Table 1.3 it can be seen that though there was almost no change in the overall system inductance (it in fact increased by 1%), the overall system capacitance was reduced by a factor of more than 6! Using this encouraging result, the following is proposed in the design of a dc active power filter in Table 1.4.

Table 1.3 Comparison between passive and earlier implemented active filter (Source, Reference [2])

	Original values in traditional EMI	Design values in the active filter
The inductor L_{in}	160 μH	160 μH
The capacitor C / C_{out}	16000 μF	1000 μF
The inductor L_A	N/A	1.6 μH
The capacitor C_A	N/A	1600 μF
Total L	160 μH	161.6 μH
Total C	16,000μF	2600 μF

Table 1.4 Proposed dc active power filter summary

System Parameters	Proposed values for dc active power filter
Input inductor Lin/Lp	160μH
Output capacitor Cout/Cp	400μF
Active inductor La	1.6μH
Active capacitor Ca	800μF
Overall L	161.6μH
Overall C	1200μF

The goal of this research is to successfully implement a hybrid active filter with an overall capacitance reduction factor of more than 13 when compared to the original passive filter while the inductance remains unchanged. The duty cycle control is implemented through proportional feedback control and full state state-space feedback. The former is ultimately selected for implementation due to the benefits it offers and is duly explained in the design chapter.

1.4 Thesis Outline

This thesis is organized beginning with this chapter, chapter 1, summarizing the thesis goals, giving background information, a summary of relevant previous work, as well as a glimpse of the proposed design approach. This is followed by chapter 2 which describes

the active filter design. In this chapter the circuit and mathematical modeling procedures are explained followed by the feedback design for the two different control schemes. The simulation results help in choosing one of the two control schemes. . Chapter 3 describes the development of systems models and system simulations for the active power filter with chosen control scheme. The results from the system simulations using different simulation environments are presented. This is then followed by chapter 4 that describes the experimental system. This includes device (MOSFET) selection, inductor design, heat sink selection and issues with PWM and gating circuits. Chapter 5 presents results from physical model experiments and compares it to simulation results. Chapter 5 is concluded with inferences and scope for further study. Additional information is presented in the Appendices to avoid digressing from the main thesis topic.

2 Hybrid Active Power Filter Design

2.1 Introduction

This chapter presents design of the hybrid active EMI filter starting with a description of the original benchmark passive EMI filter. The passive filter and proposed hybrid active filter are both designed to attenuate load harmonics arising from a SRM drive. An introduction to SRMs, and the SRM drive model (in Simulink) used in this thesis is also given. The performance of the baseline passive filter with the SRM drive load is provided for comparison with the hybrid active filter's performance. A detailed model of the proposed hybrid active power filter (in Simulink) is presented. This filter's performance under constant duty cycle control is discussed. Based on the results for constant duty cycle control, the desirability of using feedback control is shown. Different feedback control schemes are analyzed and the best is chosen. The chosen feedback control scheme is discussed before concluding this chapter.

2.2 Passive EMI Filter

An input EMI filter is necessary since the SRM drive must meet a conducted EMI requirement. In the case of the aerospace application being addressed here the ripple current drawn from the DC supply is governed by Military STD 461. The original benchmark passive EMI filter is presented in Figure 2.1 [2]. The original passive EMI filter's component values are summarized in Table 2.1.

Table 2.1 Summary of Benchmark Passive EMI Filter Component Values

Filter	Passive EMI Filter
Passive Inductance (Lpassive)	160uH
Passive Capacitance (Cpassive)	16000uF

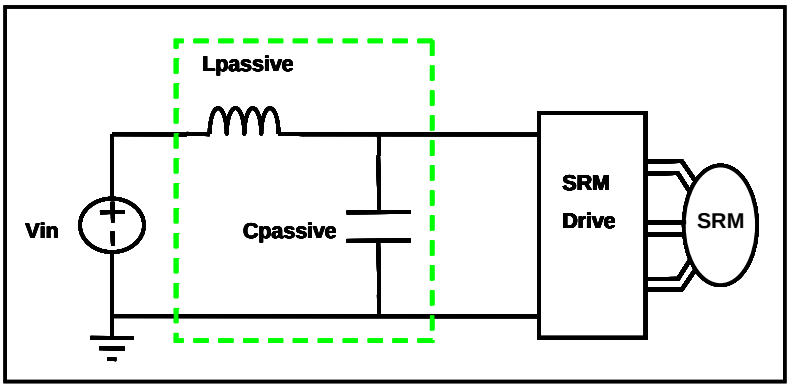


Figure 2.1 Passive EMI Filter

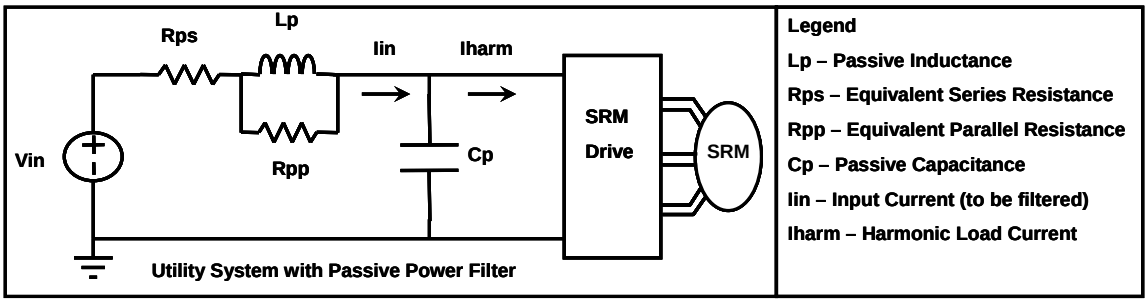


Figure 2.2 Passive EMI Filter Schematic

2.2.1 Analysis of Passive EMI Filter

The passive EMI filter schematic is shown in Figure 2.2. This circuit includes the equivalent series and parallel resistances of the filter's inductor. These are included since they determine the Q or damping of the filter and thus the amount of filter ring that occurs in response to transients.

The above two port circuit is analyzed using circuit equations. Kirchoff's Voltage Law (KVL) and Kirchoff's Current Law (KCL) are employed. First, KVL is applied to the input loop.

$$V_{in} = R_{ps} \cdot \left(I_{lp} + \frac{L_p}{R_{pp}} \cdot \frac{dI_{lp}}{dt} \right) + L_p \cdot \frac{dI_{lp}}{dt} + V_{cp} \qquad \textbf{2.1}$$

$$\frac{dI_{lp}}{dt} = -\frac{R_{ps} \cdot R_{pp}}{L_p \cdot \left(R_{ps} + R_{pp}\right)} \cdot I_{lp} - \frac{R_{pp}}{L_p \cdot \left(R_{ps} + R_{pp}\right)} \cdot V_{cp} + \frac{R_{pp}}{L_p \cdot \left(R_{ps} + R_{pp}\right)} \cdot V_{in} \quad \textbf{2.2}$$

Next, KCL is applied to the only node. This gives

$$\left(I_{lp} + \frac{L_p}{R_{pp}} \cdot \frac{dI_{lp}}{dt}\right) = C_p \cdot \frac{dV_{cp}}{dt} + I_{harm} \quad \textbf{2.3}$$

$$\frac{dV_{cp}}{dt} = \frac{R_{ps}}{C_p \cdot \left(R_{ps} + R_{pp}\right)} \cdot I_{lp} - \frac{1}{C_p \cdot \left(R_{ps} + R_{pp}\right)} \cdot V_{cp} + \frac{1}{C_p \cdot \left(R_{ps} + R_{pp}\right)} \cdot V_{in} - \frac{1}{C_p} \cdot I_{harm} \quad \textbf{2.4}$$

The above equations are written in state space format as shown below.

$$\begin{bmatrix} \frac{dI_{lp}}{dt} \\ \frac{dV_{cp}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-R_{ps} \cdot R_{pp}}{L_p \cdot \left(R_{ps} + R_{pp}\right)} & \frac{-R_{pp}}{L_p \cdot \left(R_{ps} + R_{pp}\right)} \\ \frac{R_{pp}}{C_p \cdot \left(R_{ps} + R_{pp}\right)} & \frac{-1}{C_p \cdot \left(R_{ps} + R_{pp}\right)} \end{bmatrix} \cdot \begin{bmatrix} I_{lp} \\ V_{cp} \end{bmatrix} + \begin{bmatrix} \frac{R_{pp}}{L_p \cdot \left(R_{ps} + R_{pp}\right)} & 0 \\ \frac{1}{C_p \cdot \left(R_{ps} + R_{pp}\right)} & \frac{-1}{C_p} \end{bmatrix} \cdot \begin{bmatrix} V_{in} \\ I_{harm} \end{bmatrix} \quad \textbf{2.5}$$

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_{lp} \\ V_{cp} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_{in} \\ I_{harm} \end{bmatrix} \quad \textbf{2.6}$$

Equations 2.5 and 2.6 have the standard state space equation format shown below.

$$\dot{x} = A \cdot x + B \cdot u \quad \textbf{2.7}$$

$$y = C \cdot x + D \cdot u \quad \textbf{2.8}$$

It is assumed in the state equations that the SRM drive input ripple current (non-linear SRM drive load) and the DC supply voltage (input voltage to the SRM drive) are both inputs to the filter. It should be noted that the DC supply voltage is akin to the bias supply

voltage in an op-amp. The signal input to the passive filter is the harmonic load current (to be filtered). The type of current drawn by the SRM was discussed in detail in section 1.1.1.

2.2.2 Definition of Filter Models

Various models are used in this thesis and for ease of comprehension, these are defined below.

2.2.2.1 Average Model

Average model is a power electronic system model that replaces the semiconductor switches with controlled sources with values that equal the average value over multiple switching cycles of the voltages and currents produced by the semiconductor switches. This model can be simulated in Simulink like or Spice like simulation programs. Being an average model, it runs faster than detailed model (in simulations).

2.2.2.2 Linearized or Small Signal Average Model

This is an average model where the controlled sources have been replaced by their linearized equivalents. This is used extensively for feedback control design.

2.2.2.3 Detailed Model

It is a power electronic system model that replaces the semiconductor switches with ideal switches that switch in zero time and includes mathematical descriptions of control blocks (typical in Simulink environment).

2.2.2.3.1 Detailed Circuit Model

This is a detailed circuit model that includes parasitic components.

2.2.2.4 Circuit Model

This is a circuit schematic based model that uses SPICE like semiconductor models and circuit elements like operational amplifiers and comparators to implement control functions.

2.3 Switched Reluctance Motor (SRM) Drive Model

The SRM drive (non-linear load) is the source of ripple current to be filtered as described in section 1.1.1. It was shown that the SRM drive is necessary to supply the SRM with the required pulsating current and the SRM drive draws current from a DC voltage source.

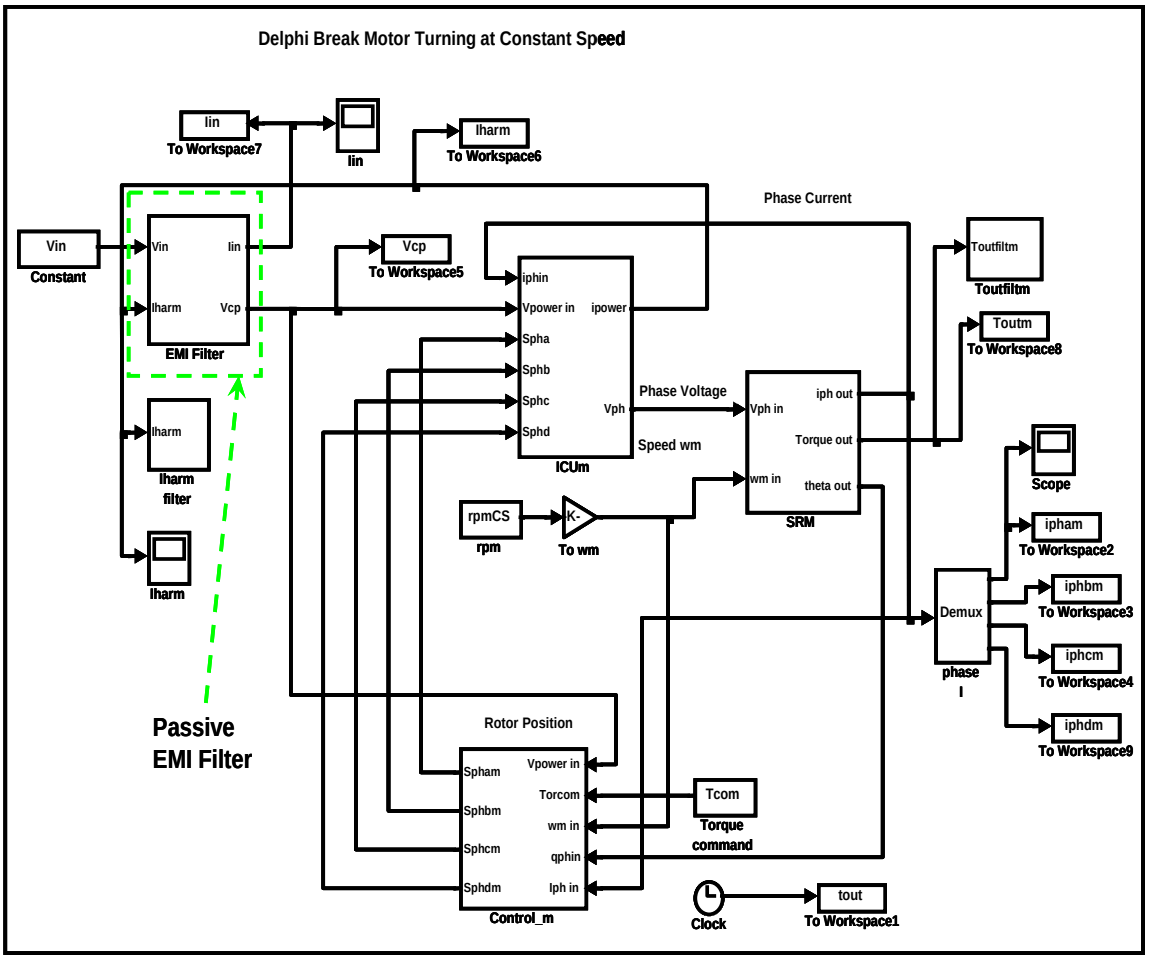


Figure 2.3 Simulink SRM Drive Model with Passive EMI Filter

However, the SRM drive is non-linear and therefore, the current drawn from the DC voltage source will not be a DC current. It includes ripple or noise. The passive EMI filter in section 2.2 reduces this noise or ripple current. To analyze the SRM drive's interaction with the passive EMI filter, a model of the SRM drive is necessary.

A Simulink model of the SRM drive (also used in [2]) is shown in Figure 2.3. It can be seen that the passive EMI filter is included in this model. The Simulink passive EMI filter subsystem uses the state space equation model developed in section 2.2 (shown in Equations 2.1 – 2.6). Comparing the filter model in Equations 2.2 and 2.4 with the Simulink passive EMI filter subsystem shows that the DC voltage source and the harmonic load current are inputs to both. The voltage across the passive capacitor is one output in the passive filter subsystem. Another output is the current through the input passive inductor.

The Matlab m-file that is used to build the filter block is presented in Appendix B. The Simulink passive EMI filter sub-system is shown in Figure 2.4. The current drawn by the non-linear SRM drive, I_{harm} which generates the ripple current drawn from the DC source, is shown in Figure 2.5.

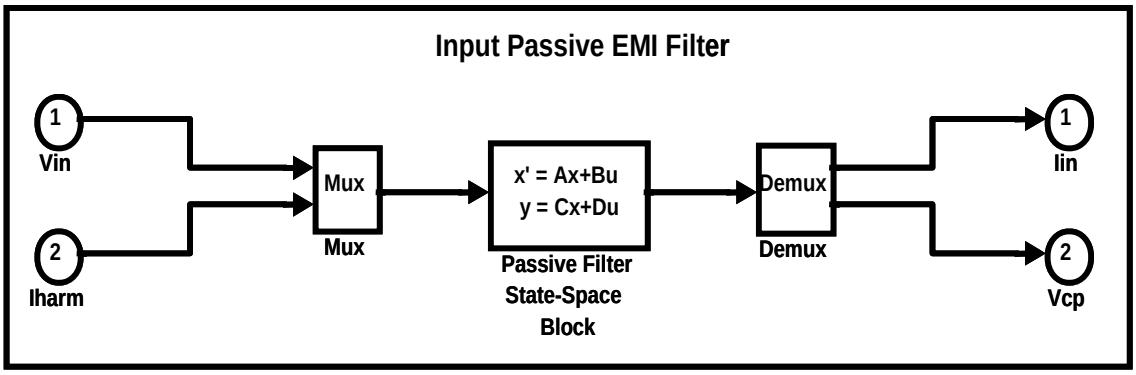


Figure 2.4 Simulink Passive EMI Filter Subsystem

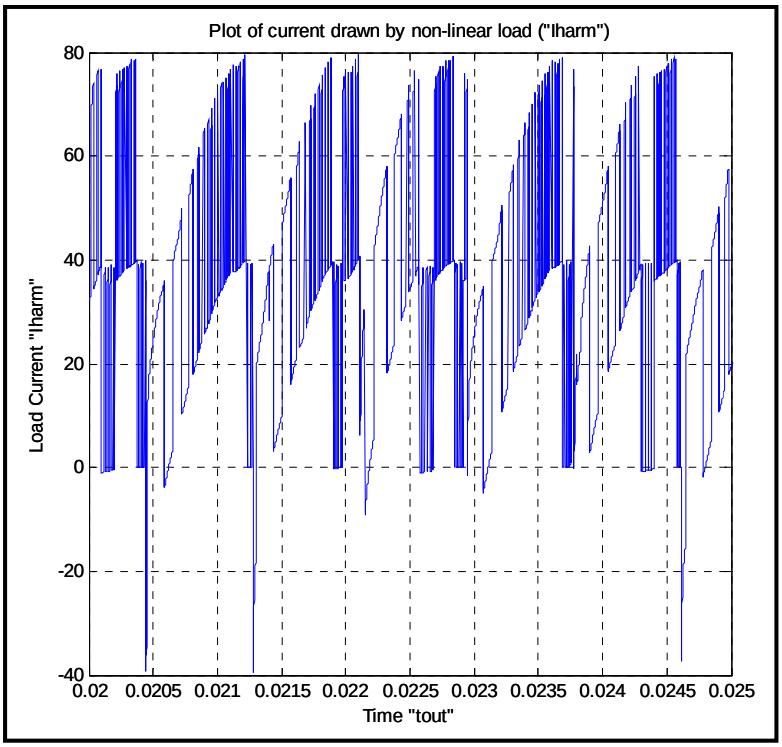


Figure 2.5 Non-linear SRM Drive Load Current

The fundamental frequency **(**F_{fund}) from the above waveform is determined to be approximately 1.2 KHz.

The current "I_{harm}" is defined in Figure 2.2. In the absence of the passive EMI filter (shown in Figure 2.1 & Figure 2.2) this current would be drawn from the DC voltage source (or $I_{in} = I_{harm}$). The ripple in this current waveform is too high and it does not meet the Military STD 461 specification for input ripple.

2.3.1 Passive EMI Filter with SRM Drive

The current drawn from the DC voltage source and the voltage across the passive filter capacitance "C_p" (Figure 2.2) using the passive EMI filter (original benchmark filter) are shown in Figure 2.6. The plot in Figure 2.6 is magnified along the time axis to aid analysis. This magnified plot is shown in Figure 2.7.

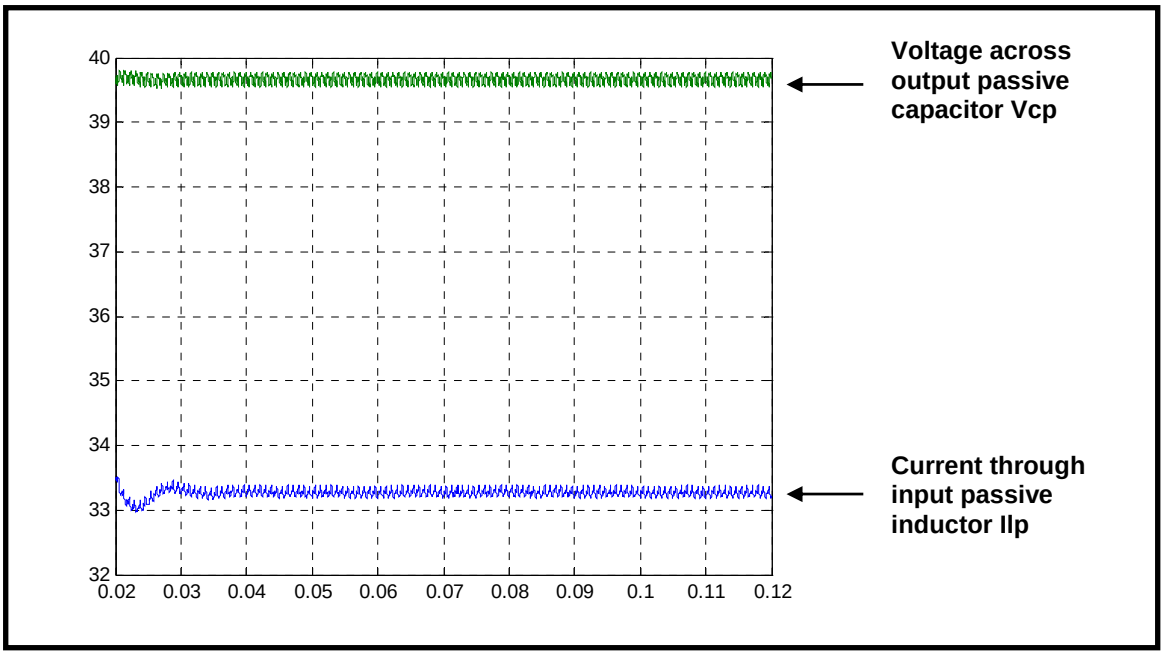


Figure 2.6 Plot of the Voltage "Vcp" and Current "Ilp" for Passive EMI Filter

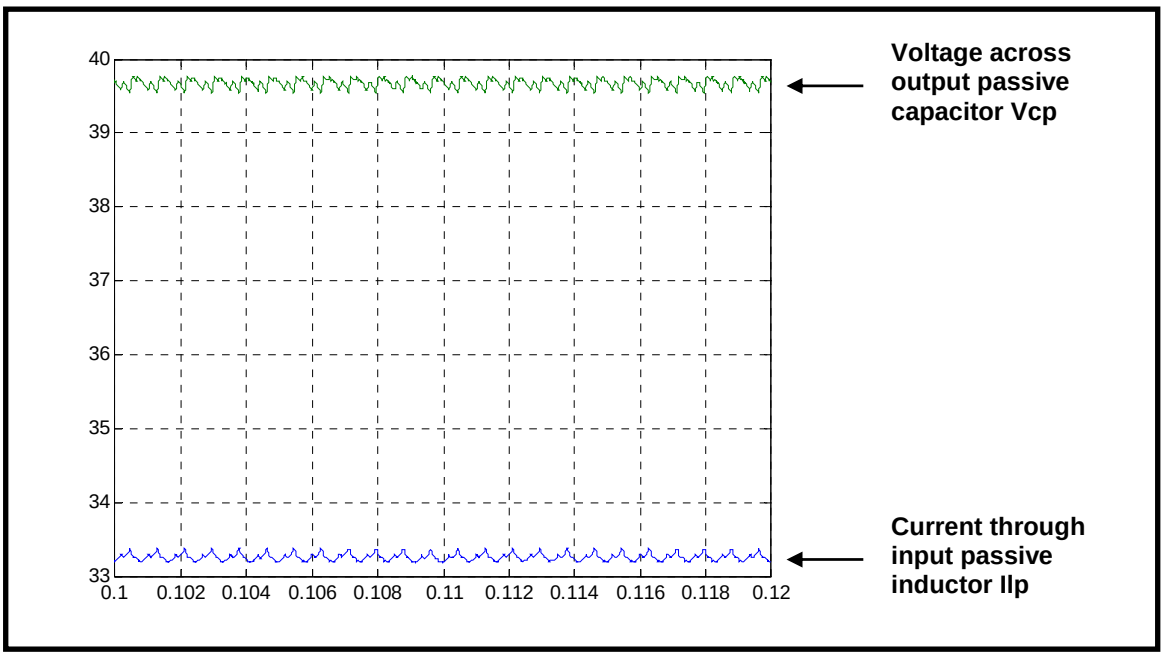


Figure 2.7 Magnified plot of "Vcp" and "Ilp" for Passive EMI Filter

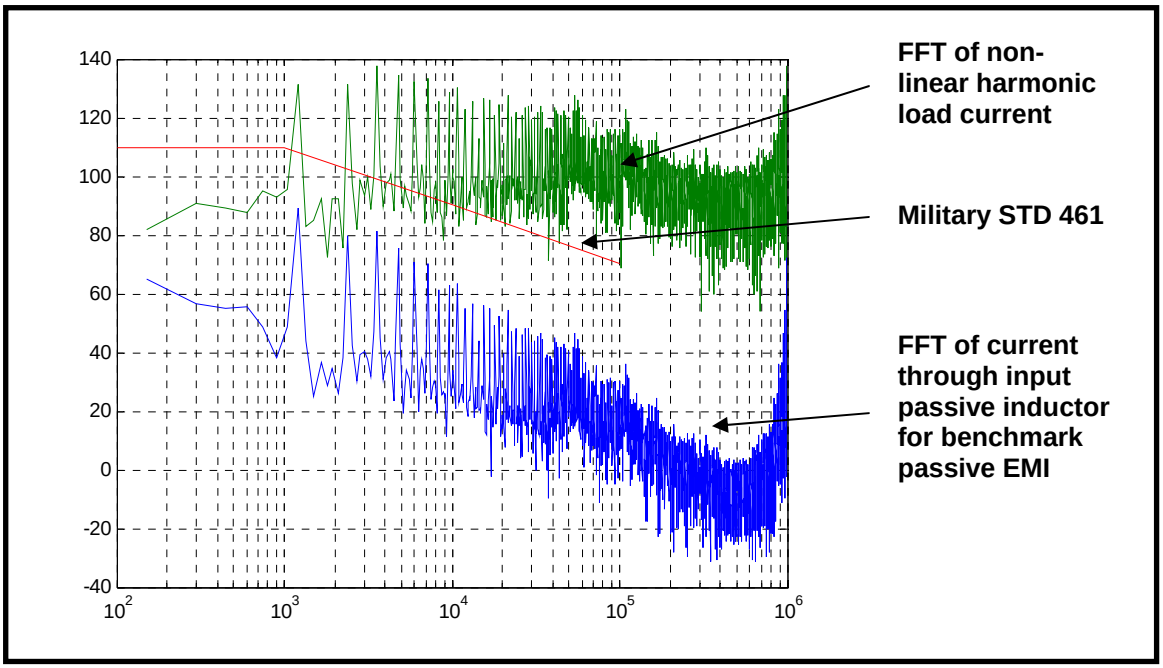


Figure 2.8 Spectrum plot of Military STD 461, Non-linear Load Current (I_{harm}) and Input Current

Now the ripple in the input current is about +- 0.1 A (minimal). The ripple in the voltage across the filter output capacitor is about +- 0.1 V (minimal). The input current's spectrum is found using the m-file presented in Appendix C. The input current spectrum, I_{harm} current spectrum, and Mil STD 461 are plotted in Figure 2.8. The I_{harm} current spectrum (top plot) is outside the MIL. STD. 461 limit. The input current spectrum (bottom plot) in Figure 2.8 lies well within the limit specified by MIL. STD. 461 (middle plot).

2.4 Detailed Model of Hybrid Active Power Filter

The proposed hybrid active filter developed in this thesis is similar to the one developed by [2]. It was stated in [2] that the performance of the active power filter developed there could be improved, as discussed in chapter 1 of this thesis. The components used in the benchmark passive filter, earlier implemented hybrid active filter and the one proposed in this thesis are summarized in Table 2.2. Note that the duty cycle included below is obtained as the averaged value from simulations in Simulink.

Starting with the hybrid active filter topology presented in chapter 1, a detailed circuit model of the filter is developed in this section. The approach is similar to the analysis of the passive filter in section 2.2.

Table 2.2 Summary of Different Filters

Filter Component	Passive EMI Filter	Earlier Active Filter Implementation	Proposed Active Filter
Passive Inductance (Lp)	160uH	160uH	160uH
Passive Capacitance (Cp)	16000uF	1000uF	400uF
Active Inductance (La)	-	1.6uH	1.6uH
Active Capacitance (Ca)	-	1600uF	800uF
Duty Cycle (D)	-	0.333	0.347
Effective Capacitance (Ca/D^2)	-	16000uF (approximately)	6650uF (approximately)

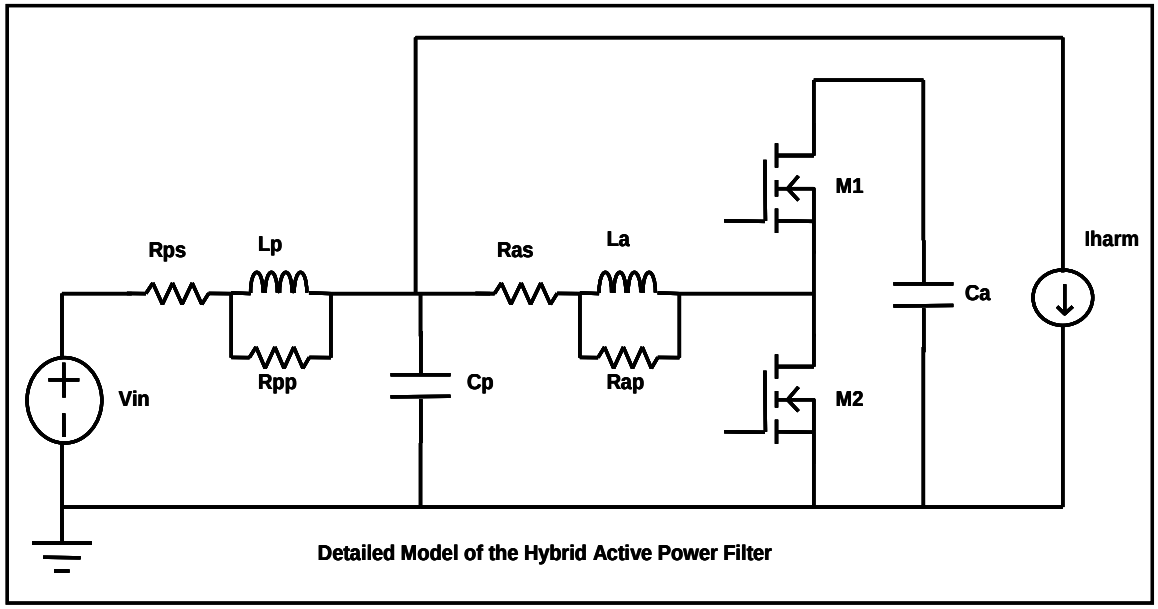


Figure 2.9 Detailed Model of Hybrid Active Power Filter

A circuit oriented approach is used to obtain state space equations describing the filter. These equations are then used to obtain a Simulink model of the filter. This Simulink model of the hybrid active filter is analyzed first as a standalone unit and then added to the SRM model, which generates ripple as seen in section 2.3 and 2.3.1. The hybrid active filter model is described. Then the hybrid active filter, coupled to the SRM Drive (in Simulink) is simulated with a constant duty cycle. Observations from these simulations are presented. Following this, the use of feedback control to improve the hybrid active filter's performance is discussed including different feedback control schemes. The A circuit schematic of the hybrid active power filter used to develop its detailed model is shown in Figure 2.9.

The inductors include an equivalent series resistance (Copper losses) and equivalent parallel resistance (Iron losses). The capacitors in turn are assumed to be lossless. This is based on the type of capacitor selected as explained in section 1.3 and [2]. The harmonic current to be filtered by the filter is modeled as a current source to obtain a standalone model. This is only an assumption for ease of analysis. The harmonic current used is the same one shown in Figure 2.5.

Loop and node equations are written for the circuit in Figure 2.9 using Kirchoff's voltage (KVL) and current laws (KCL). Note that there are two switches in the circuit in Figure 2.9 and equations are written for the two cases when each switch is closed and the other is open. The state of these switches is summarized by the variable S defined by Equation 2.9

$$S = \begin{cases} 0, \text{ upperswitch open, lower switch closed} \\ 1, \text{ upper switch closed, lower switch open} \end{cases} \quad \textbf{2.9}$$

By applying KVL to the input loop

$$V_{in} = R_{ps} \cdot (I_{lp} + \frac{L_p}{R_{pp}} \cdot \frac{dI_{lp}}{dt}) + L_p \cdot \frac{dI_{lp}}{dt} + V_{cp} \quad \textbf{2.10}$$

This gives

$$\frac{dI_{lp}}{dt} = \frac{-I_{lp} \cdot R_{ps} \cdot R_{pp}}{L_p \cdot (R_{ps} + R_{pp})} - \frac{V_{cp} \cdot R_{pp}}{L_p \cdot (R_{ps} + R_{pp})} + \frac{V_{in} \cdot R_{pp}}{L_p \cdot (R_{ps} + R_{pp})} \quad \textbf{2.11}$$

By KCL at the first node

$$I_{lp} + \frac{L_p}{R_{pp}} \cdot \frac{dI_{lp}}{dt} = C_p \cdot \frac{dV_{cp}}{dt} + (I_{la} + \frac{L_a}{R_{ap}} \cdot \frac{dI_{la}}{dt}) + I_{harm} \quad \textbf{2.12}$$

Due to the presence of other derivatives in the above equation, substitution is used to arrive at the final equation which is

$$\frac{dV_{cp}}{dt} = \frac{I_{lp}}{C_p} \cdot \frac{R_{pp}}{(R_{ps} + R_{pp})} - \frac{V_{cp}}{C_p} \cdot (\frac{1}{(R_{as} + R_{ap})} + \frac{1}{(R_{ps} + R_{pp})}) + \frac{I_{la}}{C_p} \cdot \frac{(-R_{ap})}{(R_{as} + R_{ap})} + \frac{V_{ca}}{C_p} \cdot \frac{S}{(R_{as} + R_{ap})} - \frac{I_{harm}}{C_p} + \frac{V_{in}}{C_p} \cdot \frac{1}{(R_{ps} + R_{pp})} \quad \textbf{2.13}$$

By KVL in the second loop

$$V_{cp} = R_{as} \cdot (I_{la} + \frac{L_a}{R_{ap}} \cdot \frac{dI_{la}}{dt}) + L_a \cdot \frac{dI_{la}}{dt} + S \cdot V_{ca} \quad \textbf{2.14}$$

Upon simplification

$$\frac{dI_{la}}{dt} = \frac{V_{cp} \cdot R_{ap}}{L_a \cdot (R_{as} + R_{ap})} - \frac{I_{la} \cdot R_{as} \cdot R_{ap}}{L_a \cdot (R_{as} + R_{ap})} - \frac{S \cdot V_{ca} \cdot R_{ap}}{L_a \cdot (R_{as} + R_{ap})} \quad \textbf{2.15}$$

By KCL at the second node

$$S \cdot (I_{la} + \frac{L_a}{R_{ap}} \cdot \frac{dI_{la}}{dt}) = C_a \cdot \frac{dV_{ca}}{dt} \quad \textbf{2.16}$$

Substituting and simplifying yields

$$\frac{dV_{ca}}{dt} = \frac{S \cdot I_{la} \cdot R_{ap}}{C_a \cdot (R_{as} + R_{ap})} + \frac{S \cdot V_{cp}}{C_a \cdot (R_{as} + R_{ap})} - \frac{S \cdot S \cdot V_{ca}}{C_a \cdot (R_{as} + R_{ap})} \qquad \textbf{2.17}$$

Equations 2.11, 2.13, 2.15 and 2.17 are combined together and represented in standard state space matrix format as shown below in Equation 2.18.

$$\begin{bmatrix} \frac{dI_{lp}}{dt} \\ \frac{dV_{cp}}{dt} \\ \frac{dI_{la}}{dt} \\ \frac{dV_{ca}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-R_{ps} \cdot R_{pp}}{L_p \cdot (R_{ps} + R_{pp})} & \frac{-R_{pp}}{L_p \cdot (R_{ps} + R_{pp})} & 0 & 0 \\ \frac{R_{pp}}{C_p \cdot (R_{ps} + R_{pp})} & \frac{-1}{C_p} \cdot \left(\frac{1}{R_{as} + R_{ap}} + \frac{1}{R_{ps} + R_{pp}}\right) & \frac{-R_{ap}}{C_p \cdot (R_{as} + R_{ap})} & \frac{1 \cdot S}{C_p \cdot (R_{as} + R_{ap})} \\ 0 & \frac{R_{ap}}{L_a \cdot (R_{as} + R_{ap})} & \frac{-R_{as} \cdot R_{ap}}{L_a \cdot (R_{as} + R_{ap})} & \frac{-R_{ap} \cdot S}{L_a \cdot (R_{as} + R_{ap})} \\ 0 & \frac{1 \cdot S}{C_a \cdot (R_{as} + R_{ap})} & \frac{R_{ap} \cdot S}{C_a \cdot (R_{as} + R_{ap})} & \frac{-S \cdot S}{C_a \bullet (R_{as} + R_{ap})} \end{bmatrix} \cdot \begin{bmatrix} I_{lp} \\ V_{cp} \\ I_{la} \\ V_{ca} \end{bmatrix} + \begin{bmatrix} \frac{R_{pp}}{L_p \cdot (R_{ps} + R_{pp})} \\ \frac{1}{C_p \cdot (R_{ps} + R_{pp})} \\ 0 \\ 0 \end{bmatrix} \cdot V_{in} + \begin{bmatrix} 0 \\ \frac{-1}{C_p} \\ 0 \\ 0 \end{bmatrix} \cdot I_{harm} \qquad \textbf{2.18}$$

The switch state variable, S makes the above system of equations for the detailed model of the active power filter non-linear in nature. These equations are implemented in a MATLAB m-file. This m-file is used in Simulink to obtain a detailed model of the filter. This Simulink filter model can be used as a standalone model or combined with the SRM drive Simulink model and simulated for different values of filter's switch duty cycle. This

is done to obtain the response of the proposed filter to the load harmonics and to select the best duty cycle for operation.

2.4.1 Constant Duty Cycle Operation of Hybrid Active Power Filter (APF) with SRM Drive Model

In this section, constant duty cycle operation of the Hybrid APF is studied by combining it with the SRM drive model in Simulink. This combined model is then simulated for a constant duty cycle. This Simulink model is shown in Figure 2.10.

The state space equations' based Simulink subsystem of the hybrid APF is shown in Figure 2.11. And the Hybrid APF subsystem is shown in Figure 2.12. It should be noted that this includes the passive filter.

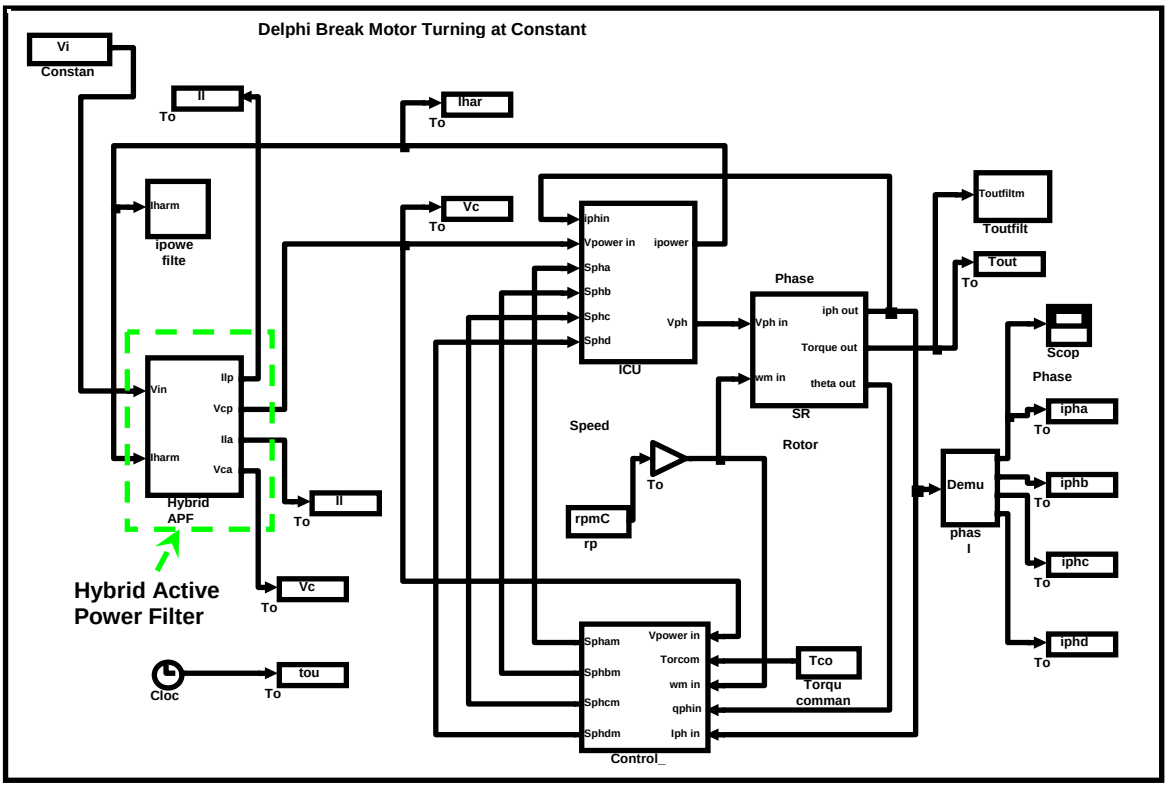


Figure 2.10 Simulink Model of Hybrid APF coupled to SRM Drive

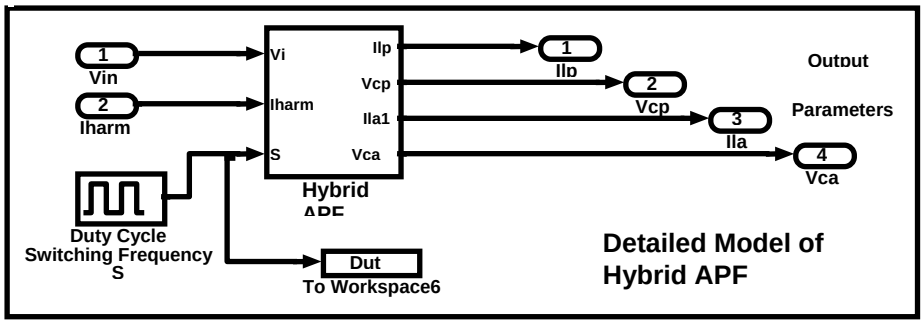


Figure 2.11 Detailed Model of Hybrid APF

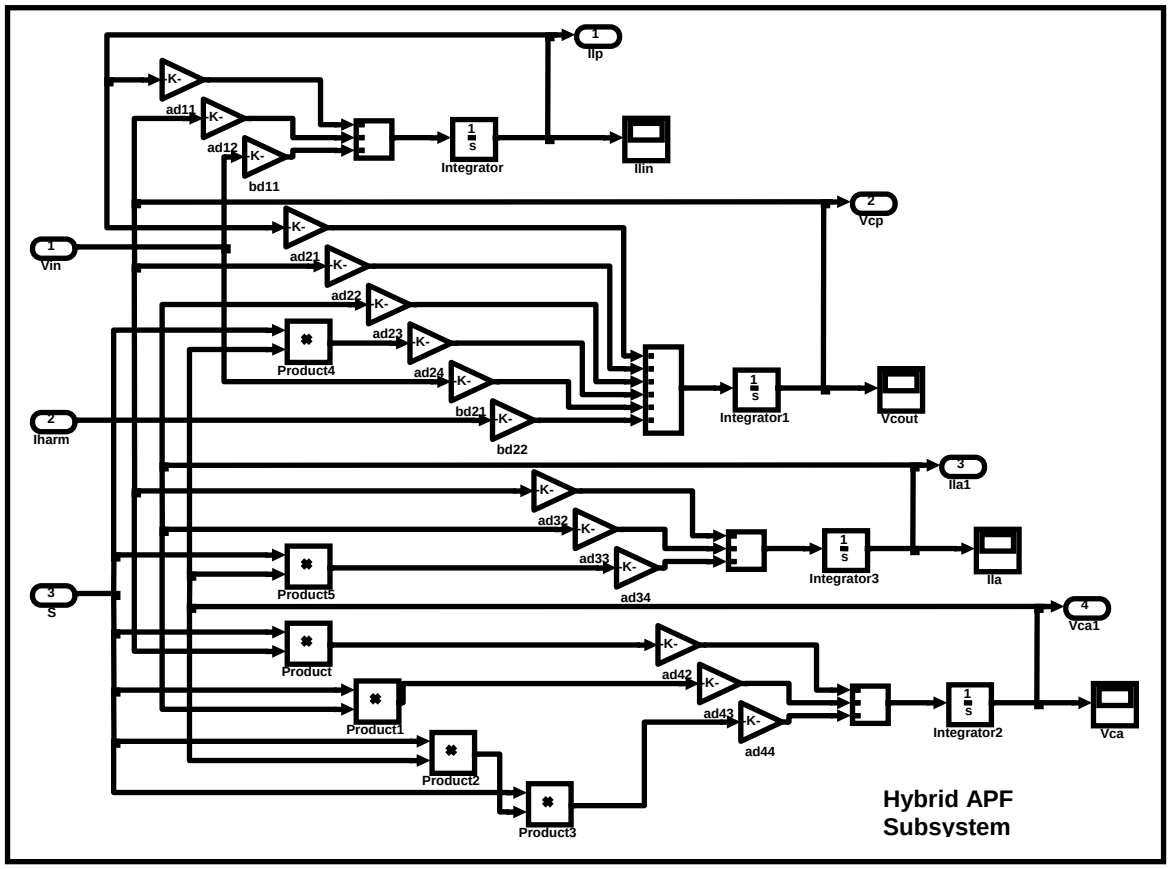


Figure 2.12 Subsystem of Detailed Model of Hybrid APF

The hybrid active filter uses more components than the passive filter it replaces but benefits from the use of passive components of smaller physical size. Similar to the passive filter, the voltage output across the passive capacitor serves as the input to the SRM drive. The harmonic load current is filtered using the combination of passive and

active sections of the hybrid APF as discussed in section 1.3. A pulse generator is used in Simulink at a switching frequency of 100 kHz and a constant duty cycle to produce the switch state variable S.

Before beginning to analyze the simulation results for different duty cycles ranging from 20 % to 70 %, it is necessary to discuss some of the assumptions made. The proposed active filter is of a boost converter topology. The active capacitor voltage (voltage across the capacitor Ca connected across the two switches) is always higher than the input voltage to the active filter which is also the input voltage to the switched reluctance motor drive. This voltage across Ca is inversely proportional to the duty cycle. Therefore utilizing a higher duty cycle reduces the voltage across the active capacitor. This in turn reduces the size of the capacitor assuming its value does not change since a capacitor's size is proportional to the energy it must store. Therefore a higher duty cycle was used initially. The results for a 70 % constant duty cycle are shown in Figure 2.13.

The current through the input passive inductor "Lp" and voltages across passive output capacitor "Cp" and active capacitor "Ca" oscillate at a low frequency of about 110 Hz.

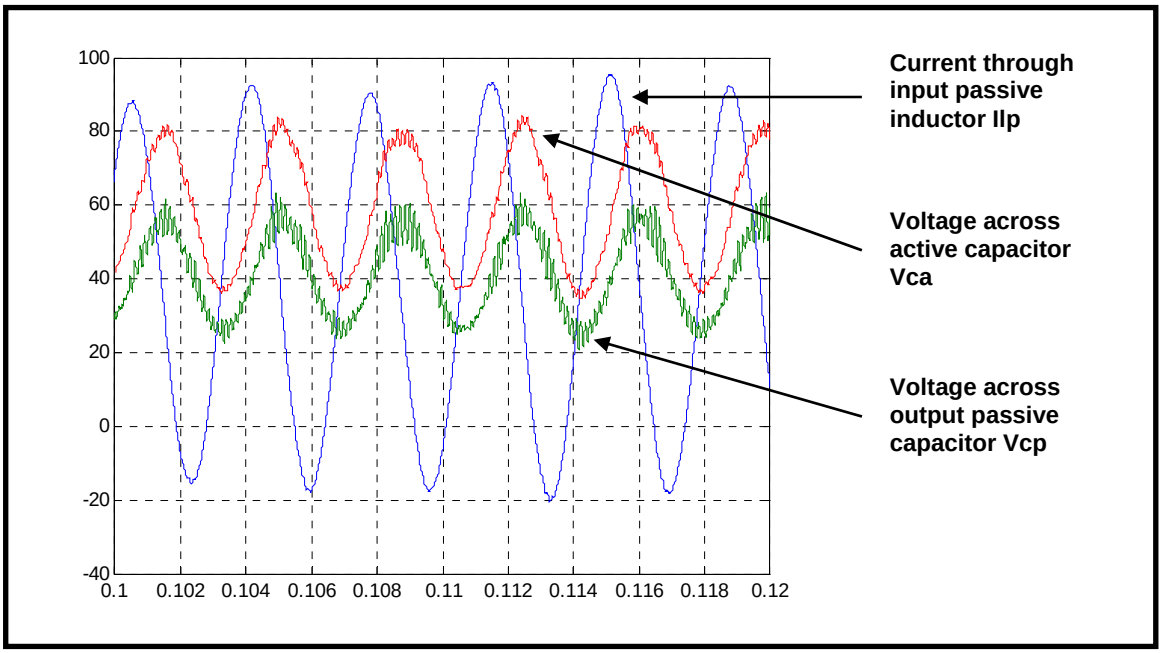


Figure 2.13 Output Parameters from 70 % Constant Duty Cycle Operation

It should also be noted that the monitored output parameters have not settled. It can be concluded that the filter is unstable at this duty cycle. The spectrums of current through input passive inductor and load current I_{harm} and Mil STD 461 are plotted in Figure 2.14.

It can be seen that the spectrum of current through input passive inductor (middle plot) does not meet Mil. STD 461 (bottom plot). The top plot is the spectrum of non-linear load current. From this it can be concluded that the active filter design with the given component values operating at a high duty cycle is not adequate.

Simulations were done with sequential reduction of the duty cycle from 70 % to 50 %, 30 % and 20 %. The simulation results are shown starting with Figure 2.15 and summarized in Table 2.3.

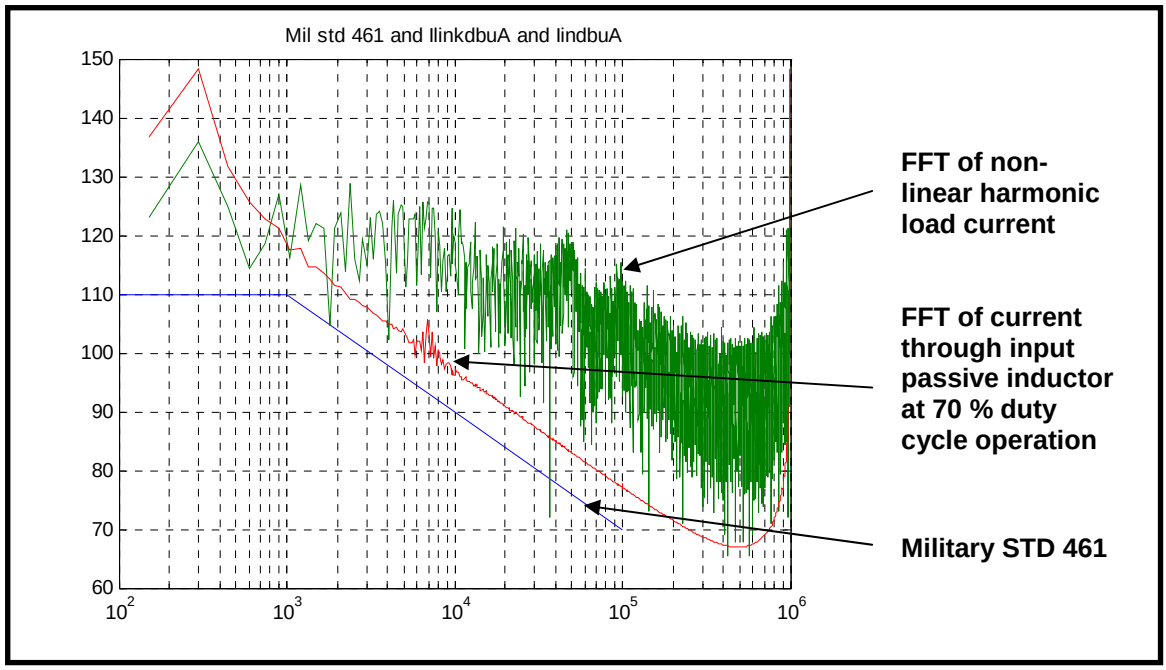


Figure 2.14 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 at 70 % Duty Cycle Operation

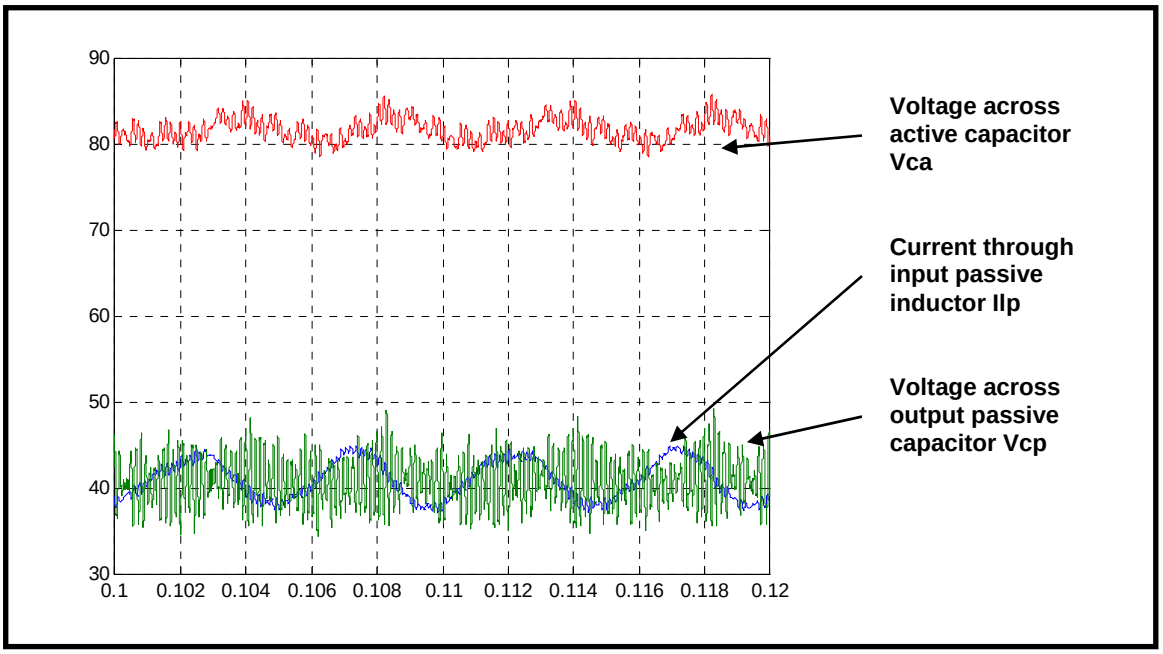


Figure 2.15 Output Parameters from 50 % Constant Duty Cycle Operation

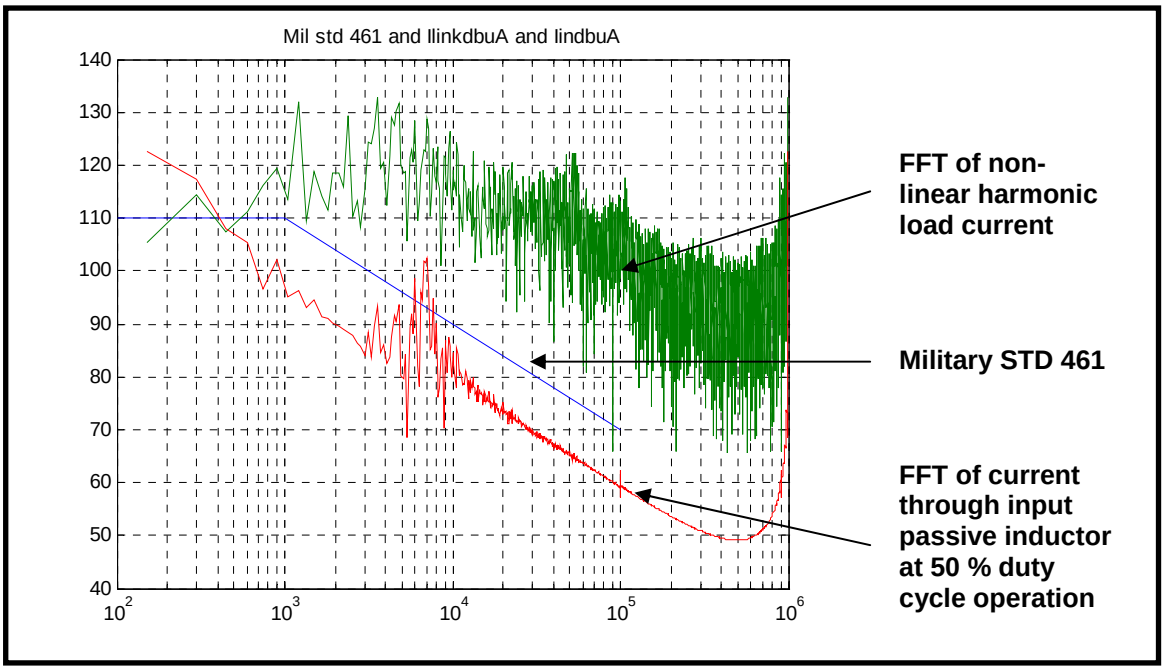


Figure 2.16 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 at 50 % Duty Cycle Operation

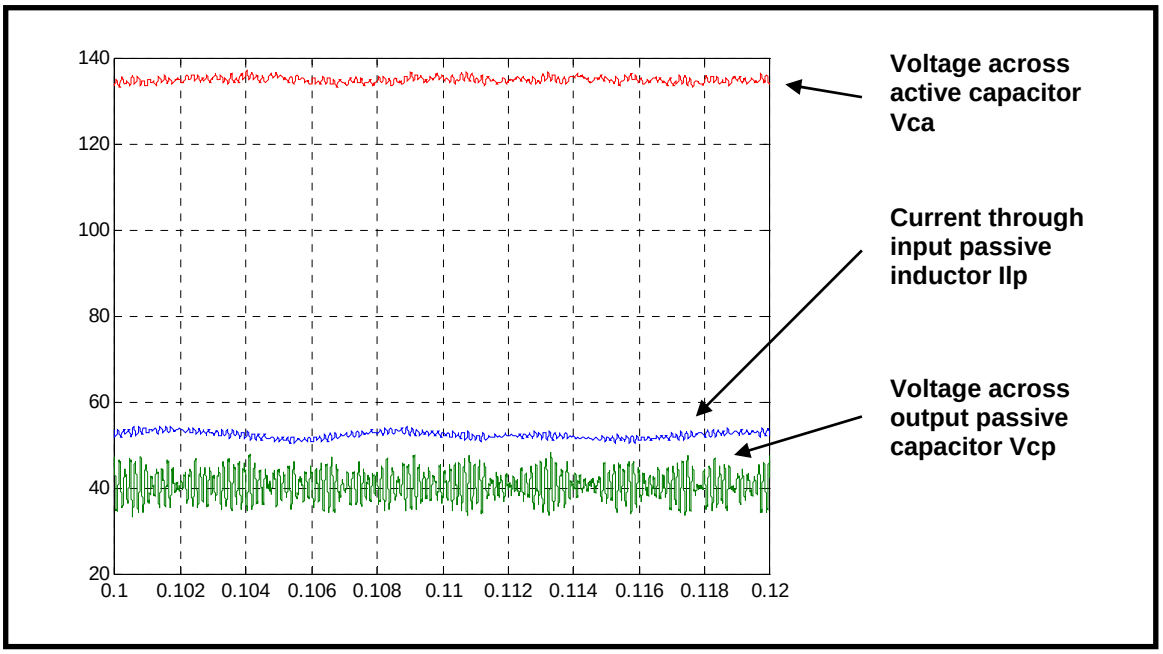


Figure 2.17 Output Parameters from 30 % Constant Duty Cycle Operation

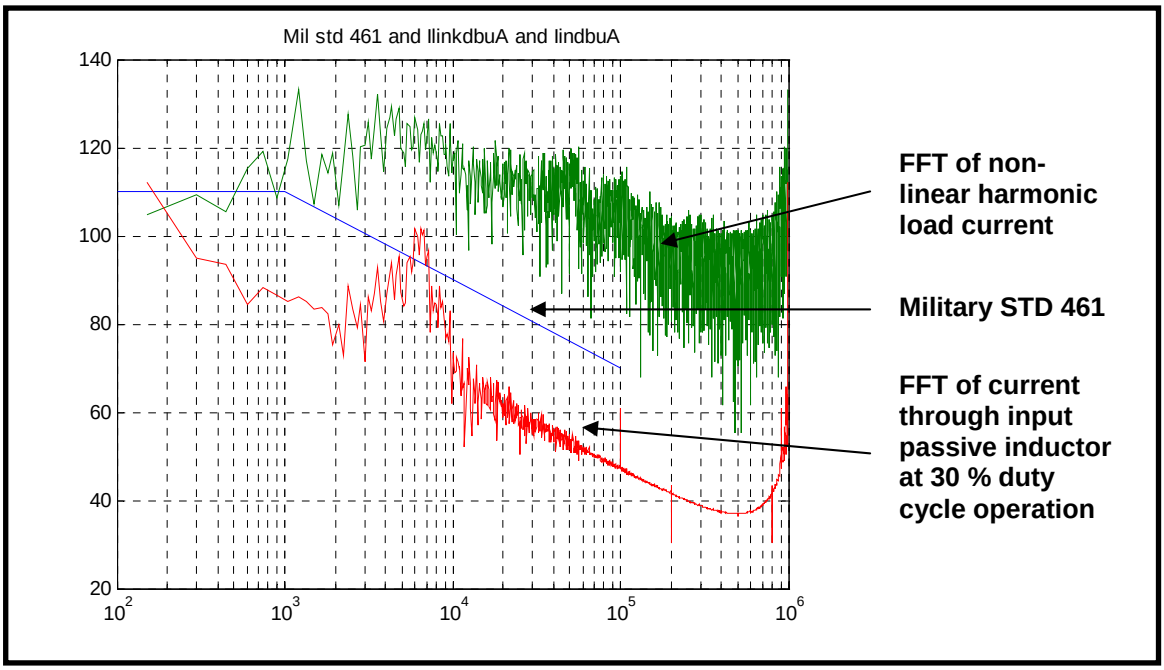


Figure 2.18 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 at 30 % Duty Cycle Operation

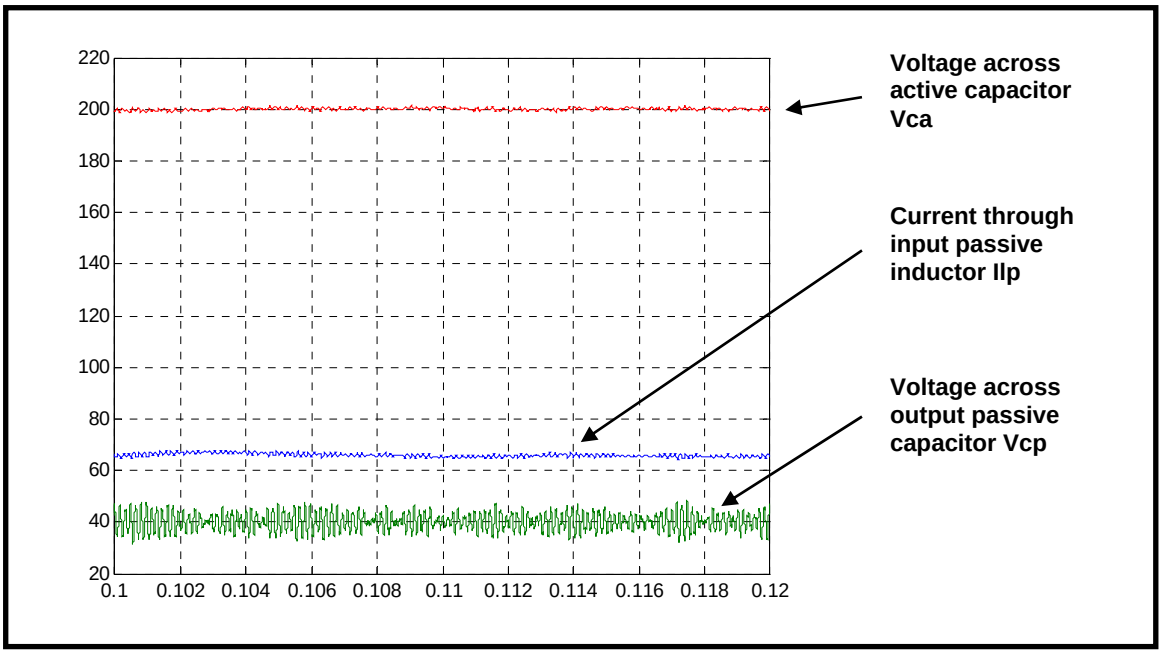


Figure 2.19 Output Parameters from 20 % Constant Duty Cycle Operation

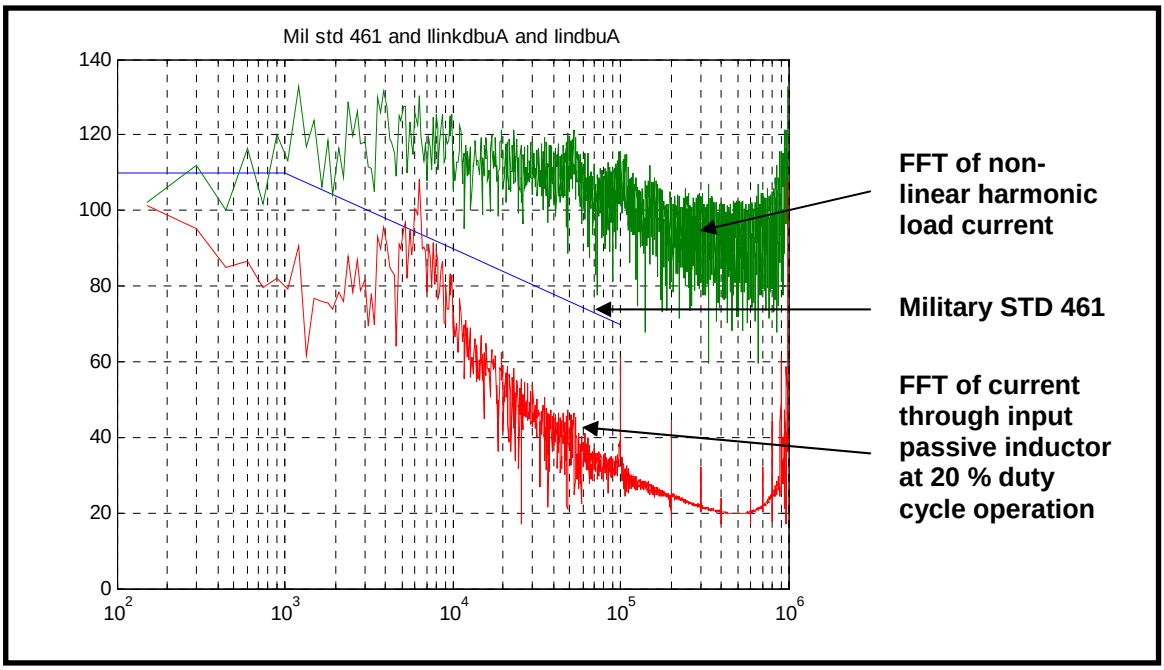


Figure 2.20 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 at 20 % Duty Cycle Operation

Table 2.3 Summary of Constant Duty Cycle Simulations

Constant Duty Cycle	50 %	30 %	20 %
Mean input passive inductor current	41 A	52 A	66 A
Input passive inductor ripple current	+- 8 A	+- 4 A	+- 3 A
Mean output capacitor voltage	42 V	41 V	40 V
Output capacitor ripple voltage	+- 14 V	+ - 14 V	+- 16 V
Mean active capacitor voltage	82 V	135 V	200 V
Active capacitor ripple voltage	+- 7 V	+ - 3 V	+- 3 V
Mil STD 461	Does not meet	Does not meet	Does not meet
Margin to Mil STD 461 (at 100 kHz)	10 dB	20 dB	40 dB

From these plots and the above summary the following observations are made:

- When the duty cycle is increased (tends to 100 %)
  - The input passive inductor current magnitude decreases
  - The input passive inductor ripple current increases
  - The active capacitor voltage gets closer to the passive capacitor voltage
  - The FFT of the input current ripple gets further away from meeting Mil. STD 461.
- When the duty cycle is decreased (tends to 0 %)
  - The input passive inductor current magnitude increases
  - The input passive inductor ripple current decreases
  - The active capacitor voltage gets bigger than the passive capacitor voltage
  - The FFT of the input current ripple gets closer to meeting Mil. STD 461 and gets within it

However, there is a spike in the input passive inductor current spectrum at 6 kHz which corresponds to resonant frequency of the filter's active inductor and passive output capacitor ($\frac{1}{2\pi\sqrt{L_a C_p}}$ gives 6.3 kHz). In addition, the resonant frequency of the filter's

active inductor and active capacitor is 4.5 kHz ($\frac{1}{2\pi\sqrt{L_a C_a}}$). Reference [2] used feedback control to address this issue. Therefore feedback control is necessary to limit this spike in the input current spectrum and meet the Military STD 461 specification.

This brings up another question. At which steady state duty cycle value should feedback control be employed? It was seen earlier that having a high duty cycle made the AC part of input current high. Also lower values of duty cycle increase the value of input current. It should be noted that the current drawn by the SRM is dependent on its power rating and not directly on the duty cycle of the hybrid active filter. However, with lower ripple content in the input passive inductor current, the power to the SRM increases. Lower duty cycle operation also increased the active capacitor voltage and the effective capacitance. Therefore a trade-off is necessary. Steady state duty cycle of 25 % (lying between 20 % and 30 %) was chosen considering these constraints. Having concluded that feedback control is necessary, the next question arising is the choice of feedback control scheme. The first feedback control scheme is discussed in the following section.

2.5 Full State State-Space Feedback Control for Hybrid APF

Full state state-space feedback control technique is chosen as a feedback control scheme. In this thesis, full state feedback control is used to not only ensure that the filter meets its EMC standards, but to significantly reduce the physical size of the filter. To complete the full state feedback control, a linear model of the filter system is necessary. There are two problems that must be addressed here.

1. The switch state variable S can only be 0 or 1. It is the fraction of time that S =1 that is the control variable not the value of S. This problem is solved by making an average model, which is still nonlinear.
2. The system is nonlinear, even the average model is nonlinear. This is solved by linearizing the average model.

The detailed model of the hybrid active filter discussed in the previous section was found to be non-linear due to the presence of the switch state variable S. Therefore, a

linearization of the detailed model is performed. The previously obtained sets of non-linear equations are linearized around a steady state operating value using Taylor series expansion. Since the operating frequency for the switches is high (100 kHz), it is assumed that the state variables doesn't change significantly during a single switching cycle. Using this assumption, non-linear terms obtained through Taylor series expansion are discarded. Due to this, the system's parameters are valid only for small variations around their steady state operating values. This system is termed as a small signal system.

Two techniques for obtaining a small signal linear model from an average model have been researched. An average model of the switch has been proposed by [10 – 12]. State space averaging has been described in [1] and used in [2]. However, the average models are non-linear. In this thesis, both the above two techniques were used separately to obtain an average model first. Small signal models were individually developed from both the average models. It was verified from the resulting state space equations that both the small signal models were similar. Owing to the mathematical ease in analysis the first technique that uses an average model of a switch was chosen finally. The small signal model obtained using this average model serves as a crux for state space feedback control.

Various control schemes for active power filters have been proposed in [2, 6, 11, 17 – 21, 24, 26 – 28]. These control schemes generate a current or voltage which compensates for the ripple entering a system due to switching circuit loads. However this requires a reference signal (current/voltage) for comparing the measured current/voltage to obtain the error which in turn is used in error compensation. The reference signals can be estimated using either frequency domain or time domain approaches. Frequency domain approaches are not preferable due to the time delay in determining signal parameters and transformation of the obtained information to reference signals in the time domain, which are required in the physical circuit. The time domain estimation techniques presented in [24, 26 – 28] are mostly for three phase ac systems with some for single phase ac systems. Root Locus based PI or PID error compensation control doesn't require any special signal estimation. The input power supply voltage serves as the reference voltage and the voltage across the passive filter capacitor (Cp) is the output. Both of these

voltages are readily available and measured. The difference between these two voltages gives the error signal. Full state, state space feedback may require the design of a full/reduced state observer for signal estimation as not all of the states may be easily measurable directly using current and voltage sensors nor are their desired values easily determined. The signal estimation in either of the above control schemes, use analog electronic circuits and is theoretically faster than frequency domain techniques.

Getting back to selection of a control scheme, it should be noted that the active filter system being proposed in this thesis utilizes dc power. Literature on control schemes for such a topology is limited. The control schemes presented for three phase and single phase AC systems give a general idea which is used to proceed. Linear control techniques use error compensation with Proportional, Integral and Derivative control. Mixing and matching is used as needed (P, PI or PID). Other control schemes such as hysteresis control [24], dead beat current control [29], and predictive current control [30] have been reported for error compensation. However, these techniques are not suitable for this design. The drawbacks of some of the above reported designs are discussed later in detail.

2.5.1 Small Signal Model of the Active Filter

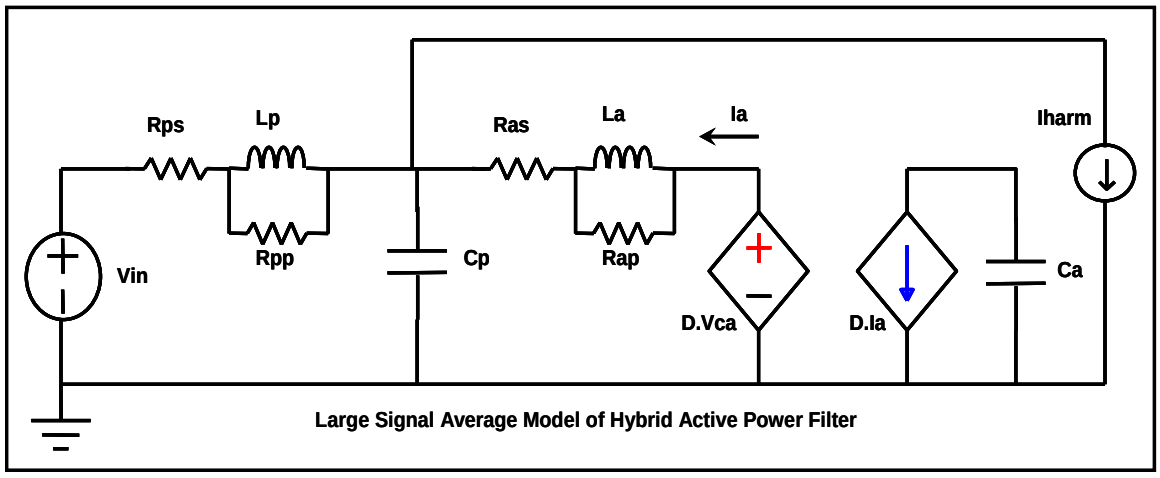


Figure 2.21 Large Signal Average Model of Active Power Filter

Starting with the detailed model of the hybrid APF in Figure 2.9, the large signal average model of the hybrid APF model is found. The process described in references [11 – 12] is used. This large signal average model is shown in Figure 2.21.

The dependent current and voltage sources in the above figure are the average model of the MOSFET switches as discussed earlier (and in section 2.5). The dependent sources are nonlinear by the product of the MOSFET switches duty cycle as in the current through the second loop, *Ia (sum of current through the inductor (Ila) and its equivalent parallel resistance (*$\frac{L_a}{R_{ap}} \cdot \frac{di_{la}}{dt}$*))*, and the voltage across capacitor Ca, *Vca*. Note that in state space analysis, the current through an inductor (current through inductor Lp, *Ilp* and current through inductor La, *Ila*) and voltage across a capacitor (voltage across capacitor Cp, *Vcp*, in addition to *Vca*) are typically used as the state variables though the choice of state variables is not unique. In general, any energy storing element can be considered a state variable. In Figure 2.21, the two dependent sources are dependent on the state variables and duty cycle (The duty cycle varies with time. It is the average of switch state variable S(t) which is a square wave with a time varying duty cycle.)

The nonlinear large signal average model shown in Figure 2.21 is used to obtain the linear small signal average model. Assume that there is a small perturbation in the state variables, inputs and outputs. The state variables in the above model with small perturbations are defined as shown below along with the duty cycle and its small perturbation.

$$\left.\begin{aligned} I_{lp} &= I_{lp0} + i_{lp} \\ V_{cp} &= V_{cp0} + v_{cp} \\ I_{la} &= I_{la0} + i_{la} \\ V_{ca} &= V_{ca0} + v_{ca} \\ D &= D_0 + d \end{aligned}\right\} \qquad \textbf{2.19}$$

The terms in lower case are the perturbation terms and the terms in upper case with “0” appended are the steady state or quiescent values in equation 2.19.

Now, the dependent sources from the large signal model in Figure 2.21 are analyzed.

$$D \cdot V_{ca} = (D_0 + d)(V_{ca0} + v_{ca}) = \{D_0 \cdot V_{ca0}\} + \{D_0 \cdot v_{ca} + d \cdot V_{ca0}\} + \{d \cdot v_{ca}\} \quad \textbf{2.20}$$

Equation 2.20 is separated into the three terms in the three brackets. The first term is the steady state DC component. The second term has two parts proportional to the small signal state variable v_{ca} and the small signal duty cycle respectively. The third term is non-linear and being smaller than the rest of the terms is discarded (leaving a final system with only linear terms). For small signal analysis, the steady state DC component is also discarded so the final equation for the voltage dependant source is

$$D \cdot V_{ca} = D_0 \cdot v_{ca} + d \cdot V_{ca0} \quad \textbf{2.21}$$

Similarly,

$$D \cdot I_a = (D_0 + d)(I_{a0} + i_a) = \{D_0 \cdot I_{a0}\} + \{D_0 \cdot i_a + d \cdot I_{a0}\} + \{d \cdot i_a\} \quad \textbf{2.22}$$

Equation 2.22 is separated into three terms again. However, the current, *D.Ia*, flows into a capacitor and, the average current through a capacitor is zero. Using this result all the terms in equation 2.22 with steady state currents are eliminated. In addition, the steady state DC component and non-linear component are discarded. This results in the following final equation for the current dependant source.

$$D \cdot I_a = D_0 \cdot i_a \quad \textbf{2.23}$$

In addition, independent voltage and current sources (or all sources) are assumed to have no perturbations and are zero for small signal analysis. Therefore the input voltage source, *Vin*, and the load current source, *Iharm* in Figure 2.21 are zero in the small model shown in Figure 2.22. The two series dependant sources and the active filter capacitor can be simplified further as shown in Figure 2.23.

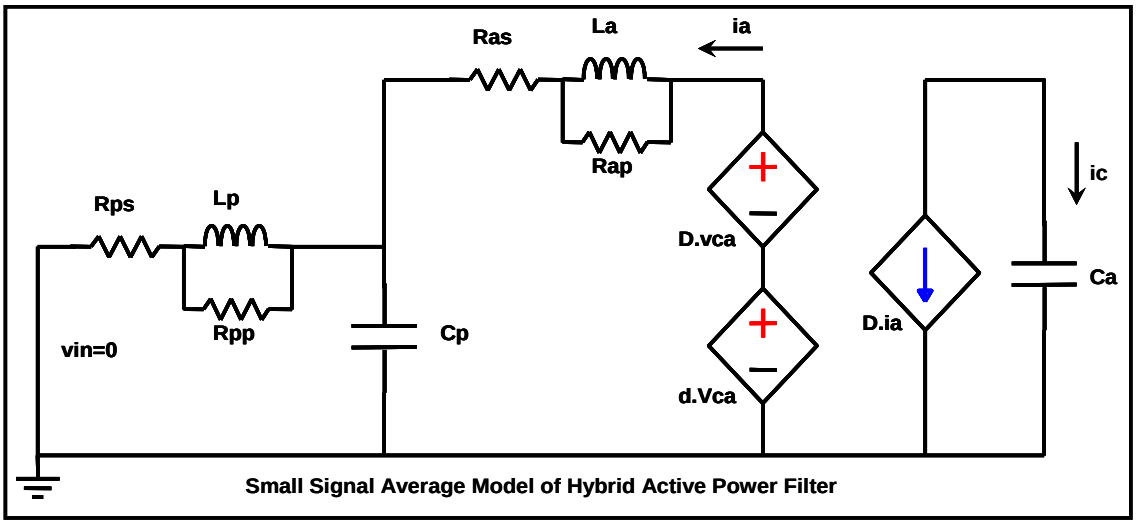


Figure 2.22 Small Signal Model of Hybrid Active Power Filter

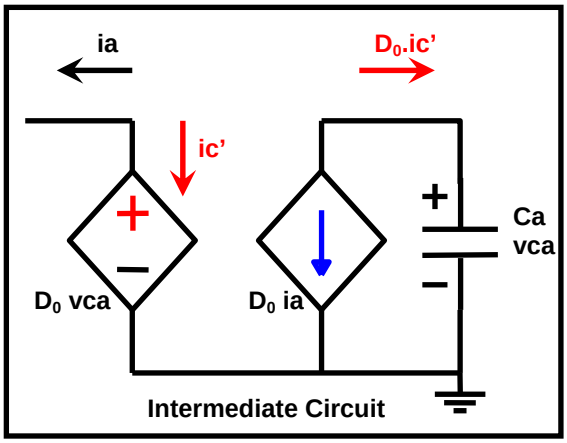


Figure 2.23 Intermediate Small Signal Circuit

Then D_0 ia = - D_0 ic′ and thus ia = - ic′. The capacitor current equation is given by equation 2.24.

$$D_0 \cdot i_a = -D_0 \cdot i_{c'} = -C_a \cdot \frac{dv_{ca}}{dt} = -C_a \cdot \frac{d}{dt}\left(\frac{1}{D_0} \cdot D_0 \cdot v_{ca}\right), \text{ which gives}$$

$$i_{c'} = \frac{C_a}{D_0^{\,2}} \cdot \frac{d}{dt}\left(D_0 \cdot v_{ca}\right) \qquad \textbf{2.24}$$

Using equation 2.24 and the above intermediate small signal circuit, an equivalent model is obtained for the active capacitor "Ca" and the current source connected in series with it. This is shown in Figure 2.24. Using the equivalent circuit from Figure 2.24, the final small signal model of the proposed hybrid active filter is shown in Figure 2.25. Note that the output transfer function (for *d* as the small signal duty cycle input generating *vcp* as the output) is zero under DC conditions since the capacitor Ca/D_0^2 is connected in series with the dependant voltage source.

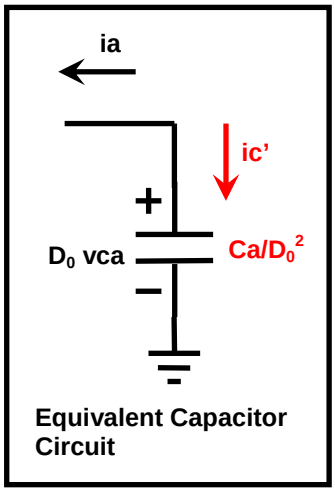


Figure 2.24 Equivalent Circuit of Capacitor with Current Source

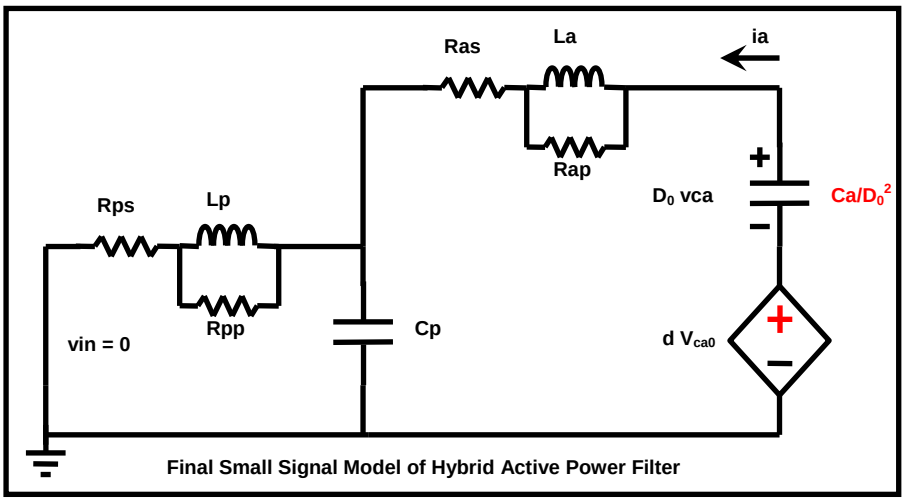


Figure 2.25 Final Small Signal Model of Hybrid Active Power Filter

The small signal circuit model shown in Figure 2.25 is used for the control design. Again, KVL and KCL are used to obtain the state equations for the linear small signal model of the proposed active power filter.

Applying KVL to the first loop gives the following

$$v_{cp} = L_p \cdot \frac{di_{lp}}{dt} + R_{ps} \cdot \left(i_{lp} + \frac{L_p}{R_{pp}} \cdot \frac{di_{lp}}{dt} \right) \qquad \textbf{2.25}$$

$$\frac{di_{lp}}{dt} = \frac{-R_{ps} \cdot R_{pp}}{L_p \cdot \left(R_{ps} + R_{pp}\right)} \cdot i_{lp} + \frac{R_{pp}}{L_p \cdot \left(R_{ps} + R_{pp}\right)} \cdot v_{cp} \qquad \textbf{2.26}$$

Assuming that the current flows from right to left half (as shown by the direction of current of *ia*) in Figure 2.25, KCL is applied at the three way node.

$$i_a = i_{la} + \frac{L_a}{R_{ap}} \cdot \frac{di_{la}}{dt} = C_p \cdot \frac{dv_{cp}}{dt} + i_{lp} + \frac{L_p}{R_{pp}} \cdot \frac{di_{lp}}{dt} \qquad \textbf{2.27}$$

However, equation 2.27 has three derivative terms of which only one is known (equation 2.26). The second state equation is for the voltage across capacitor Cp, *vcp*. To find this derivative, the derivative of current through the active filter inductor La, *ila*, must be found first. This is done by applying KVL to the second loop of the circuit model in Figure 2.25. This is shown below.

$$d \cdot V_{ca0} + D_0 \cdot v_{ca} = L_a \cdot \frac{di_{la}}{dt} + R_{as} \cdot \left(i_{la} + \frac{L_a}{R_{ap}} \cdot \frac{di_{la}}{dt} \right) + v_{cp} \qquad \textbf{2.28}$$

$$\frac{di_{la}}{dt} = -\frac{R_{ap}}{L_a \cdot \left(R_{as} + R_{ap}\right)} \cdot v_{cp} - \frac{R_{as} \cdot R_{ap}}{L_a \cdot \left(R_{as} + R_{ap}\right)} \cdot i_{la} + \frac{R_{ap}}{L_a \cdot \left(R_{as} + R_{ap}\right)} \cdot D_0 \cdot v_{ca} + \frac{R_{ap}}{L_a \cdot \left(R_{as} + R_{ap}\right)} \cdot V_{ca0} \cdot d \qquad \textbf{2.29}$$

Substituting equations 2.28 and 2.29 in to equation 2.27 and simplifying yields the following.

$$\frac{dv_{cp}}{dt} = \frac{-R_{pp}}{C_p \cdot \left(R_{ps} + R_{pp}\right)} \cdot i_{lp} - \left[\frac{1}{C_p \cdot \left(R_{ps} + R_{pp}\right)} + \frac{1}{C_p \cdot \left(R_{as} + R_{ap}\right)}\right] \cdot v_{cp} + \frac{R_{ap}}{C_p \cdot \left(R_{as} + R_{ap}\right)} \cdot i_{la} + \frac{1}{C_p \cdot \left(R_{as} + R_{ap}\right)} \cdot D_0 \cdot v_{ca} + \frac{1}{C_p \cdot \left(R_{as} + R_{ap}\right)} \cdot V_{ca0} \cdot d \quad \textbf{2.30}$$

The final state space equation is obtained by writing the equation for current through the active filter capacitor Ca, *ic*.

$$-\left[i_{la} + \frac{L_a}{R_{ap}} \cdot \frac{di_{la}}{dt}\right] = \frac{C_a}{D_0^{\,2}} \cdot \frac{d}{dt}\left(D_0 \cdot vca\right) \quad \textbf{2.31}$$

Again, equation 2.31 has two derivative terms and only one of them (the derivative of voltage across the active filter capacitor Ca, *vca*) is needed. Therefore equation 2.29 is substituted in to equation 2.31 and simplified to give the following.

$$\frac{dv_{ca}}{dt} = \frac{1}{C_a \cdot \left(R_{as} + R_{ap}\right)} \cdot D_0 \cdot v_{cp} - \frac{R_{ap}}{C_a \cdot \left(R_{as} + R_{ap}\right)} \cdot D_0 \cdot i_{la} - \frac{1}{C_a \cdot \left(R_{as} + R_{ap}\right)} \cdot D_0^{\,2} \cdot v_{ca} - \frac{1}{C_a \cdot \left(R_{as} + R_{ap}\right)} \cdot D_0 \cdot V_{ca0} \cdot d \quad \textbf{2.32}$$

Equations 2.26, 2.29, 2.30 and 2.32 are collectively represented in state space matrix format as shown below in equation 2.33.

$$\begin{bmatrix} \frac{di_{lp}}{dt} \\ \frac{dv_{cp}}{dt} \\ \frac{di_{la}}{dt} \\ \frac{dv_{ca}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-R_{ps}\cdot R_{pp}}{L_p\cdot\left(R_{ps}+R_{pp}\right)} & \frac{R_{pp}}{L_p\cdot\left(R_{ps}+R_{pp}\right)} & 0 & 0 \\ \frac{-R_{pp}}{C_p\cdot\left(R_{ps}+R_{pp}\right)} & \frac{-1}{C_p}\cdot\left[\frac{1}{R_{ps}+R_{pp}}+\frac{1}{R_{as}+R_{ap}}\right] & \frac{R_{ap}}{C_p\cdot\left(R_{as}+R_{ap}\right)} & \frac{D_0}{C_p\cdot\left(R_{as}+R_{ap}\right)} \\ 0 & \frac{-R_{ap}}{L_a\cdot\left(R_{as}+R_{ap}\right)} & \frac{-R_{as}\cdot R_{ap}}{L_a\cdot\left(R_{as}+R_{ap}\right)} & \frac{R_{ap}\cdot D_0}{L_a\cdot\left(R_{as}+R_{ap}\right)} \\ 0 & \frac{D_0}{C_a\cdot\left(R_{as}+R_{ap}\right)} & \frac{-R_{ap}\cdot D_0}{C_a\cdot\left(R_{as}+R_{ap}\right)} & \frac{-D_0^{\,2}}{C_a\cdot\left(R_{as}+R_{ap}\right)} \end{bmatrix} \cdot \begin{bmatrix} i_{lp} \\ v_{cp} \\ i_{la} \\ v_{ca} \end{bmatrix}$$

$$+ \begin{bmatrix} 0 \\ \frac{1}{C_p\cdot\left(R_{as}+R_{ap}\right)}\cdot V_{ca0} \\ \frac{R_{ap}}{L_a\cdot\left(R_{as}+R_{ap}\right)}\cdot V_{ca0} \\ \frac{-1}{C_a\cdot\left(R_{as}+R_{ap}\right)}\cdot V_{ca0}\cdot D_0 \end{bmatrix} \cdot d \qquad \textbf{2.33}$$

Equation 2.33 is the final state space matrix representation of the small signal model of the active filter. This equation is similar to the standard state space equations' format presented earlier in equations 2.7 and 2.8.

Equation 2.7 is known as the differential equation and equation 2.8 is the output equation with u the input and y the output. From equation 2.33 it is seen that the small signal system has a single input, the small signal duty cycle, *d*.

The goal of this thesis is to limit the ripple current entering the input to the SRM drive drawn from the DC power supply. From the circuit model shown in Figure 2.9 it is clear that this ripple current generates a ripple voltage which ensures that the output voltage of the system, the steady state voltage across capacitor Cp, *Vcp*, is not equal to the input voltage *Vin*. A measure of the deviation in the voltage *Vcp* from *Vin* gives a measure of the deviation in steady state current *Ia* due to the ripple from the non-linear load.

Therefore the output to be monitored is the small signal voltage across the capacitor Cp, *vcp*. This is the small signal model's output and in effect the ripple voltage (since all independent sources are zero in the small signal analysis) due to small perturbations in

the input small signal duty cycle. This small signal output is written in the same format as equation 2.8.

$$y = v_{cp} = \begin{bmatrix} 0 & 1 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{lp} \\ v_{cp} \\ i_{la} \\ v_{ca} \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix} \cdot d \qquad \textbf{2.34}$$

From equations 2.33 and 2.34 it is evident that this small signal system is a single input single output (SISO) system. This gives the added benefit of being able to employ transfer function based frequency domain stability analysis and feedback design. The transfer function for a system defined by equations 2.7 and 2.8 is obtained as shown below using Laplace transformation [31, 32].

$$L\left\{\dot{x}\right\} = L\left\{A \cdot x + B \cdot u\right\}$$

$$s \cdot X(s) - X(0) = A \cdot X(s) + B \cdot U(s)$$

$$X(s) \cdot \left\{s \cdot I - A\right\} = B \cdot U(s) + X(0)$$

$$X(s) = \left\{s \cdot I - A\right\}^{-1} \cdot \left\{B \cdot U(s) + X(0)\right\}$$

$$L\left\{y\right\} = L\left\{C \cdot x + D \cdot u\right\} = Y(s) = C \cdot X(s) + D \cdot U(s)$$

$$Y(s) = C \cdot (s \cdot I - A)^{-1} \cdot B \cdot U(s) + D \cdot U(s) + C \cdot (s \cdot I - A)^{-1} \cdot B \cdot X(0)$$

$$Y(s) = \left\{\left[C \cdot (s \cdot I - A)^{-1} \cdot B + D\right] \cdot U(s)\right\} + \left\{C \cdot (s \cdot I - A)^{-1} \cdot B \cdot X(0)\right\} \qquad \textbf{2.35}$$

Equation 2.35 gives the output (in Laplace or 's' domain) of the system of equations defined in 2.7 and 2.8. There are two portions on the right hand side of equation 2.35. The first part is known as the zero state response (ZSR) and it occurs when the system has zero initial conditions/states. The second part is known as the zero input response

(ZIR) and it occurs when there is no external input to the system. This is also known as the natural response of the system. For stability analysis zero initial conditions can be assumed. Also, from equation 2.34 it is clear that the D matrix for this system is zero (It should be noted that this must not be mistaken with the duty cycle term D_0). This reduces equation 2.35 to the following.

$$Y(s) = \left\{C \cdot (s \cdot I - A)^{-1} \cdot B\right\} \cdot U(s)$$

$$\frac{Y(s)}{U(s)} = G(s) = C \cdot (s \cdot I - A)^{-1} \cdot B \qquad \textbf{2.36}$$

Equation 2.36 is the output transfer function of the system of equations defined by 2.7 and 2.8. For the proposed values for the hybrid active filter given in Table 2.2 the small signal transfer function is

$$G(s) = \frac{8.391 \cdot 10^4 \cdot s^3 + 2.622 \cdot 10^{11} \cdot s^2 + 4.458 \cdot 10^{13} \cdot s - 6}{s^4 + 4858 \cdot s^3 + 1.629 \cdot 10^9 \cdot s^2 + 3.714 \cdot 10^{11} \cdot s + 7.539 \cdot 10^{14}} \qquad \textbf{2.37}$$

The transfer function is 4th order and the small signal system's poles and zeros are found for stability analysis.

The poles are: $p_{1,2} = -2315.8 \pm i40274.78,\ p_{3,4} = -113.43 \pm i671$

The zeros are: $z1 = -3125000,\ z2 = -170,\ z3 = 1.35 \cdot 10^{-13}$

The poles of the system determine the stability of the system. It can be seen that all the poles have negative real parts and hence the system is stable. It must be noted that one of the zeros is positive and close to zero. Its effect is negligible unless there are poles in its vicinity. This is true for the other zeros as well. Zeros close to the poles affect the transient response. The pole pair, *P3,4*, has the greater real part and is thus the dominant pole pair. The settling time of the system is based on the dominant poles and is found using the equation given below [31, 32].

$$t_s = \frac{4}{|\mathrm{Re}(p)|} \quad \textbf{2.38}$$

The poles of the system are found so that pole placement using state space feedback can be employed based on the open loop location of the poles. This forms the base for the next section where state space feedback control is discussed.

2.5.2 State Space Feedback Control Design for Small Signal Model of Hybrid Active Power Filter

In this section, full state, state space feedback control of the small signal model of the hybrid active filter's switching circuit is developed. Full state, state space feedback control allows placement of the closed loop poles of the system at any desired location in the left half s-plane (stable region). All poles of the original small signal system can be placed based on the settling time design constraint which gives a good measure of speed of response of system. It can be seen from the open loop poles of the system that their imaginary parts are greater than their real parts. This affects the damping factor of the system. This brings up the inherent properties of this filter system, especially the damping factor. The damping factor determines the way a system responds (transient response) to changes in control parameters (duty cycle). An under-damped system tends to oscillate quite a bit before reaching its steady state value. A complex pole pair with imaginary part greater than the real part has a low damping factor. The intent is to address this with pole placement. Consider the original poles of the small signal system found in section 2.5.1.

$$p_{1,2} = -2315.8 \pm i40274.78,\ p_{3,4} = -113.43 \pm i671$$

This is compared to the standard second order system pole equation [31, 32].

$$s_{a,b} = -\zeta \cdot \omega_n \pm i \cdot \omega_n \cdot \sqrt{1-\zeta^2} \quad \textbf{2.39}$$

The 4^{th} order small signal system's two complex conjugate pole pairs have damping factors of 0.17 and 0.057, with the higher value corresponding to the dominant pole pair. It is clear from these values (lower than 1) that the filter system is highly under-damped.

Feedback control for variable duty cycle (to generate gating pulses for the switches incorporated in the active section) can be done using full state, state space feedback. The advantage of full state feedback is that all poles can be replaced so that the damping factor improves, which will also reduce the input current ripple. It also improves the system's settling time by reducing it. The state space feedback law [31, 32] is given as below.

$$u = -k \cdot x \qquad \textbf{2.40}$$

Substituting 2.40 into the standard state space differential equation in 2.7 gives the following,

$$\dot{x} = A \cdot x + B \cdot \left(-k \cdot x\right)$$

$$\dot{x} = \left[A - B \cdot k\right] \cdot x \qquad \textbf{2.41}$$

It should be noted that the filter system has a zero D matrix (refer to equation 2.8). And therefore, the output equation 2.8 doesn't change. The new feedback law involves setting the poles of the $\left[A - B \cdot k\right]$ matrix such that all the poles are more stable (having greater negative real part) and more damped (smaller ratio of the imaginary over the real part). Compare equation 2.41 to the standard state equation in 2.7. This equation has no external input. Since the small signal system's poles have negative real parts, the individual states of the system tend to zero (asymptotical stability). The feedback control law therefore only speeds up the response of the system to small perturbations in the states. The small perturbations in the state generate a small perturbation in the input which reduces the perturbation in the state to zero.

To complete the design the gain vector k must be chosen so that the matrix A-B.k has the desired Eigen values and thus the system has the desired closed loop poles. To ensure that this is possible the controllability of the system must be established [31, 32]. A system (defined in equation 2.7) is said to be controllable if there exists an unconstrained input, *u,* that can transfer any initial state, *x(0)*, to any other desired location *x(t)* [31, 32]. An analytical test for controllability based on the controllability matrix is shown below in equation 2.42.

$$ctr = \begin{bmatrix} B & A \cdot B & A \cdot A \cdot B & A \cdot A \cdot A \cdot B \end{bmatrix} \qquad \textbf{2.42}$$

If "*ctr"* has full rank or equivalently if its determinant has a non-zero value, the system is said to be completely controllable. Since the filter system described here is 4th order, the rank of this matrix must be 4 for the system to be controllable.

If all of the system states cannot be measured but rather only the outputs can be measured it will be necessary to estimate the unmeasured states from the measured output. This will be possible if the system is observable. A system (defined in equation 2.8) is said to be observable if and only if there exists a finite time interval, *T*, such that the initial state, *x(0)*, can be determined from the observed output, *y(t)*, when the input *u(t)* is known. Again, an analytical test for observability exists based on the observability matrix given in equation 2.43.

$$obs = \begin{bmatrix} C \\ C \cdot A \\ C \cdot C \cdot A \\ C \cdot C \cdot C \cdot A \end{bmatrix} \qquad \textbf{2.43}$$

If "*obs*" has full rank or equivalently if its determinant has a non-zero value, the system is said to be completely observable. Similar to the controllability matrix for this hybrid active filter system, the expected rank must be 4.

Summarizing, controllability determines the existence of a path to control a specific state (pole) and observability determines the existence of a path to measure a specific state.

Simple commands used in matlab reveal that the 4th order small signal system is fully controllable and observable. However, only the controllability test is necessary in this design as all state variables (states) are measurable. Also, the system is already stable. In case the system was not fully controllable, stabilizability (uncontrollable state's real part must be negative) would be a major requirement for state feedback control design. The pole corresponding to the uncontrollable state cannot be modified (placed anywhere in the left half s-plane).

The full state space feedback control is shown in Figure 2.26. The four states of the system, currents through the input passive and active filter inductors and voltages across output and active filter capacitors are required (for state feedback through gain multiplication).

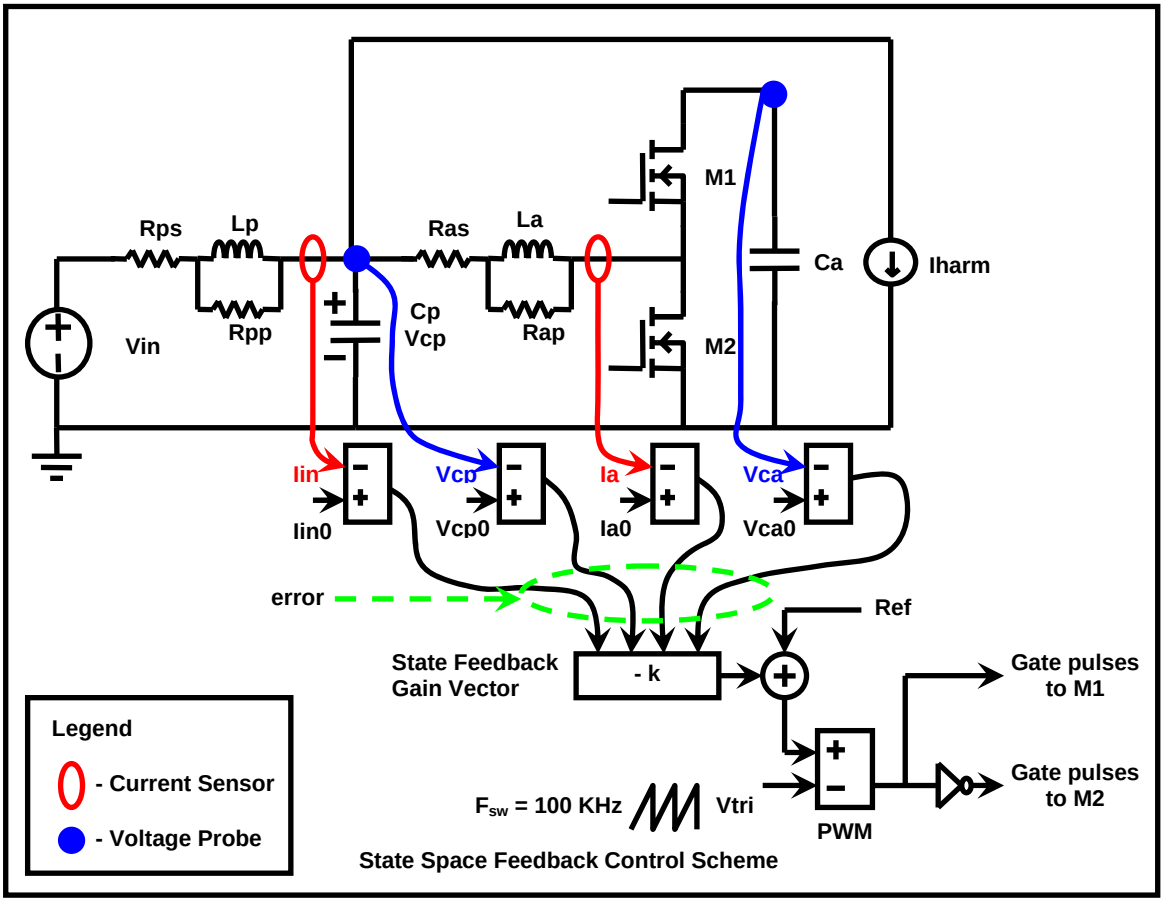


Figure 2.26 Detailed Model of Active Power Filter with State Space Feedback Control

These states are first sensed. The individual state error is found by comparing the sensed states to their reference values. This error is then multiplied by the gain, *k*, and the result summed with the duty cycle reference value to obtain the input, *u*. This input is the duty cycle of the upper MOSFET switch in Figure 2.26 and must be turned into the time duration the upper MOSFET switch is on and thus into the gating signals for the MOSFETs. The hybrid active filter's states can be sensed directly if the circuit permits the placement of current sensors and probes for measuring voltages. Otherwise, a full state, state space observer (or reduced state, state space observer as deemed necessary) is needed to estimate (sense) the instantaneous value of the unmeasured states. Another reason for employing indirect measuring techniques is the cost of sensors. However, observation of the detailed model reveals that the hybrid active power filter circuit is compatible for full state feedback.

The state feedback gain determined for the small signal system is used with the original detailed model for generating gating pulses (for the MOSFETs). The scalar input resulting from the multiplication of gain vector with all constituent states (*u = -k.e+ref, where e is the state error*) is used as a reference with the pulse width modulation (PWM) circuit for generating gating pulses.

Current sensors and voltage probes are used to obtain a continuous measurement of individual states. A matlab m-file was developed to obtain the small signal transfer function, poles, zeros and finally the state feedback gains for selected pole pairs. The m-file is presented in Appendix C. The previously developed hybrid filter model in Simulink was modified to include the full state feedback. The modified hybrid filter subsystem based on the block diagram from Figure 2.26 is shown in Figure 2.27. The currents *Iin* and *Ia* from Figure 2.26 are replaced with currents *Ilp* and *Ila* in the subsystem and for subsequent analysis and simulations. The reason for this is that in the physical circuit model, it is impossible to separate the currents flowing through the equivalent parallel resistance (EPR) and the inductor.

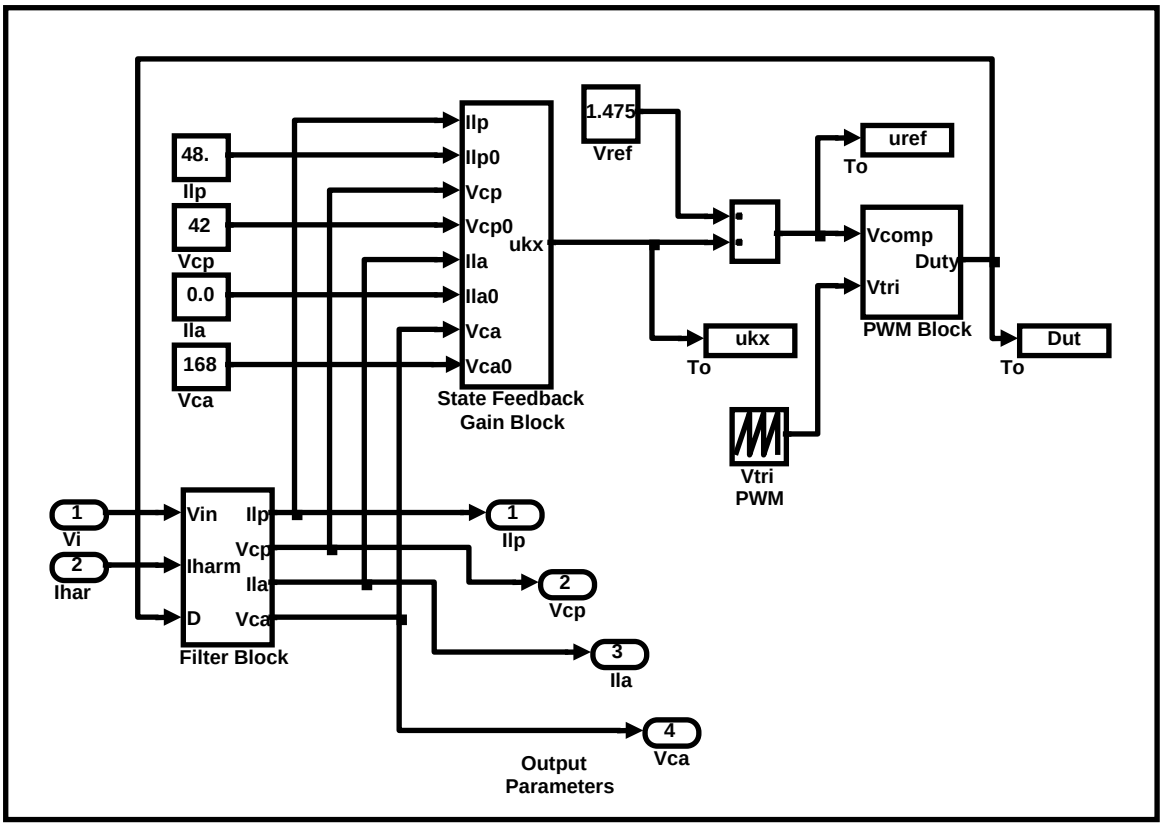


Figure 2.27 Hybrid APF Subsystem with State Feedback Gain

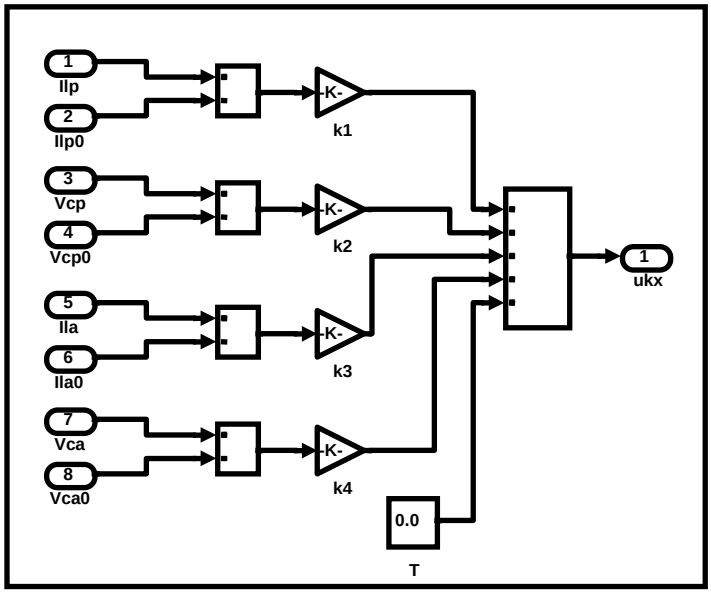


Figure 2.28 State Feedback Gain Block

The individual state error is determined by comparing the sensed state value with the state's reference value. The reference voltages are determined based on the input DC source's magnitude of 42 V (the target output of the filter) and the active capacitor's voltage of 168 V (based on 25 % duty cycle operation, this voltage found as 42/0.25). The current through the active inductor has an average value of 0 A based on the premise of the hybrid filter proposed here (refer to section 1.3) and is used as a reference. The reference value of 48 A for the current through the input passive inductor is determined from simulations performed in this section. And the state feedback gain block subsystem is shown in Figure 2.28.

It was seen from equation 2.41 that asymptotic stability is attainable. However, the feedback problem being addressed in this thesis necessitates inclusion of a reference input in addition to the compensated state error feedback. This was referred to as *ref* in Figure 2.26 and as *Vref* in Figure 2.27.

The relationship between *ref*, *Vref* and the duty cycle is discussed below. Pulse width modulation (PWM) implementation aids this discussion. The PWM block from Figure 2.27 works as per the pictorial representation in Figure 2.29.

$$duty\ cycle = u = -k \cdot e + ref \qquad 2.44$$

Here *ref* is the steady state duty cycle with the value 0.25.

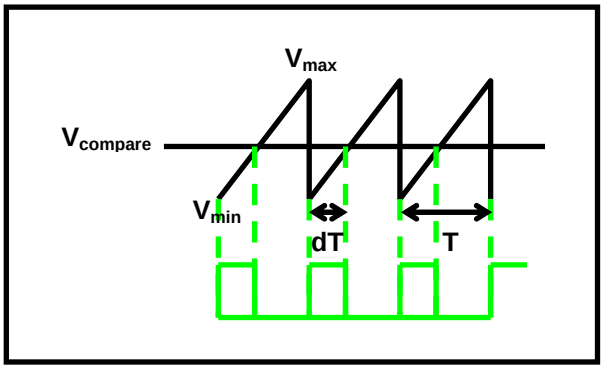


Figure 2.29 PWM Block Operation Principle

$$duty\ cycle = d = 0.25 - k \cdot e \quad \textbf{2.45}$$

The above equation is obtained by replacing *u* in equation 2.44 with *d*. This is the desired duty cycle from the PWM block shown in Figure 2.27.

The equation governing PWM block operation is given below. At time dT,

$$V_{compare} = V_{\min} + \frac{V_{\max} - V_{\min}}{T} \cdot dT \quad \textbf{2.46}$$

Simplification of this yields the following equation.

$$d = \frac{V_{compare} - V_{\min}}{V_{\max} - V_{\min}} = \frac{1}{V_{\max} - V_{\min}} V_{compare} - \frac{V_{\min}}{V_{\max} - V_{\min}} = \left(0.25 - k \cdot e\right) \quad \textbf{2.47}$$

Thus

$$V_{compare} = \left(V_{\max} - V_{\min}\right)\left(0.25 - k \cdot e\right) + V_{\min} \quad \textbf{2.48}$$

Equation 2.48 is evaluated based on the PWM IC's triangle wave's lower and upper limit specification. The evaluated value is used in Figure 2.27.

Having done this, the poles chosen for pole placement are $p_{1,2} = -2315.8 \pm i500,\ p_{3,4} = -500 \pm i100$.

The state feedback gain vector obtained for the above poles for pole placement is:

$$k = [-3.75 \cdot 10^{-5}, -0.006, 1.23 \cdot 10^{-5}, 0.0015] \quad \textbf{2.49}$$

The results from full state state-space feedback with the above state feedback gains are shown in Figure 2.30 and Figure 2.31.

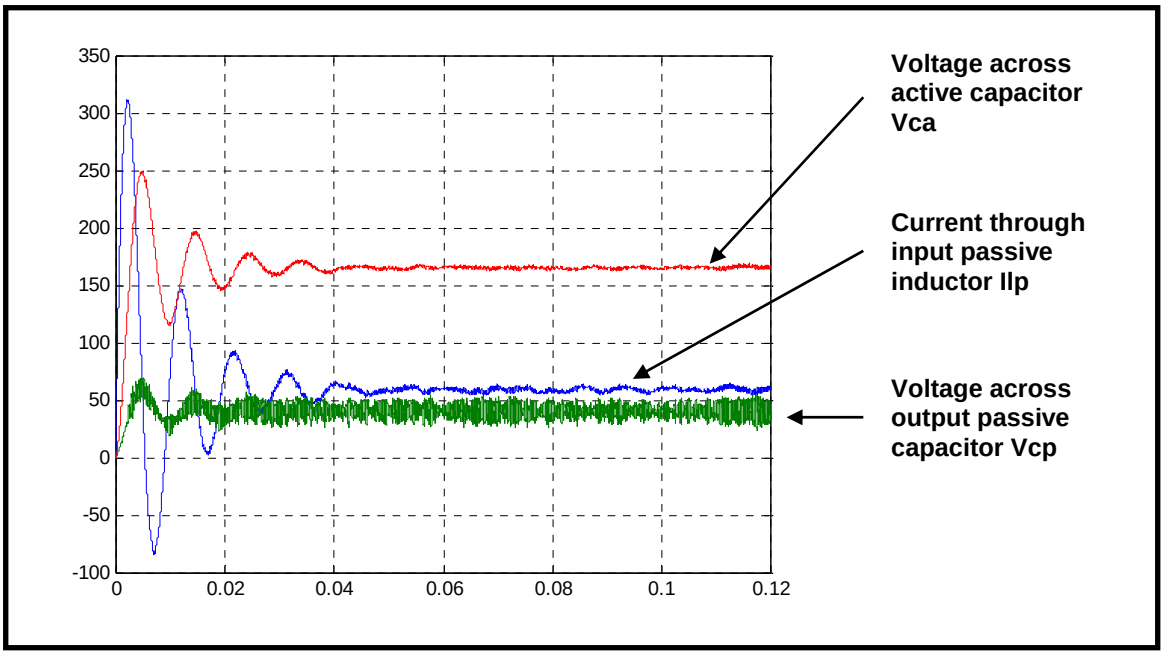


Figure 2.30 Hybrid APF State Feedback Control Output (First Attempt)

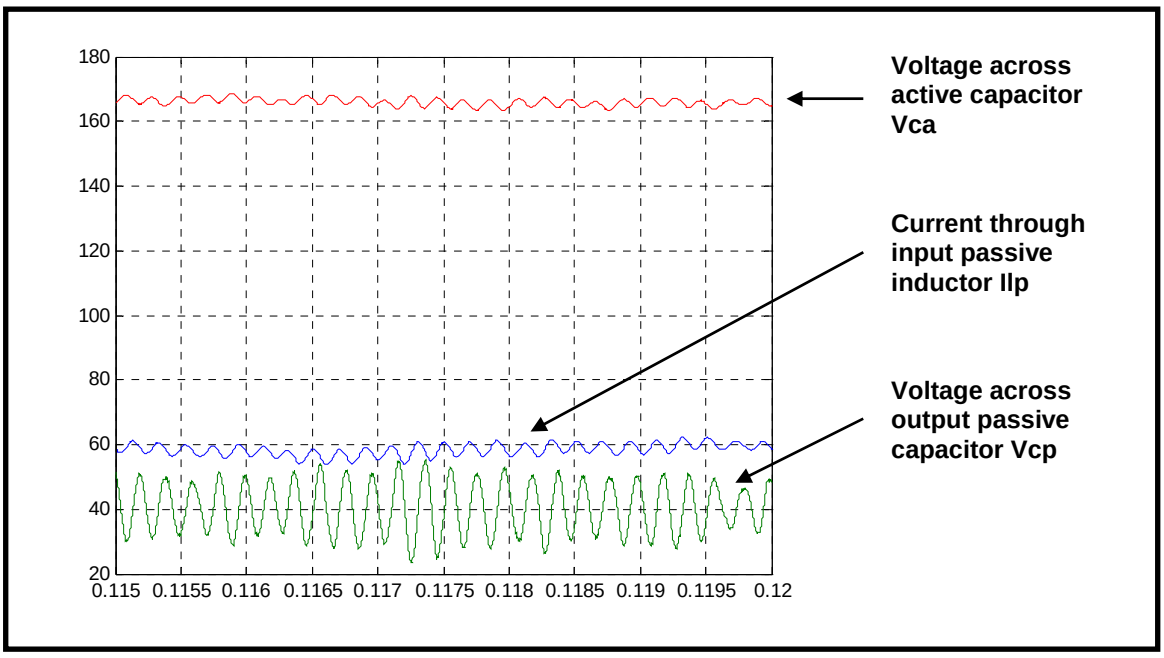


Figure 2.31 Hybrid APF State Feedback Control Output Magnified (First Attempt)

The spectrum of the currents through the input passive inductor and load and the Mil STD 461 is plotted in Figure 2.32.

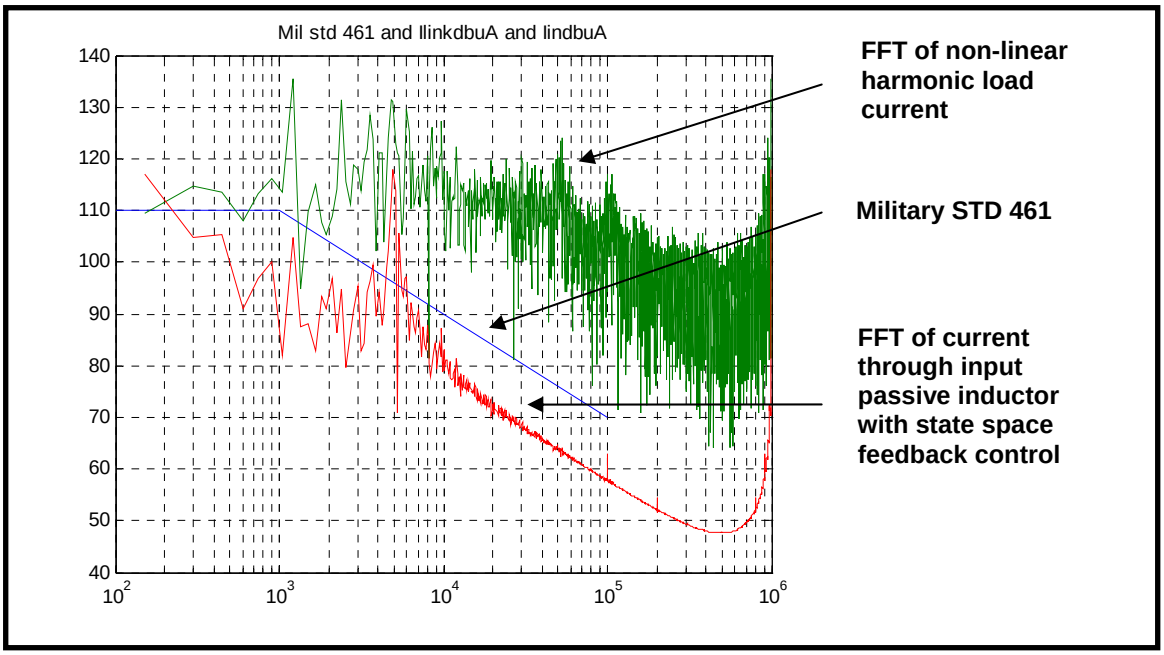


Figure 2.32 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 for State Feedback (First Attempt)

Table 2.4 Summary of State Space Feedback Control Simulation (First Attempt)

State Space Feedback Control (pole placement)	Value
Mean input passive inductor current	59 A
Input passive inductor ripple current	+- 5 A
Mean output capacitor voltage	40 V
Output capacitor ripple voltage	+- 15 V
Mean active capacitor voltage	165 V
Active capacitor ripple voltage	+- 3 V
Mil STD 461	Does not meet
Margin to Mil STD 461 (at 100 kHz)	13 dB

The output parameters from this simulation are summarized in Table 2.4. The above simulation results are from one of the many trials with different poles chosen for each simulation run. Unfortunately, none of them met the Military STD 461. Though the poles were so chosen that they had real parts much greater than the imaginary parts to reduce

ripple, this wasn't seen in the outputs obtained. The size of capacitors "Cp" and "Ca" were also altered from the chosen ones (in Table 2.2) to see the change. However, no significant improvement was observed. It can be concluded that the feedback gains are not effective in attenuating the ripple to a level that meets Military STD 461.

Another attempt at state feedback is done based on the proportional feedback implemented by [2]. An individual gain of value 0.2 was used by [2] for compensating the voltage error at the output voltage (which is *Vcp* here). This individual gain, *kp,* of 0.2, was modified to a value suitable in this thesis. In addition, the other gain elements from the vector were also modified. This new gain vector's elements are shown below.

$$k_{new} = [0.003, -0.175, 0.0005, 0.001] \qquad \textbf{2.50}$$

The output parameters from this simulation are shown successively from Figure 2.33 to Figure 2.37.

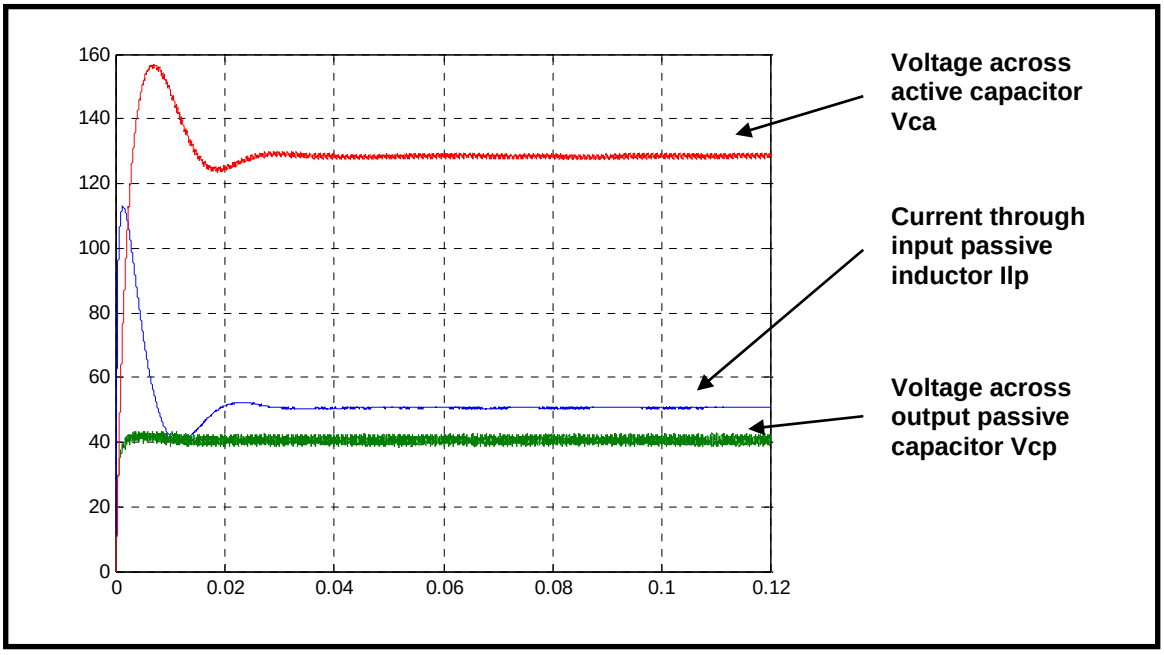


Figure 2.33 Hybrid APF State Feedback Output (Second Attempt)

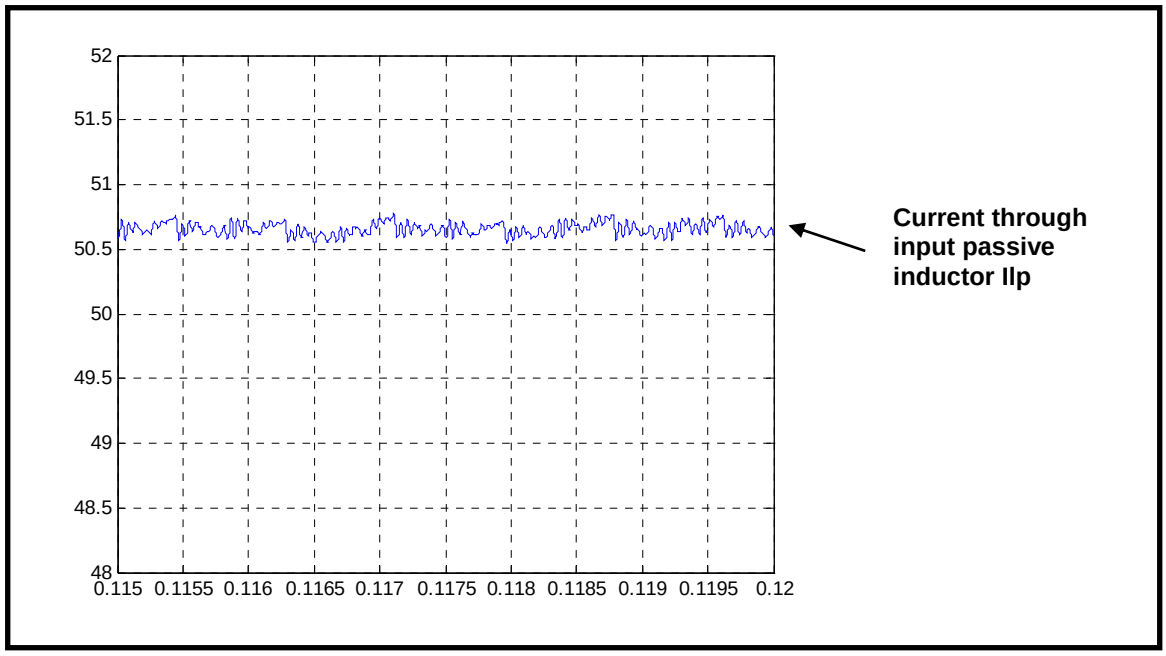


Figure 2.34 Hybrid APF State Feedback Output Ilp Magnified (Second Attempt)

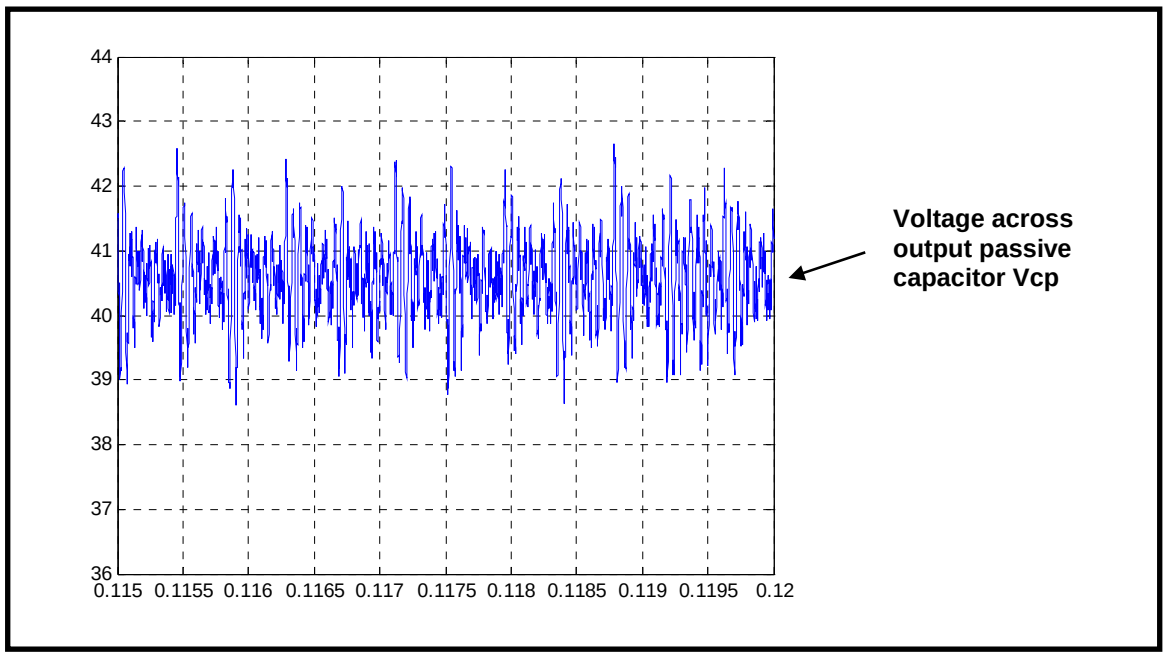


Figure 2.35 Hybrid APF State Feedback Output Vcp Magnified (Second Attempt)

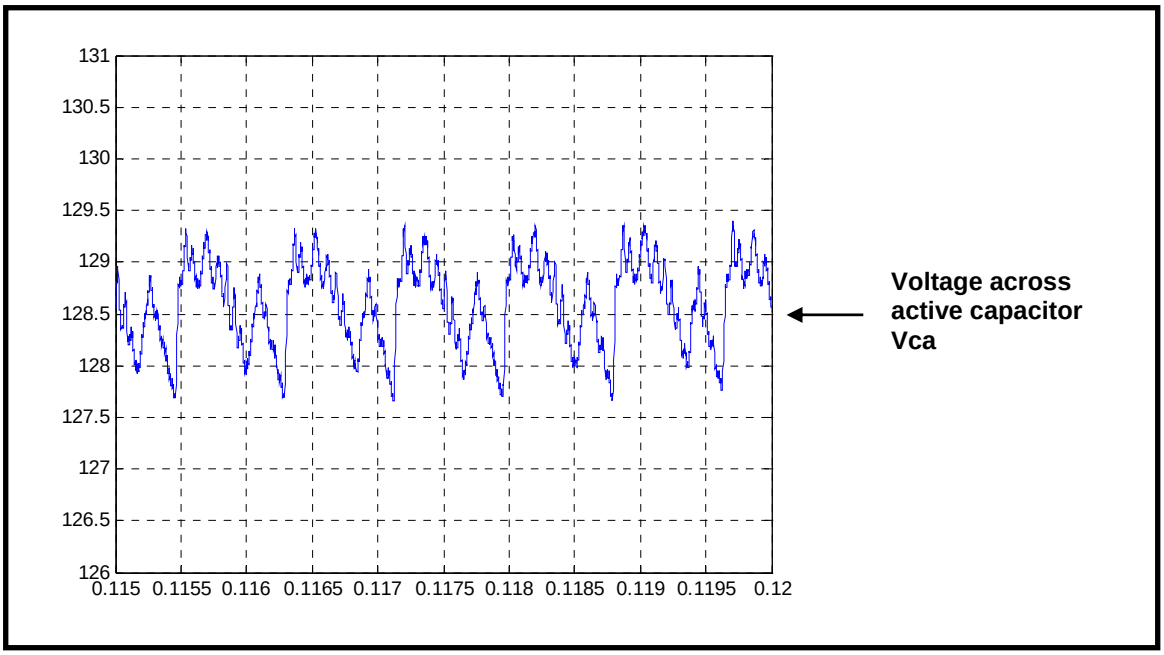


Figure 2.36 Hybrid APF State Feedback Output Vca Magnified (Second Attempt)

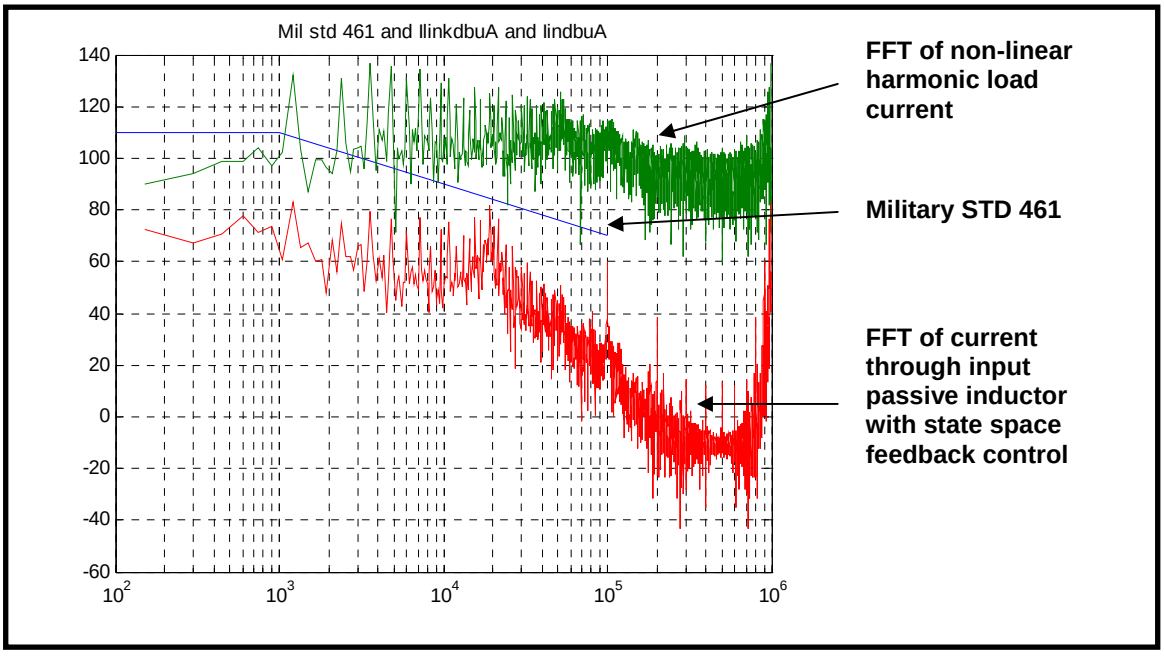


Figure 2.37 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 for State Feedback (Second Attempt)

The output parameters from this simulation are summarized in Table 2.5.

Table 2.5 Summary of State Space Feedback Control Simulation (Second Attempt)

State Space Feedback Control (pole placement)	Value
Mean input passive inductor current	50.6 A
Input passive inductor ripple current	+- 0.2 A
Mean output capacitor voltage	40.6 V
Output capacitor ripple voltage	+- 1.6 V
Mean active capacitor voltage	128.5 V
Active capacitor ripple voltage	+- 1 V
Mil STD 461	Meets STD
Margin to Mil STD 461 (at 100 kHz)	50 dB

The spectrum plot in Figure 2.37 reveals that the filter meets the Military STD 461 when the state feedback gain vector is modified. The spike in the input passive inductor current spectrum at 4.5 kHz seen in Figure 2.32 is suppressed here. This spike corresponds to the resonant frequency caused by the active inductor and active capacitor. However, there is another significant spike in the spectrum with occurs at 100 kHz. This spike corresponds to the switching frequency of the switches in the active section of the hybrid filter.

The final attempt in state feedback control simulation is done by changing the value of element *T* in Figure 2.28 to a non-zero value. This element is termed in this thesis as "*state feedback threshold input*". This *T* is finally chosen to be 0.3 by a trial and error process. The state feedback gain vector remains unchanged from the earlier simulation (equation 2.50). The results from this simulation are shown successively from Figure 2.38 to Figure 2.42.

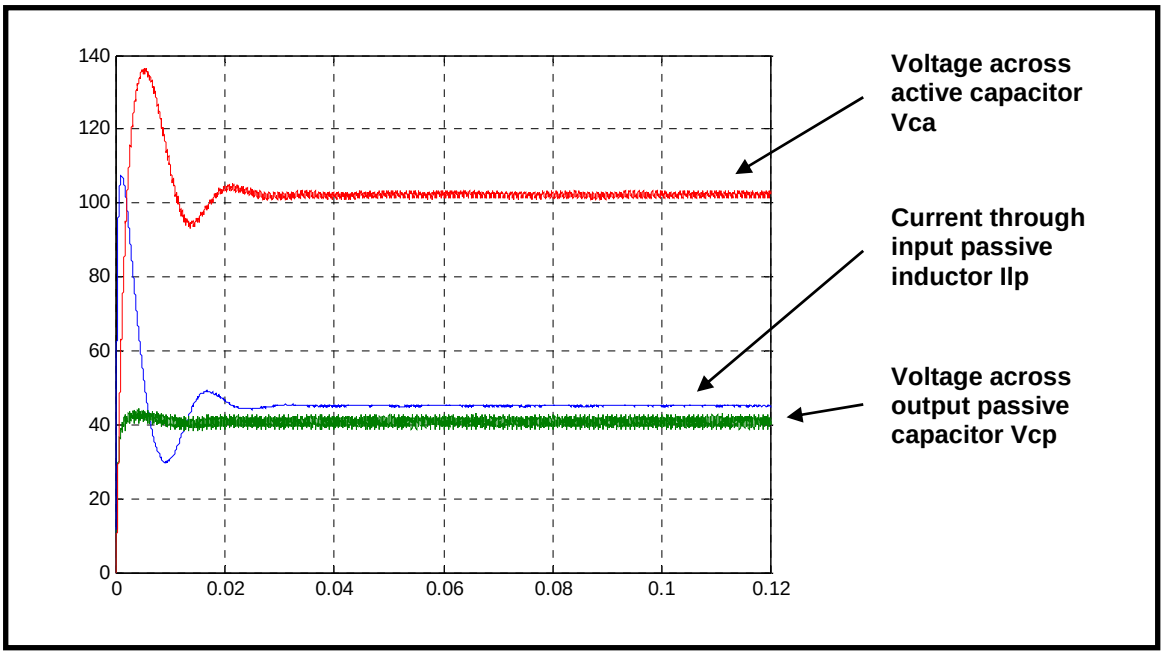


Figure 2.38 Hybrid APF State Feedback Output (Third Attempt)

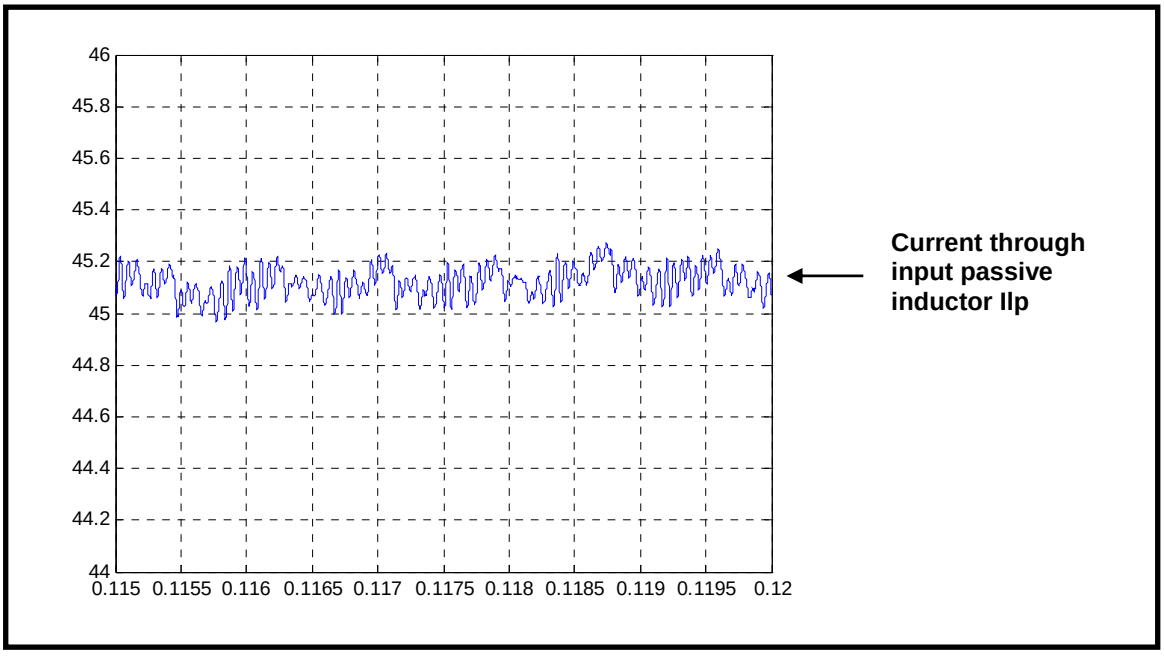


Figure 2.39 Hybrid APF State Feedback Output Ilp Magnified (Third Attempt)

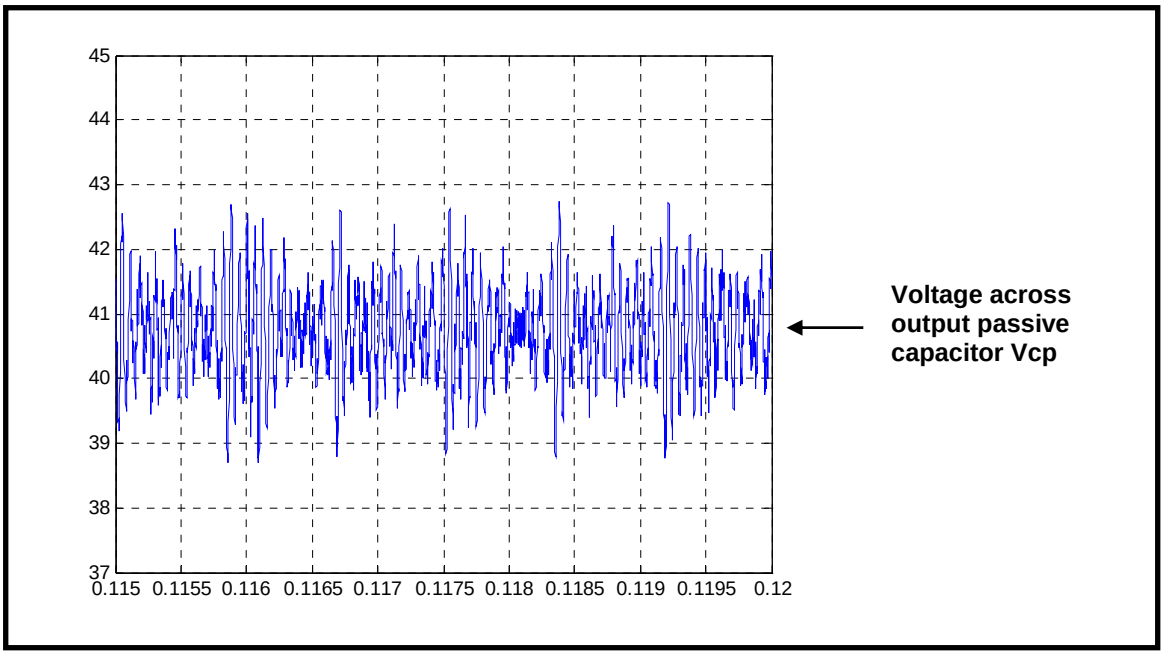


Figure 2.40 Hybrid APF State Feedback Output Vcp Magnified (Third Attempt)

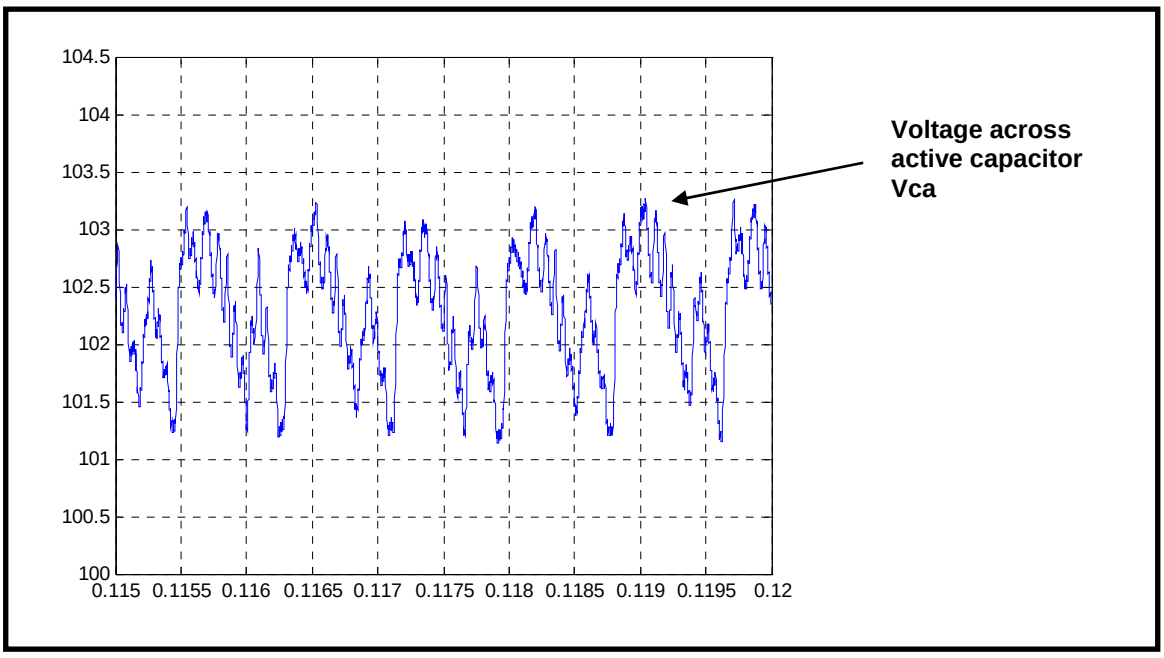


Figure 2.41 Hybrid APF State Feedback Output Vca Magnified (Third Attempt)

The spectrum plot from the third attempt at state feedback control reveals that the hybrid filter meets Mil STD 461. The output parameters from this simulation are summarized in Table 2.6.

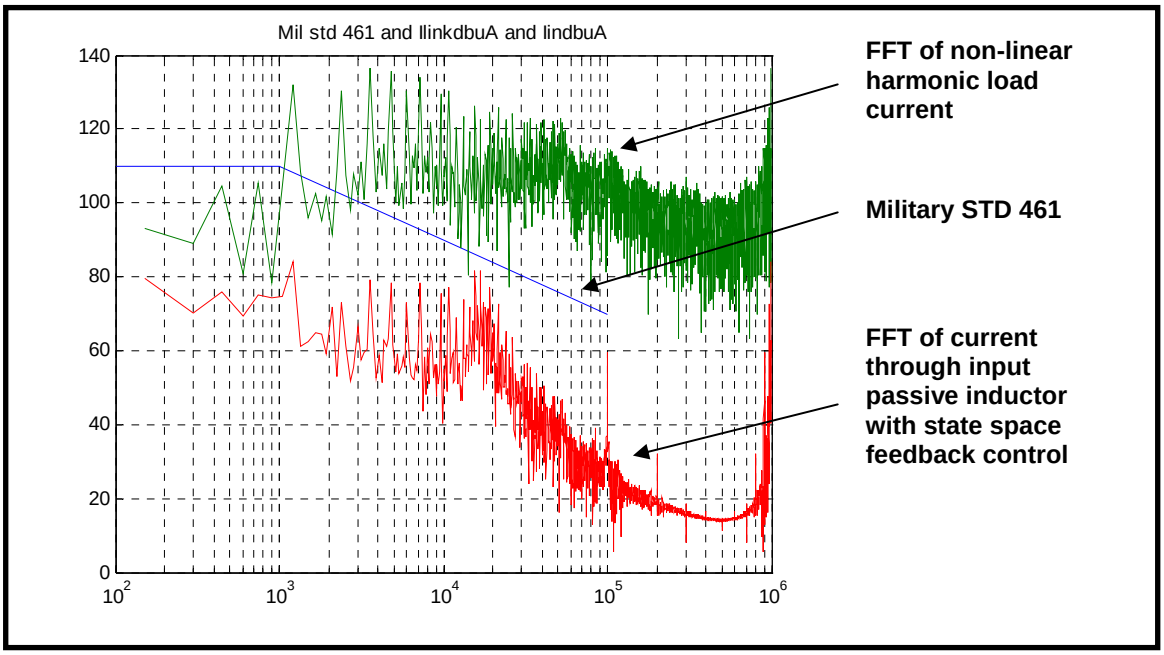


Figure 2.42 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 for State Feedback (Third Attempt)

Table 2.6 Summary of State Space Feedback Control Simulation (Third Attempt)

State Space Feedback Control (pole placement)	Value
Mean input passive inductor current	45.1 A
Input passive inductor ripple current	+- 0.1 A
Mean output capacitor voltage	40.75 V
Output capacitor ripple voltage	+- 2 V
Mean active capacitor voltage	102.25 V
Active capacitor ripple voltage	+- 1 V
Mil STD 461	Meets STD
Margin to Mil STD 461 (at 100 kHz)	45 dB

The mean value of the input passive inductor current has reduced from 50.6 A to 45.1 A. The ripple content in this current for this case has reduced from 0.2 A to 0.1 A. There is no significant change in the mean value of the output capacitor voltage. In addition there is no significant change in the voltage ripple. The active capacitor voltage has reduced from 128 V to 102 V. The ripple content in this voltage remains the same. The gain margin at 100 kHz has reduced from 50 dB to 45 dB. Use of a non-zero value for the "*state feedback threshold input*" was successful in reducing the input passive inductor ripple level to 0.1 A.

The goal of this thesis was to design a hybrid active filter with much lesser values for filter components than used in an earlier implementation ([2]). Another goal was to employ more complex feedback control techniques than simple proportional feedback control already implemented by [2]. Using state feedback control, both these goals have been met.

2.6 Proportional Feedback Control Design for Hybrid APF

Feedback control using a single state (voltage across output passive capacitor "Cp") of the hybrid filter to determine the error was used successfully by [2] to meet Military STD 461 combining it with constant duty cycle control. However the filter's physical size reduction was not satisfactory as shown in Table 2.2.

The block diagram of the proportional feedback control compensation scheme is shown in Figure 2.43. It should be noted that proportional control is a special case of full state feedback control. This is analogous to including only one element in the state feedback gain vector in equation 2.50. The state space equations developed for the detailed model in section 2.4 are used as a reference here to explain this analogy. The state variable vector is

$$\begin{bmatrix} I_{lp} \\ V_{cp} \\ I_{la} \\ V_{ca} \end{bmatrix} \qquad \textbf{2.51}$$

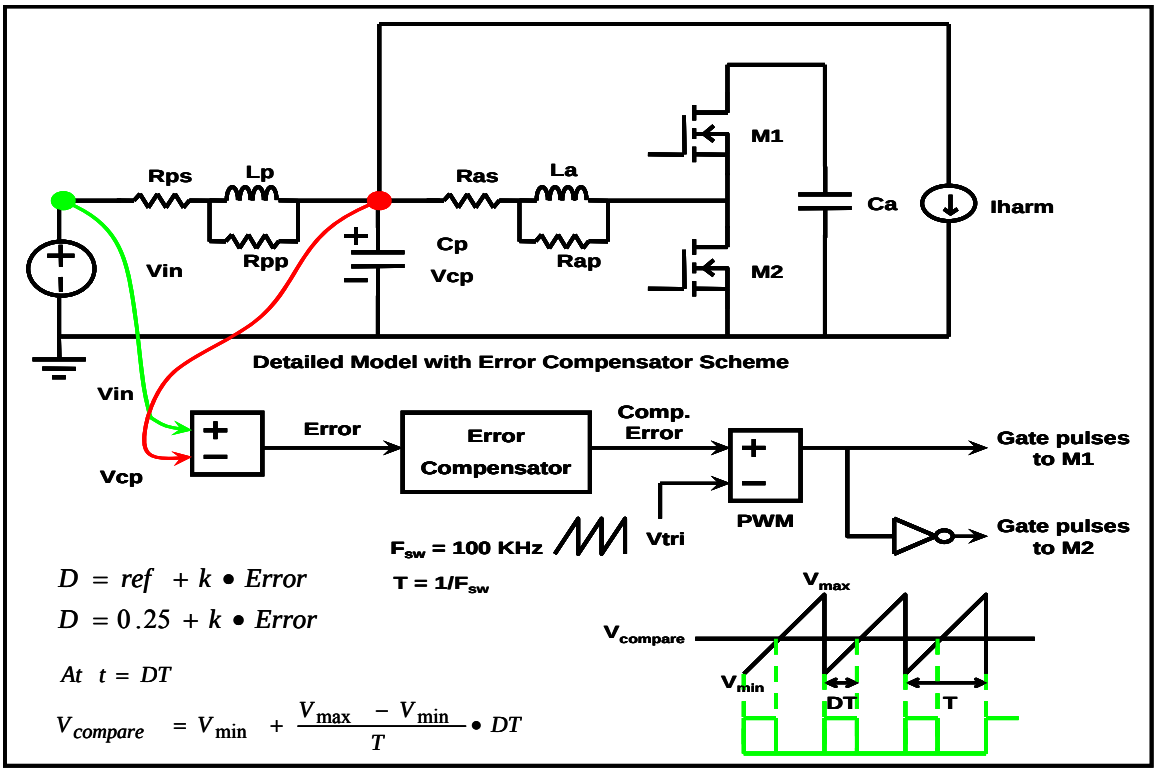


Figure 2.43 Detailed Model of Hybrid APF with Proportional Compensator

The second element of this vector is the state variable used for determining the error as shown in Figure 2.43. For proportional feedback control implementation, the following modification is made to the state feedback gain vector from equation 2.50. This is shown in equation 2.52.

$$k_{proportional} = [0.0, -0.175, 0.0, 0.0] \qquad \textbf{2.52}$$

With the above gain vector, simulations are run with the earlier developed Simulink model of the hybrid filter. The results from this simulation are shown successively from Figure 2.44 to Figure 2.48.

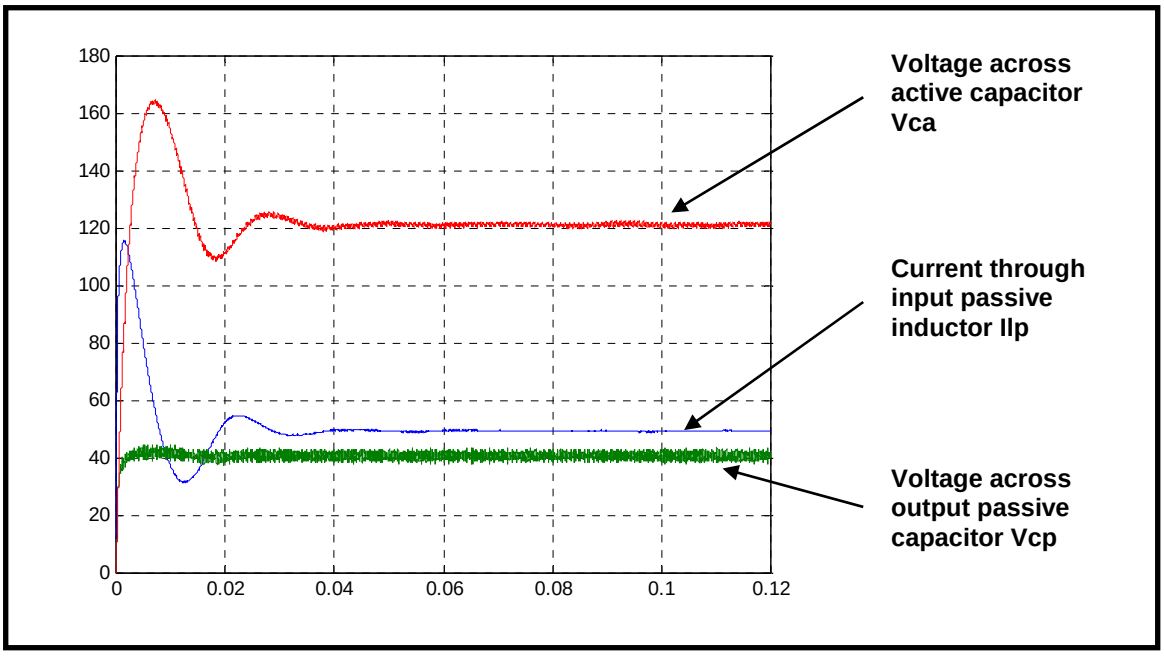


Figure 2.44 Hybrid APF Proportional Feedback Control Output

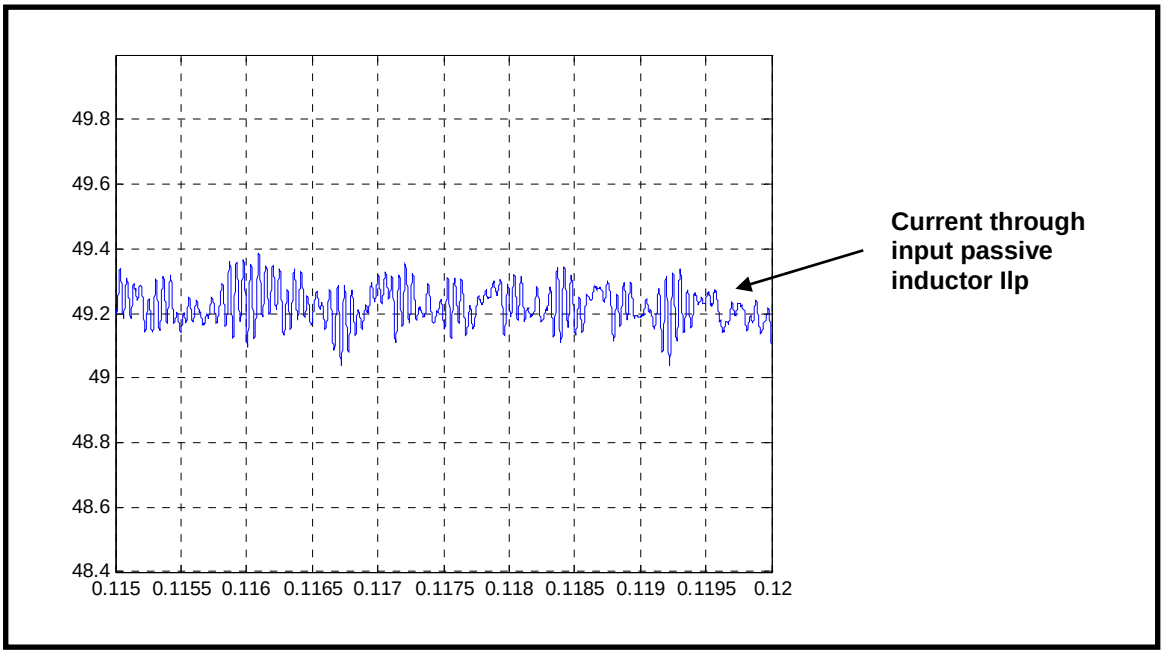


Figure 2.45 Hybrid APF Proportional Feedback Control Output Ilp

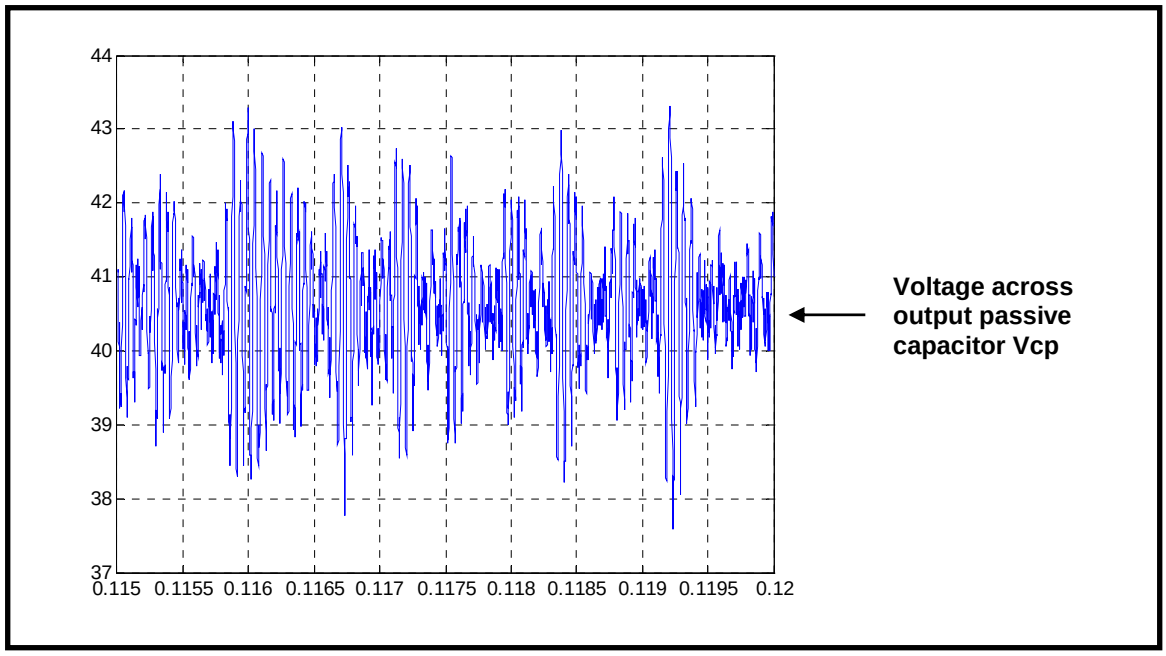


Figure 2.46 Hybrid APF Proportional Feedback Control Output Vcp

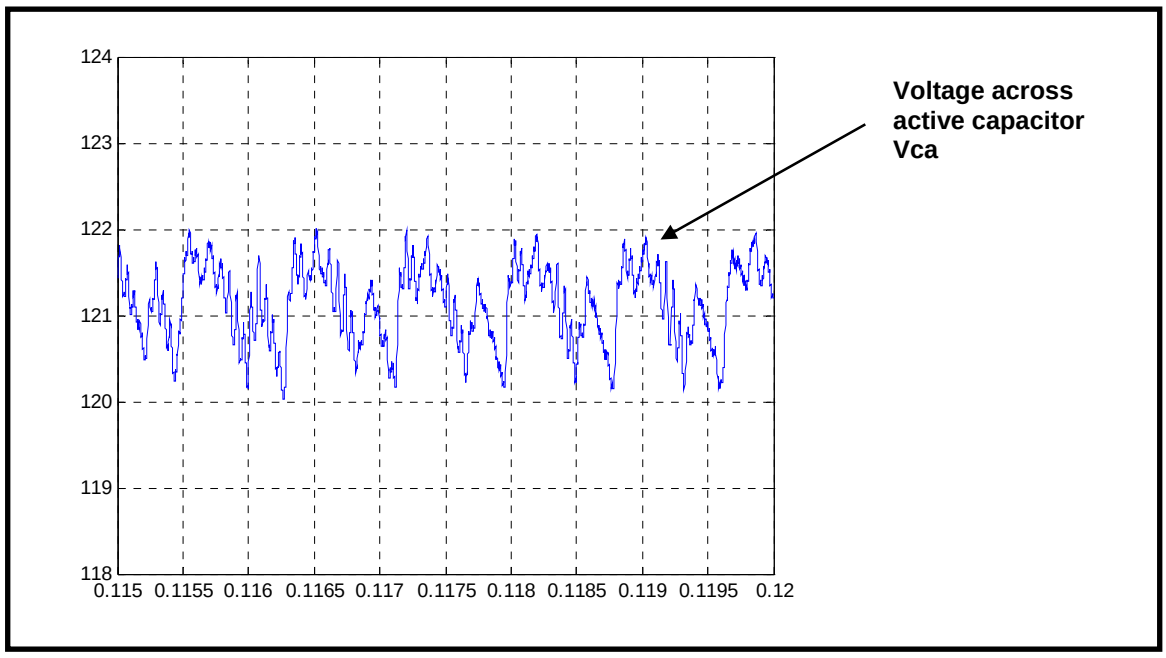


Figure 2.47 Hybrid APF Proportional Feedback Control Output Vca

The spectrum plot from proportional feedback control also reveals that the hybrid filter meets Mil STD 461. The output parameters from this simulation are summarized in Table 2.7.

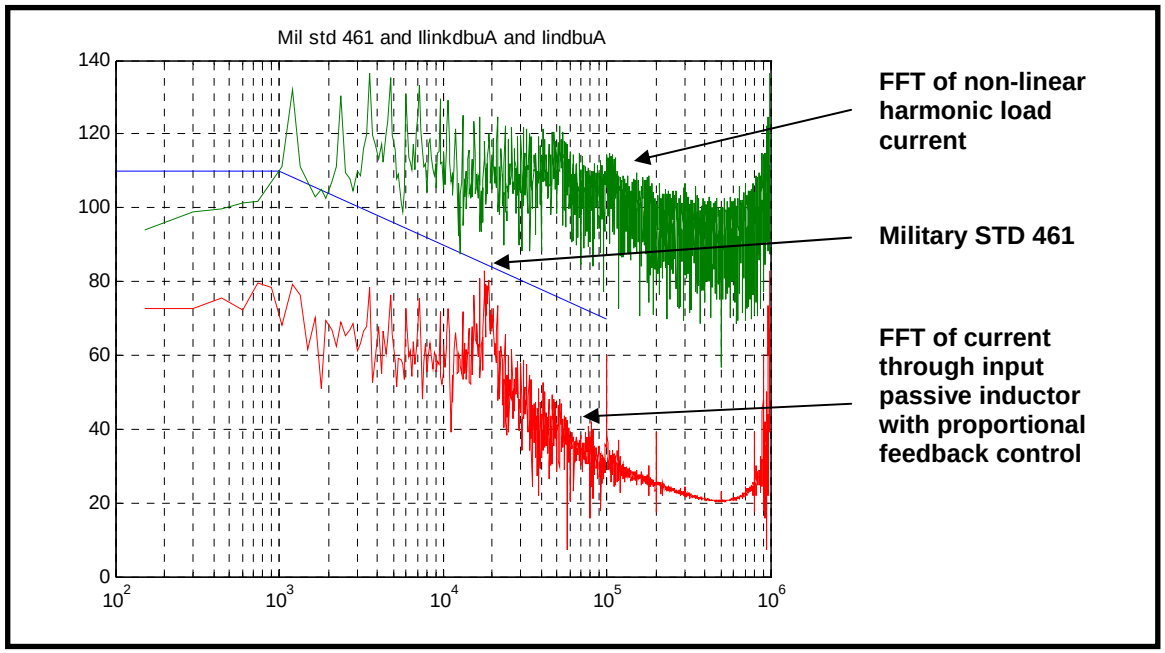


Figure 2.48 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 for Proportional Feedback Control

Table 2.7 Summary of Proportional Feedback Control Simulation

Proportional Feedback Control	Value
Mean input passive inductor current	49.2 A
Input passive inductor ripple current	+- 0.15 A
Mean output capacitor voltage	40.5 V
Output capacitor ripple voltage	+- 2.5 V
Mean active capacitor voltage	121 V
Active capacitor ripple voltage	+- 1 V
Mil STD 461	Meets STD
Margin to Mil STD 461 (at 100 kHz)	40 dB

It should be noted that the FFT plot from this simulation is very similar to the earlier obtained FFT plots from state feedback control simulations. The following comparisons are with respect to the results obtained from the third attempt of state feedback control. The current through the input passive inductor Lp has an average value of 49.2 A. This is greater by around 4 A. The AC component in this current around the steady state value is around 0.15 A. This ripple content is slightly higher by around 0.05 A. The voltage across the output passive capacitor Cp has an average value of 40.5 V with +- 2.5 V ripple. It should be noted that this ripple content level has increased by around 0.5 V. The voltage across the active capacitor Ca has an average value of 121 V with +- 1 V ripple. The mean active capacitor voltage has increased by around 20 V. However, the ripple content in this voltage has remained the same. Finally, the gain margin at 100 kHz has reduced by around 5 dB. This comparison of results from the third attempt of state feedback control and proportional feedback control reveal that the former control method is relatively better.

2.7 Proportional Integral (PI) Feedback Control Design

In this section, a PI/PID feedback compensation design is completed to see if presents a viable option for implementation. The circuit model for PI/PID feedback compensation is shown in Figure 2.49.

The PI/PID feedback compensation design starts with the small signal system's transfer function (section 2.5.1) which reveals that the system is a type '0' system (system that has no poles at the origin). The input to this system is the duty cycle which is a scalar value (a constant average value). This is equivalent to a step input with the average value of the duty cycle as the magnitude. A type '0' system cannot follow a step input. This is explained below. The position constant for a SISO system is given by equation 2.53 [31, 32].

$$Kpos = \frac{\lim}{s \to 0} G_{eq}(s) \qquad \textbf{2.53}$$

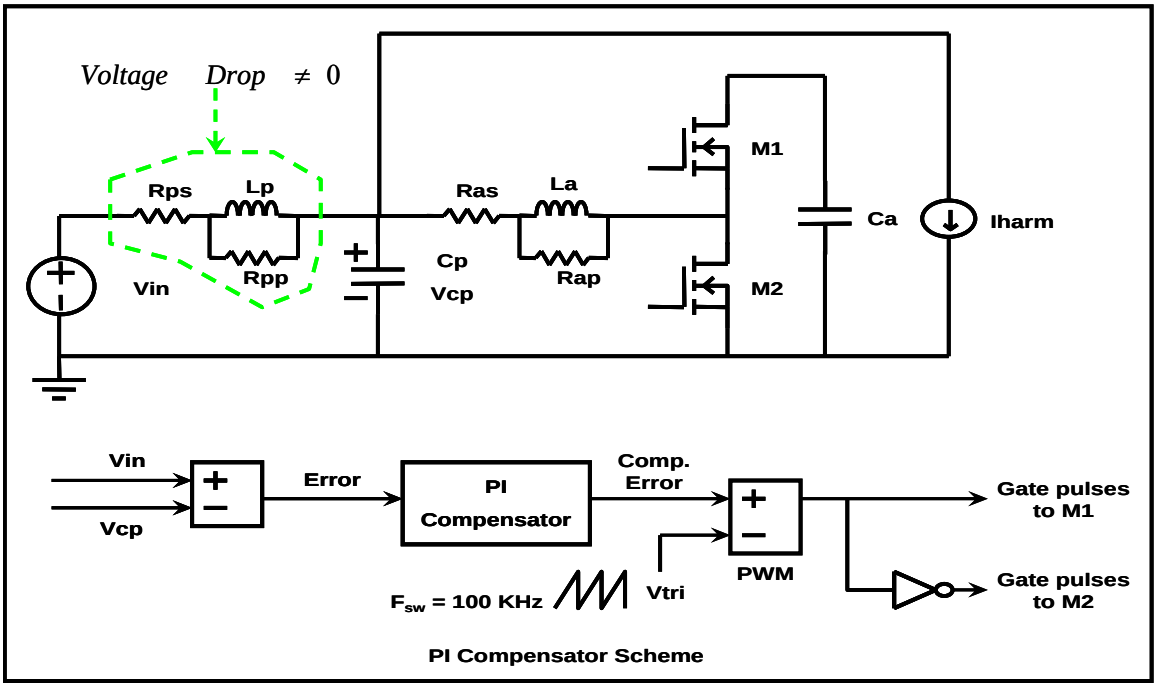


Figure 2.49 Detailed Model of Hybrid APF with PI Control

This when applied to the 4th order system given in equation 2.37 gives a non-zero value for the position constant. This is a small value in the order of 10^{-14}. The error constant corresponding to a step input for the same system is given by equation 2.54 [31, 32].

$$Ess_{step} = \frac{1}{1 + Kpos} \qquad \textbf{2.54}$$

Since the position constant is a negligible value, the error constant is 1. This shows that a type '0' system cannot follow a step input. Therefore the type number of the system has to be increased. This is possible with either a Proportional and Integral (PI) compensator or Proportional, Integral and Derivative (PID) compensator. However, both these schemes would be impractical in this case. The intent is to eliminate the voltage error which is the voltage drop across the input passive inductor "Lp". This is impossible as shown in Figure 2.49 ! Even if a piece of wire was stuck instead of an inductor between the DC voltage source and output capacitor, there would be a voltage drop. Therefore trying to eliminate this with a PI compensator is not a feasible control scheme.

2.8 Summary

A sequential approach was used to obtain an effective model of the hybrid active filter and its feedback control scheme. The original benchmark passive filter formed the basis for active filter design. The harmonic generating non-linear load was discussed to emphasize the need for filtering. Following this, a model for the active filter was developed. Constant duty cycle (open loop control) was discussed followed by feedback control schemes starting with state feedback control. Proportional feedback control being a special case of state feedback was shown. Following this, PI/PID feedback control not being a viable control technique was discussed. The simulation results obtained show that state feedback control is the most effective control scheme. Therefore, state feedback control is the proposed design. The following chapter deals with verification of this proposed design along with the hybrid filter's experimental setup and other concerned issues.

3 Hybrid Active Power Filter – Experimental Design

3.1 Introduction

This chapter deals with the experimental design of the hybrid active filter. The non-linear load which is the source of the ripple in the input current is described. In the previous chapter, the hybrid active filter was simulated in the Simulink environment. Here, a SPICE model is created. This SPICE filter model is coupled to the load and simulated. The results from SPICE simulation are compared to the ones from the Simulink simulation. Inferences are finally presented.

The SRM drive model from chapter 2 is the real non-linear load whose input harmonic current is to be filtered by the hybrid active filter that is the subject of this thesis. However, a SRM drive was not available to evaluate the performance of the designed hybrid active filter. The current drawn by the SRM drive can be treated as a harmonic current source as shown in Figure 2.2 and Figure 2.9 for ease in analysis and representation. This suggests using an equivalent non-linear load circuit [2]. The SPICE circuit of the non-linear load used to generate an equivalent current to filter is shown in Figure 3.1.

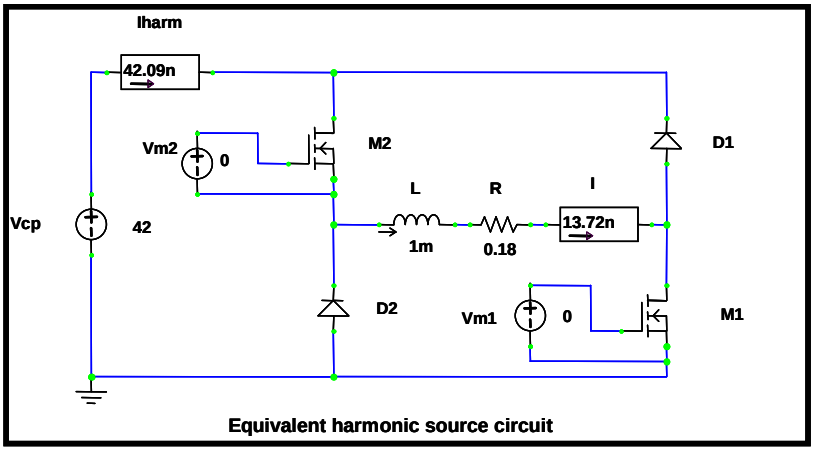
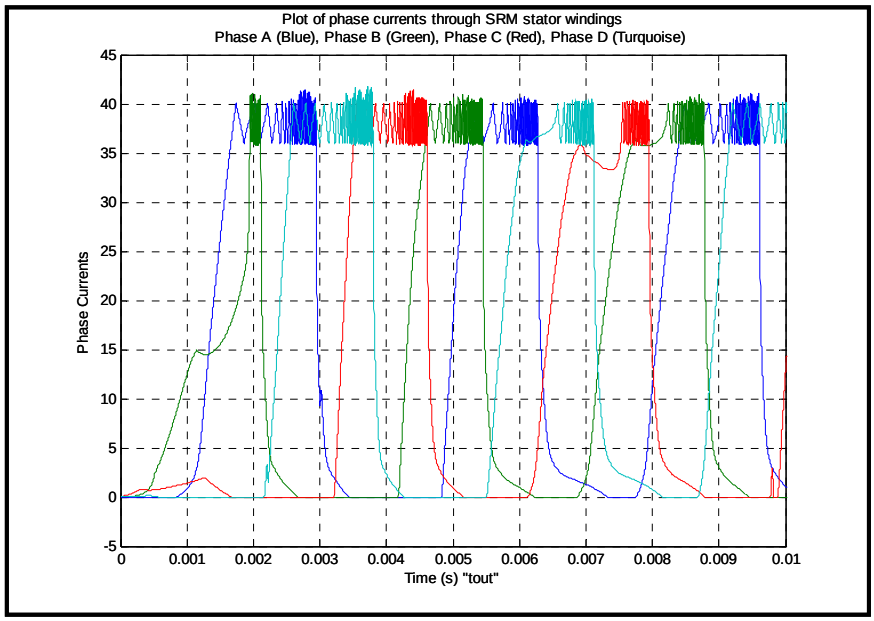
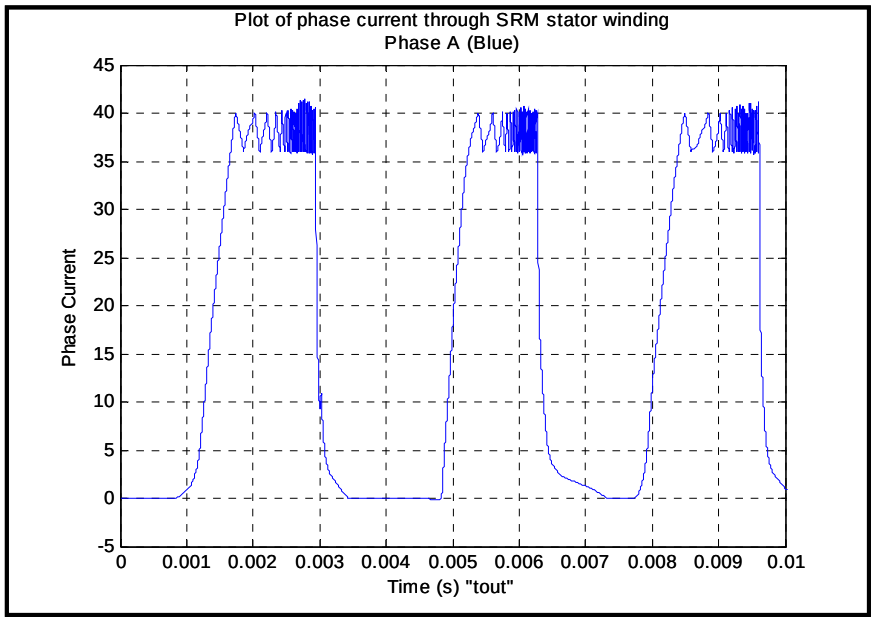


Figure 3.1 SPICE Equivalent Load Circuit

Prior to analyzing the current through the load inductor in the equivalent load circuit and the resulting current drawn from the constant DC voltage source a review of the corresponding currents from the Simulink SRM drive model are reviewed for comparison. The phase currents for the four phase SRM are shown in Figure 3.2 (a) with a single phase's current isolated in Figure 3.2 (b).



(a)



(b)

Figure 3.2 Phase Currents through SRM Stator Windings

The current into the SRM drive (I_{harm}) is equal to the sum of the four switched phase currents in the upper IGBTs or diodes of the SRM inverter. The time period during which each phase is ON is one quarter of the fundamental frequency (F_{fund} = 1200 kHz) of the current into the drive due to all four phases. In addition there is a frequency component due to the semiconductor switching within a cycle as well has harmonic frequencies. The design of the equivalent SRM drive circuit and the choice of switching frequency of its switches is driven by the frequency content of the drive current to be generated. The equivalent SRM drive circuit in Figure 3.1 is a simple H-bridge topology and is equivalent to one phase of the actual SRM drive circuit (the SRM drive being the non-linear load). The inductor L plays the role of one phase of the 4 phase (2 poles per phase) stator winding of the 8/6 SRM.

The gate to source voltage for both the MOSFETs M1 and M2 are turned ON and OFF at the same time. Current flows through the inductor L (with its equivalent series resistance of R) in the direction of the arrow mark when the two MOSFETs are ON. The diodes D1 and D2 ensure that the inductor current is continuous when the MOSFETs are turned OFF. This is necessary because an inductor inherently opposes change in the current flowing through it. The absence of a current path when MOSFETs are turned OFF would result in a large di/dt with a corresponding large voltage across the MOSFETs resulting in their breakdown and subsequent failure.

The current flowing through the load inductance L and the resulting current drawn from the constant DC voltage source are shown in Figure 3.3. The current through the equivalent drive load will have same time period as the current in each phase of the SRM as generated by the Simulink SRM drive model if the device gating frequency is the same for both. Since ideally the equivalent drive load is lossless the power drawn from the DC voltage source and thus the current drawn from the DC voltage source have zero average value. The current is positive when the two MOSFETs are turned ON and is negative when they are turned OFF. Thus current and energy is drawn from the source during one part of the cycle and then returned to the source during the remaining part of the cycle.

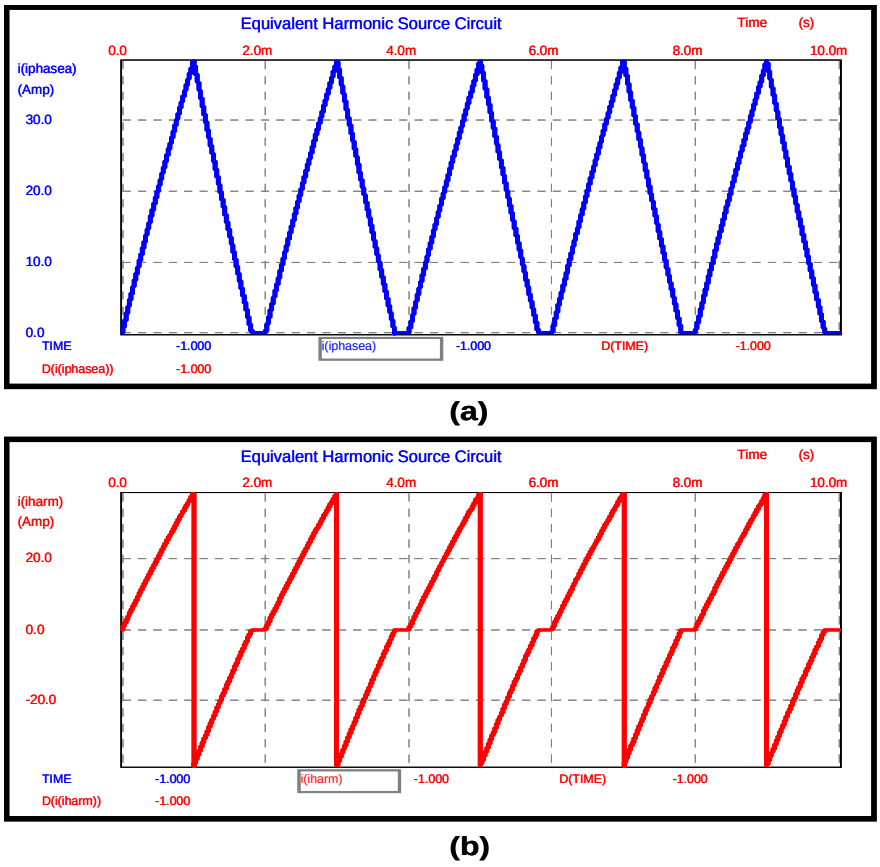


Figure 3.3 (a) Current through load inductor L, (b) Current from the constant DC voltage source

3.2 Detailed Model of the Hybrid Active Power Filter (HAPF) with Constant Duty Cycle Control Simulation in Simulink

In this section the detailed model of the HAPF is revisited. Here the detailed model is simulated with the equivalent drive load circuit used in the experiments for constant duty cycle control.

The Simulink model described in chapter 2 is used with the Simulink SRM drive's generated harmonic current I_{harm} (to be filtered by the proposed APF), replaced with the repeating sequence of current in Figure 3.3 (b). The block diagram for this simulation is shown in Figure 3.4.

The results obtained with this model for a 25 % steady state duty cycle are shown successively from Figure 3.6 to Figure 3.10.

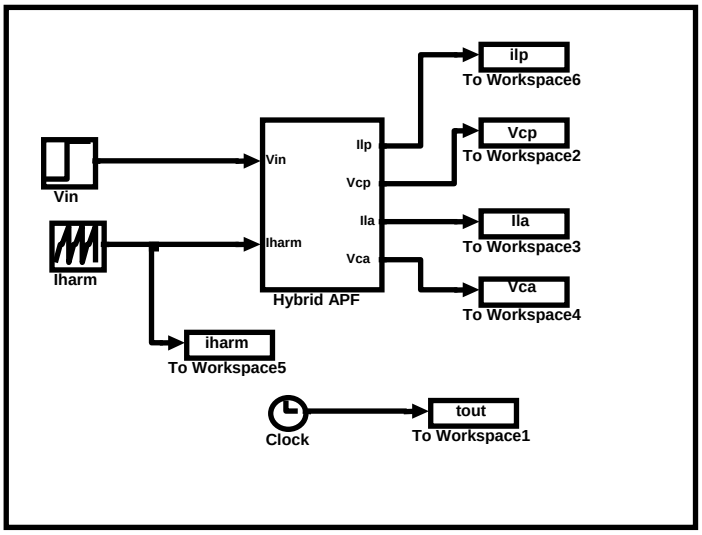


Figure 3.4 Simulink Filter Model with Harmonic Current Source

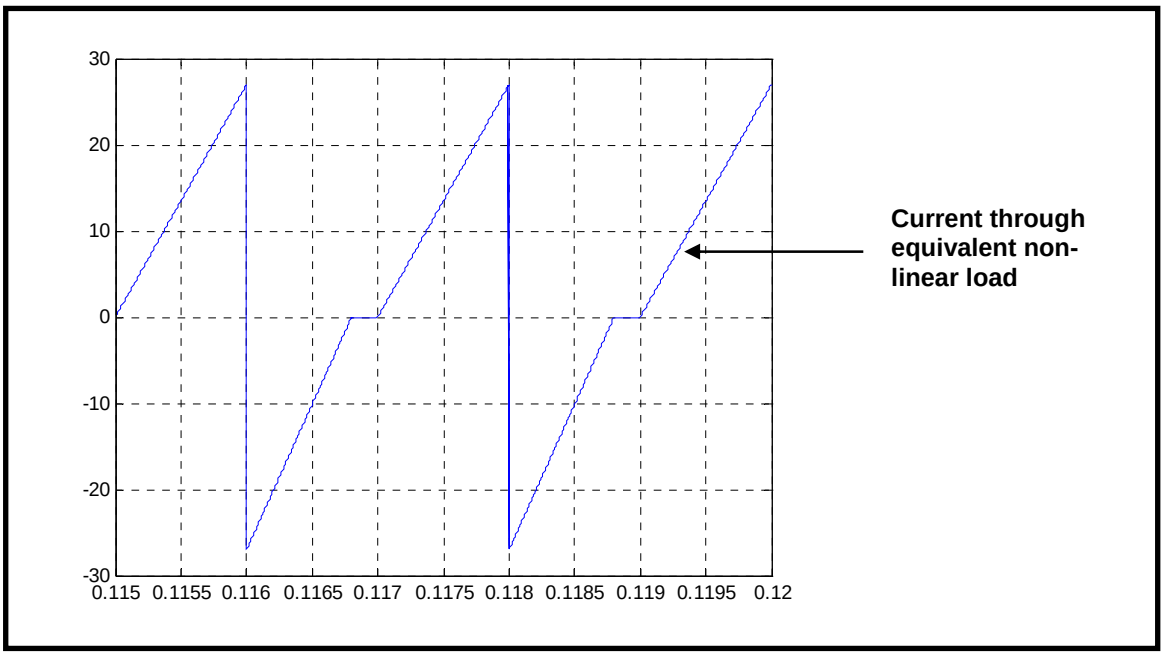


Figure 3.5 Equivalent Drive Load Current I_{harm}

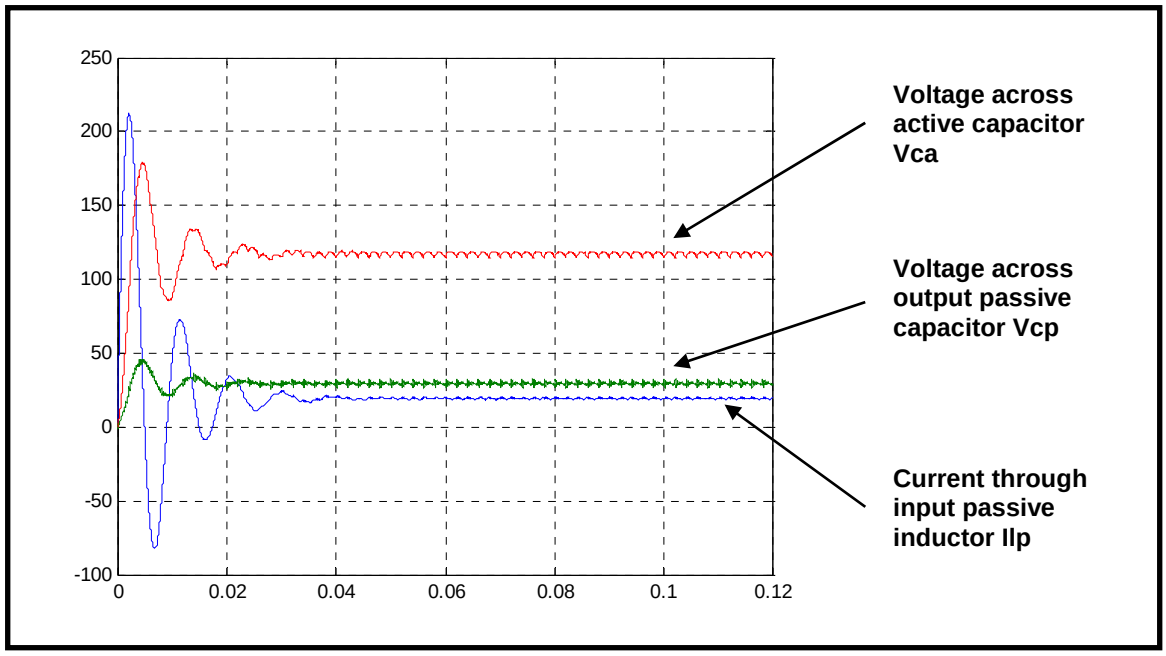


Figure 3.6 Hybrid APF with Equivalent Drive Load under Constant Duty Cycle Control Output

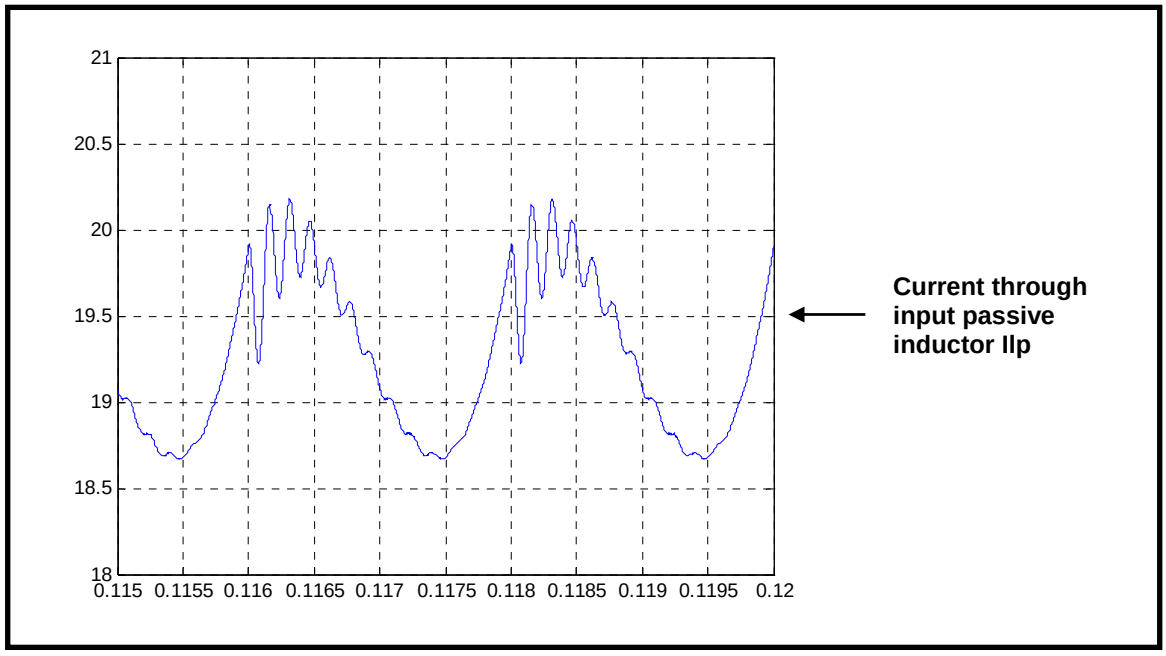


Figure 3.7 Hybrid APF with Equivalent Drive Load Output Ilp

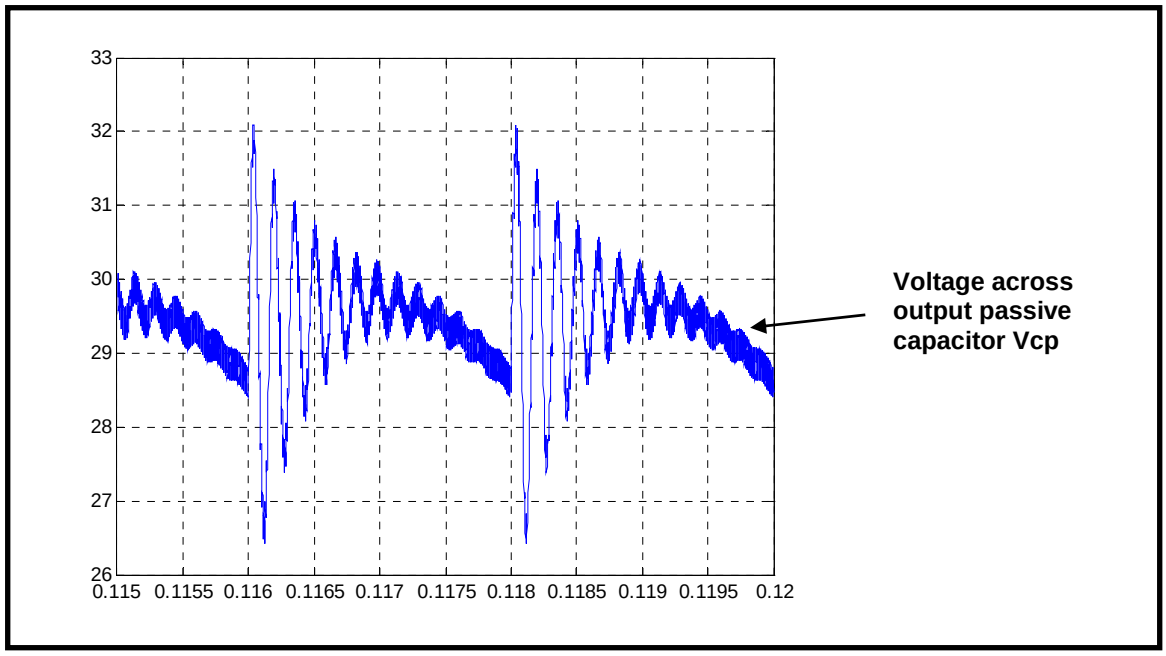


Figure 3.8 Hybrid APF with Equivalent Drive Load Output Vcp

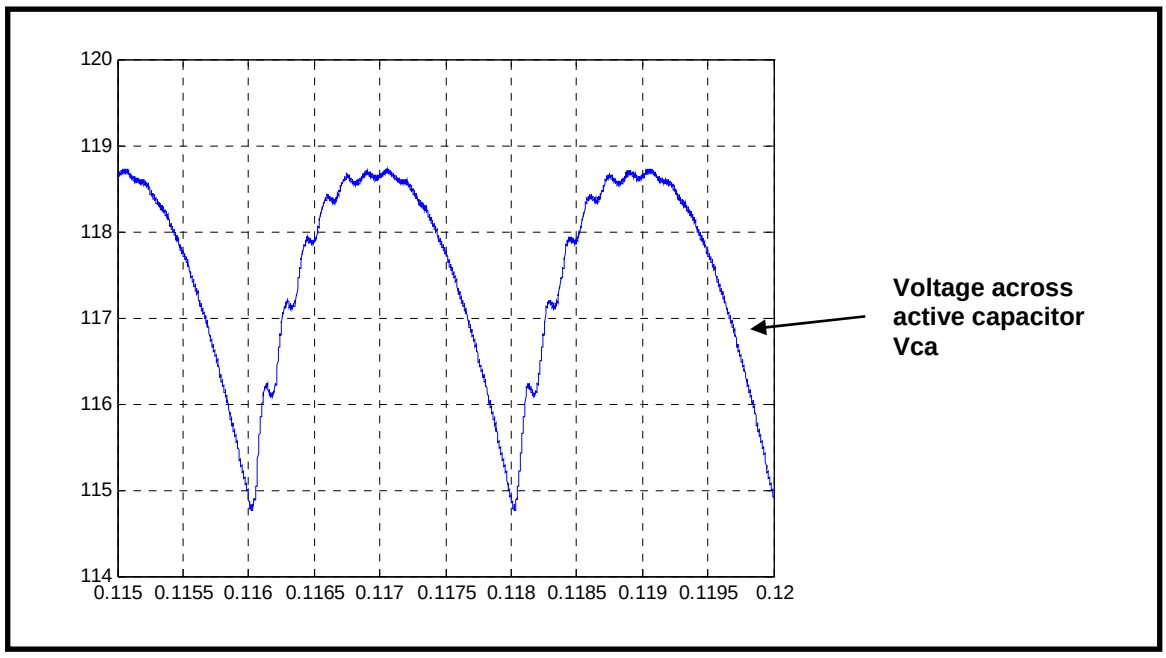


Figure 3.9 Hybrid APF with Equivalent Drive Load Output Vca

The spectrum plot from constant duty cycle operation of the hybrid APF with equivalent non-linear load shows that it meets Mil STD 461.

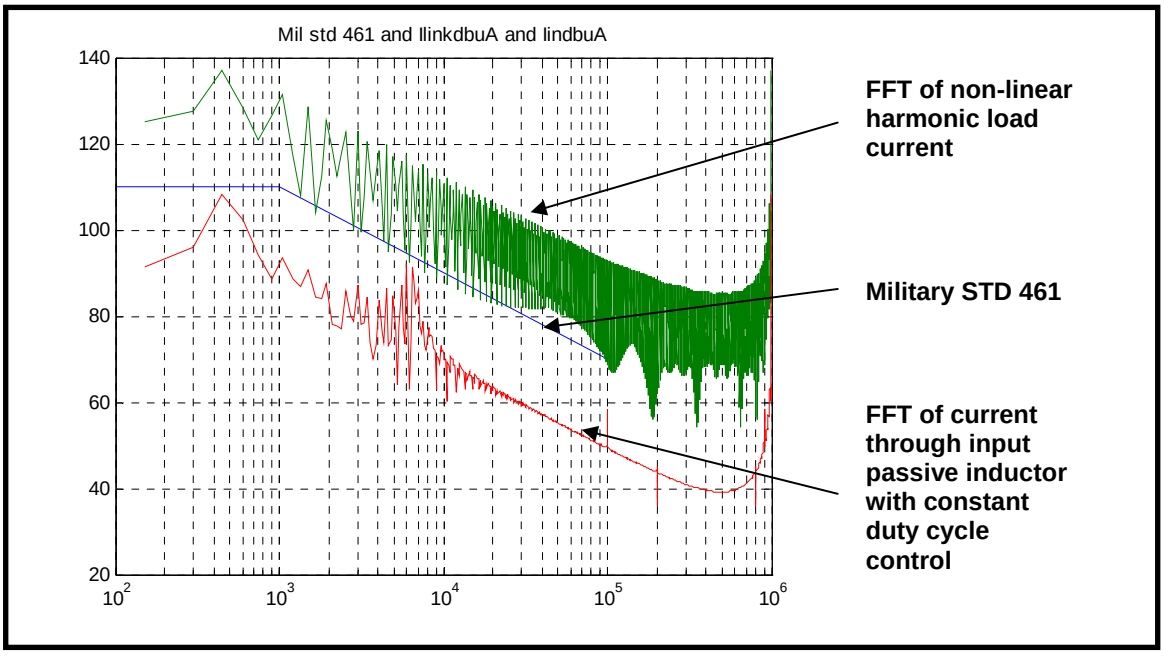


Figure 3.10 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 for Hybrid APF with Equivalent Drive Load under Constant Duty Cycle Control

Table 3.1 Summary of Constant Duty Cycle Simulation of Hybrid APF with Equivalent Drive Load

Constant Duty Cycle Control of Hybrid APF with Equivalent Drive Load	Value
Mean input passive inductor current	19.4 A
Input passive inductor ripple current	+- 0.7 A
Mean output capacitor voltage	29.3 V
Output capacitor ripple voltage	+- 2.8 V
Mean active capacitor voltage	116.75 V
Active capacitor ripple voltage	+- 2 V
Mil STD 461	Meets STD
Margin to Mil STD 461 (at 100 kHz)	20 dB

The output parameters from this simulation are summarized in Table 3.1. In this simulation, the input voltage was reduced from 42 V to 30 V for ease of testing in the laboratory environment. It should be noted that though constant duty cycle control is used, the hybrid APF just meets Military STD. 461. The gain margin at 100 kHz is around 20 dB. Simulations from sections 2.5 and 2.6 of the hybrid APF meet the Military STD 461 with large gain margins of 45 dB and 40 dB at 100 kHz. In addition earlier results from section 2.4 show that constant duty cycle is not suitable for operation of the hybrid filter with SRM drive load. These results are conflicting.

The reason the hybrid APF coupled with this equivalent drive load meets Military STD. 461 may be due to the load approximated as being much simpler than the SRM drive load which is the real source of ripple considered in this thesis. Therefore in the following section, feedback control of the hybrid APF with the equivalent drive load is proposed.

3.3 Detailed Model of the Hybrid APF with Proportional Feedback Control in Simulink

In this section the detailed model of the HAPF is simulated with the equivalent drive load circuit which will be used in the experimental testing of the proportional feedback control. It was concluded in chapter 2 that full state feedback was marginally better than plain proportional feedback control as a control technique for this thesis design problem.

As discussed in section 2.5, full state feedback necessitates use of direct or indirect techniques for signal estimation which is used for feeding back individual states. This technique increases circuit complexity while being marginally better in reducing input current ripple. Plain proportional feedback control is therefore chosen due to its ease of implementation in this thesis. The Simulink model used for this simulation is exactly the same as the one used in section 2.6 except that the SRM drive load is replaced with a harmonic current source as shown earlier in Figure 3.4. A quiescent operating duty cycle of 25 % was used here. The hybrid APF model was simulated with the gain of 0.175 found in section 2.6. The simulation results obtained are shown successively from Figure 3.11 to Figure 3.15.

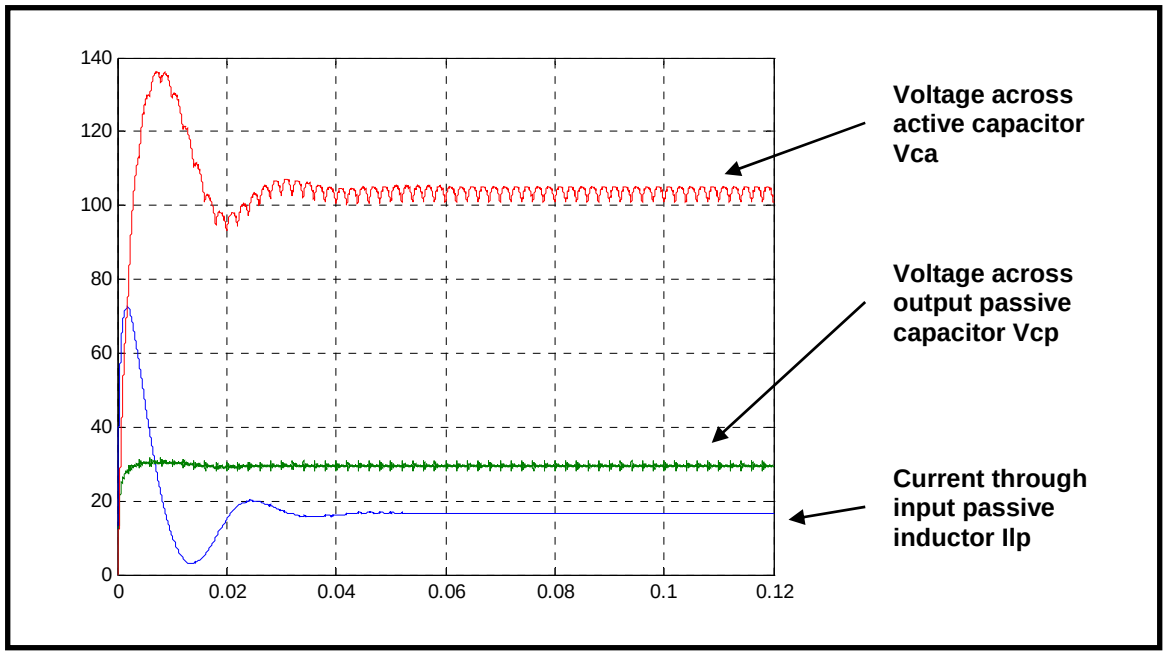


Figure 3.11 Proportional Feedback Control of Hybrid APF with Equivalent Drive Load Output (First Attempt)

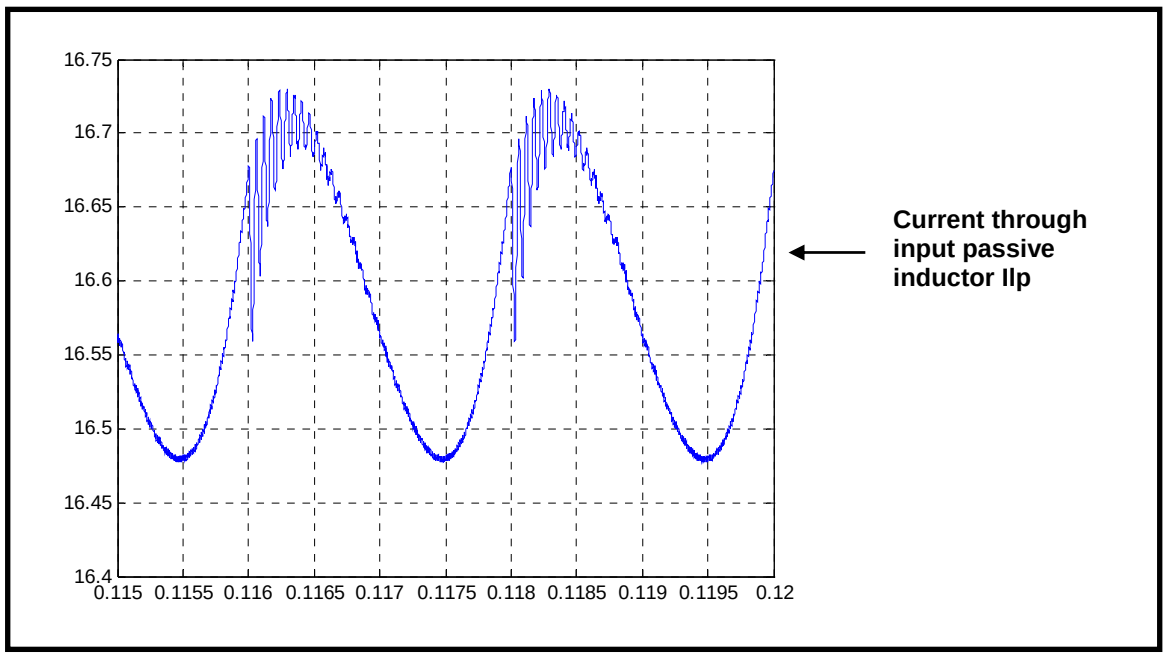


Figure 3.12 Proportional Feedback Control of Hybrid APF with Equivalent Load Circuit Output Ilp (First Attempt)

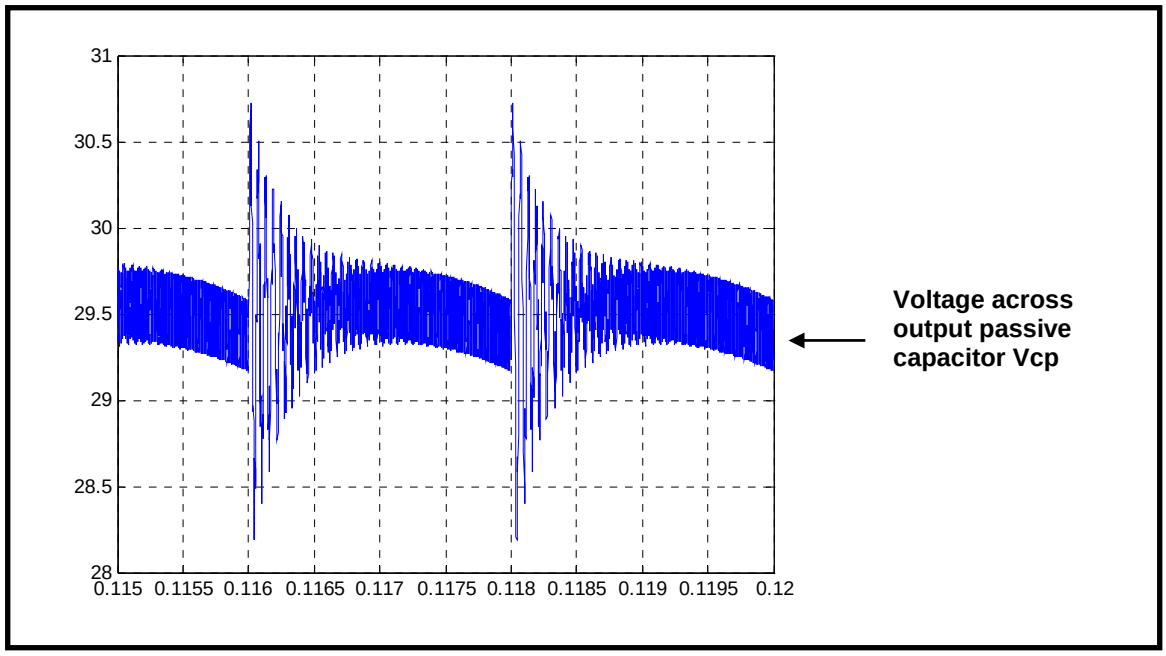


Figure 3.13 Proportional Feedback Control of Hybrid APF with Equivalent Load Circuit Output Vcp (First Attempt)

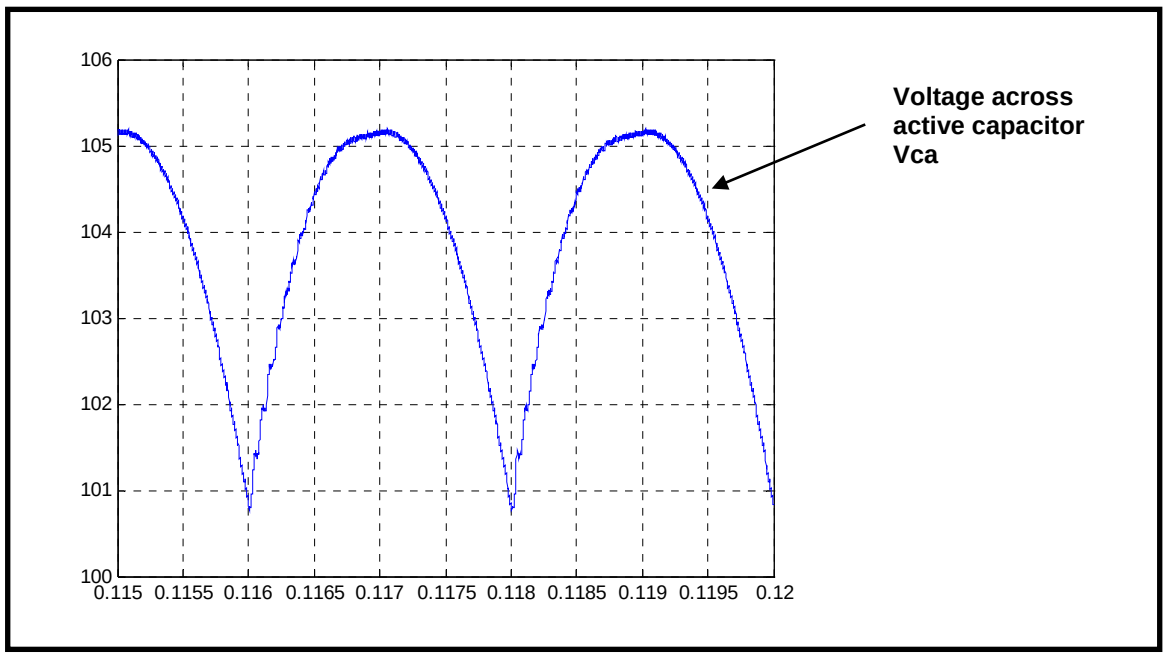


Figure 3.14 Proportional Feedback Control of Hybrid APF with Equivalent Load Circuit Output Vca (First Attempt)

The spectrum plot from proportional feedback control of the hybrid APF with equivalent drive load shows that it meets Mil STD 461.

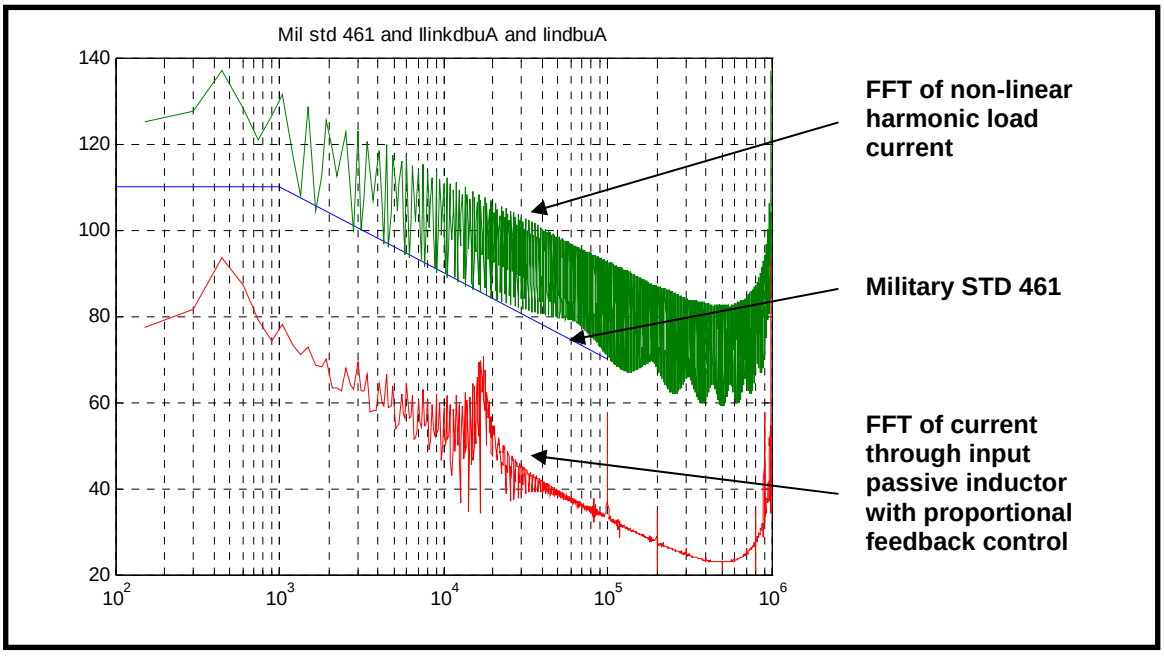


Figure 3.15 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 of Hybrid APF with Equivalent Drive Load for Proportional Feedback Control (First Attempt)

Table 3.2 Summary of Hybrid APF with Equivalent Drive Load with Proportional Feedback Control (First Attempt)

Proportional Feedback Control of Hybrid APF with Equivalent Drive Load	Value
Mean input passive inductor current	16.6 A
Input passive inductor ripple current	+- 0.125 A
Mean output capacitor voltage	29.5 V
Output capacitor ripple voltage	+- 1.25 V
Mean active capacitor voltage	103 V
Active capacitor ripple voltage	+- 2.25 V
Mil STD 461	Meets STD
Margin to Mil STD 461 (at 100 kHz)	40 dB

The output parameters from this simulation are summarized in Table 3.2. The results from this simulation in Table 3.2 are compared with the earlier results in Table 3.1.

With proportional feedback control, the ripple content in the input current has reduced from +- 0.7 A to +- 0.125 A while the mean input current value has decreased by around 3 A. In addition the ripple content in output voltage had reduced from +- 2.8 V to +- 1.25 V while the mean output voltage hasn't changed significantly. The ripple content in active capacitor voltage is almost the same and the mean value has reduced by around 14 V.

Also, the gain margin has increased from 20 dB to 40 dB at 100 kHz. This current ripple is also close to the current ripple with the baseline passive EMI filter with SRM drive load which had a value of +- 0.1 A. This can be attributed to the relatively less complex non-linear load considered in this experimental circuit model. Though the mean value of the input current has reduced by 3 A, it is still high at around 16 A.

Results from constant duty cycle operation summarized in Table 2.3 show that if duty cycle is increased, the current drawn from the DC power supply reduces while its ripple content increases.

However, with feedback control this ripple can be attenuated to a level such that EMC standards are met. Therefore another simulation trial is proposed for feedback control with a quiescent operating duty cycle of 50 %. Simulation outputs for this run are shown successively starting from Figure 3.16 to Figure 3.20.

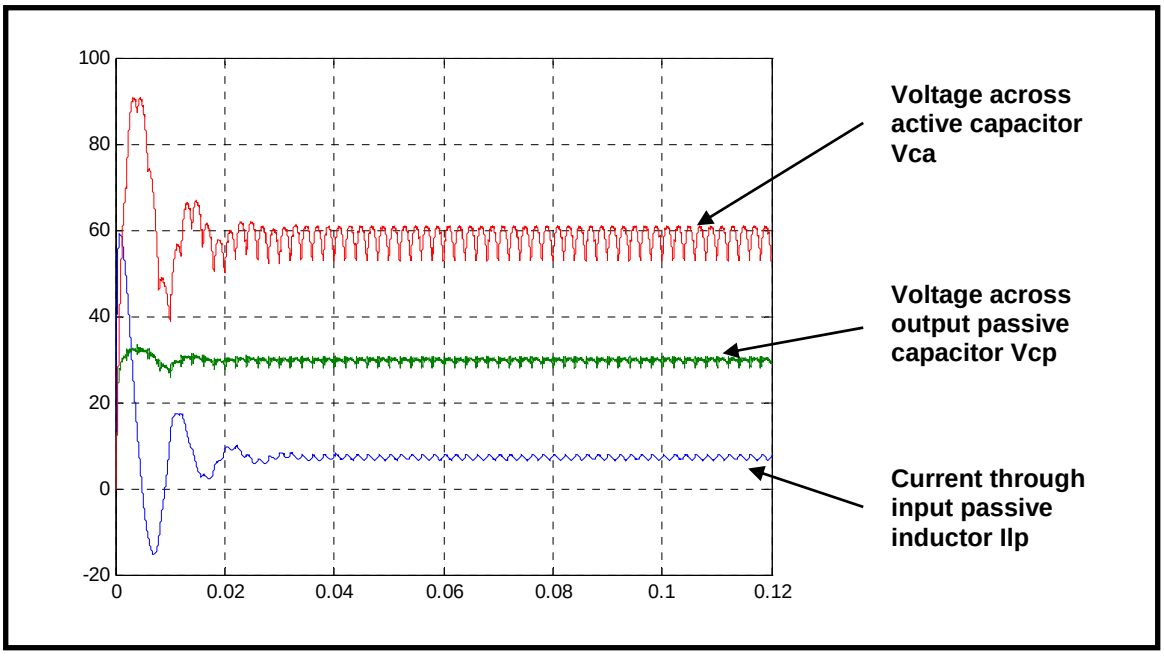


Figure 3.16 Proportional Feedback Control of Hybrid APF with Equivalent Drive Load Output (Second Attempt)

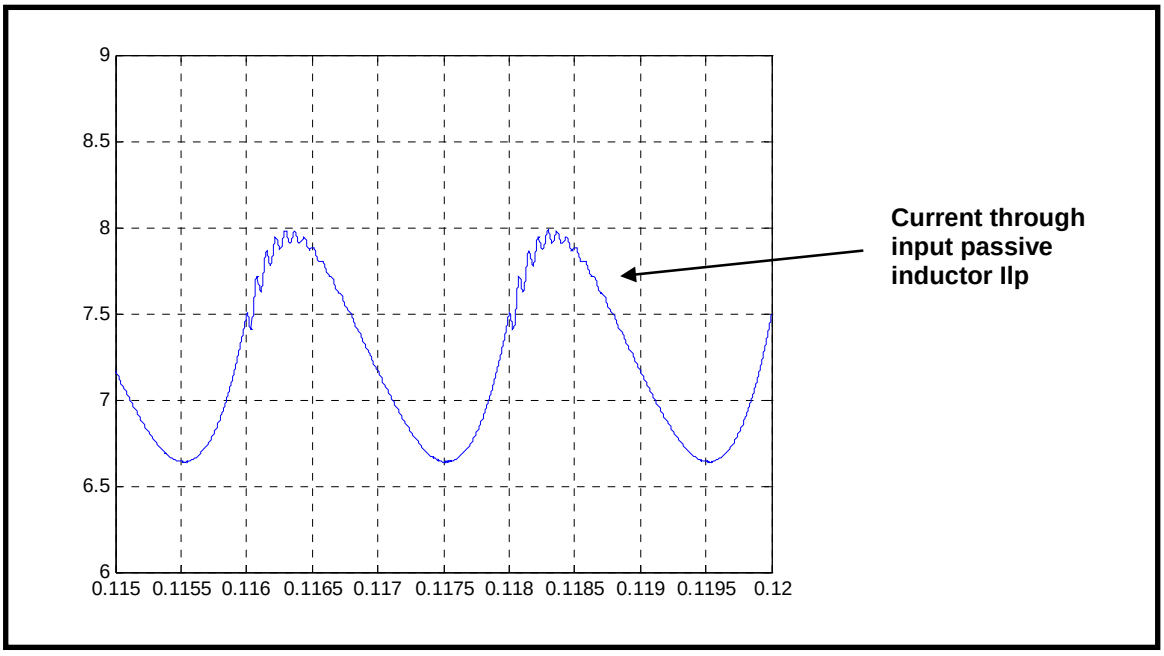


Figure 3.17 Proportional Feedback Control of Hybrid APF with Equivalent Load Circuit Output Ilp (Second Attempt)

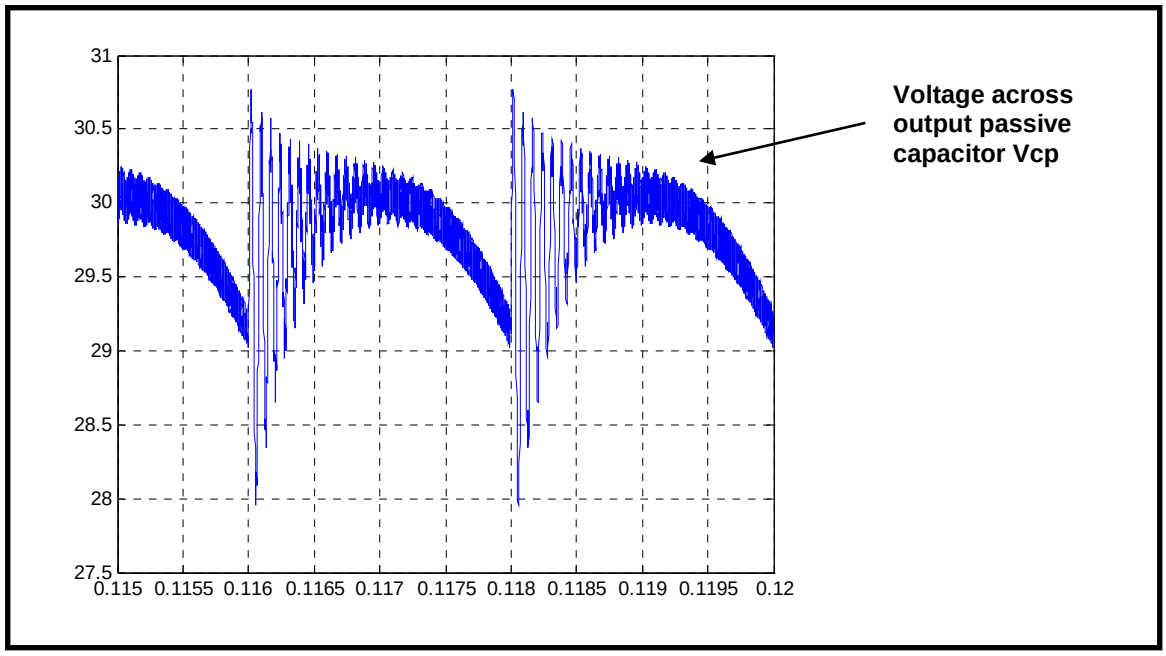


Figure 3.18 Proportional Feedback Control of Hybrid APF with Equivalent Load Circuit Output Vcp (Second Attempt)

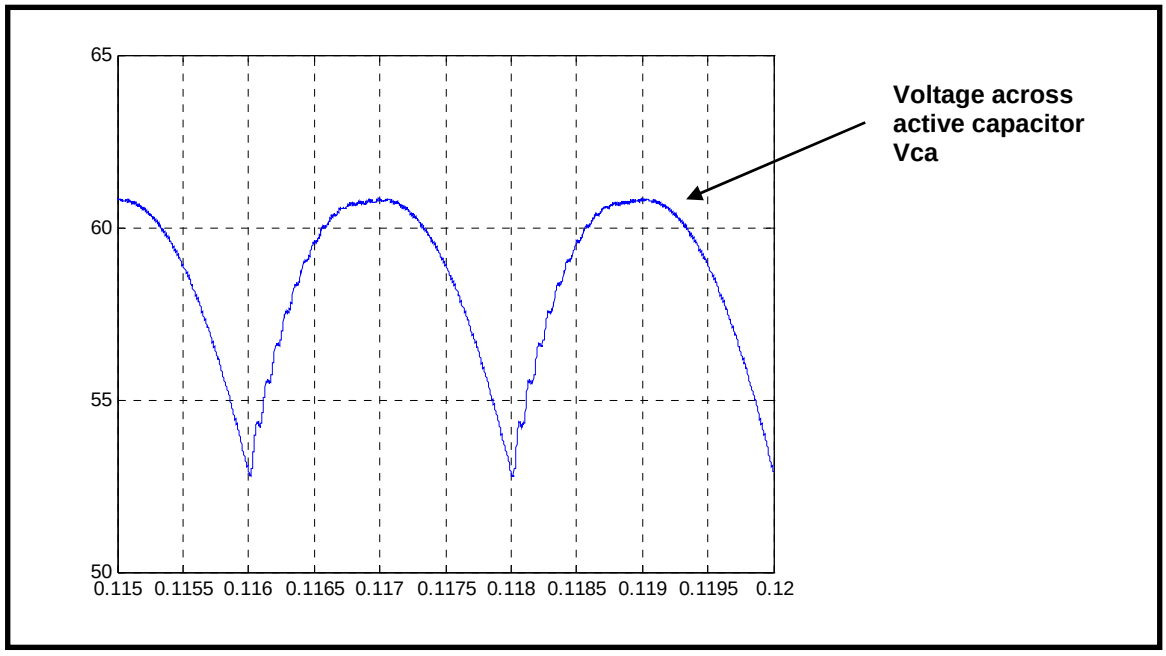


Figure 3.19 Proportional Feedback Control of Hybrid APF with Equivalent Load Circuit Output Vca (Second Attempt)

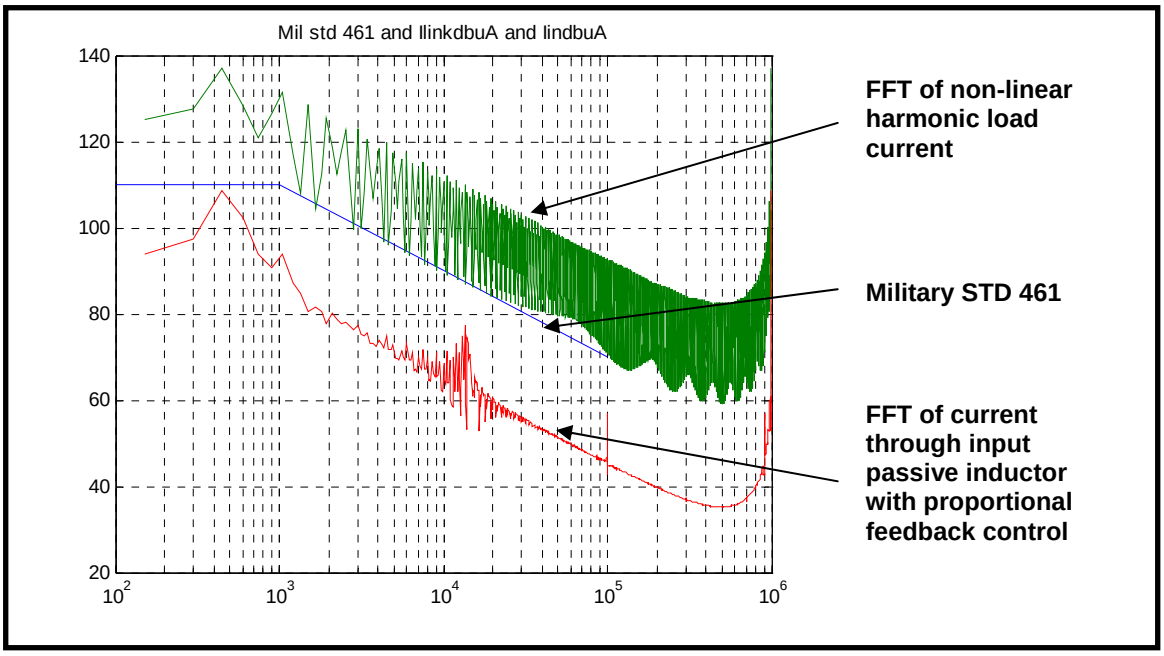


Figure 3.20 Spectrum plot of Input Passive Inductor Current, Load Current I_{harm} and Military STD 461 of Hybrid APF with Equivalent Drive Load for Proportional Feedback Control (Second Attempt)

The spectrum plot from proportional feedback control of the hybrid APF with equivalent drive load shows that it meets Mil STD 461. The output parameters from this simulation are summarized in Table 3.3.

The results from 50 % duty cycle operation in Table 3.3 are compared with the results from 25 % duty cycle operation tabulated earlier in Table 3.2. By increasing the duty cycle by a factor of 2, the effective capacitance has reduced by a factor of 4. This is the reason for higher ripple content in the input current. This ripple has increased from +- 0.125 A to 0.65 A. However, the mean value of the input current has reduced by a factor of more than 2 from around 16 A to 7 A. The ripple in the output capacitor voltage hasn't changed significantly. The mean output capacitor voltage has remained almost the same. The ripple in active capacitor voltage has increased by a factor of around 2 from +- 2.25 V to 4 V. The mean active capacitor voltage has reduced by a factor of 2 from 103 V to 56.75 V. In addition, the hybrid APF with proportional feedback control operating at 50 % quiescent duty cycle still meets the Military STD. 461.

Table 3.3 Summary of Hybrid APF with Equivalent Drive Load with Proportional Feedback Control (Second Attempt)

Proportional Feedback Control of Hybrid APF with Equivalent Drive Load	Value
Mean input passive inductor current	7.3 A
Input passive inductor ripple current	+- 0.65 A
Mean output capacitor voltage	29.35 V
Output capacitor ripple voltage	+- 1.4 V
Mean active capacitor voltage	56.75 V
Active capacitor ripple voltage	+- 4 V
Mil STD 461	Meets STD
Margin to Mil STD 461 (at 100 kHz)	25 dB

However, the gain margin at 100 kHz has reduced from around 40 dB to 25 dB. The benefits of operating at this new quiescent duty cycle of 50 % are two fold. Firstly, the mean value of input current has reduced to a low value of 7.3 A, and secondly the active capacitor voltage had reduced to a low value of around 57 V. This voltage level is much easier to handle in a laboratory environment.

It was suggested by [2] to try a maximum reduction factor of 2 in the active capacitor's size and a maximum reduction factor of 10 in the output capacitor's size. The active capacitor Ca's value was reduced from 1600 uF (used in [2]) to 800 uF in this thesis. In addition the output capacitor Cp's value was reduced from 1000 uF (used in [2]) to 400 uF which is a factor of 2.5 rather than 10. Further reductions in the output capacitor Cp's size prevented the filter from meeting the Military STD. 461. It should be noted that in all the above simulations in this chapter, the filter components' size as chosen and tabulated in Table 2.2 are unchanged. Thus the above filter setup is chosen for simulation in SPICE environment which is discussed in the next section.

3.4 Detailed Model of HAPF with Proportional Feedback Control in SPICE

In this section, the SPICE circuit of the detailed model of the filter with proportional feedback control with the equivalent drive load circuit is presented. The SPICE model is necessary to verify the results from the Simulink model discussed in section 3.3 and the experimental implementation. The SPICE circuit model used in this section is shown in Figure 3.21. The components of the circuit model are explained as follows:

3.4.1 Hybrid Active Power Filter

The hybrid active filter shown below is exactly the same as the one discussed in section 2.6 with proportional feedback control.

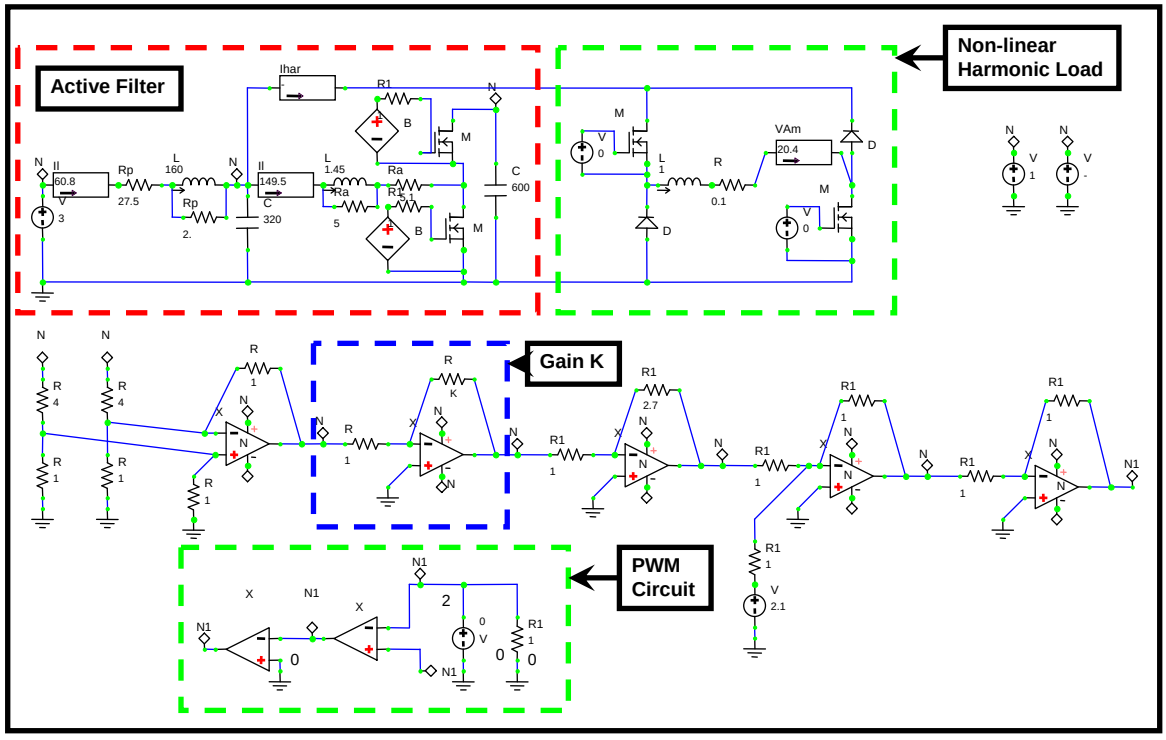


Figure 3.21 SPICE Detailed Model of the HAPF with Proportional Feedback Control

The ammeters in the above figure shown in sequence from left to right are used to measure the current from the constant DC power supply, current through the active inductance La (Ila), harmonic load current (I_{harm} which is to be filtered by the HAPF) and current through the load inductance (Vam3) respectively which was shown in Figure 3.3 (a).

3.4.2 Load Circuit

The non-linear load circuit shown in Figure 3.21 is the one which was discussed in section 3.1.

3.4.3 Error Amplifier

The first op-amp (from left to right) operates as a differential op-amp. A voltage divider with a division factor of 5 is used to reduce the constant DC voltage source value and voltage across the passive output capacitor (Vcp) to a level within the bias voltage range of the op-amp (which is +- 15 V). The error voltage is found after this voltage division. This op-amp's operation is analyzed here starting with the following figure in Figure 3.22.

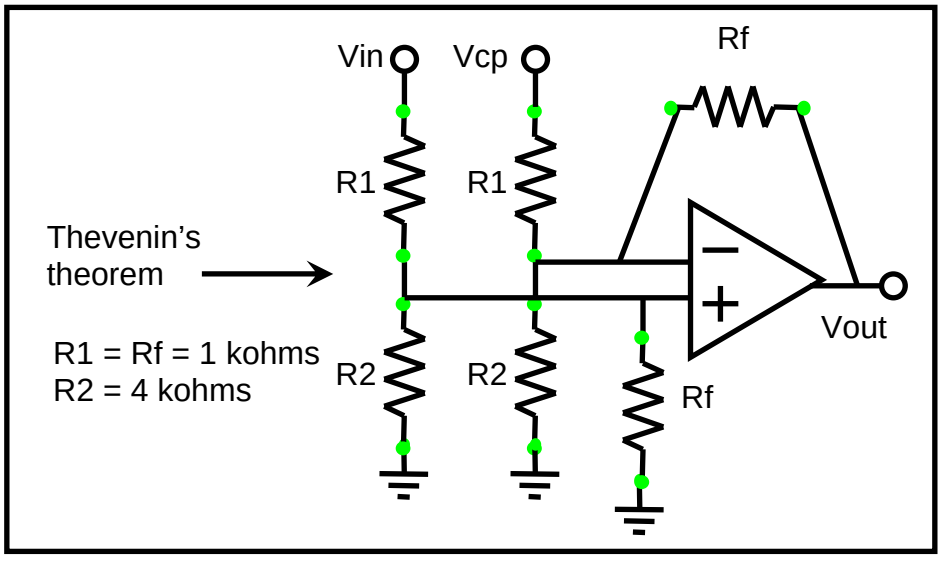


Figure 3.22 Differential Error Amplifier

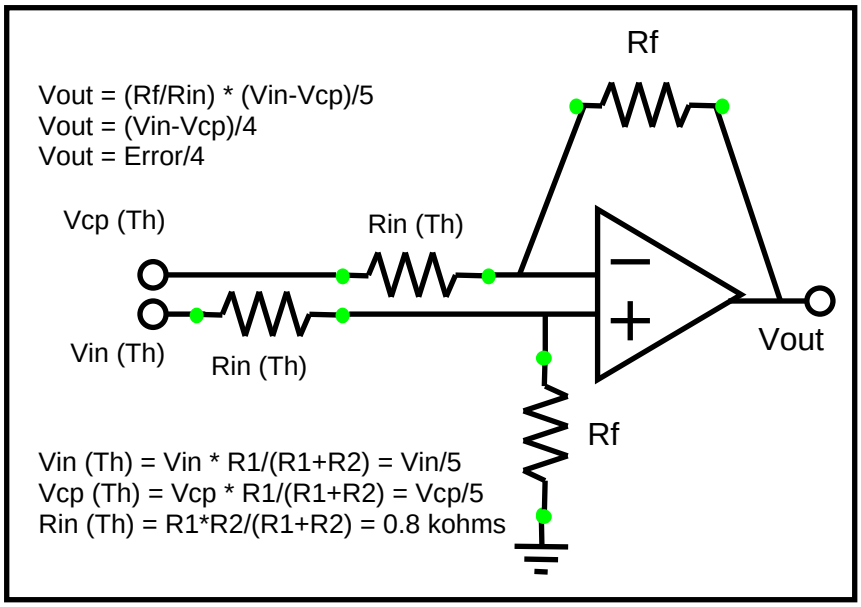


Figure 3.23 Thevenized Differential Error Amplifier

Based on the values of resistances shown in Figure 3.22, a simplified circuit schematic is shown in Figure 3.23.

The application of Thevenin's theorem leads to the final output of the differential error amplifier being an error voltage reduced by a factor of 4.

3.4.4 Gain Multiplier 1

The next op-amp (marked in blue) is a gain multiplier. The gain multiplier's gain value is found to be 0.24. This value is equivalent to the value of 0.175 found in section 2.6. This equivalence will be explained in section 3.4.6.

3.4.5 Gain Multiplier 2, Summing Amplifier and Inverter

The third op-amp (from left to right) is another gain multiplier. This is followed by a summer. These two op-amps function as per equations 2.44 – 2.48 and shown in Figure 2.29. An inverter is used finally (last op-amp at the right end) as all the op-amps other than the error amplifier are used in their inverting mode. The output of the inverting op-amp is one of the two inputs to the PWM op-amp.

3.4.6 PWM Circuit

The final part of the SPICE circuit is the PWM circuit. This circuit operates as per the representation in Figure 2.23. Two op-amps are used to generate complementary outputs for the two MOSFETs.

The duty cycle equation 2.44 is referred to, for deriving the equivalence of two gains discussed in section 3.4.4.

$$duty\ cycle = u = -k \cdot e + ref \quad \textbf{3.1}$$

$$duty\ cycle = d = 0.25 - k \cdot e \quad \textbf{3.2}$$

$$V_{compare} = V_{\min} + \frac{V_{\max} - V_{\min}}{T} \cdot dT \quad \textbf{3.3}$$

$$V_{compare} = \left(V_{\max} - V_{\min}\right)\left(0.25 - k \cdot e\right) + V_{\min} \quad \textbf{3.4}$$

A PWM chip is used to implement PWM instead of the op-amp circuitry used in the SPICE circuit model for simulation. The reference periodic triangle wave of the PWM chip has a minimum value of 0.4 V and maximum value of 3.3 V with period equal to 10 microseconds (the inverse of 100 kHz switching frequency). These minimum and maximum values are substituted in equation 3.4 in addition to the *k* value of 0.24 (section 3.4.4) and voltage division factor of 5 (section 3.4.3).

In addition the quiescent duty cycle value is changed from 25 % to 50 %. The benefits of using 50 % duty cycle were discussed in section 3.3. With these changes made, the resultant equation is shown below.

$$V_{compare} = \left(3.3_{\max} - 0.4_{\min}\right)\left(0.50 - 0.24 \cdot \frac{e}{4}\right) + 0.4_{\min} \quad \textbf{3.5}$$

Simplification yields,

$$V_{compare} = (2.9)\left(0.50 - 0.24 \cdot \frac{e}{4}\right) + 0.4$$

$$V_{compare} = (1.45 + 0.4) - (2.9).(0.24) \cdot \frac{e}{4} \qquad \textbf{3.6}$$

Simplification of the coefficients of the second term in equation 3.6 results in a value of 0.175. This completes the equivalence relation between gain value of 0.175 used in section 3.2 and of 0.24 used here.

Simulations are run for the SPICE circuit model. The simulation results obtained are shown successively from Figure 3.24 to Figure 3.28. The outputs from SPICE simulation of detailed model of HAPF in Figure 3.24 are magnified individually along the time axis and shown.

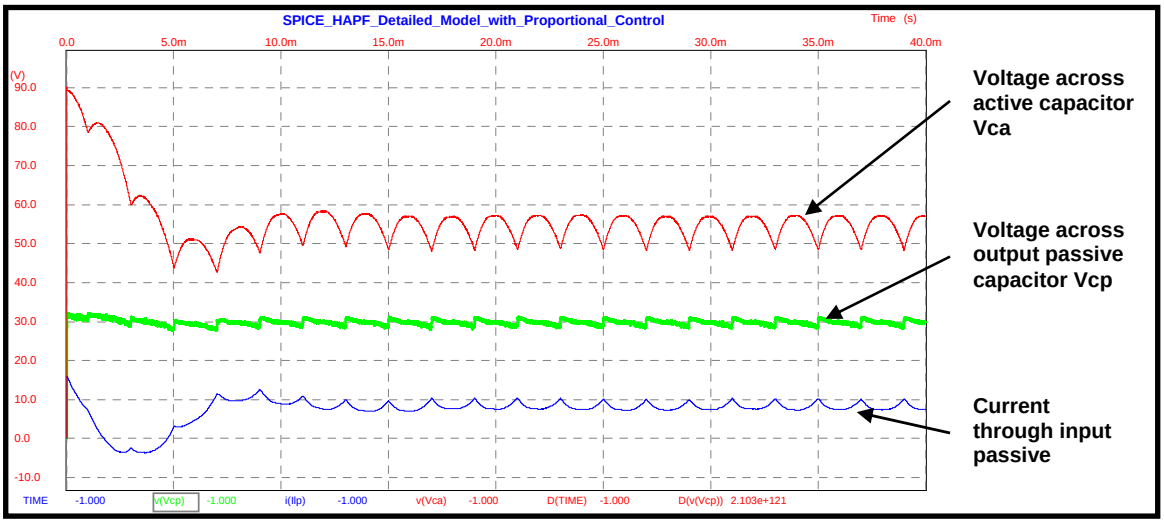


Figure 3.24 Output from SPICE Detailed Model of HAPF with Proportional Feedback Control

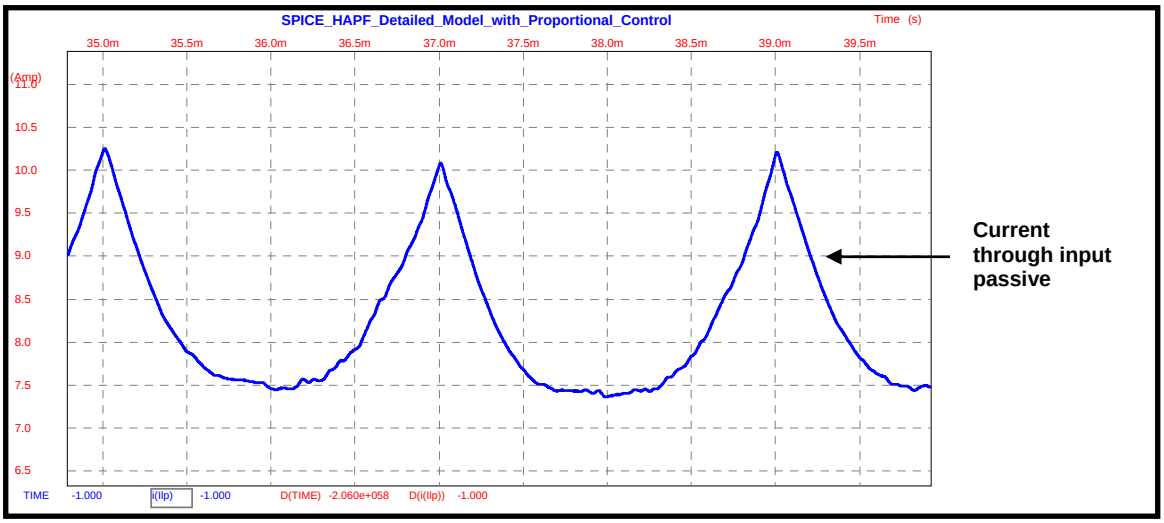


Figure 3.25 Output Ilp from SPICE Detailed Model of HAPF with Proportional Feedback Control

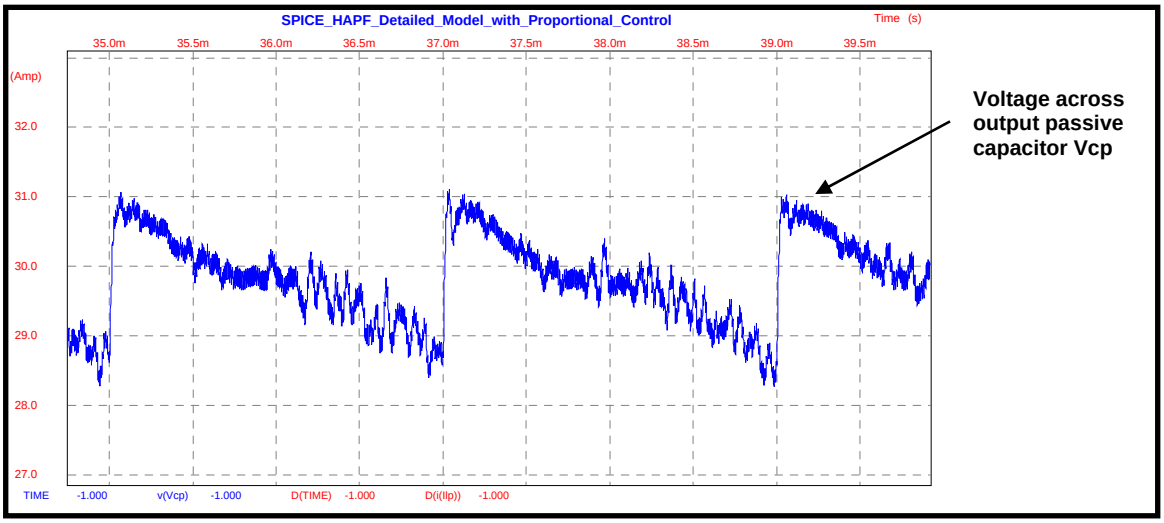


Figure 3.26 Output Vcp from SPICE Detailed Model of HAPF with Proportional Feedback Control

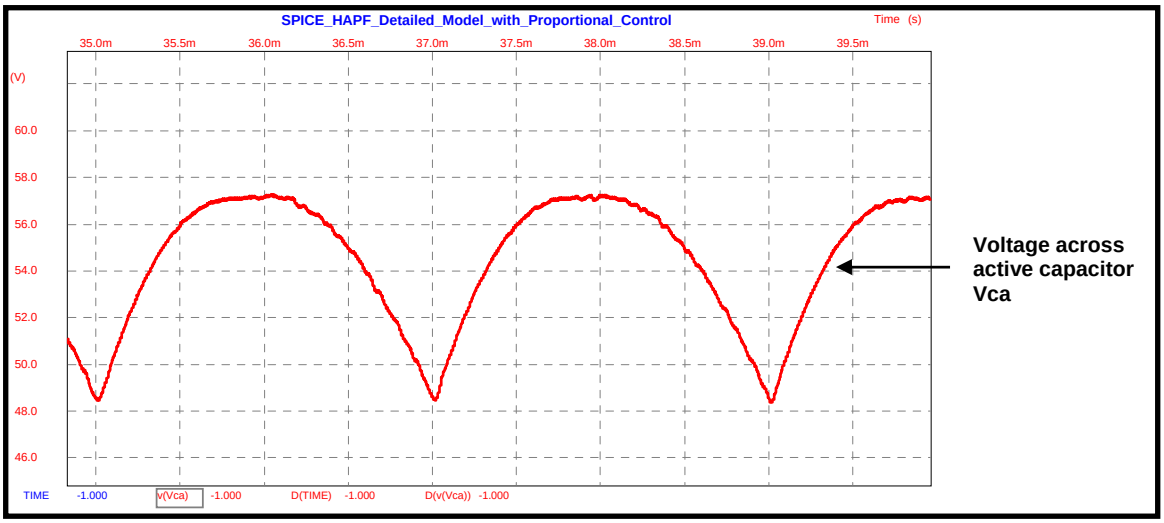


Figure 3.27 Output Vca from SPICE Detailed Model of HAPF with Proportional Feedback Control

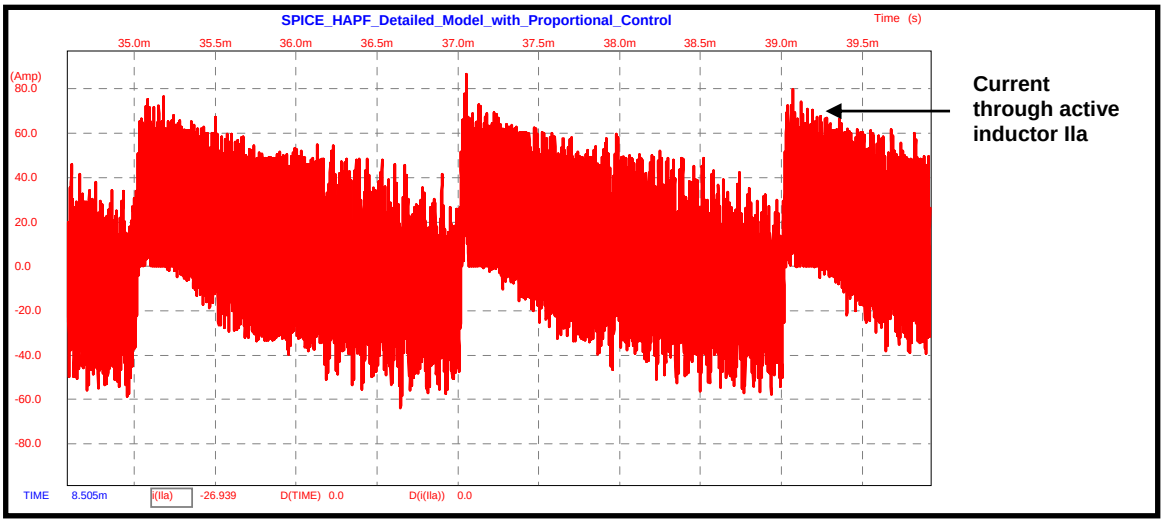


Figure 3.28 Output Ila from SPICE Detailed Model of HAPF with Proportional Feedback Control

The output parameters from this SPICE simulation are summarized in Table 3.4.

Table 3.4 Summary of SPICE Simulation of Hybrid APF with Equivalent Drive Load with Proportional Feedback Control

Proportional Feedback Control of Hybrid APF with Equivalent Drive Load	Value
Mean input passive inductor current	8.8 A
Input passive inductor ripple current	+- 1.5 A
Mean output capacitor voltage	29.75 V
Output capacitor ripple voltage	+- 1.25 V
Mean active capacitor voltage	52.85 V
Active capacitor ripple voltage	+- 4.65 V
Mean active inductor current	~ 10 A
Active inductor ripple current	+- 50 A

The results from SPICE simulation are compared to Simulink results from Table 3.3. The mean input passive inductor current value has increased by around 1.5 A from 7.3 A to 8.8 A. The corresponding ripple content has increased from +- 0.65 A to +- 1.5 A. The rise in this value is very significant. The mean output capacitor voltage has increased by 0.4 V from 29.35 V to 29.75 V. The corresponding ripple content has reduced by from +- 1.4 V to +- 1.25 V. The mean active capacitor voltage has reduced from 56.75 V to 52.85 V by around 4 V. The corresponding ripple content has increased from +- 4 V to +- 4.65 V.

Since the differences in these values are not minor when compared to the results from Simulink simulation, it is necessary to discuss the cause for this. The biggest assumption made in the Simulink model is that the switches are ideal, i.e., they have zero switching time and that they are lossless. However, this is not true in the real world. On the other hand, the SPICE model is closer to the real world model. This is because it includes the non-linear behavior of switches (non-zero switching times and switching losses). In addition op-amps used in the circuit model as gain multipliers, error amplifiers and in PWM implementation cause changes to the physical circuit which is significantly different from ideal behavior (as seen in Simulink model). It is due to this non-ideal

behavior that changes are seen in the outputs being monitored for analysis. In this simulation, the current through the active inductor is also monitored and analyzed.

In this thesis, the role of hybrid filter's active section is to generate a current equal and opposite to the harmonic load current. The current through the active inductor is also assumed to have a zero average value. From the plot shown in Figure 3.28 and summary in Table 3.4, it can be seen that this active inductor current does not have a zero average value. The mean current through the active inductor is approximately 10 A. The ripple content in this current is around +- 50 A. Due to the non-zero mean value, the losses in the circuit increase. This also causes more power to be drawn from the power supply.

The plots of current through input passive inductor from Simulink (Figure 3.17) and SPICE (Figure 3.25) simulation which is the current emanating from the DC voltage source reveal that it is not DC. The goal of this thesis was to reduce the ripple content in this current to a level such that the SRM drive which includes the hybrid active filter with smaller sized passive components, meets EMC standards (Military STD. 461). Though this current is not pure DC, the ripple is low enough that EMC standards are met (in Simulink simulation).

Since the results from SPICE and Simulink simulations for the hybrid active filter with proportional control for the same equivalent drive load are close, it can be concluded that they complement each other. To verify the simulation results obtained so far in an effective manner, the proposed filter is built in a laboratory environment and tested. The final analysis of this filter design is held back until the results from testing are obtained. Inferences will then be presented. This concludes chapter 3. The next chapter, 4, presents the experimental physical circuit, its components and their layout.

4 Hybrid Active Power Filter – Physical Setup

4.1 Introduction

This chapter deals with the physical setup of the active power filter with proportional feedback control. The physical model which will be implemented is presented followed by the components being used in it. These include the ICs for performing pulse width modulation (PWM), gate driving, pulse generation, gain multiplication and amplifiers. Following this the passive components such as inductances and capacitances are discussed as well as some useful circuit building tips.

4.2 ICs

4.2.1 Pulse Width Modulation IC – UC2526AN

The UC2526AN is part of Unitrode (now owned by TI) UC1526A Series' PWM circuits. High frequency operation up to 600 KHz is possible with this series and is chosen as the duty cycle and switching frequency used in this design fall within its range of operation. The duty cycle range for this IC is between 0 % and 49 % which is best for this design which utilizes effective final duty cycle of around 0.5. Extra connections are made to this IC to ensure that the necessary duty cycle for operation is obtained. This is explained later. The external connections made to this IC for operation are shown below in Figure 4.1. The internal block diagram of the IC is shown in Figure 4.2. The compensated error which is the output of the right most op-amp from SPICE detailed model of hybrid APF with proportional feedback (in section 3.4) is fed into pin 1. The error amplifier section of the PWM chip (amplifier connected to pins 1 and 2) is used as a voltage follower as the error voltage and compensated error were determined using external op-amps (section 3.4). The resistor and capacitor connected to pins 9 and 10 respectively form the components of the PWM chip's oscillator section and for generating the switching frequency of 100 KHz in this design. The corresponding period is 0 microseconds which is used to select the components' size from the chart shown in Figure 4.3.

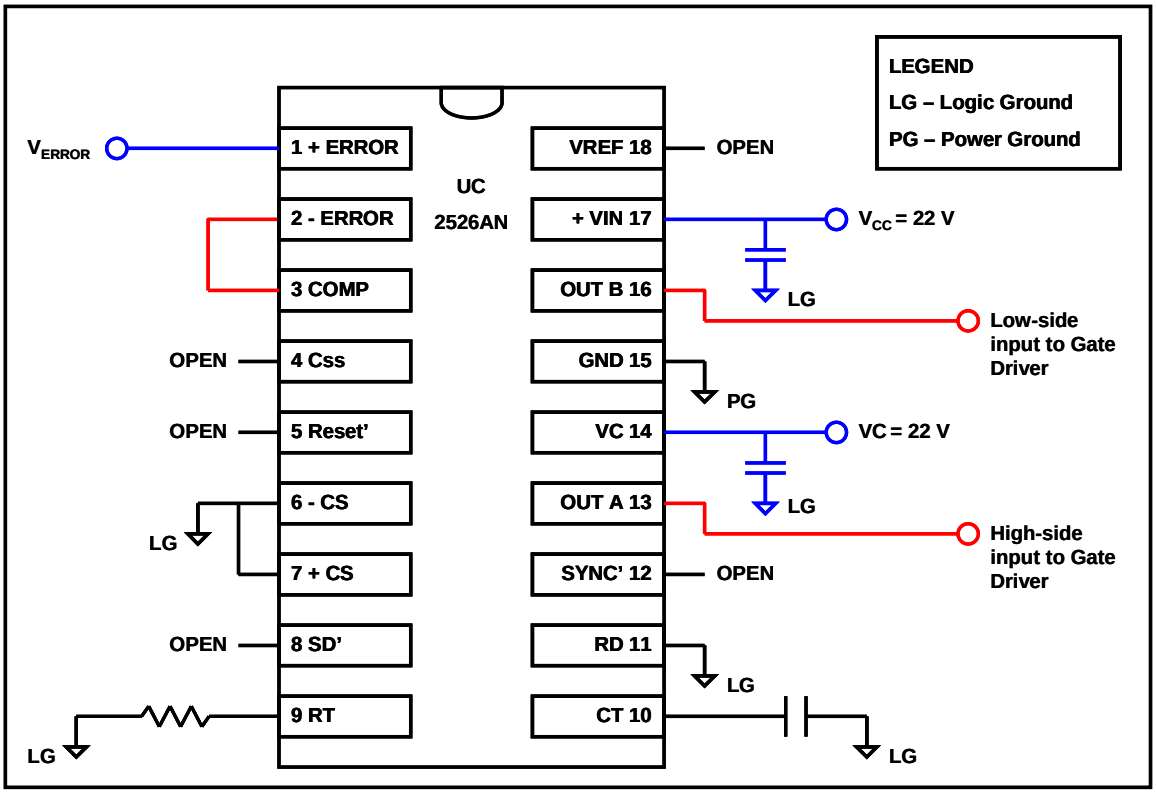


Figure 4.1 External Connections for PWM IC

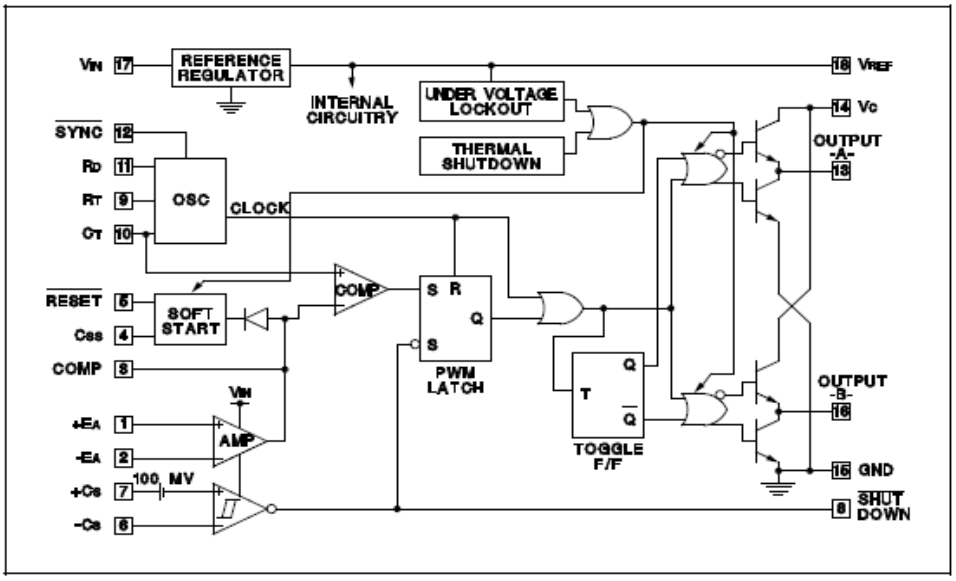


Figure 4.2 Internal Block Diagram of UC2526AN (Source, Reference [33])

The pins connected to voltage sources (pins 14 and 17) are shorted to ground using 2.2 uF capacitances to ensure that pure DC is available. The outputs from pins 16 and 13 form the input to the gate driver IC which is discussed in the next section.

Based on the connections in Figure 4.1, the circuit was tested with an arbitrary input error voltage. Firstly, the voltage across pin 10 was observed. This being the output of the oscillator section, a triangular waveform was expected. The output from this pin is shown in Figure 4.4. The triangle wave output is obtained as designed. An external voltage greater than 3.3 V is fed into pin 1 as a check. Since the input voltage is greater than the maximum voltage of the triangle wave oscillator output, a 100 % duty cycle is expected.

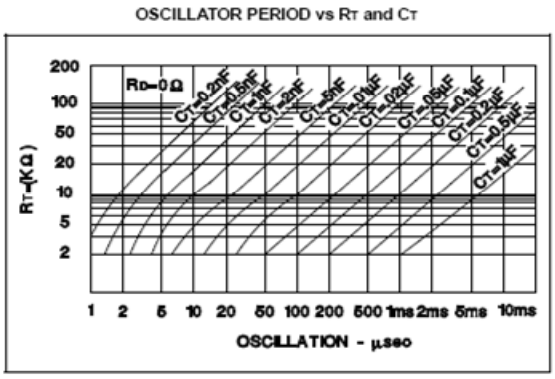


Figure 4.3 Oscillator Section Selection Chart (Source, Reference [33])

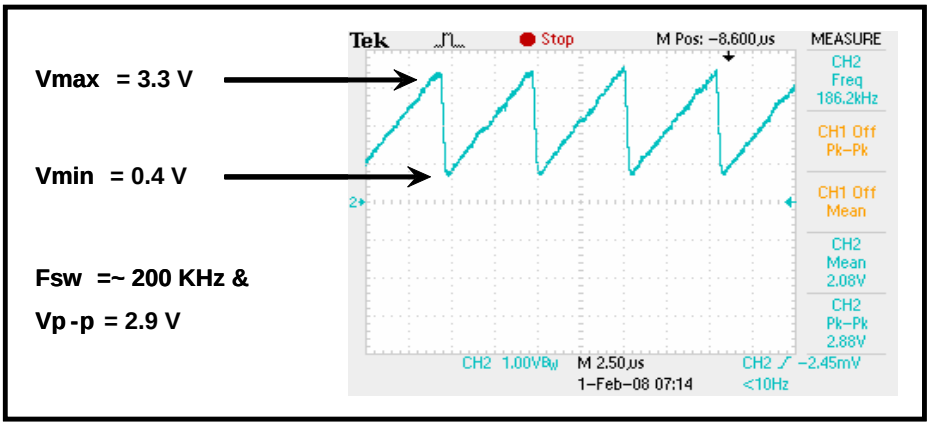


Figure 4.4 Oscillator Section Output

However, it is not so. The complementary pulses generated at pins 13 and 16 are shown in Figure 4.5. It should be noted that the frequency of these pulses (encircled, approximately 97 KHz) is half of frequency seen in Figure 4.4 (approximately 187 KHz) equating to a duty cycle of around 50 %. This halving of frequency is inherent to this IC which is evident from the maximum duty cycle operation specification (49 %). In case the error voltage is within the range of the triangle wave (between 0.4 V and 3.3 V), the final duty cycle seen would be half of what is needed for this design.

This leads to incorporation of additional circuitry to ensure that the MOSFETs of the hybrid active filter see a duty cycle as per the design rather than half of it. This is done using a logical AND gate. The two complementary outputs (original PWM IC's output) are combined to form one train of pulses (equal to the desired frequency of operation). A logical NOT gate is then used to invert this first train of pulses to form the second train of pulses. Signal MOSFETs are used to implement logical AND and logical NOT operations. Additional external circuit connections are made to the circuit shown in Figure 4.1. These are shown in Figure 4.6. The output obtained from the PWM IC with the extra connections made is shown in Figure 4.7.

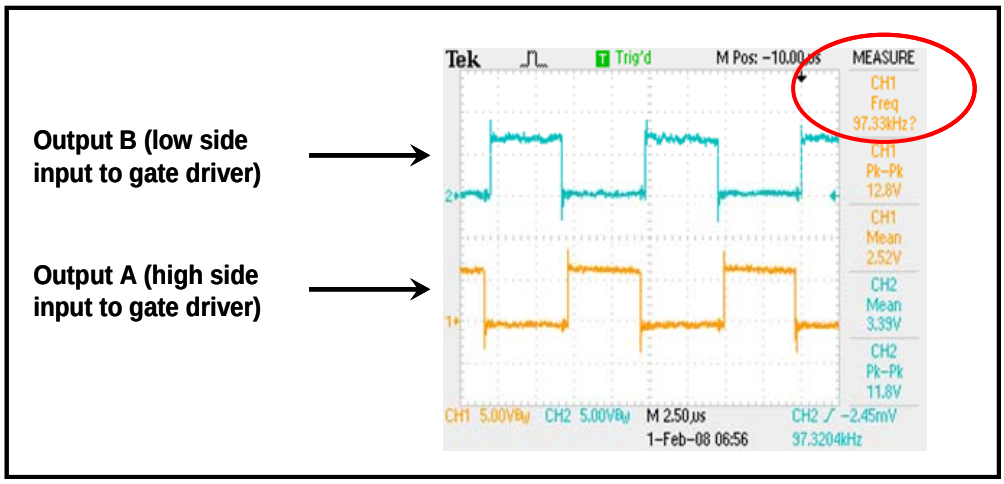


Figure 4.5 PWM IC Complementary Output Pulses

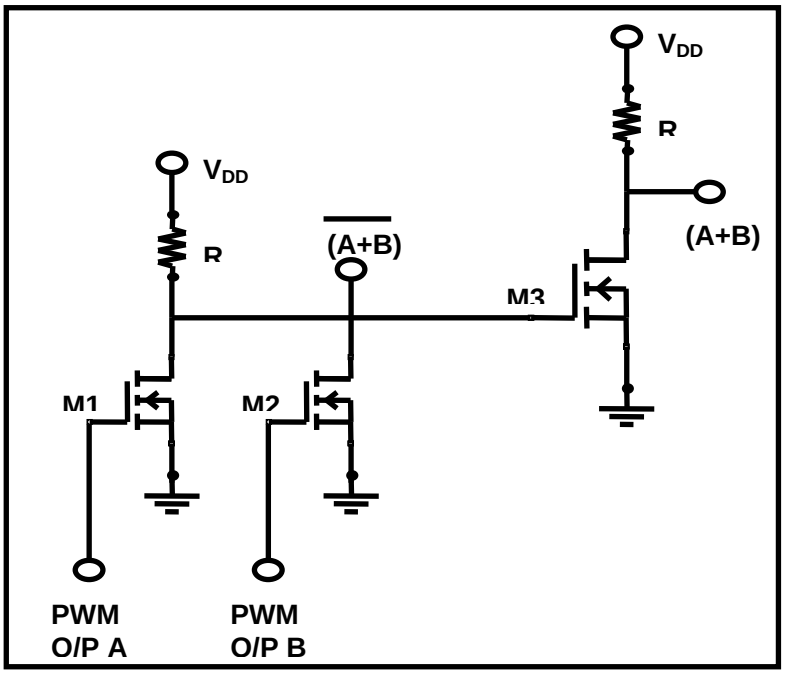


Figure 4.6 Extra Connections to PWM IC

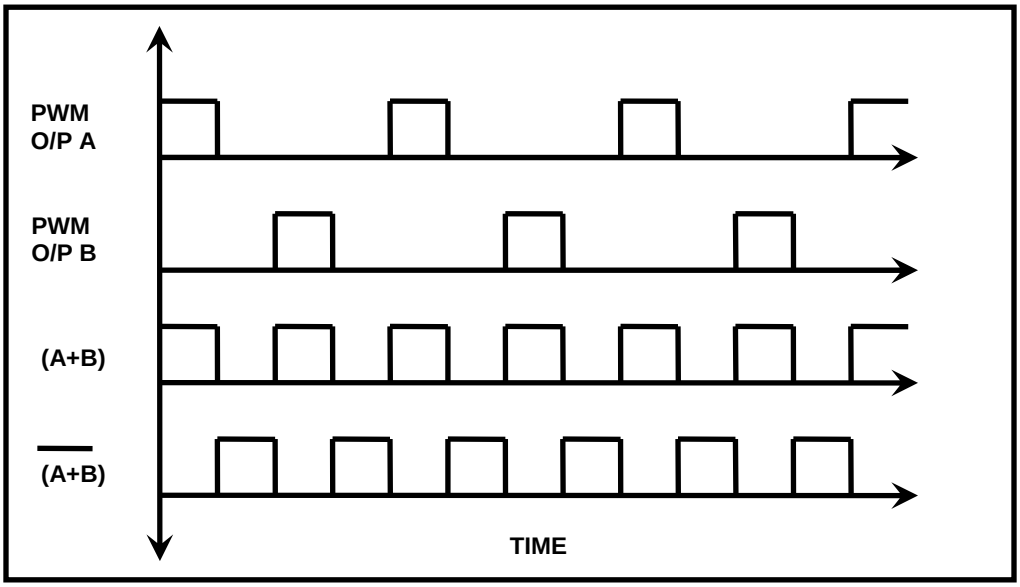


Figure 4.7 Output with Extra Connections to PWM IC

These two new complementary trains of pulses form the final input to the gate driver IC which is discussed in the following section. It should be noted that the peak to peak voltage of these pulses is around 12 V which is greater than the threshold voltage of the

power MOSFETs used (around 3 V) in this implementation. Since the output gate pulses from the gate driver IC are greater than this threshold voltage, turn ON of power MOSFETs is certain. More information (parameter specifications) regarding this gate driver IC can be found in Reference [34].

4.2.2 Gate Driver IC – IR2110

The IR2110 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels [34]. It has a high side maximum voltage of 600 V, much higher than the voltage considered in this design (Vca of around 105 V as per our simulation results). The external connections made to this IC for operation are shown in Figure 4.6.

This IC is needed for shifting the gate to source voltage to a level greater than 0 V. This is necessary as the high side MOSFET's source is not at ground potential. External connections shown are made using an application note [35].

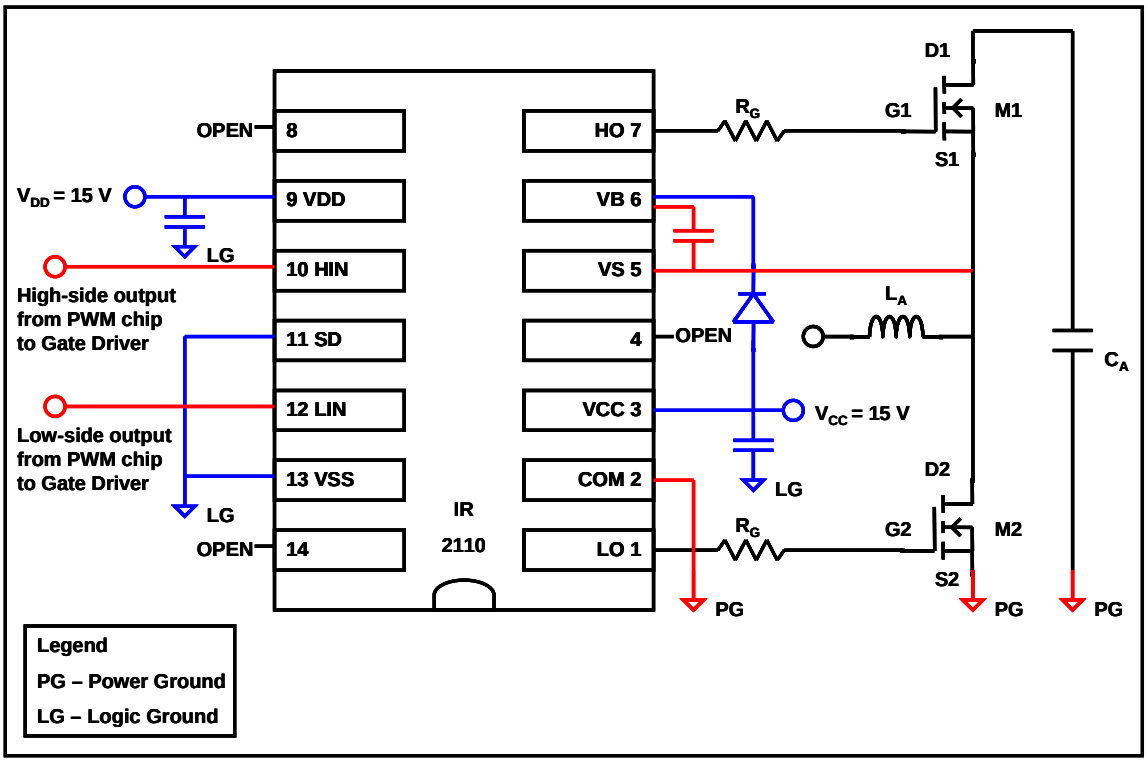


Figure 4.8 External Connections to Gate Drive IC for HAPF

The capacitors are chosen to ensure that only DC voltage is seen at pins 9 and 3. Resistors are connected from the output pins 1 and 7 to the low and high side MOSFETs' gates. This is done to limit the current entering the gate. In addition they help in controlling the switching period of the MOSFETs. This is imperative as fast changes in current could lead to generation of voltages across stray inductances which are unavoidable due to common use of wired connections. Voltage VDD determines the input pulse voltage level. This must be greater than the peak to peak voltage of the pulse output from the PWM IC.

Figure 4.8 shows external connections made to the gate driver IC which drives the MOSFETs of the active section of the HAPF. The equivalent drive load circuit also requires a gate driver IC. However, the topology of the active section and the equivalent drive load are not the same. The latter is an H-Bridge topology. The external connections made to the gate driver IC of the equivalent drive load circuit are shown in Figure 4.9. The output from the gate driver IC with the external connections is shown in Figure 4.10.

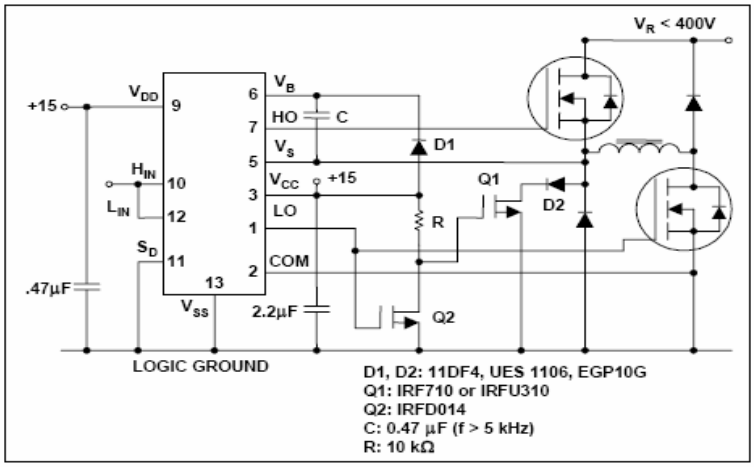


Figure 4.9 External Connections to Gate Drive IC for Equivalent Drive Load (Source, Reference [35])

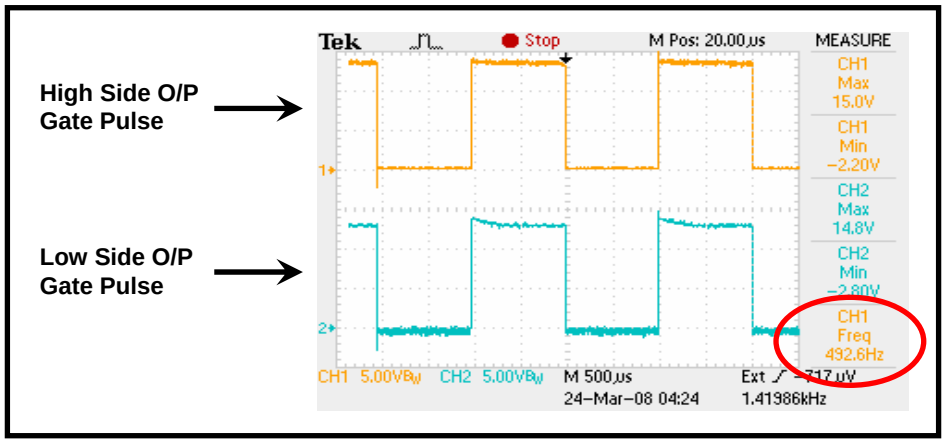


Figure 4.10 Gate Driver IC Output for Equivalent Drive Load Circuit

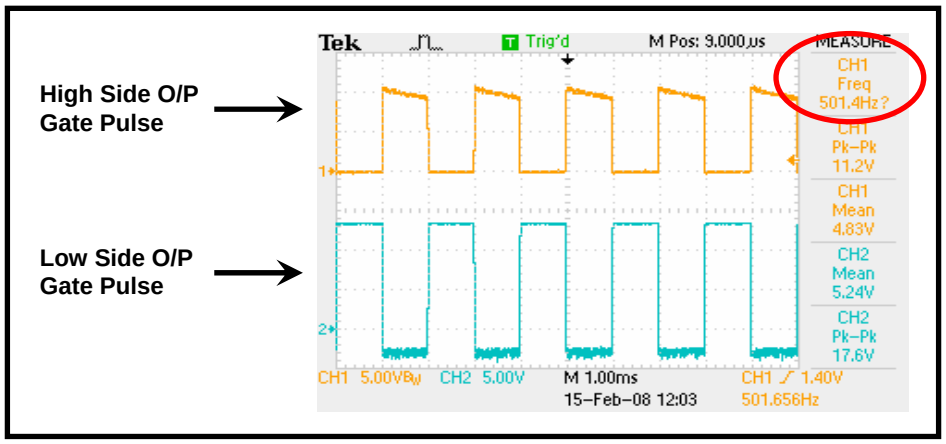


Figure 4.11 Gate Driver IC Output for Active Section of HAPF

It can be seen that the frequency of the above pulses (encircled) is around 500 Hz. Also, the above sets of pulses are in sync with each other as per the design of the equivalent drive load circuit discussed in section 3.1.

However, the gates of the MOSFETs (of the active section of the HAPF) need to be driven such that only one MOSFET is turned ON at any instant of time. With input pulses to the gate driver IC at 500 Hz, the output gate pulses obtained for the active section of HAPF are as shown in Figure 4.11.

It should be noted that the MOSFETs of the active section of the HAPF need to be driven at 100 kHz rather than 500 Hz. The lower two trains of pulses from Figure 4.7 form the input to the gate driver IC for the MOSFETs of the active section of the HAPF.

4.2.3 Operational Amplifier IC as Gain Multiplier/Summer/Inverter – LM741CN

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations. The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C [36].

The LM741CN operational amplifier is used in implementing the physical filter circuit shown in Figure 3.21.

4.2.4 Inductors of HAPF

Two inductors are part of the HAPF in this thesis. The larger passive inductor is of 160 uH and the smaller active inductor is of 1.6 uH. These two inductors were previously designed by [2]. They are used '*as is*' in this thesis' physical implementation.

4.2.5 Capacitors of HAPF

In section 1.3 the use of fluorinated polyethylene (FPE) plastic film capacitors was proposed. However, being in development, these capacitors are expensive. Therefore polypropylene plastic film capacitors, being electrically similar to FPE plastic film capacitors (their maximum operating temperature is much lower at about 105°C) and less expensive are used. Capacitors of the active filter are designed for a 270V DC voltage rating to eliminate experimental safety issues. It should be noted that this voltage level is under consideration as a new standard for automotive DC voltage to replace the present

42V DC. The circuit parameters used for the design issues and challenges of control schemes do not depend on this input voltage and thus the results obtained can be generalized to systems that have similar current levels.

The two capacitors used in this implementation as shown in Figure 3.21 are the output capacitor of 400 uF and the active capacitor is of 800 uF. An already available 400 uF capacitor was used as the output capacitor. Four 200 uF capacitors were connected in parallel to create the 800 uF active capacitor. A DC bus was used for connecting these 200 uF in parallel by [2] which is discussed next. In should be noted that these capacitors are capable of handling up to 600 V.

4.2.6 DC Bus

A DC bus was used by [2] instead of copper wire as a current carrying medium for connecting the active capacitor as the magnitude of current flowing through it was high. SPICE simulation results show the maximum instantaneous active inductor current being around 65 A. This is the current flowing through the active capacitor when the upper MOSFET M1 is turned ON. Again, the same DC bus used earlier in [2] is used in this thesis. Reference [2] provides detailed design of the DC bus.

4.2.7 Circuit Layout

The experimental layout of the HAPF being developed in this thesis is shown in Figure 4.12. Though this layout of the circuit is very similar to the SPICE circuit layout in Figure 3.21, the focus here is on optimizing the placement of individual components. Also, the control circuit which is implemented on bread boards is excluded in this discussion. Figure 3.24 Two areas of the circuit layout are shaded. The first shaded area includes the active section of the HAPF with MOSFETs switching at 100 kHz. The second shaded area with dotted lines includes the equivalent load drive circuit with MOSFETs switching at 500 Hz. It should be noted that these two areas are connected across the output capacitor Cp. Connecting wires to these two areas essentially behave as inductors of very low inductance. During turn ON and turn OFF of the MOSFETs very high currents flow through the connecting wires.

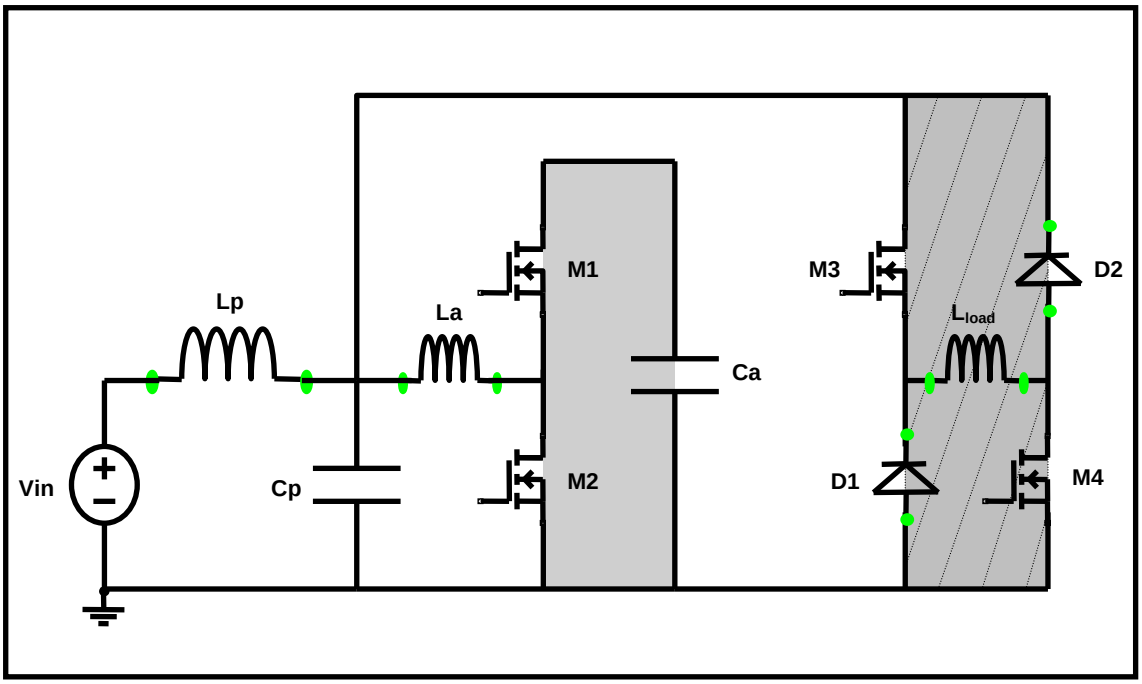


Figure 4.12 Experimental Circuit Layout

Therefore it is essential to minimize the length of connecting wires in these two areas to ensure that effects of stray inductor based voltages are minimal. Twisted wires are employed for connection as they also help in reducing effects of stray inductance.

4.2.8 Heatsink Design

The MOSFETs of the active section of the HAPF operate at a high switching frequency of 100 kHz. This leads to generation of heat. Natural air cooling of these MOSFETs is not sufficient. Therefore heatsinks are necessary for dissipation of the heat generated. Heatsinks are made of aluminum based alloys and have a wide surface area. The MOSFETs used here have four terminals, with the fourth terminal being the second drain terminal. The first drain terminal of the MOSFET extends to the rear of the MOSFET and becomes the fourth terminal and is the surface in contact with the heatsink when the MOSFET is screwed on to it. Since both the surfaces in contact here are metallic, an insulator is necessary. It is essential that the contact between the MOSFET and the heatsink with an insulator is effective in transferring heat. The heatsink surface may have minor indentations and this may not create a smooth contact. Therefore a heatsink

compound is applied to the surface of the heatsink on which the insulator is placed and MOSFET screwed upon. However, care must be taken to ensure that only a thin layer of heatsink compound exists. Else, the heat dissipation will not be effective. A total of six are used with two for the MOSFETs of the HAPF and four for the two MOSFETs and two diodes of the equivalent drive load circuit.

4.2.9 Bill of Materials

In this thesis, the components used for implementation are summarized in Table 4.1.

Table 4.1 Bill of Materials

Item	Part Number	Description	Quantity
1	IR2110	Gate Driver IC	2
2	UC2526AN	PWM IC	1
3	LM741CN	Operational Amplifier	5
4	IRFP90N20	Power MOSFET for HAPF	2
5	IRF3710	Power MOSFET for Equivalent Drive Load Circuit	2
6	30ETH06	Diodes for Equivalent Drive Load Circuit	2
7	IN4148	Diodes for Gate Driver IC Circuit	2
8	HFA15TB60	Diode for Gate Driver IC Circuit	1
9	IRF740	MOSFET for Gate Driver IC Circuit	1
10	IRF510	MOSFET for Gate Driver IC Circuit	1
11	-	200 uF Capacitor	4
12	-	400 uF Capacitor	1
13	-	160 uH Inductor	1
14	-	1.6 uH Inductor	1
15	-	Resistors (various values)	18
16	-	Ceramic Capacitors (various values)	10
17	-	DC Bus	1
18	-	Phase Bus	1
19	-	Heatsink	6

20	-	Signal Generator	1
21	-	DC Power Supply	4
22	Tektronix	Current Sensor	1
23	Tektronix	Oscilloscope	1

This concludes chapter 4. The following chapter discusses the results from the experimental HAPF circuit which are analyzed and compared to the simulation results from chapter 3.

5 Active Power Filter – Test Results

5.1 Introduction

The physical hybrid active power filter implemented in this thesis is shown in Figure 5.1.

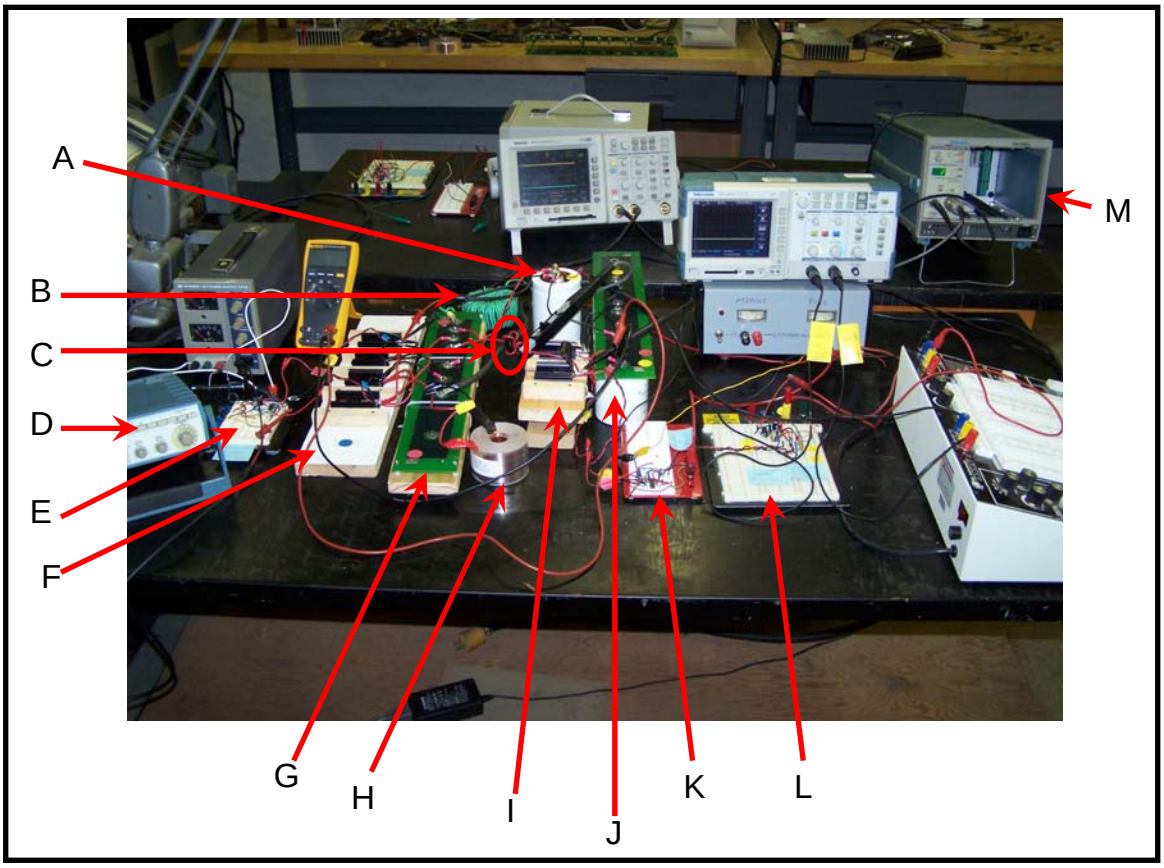


Figure 5.1 Snapshot of Filter Physical Implementation

Table 5.1 Legend for Filter Physical Implementation Snapshot

Part of Filter	Description
A	Passive Capacitor (Cp)
B	Passive Inductor (Lp)
C	Active Inductor (La)

D	Signal Generator
E	Gate Driver for Equivalent Non-Linear Load
F	Equivalent Non-Linear Load
G	Phase Bus
H	Load Inductor (Lload)
I	Active Section of HAPF
J	Active Capacitor (Ca)
K	Gate Driver for Active Section
L	Pulse Width Modulation Section
M	Current Probe Module

5.2 Test Results

In chapter 3, the hybrid active power filter shown in Figure 5.1 was simulated in Simulink and then SPICE environments at 30 V DC input voltage. This voltage was chosen due to the benefit it offered in terms of ease of testing in a laboratory environment. However, while testing the filter, it was seen that there were switching frequency dependent spikes in the gate pulses fed to the MOSFETs of the active section. The magnitude of these spikes especially at the turn ON and turn OFF instants, increase when the input voltage to the filter increases. To counter these spikes, the gate resistor value was increased. This was done to increase the turn ON time and to smoothen the turn ON transient. In addition, electrolytic capacitors used in the gate driver section were replaced with ceramic capacitors. Aluminum electrolyte (barrel shaped) capacitors tend to have considerably higher equivalent series resistance and inductance. Also, the connecting leads from the active and passive capacitors were reduced. This was to reduce the area of the shaded regions shown in Figure 4.12. These spikes could potentially go higher than the rated voltage of the MOSFETs used in the active section which is 200 V.

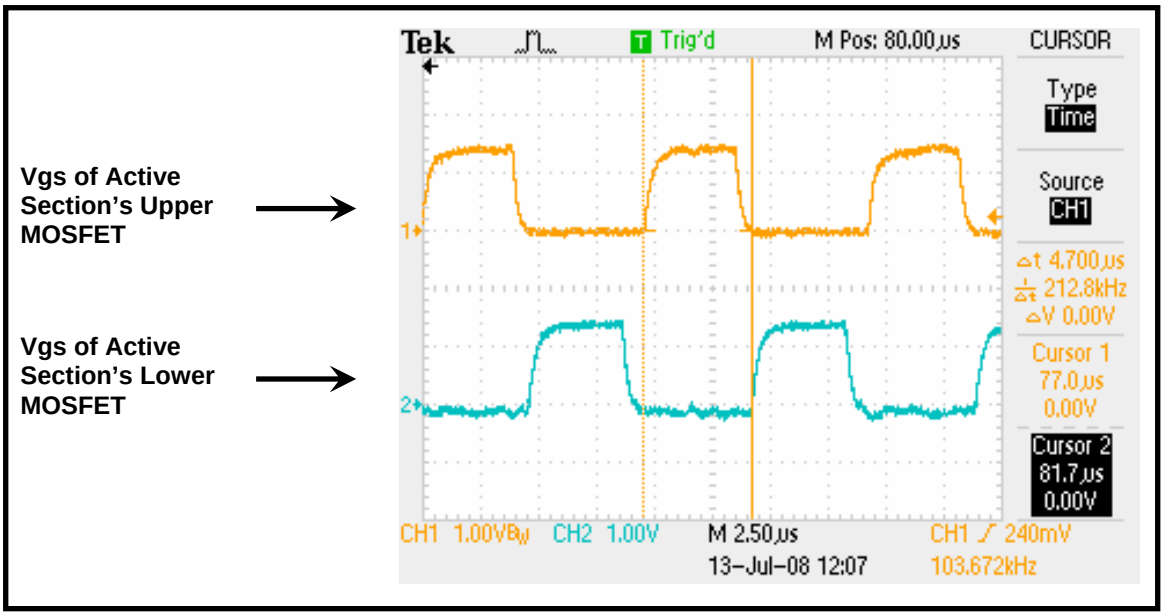


Figure 5.2 Gate Pulses to MOSFETs of Active Section at 0 V Input Voltage, Ch 1 (Upper plot) & Ch 2 (Lower plot), 1 V/Div, 10 x multiplier

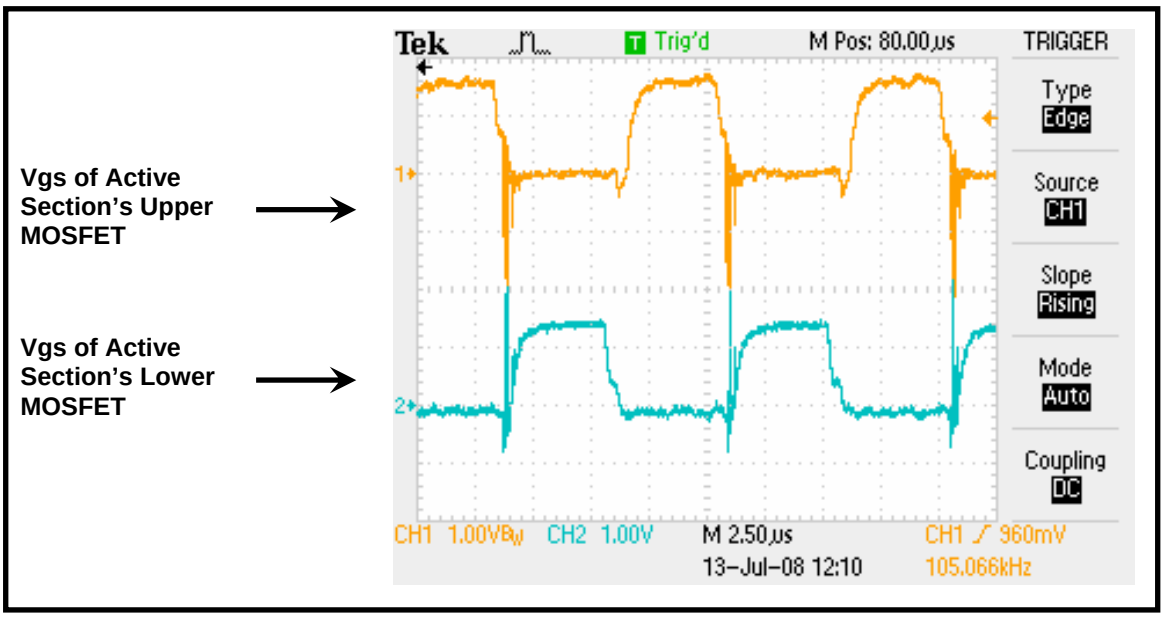


Figure 5.3 Gate Pulses to MOSFETs of Active Section at 20 V Input Voltage, Ch 1 (Upper plot) & Ch 2 (Lower plot), 1 V/Div, 10 x multiplier

If such a spike occurred, there could be a "shoot through" effect damaging the MOSFETs. The gate pulses to the MOSFETs of the active section at two different input

voltages are shown in Figure 5.2 and Figure 5.3. Therefore, the physical filter circuit was tested at 20 V DC only. This was done for constant duty cycle operation and for proportional feedback duty cycle operation.

In chapter 3, the equivalent non-linear drive was designed to operate at a switching frequency of 500 Hz and a duty cycle was 50 %. With these settings, the active power filter system was tested. The harmonic current generated by this load circuit when tested as a stand alone unit at 30 V input voltage is shown in Figure 5.4.

The harmonic current has a low value of around -35 A and a high of around +32 A. The low value is greater than high value due to a small spike. However, the plot shows that the current magnitude and ripple content are high. Therefore, it is desirable to reduce the current. It should be noted that the equivalent drive load is driven by a gate driver whose input gate pulses are fed from a signal generator. To reduce the current, the duty cycle was reduced to around 25 % and the signal offset was changed. Then the entire filter setup was tested. The load current after these changes is as shown in Figure 5.5.

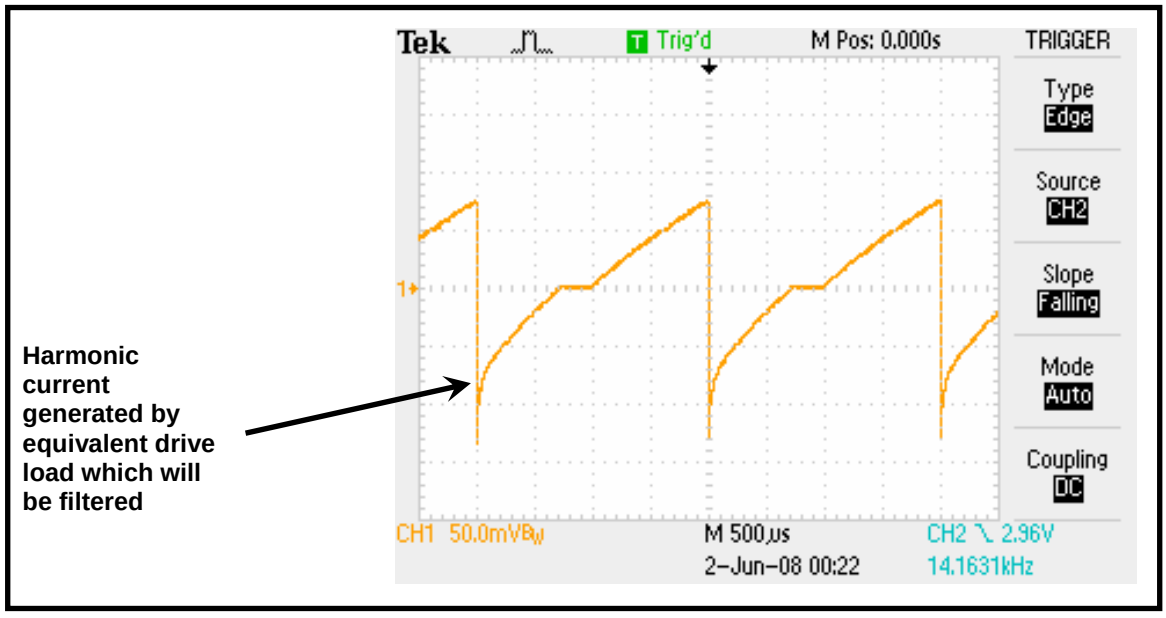


Figure 5.4 Equivalent Non-Linear Drive Load Circuit Results at 30 V Input Voltage, Ch 1 at 50 mV/Div & 5 A scale

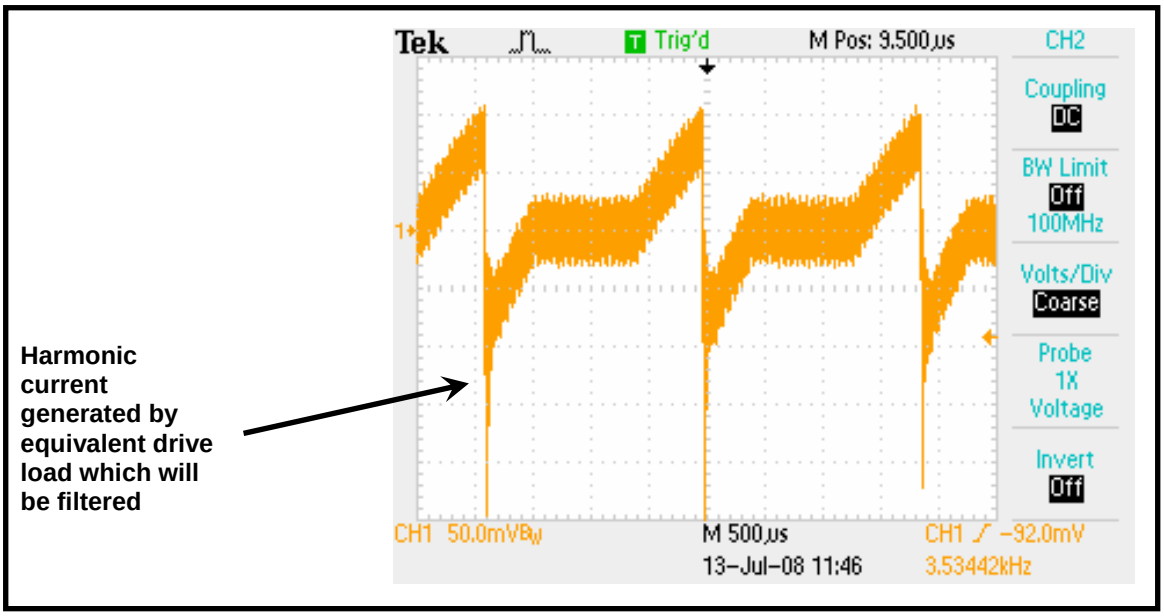


Figure 5.5 Equivalent Non-Linear Drive Load Circuit Results at 20 V Input Voltage, Ch 1 at 50 mV/Div & 2 A scale

The above harmonic current plot when compared to one from Figure 5.4 shows the effect of active section's MOSFETs switching at 100 kHz. The adjustment made to the duty cycle and signal offset can be seen here. The duration of the current around the zero point has increased. This reduces the current as was desired.

5.2.1 Test Results from Constant Duty Cycle Operation of HAPF Circuit

The physical HAPF circuit as shown in Figure 5.1 is run at 20 V input voltage. The test results are shown below starting with Figure 5.6. This figure shows the voltage across the output passive capacitor, Vcp and the active capacitor, Vca at low frequency. Figure 5.7 shows the same voltages at high frequency. It should be noted that there are two main frequencies of interest in all the test results' plots, the first being the low frequency corresponding to the load circuit switching frequency of 500 Hz and the second being the high frequency corresponding to the active section's switching frequency of 100 kHz.

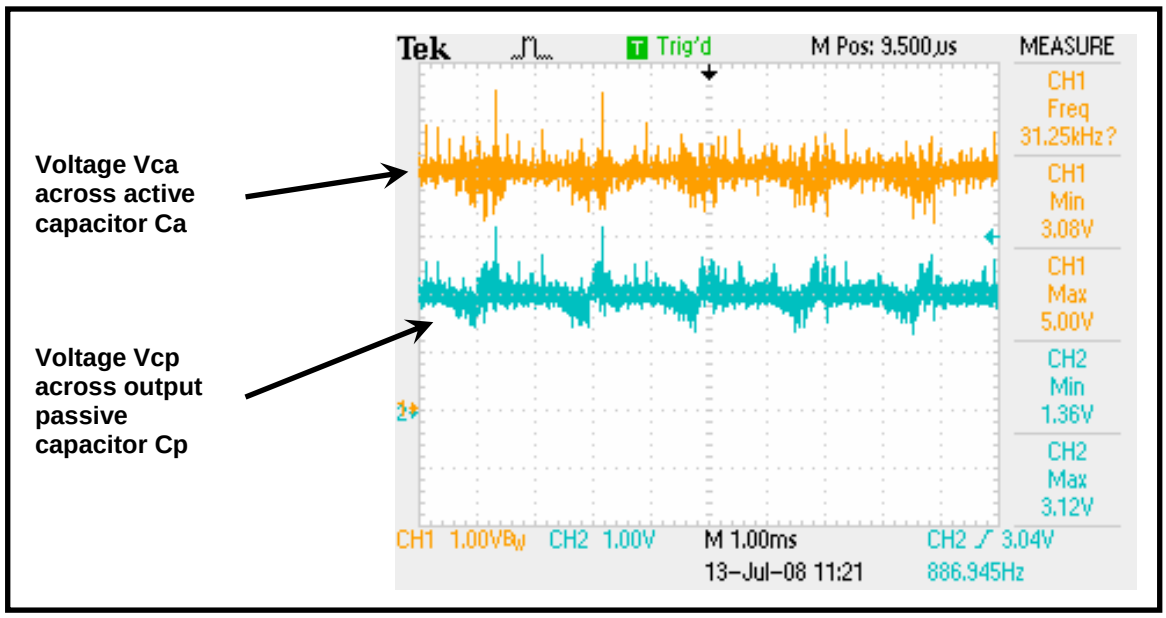


Figure 5.6 Low Frequency Passive Capacitor Voltage Vcp (Lower plot) and Active Capacitor Voltage Vca (Upper plot) at 20 V Input Voltage, Ch 1 & Ch 2 at 1 V/Div & 10 x multiplier

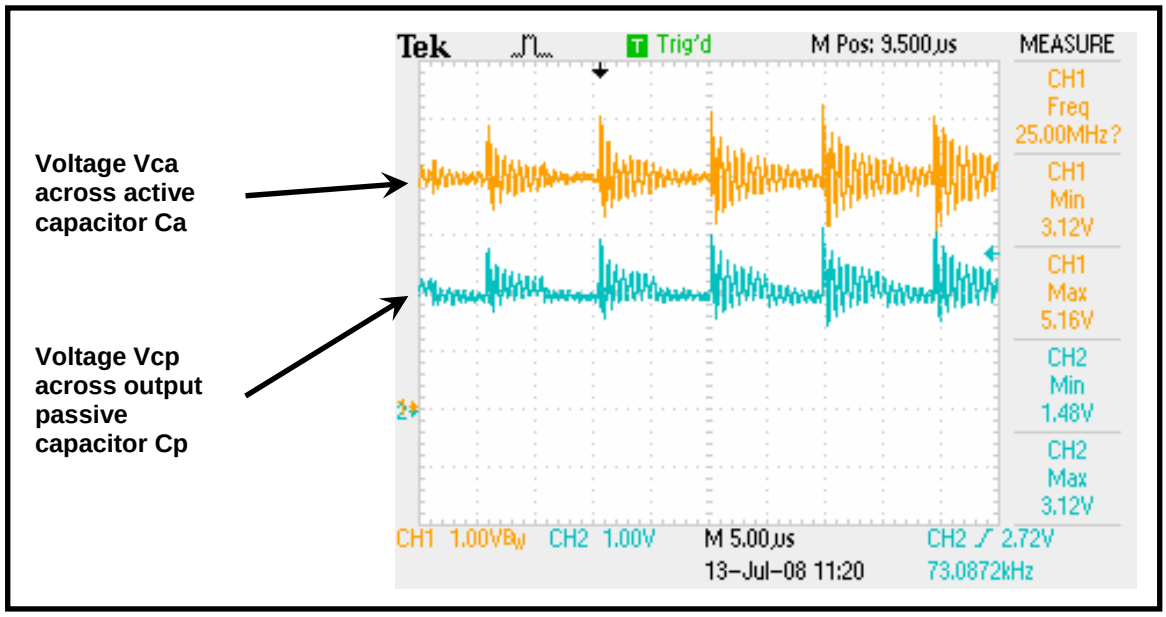


Figure 5.7 High Frequency Passive Capacitor Voltage Vcp (Lower plot) and Active Capacitor Voltage Vca (Upper plot) at 20 V Input Voltage, Ch 1 & Ch 2 at 1 V/Div & 10 x multiplier

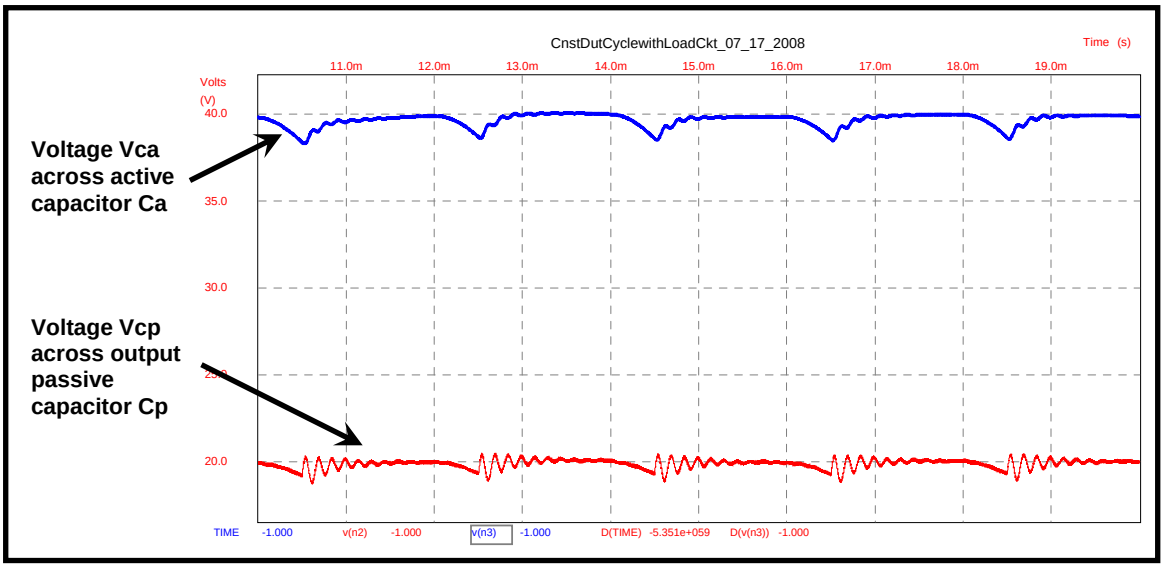


Figure 5.8 Low Frequency Passive Capacitor Voltage Vcp (Lower plot) and Active Capacitor Voltage Vca (Upper plot) at 20 V Input Voltage from SPICE simulation

From the test circuit plots it can be seen that the mean value of passive capacitor voltage is 20 V and active capacitor voltage is 40 V. The ripple in the passive capacitor voltage is around +- 8 V. The ripple in the active capacitor voltage is around +- 10 V. The earlier SPICE model is modified such that the input voltage is 20 V and simulated. The passive capacitor voltage and active capacitor voltage is shown in Figure 5.8.

On comparison with the plot in Figure 5.6 it can be seen that the mean values from SPICE simulation match the test results' values. However, the noise seen in the test circuit is not present here.

The current through the input passive inductor from the test circuit is shown in Figure 5.9 and from SPICE simulation in Figure 5.10.

The input passive inductor current from the test circuit has a mean value of 1.4 A with a ripple of +- 0.4 A. SPICE simulation shows that the mean value is 4.5 A with a ripple of +- 0.6 A. It should be noted that the mean value does not match due to the changes made in the physical test circuit to reduce the magnitude of current.

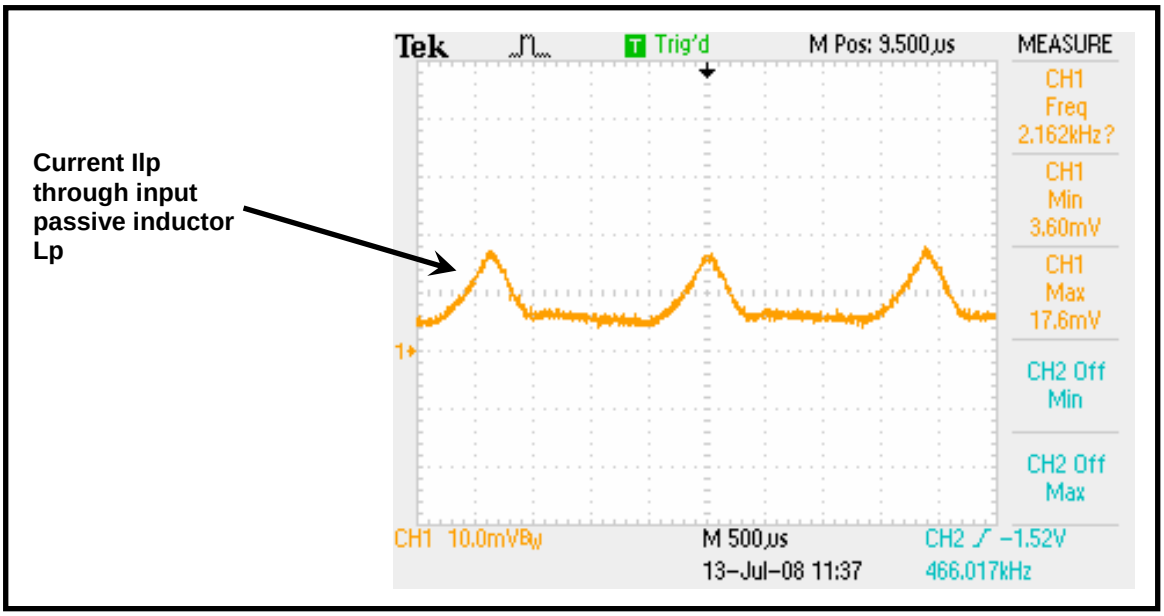


Figure 5.9 Low Frequency Input Passive Inductor Current at 20 V Input Voltage, Ch 1 at 10 mV/Div & 2 A scale

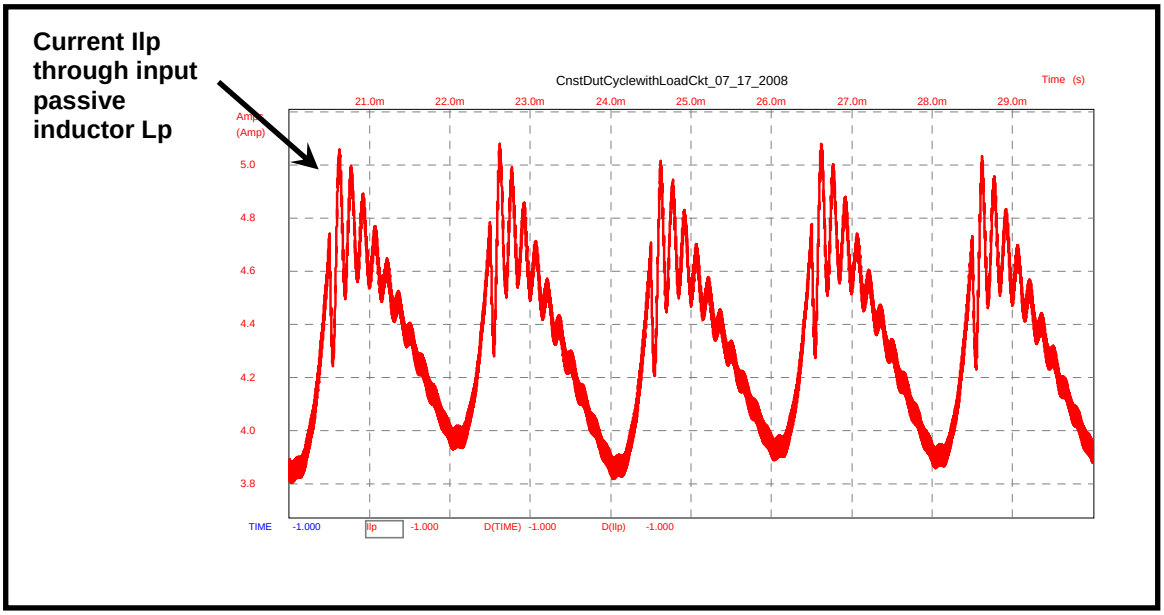


Figure 5.10 Low Frequency Input Passive Inductor Current at 20 V Input Voltage from SPICE simulation

The current through the active inductor and voltage across it are shown in Figure 5.11.

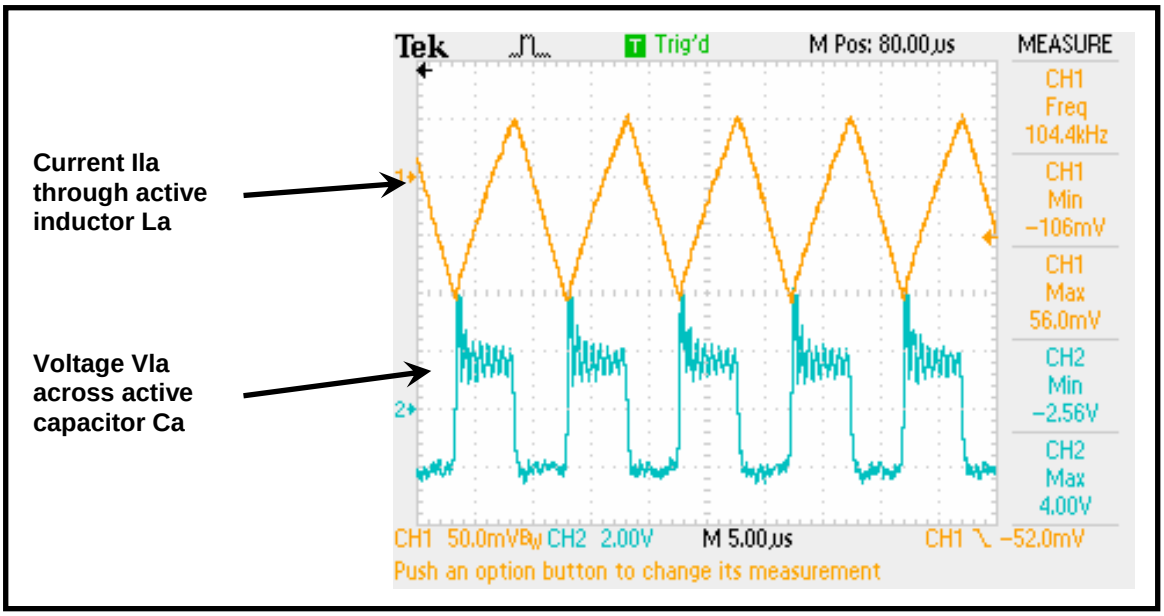


Figure 5.11 High Frequency Active Inductor Current (Upper plot) and Voltage (Lower plot) at 20 V Input Voltage, Ch 1 at 50 mV/Div & 2 A scale, Ch 2 at 2 V/Div & 10 x multiplier

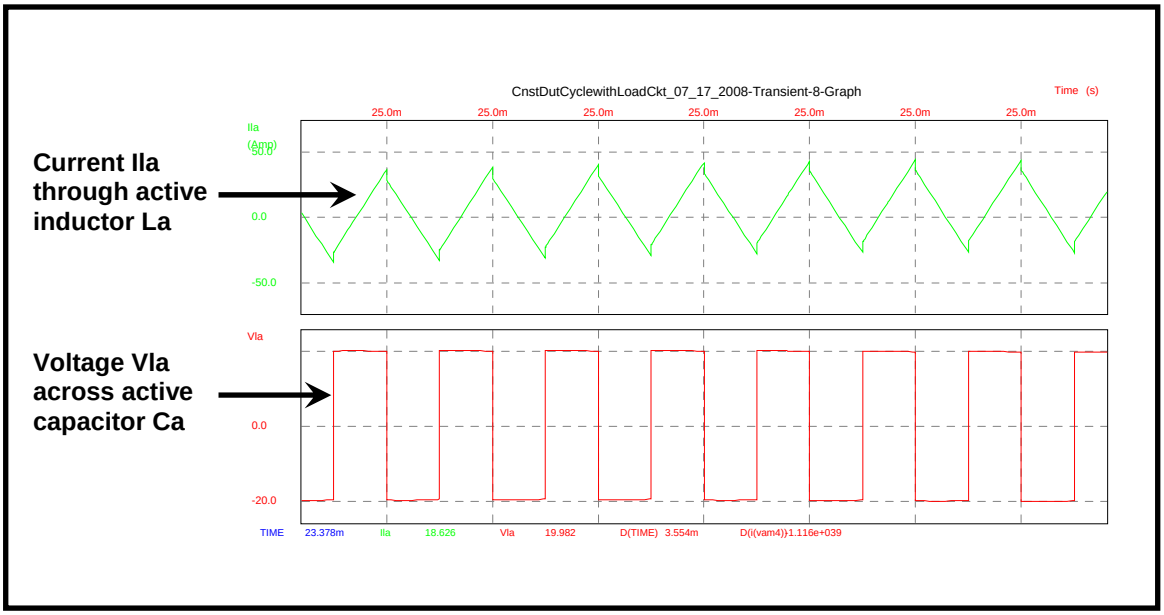


Figure 5.12 High Frequency Active Inductor Current (Upper plot) and Voltage (Lower plot) at 20 V Input Voltage from SPICE simulation

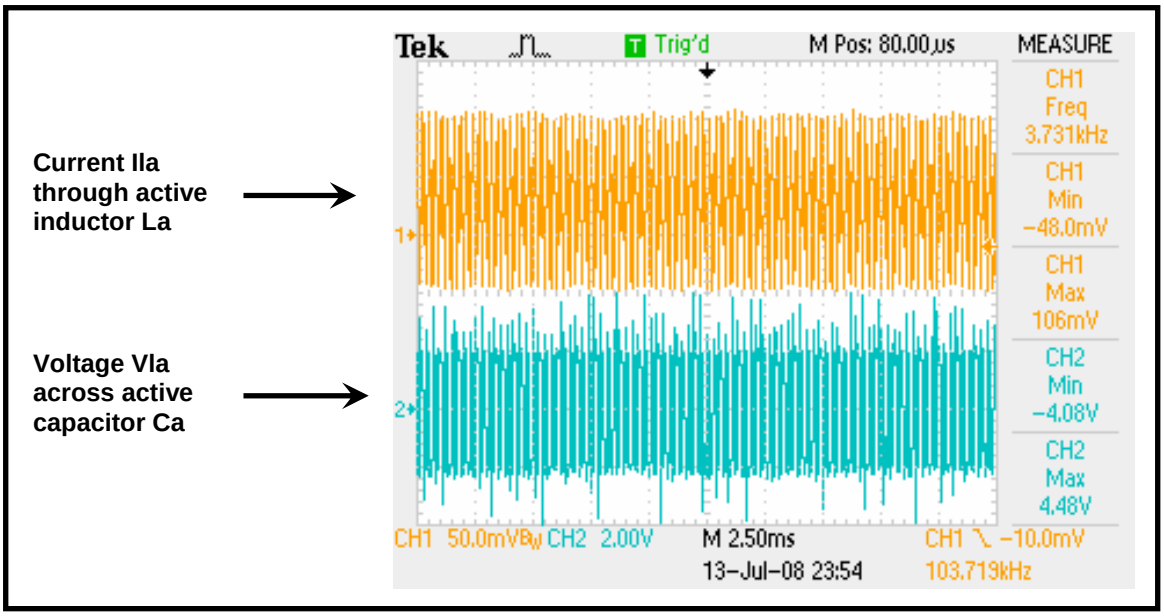


Figure 5.13 Low Frequency Active Inductor Current (Upper plot) and Voltage (Lower plot) at 20 V Input Voltage, Ch 1 at 50 mV/Div & 2 A scale, Ch 2 at 2 V/Div & 10 x multiplier

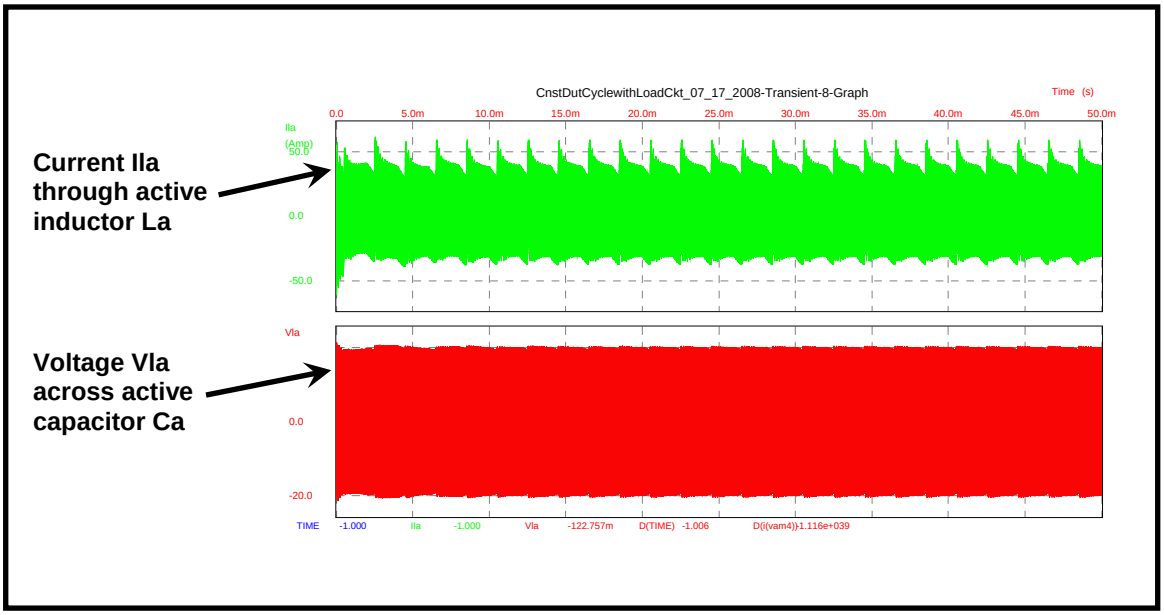


Figure 5.14 Low Frequency Active Inductor Current (Upper plot) and Voltage (Lower plot) at 20 V Input Voltage from SPICE simulation

The same parameters from SPICE simulation are shown in Figure 5.12. These same parameters are observed at low frequency. The test results are shown in Figure 5.13 and the SPICE simulation results are shown in Figure 5.14.

While the SPICE simulation results at high frequency and low frequency show that the average active inductor current and average active inductor voltage have a mean value of zero, the tests results show that the current has a non-zero average value. The voltage has a mean value of zero. This anomaly is due to the stray inductances, switching frequency noise and test circuit settings.

5.2.2 Test Results from Proportional Feedback Controlled Duty Cycle Operation of HAPF Circuit

In this section, the physical HAPF circuit as shown in Figure 5.1 is run at 20 V input voltage with proportional feedback controlled duty cycle. The test results are shown starting with Figure 5.15.

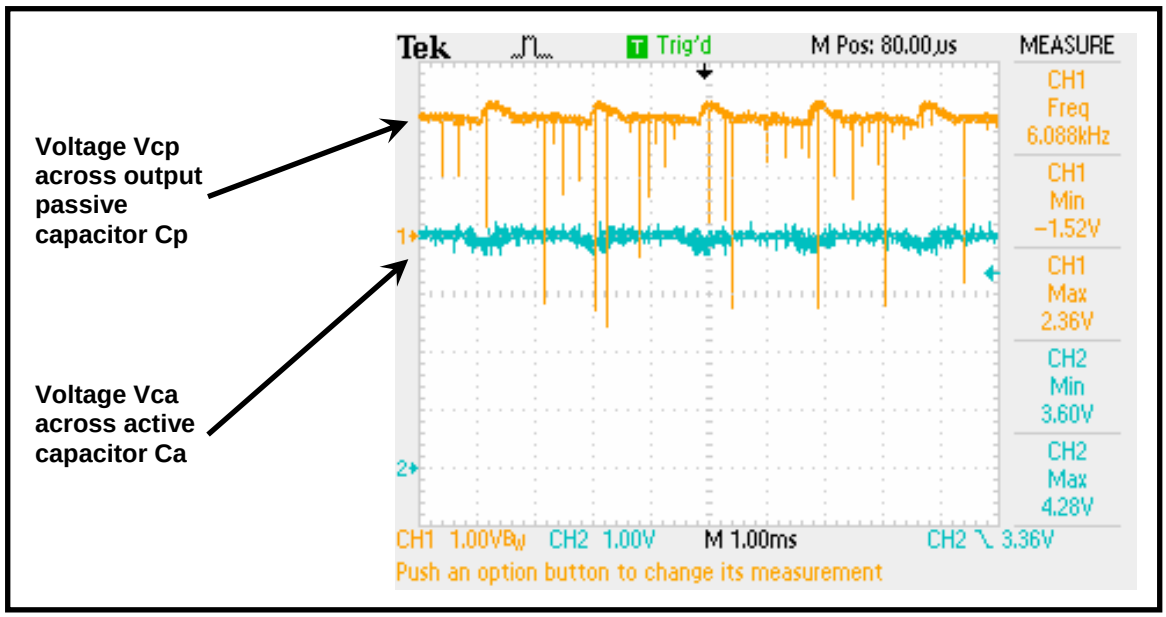


Figure 5.15 Low Frequency Passive Capacitor Voltage Vcp (Upper plot) and Active Capacitor Voltage Vca (Lower plot) with Proportional Feedback Control of Duty Cycle at 20 V Input Voltage, Ch 1 & Ch 2 at 1 V/Div & 10 x multiplier

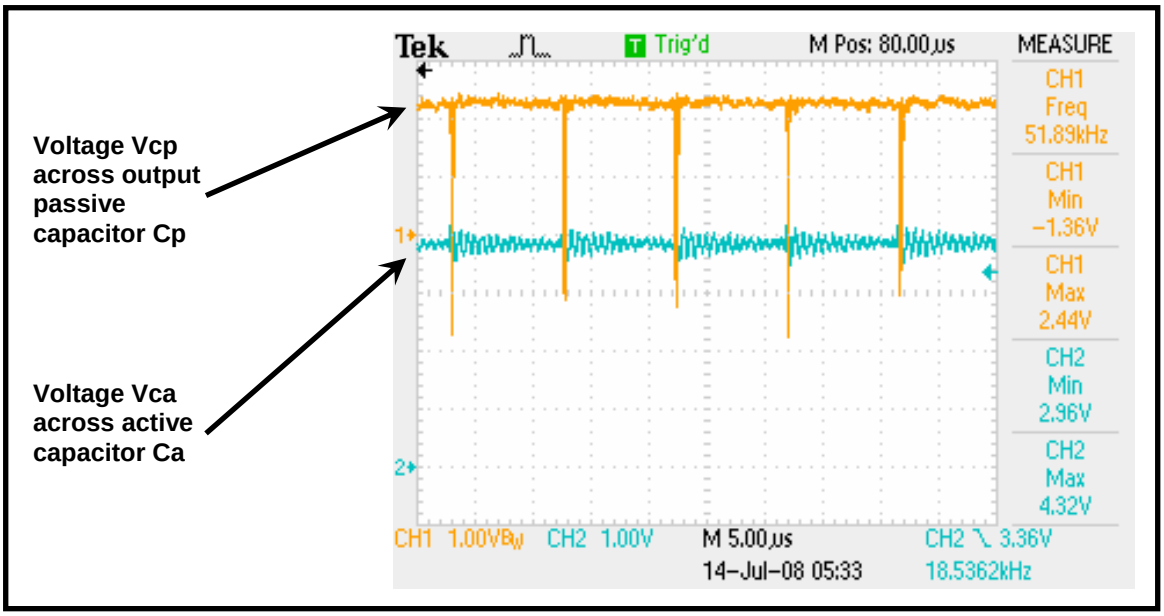


Figure 5.16 High Frequency Passive Capacitor Voltage Vcp (Upper plot) and Active Capacitor Voltage Vca (Lower plot) with Proportional Feedback Control of Duty Cycle at 20 V Input Voltage, Ch 1 & Ch 2 at 1 V/Div & 10 x multiplier

This figure shows the voltage across the output passive capacitor, Vcp and the active capacitor, Vca at low frequency. Figure 5.16 shows the same voltages at high frequency. It should be noted that there are two main frequencies of interest in all the test results' plots, the first being the low frequency corresponding to the load circuit switching frequency of 500 Hz and the second being the high frequency corresponding to the active section's switching frequency of 100 kHz.

From the test circuit plots it can be seen that the mean value of the output passive capacitor voltage is around 21 V with ripple of +- 2 V. The mean value of the active capacitor voltage is around 40 V with ripple of +- 2 V. These results are compared with the ones from section 5.2.1 in Figure 5.6 and Figure 5.7. With feedback control there is a significant reduction in the ripple. The ripple content in the output passive capacitor voltage has reduced by 6 V. And the ripple content in the active capacitor voltage reduced by 4 V. However, there is a switching frequency component in the output passive capacitor voltage.

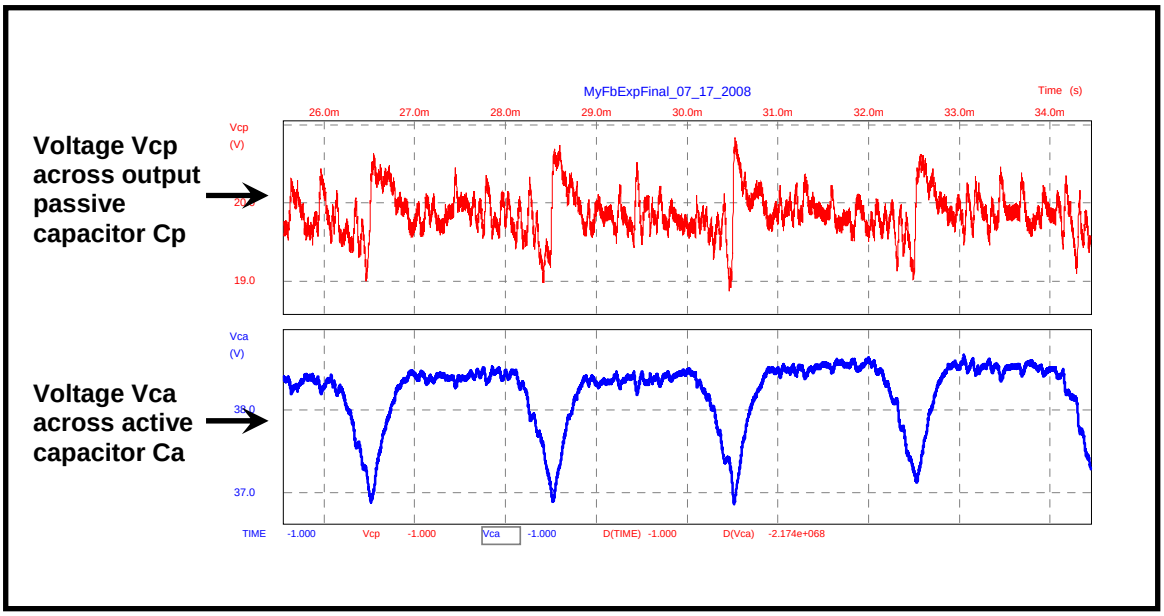


Figure 5.17 Low Frequency Passive Capacitor Voltage Vcp (Upper plot) and Active Capacitor Voltage Vca (Lower plot) at 20 V Input Voltage from SPICE simulation with Proportional Feedback Control of Duty Cycle

The SPICE model discussed in section 3.4 is modified such that the input voltage is 20 V and simulated. The passive capacitor voltage and active capacitor voltage is shown in Figure 5.17.

On comparison with the plots in Figure 5.15 and Figure 5.16, the mean value of the output passive capacitor voltage has reduced from 21 V to around 19.5 V. The mean value of the active capacitor voltage has reduced from 40 V to around 37.8 V. The ripple content seen in the test results are much greater than the ripple seen in the simulation results which is around +- 0.6 V. This is due to the SPICE circuit model being based on ideal conditions and components. The ripple seen in the physical circuit is due to noise entering the system and being exacerbated by stray inductances due to connecting wires.

The current through the input passive inductor from the test circuit is shown in Figure 5.18 and from SPICE simulation in Figure 5.19.

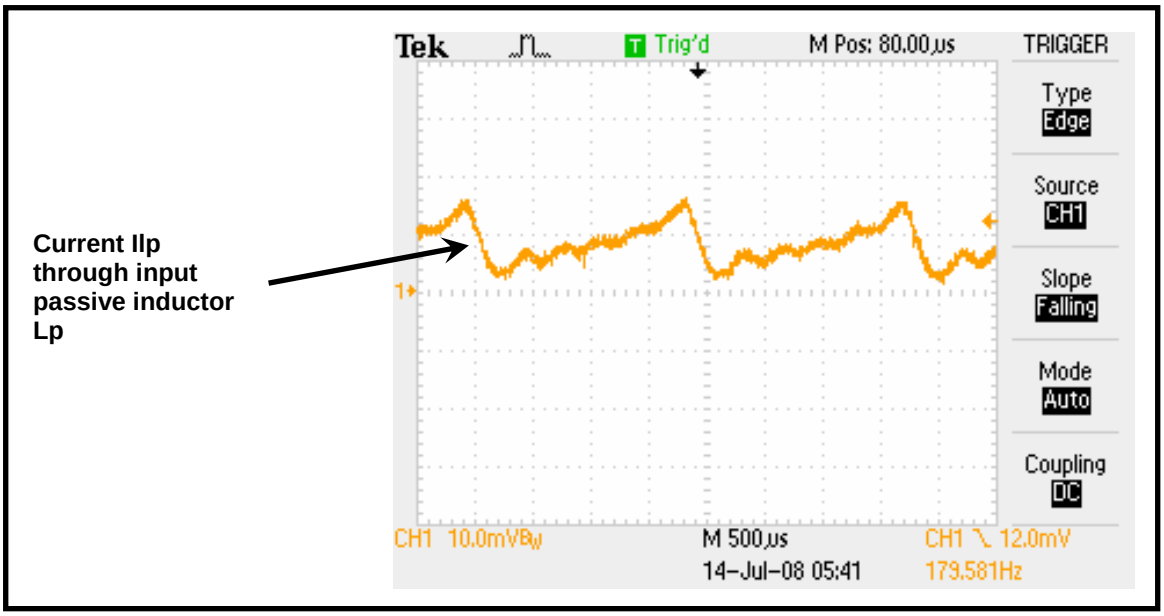


Figure 5.18 Low Frequency Input Passive Inductor Current with Proportional Feedback Control of Duty Cycle at 20 V Input Voltage, Ch 1 at 10 mV/Div & 2 A scale

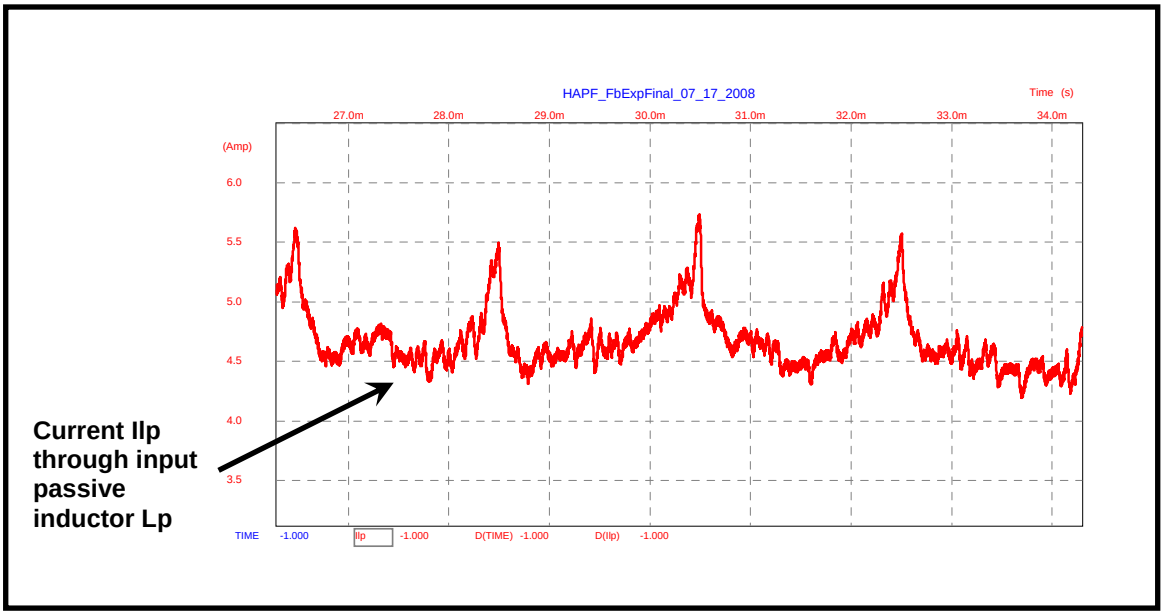


Figure 5.19 Low Frequency Input Passive Inductor Current at 20 V Input Voltage from SPICE simulation with Proportional Feedback Control of Duty Cycle

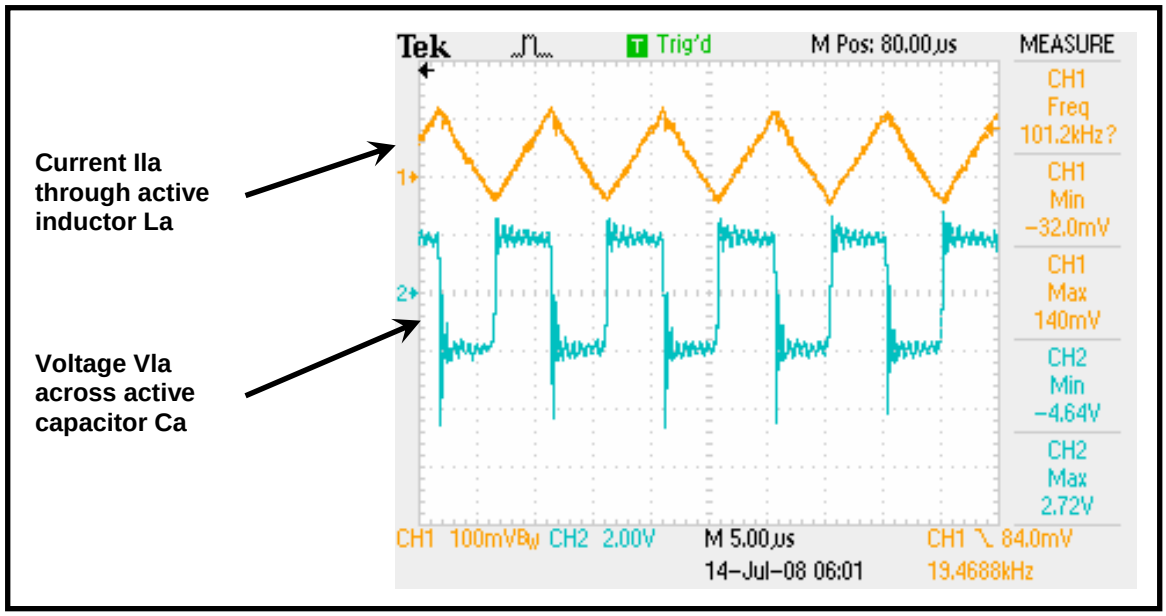


Figure 5.20 High Frequency Active Inductor Current (Upper plot) and Voltage (Lower plot) with Proportional Feedback Control of Duty Cycle at 20 V Input Voltage, Ch 1 at 100 mV/Div & 2 A scale, Ch 2 at 2 V/Div & 10 x multiplier

The input passive inductor current from the test circuit has a mean value of 1.4 A with a ripple of +- 0.4 A. SPICE simulation shows that the mean value is 4.75 A with a ripple of +- 0.4 A. It should be noted that the mean value does not match due to the changes made in the physical test circuit to reduce the magnitude of current.

The current through the active inductor and voltage across it are shown in Figure 5.20. The same parameters from SPICE simulation are shown in Figure 5.21.

These same parameters are observed at low frequency. These test results are shown in Figure 5.22.

The SPICE simulation results with the same parameters are shown in Figure 5.23.

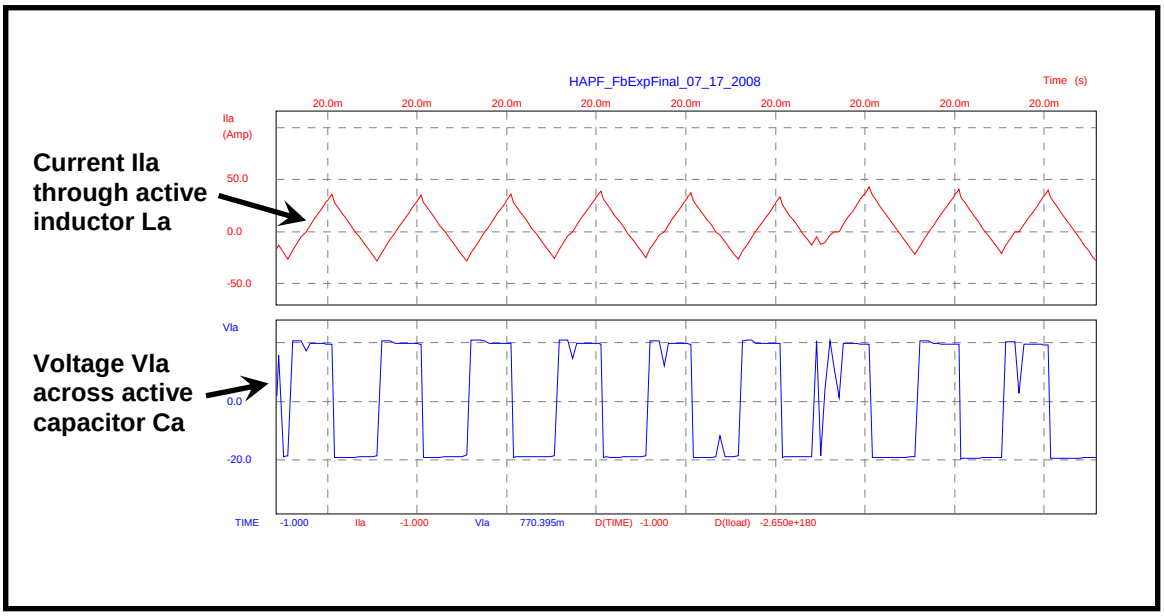


Figure 5.21 High Frequency Active Inductor Current (Upper plot) and Voltage (Lower plot) with Proportional Feedback Control of Duty Cycle at 20 V Input Voltage from SPICE simulation

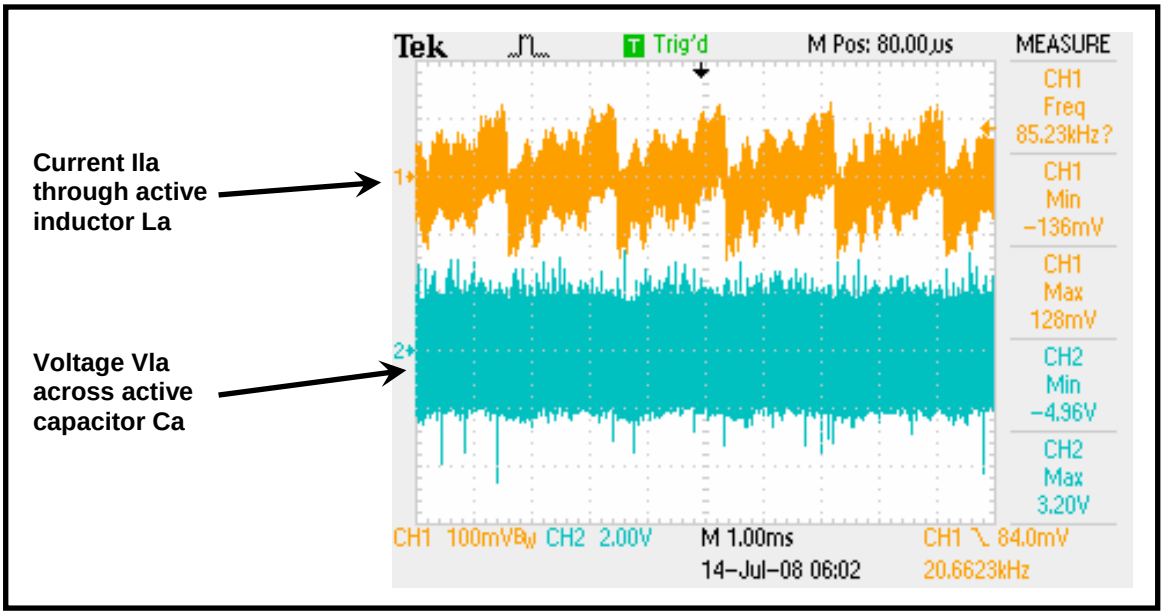


Figure 5.22 Low Frequency Active Inductor Current (Upper plot) and Voltage (Lower plot) with Proportional Feedback Control of Duty Cycle at 20 V Input Voltage, Ch 1 at 50 mV/Div & 2 A scale, Ch 2 at 2 V/Div & 10 x multiplier

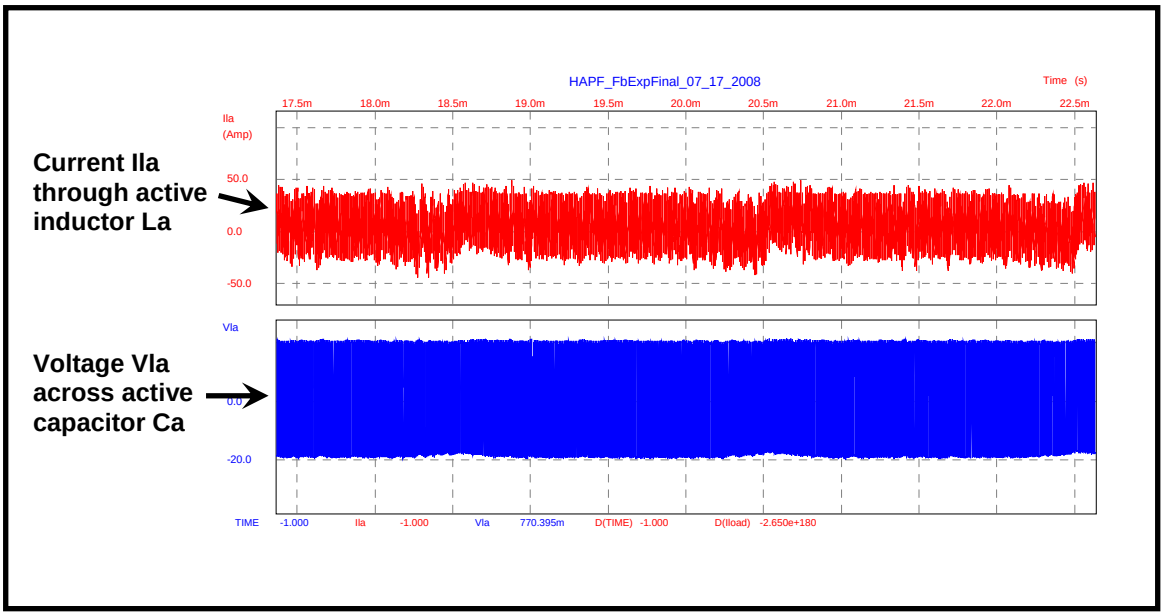


Figure 5.23 Low Frequency Active Inductor Current (Upper plot) and Voltage (Lower plot) with Proportional Feedback Control of Duty Cycle at 20 V Input Voltage from SPICE simulation

SPICE simulation results at high frequency and low frequency show that the average active inductor current and average active inductor voltage have a mean value of zero. With proportional feedback control of duty cycle, the test results show that the same current and voltage have a mean value of around zero.

In chapter 1, it was discussed that the benefit of using an active filter was the generation of equal and opposite current ripple which cancels the ripple generated by non-linear loads. The active section's current and voltage plot in Figure 5.22 is an indication of this compensation.

The results from constant duty cycle and proportional feedback control of duty cycle are summarized in Table 5.2.

Table 5.2 Comparison Table of Test Circuit and SPICE Simulation Results of Hybrid Active Power Filter with Constant Duty Cycle and Proportional Feedback Control of Duty Cycle

Parameter	Constant Duty Cycle Operation		Proportional Feedback Control of Duty Cycle	
	Circuit Test Results	Simulation Results	Circuit Test Results	Simulation Results
Vcp	22 V (mean) +- 8 V (ripple)	19.5 V (mean) +- 1 V (ripple)	22 V (mean) +- 1 V (ripple)	19.8 V (mean) +- 0.6 V (ripple)
Vca	40 V (mean) +- 10 V (ripple)	39.25 V (mean) +- 0.75 V (ripple)	39 V (mean) +- 2 V (ripple)	37.75 V (mean) +- 0.75 V (ripple)
Ilp	1.4 A (mean) 0.4 A (ripple)	4.5 A (mean) 0.6 A (ripple)	1.4 A (mean) 0.4 A (ripple)	4.75 A (mean) 0.4 A (ripple)
Ila	10 A (mean) +- 20 A (ripple)	10 A (mean) +- 40 A (ripple)	0 A (mean) +- 20 A (ripple)	0 A (mean) +- 40 A (ripple)
Vla	0 A (mean) +- 20 V (ripple)	0 A (mean) +- 20 V (ripple)	0 A (mean) +- 20 V (ripple)	0 A (mean) +- 20 V (ripple)

5.2.3 Test Circuit Concerns

The summary of results in Table 5.2 show significant differences between test circuit results and simulation results. This is mainly in terms of the voltage ripple in output

passive capacitor voltage and active capacitor voltage, mean current value in input passive inductor current, and mean current value in active inductor current and its ripple value. The reason behind this is two fold, the first being stray inductance and the second being circuit grounding. Stray inductances in the physical filter circuit are unavoidable due to connecting wires. The effect of stray inductances is explained using the following equation.

$$V_{wire} = L_{wire} \cdot \frac{dI_{wire}}{dt} \quad \textbf{5.1}$$

The plot of current through active section's inductor La shown in Figure 5.11, Figure 5.12, Figure 5.20 and Figure 5.21 is triangular. The above equation gives rise to a stray voltage which is a square wave. The active section of the hybrid filter operates at 100 kHz switching frequency and the stray inductance causes switching frequency noise to enter the whole filter system. The effect of this can be seen in the gate pulses driving the MOSFETs of the active section as shown in Figure 5.3. These spikes at turn ON and turn OFF are of the order of around 40 V. This value increases if the input voltage is increased. However, the spikes seen in the drain to source voltage of the active section's MOSFETs was greater than the ones seen in the gate to source voltage. And these MOSFETs have a maximum rating of 200 V. To ensure that none of the MOSFETs fail, the input voltage was not increased over 20 V.

The active section, passive section and equivalent load of the hybrid filter are connected across the terminals of the phase bus. This connection is shown below in Figure 5.24. The lower phase bus terminal is connected to the negative terminal of the DC power supply and the source of the MOSFET M2. This is also the ground terminal of the physical filter circuit. This connection causes noise to enter the equivalent load circuit gate driver, op-amp based feedback control circuit, the voltage sources powering the feedback control circuit, gate driver, PWM circuit and the input DC power supply Vin. The effect of this is shown in Figure 5.25, Figure 5.26 and Figure 5.27.

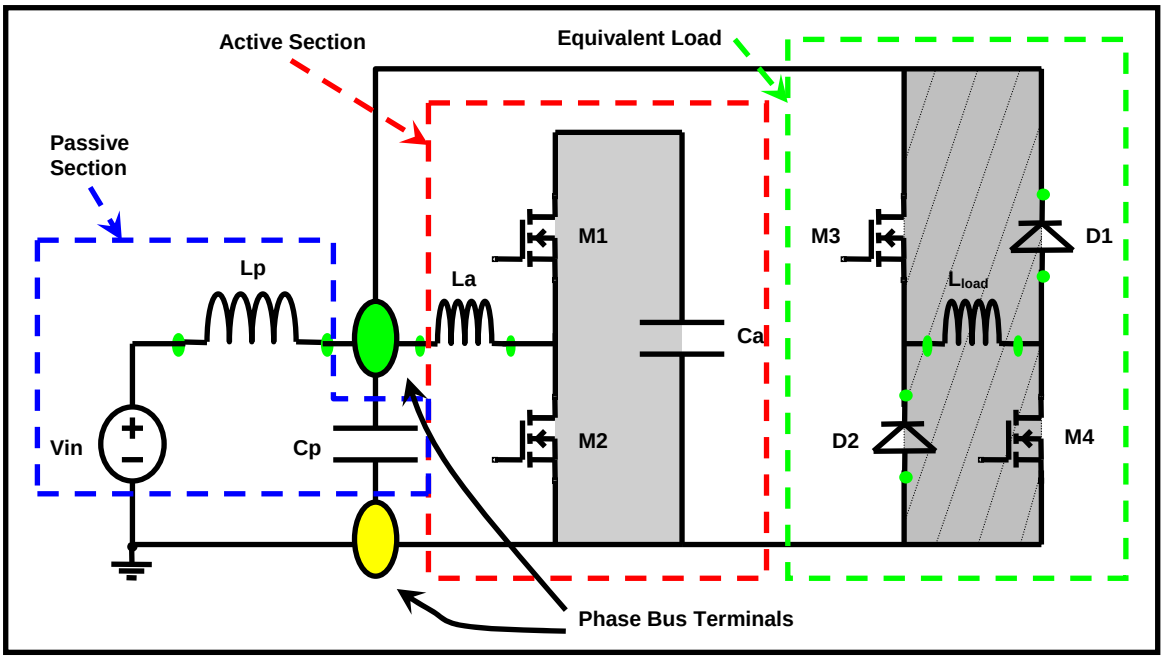


Figure 5.24 Hybrid Active Power Filter with Phase Bus Connections

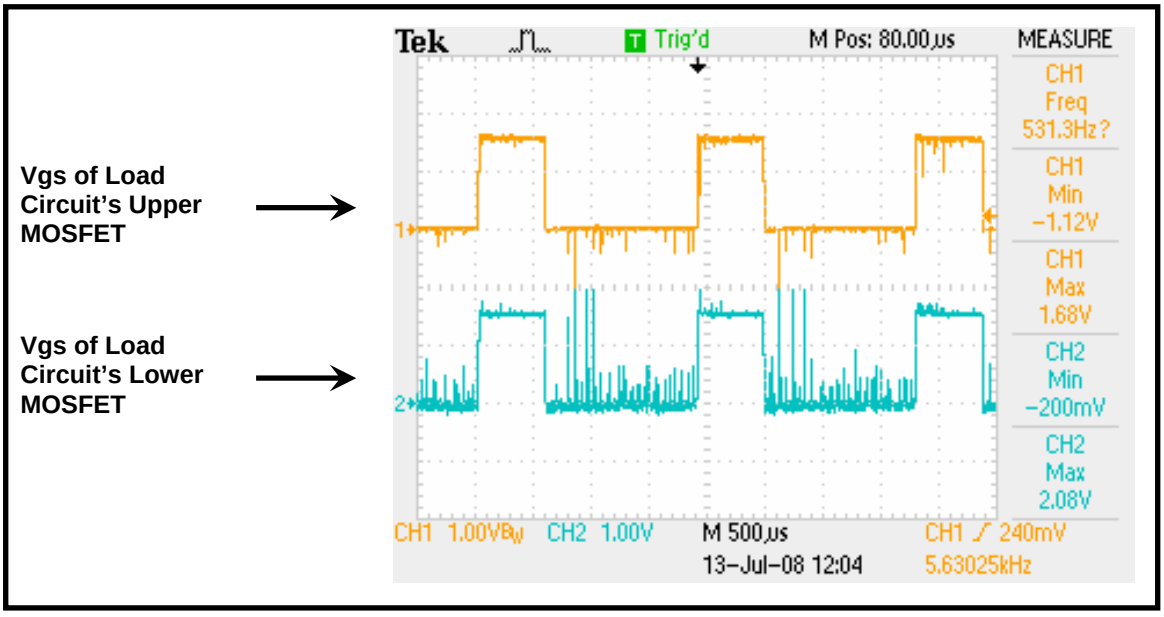


Figure 5.25 Spikes in Gate Pulses to MOSFETs of Load Circuit at 20 V Input Voltage, Vgs (M3, upper plot) & Vgs (M2, lower plot), 1 V/Div, 10 x multiplier

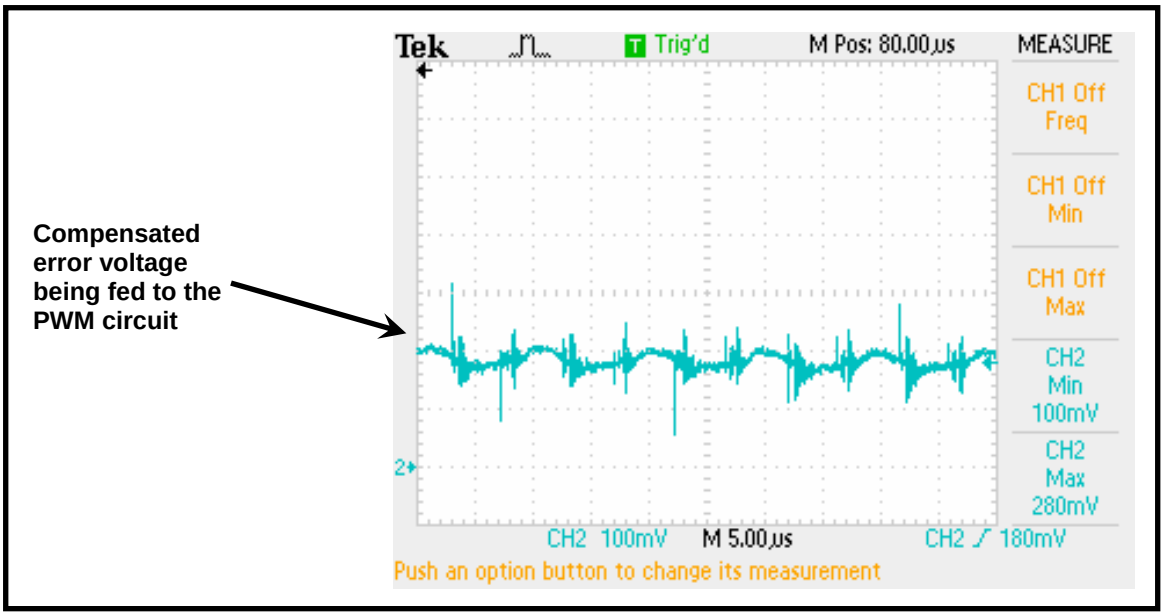


Figure 5.26 Spikes in compensated error voltage from op-amp based feedback control circuit fed to PWM circuit

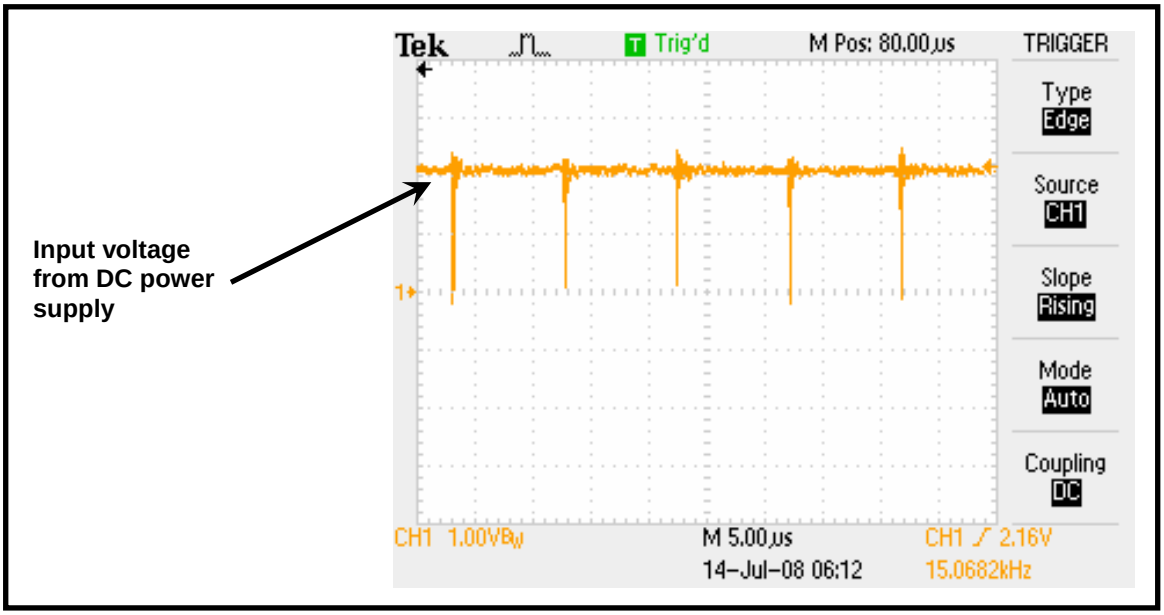


Figure 5.27 Spikes in input voltage supplied from DC power supply

6 Conclusion

The goal of this thesis was to design an input EMI filter for a SRM drive used in an aerospace application. The ripple current drawn from the DC supply by the SRM drive must meet conducted EMI regulations governed by Military STD 461. Due to size limitations in this application, it was necessary to reduce the size the input EMI filter.

This was addressed by implementing a hybrid active power filter that used passive components of smaller size when compared to a plain passive filter for achieving the same attenuation level. The hybrid active power filter that is the subject of this thesis was presented in the first chapter. The second chapter discussed different duty cycle control techniques that could be used. Firstly, constant duty cycle control was found to be unsuitable. Full state, state space feedback control and proportional feedback control of duty cycle were found to be suitable with the former being more effective. This was proved by simulating a Simulink model of the filter based on mathematical modeling. In the third chapter, an experimental design was proposed with proportional feedback control of duty cycle for the filter due to its ease in implementation in a laboratory environment. Chapter four discussed the components used in the filter test circuit. And chapter five presented results from laboratory testing of the filter circuit.

The test results show that proportional feedback control of duty cycle reduces the ripple content in the input current drawn from the DC supply. Additionally, the size of the filter was reduced.

The size reduction achieved in this thesis when compared to the original benchmark passive EMI filter is summarized in Table 6.1. The size reduction achieved in this thesis when compared to an earlier implementation [2] is summarized in Table 6.2.

Table 6.1 Summary of component values from benchmark passive EMI filter and hybrid active power filter

Component	Benchmark Passive EMI Filter	Hybrid Active Power Filter
Input Passive Inductor Lp	160 μH	160 μH
Output Passive Capacitor Cp	16,000 μF	400 μF
Active Inductor La	NA	1.6 μH
Active Capacitor Ca	NA	800 μF
Total Inductance	160 μH	161.6 μH
Total Capacitance	16,000 μF	1,200 μF

Table 6.2 Summary of component values from earlier novel filter [2] and current hybrid active power filter

Component	Earlier Novel Filter Implementation [2]	Hybrid Active Power Filter
Input Passive Inductor Lp	160 μH	160 μH
Output Passive Capacitor Cp	1,000 μF	400 μF
Active Inductor La	1.6 μH	1.6 μH
Active Capacitor Ca	1,600 μF	800 μF
Total Inductance	161.6 μH	161.6 μH
Total Capacitance	2,600 μF	1,200 μF

From the above two tables it can be seen that the overall inductance has not reduced by a significant margin. However, the hybrid filter implemented in this thesis has an overall capacitance reduction percentage of 92.5 % when compared to the benchmark passive EMI filter and 54 % when compared to an earlier novel filter implementation.

7 Future Research

The results from this thesis provide opportunities for further research without adversely affecting the performance of the filter. These are summarized below:

1. Evaluate impact of size reduction in output passive capacitor by a factor of 2.
2. Design an estimator for determining the individual states for state space feedback.
3. Verify simulation results from state space feedback control of duty cycle with state space estimator for the hybrid filter with SRM drive.
4. Physical implementation of current hybrid active power filter with state space estimator and state space feedback control for the hybrid filter with SRM drive.
5. Evaluate use of digital control techniques for duty cycle control
6. Evaluate performance of digital control of duty cycle for the hybrid filter with SRM drive using simulations
7. Physically implement hybrid filter with digital duty cycle control and evaluate its performance when coupled to SRM drive and SRM.

Appendix

Appendix A

Two different power filter topologies are presented here. These are used to highlight the benefits of using an active power filter with switching elements over a classic L-section passive power filter.

Passive Filter

Consider the first topology which shows a classic L-section filter in Figure A 1.

The system transfer function (output to input) for this filter is given by:

$$\frac{Vout}{Vsource} = \frac{1}{1 + \omega^2 \bullet L \bullet C}$$

The corresponding cutoff frequency is given by:

$$f_c = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C}}$$

With Lin = 1mH and Cin = 1μF, the cutoff frequency is 5.033 KHz.

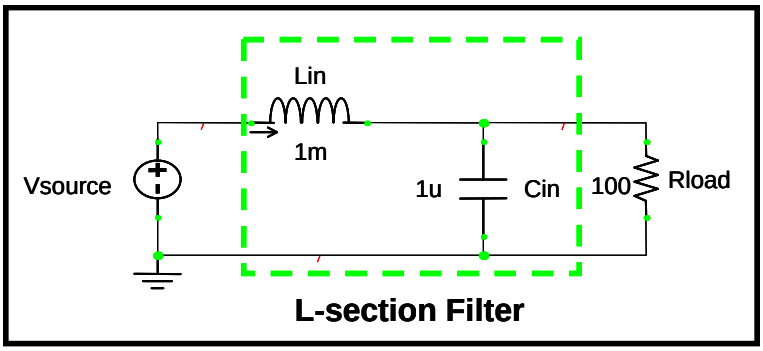


Figure A 1 An L-section filter

Active Filter

The second topology obtained from Reference [2] is explained starting with the circuit in Figure A 2.

The capacitor current (same as the inductor current) is given by:

$$Vsource = Vl + Vc$$

$$iC = iL = C \bullet \frac{dVc}{dt}$$

$$iC = C \bullet \frac{d(Vsource - Vl)}{dt}$$

Now consider a switch based filter (active filter) as shown in Figure A 3.

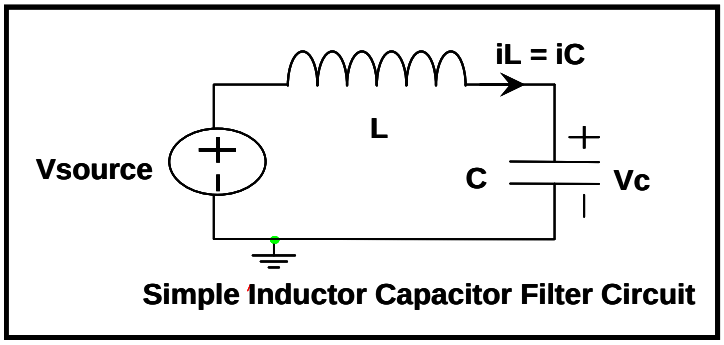


Figure A 2 A simple inductor capacitor based filter circuit

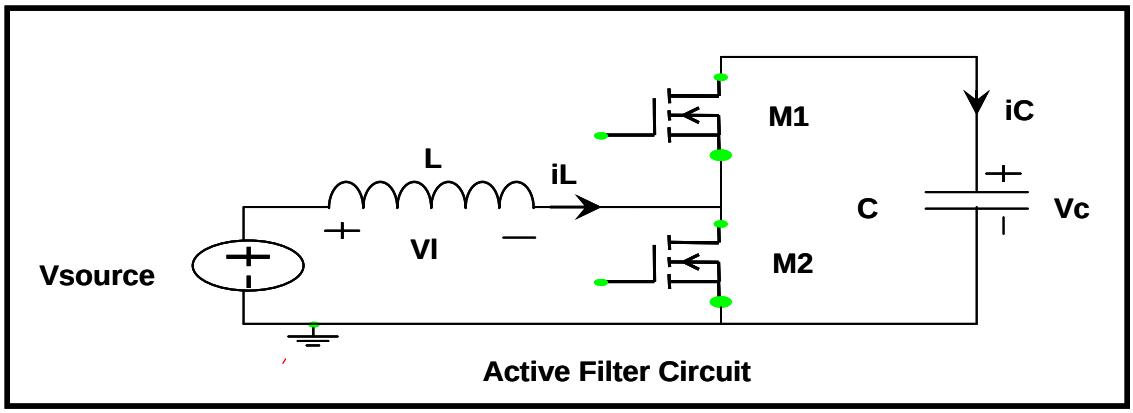


Figure A 3 Proposed active filter circuit configuration

From Figure A 3 it is evident that the switching circuit resembles a boost converter topology. The capacitor current exists only when the upper switch (MOSFET M1) is closed. Also, voltage builds up across the capacitor. The duty cycle of the switch is given as the ratio of its on-time to off-time over a single period. This period depends on the switching frequency of the switches Based on this the following equations for capacitor current and voltage are obtained.

$$iC = D \bullet iL$$
$$Vsource = D \bullet Vc + Vl$$
$$Vc = \frac{Vsource - Vl}{D}$$

Using these equations, the current through the capacitor is found as shown below.

$$iC = C \bullet \frac{dVc}{dt}$$
$$D \bullet iL = C \bullet \frac{d(\frac{Vsource - Vl}{D})}{dt}$$
$$iL = \frac{C}{D^2} \bullet \frac{d(Vsource - Vl)}{dt}$$
$$iL = C_{eq} \bullet \frac{d(Vsource - Vl)}{dt}$$
$$C_{eq} = C / D^2$$

Using these above set of equations, a circuit similar to the one in Figure A 2 is obtained with an equivalent capacitor replacing the switch-capacitor combination. This is shown in Figure A 4.

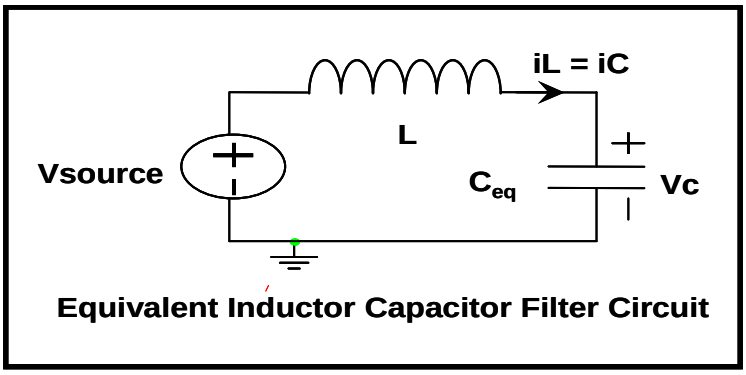


Figure A 4 Equivalent circuit obtained from the active filter circuit

Table A 1 Comparison table showing the benefit of using an active filter versus a conventional L-section filter.

Filter Type	L-section Filter	Active Filter
Inductance L	1mH	1mH
Capacitance C	1uF	1uF (Equivalent Capacitance)
Cutoff Frequency Fc	5.033KHz	5.033KHz
Duty Cycle D	NA	0.75
Actual Capacitance	1uF	1uF x (0.75^2) = 0.5625uF
Reduction in Capacitance (%)	0	43.75%

The use of active switching elements has reduced the size of the capacitor by a factor of D^2 where D is the duty cycle of the switch and is always less than 1. Note that the above circuit is similar to that of the earlier discussed L-section filter. The results of using the L-section filter and active filter are as tabulated in Table A 1 for the same cut-off frequency.

A duty cycle value of 0.75 is used in the above calculated results. Since the proposed active filter is of boost converter topology, the active capacitor voltage (voltage across the capacitor connected across the two switches) is always higher than the input voltage (source voltage). This voltage is inversely proportional to the duty cycle. If the duty cycle is low, the capacitance reduction is huge, but the downside is that the capacitor voltage increases proportionately. This defeats the purpose of reducing the size of the capacitor

(as the size of a capacitor is determined in terms of its energy rating). Using a constant duty cycle is also detrimental (explained in introduction chapter). Therefore, a higher duty cycle was used in the above calculation.

However, when the same was extended in the design of the active filter in this thesis, it was found that due to the high duty cycle, the effective capacitance was reduced. This caused more ripple to enter the system. Simulation results (from constant duty cycle operation in chapter 2) show that a steady state operating duty cycle between 20 % and 30 % produced the most satisfactory results.

Appendix B

Matlab code used in Simulink to run simulations with proposed hybrid filter model coupled with SRM drive

```
%% Small signal model state space equations

Rsin = 27.5*10^-3;
Rpin = 2.5; %1*10^3;
Lin = 160*10^-6; %160*10^-6;
Vindc = 42;
Cout = 400*10^-6;
Rsa = 5.1*10^-3;
Rpa = 5; %1*10^3;
La = 2.3*10^-6; %1.6*10^-6;
Ca = 800*10^-6;
Dbar = 0.25;

a11 = -Rsin/(Lin*(1 + Rsin/Rpin));
a12 = 1/(Lin*(1 + Rsin/Rpin));
a13 = 0;
a14 = 0;

a21 = -Rpin/(Cout*(Rsin+Rpin));
a22 = (-1/Cout)*(1/(Rsin+Rpin) + 1/(Rsa+Rpa));
a23 = Rpa/(Cout*(Rsa+Rpa));
a24 = Dbar/(Cout*(Rsa+Rpa));

a31 = 0;
a32 = -1/(La*(1 + Rsa/Rpa));
a33 = -Rsa/(La*(1 + Rsa/Rpa));
a34 = Dbar/(La*(1 + Rsa/Rpa));

a41 = 0;
a42 = Dbar/(Ca*(Rsa+Rpa));
a43 = -Dbar*Rpa/(Ca*(Rsa+Rpa));
a44 = -(Dbar^2)/(Ca*(Rsa+Rpa));


b1 = 0;
b2 = Vindc/(Dbar*Cout*(Rpa+Rsa));
b3 = Vindc/(Dbar*La*(1 + Rsa/Rpa));
b4 = -Vindc/(Ca*(Rsa+Rpa));

%% Small signal analysis based on the linearization of the state space
averaged non-linear model

Asmsg = [a11 a12 a13 a14;
         a21 a22 a23 a24;
         a31 a32 a33 a34;
         a41 a42 a43 a44];
```

```
Bsmsg = [b1; b2; b3; b4];

Csmsg = [0 1 0 0];

Dsmsg = [0];

eigasmsg = eig(Asmsg);

[num1, den1] = ss2tf(Asmsg, Bsmsg, Csmsg, Dsmsg);
sys1 = tf(num1, den1);
%rlocus(sys1)
%bode(sys1)

ctr = ctrb(Asmsg, Bsmsg)
obs = obsv(Asmsg, Csmsg)

%% State space feedback
polesmsg = eig(Asmsg);
p1 = polesmsg(1);
rep1 = real(p1);
imp1 = imag(p1);
newimp1 = 500;

pol1 = rep1+newimp1*i;
pol2 = conj(pol1);

pol = [pol1 pol2 -500+100i -500-100i]
% Note that I'm changing the dominant poles and only the imaginary part
of the other two poles, this implementation doesn't meet MIL STD 461

kpol = place(Asmsg, Bsmsg, pol)
knew = [0.003, -0.175, 0.0005, 0.001];
%Based on individual state error feedback, values found by trial and
error starting with proportional feedback gain value of 0.2 for 2nd
state, used in chapter 2 in state space feedback section

%% My Detailed Model of Active Filter which uses above found gains for
feedback control

ad11 = -Rsin*Rpin/(Lin*(Rsin+Rpin));
ad12 = -Rpin/(Lin*(Rsin+Rpin));
ad13 = 0;
ad14 = 0;

ad21 = Rpin/(Cout*(Rsin+Rpin));
ad22 = (-1/Cout)*(1/(Rsin+Rpin) + 1/(Rsa+Rpa));
ad23 = -Rpa/(Cout*(Rsa+Rpa));
ad24 = 1/(Cout*(Rsa+Rpa));

ad31 = 0;
ad32 = Rpa/(La*(Rsa+Rpa));
ad33 = -Rsa*Rpa/(La*(Rsa+Rpa));
ad34 = -1*Rpa/(La*(Rsa+Rpa));
```

```
ad41 = 0;
ad42 = 1/(Ca*(Rsa+Rpa));
ad43 = 1*Rpa/(Ca*(Rsa+Rpa));
ad44 = -(1^2)/(Ca*(Rsa+Rpa));

bd11 = Rpin/(Lin*(Rsin+Rpin));
bd12 = 0;

bd21 = 1/(Cout*(Rsin+Rpin));
bd22 = -1/Cout;

bd31 = 0;
bd32 = 0;

bd41 = 0;
bd42 = 0;

%% My Detailed Model State Space Equations (Passive + APF)
Adtld = [ad11 ad12 ad13 ad14;
         ad21 ad22 ad23 ad24*Dbar;
         ad31 ad32 ad33 ad34*Dbar;
         ad41 ad42*Dbar ad43*Dbar ad44*Dbar*Dbar];

Bdtld = [bd11 bd12; bd21 bd22; bd31 bd32; bd41 bd42];

Cdtld = [0 1 0 0];

Ddtld = [0 0];

eigadtld = eig(Adtld);

%%Passive filter used in Dr.Radun's SRM Model (equations developed by
GM)
Vsource = 42;
Cpowerm = 16e-3;
Rpowerm = 0; %equivalent series resistance of the capacitor

Lm = 160e-6;
Rsm = 70e-3; %equivalent series resistance of the inductance
Rpm = 2; %equivalent parallel resistance of the inductance

Apassive = [-Rsm*Rpm/(Lm*(Rsm+Rpm)) -Rpm/(Lm*(Rsm+Rpm));
            Rpm/(Cpowerm*(Rsm+Rpm)) -1/(Cpowerm*(Rsm+Rpm))]

Bpassive = [Rpm/(Lm*(Rsm+Rpm)) 0;
            1/(Cpowerm*(Rsm+Rpm)) -1/Cpowerm]

Cpassive = [1 0;
            0 1]

Dpassive = [0 0;
            0 0]

eigpassive = eig(Apassive)
```

```
%%Passive filter used in Xiaohu's thesis (equations developed by GM)

Vs = 42;
Cp = 1000e-6;
Rcp = 0; %equivalent series resistance of the capacitor

Lp = 160e-6;
Rps = 27.5e-3; %equivalent series resistance of the inductance
Rpp = 2.5; %equivalent parallel resistance of the inductance

Ax = [-Rps*Rpp/(Lp*(Rps+Rpp)) -Rpp/(Lp*(Rps+Rpp));
            Rpp/(Cp*(Rps+Rpp)) -1/(Cp*(Rps+Rpp))]

Bx = [Rpp/(Lp*(Rps+Rpp)) 0;
            1/(Cp*(Rps+Rpp)) -1/Cp]

Cx = [1 0;
            0 1]

Dx = [0 0;
            0 0]

eigax = eig(Ax)
```

Appendix C

Matlab code to obtain FFT

```
%
%   Compute the FFT of one cycle of the 400Hz.
%
%   and plot the transfer function with the output FFT
%
clear Icyclink Vcycpower Icycin Fh tff Ifflink Vffpower Iffin;
clear vIpowerff vIpowerdb Iiinff Iiindb;
clear Ilinkdb Vpowerdb IindbuA;
clear  vHIpowerff  vHIpowerdb  phvHIpowerdeg  iHIinff  iHIindbuA  phiHIindeg
HIinff HIindbuA;
clear Ittlink vHIpowertt iHIintt;
%
%  Compute the number of points in a cycle
%
ncyc=8;
tl=length(tout1);
Flinkm=(rpmCS/60)*Nrpm*Nrepm*Nphm;
Tlinkm=1/Flinkm;
Npntcyc=floor(Tlinkm/tsave);
%
%   Create the link voltage (Vpower) and input current (Ilink) for one
cycle.
%
Icyclink(1:ncyc*Npntcyc)=iharm(tl+(1:ncyc*Npntcyc)-ncyc*Npntcyc);
Ilinkdc=mean(Icyclink);
Vcycpower(1:ncyc*Npntcyc)=Vcp(tl+(1:ncyc*Npntcyc)-ncyc*Npntcyc);
Vpowerdc=mean(Vcycpower);
Icycin(1:ncyc*Npntcyc)=Ilp(tl+(1:ncyc*Npntcyc)-ncyc*Npntcyc);
Iindc=mean(Icycin);
%
%  Make the harmonic frequency vector and the inverse fft time vector
%
Fh(1:ncyc*Npntcyc)=(0:(ncyc*Npntcyc-1))*Flinkm/ncyc;
tff(1:ncyc*Npntcyc)=(0:(ncyc*Npntcyc-1))*tsave;
%
%  Take the FFT of Ilink, Vpower, and Iin
%
Ifflink=sqrt(2)*fft(Icyclink)/(ncyc*Npntcyc);
Ifflink(1)=1;
Vffpower=sqrt(2)*fft(Vcycpower)/(ncyc*Npntcyc);
Vffpower(1)=1;
Iffin=sqrt(2)*fft(Icycin)/(ncyc*Npntcyc);
Iffin(1)=1;
%
%  Express the FFT of Ilink, Vpower, and Iin in db
%
IlinkdbuA=20*log10(abs(Ifflink/1e-6))-3.01;
Vpowerdb=20*log10(abs(Vffpower));
IindbuA=20*log10(abs(Iffin/1e-6))-3.01;
%
% Compute the filters performance using the Fourier spectrum of Ilink
```

```
%
Aemi=[-Rsm/(Lm*(1+Rsm/Rpm))            -1/(Lm*(1+Rsm/Rpm))
      1/(Cpowerm*(1+Rsm/Rpm))          -1/(Cpowerm*(Rsm+Rpm))];
Bemi=[0
      -1/Cpowerm ];
CIemi=[1/(1+Rsm/Rpm)           -1/(Rsm+Rpm)];
CVemi=[0                       1];
Iemi=eye(size(Aemi));
for n=1:ncyc*Npntcyc
   jw=i*2*pi*Fh(n);
   AIemi=jw*Iemi-Aemi;
   vHIpowerff(n)=CVemi*(AIemi\Bemi)*Ifflink(n);
   vHIpowerdb(n)=20*log10(abs(vHIpowerff(n)));
   phvHIpowerdeg(n)=180*angle(vHIpowerff(n))/pi;
   iHIinff(n)=CIemi*(AIemi\Bemi)*Ifflink(n);
   iHIindbuA(n)=20*log10(abs(iHIinff(n)/1e-6))-3.01;
   phiHIindeg(n)=180*angle(iHIinff(n))/pi;
   HIinff(n)=CIemi*(AIemi\Bemi);
   HIindbuA(n)=20*log10(abs(HIinff(n)));
end;
%
% Specification
%
idbuAspec=[110, 110, 90, 70];
Fspec=[1.0e+2, 1.0e+3, 1.0e4, 1.0e+5];
%
% plot 1
semilogx(Fh,Vpowerdb,Fh,vHIpowerdb); grid
title('Link Voltage db, Link Voltage db from ilink')
%
%    Compute the inverse Fourier transforms of spectrum calculated
quantities
Ifflink(1)=0;
Ittlink=ncyc*Npntcyc*real(ifft(Ifflink))/sqrt(2)+Ilinkdc;
vHIpowerff(1)=0;
vHIpowertt=2*ncyc*Npntcyc*real(ifft(vHIpowerff))/sqrt(2)+Vpowerdc;
iHIinff(1)=0;
iHIintt=2*ncyc*Npntcyc*real(ifft(iHIinff))/sqrt(2)+Ilinkdc;
%
% plot 2
figure;
plot(tff,Ittlink,tff,Icyclink); grid
title('Ipower/Ilink simulation and harmonic')
%
% plot 3
figure
plot(tff,vHIpowertt,tff,Vcycpower); grid
title('Vcycpower from simulation and vHIpowertt from harmonic')
%
% plot 4
figure
semilogx(Fh,IindbuA,Fh,iHIindbuA,Fspec,idbuAspec); grid
title('IindbuA and iHIindbuA computed from the transfer function and
mil std 461')
%
% plot 5
figure
```

```
plot(tff,Icycin,tff,iHIintt); grid
title('Icycin from simulation and iHIintt from harmonic')
%
% plot 6
figure
semilogx(Fh,HIindbuA); grid
title('The transfer function from Vpower to Iin')
% plot 7
figure
semilogx(Fspec,idbuAspec,Fh,IlinkdbuA); grid
title('mil std 461 and IlinkdbuA')
% plot 8
figure
semilogx(Fspec,idbuAspec,Fh,IlinkdbuA,Fh,IindbuA); grid
title('Mil std 461 and IlinkdbuA and IindbuA')
```

References

[1] Power Electronics – Converters, Applications and Design, Ned Mohan, Tore M. Undeland and William P. Robbins, John Wiley & Sons, Inc., 2003

[2] Active Filter for Improving a Switched Reluctance Motor Drive's Input Power Quality – Xiaohu Feng, Master's Thesis, University of Kentucky, March 2005

[3] Theoretical and Experimental Investigation of the Fast- and Slow-Scale Instabilities of a DC–DC Converter, Sudip K. Mazumder, Ali H. Nayfeh, and Dushan Boroyevich, IEEE Transactions on Power Electronics, VOL. 16, NO. 2, March 2001

[4] Active Filter Design Techniques, Chapter 16, Texas Instruments, 2001

[5] Understanding Power System Harmonics, W. Mack Grady, and Surya Santoso, IEEE Power Engineering Review, November 2001

[6] Design and Evaluation of Feedforward Active Ripple Filters, Mingjuan Zhu, David J. Perreault, Vahe Caliskan, Timothy C. Neugebauer, Stephan Guttowski, and John G. Kassakian, IEEE Transactions on Power Electronics, VOL. 20, NO. 2, March 2005

[7] A Basic Introduction to Filters - Active, Passive, and Switched-Capacitor, National Semiconductor Application Note 779, Kerry Lacanette, April 1991

[8] Power Line Filter Design Considerations for DC-DC Converters, Daniel M. Mitchell, IEEE Industry Applications Magazine, November/December 1999

[9] EMI Suppression with Switching Frequency Modulated DC-DC Converters, Mahinda Vilathgamuwa, J Deng and K. J. Tseng, IEEE Industry Applications Magazine, November/December 1999

[10] Simplified Analysis of PWM Converters Using Model of PWM Switch Part1: Continuous Conduction Mode, Vatche Vorperian, IEEE Transactions on Aerospace and Electronic Systems, VOL. 26, NO. 3, May 1990

[11] A Large Signal Dynamic Model for DC-DC Converters with Average Current Control, Yun W. Lu, Guang Feng, Yan-Fei Liu, Applied Power Electronics Conference and Exposition, 2004, APEC 2004, Nineteenth Annual IEEE, VOL. 2, On page(s): 797-803

[12] A general unified approach to modeling switching-converter power stages, R. D. Middlebrook and Slobodan Cuk, IEEE Power Electronics Specialists Conference, 1976, On page(s): 18-34.

[13] Switched Reluctance Motor Drives: Modeling, Simulation, Analysis, Design, and Applications, R. Krishnan, CRC Press, 2001

[14] Small-capacitance non-dissipative ripple filters for DC supplies, S. Feng, W. Sander, and T. Wilson, IEEE Transactions on Magnetics, VOL. 6, Issue. 1, Mar 1970, On page(s): 137 – 142

[15] Active filters for 1-MHz power circuits with strict input/output ripple requirements, L. E. LaWhite and M. F. Schlecht, IEEE Transactions on Power Electronics, VOL. PE-2, NO. 4, Oct. 1987, On page(s): 282 – 290

[16] Active Power Filter for Nonlinear AC Loads, Janko Nastran, Rafael Cajhen, Matija Seliger, and Peter Jereb, IEEE Transactions on Power Electronics, VOL. 9, NO. 1, January 1994, On page(s): 92 – 96

[17] A Novel Control Approach to the DC Active Power Filter Used in a Low Ripple and Large Stable/Pulse Power Supply, Guochun Xiao, Yunqing Pei, Kuang Li, Xu Yang, and Zhaoan Wang, IEEE Power Electronics Specialist Conference, 2003(34th Annual), VOL. 4, Issue, 15-19 June 2003, On page(s): 1489 – 1493

[18] Comparison of Four Control Methods to Active Power Filters Applied in Accelerator Power Supplies, Kuang Li, Guochun Xiao, Jinjun Liu, and Zhaoan Wang, 35th Annual IEEE Power Electronics Specialists Conference, 2004

[19] A Simple Control Scheme for Hybrid Active Power Filter, Darwin Rivas, Luis Moran, Juan Dixon, Jose Espinoza, 31st Annual IEEE Power Electronics Specialists Conference, VOL. 2, 2000, On page(s): 991 – 996

[20] Techniques for Input Ripple Current Cancellation: Classification and Implementation, N. K. Poon, J. C. P. Liu, K. Tse, and M. H. Pong, IEEE Transactions on Power Electronics, VOL. 15, NO. 6, November 2000

[21] Design and Evaluation of a Hybrid Passive/Active Ripple Filter with Voltage Injection, Albert C. Chow and David J. Perreault, IEEE Transactions on Aerospace and Electronic Systems, VOL. 39, NO. 2, April 2003

[22] A Hybrid Active Filter for Damping of Harmonic Resonance in Industrial Power Systems, Hideaki Fujita, Takahiro Yamasaki, and Hirofumi Akagi, IEEE Transactions on Power Electronics, VOL. 15, NO. 2, March 2000

[23] Motor Drive Active DC Link Filter – Progress Report, Art V. Radun, University of Kentucky, February 2006

[24] Harmonics Mitigation Using Active Power Filter: A Technological Review, Zainal Salam, Tan Perng Cheng and Awang Jusoh, Elektrika, VOL. 8, NO. 2, 2006, On page(s): 17 – 26

[25] New Trends in Active Filters for Power Conditioning, Hirofumi Akagi, IEEE Transactions on Industry Applications, VOL. 32, NO. 6, November/December 1996

[26] Active power filters – A review, M.El-Habrouk, M.K.Darwish and P.Mehta, IEE Proceedings – Electrical Power Applications., VOL. 147, NO. 5, September 2000

[27] Performance comparison of three phase active power filter algorithms, H. L. Jou, IEE Proceedings – Generations, Transmission and Distribution, VOL 142, NO. 6, November 1995

[28] Design and implementation of a modified Fourier analysis harmonic current computation technique for power active filters using DSPs, M.El-Habrouk and M.K.Darwish, IEE Proceedings – Electrical Power Applications, VOL. 148, NO. 1, January 2001

[29] Dead-Beat Current Control for Active Filters, L Malesani, P. Mattavelli and S. Buso, Proceedings of the Industrial Electronics Conference (IECON), Aachen, Germany, 1998, On page(s): 1859 – 1864

[30] DSP – Based Active Power Filter with Predictive Current Control, Seung – Gi Jeong and Myung – Ho Woo, IEEE Transactions on Industrial Electronics, VOL. 44, NO. 3, June 1997

[31] Modern Control Systems, Richard C. Dorf and Robert H. Bishop, 8th Edition, 2004

[32] Feedback Control of Dynamic Systems, Gene F. Franklin, J. David Powell and Abbas Emami – Naeini, 4th Edition, 2002

[33] Regulating Pulse Width Modulator UC25256AN Specification Sheet, Unitrode (TI), 1999

[34] IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF, Data Sheet No. PD60147 rev.U, 03/23/2005, www.irf.com

[35] Application Note AN-978, RevD, 03/23/2007, www.irf.com

[36] LM741 Operational Amplifier Specification Sheet, National Semiconductor, August 2000

VITA

Govind Malleichervu was born in Hyderabad, India. He received his Bachelor degree in Electrical and Electronics Engineering from Rashtreeya Vidyalaya College of Engineering, Bangalore, Karnataka, India, affiliated to Visveswaraiah Technological University in 2003. He worked as an OEM (Original Equipment Manufacturer) Application Engineer for Rockwell Automation in New Delhi/Chennai, India from 2003 to 2005. In the fall of 2005, he started his Master of Science degree in Electrical Engineering at the University of Kentucky in Lexington, Kentucky, USA. He worked as a funded Research Assistant under Dr. Arthur V. Radun from January 2006 to December 2006. During the course of his Master's he interned with Control & Automation Inc, Lexington, Kentucky, USA in the summer of 2006 and with Robert Bosch GmbH, Stuttgart, Germany in the summer of 2007. He has been working with Cummins Inc, Columbus, Indiana, USA as a Controls Test Engineer since February 2008.