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INVESTIGATIONS OF $CuInTe_2$ / CdS & CdTe / CdS HETEROJUNCTION SOLAR CELLS

THESIS

A thesis submitted in partial fulfillment of the
requirements for the degree of Master of Science in Electrical Engineering
in the College of Engineering
at the
University of Kentucky

By

Venkatesh Gutta

Lexington, Kentucky

Director: Dr. Vijay P. Singh, Professor of EE

Lexington, Kentucky

2011

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ABSTRACT OF THESIS

INVESTIGATIONS OF $CuInTe_2$ / CdS & CdTe / CdS HETEROJUNCTION SOLAR CELLS

Thin film solar cells of Copper Indium Telluride and Cadmium Sulfide junctions were fabricated on plain ITO glass slides and also on those coated with intrinsic Tin Oxide. CdS was deposited through chemical bath deposition and CIT by electrodeposition. Both compounds were subjected to annealing at temperatures between 350°C and 500°C which produced more uniform film thicknesses and larger grain sizes. The CIT/ CdS junction was characterized after performing XRD and spectral absorption of individual compounds.

Studies were also made on CdS / CdTe solar cells with respect to effect of annealing temperatures on open circuit voltages. NP acid etch, the most important process to make the surface of CdTe tellurium rich, was also studied in terms of open circuit voltages. Thermally evaporated CdS of four different thicknesses was deposited on Tin Oxide coated ITO and inferences were drawn as to what thickness of CdS yields better results.

KEYWORDS: Copper Indium Telluride (CIT), Electrodeposition, Chemical Bath Deposition, Cadmium Sulfide, Cadmium Telluride, Thermal Evaporation

Venkatesh Gutta

November 16th 2011

INVESTIGATIONS OF $CuInTe_2$ / CdS & CdTe / CdS HETEROJUNCTION SOLAR CELLS

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THESIS

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2011

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Chapter 1 Introduction

1.1 Introduction

Global energy production levels are falling short of demand. The situation is worse in many third-world countries. The abundance and quality of electricity and its perennial supply are the most important factors contributing to the growth of a country's economy. As per U.S. Energy and Information Administration's data [1], the world energy consumption shall rise drastically in countries outside the Organization for Economic Cooperation and Development (non-OECD nations).

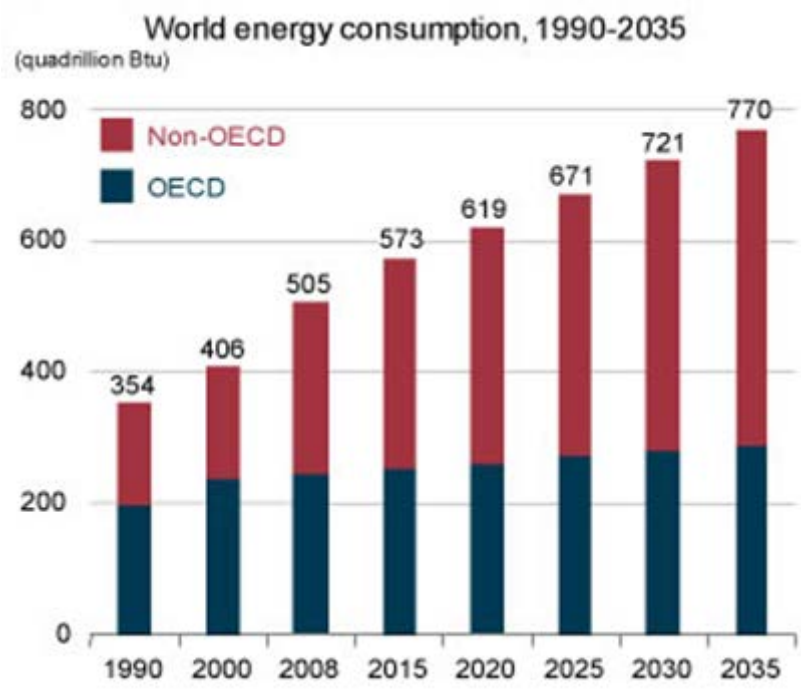


Figure 1.1: World Energy Consumption 1990-2035 in Quadrillion Btu units forecasted by U.S. Energy and Information Administration (EIA) in report DOE/EIA-0484 (2011) [Ref. 1]

The increasing gap in demand and supply of electricity can be shortened if electricity production from non-conventional sources is encouraged. Traditionally, electricity production is done through coal, oil or natural gas [2]. The overwhelming demand for these fuel sources combined with the inability to produce from or restore

the depleted layers of rock which are the main source of these traditional fuels has had a great impact on every country's economy. Here comes the need for non-traditional energy sources or the so called renewable energy sources like water, wind, biomass, solar, tides, geothermal and nuclear power [2]. Renewable energy sources contribute towards more than 16% of world's energy supply.

Renewable energy sources are those available in nature free-hand. If used wisely, these sources can completely eliminate the dependence on traditional energy sources. Currently, electricity is being produced in various countries by water and wind. Electricity from water is produced at a hydro-power station from water falling on turbines and that from wind is produced at a wind-mill where the wind rotates rotor blades. As per 2010 data, hydro-power has a worldwide capacity of 1,010 GW. This makes up to 21% of electricity from renewable sources [3]. Wind power of 197 GW has been reported in 2010 world energy census [4].

Nuclear fission and fusion reactions are the sources of nuclear power [5]. A controlled fission or fusion reaction can produce quantifiable heat which produces steam and in-turn steam rotates the turbines to produce electricity. Nuclear power has a world share of 14% with a majority of that share being generated in first-world countries. Uncontrolled nuclear fission and fusion reactions pose a risk to the environment. If these reactions are not properly controlled they may lead to a nuclear disaster which can destroy a city or a country including all life and property in that area. These potential risks from nuclear energy ask for high end nuclear reactors with up-to-date security features. Such a project would take a large amount of public money and the cost of such power is higher than that produced from other traditional and non-traditional energy sources.

Solar power is generated from the solar radiation incident on our planet [6]. The abundance of such an energy source combined with its availability at various regions on the planet has proved to be a boon for mankind. Most ancient users of solar radiation are plants and trees as they use the radiation from the Sun during the process of

photosynthesis to convert water and carbon dioxide to carbohydrates in presence of Chlorophyll. The photoelectric effect [7] was first observed by Heinrich Hertz and is described as a process by which electrons can be emitted from a metal or a non-metallic solid by exposing them to radiation. This was later verified by Albert Einstein and a series of papers published by him on the photoelectric effect has brought him a Nobel Prize in 1921.

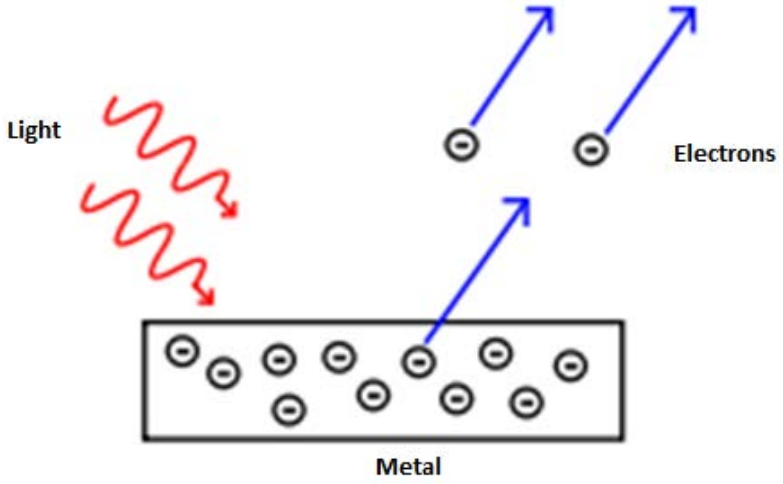


Figure 1.2: Illustration of Photoelectric effect [Ref 7]

Solar energy has been used by many ancient civilizations for a variety of works [6]. The most important of all those uses is heating materials with the help of solar energy. Solar radiation consists of UV, Visible and IR wavelengths. IR wavelength radiation is responsible for heating of materials. Solar water heaters and cookers are most prominent in different third-world economies. Solar water heaters installed over house roofs are perfect examples for heating property of Sun's radiation.

Figure 1.3: Illustration of Solar energy utilization for heating purposes [Ref 6]

Solar power generation is the process of converting solar energy into electricity. This is done using Photovoltaic materials. Photovoltaic materials are those in which electron-hole pairs are generated as a result of incident solar radiation. These electron-hole pairs are separated inside the solar cell by the presence of an electric field. The electrons then travel through the external circuit before they recombine with the holes.

Shockley-Queisser Theory:

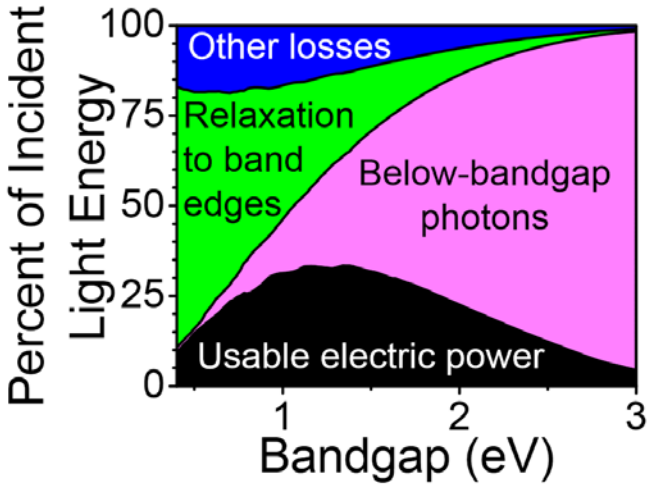


Figure 1.4: Shockley-Queisser depiction of light energy used against band-gap of material [Ref 8]

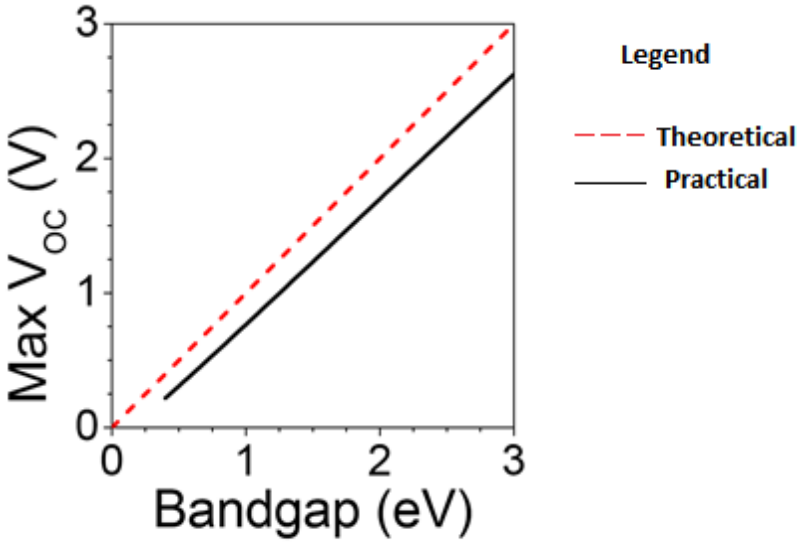


Figure 1.5: Shockley-Queisser depiction of open circuit voltage against band-gap of material [Ref 8]

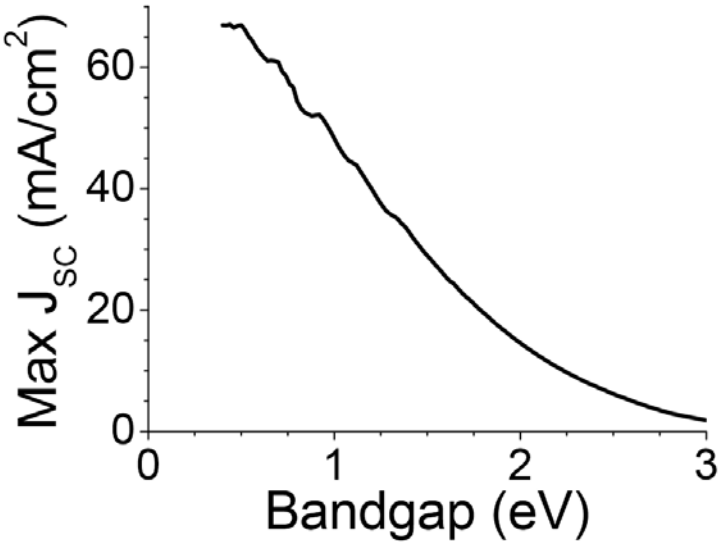


Figure 1.6: Shockley-Queisser depiction of short circuit current against band-gap of material [Ref 8]

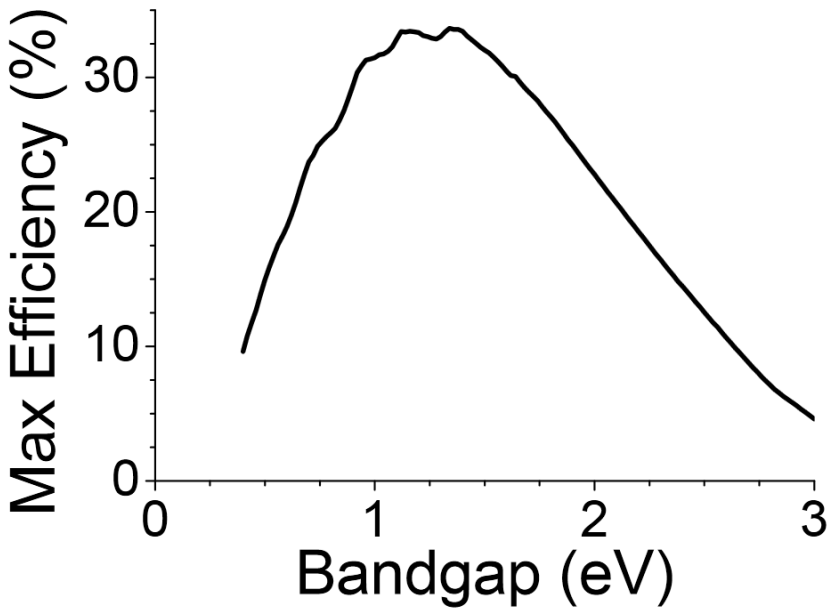


Figure 1.7: Shockley-Queisser depiction of maximum possible efficiency against band-gap of material [Ref 8]

Ideally, the open circuit voltage seen on the solar cell should be equal to the built-in potential difference at the junction in the solar cell. But the recombination process and other factors decrease the open circuit voltage seen across the device. This has been studied by William Shockley and Hans Queisser [8]. They've also studied the factors that contribute toward short-circuit current losses. The major factors are reflection, glass absorption, TCO absorption, window layer absorption, and deep-penetration losses.

Solar cells can be made by a p-n homo-junction or hetero-junction based device. Solar cells based on multi-junction concentrators have also been studied by various groups and they do not follow the limits set forth by Shockley and Queisser. A homo-junction based solar cell is made from a single crystal in which n-type and p-type dopants are induced from either side. These can be abrupt junctions or graded junctions. A hetero-junction based device on the other hand is made by bringing

together two completely different crystals one each doped with n-type and p-type materials.

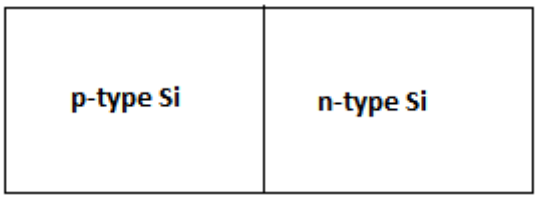


Figure 1.8: Illustration of homo-junction solar cell

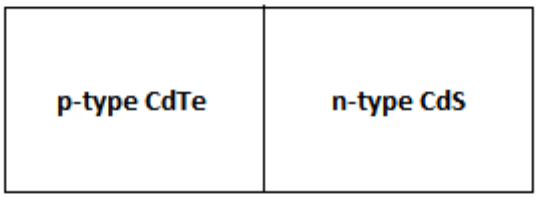


Figure 1.9: Illustration of hetero-junction solar cell

Solar cells can be fabricated using Silicon or Thin Film technology. Silicon based solar cells have been researched for a long time and provide the maximum efficiencies known to date with respect to regular solar cells [9]. Thin Film technologies have been investigated in the past couple of decades as a means to overcome the increasing costs of silicon solar cell fabrication. Thin Film technologies can be based over the following –

- Cadmium Telluride
- Copper Indium Gallium Selenide (CIGS)
- Gallium Arsenide
- Light Absorbing Dyes (DSSC)
- Organic / Polymer materials

Thin Film solar cells are being preferred to Silicon solar cells because Silicon is an indirect band-gap semiconductor. Silicon solar cell fabrication costs are rising too leaving the market open for Thin Film Solar cells.

The high cost of photovoltaic (PV) solar panels remains a major obstacle for rapid market penetration. There is a considerable amount of worldwide research to develop a low-cost device with an adequate efficiency for solar energy conversion [10]. Among the most promising materials suitable for the fabrication of low-cost thin film solar cells, ternary I-III-VI_2 semiconductors with chalcopyrite structure are considered as leading candidates. The most studied member of the family CuInGaSe2 (CIGS) has a direct band gap of about 1.20 eV and a high absorption coefficient ($1*10^5$ cm^{-1}). Interest in these materials has increased since 19.7% efficiency was reported by the NREL group [11], while in the superstate mode, Solar cells of 12.8% efficiency under normal operation have also been reported [12]. However, the efficiency of CIGS seems to saturate and further improvements require a deeper understanding of the underlying physics of the device, in addition to optimization of material growth and post-deposition processing steps. One of the challenges with this alloy material is the high volatility of selenium. This problem should be alleviated by substituting the selenium by the less volatile element tellurium.

The present research project is aimed at exploring the growth of $CuInTe_2$ (CIT) using a low-cost electrodeposition technique, characterizing the material in order to establish required properties for solar cells, and fabrication of devices from the resulting layers. The advantages of electrodeposition as a method of preparing thin films for photovoltaic applications are well-known [13], and include - the low capital cost of the equipment required, the adaptability to large area growth and the use of normal laboratory conditions for growing materials, without the requirement of vacuum systems.

CdTe based solar cells, on the other hand, are the most researched after Silicon solar cells. To date solar cells of 17.3% efficiency [14] have been reported and panels of

12% efficiency and more have also been reported. CdTe has a direct band gap of 1.44eV which is ideal for a photo semiconductor application as per Shockley-Queisser theory. Also the ease and effectiveness of Chemical Bath Deposition of CdS is a reason behind the great success of these solar cells [15]. CdTe is a direct band-gap material unlike Silicon which is an indirect band-gap material. Indirect band-gap materials are not efficient in terms of energy conversion. From Shockley Queisser Theory [15], it is evident that CdTe has a theoretical maximum efficiency of around 34%. CdTe for CdTe based solar cells can be deposited through Thermal Evaporation or Closed Space Sublimation (CSS) techniques. From many studies it was concluded that Closed Space Sublimation produces better results when compared to Thermal Evaporation. CdS for CdTe based solar cells can be made by Chemical Bath Deposition (CBD) or Thermal Evaporation. CBD is by far the most fruitful method of CdS deposition.

Let us now dive into the theory of solar cells, principles of operation of CIT-CdS and CdTe-CdS solar cells and their fabrication techniques.

Chapter 2 Theory

2.1 Semiconductor device structure and p-n junction formation

Semiconductors are solid state materials whose conductivity can be changed very low (insulators) or very high (as in the case of metals). Electric current in both metals and semiconductors is closely related to the flow of electrons. Many electrons are tied to the parent atom and are unable to contribute to the electric current. However, the regular placement of atoms in metals and semiconductors provides the conditions for some electrons to be shared between the atoms in the crystal. It is these electrons that contribute to the electric current [16].

Semiconductors as we know are materials whose characteristics can be modified by doping. Doping with n-type material gives the semiconductor properties with predominantly electron-based conduction while that with a p-type material gives the semiconductor a hole dominant conduction property.

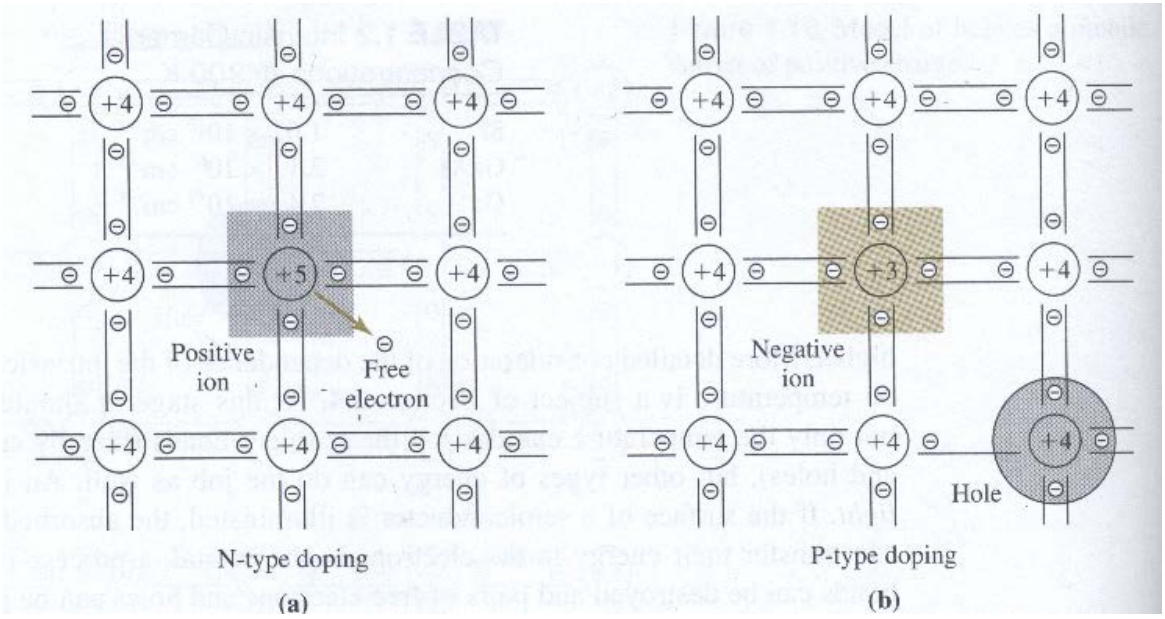


Figure 2.1: Two dimensional model of Silicon with dopants of a) n-type b) p-type [Ref.42]

2.1.1 p-n Junction

When a p-type semiconductor and an n-type semiconductor are fabricated in the same material they form what is called a p-n junction. The energy band diagrams related to the p-n junction formation are shown below –

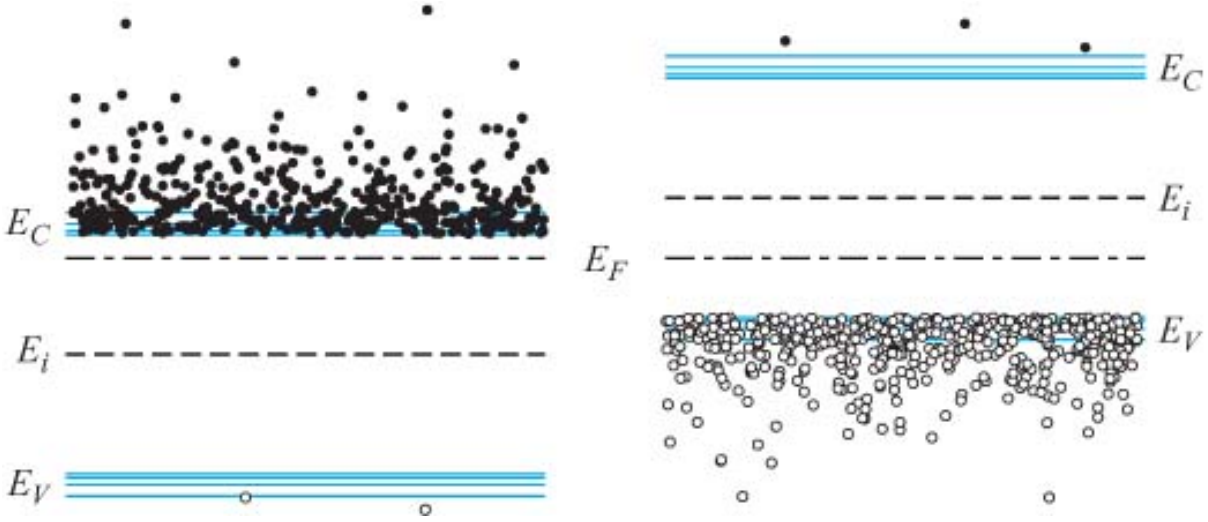


Figure 2.2: Energy band diagrams of n-type (left) and p-type (right) semiconductors [Ref.16]

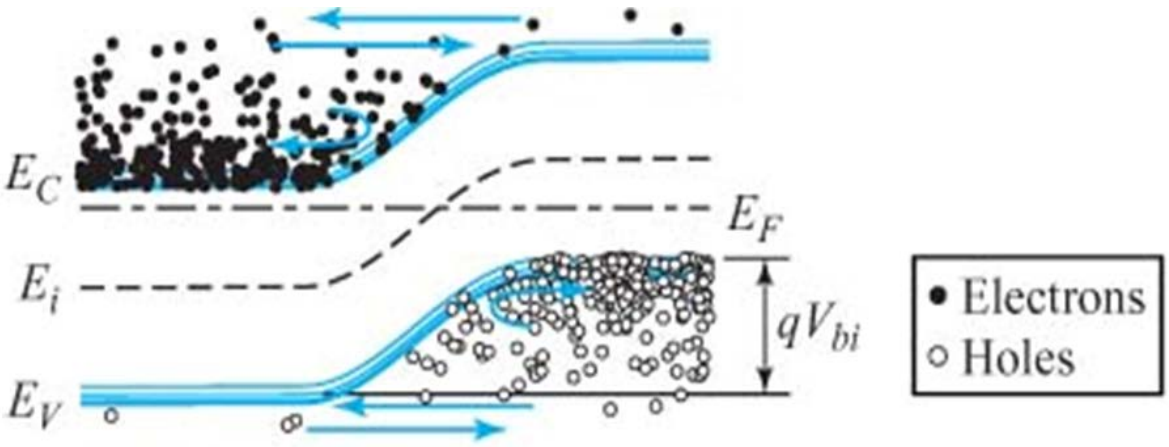


Figure 2.3: p-n junction energy band diagram [Ref. 16]

During this process Fermi levels are aligned, E_c and E_v energy levels bend which creates an energy difference, qV_{bi} and leads to a built in potential, V_{bi}.

The junction then undergoes diffusion of charge carriers from both the sides which forms the depletion region. This diffusion creates an electric field in the depletion region which in turn stops the flow of excess charge carriers.

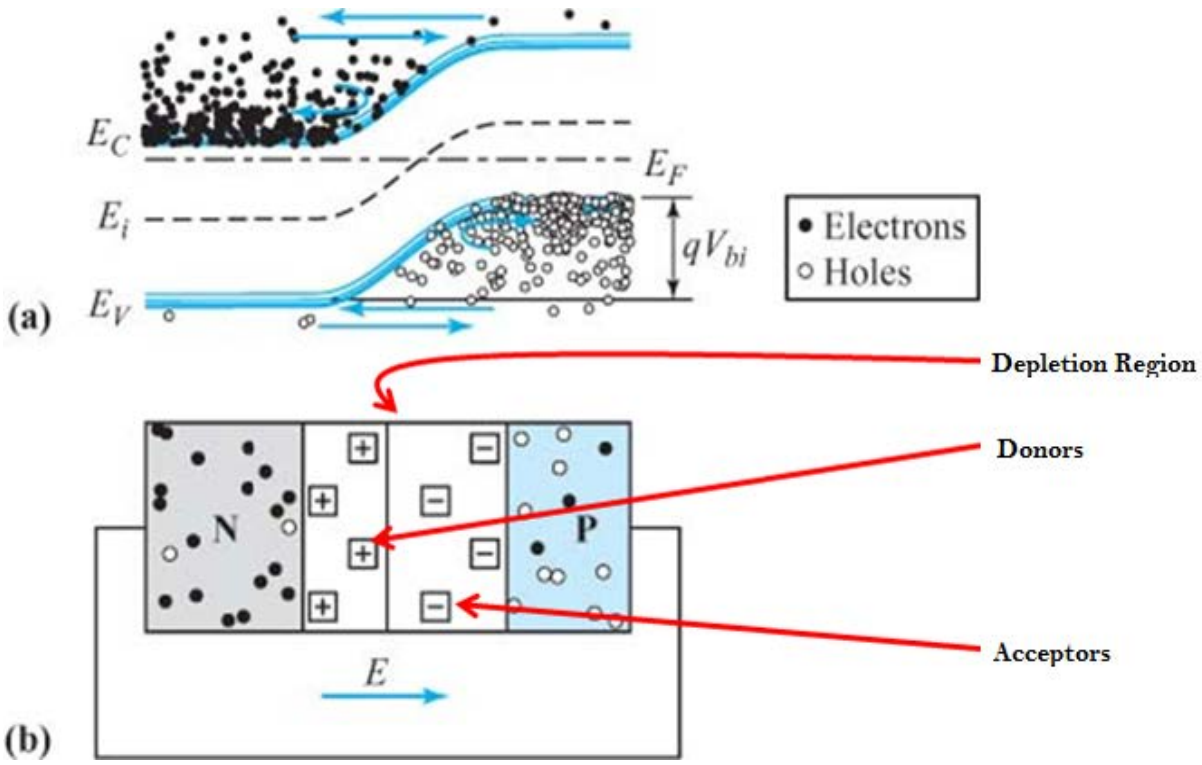


Figure 2.4: Illustration of (a) energy bands and (b) depletion region and immobile charge carriers in p-n junction under no bias [Ref. 16]

Reverse biased p-n junction:

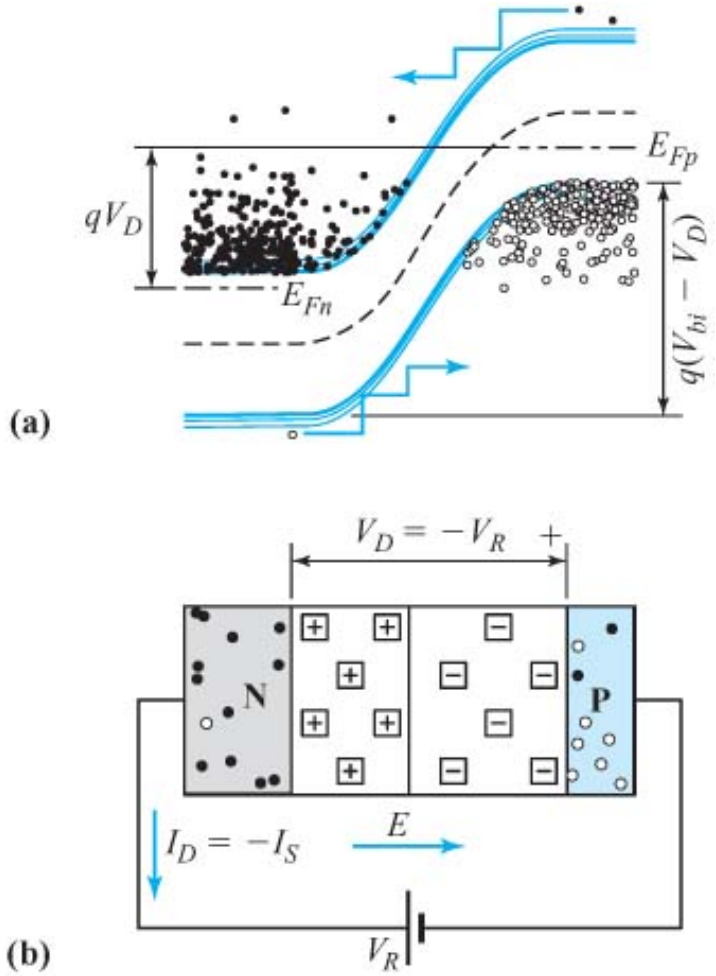


Figure 2.5: Illustration of (a) energy bands and (b) depletion region and immobile charge carriers in p-n junction under reverse bias [Ref. 16]

A negative voltage on the p-side reverse biases a pn-junction.

- The separation in bands changes by the applied voltage (in an ideal diode).
- A large barrier exists at the junction and essentially no electrons and holes can diffuse across.
- A few electrons and holes can drift across, but there are few minority carriers available for this process. Thus, we get a constant small current, I_S, in reverse bias.

Forward biased p-n junction:

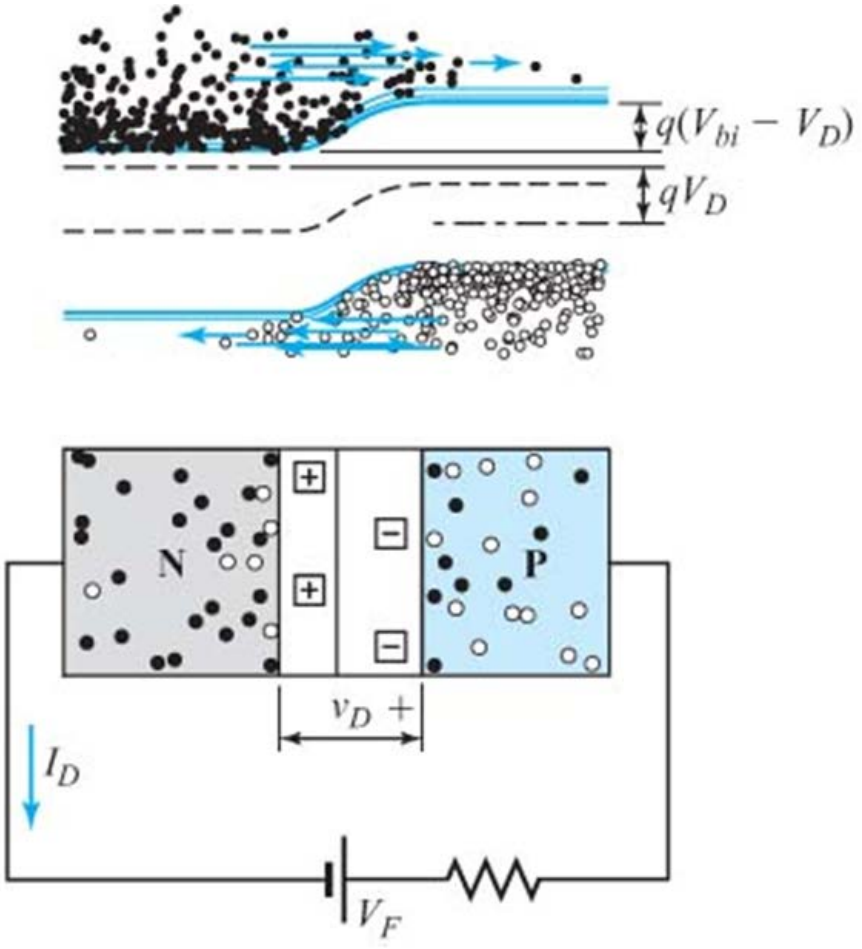


Figure 2.6: Illustration of (a) energy bands and (b) depletion region and immobile charge carriers in p-n junction under forward bias [Ref. 16]

- A positive voltage on the p-side forward biases a pn-junction.
- The separation in bands is reduced by the applied voltage (in an ideal diode).
- A small barrier exists at the junction and many electrons and holes can diffuse across.
- A few electrons and holes can still drift across the other direction, but this is usually negligible. Thus, we get an exponentially increasing current in forward bias.

The diode equation can be written as –

$$I_D = I_S\left(e^{\frac{V_D}{\eta V_t}} - 1\right)$$

2.1.2 Metal – Semiconductor Junction:

A metal – semiconductor junction can be illustrated as follows –

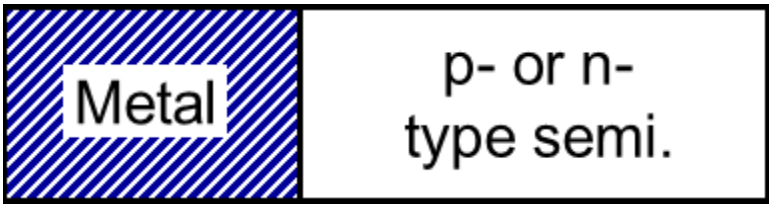


Figure 2.7: Metal – Semiconductor contact [Ref. 17]

Metal – semiconductor contact can be of two types –

- Ohmic contacts:
  - behave like resistors.
  - connect semiconductor materials to the outside world.
- Schottky diodes:
  - pn junctions (rectifying).
  - low “turn-on” voltage, high speed, sometimes used for high-power devices.

Band diagram for a Metal – Semiconductor contact:

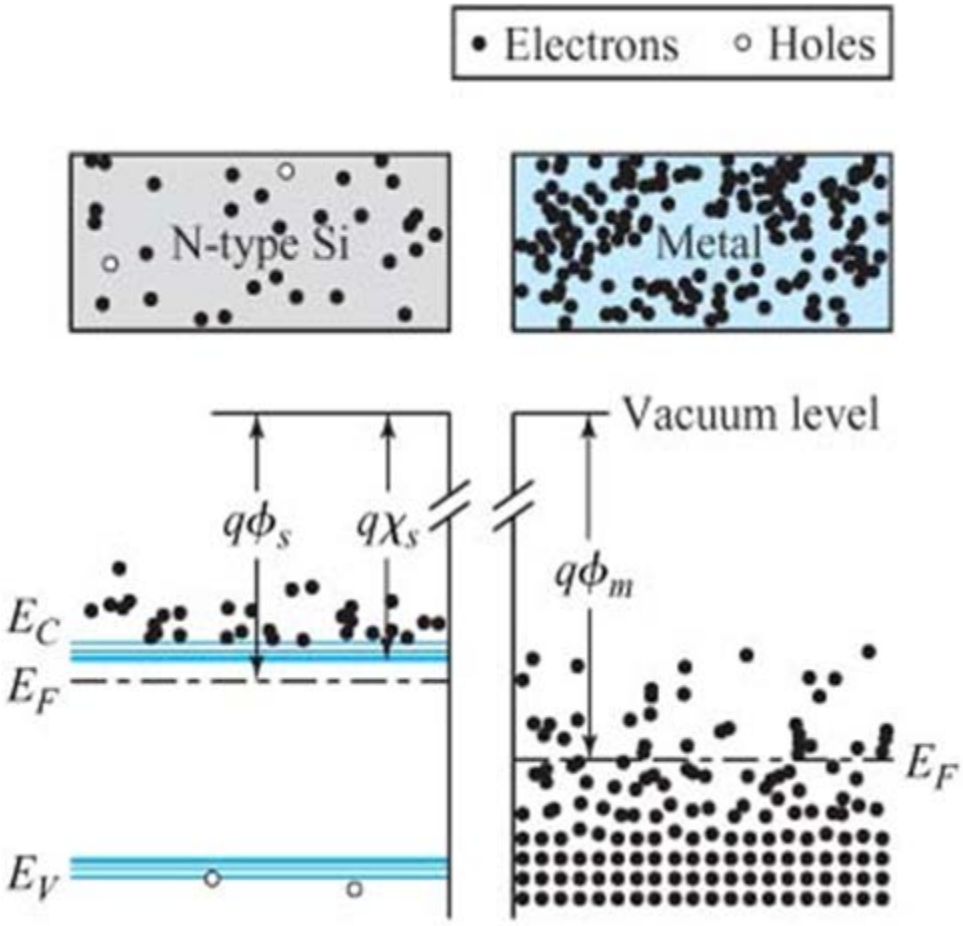


Figure 2.8: Illustration of bands in a metal and a semiconductor [Ref. 16]

- Fermi level, E_{FM}, is positioned inside the conduction band for a metal.
- Almost all states are filled up to $E_{F.}$

Band diagram for Metal – Semiconductor contact:

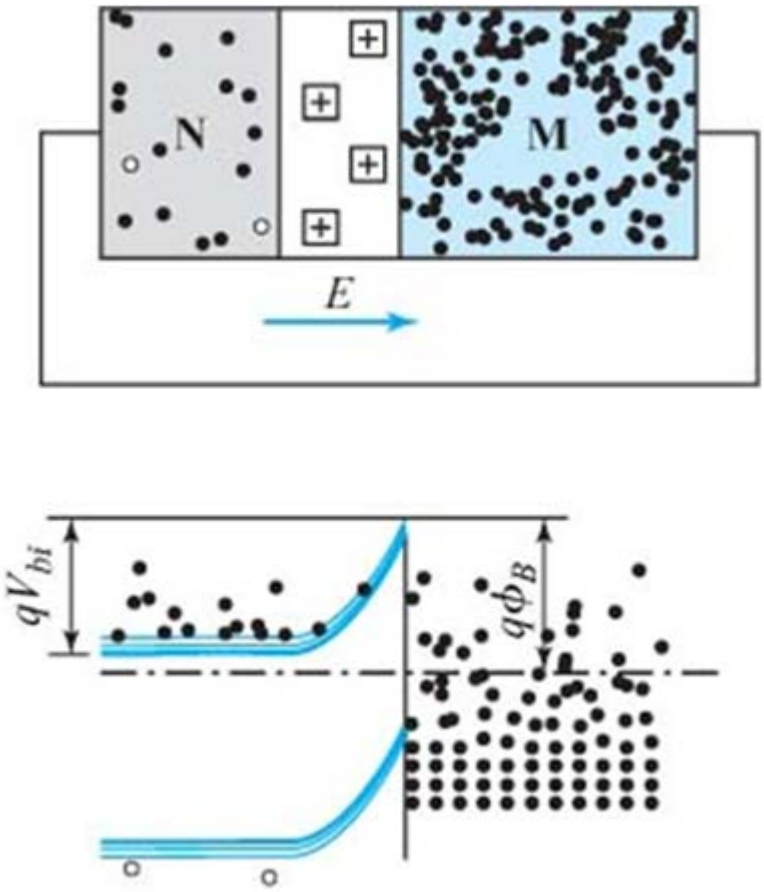


Figure 2.9: Metal – Semiconductor contact formation and energy band changes [Ref. 16]

Energy band offset is given by $q\phi_{\mathrm{B}} = \left(q\phi_m - q\chi_s\right)$

Built-in potential is given by $qV_{bi} = \left(q\phi_m - q\phi_s\right) = q\phi_{ms}$

where ϕ_{ms} is the metal semiconductor work function difference

Schottky diode in Forward Bias:

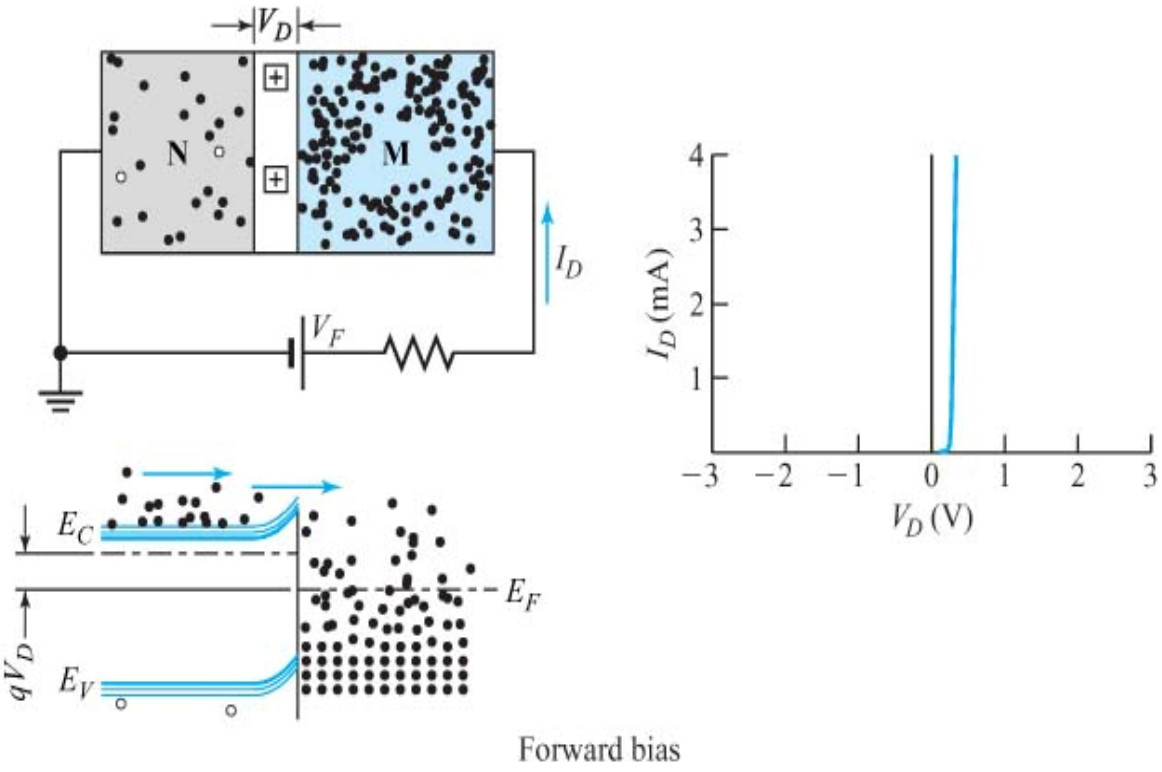


Figure 2.10: Schottky diode in Forward bias with change in energy band structure

[Ref. 16]

- In forward bias the barrier is lowered and electrons move from the semiconductor to the metal.
- This gives an IV characteristic essentially identical to the pn-junction. However, the current mechanism is different.

Schottky diode in Reverse Bias:

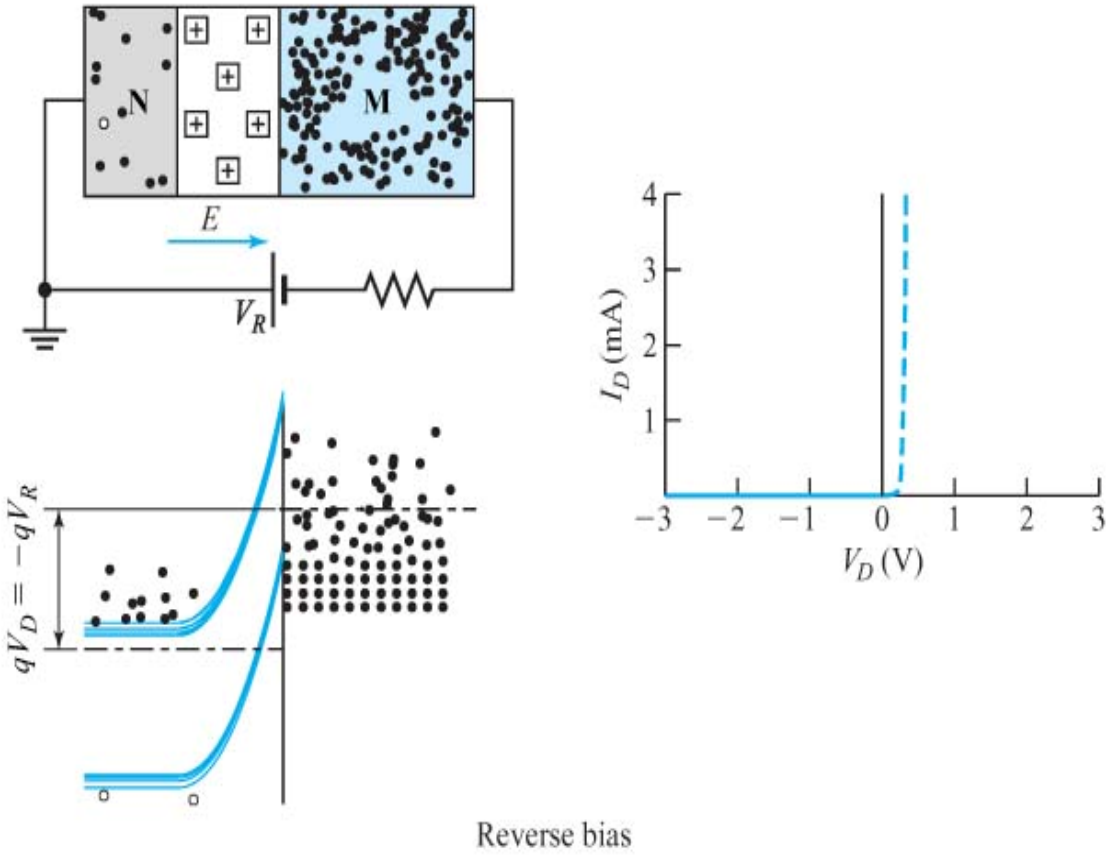


Figure 2.11: Schottky diode in Forward bias with change in energy band structure [Ref. 16]

- In reverse bias the barrier increases and no electrons can move from semiconductor to metal.
- A few electrons move from the metal to the semiconductor and we get a small reverse current.

Ohmic Contacts:

Often we do not want a metal-semiconductor contact to act like a diode. If we need to connect a device to another device, or to the outside world, we need a linear, low-resistance contact. In practice we heavily dope the region immediately adjacent to the contact and rely on tunneling between the semiconductor and the metal. Doping can be performed directly or by depositing the dopant along with the contact material and alloying at elevated temperatures.

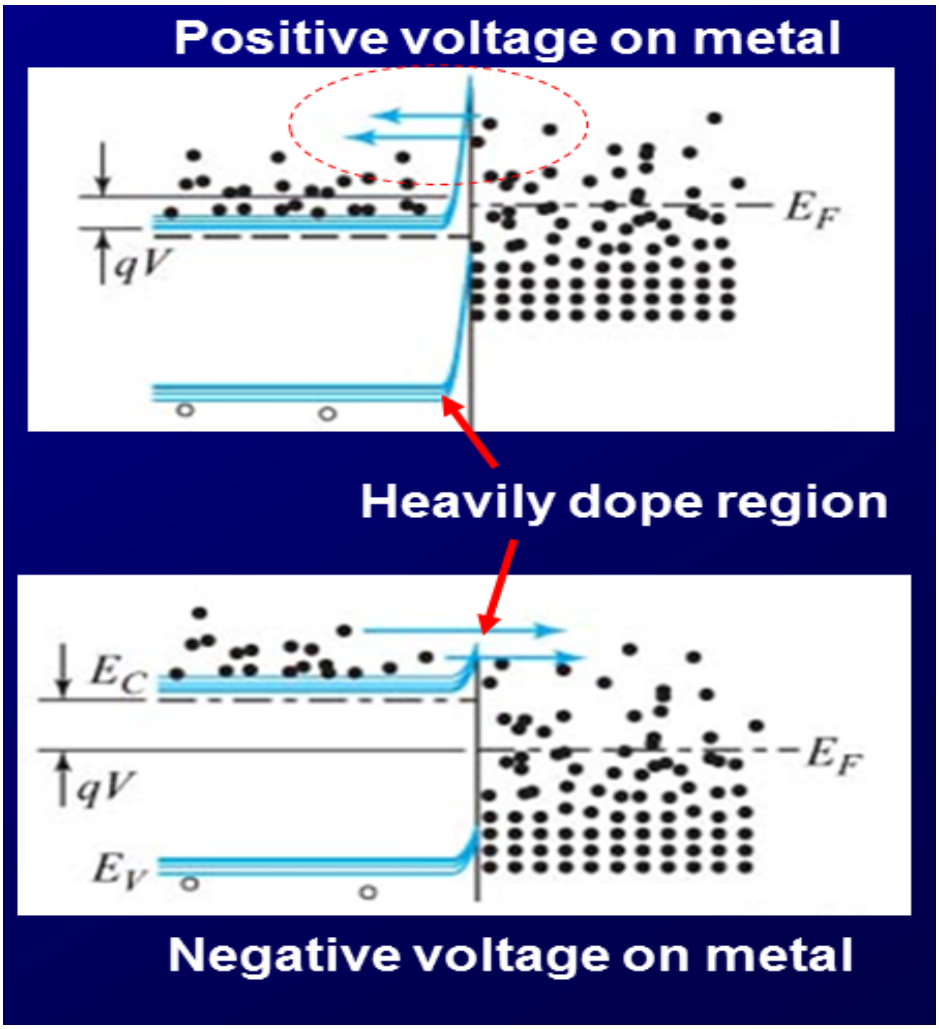


Figure 2.12: Ohmic contacts and band energy diagrams for both positive and negative voltages applied on metal [Ref. 16]

2.2 Device Structures and Principles of Operation

The device structure worked upon for CdS / CIT solar cells is shown below –

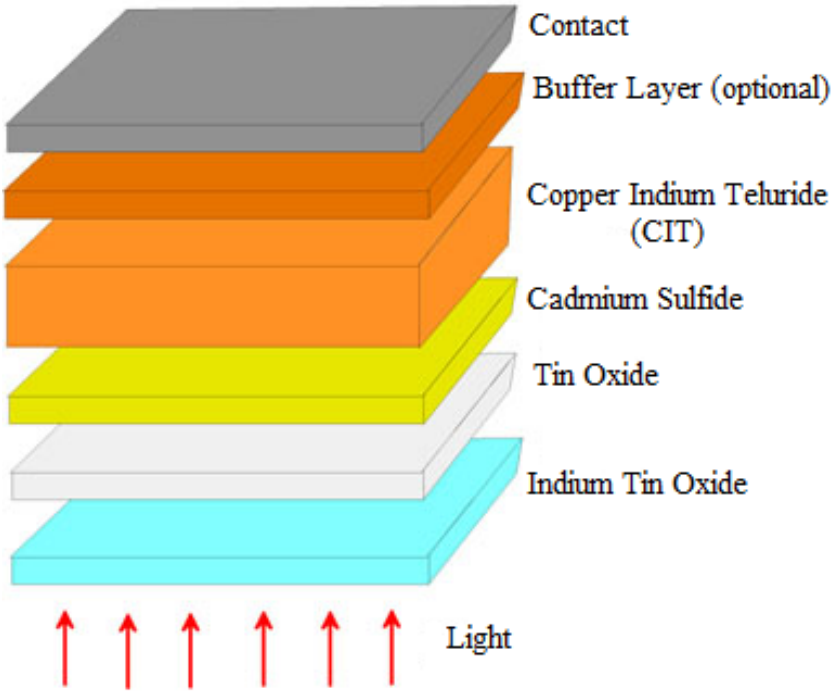


Figure 2.13: Device Structure Illustration CdS / CIT solar cell

ITO/ Tin Oxide interface forms the negative electrode contact. CdS thin films were deposited through chemical bath deposition over the RF sputtered Tin Oxide. CdS films were then annealed and CIT was electrodeposited over the annealed CdS. The samples were re-annealed in order for the CIT to yield better grain size. Finally contacts were made on the CIT films.

The device structure for CdS / CdTe solar cells is shown below –

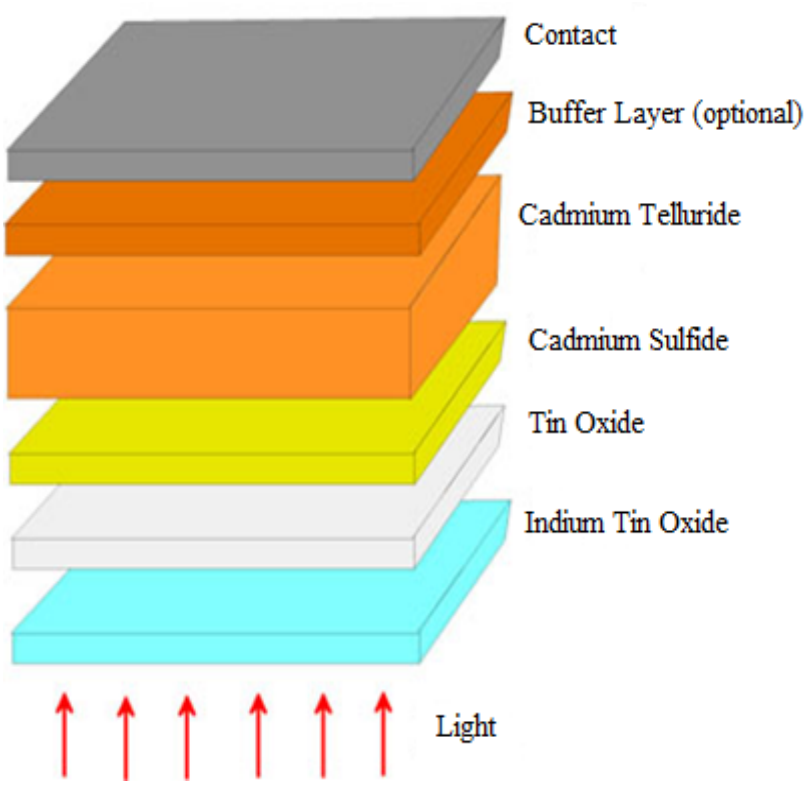


Figure 2.14: Device Structure Illustration CdS / CdTe solar cell

Again ITO/ Tin Oxide interface forms the negative electrode contact. Intrinsic Tin Oxide is deposited on ITO by RF Sputtering. CdS thin films were deposited through chemical bath deposition and also through Thermal Evaporation. CdS films were then subjected to a $CdCl_2$ dip and annealed in inert ambient. CdTe was deposited through Closed Space Sublimation technique. After in-situ annealing and $CdCl_2$ treatment samples were re-annealed. Contacts were made by Graphite and Silver paste after thin Cu sputter and NP etch.

Copper Indium Telluride

Copper Indium Telluride falls in the group of I-III-VI_2 compounds. These compounds are also referred to as the chalcopyrite compounds. They are a group of semiconducting materials with diverse optical, electrical, and structural properties [19-26]. Ternary chalcopyrite compounds appear to be promising candidates for solar-cells applications [31-34], light-emitting diodes, nonlinear optics, and optical frequency conversion applications in solid state based tunable laser systems. These have potentially significant advantages over dye lasers because of their easier operation and the potential for more compact devices. Tunable frequency conversion in the mid-infrared (IR) is based on optical parametric oscillators (OPO's) using pump lasers in the near IR. On the other hand frequency doubling devices also allow one to expand the range of powerful lasers in the far infrared such as the CO_2 lasers to the mid-infrared [27-30].

The chalcopyrite model structure is shown below:

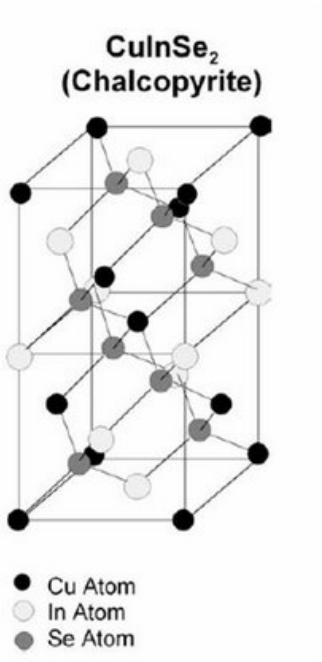


Figure 2.15: Model of Chalcopyrite Crystal Structure [Ref. 18]

At high temperature there is phase transition to a disordered zinc blende-like structure, whereas at high pressures a transition to a NaCl like structure is common, such as also occurs in zincblende compounds [35].

Copper Indium Telluride (CIT) is the least researched compound in the group. Lately it was found that CIT could be used in solar cell applications. Various groups have illustrated the deposition of CIT through vacuum evaporation, microware irradiation, electrodeposition and flash evaporation but the most promising method seems to be via electrodeposition. It has been shown by Dharmadasa and group that CIT could be electrodeposited for thin film applications as in solar cells [10]. The group has not discussed the fabrication of the solar cell but given the conditions and procedures for the electrodeposition of CIT as a thin film. This electrodeposition method for CIT has been followed in this research work with a few changes made in the process.

Cadmium Sulfide

Cadmium Sulfide is a compound that has high potential to act as a window compound for solar cell applications. Its importance has well been established by various groups and various deposition methods. Chemical bath deposition, however, is the method by which a majority of research groups deposit the compound. It is known to be cheap and yielding good films compared to other deposition techniques. The high band-gap of CdS 2.4eV is the main reason for its characteristics as a window material [36]. Most of the light incident on CdS passes through as the band-gap is high and thus its property. In order for the solar cell to work in heterojunction combination it is also necessary that one material forming the junction acts like a mobile charge carrier separator. At the CIT/ CdS junction charge carriers get separated and thus electricity is produced by flow of these carriers through the ITO / Graphite contacts. CdS films of various thicknesses have been made and characterized to yield better results with CIT films.

Cadmium Telluride

Cadmium Telluride is an interesting compound with an ideal direct band-gap of 1.5eV. The effectiveness of CdTe in a solar cell can be measured by the efficiencies it has produced. There is undoubtedly great potential for CdS / CdTe solar cells to become the most researched and most efficient. CdTe layer in CdS / CdTe solar cells is the part where light gets absorbed. Electrons and holes are produced by photon absorption and they contribute towards the current produced. CdTe layer has to be sufficiently thick so that all light gets absorbed [37]. Typical thickness is 5µm.

ITO / SnO_2

ITO glass has been the most widely used substrate for solar cell research in labs. It provides the flexibility to work on and the mechanical strength to the solar cell. ITO glass serves as one of the electrode for the solar cell. ITO is the bottom negative electrode in many solar cell applications. ITO serves as a conductor because of its low sheet resistance usually in the order of 5 - 20 Ω. In order that the compounds deposited do not shunt off with the ITO it is customary to pre-deposit the ITO glass substrates with Tin Oxide (ITO / Tin Oxide mixture) after cleaning and etching the ITO glass surface. This not only reduces the chance of shunts but also reduces the resistance that the charge carriers have to encounter [38]. It is usually seen that RF sputtered Tin Oxide on ITO glass reduces the sheet resistance to just a few ohms. Tin Oxide of various thicknesses has been RF sputtered to obtain optimum performance in the solar cell.

Contacts

As previously discussed, ITO forms the negative electrode contact and the positive electrode contact is usually graphite paste - silver paste mixture or a high work function metal. Commercially available Colloidal Graphite is also often to make contacts.

It is most widely used because of ease of use and being cheap. For metals to be used as contacts they either have to be RF sputtered or deposited with e-beam evaporation techniques. The right choice of contacts is the key to high efficiencies. In this research work Graphite paste, Silver paste and metals have been tested as contacts.

Three-electrode Potentiostat sytem

CIT was electrodeposited using a 3-electrode potentiostat. First, to know the correct deposition potential a cyclic voltagram test is performed during which voltages ranging from a given lower and upper bound were applied at the working electrode with respect to the counter electrode. During this process the compound to be deposited from the electrolyte forms at its deposition potential. Any other compounds being formed within the lower and upper bounds will also be formed. The plot of applied voltage on X-axis and deposition current on Y-axis is drawn. The potential at which there is a loop on the graph is chosen as the deposition voltage. The compounds formed at various such potentials can only be characterized by other methods like XRD and UV-Vis Absorption spectra techniques. Once the deposition potential is known, then a Chrono-Amperometry is performed during which a constant voltage is applied for a specified time period in between the working and counter electrodes. Deposition happens at the working electrode. The function of the reference electrode during the whole process is to maintain a stable potential during the redox reaction.

Chapter 3 Experimental Procedures

The fabrication procedures for the device structures illustrated in section 2.2 are given below -

3.1: Pre-Sputtering of Tin Oxide

Tin Oxide (99.99% pure, RF Sputter target) was deposited on commercially available ITO glass slides. Commercially available ITO glass slides were first cleaned in Methanol, Acetone, Isopropyl Alcohol and Deionized water after cutting them to pieces. Organic contaminants and other particle contaminants were then etched off using Microwave Induced Plasma etch for about 10 – 30 seconds. This ensures removal of any particles sticking onto the slides that would interfere with the normal operation of the solar cell. RF Sputtering of Tin Oxide on ITO glass was carried out in an evacuated chamber. After evacuating the contents of the chamber Argon was introduced at a flow rate of 15 sccm until steady gas pressure was attained in the chamber. Then the Tin Oxide target was subjected to excitation by a RF gun at a power of 75 watts and it produced a uniform film of Tin Oxide on the ITO glass. For uniform deposition on all corners of the slides it is recommended to rotate the slide at a fixed rate while the deposition is taking place. Thickness monitoring was done by a precise calibrated Gold crystal thickness monitor available in the laboratory.

3.2 Deposition of CdS by CBD

As previously mentioned CdS films were produced by chemical bath deposition technique. Chemical bath deposition is known to produce good films. Thickness of CdS films at some places on the glass slide is not uniform if the solution is being stirred during deposition. The solution to deposit CdS is made by mixing 2.025mL of Ammonium Hydroxide, 0.2738g of Cadmium Chloride and 0.27g of Ammonium Chloride in 72.975mL of DI water to form a 75mL solution. This solution is then heated to 70°C which mobilizes the ions in the solution and paves way for the formation of CdS. The RF

Sputtered ITO glass samples are immersed during heating of the solution. This makes sure that there is no temperature gradient which in any way affects the mobility of ions in the solution. Thiourea is then added to the hot solution which initiates the bonding between mobile cadmium ions in the solution and the sulfur ions from the thiourea. It is seen that there is a delay in the appearance of CdS color (orange-yellow) inside the solution due to the fact that thiourea slowly dissosciates into ions. The mobile Cadmium and Sulfur ions form Cadmium Sulfide and deposit on both sides of the suspended glass slide. It is observed that the deposition of a fair amount of CdS usually occurs after 8 minutes. This has also been exemplified in research papers of various other research groups. The usual time taken for the deposition is around 10 - 15 minutes. CdS deposition through CBD is a self-limiting process which has been shown to deposit about 80 – 120 nm of CdS

After deposition of CdS the slides were subjected to ultra-sonication for 2 minutes to remove the CdS that hasn't stuck to the glass slide quite well. This is the first step in attaining uniform thickness of CdS films. Then the backside of the glass was etched off with dilute HCl to remove CdS and the slides were subject to ultra-sonication once again. This made sure that there was no CdS on the backside that would interfere with the properties or working of the solar cells.

3.2.1 Cadmium Chloride dip

It is a custom in CdS thin film fabrication to perform a Cadmium Chloride dip. This process produces good films because it improves the grains of CdS at the boundary on the top. This is usually a wet process although dry $CdCl_2$ annealing treatments have also been studied by other research groups. The wet process is done by mixing 1.125g of 5N $CdCl_2$ powder in 75mL of industrial grade Methanol. The solution is then heated to 59°C until 75% saturation is attained and then the CdS coated glass slides are suspended in the solution for 15 minutes. It is very important that the temperature be kept constant and less than 60°C because Methanol begins to boil at 60°C. The slides

are then immediately rinsed in DI water and dried in dry-N_2 gas to remove any remaining $CdCl_2$ and moisture.

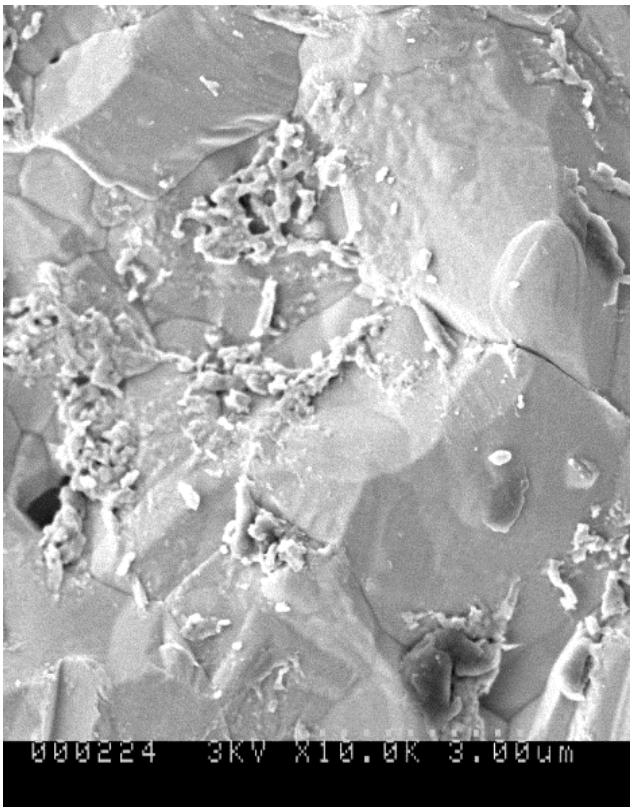


Figure 3.1: SEM image of sample showing residual $CdCl_2$

The clogs on the sample appear due to improper finishing of $CdCl_2$ dip. After $CdCl_2$ dip the samples have to be washed in DI water to remove any residual $CdCl_2$. Streaks of $CdCl_2$ appear as clogs as shown above.

3.2.2 Annealing of CdS films

The CdS films were then subject to a high temperature anneal in an inert Argon ambience at 450C for 30 minutes. Other anneal temperatures have been studied in our investigations of CdS / CdTe solar cells. It is mandatory to have an inert ambient in the annealing chamber prior to starting the heating of the slides. This makes sure that there are no unwanted substances or particles in the chamber that

may interfere with the CdS films. Formation of other compounds was seen in samples which were subject to annealing without prior evacuation of air in the chamber. For example, a CdO peak was observed in the XRD analysis of such samples.

3.3 Electrodeposition of Copper Indium Telluride

Copper Indium Telluride electrodeposition was done through a standard three electrode cell potentiostat. Gamry potentiostat was used for the process with saturated calomel electrode as the reference electrode. Dharmadasa and group have reported electrodeposition of CIT using a similar process but with an Ag/AgCl electrode. Dharmadasa's group has not investigated the use of CIT on solar cells. In this document we also investigate on how to use CIT for solar cell applications.

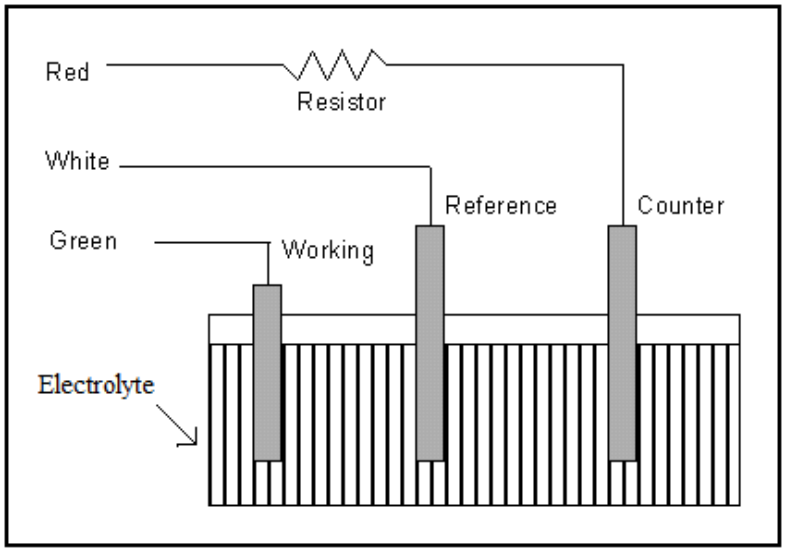


Figure 3.2: Model 3-electrode Potentiostat system [Ref 31]

Cyclic Voltagram of CdS / SnO_2 / ITO films was done in solution used for CIT deposition to find the deposition potential for CIT. The solution for electrodeposition was made from indusrial grade 1mM $CuSO_4$, 10mM $In_2(SO_4)_3$ and 0.5M TeO_2. These

commercially available products were mixed in DI water and stirred using a magnetic stirrer on commercially available magnetic hot plate stirrers. TeO_2 is a substance with low solubility at room temperature. It has been reported by various groups that heating the solution to about 100°C increases the solubility of TeO_2. Solubility of TeO_2 can also be increased by adding weak acids to the solution. Citric acid has been used in this research work. After the solution was stirred for an extended period of time of at least 4 hours, it was used for electrodeposition using the three electrode potentiostat. The pH of the solution was maintained at 1.5.

Typical deposition potentials of CIT were between 750mV and 1100mV as seen in cyclic voltagrams when different concentrations of precursors were used under varying pH conditions. It has been observed that at approximately 800mV and 1000mV, CIT deposition is faster and yielded better results. Many of the samples were deposited at voltages of 800mV because they gave better open circuit voltages than those deposited at 1000mV. Depositions were usually carried out for an hour before subjecting to annealing at temperatures between 350 and 400 C in Argon / atmospheric conditions.

3.4 Thermal Deposition of CdS

CdS for CdTe / CdS solar cells can only be deposited by other methods like Thermal Evaporation. In this method, industrial grade pure CdS powder is taken in a boat placed between two conductors. When current is passed through the conductors the material in the boat begins to vaporize and deposit all above. So, the process is carried in an evacuated bell-jar shaped chamber where the sample is placed above the boat at a certain height depending on size of the chamber, placement of thickness monitor and other factors. To evacuate the chamber a powerful two-stage rotary pump is used to create a vacuum in the range of micro Torr.

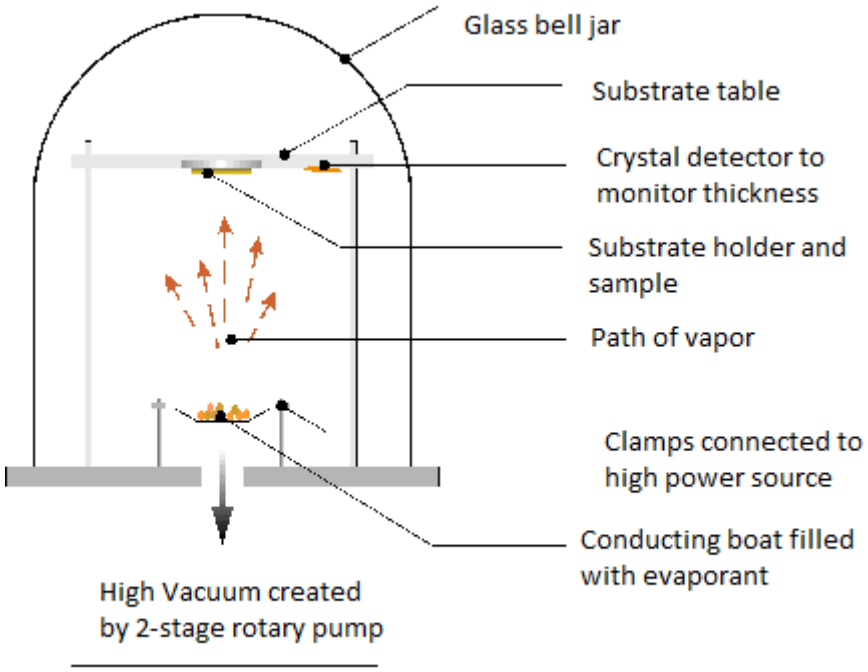


Figure 3.3: Model of Thermal Evaporator

3.5 CdTe deposition by CSS

CdTe deposition by Closed Space Sublimation method is very well known and has yielded high efficiencies. This method employs a quartz tube from which gas can be evacuated using a rotary pump. There are inlets on the quartz tube for the entry of Argon or (Helium + Oxygen) or (Argon + Oxygen) gas mixtures. The sample is placed inside a graphite block above CdTe powder or a prior CdTe-deposited metal film that can withstand high temperatures and can be used as a source of CdTe. Deposition happens after sublimation of CdTe starts from the source. CdTe sublimation occurs at 460°C. Deposition of CdTe from the source occurs if the source is at a higher temperature than the sample, which is referred to as substrate during the CSS. After reaching the desired temperatures CdTe starts to sublime from the source and deposit on the substrate. Deposition in CSS can be controlled by a number of parameters including source and substrate temperatures and gas ambient inside the quartz tube.

After depositing the required thickness of CdTe the temperature is brought down to 400°C and the substrate undergoes in-situ annealing for 10 minutes. Then the tube is allowed to cool down before removing the substrate and source.

3.5.1 Annealing of CdTe films

After removing the substrate from the CSS chamber, it is subjected to a $CdCl_2$ treatment and annealed at 400°C in an annealing furnace for 30 minutes in an inert ambient. Annealing of CdTe in other gas ambients at various pressures are being studied by other members of Dr.Vijay Singh's group.

3.5.2 NP etch of CdTe films

NP etch is an acid dip used mainly for CdS / CdTe solar cells. Formation of a low-resistance contact to CdTe is essential for commercialization of CdTe based photovoltaic devices. Various methods have been studied by other groups for surface pretreatment before contact formation like Bromine in Methanol solution, Potassium Dichromate – Sulfuric acid mixture and Nitric Phosphoric (NP) acid mixtures. NP etch process has been used for this research. 0.176mL of Nitric acid and 14.164mL of Phosphoric acid is mixed with 5.66mL of DI water. CdTe deposited samples are then immersed into this solution one at a time and removed once bubbles are seen emerging from the solution. The bubble formation is an indication that the surface has been oxidized and ready to be used for contact formation. If samples have been left in the acid after bubble formation they got over-etched forming deep trenches at the grain boundaries. Typical dip time is between 5 – 30 seconds. The effects of NP etch over open circuit voltages on CdS / CdTe solar cells are discussed in the results section.

3.6 Contacts

Contacts were made on the top of electrodeposited CIT films using graphite paste, silver paste or high work function metals. It is seen that high work function metals gave better efficiencies than others due to increased carrier collection. Graphite paste is also seen as a cheap, viable option. Contacts made using Graphite paste made it necessary that the sample dry first before testing or usage whereas high work function metals that were deposited using RF sputter or electron beam evaporation could be used immediately for testing. RF sputtered Nickel has been used for CdS / CIT solar cell.

However for CdS / CdTe solar cells after the NP etch, a thin Copper layer needs to be sputtered to increase the surface conductivity of CdTe. Typically 5nm of Copper is sputtered using a RF Sputter process as discussed in the pre-sputtering of Tin Oxide section. Graphite paste is then applied through a mask and allowed to dry before applying a small amount of Silver paste over the Graphite paste which is the final step in the fabrication process for CdS / CdTe solar cells.

Chapter 4 Characterization and Analysis

X-ray Diffraction pattern data was taken using a Bruker-AXS D8 DISCOVER Diffractometer. UV-Vis Absorption data was taken using Cary 50 Probe UV-Visible Spectrophotometer.

4.1 CdS / CIT solar cell: Characterization for CdS and CIT were done separately and as a junction using XRD, UV-Vis Absorption spectra and open circuit voltage test techniques. Samples have been made with deposition potential obtained from Cyclic Voltagram and under different annealing conditions.

XRD pattern for chemical bath deposited CdS is shown below -

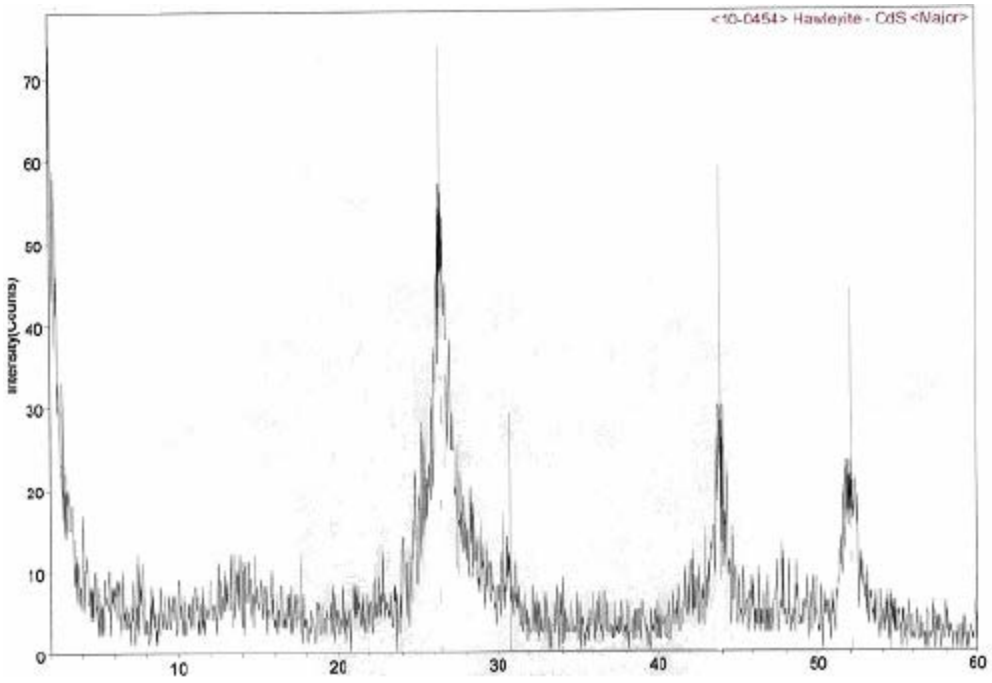


Figure 4.1: XRD pattern of CdS deposited by CBD

From the XRD pattern peaks at 27°, 44° and 52° can be seen which correspond to planes (1 1 1) , (2 2 0) and (3 1 1) respectively. XRD pattern indicates a cubic phase of CdS. This has been confirmed with theoretical values.

UV-Vis Absorption data for chemical bath deposited CdS over ITO is shown below -

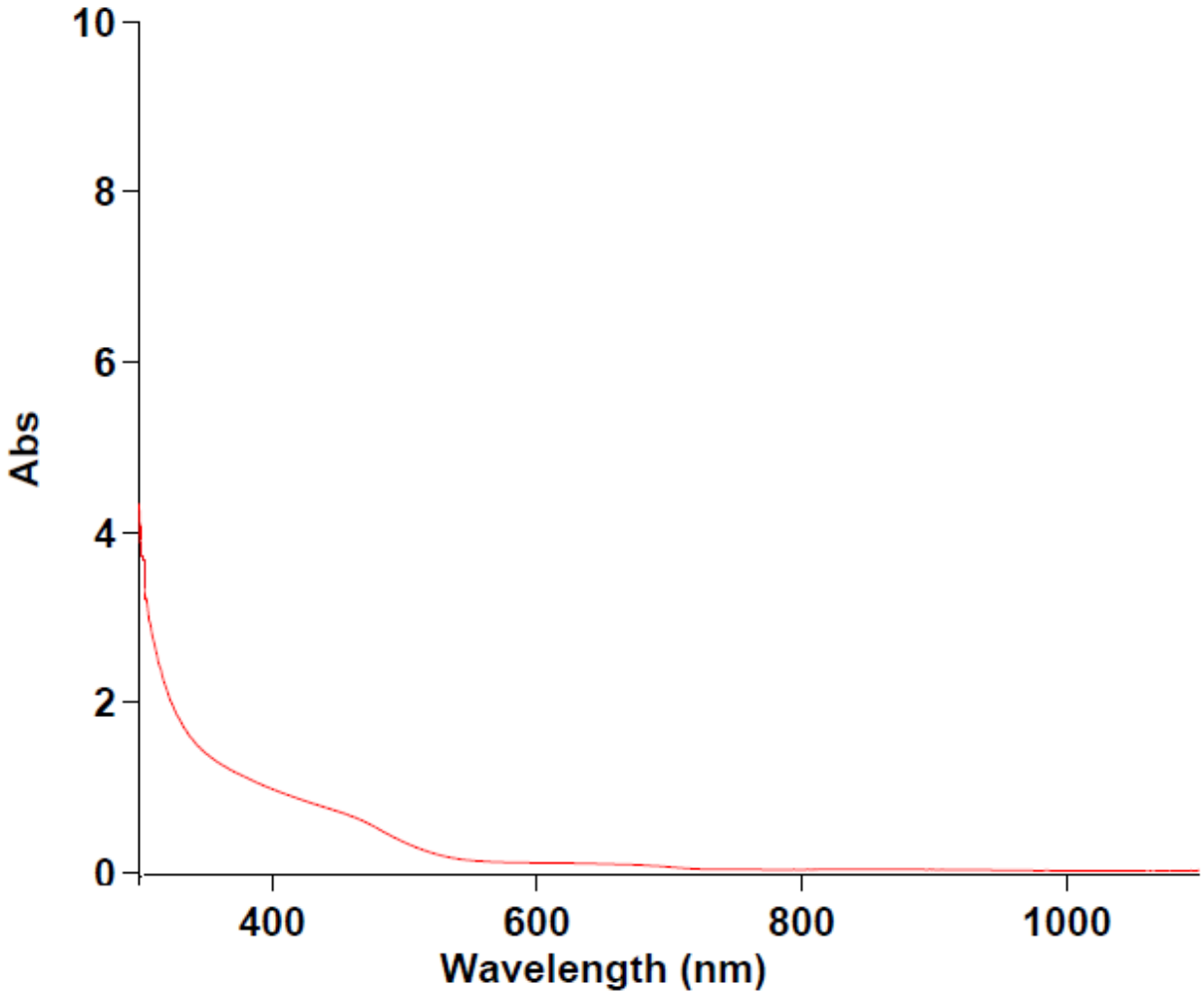


Figure 4.2: UV-Vis absorption for CBD - CdS

The absorption curve above indicates that the CdS had been deposited and confirms it. This is because it has been verified from various other sources that chemical bath deposited CdS shows a kink at 515 nm. The band-gap for CdS is 2.4eV which corresponds to 515nm in the wavelength spectra.

XRD pattern for electrodeposited CIT deposited over ITO is shown below -

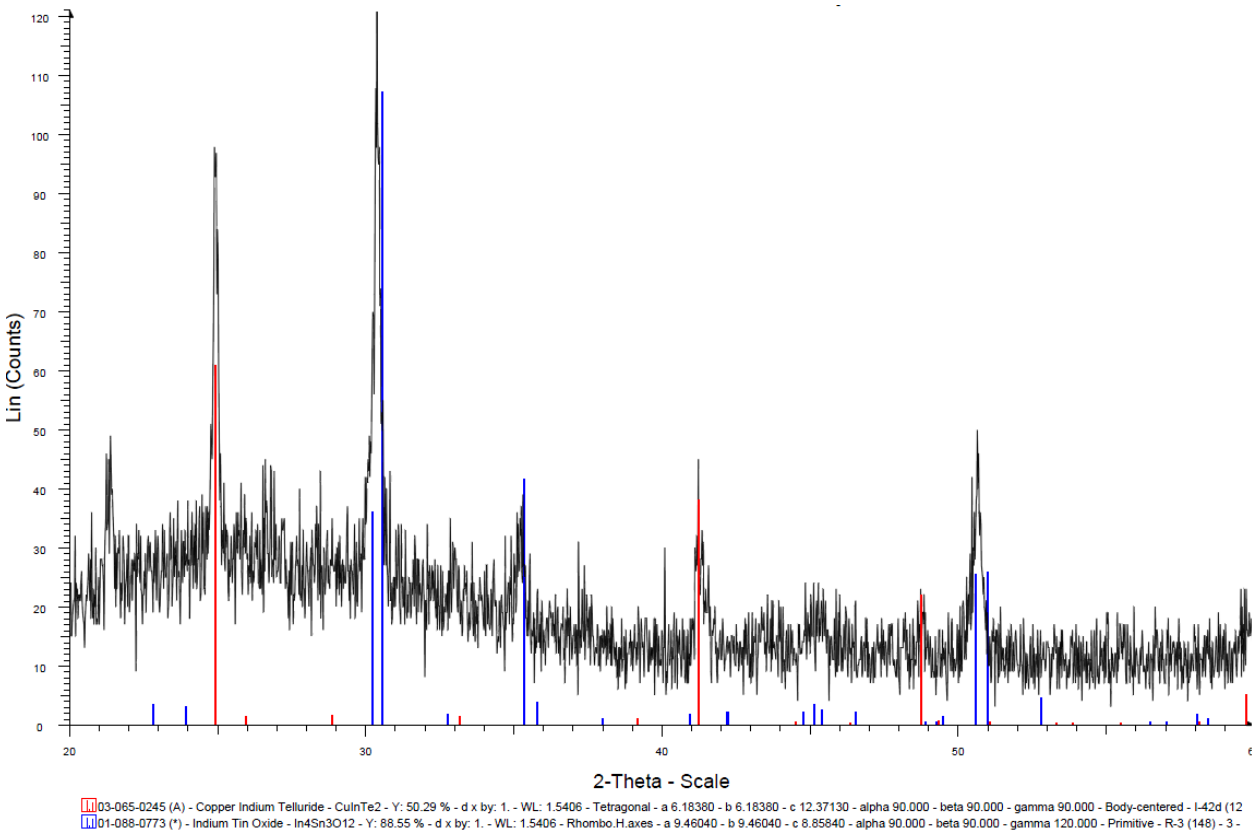


Figure 4.3: XRD data on electrodeposited CIT

From the XRD pattern above, it can be seen that the deposited material is CIT. As per JCPDS data CIT should have peaks at 2θ= 25°, 41° and 49° [43]. The peak at 30.5 is that of ITO / Tin Oxide. ITO being more crystalline then Tin Oxide has a high intensity peak compared to CIT.

UV-Vis Absorption data for electrodeposited CIT deposited over ITO is shown below -

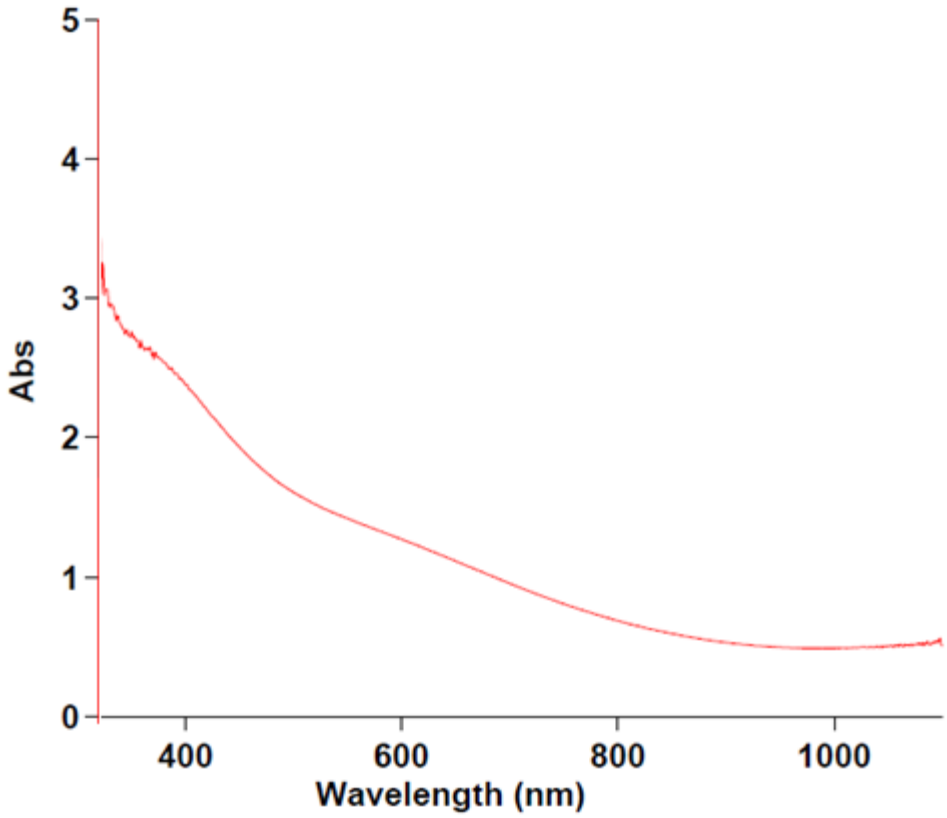


Figure 4.4: UV-Vis absorption for electrodeposited CIT

Figure 4.4 shows the absorption of a CIT film in arbitrary units in the wavelength range of 300nm – 1100nm. The energy band gap of CIT is in the range of 0.95eV to 1.1eV range which corresponds to 1127nm – 1305nm in the terms of wavelength. This range of wavelengths cannot be seen over the absorption meter used.

Figures 4.5 and 4.6 show the cyclic voltagram curves of CIT deposited over plain ITO and on CdS deposited ITO glass slides. Formation of a loop in the cyclic voltagram indicates the deposition of a compound and the voltage value where the oxidation and reduction half cycles cut is the electrodeposition voltage for that compound. For CIT deposition in both cases, the deposition potential is around 784mV.

Cyclic Voltagram of CIT electrodeposited on ITO is shown below -

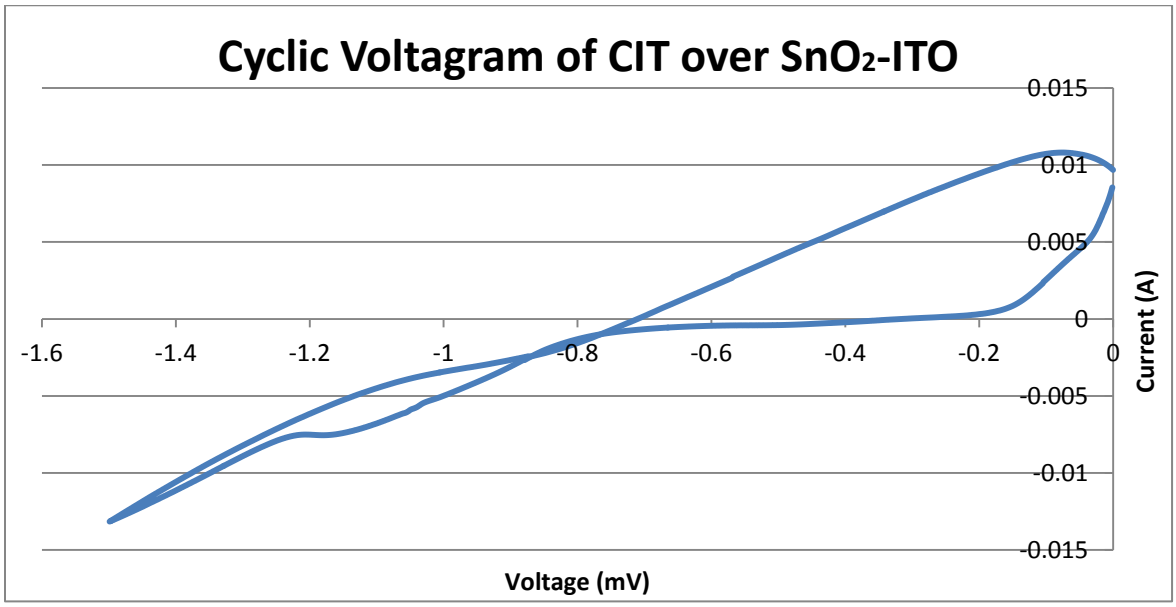


Figure 4.5: Cyclic Voltagram of electrodeposited CIT over SnO_2-ITO

Cyclic Voltagram of CIT on CdS deposited ITO is shown below –

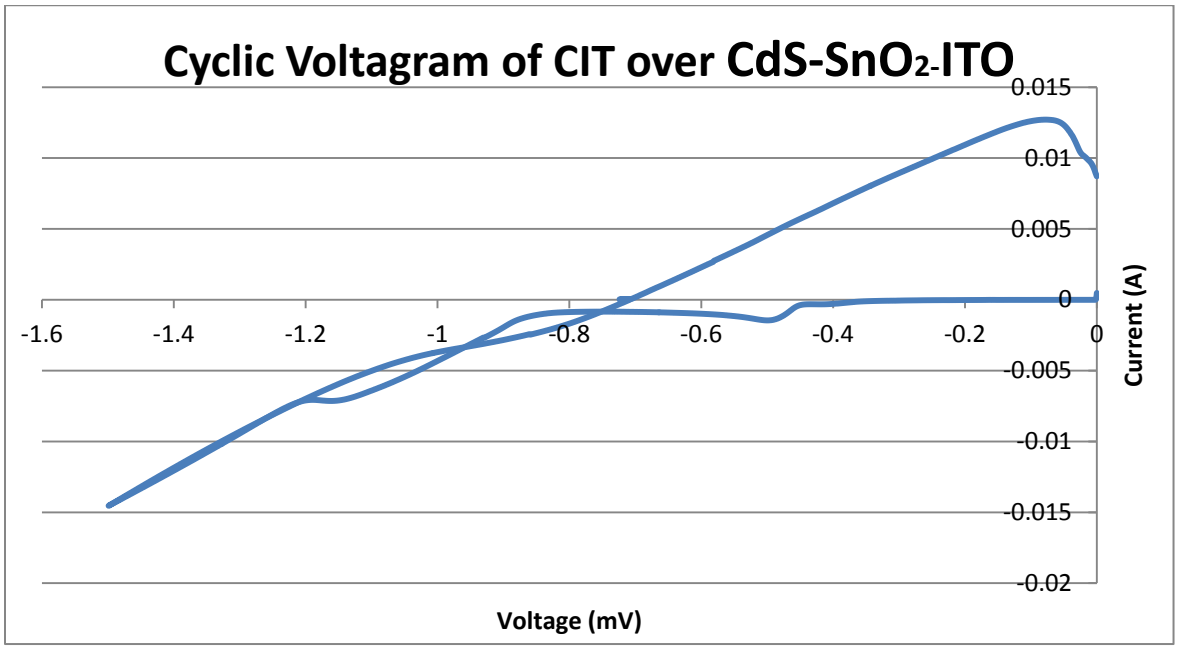


Figure 4.6: Cyclic Voltagram of electrodeposited CIT over CdS-SnO_2-ITO

4.2 CdS / CdTe solar cell:

The XRD and UV-Vis absorption data for CdS in CdS / CdTe solar cells that were used to investigate the effect of anneal temperatures on open circuit voltages is the same as those shown for the CdS / CIT solar cell in section 4.1. CdS was deposited using the same process of chemical bath deposition.

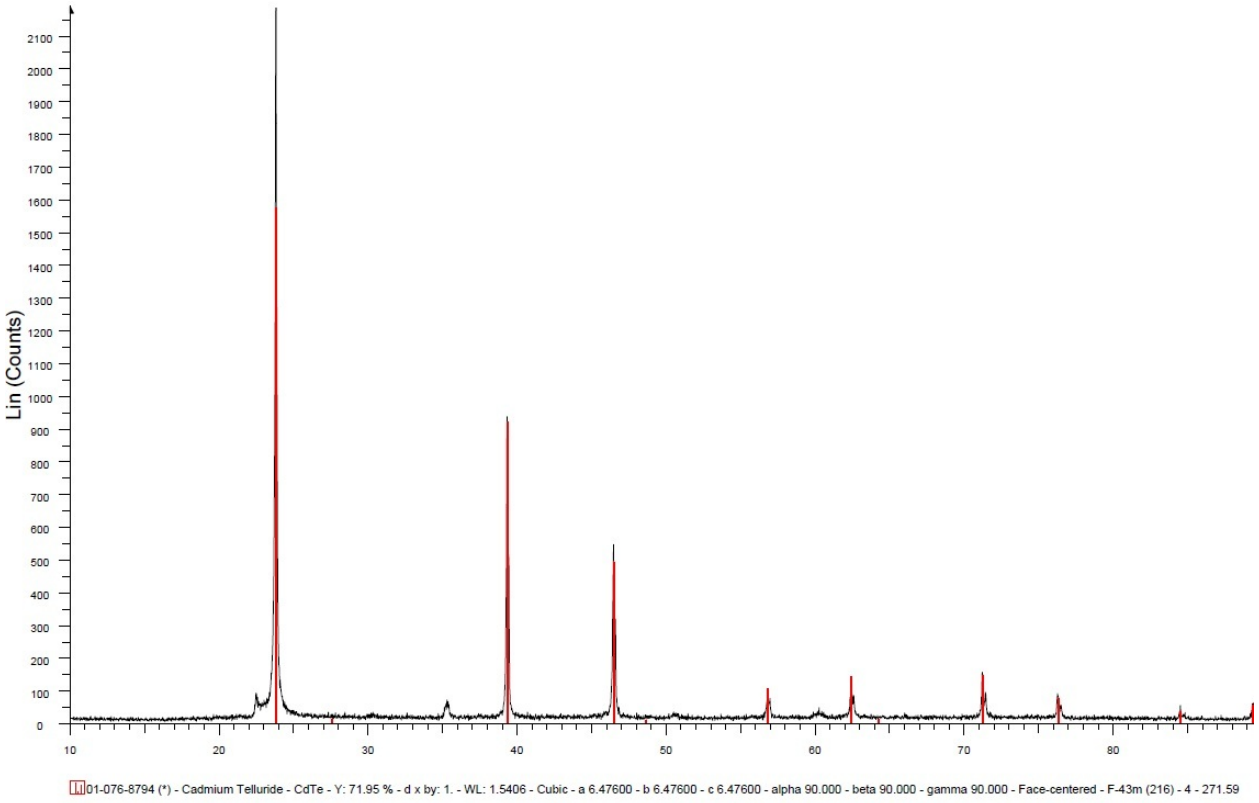


Figure 4.7: XRD pattern of CdTe

The peaks at approximately 24°, 39°, 46°, 62° and 71° correspond to cubic Cadmium Telluride. Thus from Fig. 4.7 it can be inferred that the compound is indeed Cadmium Telluride.

UV-Vis absorption measurements of CdTe film showed an absorption edge around 823nm. The edge in absorption spectra indicates high crystallinity of compounds whereas a kink indicates less crystalline structure. CdS produced by CBD is cubic but less crystalline whereas CdTe deposited by CSS has a high degree of crystallinity. The edge of 823nm for CdTe samples translated to 1.5eV in terms of band-gap which is its theoretical value.

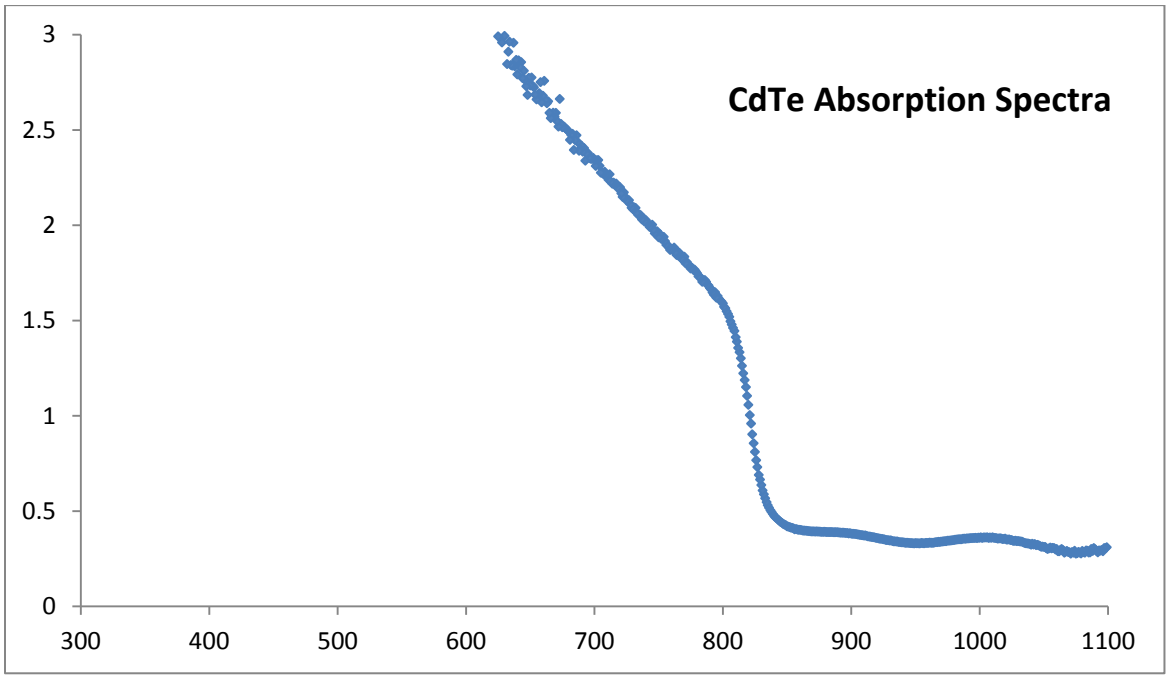
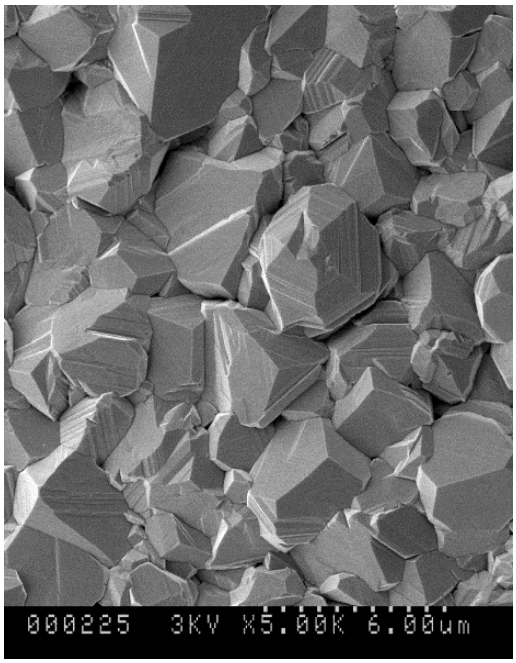
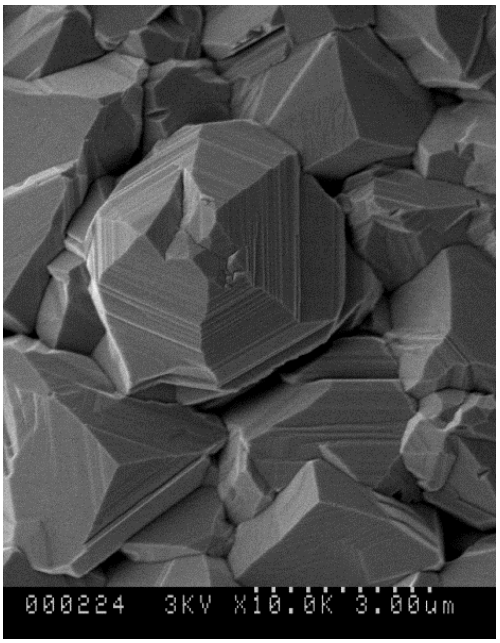


Figure 4.8: UV-Vis absorption for CdTe deposited by CSS

SEM images are taken for CdTe films deposited in vacuum using the CSS technique at 100 mTorr vacuum ($\Delta T=100^0C$). Figure 4.9 shows the images at different magnifications using Hitachi S-900 instrument available in our laboratory. It can be verified that the film being deposited is highly crystalline and has a cubic structure.



(a)



(b)

Figure 4.9: SEM images for CdTe deposited by CSS at magnifications of (a) 5K and (b) 10K

Chapter 5 Results and Discussion

5.1 CdS / CIT solar cell:

$CdCl_2$ dip for CdS / CIT solar cell:

CdS films of CdS /CIT solar cell were subject to the regular $CdCl_2$ treatment as discussed in section 3.2.1. Samples that were subject to $CdCl_2$ treatment have not shown much performance degradation over those that were not subject to the treatment. Performance degradation was measured in terms of open circuit voltage.

CIT electroeposition:

It was seen during electrodeposition that CIT sticks to the CdS / ITO substrate if the deposition time was less than 1.5hrs. For samples on which multi-hour deposition was done, the CIT film peeled off during deposition and remained as a sheet in the electrolyte.

Formation of CIT:

As discussed in section 3.3, $CuSO_4$, $In_2(SO4)_3$ and TeO_2 have been used for electrodeposition. It is important to know the kinetics of the reactions that lead to the formation of CIT. At -600mV, Te reduces to form H_2Te

$$Te + 2H^+ + 2e^- = H_2Te$$

In addition to the reaction above, other reactions taking place at anode are –

$$2H_2Te + HTeO_2^+ = 3Te + 2H_2O + H^+ \quad (1)$$

$$2H_2Te + Cu^{2+} + In^{3+} + 5e^- = CuInTe_2 + 2H_2 \quad (2)$$

$$2H_2Te + 2Cu^{2+} + 4e^- = 2Cu_xTe + 2H_2 \quad (3)$$

The main reaction taking place at cathode is

$$2Cu^{2+} + 2In^{3+} + 4HTeO_2^{+} + 14e^{-} = 2CuInTe_2 + 2H_2O + 3O_2 \quad (4)$$

The competition to consume H_2Te by reactions 1 and 2 could lead to precipitation of elemental Te or CIT at the cathode. If such precipitation occurs stoichiometric $CuInTe_2$ formation gets harder.

CIT annealing:

CIT annealing was done at temperatures of 350,400 and 450°C. It was however noted that at 450°C annealing causes the film to lose a small portion of the electrodeposited film. Effect of annealing was also compared between Argon and Oxygen gas ambients. It was seen that the annealing in Oxygen led to formation of TeO_2 on the electrodeposited film. This was confirmed by XRD. Also the change was drastic if anneal time was more than 10 minutes. More insight is needed into the solubility of TeO_2 in the electrolyte solution at this point. Thus, annealing in Argon was performed at 400°C for 30minutes which effectively strengthened the peaks in X-ray data from the film by atleast 100units.

Open Circuit Voltages for CdS / CIT solar cells:

Table 5.1 below shows the variation of open circuit voltages for different annealing temperatures used for CIT annealing for two deposition durations namely 30 minutes and 60 minutes. For these samples CdS was annealed at 400°C for 30 minutes to maintain coherence in the experiment. From Table 5.1 it can be inferred that the best annealing temperature for CIT is 400°C and better open circuit voltages are seen on those samples that had undergone CIT electrodeposition for 60 minutes. CIT electrodeposition at 30 minutes and 60 minutes can be compared and said that at 60

minutes there is more material that gets deposited on the sample than in the case of 30 minutes thus covering all of the CdS without leaving pin holes or other defects.

Table 5.1: Open circuit voltages for CdS / CIT solar cells at different anneal temperatures and deposition times

Deposition Time	Anneal Temperatures for CIT		
	350°C	400°C	450°C
30 minutes	57.4mV	121.6mV	100.2mV
60 minutes	98mV	183mV	167mV

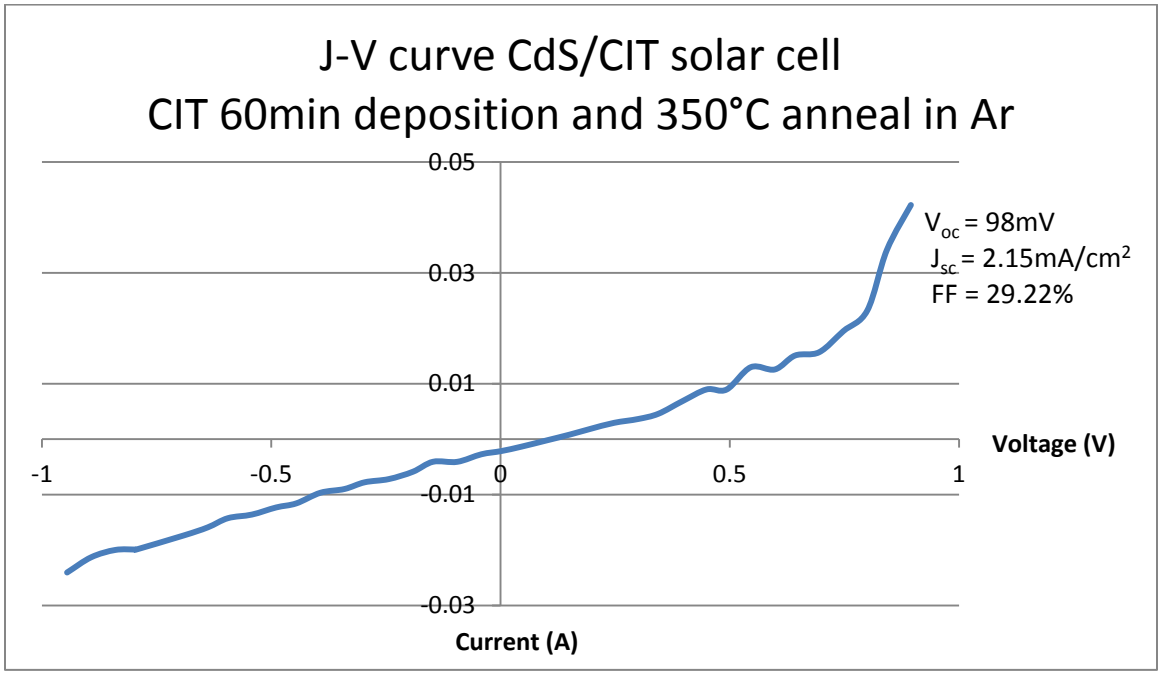


Figure 5.1: J-V curve for CdS/CIT solar cell CIT 60min deposition and 350°C anneal in Ar

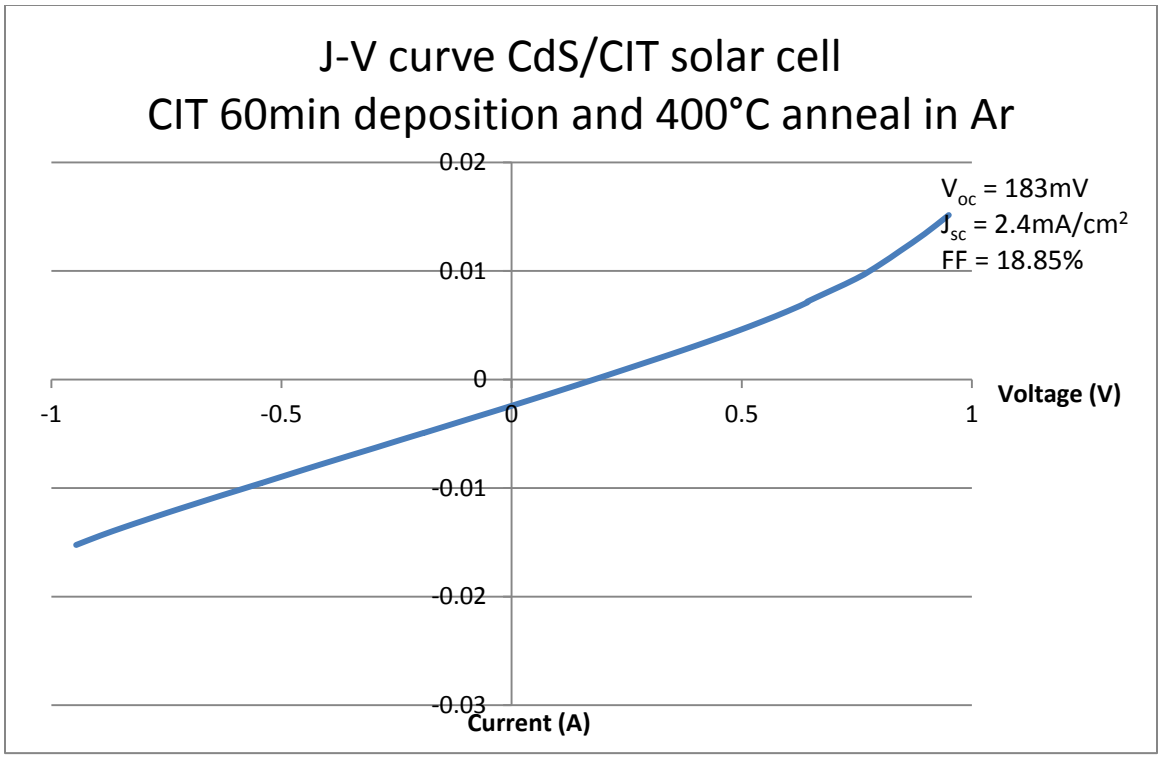


Figure 5.2: J-V curve for CdS/CIT solar cell CIT 60min deposition and 400°C anneal in Ar

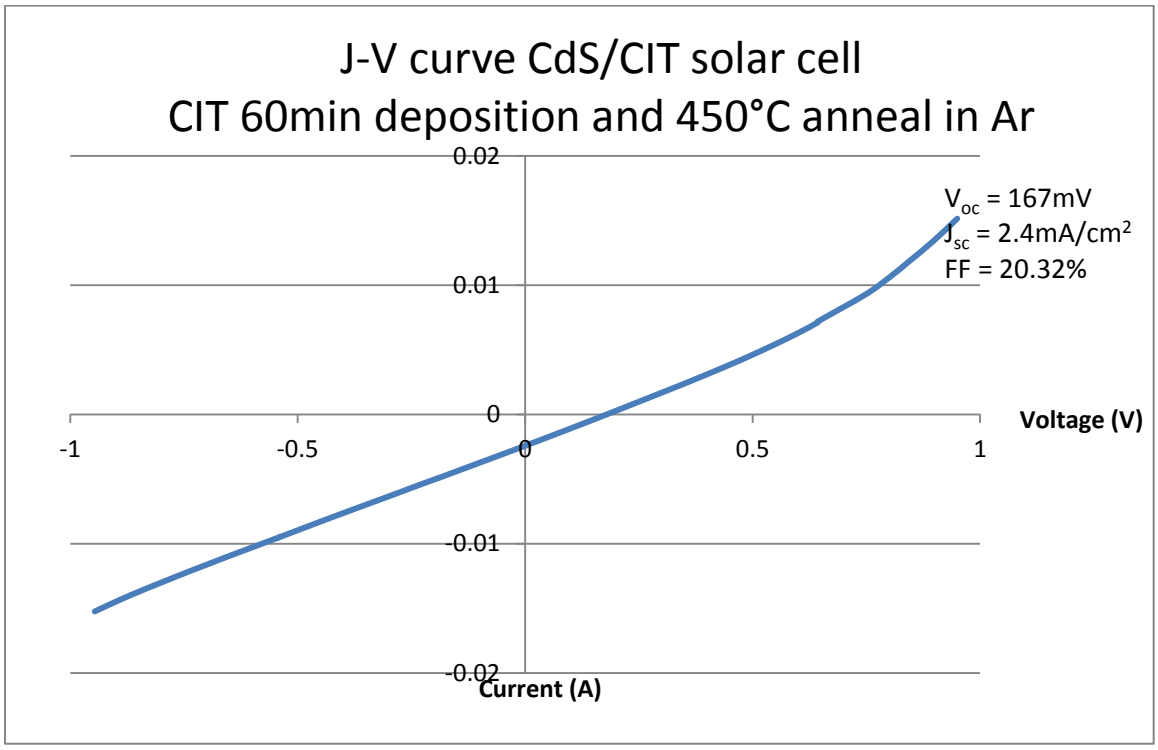


Figure 5.3: J-V curve for CdS/CIT solar cell CIT 60min deposition and 450°C anneal in Ar

Table 5.2: Open circuit voltages for CdS /CIT solar cells for different anneal ambients and deposition times

Deposition Time	Anneal Ambients for CIT	
	Ar only @ 400°C	O_2 only@ 400°C
30 minutes	121.6mV	90.9mV
60 minutes	183mV	110mV

Table 5.2 shows the variation of open circuit voltages for Ar and O_2 annealing ambients at 400°C for 30 and 60 minutes deposition times. The benefit of higher deposition time is explained in the paragraph above. Low open circuit voltages were observed when CIT was annealed in O_2 because of the formation of oxides of tellurium thus disturbing the stoichiometry of the compound $CuInTe_2$. Loss of the compound starts at the surface and goes deeper. Ample presence of O_2 and lack of protection from the top layer makes the sample prone to further deterioration.

These low open circuit voltages could be attributed to the fact that recombination centers at the CdS / CIT interface are too high in number. More insight is needed into the working of the junction at this time. Absorption of CdS has been characterized and studied by other groups. From the UV-Vis absorption for CdS one can deduce that the band-gap of 2.4eV. That means all light photons having energy more than 2.4eV are absorbed in the CdS thin film. Photons with energy less than 2.4eV pass through the CdS film. CIT has a band-gap of 0.95eV – 1.1eV. This means that the only available photons that could be absorbed are those with energies between 1.1eV and 2.4eV (1127nm – 517 nm in terms of wavelengths which is approximately half of the visible light spectrum). If doping levels, recombination centers & states and the CdS /CIT junction in particular have been characterized, it would lead to development of high

efficiencies for the CdS / $CuInTe_2$ solar cells. At this juncture a need of more precise monitoring and equipment is necessary for high efficiency CdS / CIT solar cells. But this research has shown that a junction could be formed with these materials, which has never been done to date.

5.2 CdS / CdTe solar cell:

5.2.1 Effect of CdS annealing temperatures on Open Circuit voltages:

The effect of CdS annealing temperatures on open circuit voltages of CdS / CdTe solar cells has been studied on Chemical bath deposited CdS and CSS deposited CdTe samples. The deposition and fabrication processes have been discussed in section3. Data for this experiment was obtained from samples deposited using a standard set of conditions listed below –

1) Clean all ITO samples as discussed in section 3.1.
2) Expose the cleaned samples to a microwave induced plasma etch for 30 seconds at RF power rating of 60% and Oxygen gas flow rate at 4 sccm.
3) RF Sputtering of intrinsic Tin Oxide performed at 75 W power and Argon gas flow rate of 15 sccm in an evacuated chamber to deposit 100nm of the material.
4) Chemical bath deposition as discussed in section 3.2.
5) $CdCl_2$ treatment as illustrated in section 3.2.1 followed by annealing at temperatures of 350, 400, 450 and 500°C.
6) CSS was performed as illustrated in section 3.5 to deposit CdTe of desired thickness after annealing of CdS films.
7) $CdCl_2$ treatment on CdTe film as discussed in section 3.2.1.
8) NP wet acid etch is performed by the method given in section 3.5.2.
9) Thin Cu sputter of 5nm thickness to protect CdTe film from exposure to moisture.

10) Contacts with graphite paste and silver paint.

It is observed that CdS anneal temperature has a major effect on the open circuit voltages which are defined by the junction between CdS and CdTe. The table below gives insight into the change anneal temperature has on the open circuit voltage.

Table 5.3 summarizes the measured open circuit voltages for different annealing temperatures of CdS. The temperatures chosen are close to those that other researchers have been using. It can be seen that for 400°C and 450°C the voltages are higher. This is because CdS deposited through CBD crystallizes better at those temperatures. While at 500°C, there is loss of CdS at those places where the thickness was less when CBD was done. This would leave pin holes and if they're big enough for CdTe grains to touch the Tin Oxide coated ITO, there would be a loss of open circuit voltage.

Table 5.3: Open circuit voltages for CdS / CdTe solar cells as a function of anneal temperatures of CdS

Anneal Temperature of CBD-CdS	Open Circuit Voltage (mV)
350°C	230
400°C	415
450°C	505
500°C	210

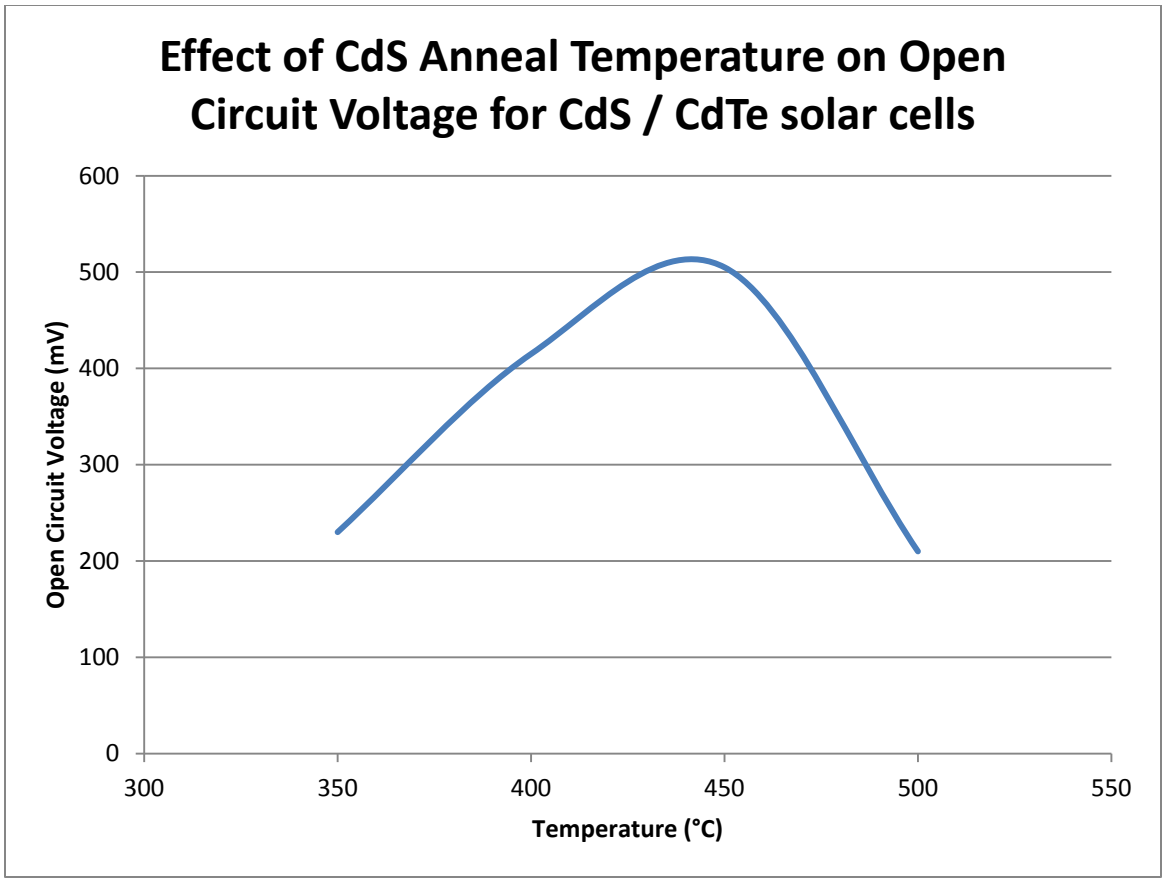


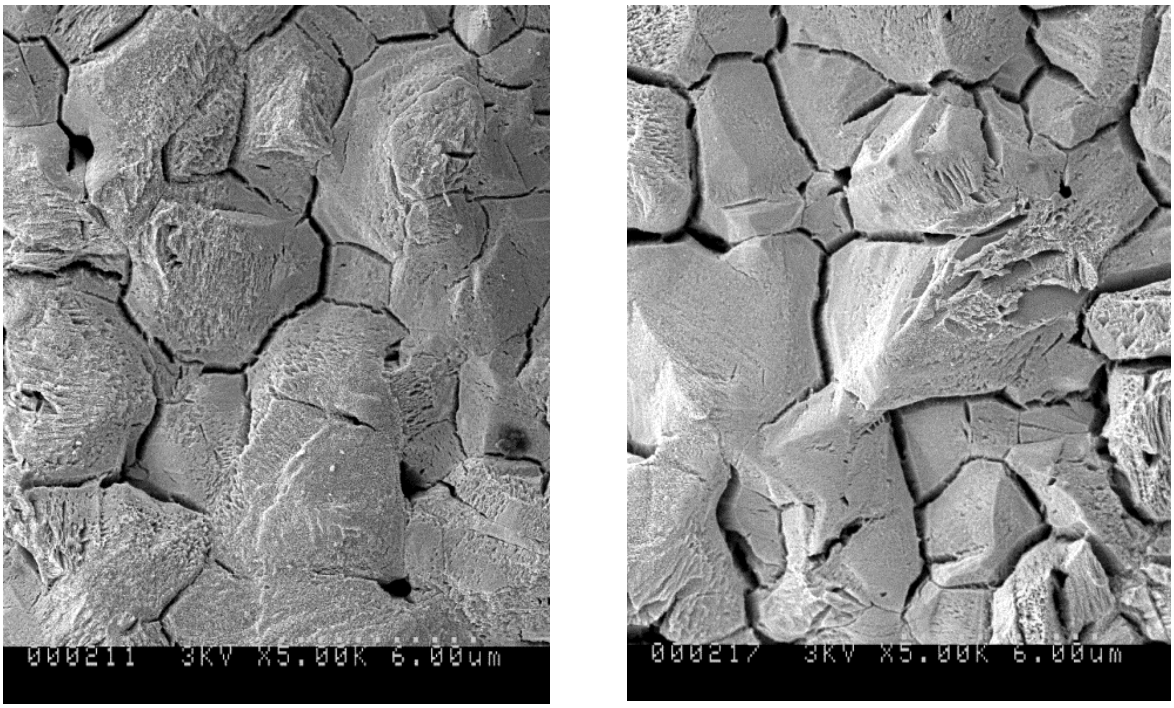
Figure 5.4: Open circuit voltages as a function of annealing temperatures for CdS / CdTe solar cells

5.2.2 Effect of NP etch on Open Circuit voltage of CdS / CdTe solar cells

NP etch process as described in section 3.5.2 is vital for the activation of CdTe film after CSS deposition. If the film is under etched the CdTe film remains unactivated resulting in low open circuit voltages. And if the film is over etched deep trenches are formed between CdTe grain boundaries resulting in drastic reduction in open circuit voltages. It has been studied by various groups that formation of bubbles during NP etch indicates when the etch process should be stopped.

The acid etch helps make the surface Te-rich that makes a better ohmic contact. Otherwise a diode is formed at the contact – CdTe interface.

The images below show those samples that underwent 15 and 30 seconds of NP etch respectively. It can be seen that the grain boundaries are reduced as etch time increases resulting in deep trenches.



(a) (b)

Figure 5.5: SEM images of CdTe film that underwent (a) 15 s etch and (b) 30 s etch

It has been observed during NP etch of all CdS / CdTe solar cells that the duration of acid contact must be 10 seconds. Once the sample is taken out of the solution it has to be rinsed in DI water to remove any remaining acid and then dried with nitrogen gas.

For the present study we've used the etch process described in section 3.5.2. The open circuit voltages have increased after the NP etch process. The increase in open circuit voltages from before and after NP etch is shown in the table below –

Table 5.4: Open circuit voltages as a function of annealing temperatures for CdS / CdTe solar cells after NP etch and net increase in open circuit voltages

Anneal Temperature of CBD-CdS	Open Circuit Voltage (mV) after NP etch	Net Increase in average value
350°C	310	80
400°C	555	140
450°C	568	63
500°C	385	175

From Table 5.4 it can be inferred that correct NP etch does have a positive effect on the open circuit voltages. A higher increase is seen in the 400°C and 500°C sample. And since the currents for the 450°C were about 18mA/cm^2 and that for the 400°C sample were about 21mA/cm^2, it can be said that 400°C is the better anneal temperature for CdS as it yields a good open circuit voltage and current after the NP etch. Other researchers have also found 410°C and 420°C to be useful to anneal CdS and also yield good results.

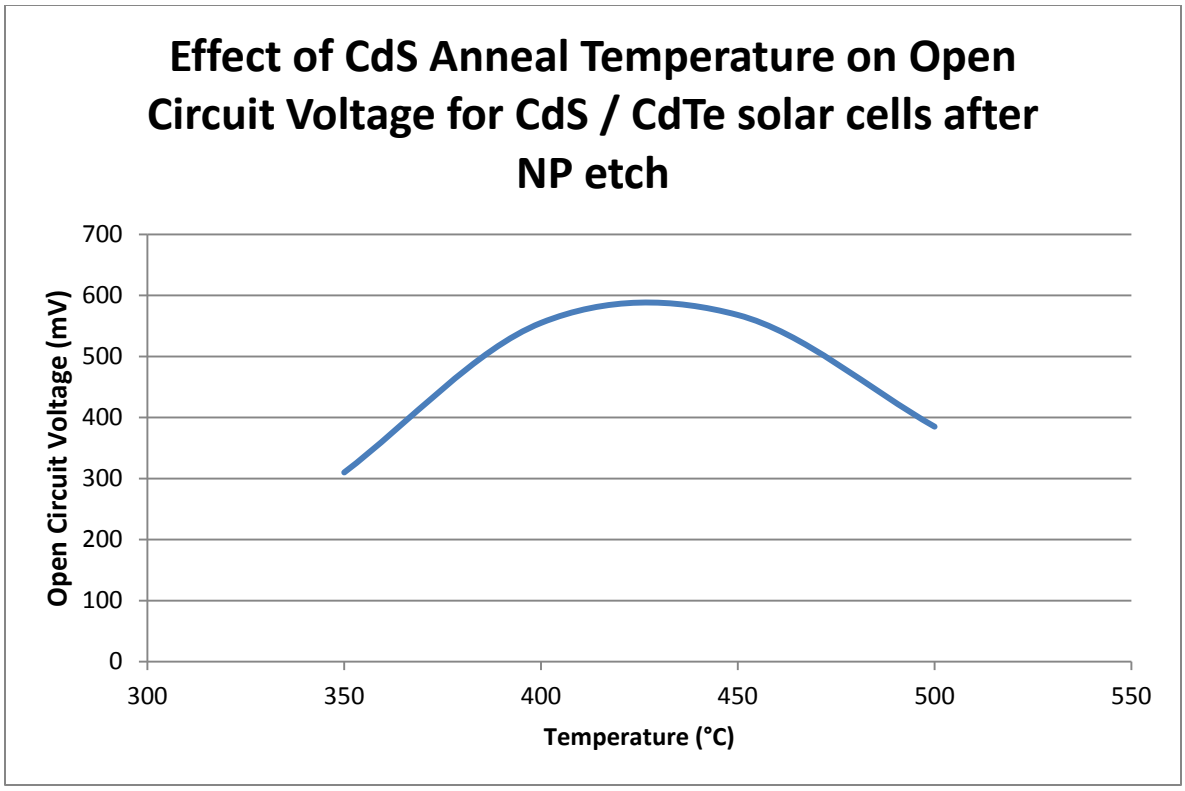


Figure 5.6: Open circuit voltages as a function of annealing temperatures for CdS / CdTe solar cells after NP etch

Table 5.5: Open circuit voltages and currents as a function of annealing temperatures for CdS / CdTe solar cells after NP etch

Anneal Temperature of CBD-CdS	Open Circuit Voltage (mV) after NP etch	Short Circuit Curent mA/cm^2
350°C	310	12.5
400°C	555	21
450°C	568	18
500°C	210	14.2

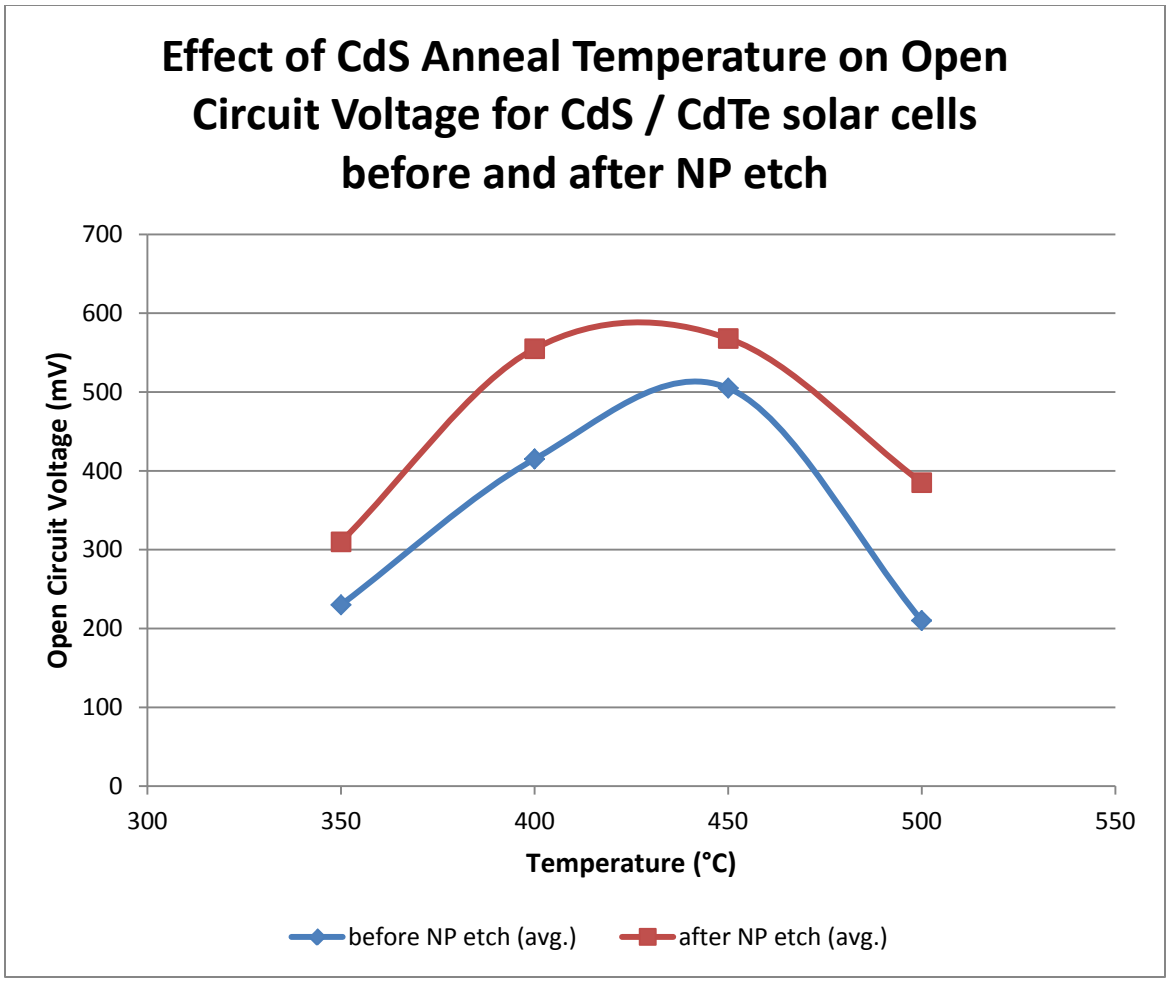


Figure 5.7: Open circuit voltages as a function of annealing temperatures for CdS / CdTe solar cells before and after NP etch

Various researchers have shown that NP etch would result in better open circuit voltage and current. The positive effect of NP etch is illustrated in Figure 5.4 for the experiment performed. It has been verified experimentally that the open circuit voltages and currents get better after NP etch.

5.2.3 Effect of Thickness of Thermal Evaporated CdS on Open Circuit Voltages

CdS can be deposited by various methods and Thermal Evaporation is one of them. Four different thicknesses of CdS have been chosen to investigate the effect of thickness of CdS on open circuit voltage. While Chemical Bath deposition technique deposits a fixed amount of CdS on Tin Oxide coated ITO, one can control the thickness of CdS deposited through Thermal Evaporation. Chemical bath deposition is self-limiting depositon process governed by the adhesion factor of CdS on Tin Oxide coated ITO.

Gold crystal thickness monitor was used with the process discussed in section 3.4 to precisely control the thickness of the material being deposited. After deposition the CdS samples were subject to the regular $CdCl_2$ treatment before moving to CSS process for CdTe deposition. Table 5.6 below shows the variation of open circuit voltages and short circuit currents as a function of thickness of thermal evaporated CdS. It is seen that higher thicknesses led to low open circuit voltage and current. This can be attributed to the fact that higher thickness of CdS would mean increased photon absorption in the CdS layer and decrease in the amount of photons available for electron-hole pair generation in CdTe layer.

Table 5.6: Open circuit voltage and short circuit currents as a function of thickness of thermal evaporated CdS in CdS / CdTe solar cells

Thickness of Thermal Evaporated CdS (nm)	Open Circuit Voltage (V_{oc}) (mV)	Short Circuit Current (J_{sc}) (mA/cm^2)
100	550	16
200	550	18
300	450	6.5
500	400	5

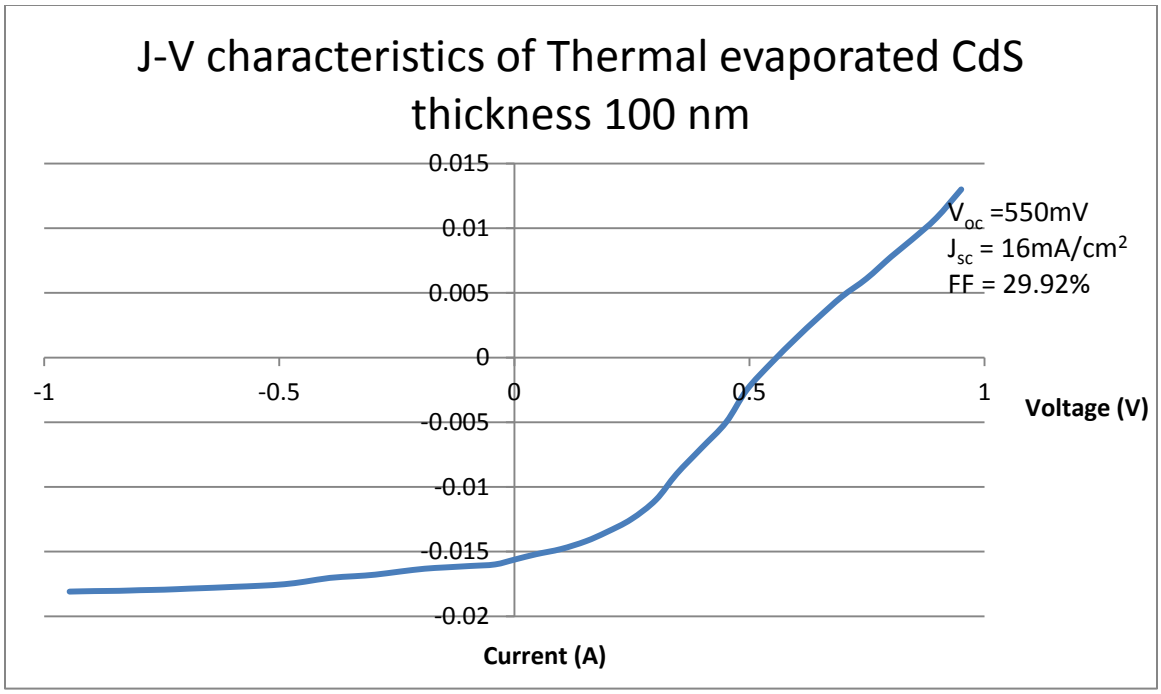


Figure 5.8: J-V characteristics of Thermal evaporated CdS thickness 100 nm

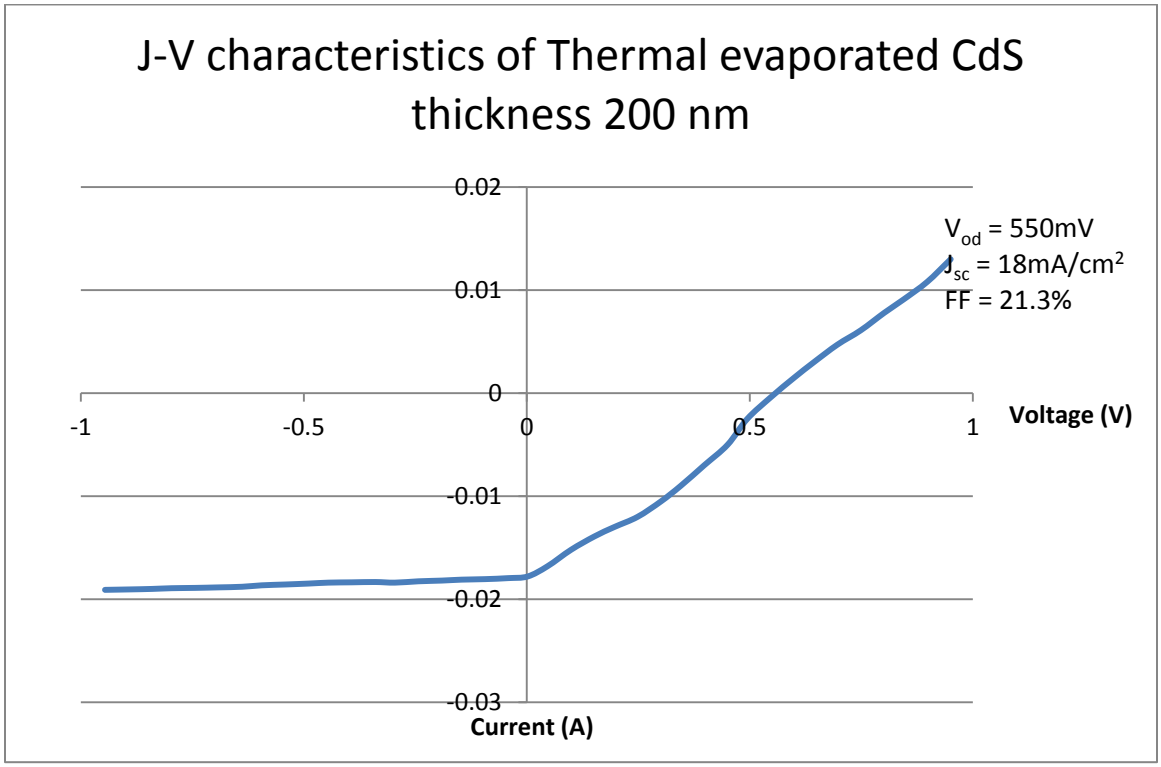


Figure 5.9: J-V characteristics of Thermal evaporated CdS thickness 200 nm

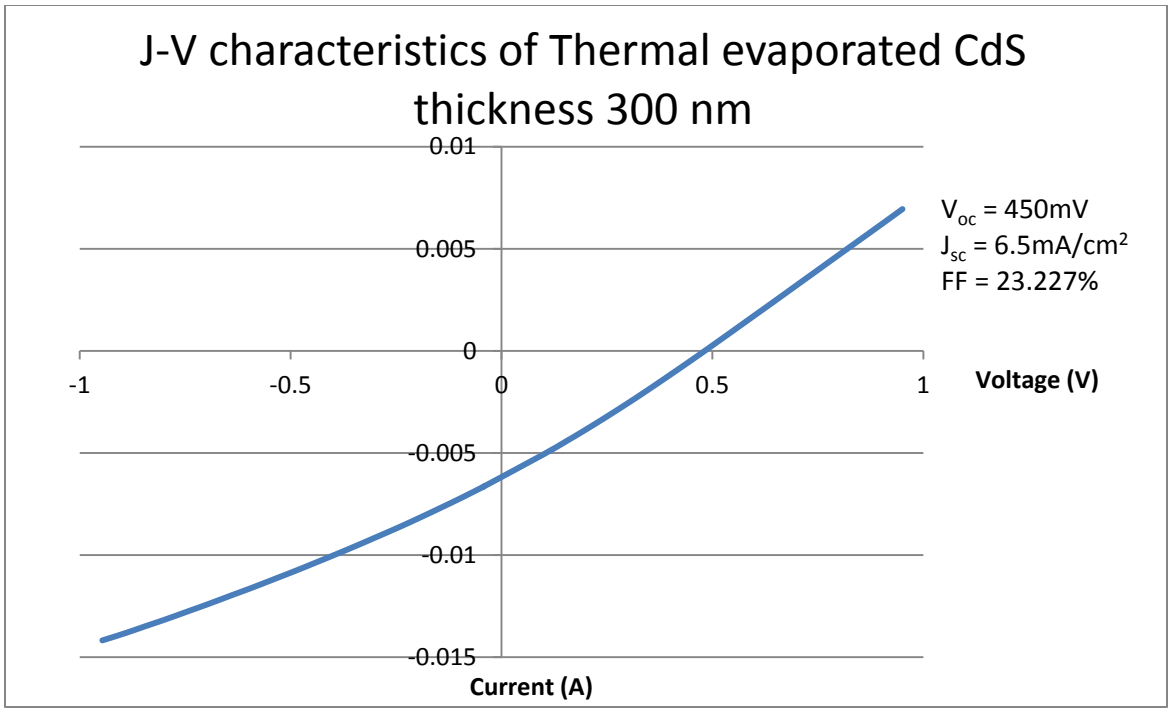


Figure 5.10: J-V characteristics of Thermal evaporated CdS thickness 300 nm

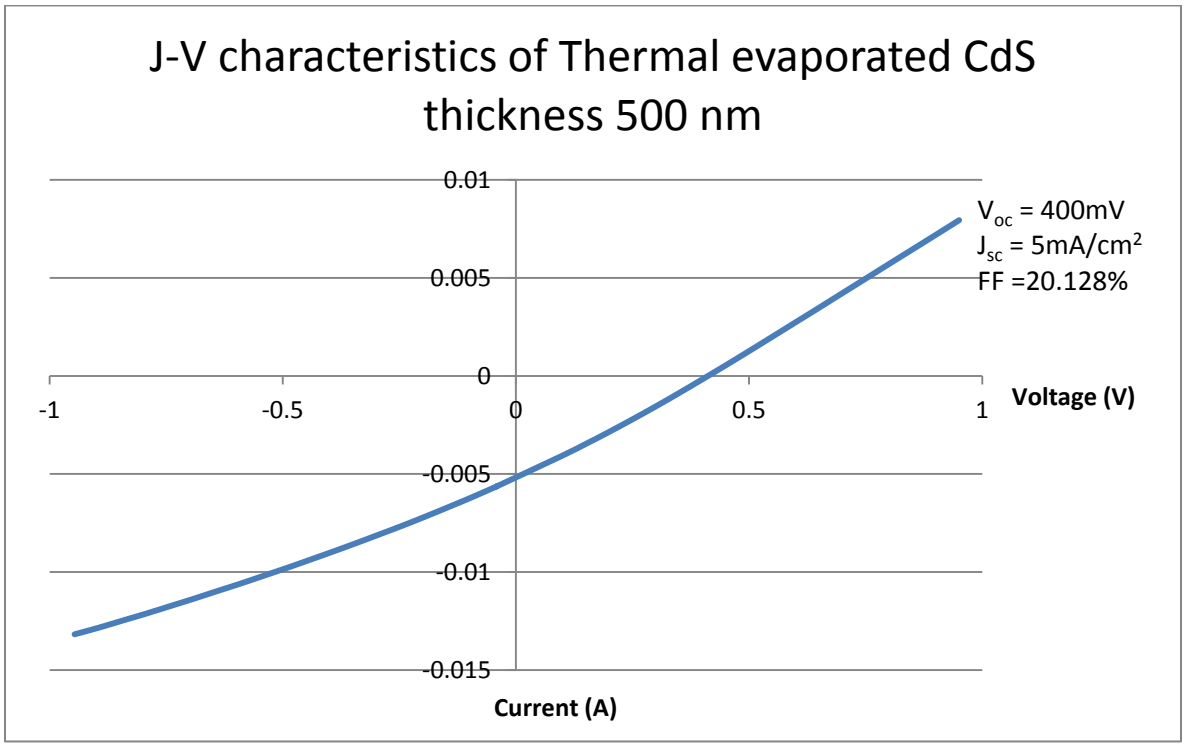


Figure 5.11: J-V characteristics of Thermal evaporated CdS thickness 500 nm

From figures 5.8, 5.9, 5.10 and 5.11, we can deduce the thickness of Thermal Evaporated CdS required for better V_{oc} and J_{sc} on a CdTe / CdS solar cell. From the figures one can say the V_{oc} is the maximum for CdS thicknesses of 100nm and 200nm. But looking at the currents one can be sure that 200nm of Thermal Evaporated CdS gives the best results (Open Circuit Voltage and Short Circuit Current). At increasing thickness of CdS the Open Circuit Voltage, Short Circuit Current and also the Fill Factor are decreasing. Another sample of thickness 1000nm of Thermal Evaporated CdS was made but the CdS peeled off as soon as it came out of the deposition chamber. It thus can be inferred that higher thicknesses of CdS do not adhere well onto Tin Oxide coated ITO glass. It is also a good point to remember here that the CdS layer does not have zero absorption. It has a finite absorption which changes with change in wavelength of incident radiation. So, as we deposit higher thicknesses of CdS we are just not risking the adherence of CdS onto the substrate but also increasing the total absorption by CdS layer. This will reduce the light available for CdTe layer thus limiting the number of photons available for absorption and carrier generation.

Chapter 6 Conclusions and Future prospects

CdS / CIT solar cells have been investigated for the first time and marginal success has been achieved in terms of open circuit voltages. CIT is a promising compound for solar cell applications provided the flexibility and the ease of fabrication. It has been noted that CIT has a direct band-gap of 0.95 – 1.1 eV. With a band-gap of 0.9 - 1 eV, CIT absorbs the Ultraviolet, Visible and Near-InfraRed portion of the incident light. But research has to be done on the boundaries of CdS-CIT and CIT-Metal contact (carrier collection process). If these boundaries were mastered then CIT solar cells have a great chance to become good solar cells and match efficiencies with other inorganic solar cells.

The effects of CdS anneal temperature and NP etch process on the chemical bath deposited CdS / CdTe solar cells have been characterized in terms of open circuit voltages. It is also seen that NP etch has a positive effect on solar cells if less acid is used. The increase in open circuit voltage is about 175mV after NP etches. If careful processing and fabrication is done, open circuit voltages could break the 1000mV barrier.

The effect of thickness of thermally evaporated CdS on the open circuit voltages and short circuit currents was also investigated. Thermally evaporated CdS has always had stiff competition from Chemcial bath deposited CdS. As seen in this experiment and in the literature Chemical bath deposited CdS has been given better results compared to thermally evaporated CdS.

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Vita

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