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ABSTRACT OF DISSERTATION

Xiaohu Feng

The Graduate School
University of Kentucky
2007

SIC BASED SOLID STATE POWER CONTROLLER

ABSTRACT OF DISSERTATION

A dissertation submitted in partial fulfillment of the
requirements for the degree of Doctor of Philosophy in the
College of Engineering
at the University of Kentucky

By

Xiaohu Feng

Lexington, Kentucky

Director: Dr. Arthur V.Radun, Professor of Electrical Engineering

Lexington, Kentucky

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ABSTRACT OF DISSERTATION

SiC Based Solid State Power Controller

The latest generation of fighter aircraft utilizes a 270Vdc power system [1]. Such high voltage DC power systems are difficult to protect with conventional circuit breakers because the current does not automatically go to zero twice per cycle during a fault like it does in an AC power system and thus arcing of the contacts is a problem. Solid state power controllers (SSPCs) are the solid state equivalent of a circuit breaker that do not arc and which can respond more rapidly to a fault than a mechanical breaker [2]. Present SSPCs are limited to lower voltages and currents by the available power semiconductors [8,9]. This dissertation presents design and experimental results for a SSPC that utilizes SiC power JFETs for the SSPC power switch to extend SSPC capability to higher voltages and currents in a space that is smaller than what is practically achievable with a Si power switch. The research started with the thermal analysis of the SSPC's power switch, which will guide the development of a SiC JFET multi-chip power module to be fabricated by Solid State Devices Inc. (SSDI) using JFETs from SiCED and/or Semisouth LLC. Multiple multi-chip power modules will be paralleled to make the SSPC switch. Fabricated devices were evaluated thermally both statically and dynamically and electrically both statically and dynamically. In addition to the SiC module research a detailed design of the high voltage SSPC control circuit capable of operating at 200ºC was completed including detailed analysis, modeling and simulations, detailed schematic diagrams and detailed drawings. Finally breadboards of selected control circuits were fabricated and tested to verify simulation results. Methods for testing SiC JFET devices under transient thermal conditions unique to the SSPC application was also developed.

KEYWORDS: SiC, JFETs, SSPC, Thermal Analysis, Multi-Chip

________Xiaohu Feng______________________

____________08/24/2007______________________

SiC Based Solid State Power Controller

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Name	Date

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SiC Based Solid State Power Controller

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Chapter1 Introduction

1.1 Background

Solid state power controllers (SSPC) were developed for power management and fault protection for aircraft power system applications [1,7]. They were first developed for the aircraft's 28Vdc power system, then for the aircraft with 115Vrms 400Hz power systems and are now under development for 270Vdc aircraft power systems. Modern aircraft have complex advanced electrical power systems that require the use of an electrical load management system [1,2]. A load management system allows the aircraft power system to make critical decisions as to which loads at any given time are mission critical, flight critical, and non-critical. The SSPC is a critical technology required to implement an electrical load management system [1,7].

In an aircraft electrical power system, the most dangerous fault is a short circuit. During a short circuit, fault the current will instantaneously increase to a value at least 10 times the rated current, a value which will cause damage to the electrical power system components. This includes overheating the power system wiring causing insulation degradation which in turn can cause arcs and arc propagation in the wiring harnesses [4]. The damage caused by such faults is minimized by turning off the fault current quickly once the fault has been detected. Faults in DC aircraft electrical power systems are especially hard to protect against since the fault current never goes to zero as it does twice per cycle in an AC system [2]. With advanced solid state device and package technology, solid state power controllers (SSPCs) can be developed for DC power systems with a turn off time that limits the energy dissipated in the wiring during a fault. This is accomplished by designing the SSPC to turn off at a chosen

$$\int i(t)^2 \, dt \propto Energy$$

called an I^2T trip curve. A typical constant I^2T trip curve is shown in Figure 1.5.

This dissertation describes research done to develop a SSPC for a 270Vdc aircraft

electrical power system. As shown in Figure1.1, the SSPC is put between the generator and the load to protect the circuitry from faults. The SSPC which is the object of this dissertation will protect against an over current that exceeds a specified maximum value, an over I^2T if the fault current is between the rated current and the specified maximum value, or an over temperature of the SSPC's main semiconductor switch by turning off the current (tripping). Thus the SSPC is essentially a smart solid-state circuit breaker which has the ability to sense current and will trip if the SSPC's current exceeds a current versus time curve. The developed SSPC can also be controlled by an external electrical signal. If the SSPC trips due to a fault it can be reset using the electrical input or a manual switch.

In the SSPC, a power semiconductor is used to turn the power being controlled on and off. The characteristics of the power semiconductor used determine the maximum current rating, power dissipation and minimum response time of the SSPC. MOSFET technology is currently used in lower current and voltage SSPCs such as DDC's SSP-21116 rated at 100V maximum with a 15 A current capability for use in 28V aircraft power systems [6,8,9]. Since available MOSFETs use Silicon (Si) they have limitations, such as high on resistance at high voltages and temperatures, high power dissipation at high temperature, a maximum 125 °C working temperature, etc.

Compared to Si, Silicon Carbide (SiC) has a number of advantages including lower on-resistance for a given chip area at high voltage and 200°C capability. A more detailed comparison between Si and SiC is given in section 1.3. In this research, the SiC JFET was chosen for the main power switching device in the SSPC to significantly improve the performance of SSPCs for use in 270Vdc aircraft power systems.

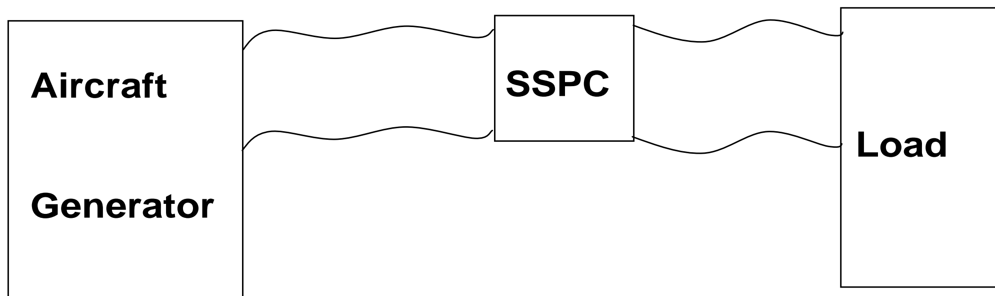


Figure 1.1 Illustration of an aircraft DC electrical power system with a SSPC

1.2 Literature Review

Conventional aircraft electrical power systems have used fuses, circuit breakers, and relays for circuit protection and control. The SSPC is an alternative to the conventional electromagnetic circuit breaker that uses a power semiconductor switch to protect the circuit. The solid state nature of these devices means there are no moving parts so that the SSPC's lifetime is much longer than a conventional electromagnetic circuit breaker's lifetime. Thus the SSPC improves the aircraft power system's reliability. The SSPC has the additional advantages that it has much faster response time and is less susceptible to vibrations [1,7].

Presently, SSPCs are most widely used in 28Vdc aircraft power generation and distribution applications. For example, the aerospace industry uses SSPCs built to various military specifications (Mil. Specs.) to control cabin lighting and temperature onboard aircraft [6]. SSPCs with digital interfaces are used to control 28 VDC loads, such as pumps, valves, lights, actuators, fans, to protect wiring harnesses and loads from fire due to wire shorts or insulation failures, and to monitor load operation and health [3-6].

Present research on SSPCs has focused on the stability analysis of aircraft power systems with SSPCs and how to increase the current and voltage ratings of SSPCs [1-9]. In this research the power semiconductor of choice for the main power switch has been the Si power MOSFET. As discussed before, the current and voltage capability of SSPCs using Si power MOSFETs is limited by the electrical properties of the Si.

1.3 SiC Versus Si

There are a number of benefits obtained by employing a SiC power semiconductor for the SSPC's main power switch. Silicon Carbide is a new semiconductor material with a much higher breakdown electric field than Si due to its higher energy gap and a material with a higher thermal conductivity than Si [18]. A comparison of the electrical properties of SiC and Si is given in Table 1.1. The

performance advantages of SiC over Si in power electronics applications include lower resistance devices for the same area due to its higher breakdown electric field, higher junction temperature operation, and thus higher case temperature operation [19].

Table 1.1 Electrical and material properties of Si, and SiC at room temperature unless otherwise noted [19]

Material property	***Si***	***SiC***
Electron mobility = $_{e}$ (at 150 ^{o}C and 600 V) (cm^2/V.sec)	576	148
Breakdown electric field = E_{max} (V/cm)	3 x 10^5	1.9 x 10^6
Dielectric constant = . $_{r}$	11.7	9.66
Built in potential (Schottky) = V_{bs} (Volt)	0.5	1.1
Built in potential (junction) = V_b (Volt)	0.7	2.1
Thermal conductivity = K_T W/(cm .C)	1.45	4.56

Silicon Carbide has a higher energy gap compared to Si, which gives it the advantage of significantly lower reverse leakage currents, especially important at high temperatures, compared to Si. Thus SiC can operate at higher junction temperatures. The higher energy gap of SiC compared to Si gives it the advantage of a much higher breakdown electric field compared to Si, while giving it the disadvantage that its forward p-n junction voltage drop is much greater than that for Si. Thus SiC device research to date has concentrated on devices that do not have a p-n junction, such as field effect transistors and Schottky diodes. It is junction field effect transistors that were applied in this research.

In power applications, an important consideration is the maximum junction temperature at which the device can operate. Figure 1.2 shows the maximum junction temperature of Si, SiC in the near term, and SiC in the far term. As Figure 1.2 shows, research results to date indicate that SiC has the potential to operate at temperatures as high as 400°C. In the near term, packaging considerations will limit SiC device junction temperatures to values more like 250°C. This is a significant improvement over Si's

maximum junction temperature of 150°C. In addition, a SiC device operating at a junction temperature of 250°C, which is significantly lower temperature than its theoretical maximum, should be more reliable than a corresponding Si device at operating at a junction temperature of 150°C [19]. High thermal stress is a leading cause of semiconductor failures.

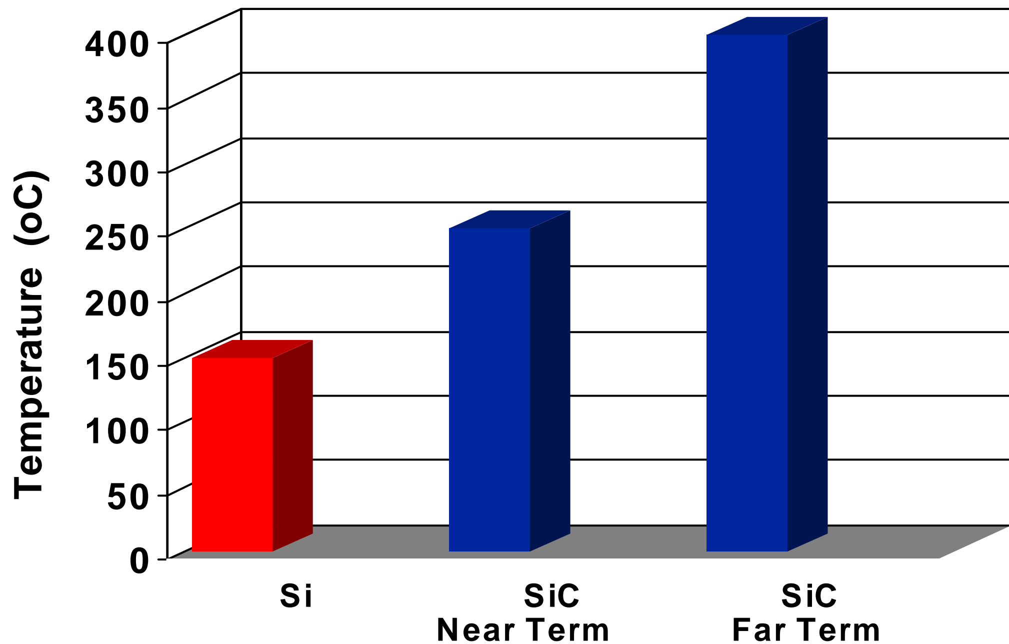


Figure 1.2 Comparison of the Maximum Semiconductor Operating Junction Temperature for Si, Near Term SiC and Far Term SiC.

Typical thermal requirements for a system employing power semiconductors are shown in Fig 1.3. As shown, this thermal system is constrained by the maximum junction temperature of the device and the maximum ambient temperature. The difference between these two temperatures is the allowed temperature rise. This temperature rise in turn constrains the product of the system's thermal resistance and the power dissipated in the power semiconductor. The total temperature rise is made up of two main parts. The first part is the temperature drop across the device itself. The thermal conductivity of SiC is about 4.5 W / (cm °C) compared to silicon's 1.5 W / (cm °C). This means that a SiC

device with the same dimensions as a Si device and with the same power dissipated in it, will have 1/3 the temperature rise in the device compared to its Si counter part. Because the resistance of a SiC device for the same voltage rating is less than that of Si, the power dissipated in a SiC device whose size is equal to that of the Si device will be less than the Si device's power dissipation resulting in lower temperature rise in the SiC device. This is illustrated in Fig 1.3, where the thermal performance of a Si device is compared to that of a near term SiC device and a far term SiC device.

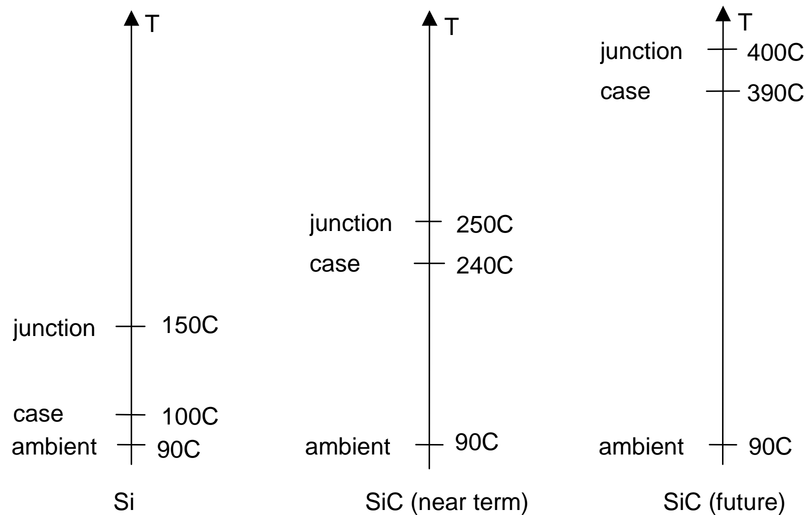


Figure 1.3 Performance Comparison for Si and SiC Technologies

For the work proposed here, it is the near term SiC case that is of greatest interest. In a typical application the maximum ambient temperature is around 90 °C. For a Si design, the maximum junction temperature is 150 °C and there is typically a 50 °C temperature drop from the device's junction to its case when it is operating at high power. This leaves only a 10 °C temperature rise from the ambient to the case of the device. Thus in such high power applications, the ambient is a liquid in order to keep the ambient to case temperature rise to this low value.

For a SiC design the maximum junction temperature in the near term is 250 °C. Because of the SiC device's higher thermal conductivity and its lower losses, it should be possible to design the thermal system so there is a 10 °C temperature drop from the device's junction to its case when it is operating at high power. This now leaves a 150 °C

temperature rise from the ambient to the case of the device. This means that the thermal resistance from the ambient to case for the SiC device can be 15 times greater than that for the Si device. This results in the opportunity to cool the SiC device with air instead of a liquid in high power applications. This is a large system advantage since it eliminates the liquid, liquid cooling hardware, a pump, and heat exchangers. This potential advantage is an important factor for the more electric aircraft.

In the case of the SSPC, the maximum aircraft structure temperature is 121°C and the aircraft structure is the final ambient the heat generated by the SSPC power semiconductors must flow to. Thus the picture in Figure 1.3 must be modified as shown in Figure 1.4. Note that the maximum junction temperature of the SiC power semiconductor has been chosen to be 225°C rather than 250°C to be conservative. For this SSPC application the temperature rise of the Si device from its junction to the aircraft surface is only 29°C while the temperature rise of the SiC device from its junction to the aircraft surface is 104°C. The increased available temperature rise of the SiC device combined with its roughly 3 times greater thermal conductivity compared to Si makes a 270VDC SSPC feasible in a reasonable package size with SiC power devices while it is not feasible with Si devices.

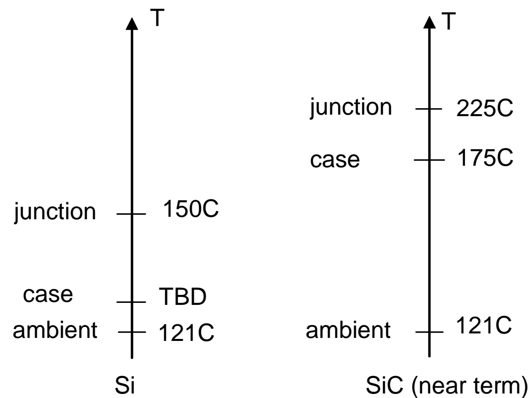


Figure 1.4 SSPC Performance Comparisons for Si and SiC Technologies

The maximum current requirement of the SSPC is shown in Fig 1.5. This specification has three regions or boundaries. In the first, if the current exceeds 10 times the SSPC's rated current the SSPC turns off immediately. In the second region the current

is above the SSPC's rated current but less than 10 times its rated current. In this region the SSPC turns off once the integral of the current above the SSPCs rated current squared exceeds a specified value.

$$I^2T = \int_{i>I_{rate}} \left(i(t) - I_{rate}\right)^2 dt \geq I^2T\Big|_{\max}$$

The specified maximum value of this integral is called the I squared T (I^2T) rating of the SSPC. In the third region, currents below the SSPC's rating, the SSPC must operate continuously. Any current above the SSPC's rated current is called a fault current.

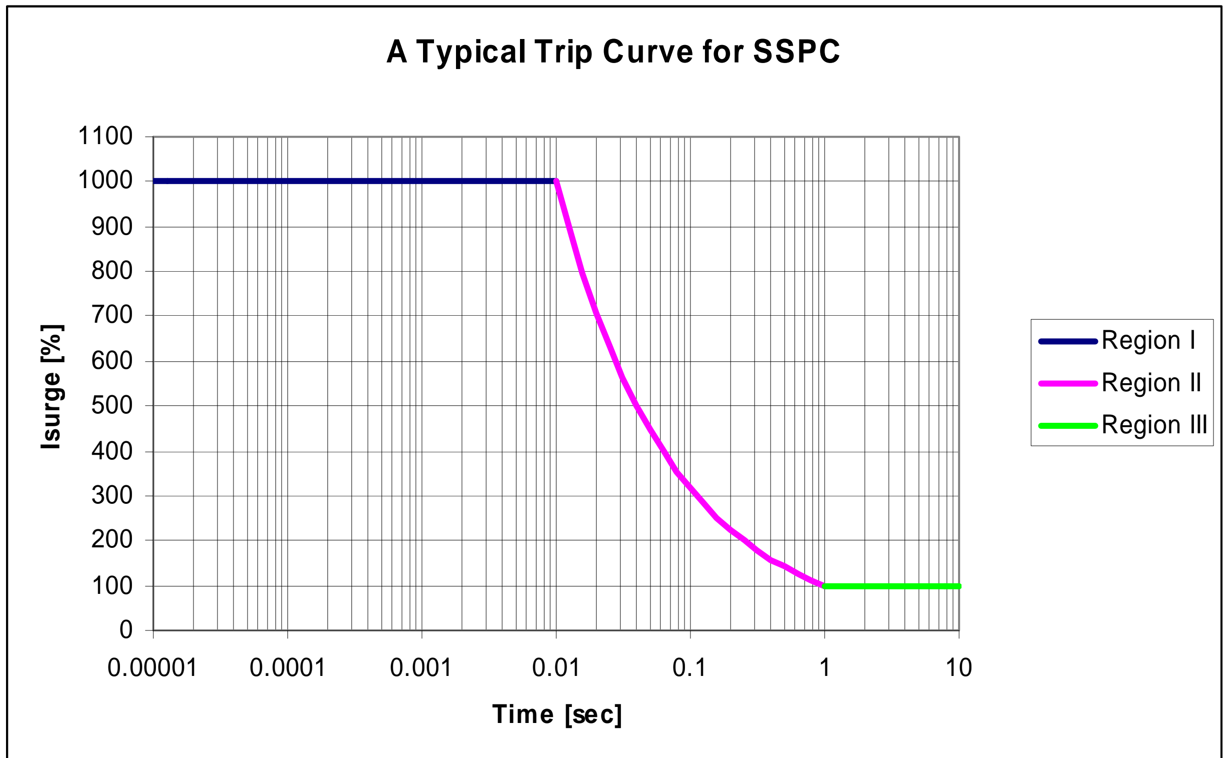


Figure 1.5 Specified SSPC over current requirement

Figure 1.6 and 1.7 show the comparison between a Si power switching device and

a SiC power switching device. Preliminary calculations show that a single SiC power module with 8 600V chips can work at 270V and 96A rated current with a 129C temperature rise from the aircraft structure to the SiC junction. For similar performance 8 Si power modules with a total of 64 chips with the same area as the SiC chips in parallel to work at 270 volts and 100A rated current with a 29C rise from the aircraft structure to the Si junction. Thus a silicon carbide (SiC) based solid-state power controller (SSPC) has smaller size and thus weight where high voltage and current are required.

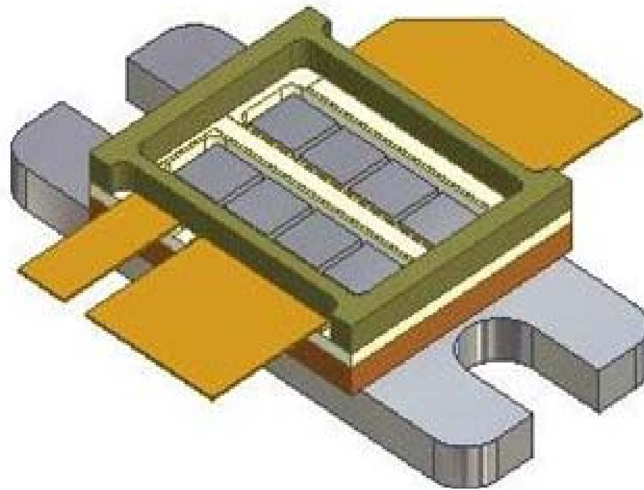


Figure 1.6 SiC power module 270 VOLTS, 64 TO 96 AMPERES, +200°C

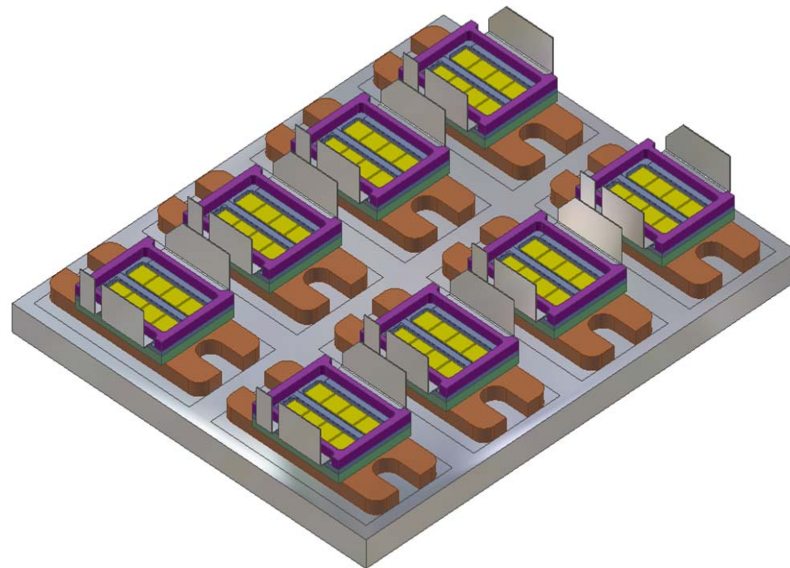


Figure 1.7 Si Power module 270 VOLTS, 100 AMPERES, +125ºC

1.4 Conventional Electromagnetic Breaker versus SSPC

Figure 1.8 shows the structure of a conventional electromagnetic circuit breaker which uses the following principles of operation:

1 Current flowing through the circuit heats the bimetallic current sensor (I^2T calculation), causing it to bend.

2 When the amount of bending exceeds a limit, the armature is released and a spring forces the contacts to open. The load current also flows through a magnetic current sensor (coil) which creates a magnetic field that will trip the armature faster than the bimetal strip can respond when very large currents flow.

3 When the contacts open, an arc will be generated that is dissipated in the arc channel. This opening to the outside prevents pressure buildup inside the breaker's case.

The conventional circuit breaker's performance is limited by:

1 Slow response time of bimetal current sensors.

2 Mechanical tolerances that affect both the thermal and the magnetic trip limits.

3 Inability to differentiate between arcing and normal start up transients due to large motors or incandescent lamps.

4 Mechanical DC switches have arc-extinguishing capabilities built into them that are not required in solid state devices.

In contrast, the SSPC using silicon carbide FET technology allows the SSPC to respond much more quickly to true circuit overload conditions. By opening the circuit in a fraction of a second after detecting an overload, the SSPC significantly reduces the chance for damaging the circuitry being protected. Moreover, advanced aircraft power systems are using 270VDC power instead of the conventional 400 Hz aircraft power. The 270VDC power is more difficult to switch than conventional 400 Hz because of arcing associated with DC Switching. Solid state devices are desirable for this type of switching because they are able to perform arc-less switching [4].

Although the SSPC offers many advantages over conventional electromagnetic

circuit breaker, it also has some disadvantages. The major disadvantage is its cost which is much higher than its conventional counterpart, especially if a SiC power semiconductor is used.

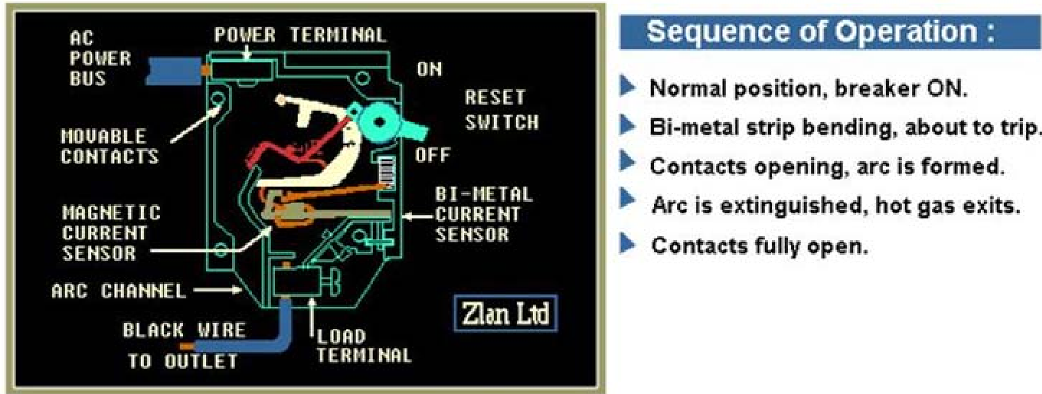


Figure 1.8 Conventional thermal/magnetic circuit structures

1.5 Summery of SSPC Requirements

Solid State Power Controllers (solid state circuit breakers) use electronic components (semiconductor devices) to monitor and control current levels rather than simple electrical devices. These elements are much more precise, and they shut down the circuit more quickly. The SSPC consists of the main JFET switch, current sensor, gate drive, bias power supply, control section, and the communications section. In the control section, there is a detection system designed to detect over-current, exceeded I^2T conditions, and over-temperature of the SSPC switch. The over-current and exceeded I^2T detection protects the external circuit while the over-temperature detection protects the SSPC's power switching device.

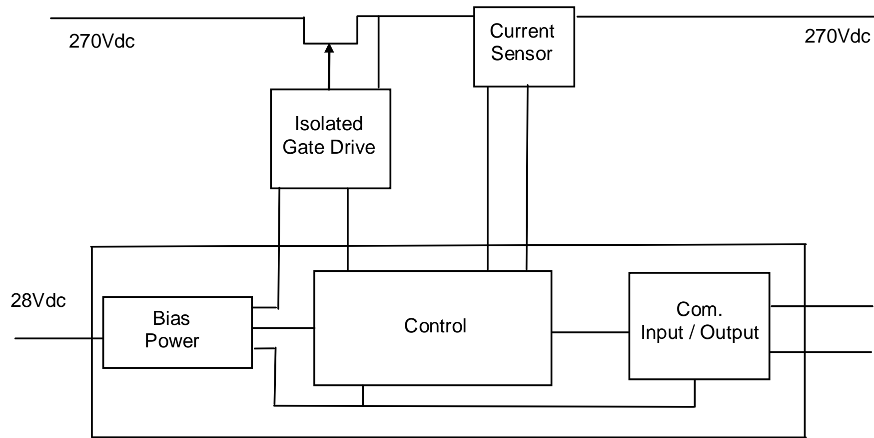


Figure 1.9 Block diagram of the SSPC.

A thermal analysis of the SSPC's power switch has been used to specify the SiC JFET switch. The results show that multiple multi-chip power modules in parallel are required to make the SSPC switch. Representative experimental SiC JFET chips have been evaluated thermally both statically and dynamically and electrically both statically and dynamically. A detailed design of a high voltage SSPC control circuit capable of operating with a 121°C mounting surface temperature and a 225°C maximum junction temperature has been completed including detailed analysis, modeling and simulations, detailed schematic diagrams and detailed drawings. Finally breadboards of the control circuits have been fabricated and tested to verify simulation results.

Chapter2 SSPC Circuit Design

2.1 Introduction

To experimentally verify the SSPC design methodology Si devices were used first to develop the test methods for characterizing the SiC JFETs thermally and to emulate the SiC JFET in the SSPC functional tests. This was done because of the limited availability of SiC devices and their high cost compared to Si devices. Also, the thermal performance of Si devices is available in their specification and this information can be used to verify the thermal models and measurement methods developed. Once the modeling and the

measurement method are correct for Si devices they can be applied to SiC devices.

The functional block diagram of the SSPC is shown in Figure 2.1. The identification and sizing of the power components can be performed independently of the design and analysis of the control circuits.

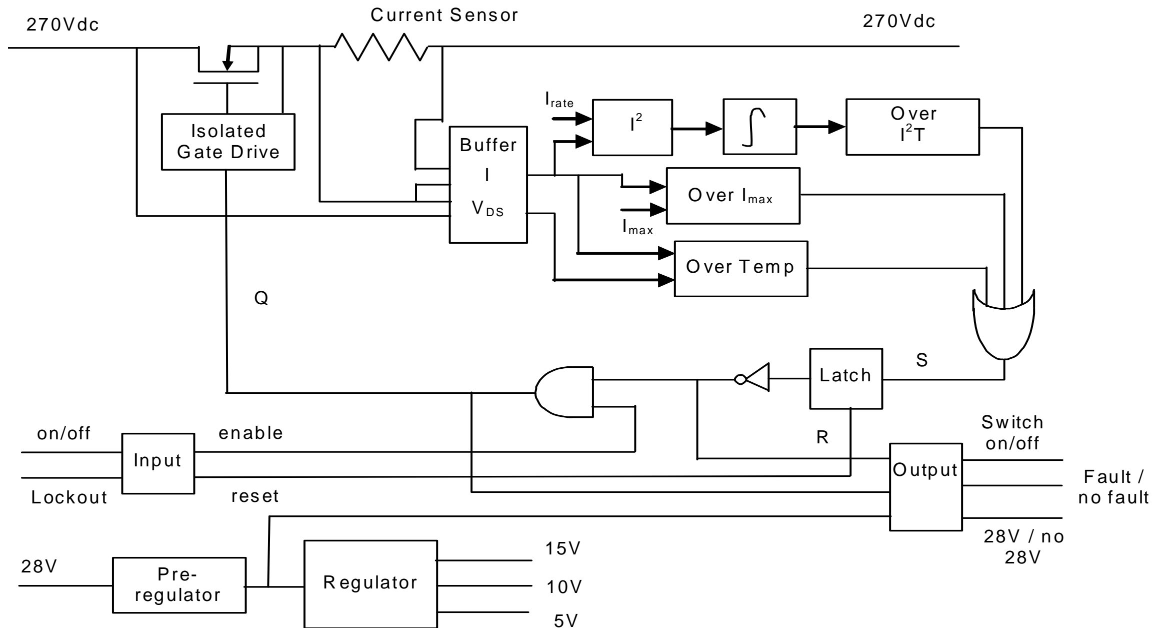


Figure 2.1 SSPC Functional Block Diagram

As stated previously and shown in Fig. 2.1, the SSPC shuts down if the I^2T of the current exceeds a maximum value, the current exceeds a maximum value, or if the main semiconductor switch's temperature exceeds a maximum value. The I^2T quantity is a measure of the heat energy developed within a circuit during a fault. It can be expressed as "melting I^2T", "arcing I^2T" or the sum of them as "clearing I^2T". "I" stands for effective let-through current (RMS), which is squared, and "T" stands for time of opening, in seconds.

One of the research goals was to implement all of the SSPC circuit functions with components capable of operation at 200°C. This meant that a microprocessor could not be used to implement the control functions and in particular could not be used to compute the I^2T of the fault current. Thus the value of I^2T and all of the other control functions needed to be implemented using the available high temperature analog circuit

components.

2.2 SSPC System Design and Design Results

2.2.1 Overview of the SSPC Design

Figure 2.2 shows a Spice model of the SSPC using conventional Si MOSFETs for the power switch.

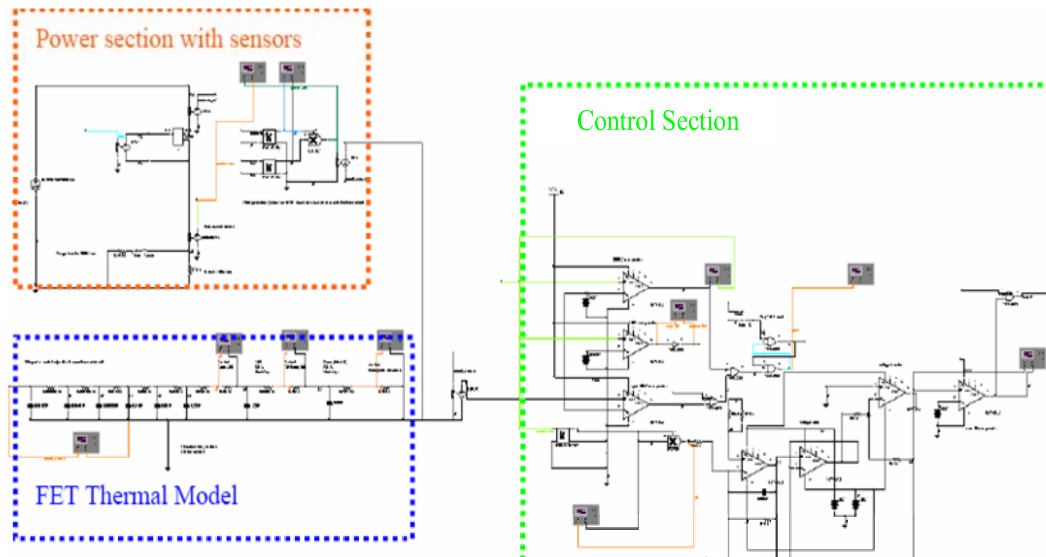


Figure 2.2 Basic SSPC model with showing its basic subsystems.

The power section (in the orange box) contains the electrical model of the power FET, continuous and surge loads, current, and temperature measurements. The control section (in the green box) contains the I^2T computation, thermal shutdown, over-current shutdown, fault store, and reset logic. The thermal model of the power MOSFET (in the blue box) predicts the temperature at various locations in the power FET to insure the FET did not become too hot. The modeling and simulation focused initially on a Si power switch, and once the Si results were satisfactory, then applied to SiC FETs. The control section was designed using available 200°C electronic components though the breadboard circuit was implemented with conventional (low temperature) electronics. The model in Figure 2.2 is setup such that the load fault current is 300A. The simulation

results are shown in Figure 2.3 where the SSPC current and the power switch's junction temperature are shown. The labeled orange trace is the Si MOSFET;s junction temperature and the red (square) trace is the load current. At time = 10msec, the fault occurs and the load current is approximately 300A. After 83msec, the I^2T value exceeds its maximum allowed value and the power FET is turned off and the fault is latched keeping the FET off. At time = 100msec, the SSPC is reset manually and the fault resumes. A second shutdown occurs at 134msec with the fault being latched again due to the MOSFET's junction temperature exceeding its maximum value. The simulation results verify two of the SSPC's fault protection features.

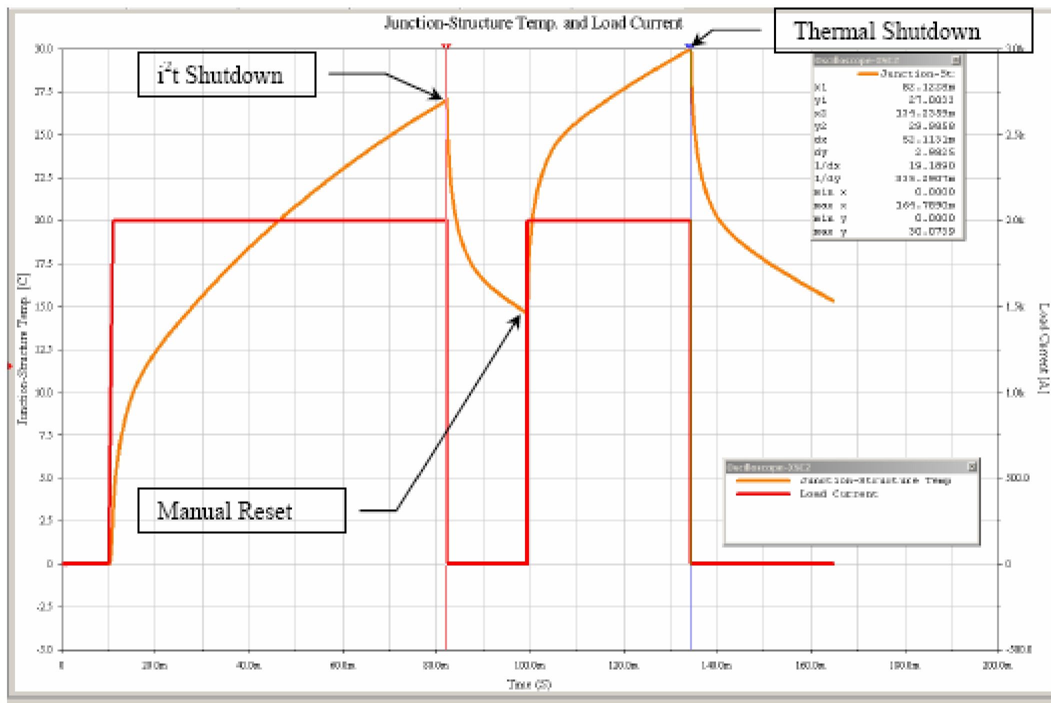


Figure 2.3 SSPC Simulation demonstrating the I^2t and thermal shutdown

2.2.2 Gate Drive Design

The Gate Drive circuit for the SSPC provides the required isolated interface between the ground referenced power switch on / off control command and the high side SiC JFET. The Gate Drive circuit is a high side driver that uses a push-pull topology to transmit pulse waveforms through pulse transformers to transmit signals from the control

ground reference to the SiC JFET's source reference. When the SSPC control issues an Off command, the gate drive circuitry pulls the gate-to-source voltage of the JFET to –40Vdc to turn off the JFET. When the SSPC control issues an On command, the gate drive circuitry pulls the JFET's gate to source voltage to 0Vdc to turn on the JFET. Like the rest of the SSPC control circuits the gate drive design is constrained by the goal that it be constructed out of components capable of operation at 200°C.

As shown in Fig. 2.4, the gate drive circuit consists of three parts, the pull up circuit, the isolated gate power circuit and the pull down circuit. The isolated gate power circuit produces an isolated 40 V dc voltage. Both the pull up circuit and the pull down circuit operate depending on the input command signals Q and not Q (Qbar). The Q and Qbar signals come from a R/S latch that stores the state of the main power switch and thus if a fault has occurred, If the switch is commanded Off etc. When Q is high and Qbar is low, one of the MOSFETs in the pull up circuit is on to essentially short the SiC JFET's gate and source turning the SiC JFET on. The two MOSFETs in the pull up section perform the logic OR function in that one or the other is on depending if the output of the pulse transformer driving these MOSFETs is positive or negative. Thus if the pull up pulse transformer's primary is being pulsed the JFET is turned on. If the pull up pulse transformer's primary is not being pulsed both pull up MOSFETs are off. When Qbar is high and Q is low, one of the MOSFETs in the pull down circuit is on connecting the SiC JFET's gate to -40 V relative to its source. In this way, the voltage between the SiC JFET's gate and source is either zero volts or -40 V, turning it on or turn off.

The SiC JFET switch for a 30A SSPC has about a 90 nF of gate to source capacitance which is denoted Cgs in the equivalent circuit in Figure. 2.4. There is a capacitor named C1 in Figure. 2.4 and 2.5 across the output of the isolated gate power circuit that generates the isolated 40 V DC voltage. When the initial voltage on Cgs is zero volts and the voltage on C1 is 40 V, the SiC JFET can either remain on or turn off depending on the values of Q and Qbar. If Q is high, one of the pull up MOSFETs is on as shown in Figure 2.5 and the SiC JFET remains on. If the initial voltage on Cgs is -40V it will discharge to zero through the gate resistor turning on the SiC JFET.

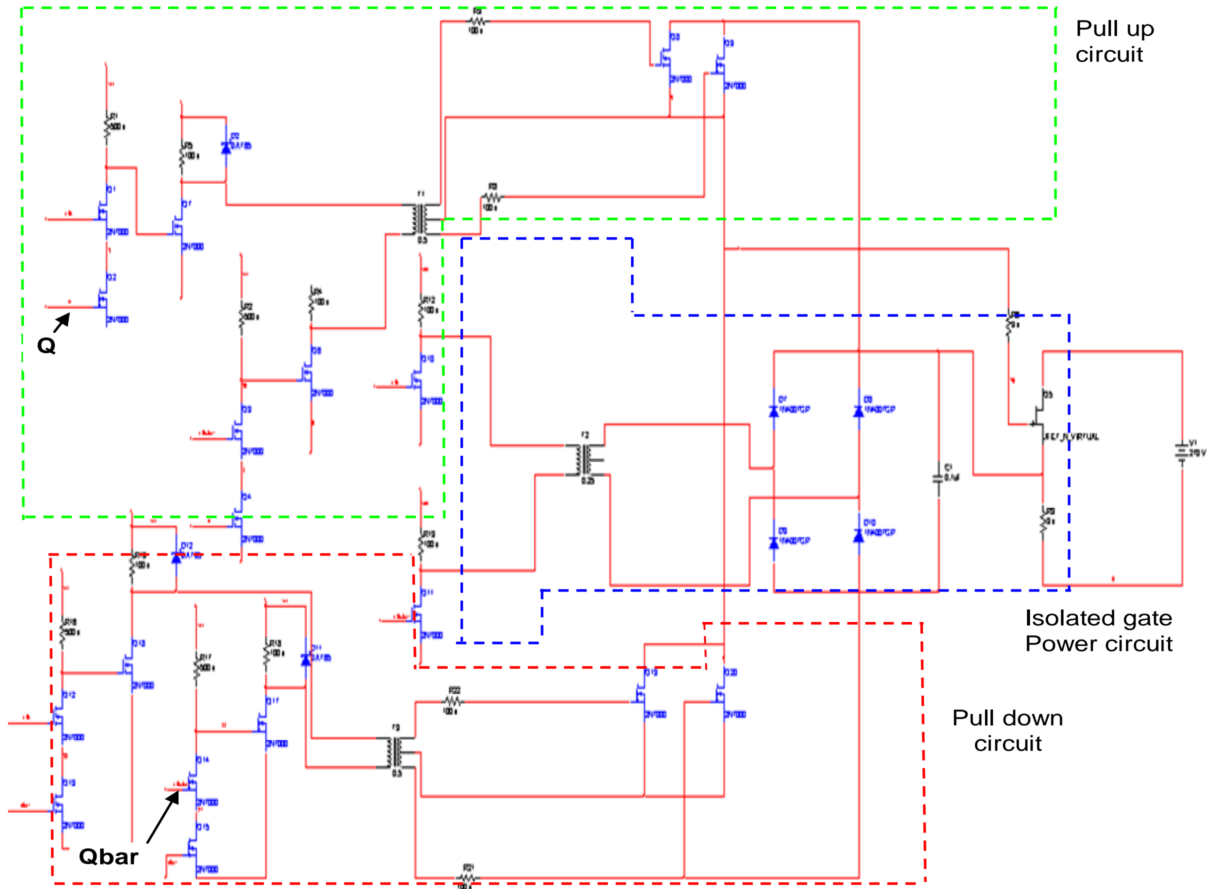


Figure 2.4 SSPC Gate Drive Schematic

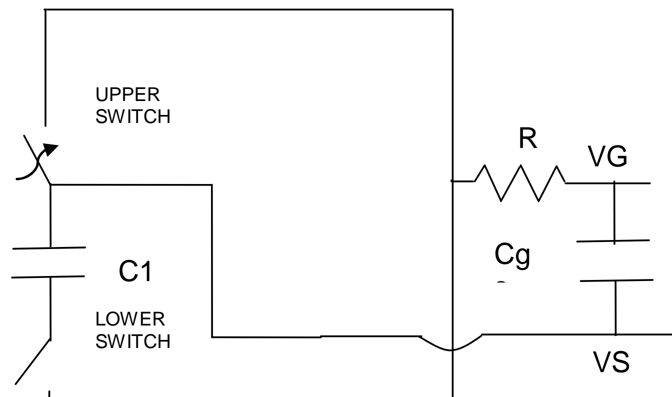


Figure 2.5 Equivalent circuit when the upper switch is closed and lower switch in open (Vgs = 0V.)

If Q is low (Qbar high), one of the pull down MOSFETs is on as shown in Figure

2.6 and the SiC JFET is turned off.

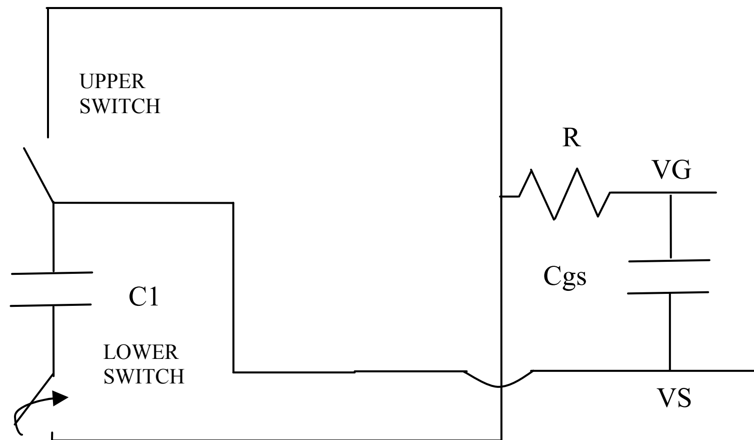


Figure 2.6 Equivalent circuit when the lower switch is closed and upper switch is open (Vgs = -40 V)

The simulation results for the circuit in Figure 2.4 are shown in Figure 2.7. The top most (blue) waveform is the isolated 40Vdc voltage, the next highest (green) waveform is the current through the SSPC and the red waveform is the gate drive signal (Vgs) to the JFET. The figure indicates that the current is 30A when the JFET is on (Vgs=0V) and is 0A when the JFET is off (Vgs=-40V). Figure 2.8 shows the same simulation results showing the relationship between the upper (purple) input command signal (Q) and the lower (blue) gate to source voltage (Vgs),

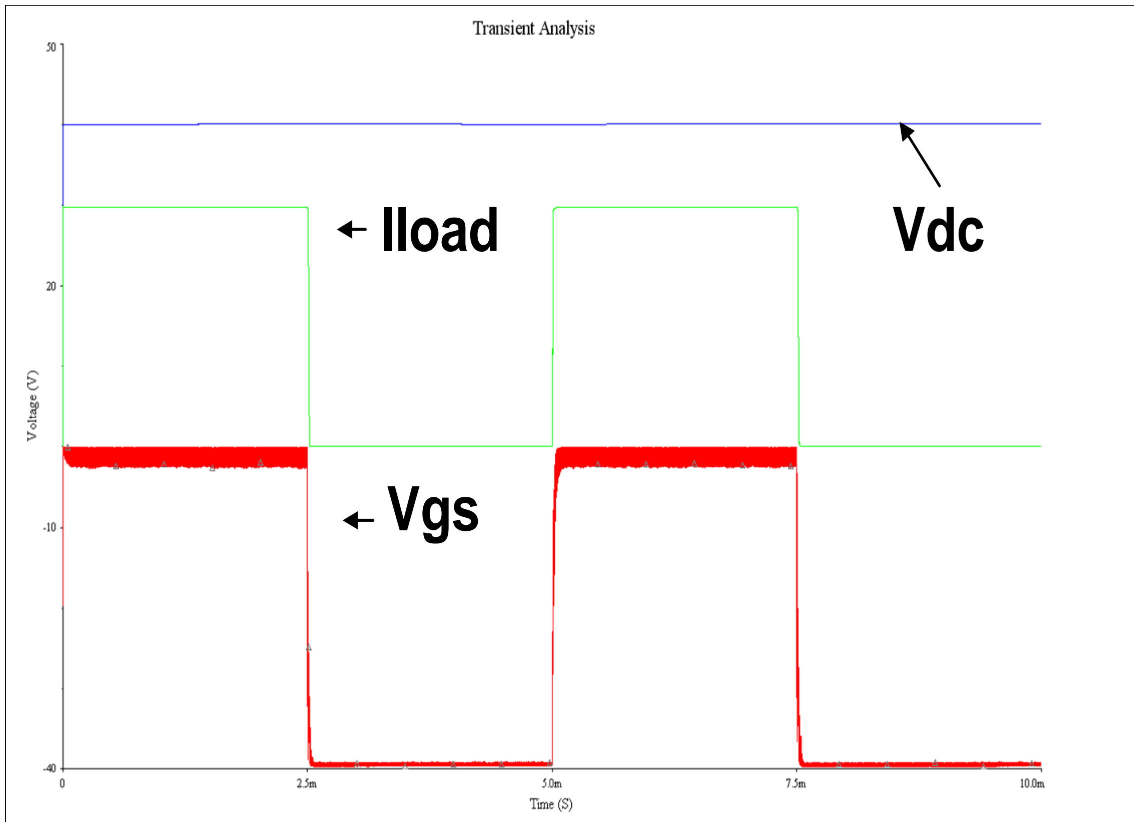


Figure 2.7 The simulation results, C2=10uF and Cgs=90 nF

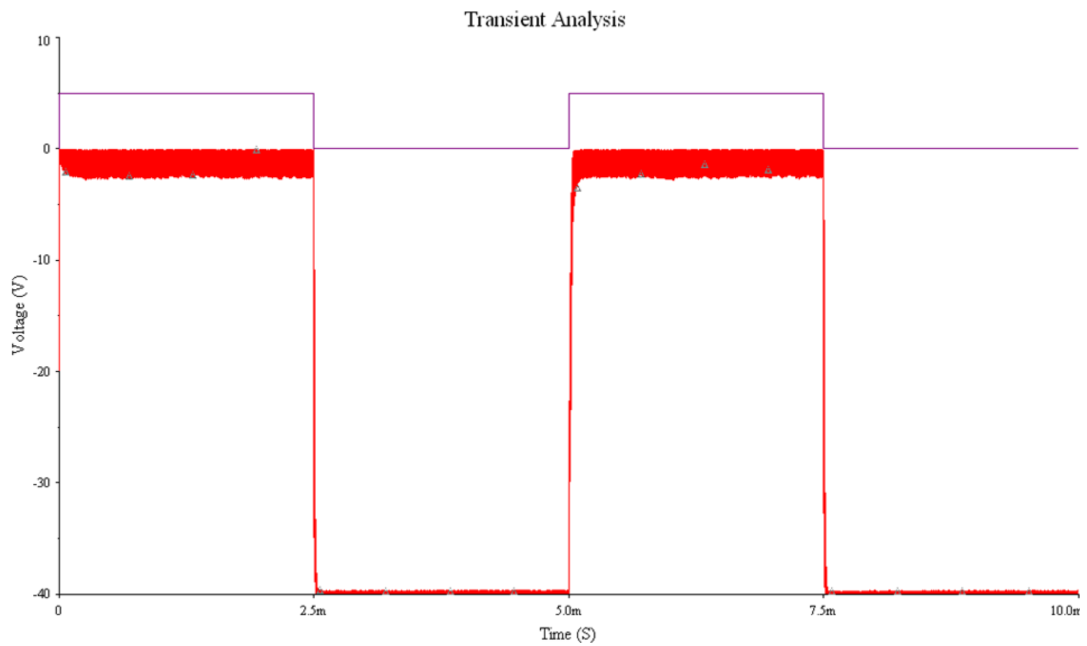


Figure 2.8 The simulations result, C1=10uF and Cgs=90nF. The upper waveform is the logic input and the lower waveform is the gate to source voltage.

2.2.3 Over Current and Over Temperature Protection Circuits

The SSPC senses temperature and current to determine when the SSPC should be on or off. To sense the main JFET switch's temperature the SSPC uses the JFET's on-resistance variation with temperature by sensing the voltage drop across the JFET via a differential op-amp. As the junction temperature of the JFET increases, the on resistance of the JFET increases nearly proportional to temperature. The circuit is set to trip at a JFET junction temperature of 225°C. This occurs at the point where the on resistance of the JFET becomes greater than some value which can be expressed as a constant times the value of the current sense resistor value which does not depend on temperature. Current is sensed using the voltage across a current sense resistor because this is the simplest technique that meets the operating temperature requirement. When the JFET's drain to source voltage becomes greater than a scaled value of the voltage across the current sense resistor the JFET turns off because its junction temperature is too high.

When the load current exceeds 1000% (10 times) the rated load the SSPC shuts down immediately with the current sensing circuit sensing the over current and issuing a shutdown command to the SSPC which is latched. The current sensing circuit senses the voltage drop across the constant 5mΩ sense resistor in series with the power FET and load. The voltage across this current sense resistor is about 0.15 V at rated load current (30A) and 1.5 V at 1000% rated load current (300A). The voltage across the sense resistor is sensed with a differential amplifier (U2) as shown in Figure 2.9 since the current sense resistor is located on the high side of the circuit. The gain of this amplifier is 2.373. The voltage out of the differential amplifier is scaled up by multiplying it by a gain of 2.1 (U3) and the result is compared to a constant voltage of 7.5Vdc (U5). Therefore, when 2.1*VISNS in Figure 2.9 becomes greater than 7.5Vdc the current sensing circuit will detect an over current condition and shutdown the SSPC. The schematic for the temperature and current sensing circuit is also shown in Figure 2.9. The voltage across the FET is sensed with a differential amplifier circuit that is identical to the one used to sense the voltage across the current sense resistor. The over current and over temperature sense circuit gain calculations are summarized below. Thus when

VTSNS becomes greater than 2.1*VISNS or if 2.1*VISNS becomes greater that 7.5Vdc the sensing circuits will sense a fault and issue shutdown command to the SSPC.

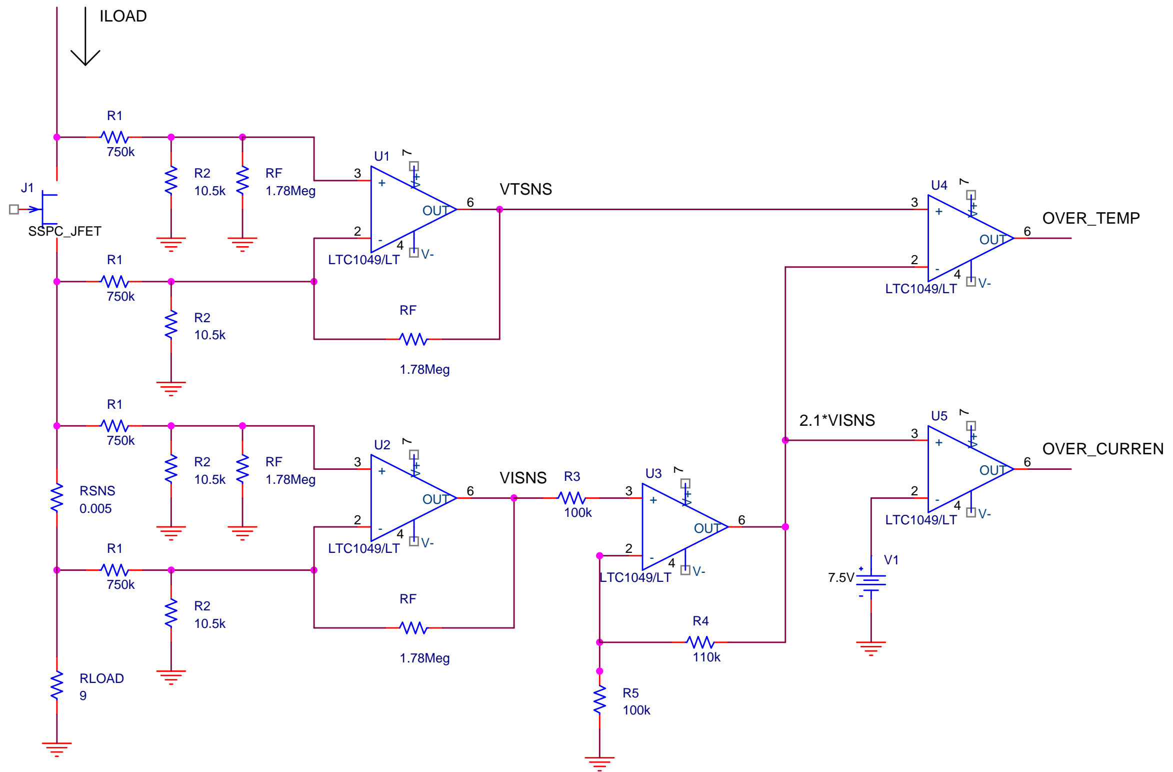


Figure 2.9 Temperature and Current Sensing circuit.

Voltage across JFET (via U1):

$$VTSNS = \frac{ILOAD \times RJFET \times RF}{R1}$$

Voltage across sense resistor (via U2):

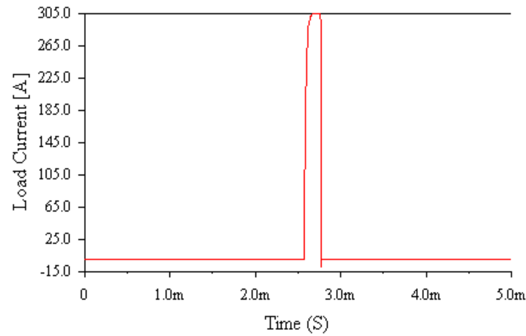
$$VISNS = \frac{ILOAD \times RSNS \times RF}{R1}$$

Voltage at U3 output:

$$2.1 \times VISNS$$

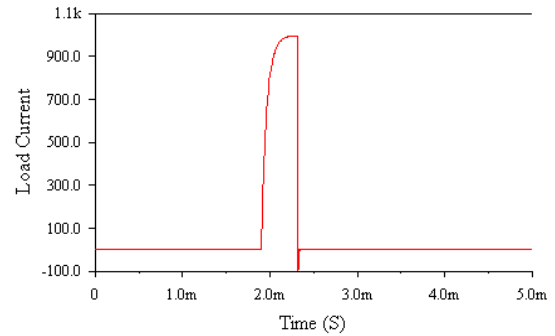
Figure 2.10 below demonstrates the over current circuit operation for an SSPC design for two different SSPC designs, one with a rated load of 30Adc and the other with a rated load of 100Adc. As shown in Figure 2.10 when the load current (Figure 2.10A and 2.10C) exceeds 1000% the rated current for each of the SSPC designs, the current sensing circuit will sense the over current (Figure 2.10B and 2.10D) and shutdown the SSPC.

$I_{LOAD} > 300A$, R_{JFET} @ 120°C

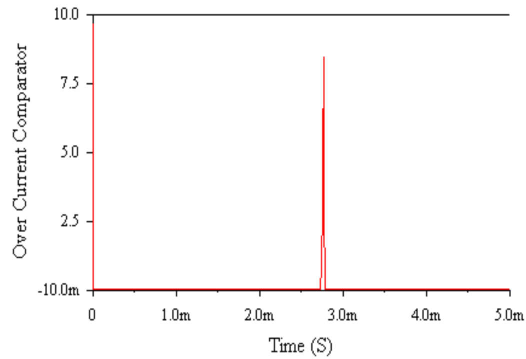


(2.10A)

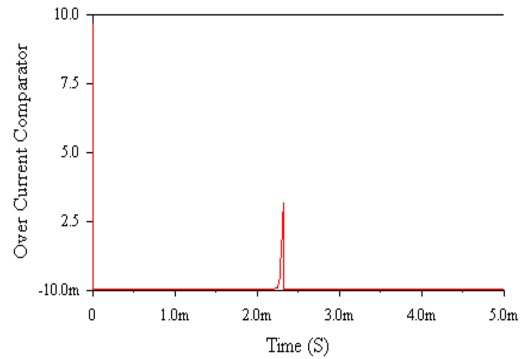
$I_{LOAD} > 1000A$, R_{JFET} @ 120°C



(2.10C)



(2.10B)



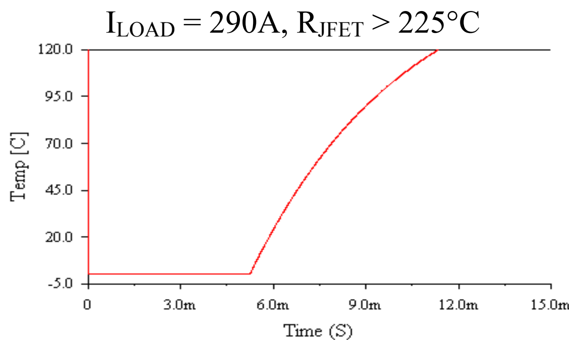
(2.10D)

Figure 2.10 Figure 2.10A and 2.10B are over current sensing simulations at a rated load current of 30Adc. 2.10C and 2.10D are over current sensing simulations at a rated load current of 100Adc.

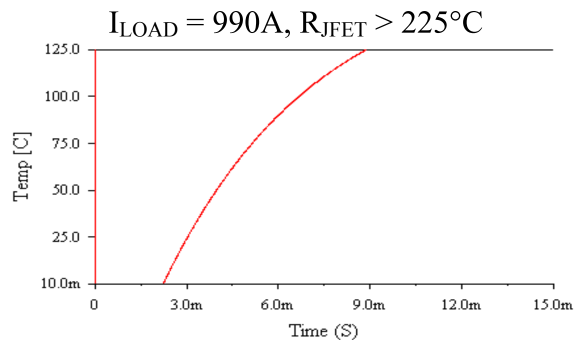
Figure 2.11 below demonstrates the operation of the over temperature circuit for two SSPC designs with rated loads of 30Adc and 100Adc. The temperature scale used in the simulations is shifted so that 0 on the scale corresponds to 120°C, the typical operating temperature of the SSPC. A delta increase of 105°C on the temperature plot in Figure 2.11 correlates to a total junction temperature of 225°C. As can be observed from the plots in Figure 2.11, once the junction temperature reaches 105°C (i.e. 225°C) the SSPC temperature sense circuit senses an over temperature and shuts down the SSPC.

Another thing to note from the plots in Figure 2.11 is that before the SSPC JFET

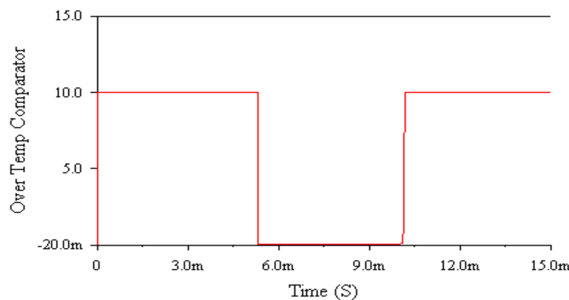
is turned on the temperature sensing circuit is indicating an over temperature fault. This is due to the fact that when the SSPC JFET is off the temperature sensing circuit shown in Figure 2.9 above is sensing the 270V drain to source voltage across the off JFET. Since the SSPC JFET is off there is no load current, and the on resistance of the JFET is theoretically infinite. Therefore, the temperature sensing circuit of the SSPC senses the 270Vdc drain to source voltage that causes the circuit to indicate a fault. To accommodate this issue with the over temperature circuit, additional circuitry has been added to the final design. Since the JFET does not heat up until it has operated above the rated load for a period of time, circuitry has been added to disable the temperature sensing circuit until after the SSPC JFET is turned on.



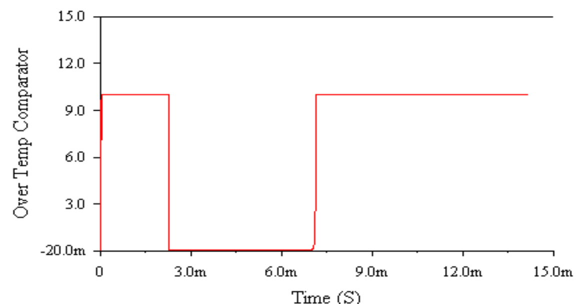
(2.11A)



(2.11C)



(2.11B)



(2.11D)

Figure 2.11 Figure 2.11A and 2.11B are over temperature sensing simulations at a rated load current of 30Adc. 2.11C and 2.11D are over temperature sensing simulations at a rated load current of 100Adc.

2.2.4 SSPC Switch Current and Voltage Measurement Issues

Because the sense resistor is on the high voltage side, the voltage on one side of the constant sense resistor is 270V and on the other side it is 269.85V or 268.5V depending on the current. The test circuit used to evaluate the current sense circuit is shown in Figure 2.12. The 270V added to the 0.15V signal is called the signal's common mode voltage while the desired 0.15V is called the signal's differential mode voltage.

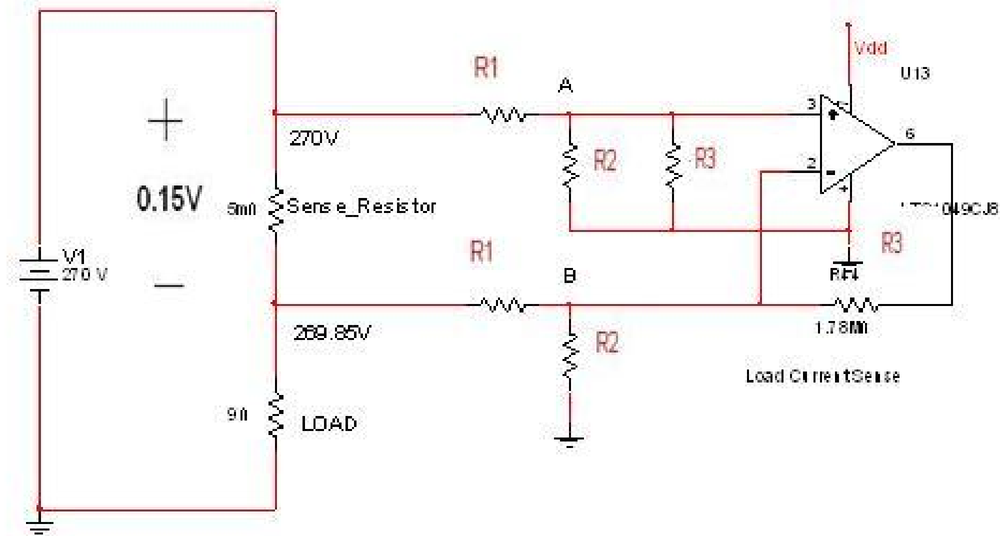


Figure 2.12 Current sense test circuit schematic

As shown in the figure 2.12, resistors R1 and R2 are used to divide the voltage on both sides of the constant sense resistor so that the voltage is small enough to be input to the differential OP-AMP. Thus the common mode part of the signal must be divided down to be within the bias voltage range of the OP-AMP. Unfortunately the small differential mode part of the signal also gets divided by the same amount. Since the voltage across the constant sense resistor is very small, it requires that the two R1 resistors must be close enough in value and the two R2 resistors must also be close enough in value so that the voltage division error between the two voltage dividers is sufficiently small compared to the small voltage drop being sensed, which is also divided by the voltage dividers.

A Spice model was constructed in order to compute the error between the desired and actual output voltages due to the resistance change of the divider resistors. Figure 2.13 shows the simulation results for the output voltage response for different values of

one R1 resistor and Table 2.1 summarizes the results in figure 2.13. Here the required value of R1 is 1Mohm and the resulting output voltage is 0.329 volt.

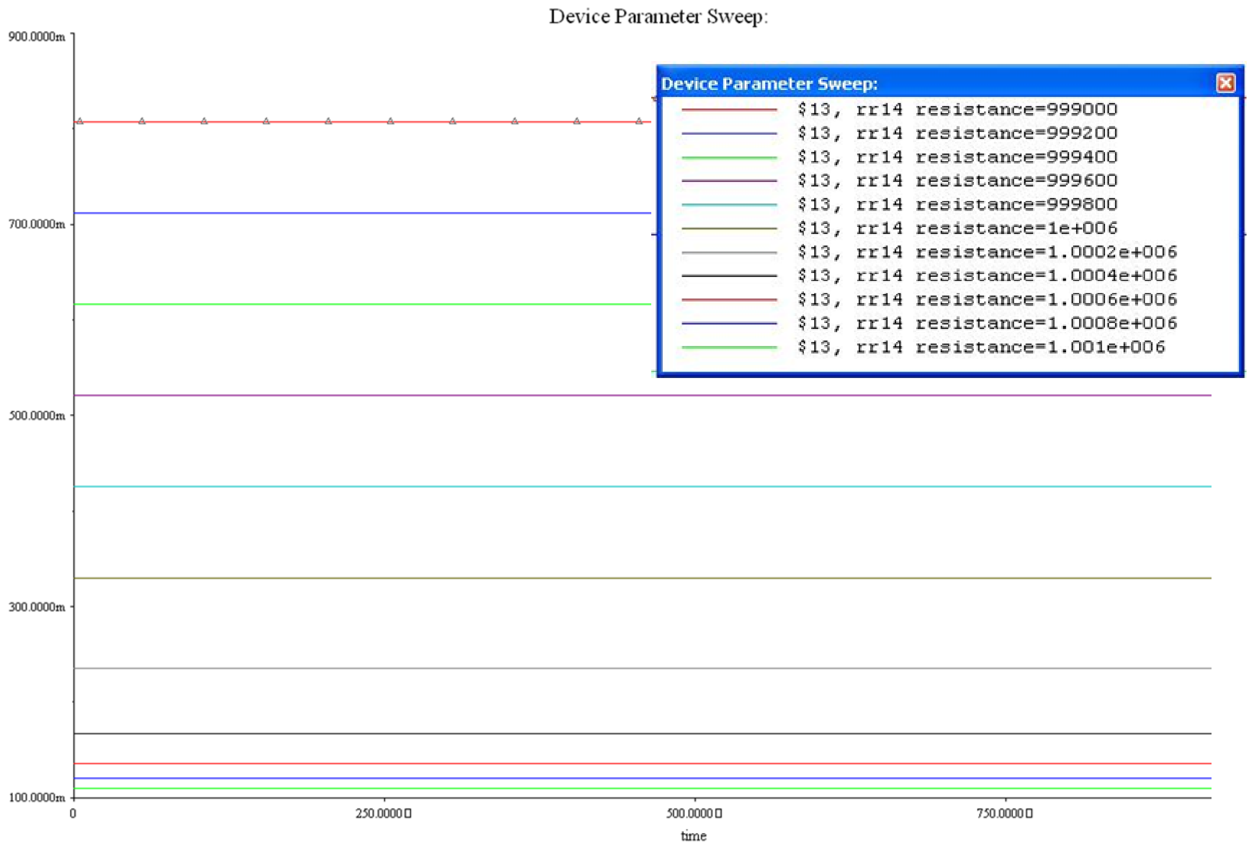


Figure 2.13 The output voltage of the current sense circuit for different values of R1.

Table 2.1 Summary of the sensitivity of the current sense circuit to changes in the value of R1.

	R1 (Mohm)	Output (Volt)	Resistor Error (%)	Output Error (%)
1	0.999	0.807	-0.1	145
2	0.9992	0.712	-0.08	116
3	0.9994	0.616	-0.06	87.2
4	0.9996	0.520	-0.04	58.1
5	0.9998	0.425	-0.02	29.1
6	1	0.329	0	0
7	1.0002	0.236	0.02	-28.2
8	1.0004	0.167	0.04	-49.2
9	1.0006	0.136	0.06	-58.6
10	1.0008	0.120	0.08	-63.5
11	1.001	0.110	0.1	-66.5

Since output error's dependence on R2 for small variations in R2's value is the same function as R1 to the simulation results are similar when the value of one of the R2 resistors is varied. The results shown in the Figure 2.14 and table 2.2 verify this. Here the required value of R2 equals 10Kohm and again the resulting output voltage is 0.329 volt.

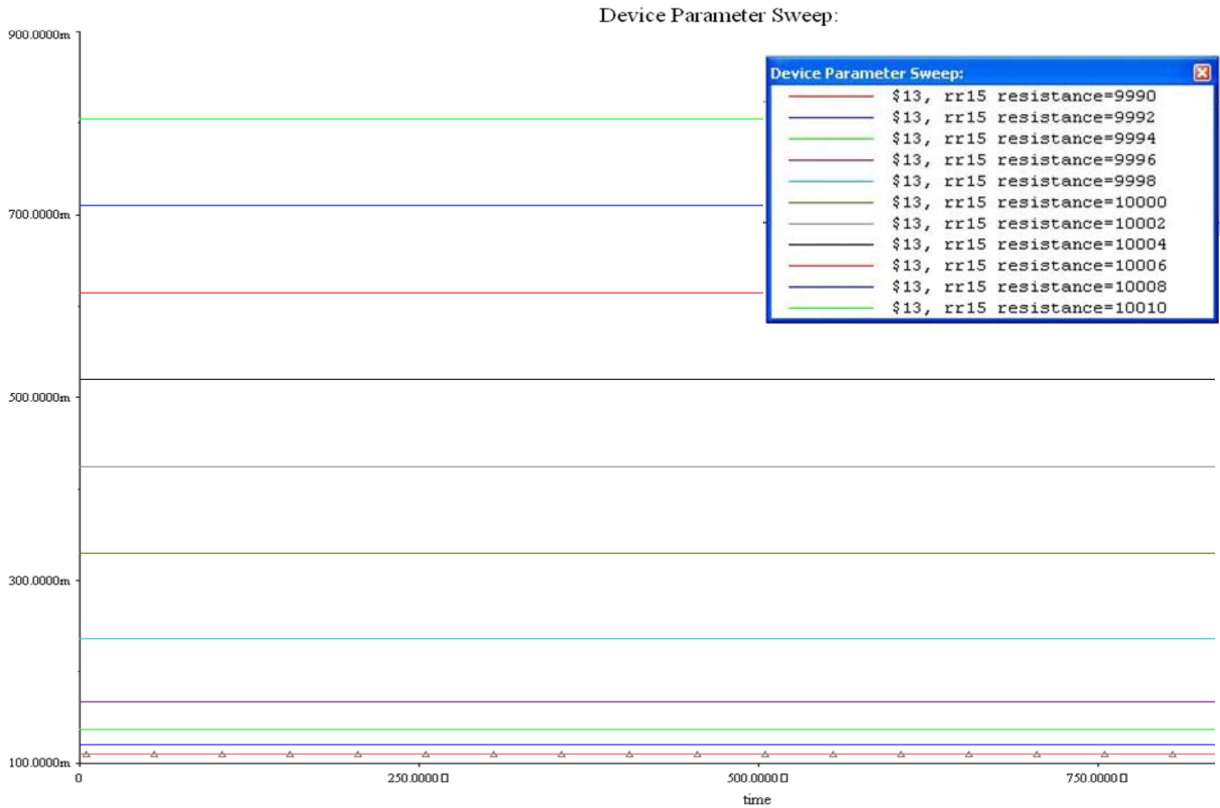


Figure 2.14 The output voltage of the current sense circuit for different values of R2.

Table 2.2 Summary of the sensitivity of the current sense circuit to changes in the value of R2

	R2 (Kohm)	Output (Volt)	Resistor Error (%)	Output Error (%)
1	9.99	0.110	-0.1	-66.5
2	9.992	0.120	-0.08	-63.5
3	9.994	0.136	-0.06	-58.6
4	9.996	0.167	-0.04	-49.2
5	9.998	0.236	-0.02	-28.2
6	10	0.329	0	0

7	10.002	0.424	0.02	29.1
8	10.004	0.519	0.04	58.1
9	10.006	0.614	0.06	87.2
10	10.008	0.709	0.08	116
11	10.01	0.804	0.1	145

With the help of Figures 2.13,2.14, and Tables 2.1, 2.2, it is clear that even a 0.02% error in the value of either resistor will cause about a 29% output error. This shows that the resistors R1 and R2 must be accurate enough so that the error resulting from voltage division of the common mode voltage is small enough.

Resistor R3 has different function from R1 and R2, and it is used to define the gain of the OP-AMP. Figure 2.15 plots the output voltage in response to the resistance change of R3, and Table 2.3 summarizes the results in Figure 2.15. Here the required value of R3 equals 1.787Mohms to obtain the desired 0.329 volt output voltage.

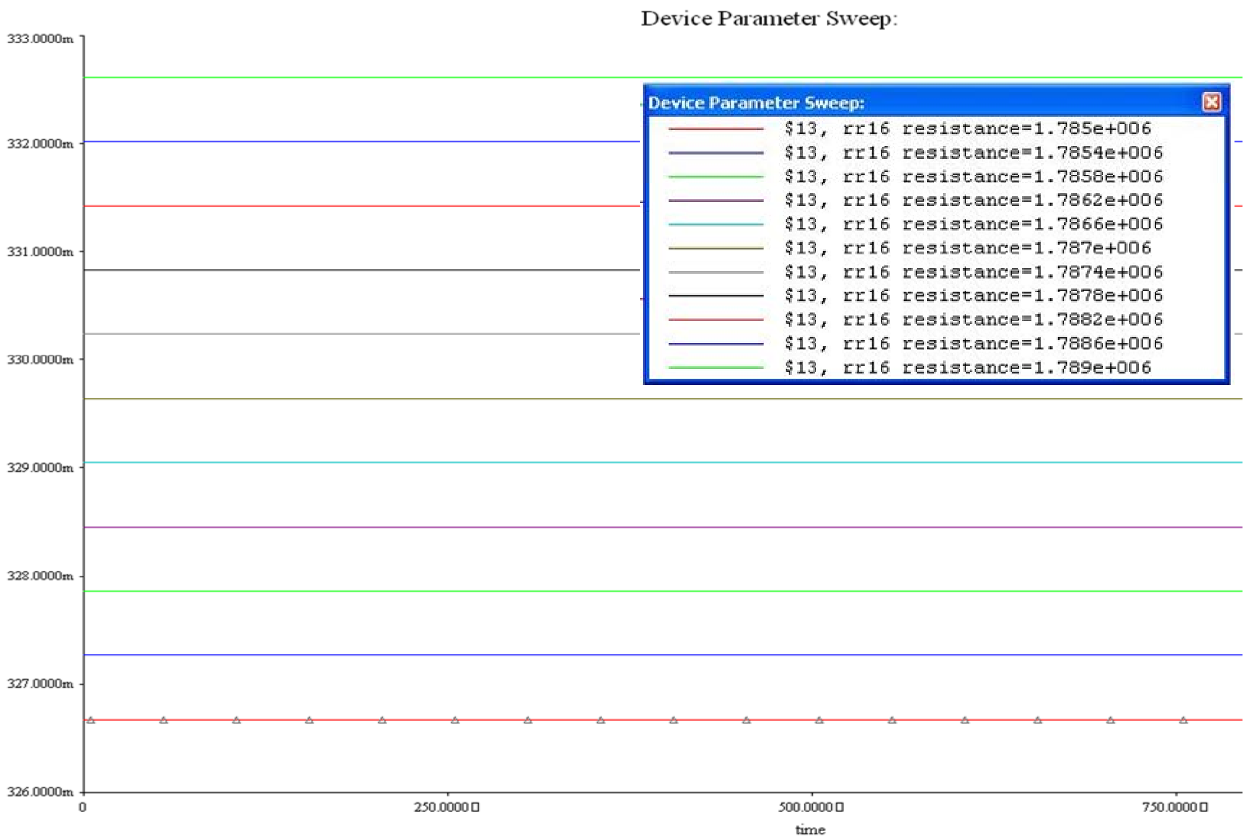


Figure 2.15 The output voltage of the current sense circuit for different values of R3.

Table 2.3 Summary of the sensitivity of the current sense circuit to changes in the value of R3

	Resistor(Mohm)	Output (Volt)	Resistor Error (%)	Output Error (%)
1	1.785	0.326	-0.1	-0.9
2	1.7854	0.327	-0.08	-0.6
3	1.7858	0.327	-0.06	-0.6
4	1.7862	0.328	-0.04	-0.3
5	1.7866	0.329	-0.02	0
6	1.787	0.329	0	0
7	1.7874	0.330	0.02	0.3
8	1.7878	0.330	0.04	0.3
9	1.7882	0.331	0.06	0.6
10	1.7886	0.332	0.08	0.9
11	1.789	0.332	0.1	0.9

Figure 4.15 and Table 2.3 demonstrate that the change in the value of the resistor R3 will not affect the output voltage much compared to changes in R1 and R2. The above results show that to obtain an accurate output voltage it is necessary to use low tolerance resistors for R1 and R2. The tolerance of R1 and R2 can be improved further by trimming their values using a small resistor in series with R1 or R2. It should be noted that if the circuit can sense the 0.15V voltage drop accurately, then it will be able to sense the 1.5V voltage drop with greater accuracy.

The circuit in Figure 2.9 was fabricated with 0.1% resistors and trimming R1 and R2 as described above. Tables 2.4 and 2.5 summarize the comparison between the simulation and experimental results for different input voltages. The simulation used the measured values of the resistors. The experimental results match the simulation results well.

Table 2.4 Simulation and experimental results versus the input (common mode) voltage with rated load current (30A) when the input voltage is 270V. The voltage drop across the

current sense resistor is 0.15V at this condition.

Common Mode Voltage	10 (V)	100 (V)	200 (V)	270 (V)
Simulation	0.2612	0.283	0.309	0.328
Experiment	0.279	0.3	0.323	0.343
Error	0.0018	0.017	0.013	0.015

Table 2.5 Simulation and experimental results versus the input voltage with 1000% rated load current (300A) when the input voltage is 270V.

Voltage Drop Results	10 (V)	270 (V)
Simulation	2.699	3.359
Experiment	2.734	3.369
Error	0.035	0.01

Another issue is that the value of the resistors will change with the temperature. The change in resistance with temperature is characterized by the resistor's temperature coefficient (labeled TC, the unit is ppm/°C). From the specification, the temperature coefficient of the resistors used in the experiment is 5 ppm/°C. The resistance change can be computed using the definition of the temperature coefficient

$$TC = \frac{\Delta R * 10^6}{R_0 * \Delta T}$$

For example, R1 is 1Mohm at 25°C, $\Delta T = 100°\text{C} - 25°\text{C} = 75°\text{C}$,

$$\Delta R = \frac{5\,ppm/°\text{C} * 10^6\,ohm * 75°\text{C}}{10^6} = 375ohm = 0.0375\%R1$$

Thus the resistance value will be 1.000375Mohm at 100°C. This change is too large for the output of the current sense circuit to be accurate. However, if the two resistors R1 or R2 have the same TC, then the output voltage will still be accurate. Table 2.6 shows the experimental result when the circuit changes from 25°C to 200°C.

Table 2.6 Experimental results Vsense changes with Temperature when the input voltage is 270VDC

Temp	25°C	47°C	60°C	84°C	113°C	131°C	160°C	200°C
Vsense	0.547	0.533	0.523	0.492	0.455	0.447	0.435	0(failed)
Error	0	2.56%	4.38%	10%	16.8%	18.28%	20.4%	N/A

The resistors R1 and R2 failed at 200°C, so Vsense and Von equals 0V. The reason for the resisitor failures is that the maximum specified operating temperature for the resistors is 150°C, and the resistor's Power Rating drop linearly above 85°C to zero at 150°C.

There are two solutions to eable the circuit to operate at high temperature,

1. Better resistors are needed than were used in the experiment, which should have low temperature coefficient and an operating temperature above 200°C.
2. Since the error is small, trim resistors should be trimmed precisely at different Temperature to get desired Von value.

2.2.5 I^2T Measurement Simulation and Test Results

The I^2T circuit turns off the SSPC main SiC JFET switch when the load current is between its rated value and 1000% of its rated load after a time duration that varies with load current so that the I^2T value of the current remains constant. A block diagram of the circuit is shown in Figure 2.16. The circuit squares the current using a multiplying digital to analog converter (DAC). In the multiplying DAC the analog DAC reference is one of the signals to be multiplied and the digital signal to be converted to analog is the other signal to be multiplied. Since one of the signals being multiplied is digital, that analog signal must be first converted to digital using an analog to digital converter (ADC).

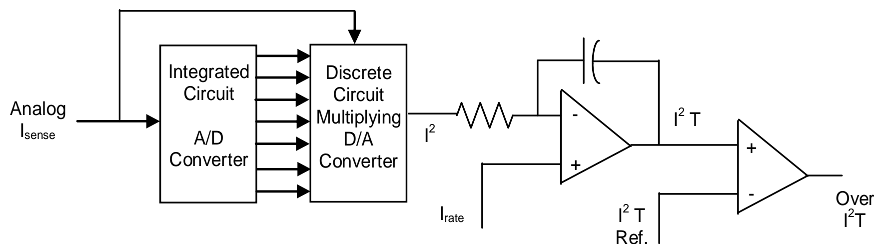


Figure 2.16 Block Diagram of the I^2T circuit.

The related current squaring circuit equations are shown below,

$$N_{digital} = 11111111 \times \frac{V_{in}}{V_{refA/D}} \tag{1}$$

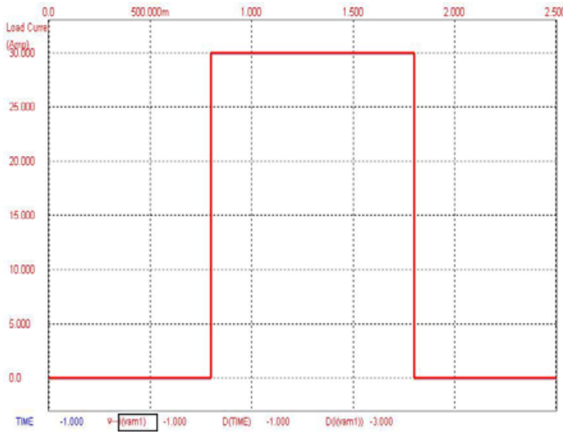
$$V_{out} = \frac{N_{digital}}{11111111} \times V_{refD/A} \qquad V_{refD/A} = V_{in} \tag{2}$$

$$V_{out} = \frac{V_{in}^{2}}{V_{refA/D}} \tag{3}$$

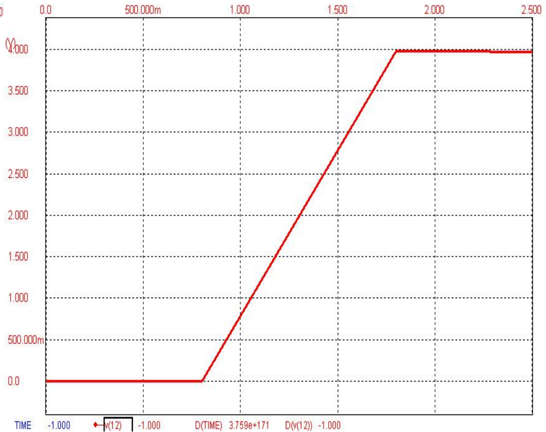
$$V_{sensor} = I\frac{R_{sensor} \times R_f}{R_{in}} \qquad V_{sensor} = V_{in} \tag{4}$$

$$V_{out} = I^2 \frac{R_{sensor}^{2} \times R_f^{2}}{R_{in}^{2} \times V_{refA/D}^{2}} = I^2 \times Gain \tag{5}$$

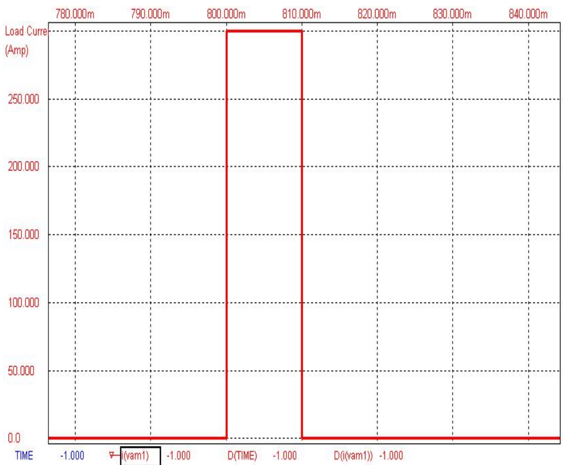
Again the design requirement that all of the components used in the circuit must be capable of operation at 200°C was imposed. A commercial ADC converter capable of operation at 200°C is available from two different venders. Thus the load current sensed by the current sensing circuit is fed into this eight-bit high temperature ADC. Unfortunately a commercial DAC capable of operation at 200°C is not available. Thus the high temperature ADC is combined with an R-2R ladder network multiplying DAC, made up of discrete components to make the I-squared circuit. This circuit was chosen because a digital circuit is inherently noise immune, fast, and 200°C ADC integrated circuits are available commercially. Also 200°C resistors and analog switches for the DAC are also available commercially. The output of the DAC is then fed into an integrator to generate the I^2T function. The I^2T signal is then compared to the scaled reference value equal to 4Vdc. When the I^2T signal exceeds 4Vdc the SSPC will trip and shutdown. This is shown in Figure 3.12 for 30A and 100A SSPC designs. This meets the trip curve requirement in Figure 2.18.



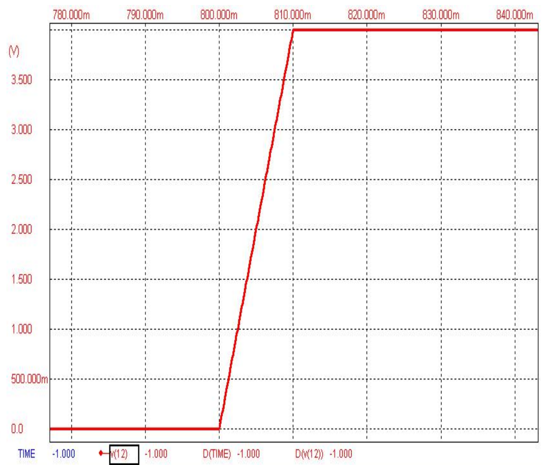
(2.17A)



(2.17B)



(2.17C)



(2.17D)

Figure 2.17 Figure 2.17A and 2.17B are I^2T simulation results at a 30A SSPC 100% load current. Figure 2.17C and 2.17D are I^2T simulation results at a 300A SSPC 1000% load current.

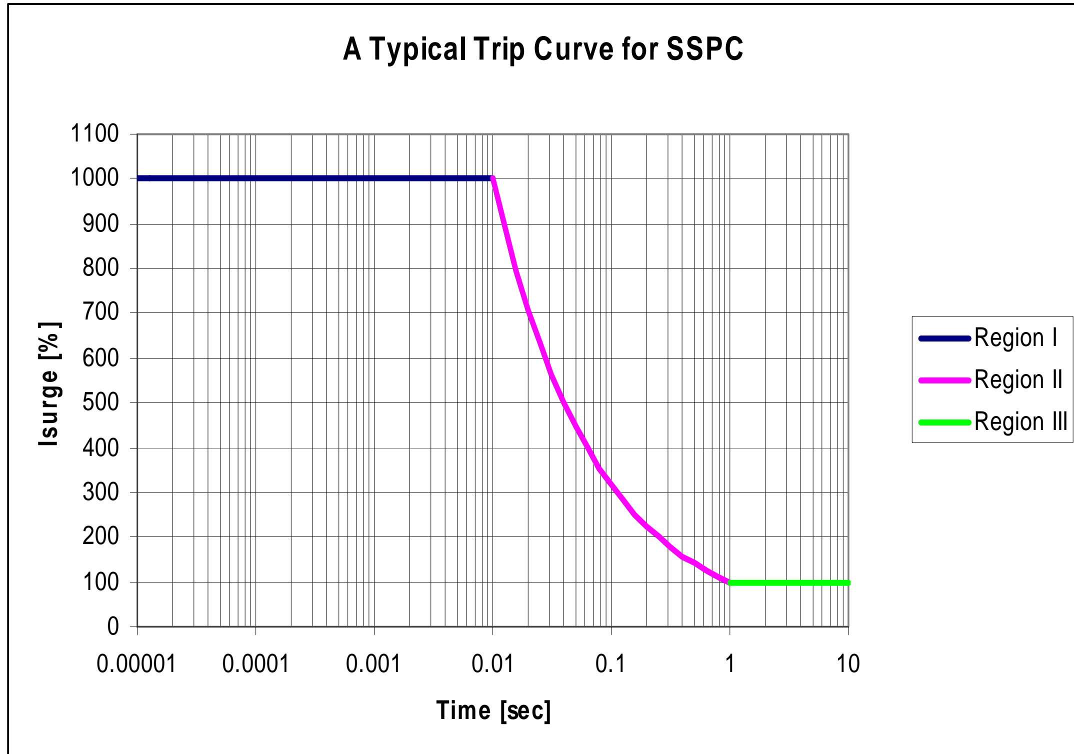


Figure 2.18 Required SSPC trip curve

Figure 2.19 shows the ADC signal definitions. The "Equiv.Output" values in Table 2.7 were computed from measurements of the ADC's binary output in order to compare the binary output to the analog input voltage. The ADC's reference voltage was measured to be 5.17 V. An analog voltage is input to the ADC and the binary output is measured. Finally, the measured binary output is converted to the "Equiv. Output" using Eq. 6.

$$Equiv.Output = \frac{Binary.Value_{measured}}{255} \times V_{ref} \tag{6}$$

Table 2.7 shows the ADC test results. It can be seen that the final error between the input and output values is about 0.3%.

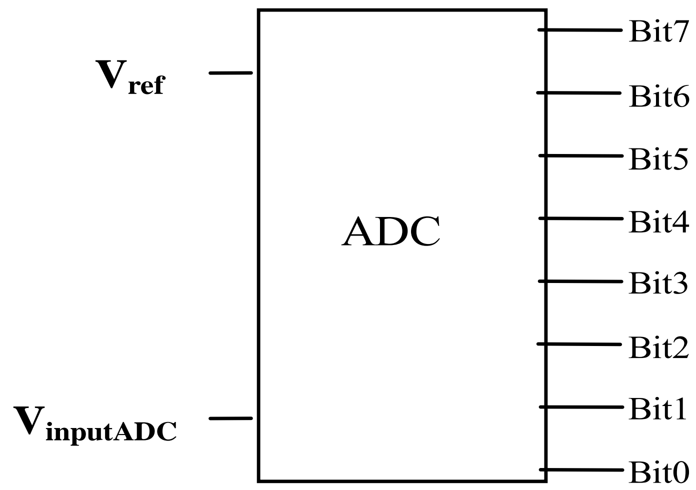


Figure 2.19 ADC schematic

Table 2.7 ADC test results and the error compared to the input value

ADC input	Bin7	Bin6	Bin5	Bin4	Bin3	Bin2	Bin1	Bin0	Dec. Value	Equiv. Output	% Error
5.17	1	1	1	1	1	1	1	1	255	5.16	0.19
4.97	1	1	1	1	0	1	0	1	245	4.95	0.27
5.11	1	1	1	1	1	1	0	0	252	5.09	0.47
4.99	1	1	1	1	0	1	1	0	246	4.97	0.45
4.87	1	1	1	1	0	0	0	0	240	4.85	0.24
4.64	1	1	1	0	0	1	0	1	229	4.63	0.34
4.56	1	1	1	0	0	0	0	1	225	4.54	0.48
4.34	1	1	0	1	0	1	1	0	214	4.33	0.32
4.24	1	1	0	1	0	0	0	1	209	4.22	0.34
4.05	1	1	0	0	1	0	0	0	200	4.05	0.24
3.97	1	1	0	0	0	1	0	0	196	3.96	0.35
3.77	1	0	1	1	1	0	1	0	186	3.76	0.29
3.63	1	0	1	1	0	0	1	1	179	3.63	0.03
3.47	1	0	1	0	1	0	1	1	171	3.46	0.34
3.12	1	0	0	1	1	0	1	0	154	3.12	0.07
3.02	1	0	0	1	0	1	0	1	149	3.02	0.10
2.90	1	0	0	0	1	1	1	1	143	2.89	0.42
2.74	1	0	0	0	0	1	1	1	135	2.73	0.37
2.62	1	0	0	0	0	0	0	1	129	2.61	0.36
2.37	0	1	1	1	0	1	0	1	117	2.37	0.30
2.27	0	1	1	1	0	0	0	0	112	2.26	0.47
2.13	0	1	1	0	1	0	0	1	105	2.11	0.79
1.97	0	1	1	0	0	0	0	1	97	1.95	0.74
1.82	0	1	0	1	1	0	1	0	90	1.81	0.92
1.62	0	1	0	1	0	0	0	0	80	1.60	1.23
1.46	0	1	0	0	1	0	0	0	72	1.45	0.67
1.36	0	1	0	0	0	0	1	1	67	1.34	1.13
1.16	0	0	1	1	1	0	0	1	57	1.15	0.75
1.07	0	0	1	1	0	1	0	1	53	1.06	1.63
0.95	0	0	1	0	1	1	1	1	47	0.94	1.35
0.77	0	0	1	0	0	1	1	0	38	0.76	0.96
0.69	0	0	1	0	0	0	1	0	34	0.68	2.08
0.61	0	0	0	1	1	1	1	0	30	0.60	2.01
0.49	0	0	0	1	1	0	0	0	24	0.48	2.18
0.41	0	0	0	1	0	1	0	0	20	0.40	2.09

The output of ADC is fed into the multiplying DAC. Here a resistor ladder

converter was chosen. Its central component is a resistor ladder network in which horizontally drawn resistors have a value of R and vertically drawn resistors have a value of 2R. This network is sometimes called an R-2R network. An 8-bit converter is shown in Figure 2.20 [22].

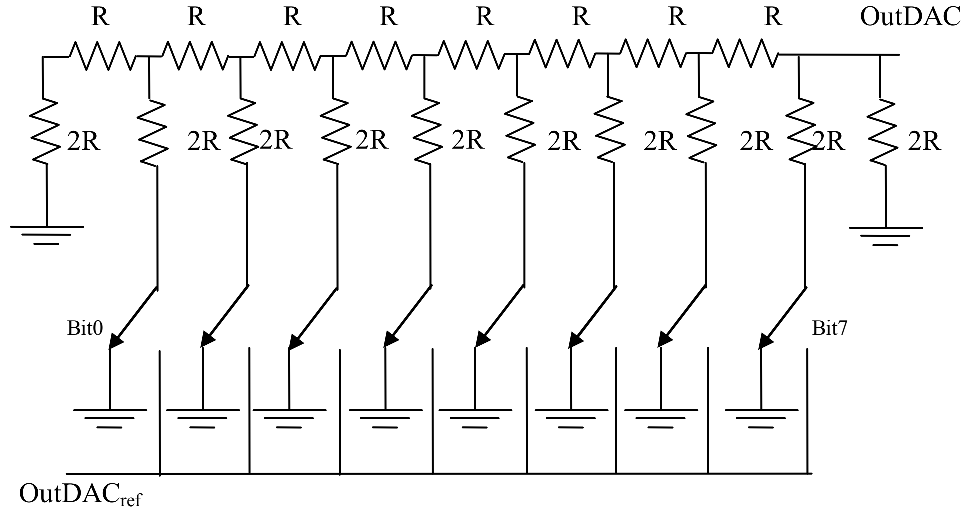


Figure 2.20 Eight-bit resistive ladder DAC

The output voltage of the circuit as a function of all the switch values is shown below [22]. Here $OutDAC_{ref}$ equals $V_{inputADC}$ and Bit_j is zero or 1.

$$OutDAC = \frac{OutDAC_{ref}}{3}\left(Bit7 + \frac{Bit6}{2} + \frac{Bit5}{4} + \frac{Bit4}{8} + \frac{Bit3}{16} + \frac{Bit2}{32} + \frac{Bit1}{64} + \frac{Bit0}{128}\right) \quad (7)$$

In Figure 2.20, 10K and 20K ohm resistors were used. The MM74HC4316 Quad Analog Switch was used for the switches. The details can be found in the Appendix. Table 2.8 summarizes the DAC test results. The variables are defined as shown below,

$OutDAC_{ex}$: The experimental results of eight-bit resistive ladder DAC. Unit is Volt.

$OutDAC_{ref}$: The reference voltage of eight-bit resistive ladder DAC, which equals to the $V_{inputADC}$. Unit is Volt.

$OutDAC_{th}$: The theoretical results of ideal eight-bit resistive ladder DAC. Unit is

Volt.

It can be seen that the DAC error between experimental and theoretical value is about 0.01%. The output of the DAC is fed into an integrator to generate the I^2T function

Table 2.8 DAC results and the error compared to the reference value

$OutDAC_{ex}$(V)	$OutDAC_{ref}$(V)	$OutDAC_{ex}/OutDAC_{ref}$	$OutDAC_{th}/OutDAC_{ref}$	Error (%)
3.43	3.43	1.00	1.00	0.01
3.16	3.29	0.96	0.96	0.01
3.34	3.38	0.99	0.98	0.01
3.18	3.30	0.96	0.96	0.01
3.03	3.22	0.94	0.94	0.01
2.76	3.07	0.90	0.89	0.01
2.66	3.01	0.88	0.88	0.01
2.41	2.87	0.84	0.84	0.01
2.30	2.80	0.82	0.82	0.01
2.11	2.69	0.78	0.78	0.01
2.02	2.63	0.77	0.77	0.01
1.82	2.50	0.73	0.73	0.01
1.69	2.41	0.70	0.70	0.01
1.54	2.29	0.67	0.67	0.01
1.25	2.07	0.60	0.60	0.01
1.17	2.00	0.58	0.58	0.01
1.08	1.92	0.56	0.56	0.01
0.96	1.81	0.53	0.53	0.01
0.88	1.73	0.51	0.50	0.01
0.72	1.57	0.46	0.46	0.01
0.66	1.50	0.44	0.44	0.01
0.58	1.40	0.41	0.41	0.01
0.49	1.30	0.38	0.38	0.01
0.42	1.20	0.35	0.35	0.01
0.33	1.06	0.31	0.31	0.01
0.27	0.96	0.28	0.28	0.01
0.23	0.89	0.26	0.26	0.01
0.17	0.76	0.22	0.22	0.01
0.15	0.70	0.21	0.20	0.01
0.12	0.62	0.18	0.18	0.01
0.08	0.51	0.15	0.15	0.01
0.06	0.45	0.13	0.13	0.01
0.05	0.40	0.12	0.12	0.01
0.03	0.32	0.09	0.09	0.01
0.02	0.26	0.08	0.08	0.01

2.2.6 Control Logic

The SSPC's control logic contains an R/S (reset/set) latch to latch an over I^2T fault, over-current fault, or over temperature condition. Thus the R/S latch stores the status of the JFET switch [15,16]. Like the other control circuits, the design goal was to implement the R/S latch using components that could operate at 200°C. The R/S circuit is shown in Figure 2.21. Under normal operating conditions without a fault R, S, and Q are low, a logic zero.

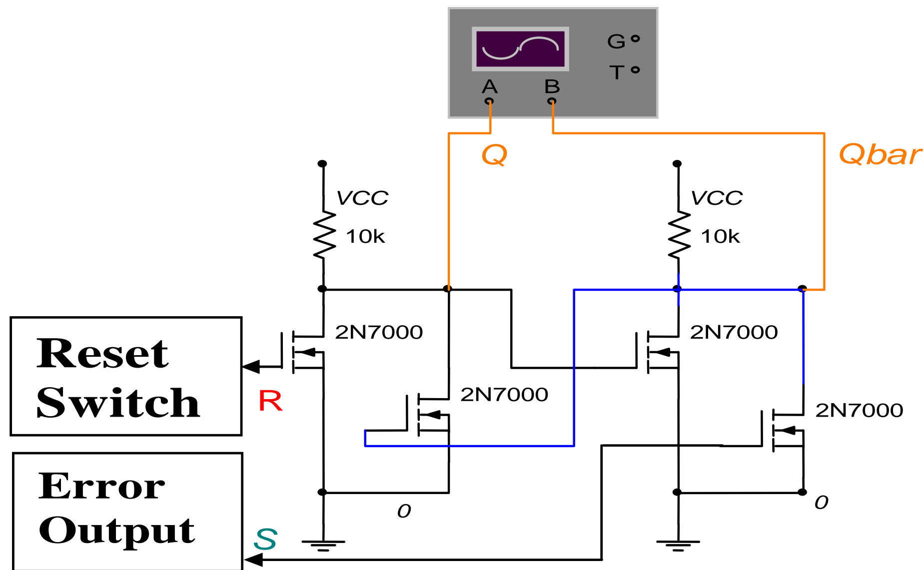


Figure 2.21 The R/S control logic circuit

Table 2.9 R/S latch output and relationship to the switch status

	R	S	Q	Qbar	status
Power up	0	0	x	x	Power up state is unknown
Reset	1	0	0	1	Reset circuit
Normal operation	0	0	0	1	On
Fault occurs	0	1	1	0	Turn off
Switch turns off	0	0	1	0	Off
User resets	1	0	0	1	Turn on
Normal Operation	0	0	0	1	On

First, the circuit was locked out and can be turned on by pressing RESET button as shown in Figure 2.22. As noticed, the reset signal turned from 1 to 0 immediately to enable the main JFET switch to turn “ON”.

If a fault occurs the R/S latch’s set input goes high so R=0, S=1, and thus Q goes high (Q=1, Qbar=0). When Q goes high it causes the SiC JFET switch to be turned off eliminating the fault current and causing the set input to the R/S latch to return to zero. The latch output remains high (stores a fault occurred) and the SiC JFET switch remains off. Thus the set input remains high only long enough to turn the SiC JFET off as shown in Figure 2.23. Once the cause of the fault has been corrected the user can make the reset high with the set input remaining low (S=0, R=1). The Q output goes low turning the SiC JFET switch back on.

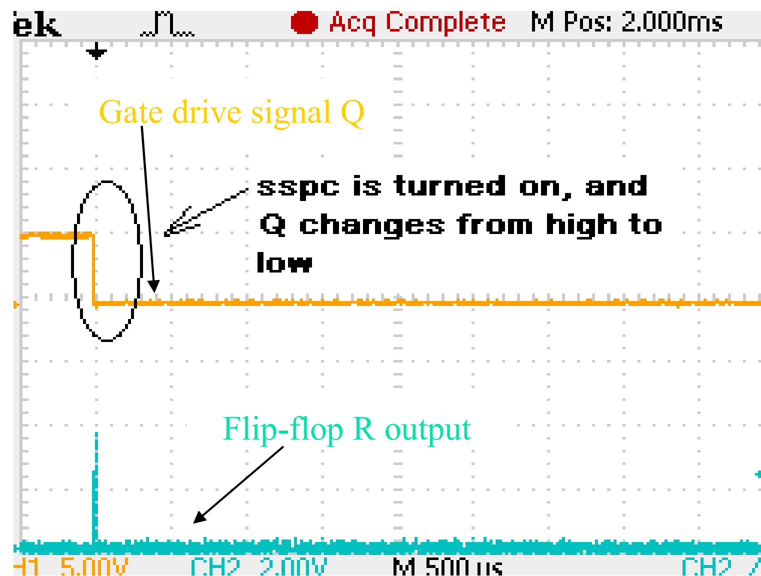


Figure 2.22 Measured Gate drive signal Q responding to the RESET signal

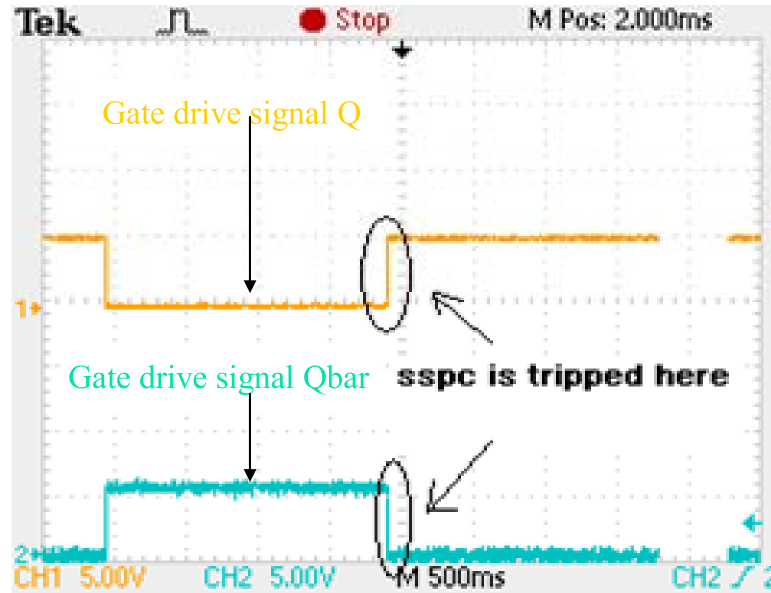


Figure 2.23 The Q and Qbar outputs when the SSPC is turned off due to a fault condition.

The R/S latch's outputs Q and Qbar have opposite values all the time and they control the turn on/off of the SiC JFET's gate drive signal shown in the section on the gate drive.

Chapter3 Power Switch Requirements

3.1 Introduction

For the SiC JFETs used in the SSPC, it is necessary to insure that their temperature rise during the single event transient faults it is protecting against stays below the maximum permissible value. Thus their junction temperature must be computed under transient operating conditions. To insure that the calculated transient behavior of the SiC JFETs is correct it is necessary to characterize the experimental SiC JFETs under transient operating conditions.

The presently available SiC devices are experimental devices that have not been fully characterized. Being experimental devices they are much more expensive and much less available than Si devices, so that Si devices were tested first to develop the test

methods for characterizing the SiC JFETs thermally. Also, Si devices have been fully characterized by their manufacturers so that the thermal performance of Si devices is available in their specification and this information can be used to verify the thermal models and measurement methods developed. Once the modeling and the measurement methods are correct for the Si devices they can be applied to SiC devices. In this research, IRF360LC Power MOSFETs from IR were tested, the details about IRF360LC Power MOSFET is shown in next section 3.2.

3.2 Measurement of the Transient Thermal Response of a Si MOSFET

Thermal resistance of a semiconductor switch is a very important parameter for characterizing semiconductor thermally under both transient and steady state condition. The electrical power consumed by semiconductor devices is converted into heat, which in turn causes a rise in the temperature of the semiconductor devices. Semiconductor devices can only operate within a limited range of junction temperatures. A primary concern in the SSPC is to not exceed the maximum junction temperature of the power semiconductor switch in order to prevent failures of the switch.

The semiconductor's thermal resistance is used to compute the temperature rise of the semiconductor from its electrical power dissipation assuming steady state thermal conditions exist. This approach is based on the mathematical analogy between the conduction of heat and the conduction of electricity or charge. While the fine details are omitted here, the analogy between a thermal system and an electrical one is obtained by substituting heat (or power) for current, temperature for voltage, and thermal resistance for electrical resistance. In other words, we have the following equations:

$$V = R \times I \tag{3.1}$$

$$\Delta T = T_{junction} - T_{case} \tag{3.2}$$

$$\Delta T = Heat(Power) * R_{\theta jc} \tag{3.3}$$

$$R_{\theta jc} = \frac{\Delta T}{Heat(power)} = \frac{\Delta T}{V \times I} = \frac{T_{junction} - T_{case}}{V \times I} \tag{3.4}$$

Hence, the units of thermal resistance are °C/W. Moreover, θ subscript is used to indicate that a given resistance is a thermal resistance rather than an electrical resistance. The thermal resistance between 2 points is indicated using subscript; for example, $R_{\theta ja}$ means thermal resistance between a semiconductor's junction and the ambient air. Thus we have the following equations:

$$R_{\theta ja} = R_{\theta jc} + R_{\theta ca} \tag{3.5}$$

Here the notation is that the thermal resistance from the junction to the ambient is equal to the sum of the thermal resistance from the junction to the case and the thermal resistance from the semiconductor package's case to the ambient.

In order to characterize the Si or SiC devices thermally, the method to measure thermal resistance for the steady state condition and the effective or transient thermal impedance for a transient condition experimentally needs to be developed. According to Eq.3.4, power dissipation, case temperature and junction temperature need to be measured to determine the thermal resistance. The power dissipated in the DUT is measured by transiently measuring the voltage across the DUT and the current through the DUT and multiply these two measured waveforms by instant to obtain a power waveform. The DUT's case temperature is measure with a thermal couple which is adequate since the case temperature changes slowly with time and is readily accessible. The junction temperature is measured by taking advantage of the fact that the on-resistance of any FET increases essentially proportional to temperature as its junction temperature increases. If the current through the FET is constant, the voltage drop across the FET also increases proportional to temperature and is thus proportional to junction temperature.

Figure 3.1 shows the schematic of the test circuit used to measure the power dissipation and on resistance for the Si or SiC devices. It consists of two IGBTs, two high-speed diodes and an inductor. The device under test (DUT) is placed in series with the lower IGBT at ground potential and is continuously gated on. Being at ground potential simplifies the connection to the oscilloscope and being continuously gated on insures there is never a large voltage across the device that is too large for the oscilloscope to measure at the scale required to observe the on-device voltage. The circuit generates a constant pulse current plus a small amount of ripple that goes through the

device under test (DUT) from drain to source. The duration and magnitude of the current pulse are set by the user. The current is regulated with a feedback control circuit. Figure 3.2 shows a typical Spice simulation result for a test circuit current pulse. The pulse current waveform in Figure 3.2 has a peak value of 31A, and the ripple current is much smaller compared to the pulse current and is ignored.

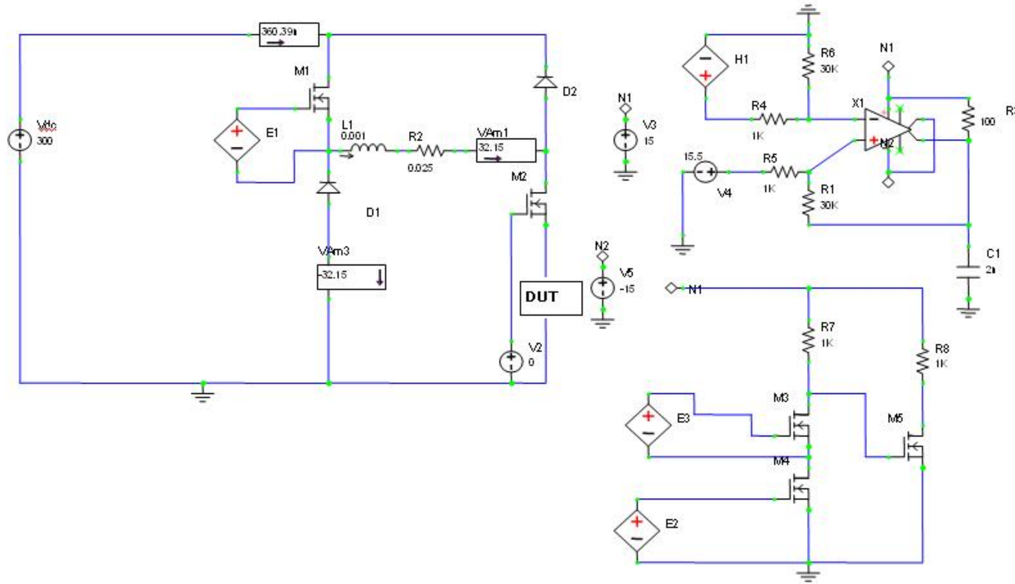


Figure 3.1 Schematic of the transient thermal response test circuit.

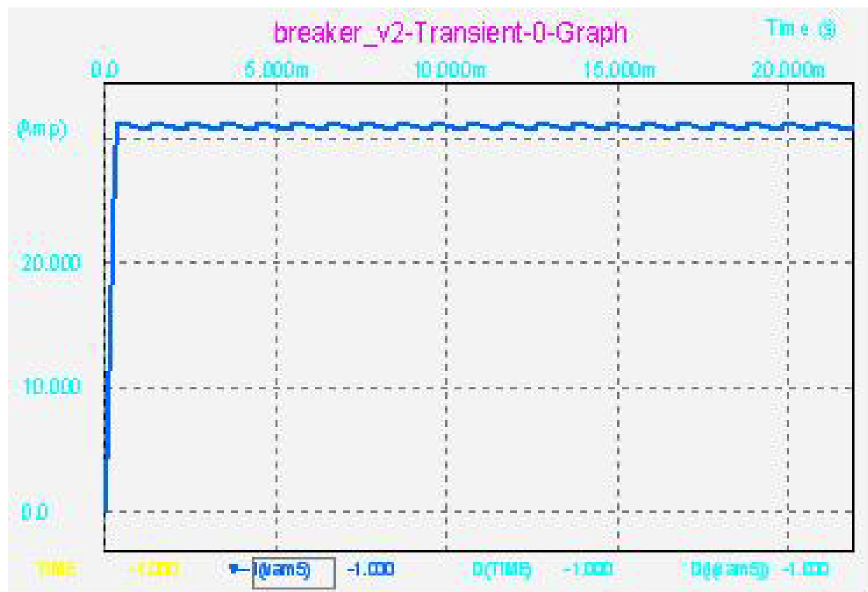


Figure 3.2 Typical test circuit transient current pulses with current 31A.

Figure 3.3 shows the experimental transient thermal response test circuit. A current sensor controls the current through the inductor using hysteresis current control. At the beginning of a current pulse both IGBTs are turned on. If the inductor current is less than the commanded current, both the upper and lower IGBTs are turned on. If the current is higher than the commanded current, the upper IGBT is turned off while the lower IGBT in series with the DUT remains on. The current sensor is a Hall affect type and its details specification is in the Appendix. The current sensors scale is 10 mV out per 1 Ampere turn. Both the number of the turns through the sensor and the current per turn determine the output voltage of the current sensor. In the circuit, 5 volt is chosen as reference voltage for the control circuit. The desired the current value can be achieved by changing the number of the turns through the sensor. For example, if the number of the turns is 20, the current will be regulated to a value of

$$I = \frac{5V}{10^{-2}\frac{V}{A}\times 20} = 25A$$

Since pulse currents with different time durations are needed, a monostable multivibrator or one-shot is used to establish the desired pulse width. At the end of the puse both IGBTs are turned off forcing the inductor current to free wheel through the two diodes to zero. Note that when the lower IGBT turns off the current in the DUT goes to zero even though the current in the inductor takes some time to go to zero. There are numerous available one-shot chips in the market. The dual retriggerable monostable multivibrator 74AHC123A chip was chosen for the experiment. The specification for the chosen one-shot can be found in the Appendix. The gate drive signal pulse width can be changed by connecting different value capacitors to the chip.

For the upper IGBT, the high side gate driver circuit was designed using the versatile fiber optic transmitter-receiver pair HFBR-0501. The details about fiber optic kit can be found in Appendix. It is suitable for solving voltage isolation problems.

In the experimental circuit, IGBTs are chose instead of the MOSFETs used in the simulation because Si IGBT modules rated to carry much higher currents than

required for the tests conducted are readily available and thus make the circuit very reliable. The main disadvantage of an IGBT is that it has slower switching speed than a MOSFET. This is not a concern in the transient thermal response test circuit because the switching time of an IGBT is much less than any of the thermal time constants.

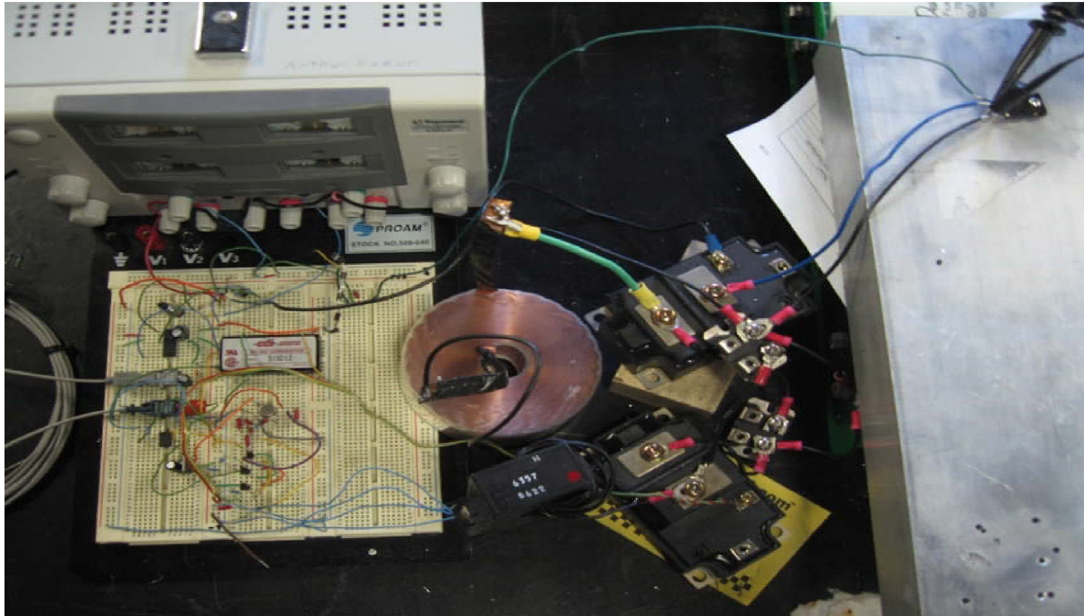


Figure 3.3 Experimental transient thermal response test circuit used for both Si and SiC devices

Figure 3.4 shows the experimental results for a Si MOSFET. The lower waveform is the measured constant current pulse I_{ds} and the upper waveform is the voltage drop V_{ds} across the device under test (DUT). The measured pulse current in Figure 3.4 matches the simulated pulse current in Figure 3.2. The transient on resistance of the DUT can be computed by dividing V_{ds} by I_{ds}. Figure 3.5 shows the computed on resistance for the Si MOSFET for times less than 4 second.

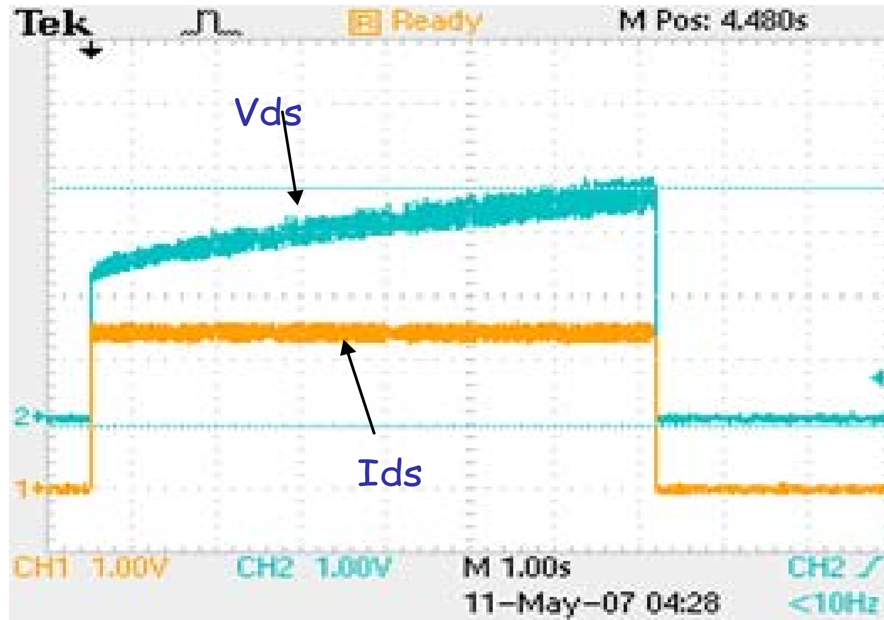


Figure 3.4 Measured 23 A current pulse (Ids 10 A/div) and device voltage drop (Vds 1 V/div) for a 6.5 s current pulse.

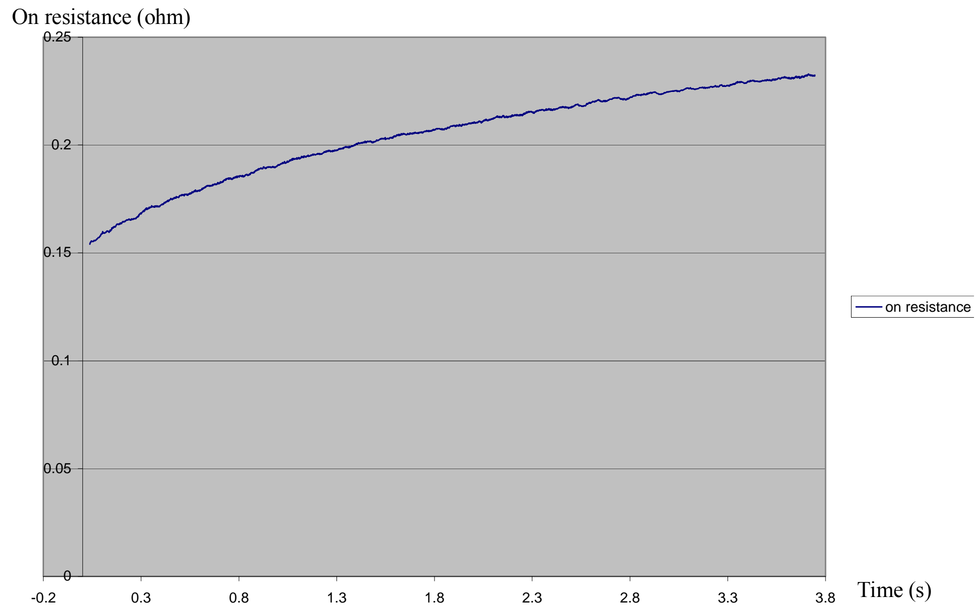


Figure 3.5 Computed on-resistance for the Si MOSFET for times less than 3.8 second

The Si device's specified on resistance versus junction temperature curve is shown in Figure 3.11. Note that the on-resistance is doubled at 110°C from its 25°C value. As shown is Table3.1, the maximum current is 23 A with the case at 25ºC and the

maximum allowed junction temperature is 150ºC due to the Silicon material property. Figure 3.12 shows the effect the case temperature has on the maximum allowed drain current.

The curve in Figure 11 was fit the following equation.

$$R(T_j) = R(T_{jo})\left(\frac{T_j}{T_{jo}}\right)^{\nu} \tag{3.6}$$

The temperatures in Eq. 3.6 should be in degrees Kelvin. Here T_{jo} is room temperature, $R(T_{jo})$ is the FET on-resistance at room temperature junction temperature, Tj is the junction temperature, R(Tj) is the FET on-resistance at Tj and ν is an empirical parameter to be calculated. After computing ν from the data in the MOSFET specification, the junction temperature T_j can be calculated from the measured on resistance using Eq.3.7

$$Tj = T_{jo}\left(\frac{R(Tj)}{R(T_{jo})}\right)^{\frac{1}{\nu}} \tag{3.7}$$

Figure 3.6 is a plot of the computed junction temperature for the Si MOSFET for the measured on-resistance data in Figure 3.5.

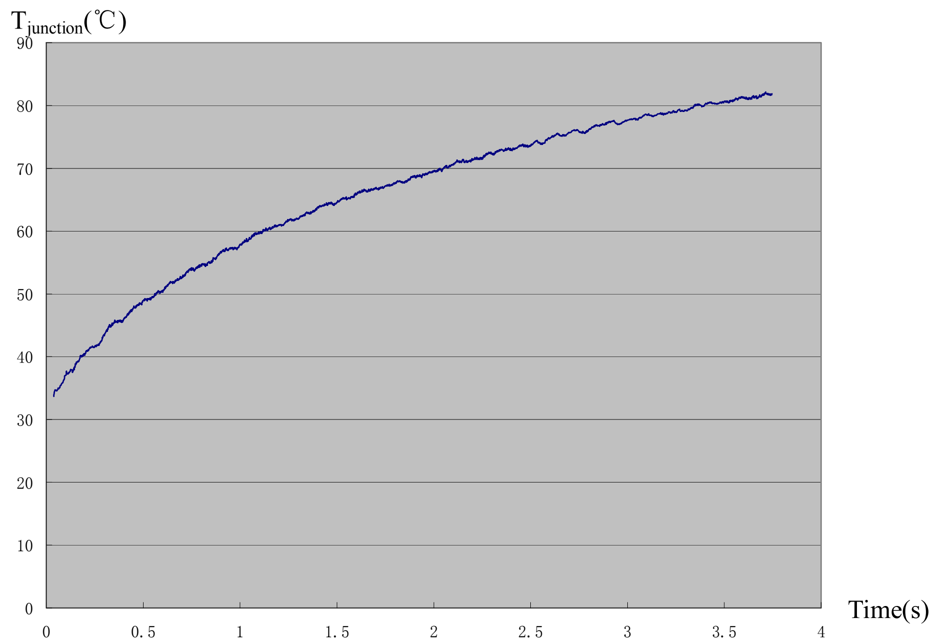


Figure 3.6 Computed T_j for the Si MOSFET data in Figure 3.5

According to Eq. 3.4, the transient T_{case}, which also increases due to power dissipation in the Si or SiC devices, must also be measured. The Si or SiC device was mounted on the heatsink and thermal couple was attached to the bottom of the device through a hole in the heatsink by using the insulated screw. The output of the thermal couple is voltage. Figure 3.7 shows the circuit designed to measure the case temperature of the Si or SiC device by measuring the thermocouple voltage. When the temperature changes from 25℃ to 225℃, the thermal couple output voltage changes from 0.96 mV to 9.1 mV. The values of thermocouple voltage are too small to be captured accurately directly measuring the thermocouple voltage with an oscilloscope. Thus the amplifier circuit in Figure 3.7 with a gain of 100 was connected to the thermal couple and the output of the amplifier was fed into the oscilloscope.

Figure 3.8 shows the experimental thermocouple voltage and MOSFET drain to source voltage. The thermocouple voltage can be converted to temperature using the thermal couple temperature versus thermocouple voltage table. Figure 3.9 shows the converted case temperature with unit of ℃. Its value is less than junction temperature and the temperature rise can be calculated by subtracting T_{case} from T_j.

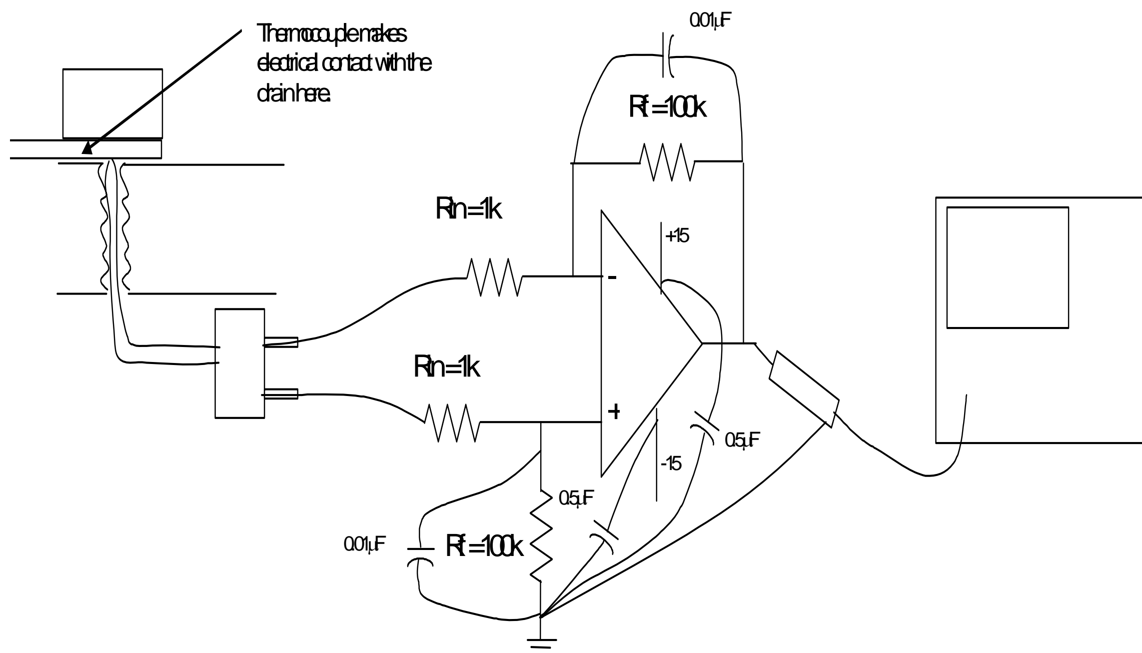


Figure 3.7 Case Temperature Measurement Circuit

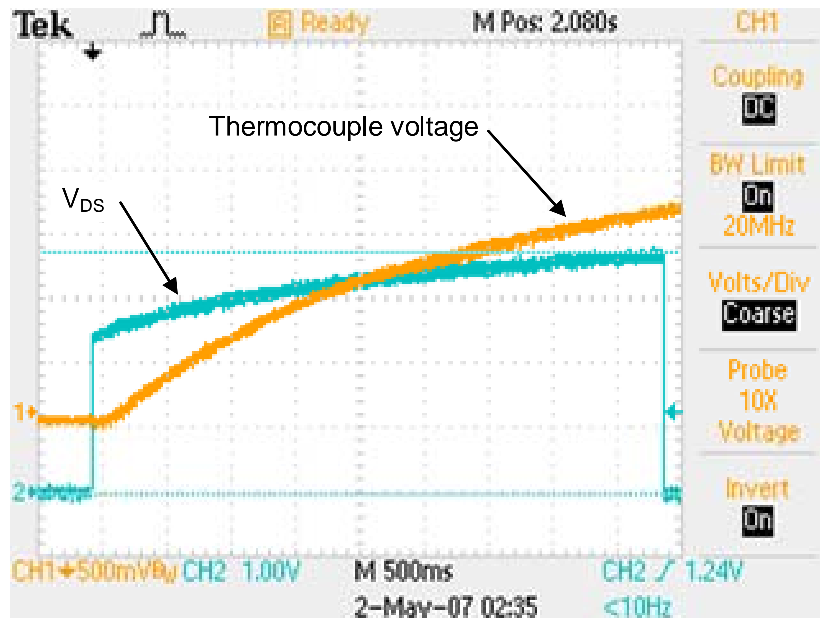


Figure 3.8 Measured thermal couple voltage and MOSFET drain to source voltage with a constant pulse current

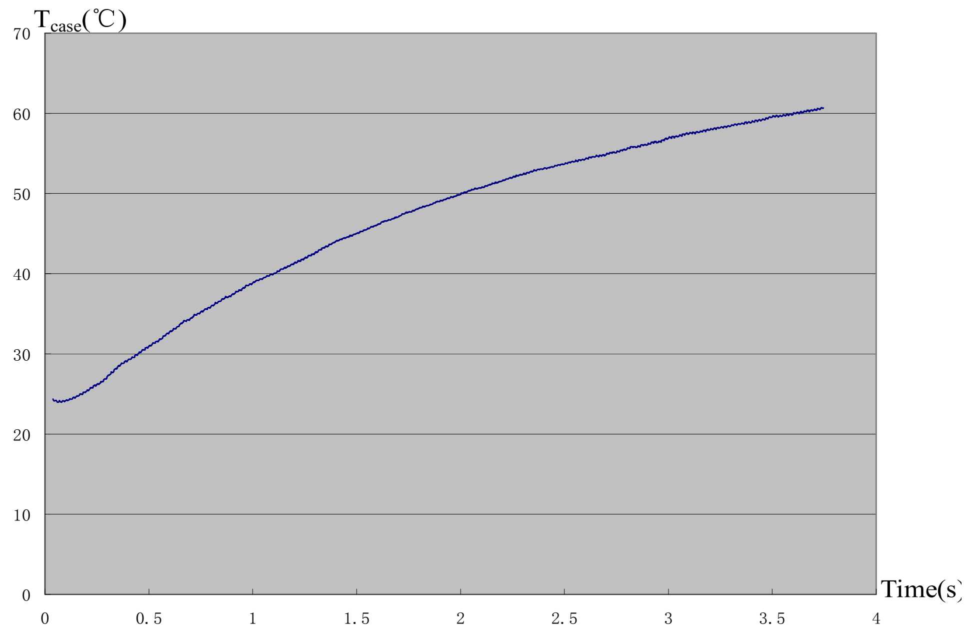


Figure 3.9 Case temperature converted from measured thermal couple output

After measuring T_{case}, T_j, V_{ds} and I_{ds}, the transient thermal resistance can be computed using Eq.3.4 as shown in Figure 3.10. The thermal resistance in Figure 3.10 was calculated from data taken with different current pulse widths. The MOSFET

manufacturer's (International Rectifier (IR)) data is also shown in Figure 3.10 for comparison. The measured data is repeatable for different current pulse widths though measured thermal resistance increases faster than the manufacturer's results do. The experimental results are in general agreement with the manufacturer's data so that the developed method for measuring the transient thermal response of the FET is ready to be applied to SiC devices.

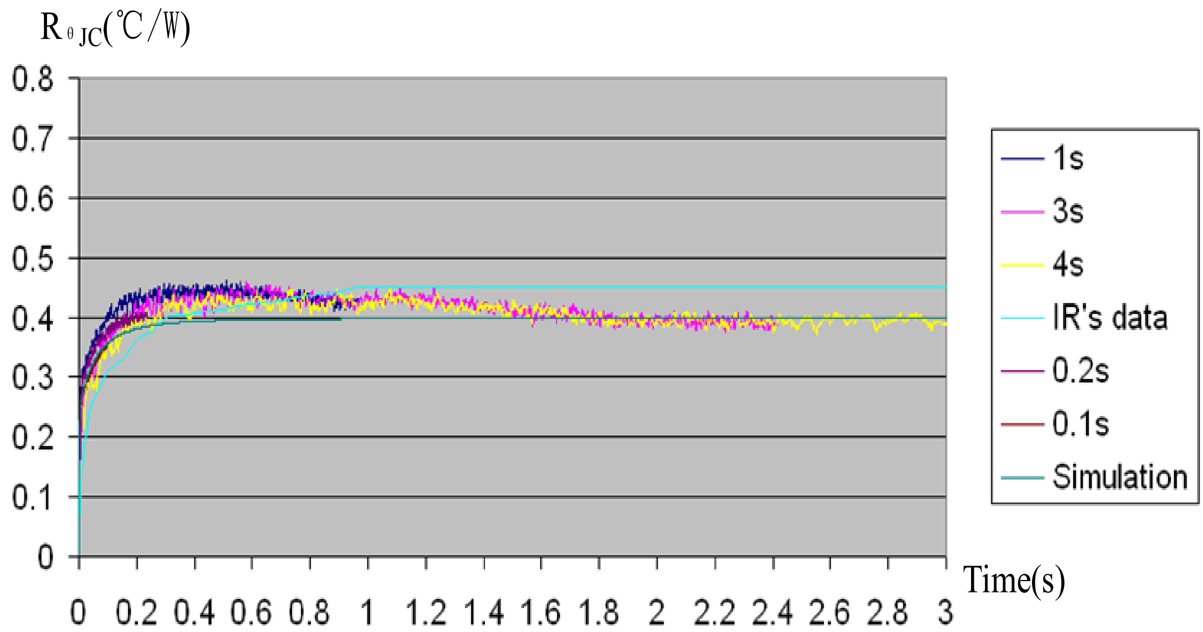


Figure 3.10 Measured transient thermal resistance under different time scales and compared to IR's data (IR only gives maximum thermal resistance).

Table 3.1 Power IRFP360LC MOSFET specification and maximum ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	23	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	14	
I_{DM}	Pulsed Drain Current ①	92	
P_D @T_C = 25°C	Power Dissipation	280	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy ②	1200	mJ
I_{AR}	Avalanche Current ①	23	A
E_{AR}	Repetitive Avalanche Energy ①	28	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Table 3.2 Thermal Resistance of Power MOSFET IRFP360LC

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	——	0.24	——	
$R_{\theta JA}$	Junction-to-Ambient		——	——	40

Table 3.2 shows the values of thermal resistance from junction to case and from case to heatsink, $R_{\theta JC}$ were used in Figure 3.10 to compare with experimental results.

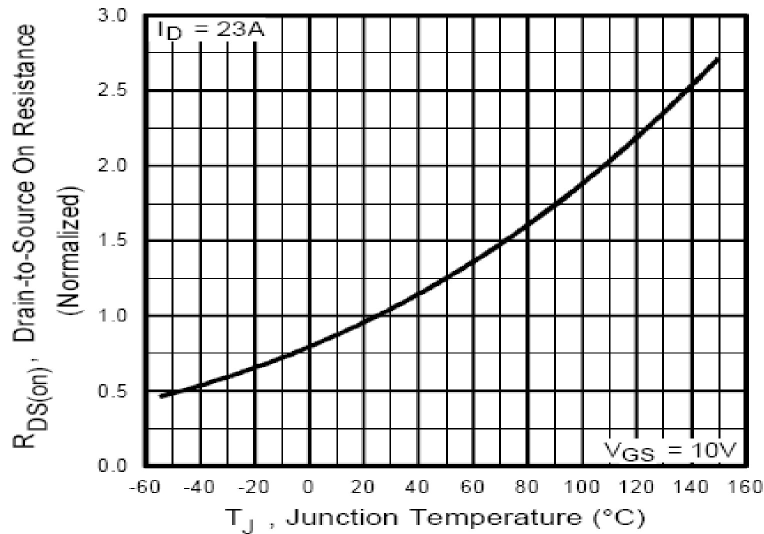


Figure 3.11 Normalized On-ResistanceVs. Temperature

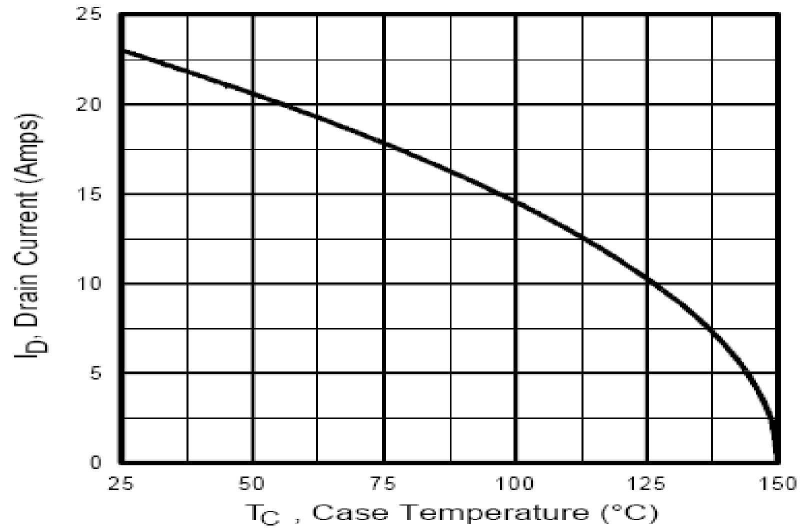


Figure 3.12 Maximum Drain Current Vs.Case Temperature

3.3 SiC JFET Power Switch Modeling

The performance of a SSPC is limited by the maximum junction temperature of its power semiconductor switch. Because the SSPC's over current requirement is a transient requirement, it is necessary to measure and compute the junction temperature of the power semiconductors under transient conditions. The complete steady state thermal schematic of a SiC power switch proposed for the SSPC mounted to an aircraft surface is shown in Fig. 3.13. Note that the switch is made up of multiple SiC JFET modules in parallel though only one module is shown in Figure 3.13 for simplicity and there are multiple SiC JFET chips in parallel within a module. As shown, the internal structure of SiC power module is made up of the SiC JFET, a thermally conducting BeO insulator, and a CuW module base. Multiple modules are mounted to a common Cu switch base. The SiC is soldered to the BeO, which is soldered to the CuW making a module. Multiple modules are then soldered to the Cu to make a switch. Each solder joint is made with a solder with the appropriate melting temperature. Finally the switch's Cu base is bolted to the aircraft surface. The heat that is generated at the junction of JFET flows from the device's junction at the top surface of the SiC chip where the power is dissipated through the internal structure of the device until it reaches the aircraft mounting surface which is assumed to be a constant temperature (infinite heatsink). Four chips are shown in each

module for simplicity even though it is presently anticipated that there will be 8 chips per module.

Figure 3.14 shows the multi-module switch thermal circuit, which is equivalent to two single module thermal circuits in parallel. Two modules are shown in parallel for simplicity even though it is anticipated that there will be 3 modules in parallel. The value of the switch thermal resistance depends on the number of SiC chips per module ($N_{JFET_per_mod}$) and the number of modules (N_{mod}). Heat capacity must also be taken into account for the switch thermal system because of the transient nature of the fault requirement. Taking into account the reduced temperature of the SiC JFET junction under transient thermal conditions due to the heat capacity of the switch's internal structural components will allow the design of a smaller and less expensive (fewer SiC chips in parallel) SSPC than could be done with only a steady state thermal analysis. The final thermal model of the SSPC power switch is shown in Figure 3.15.

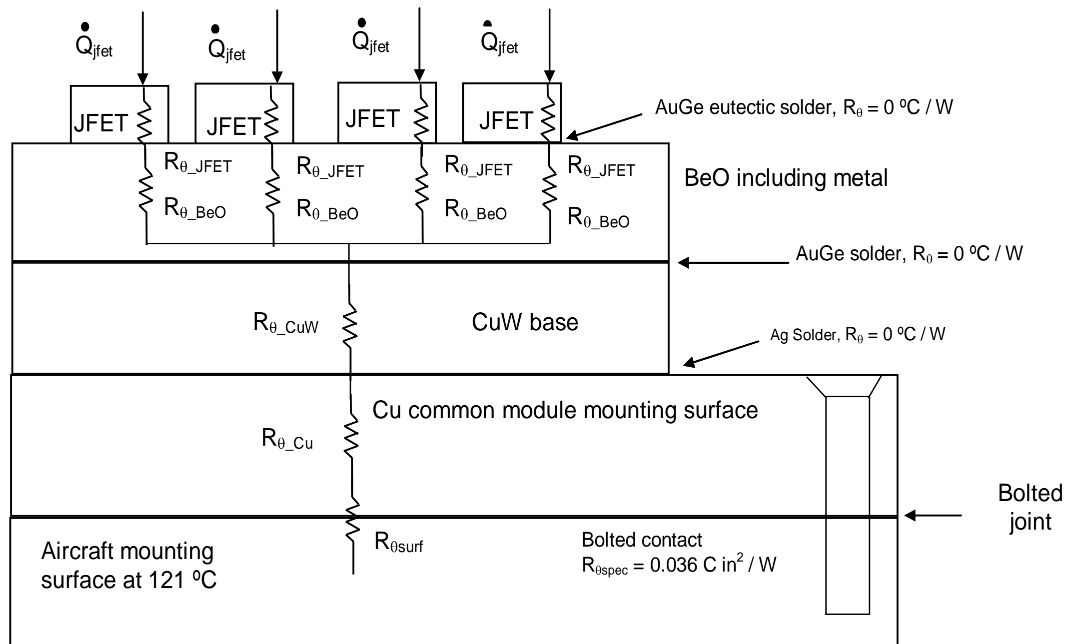


Figure 3.13 Single Module Thermal Circuit

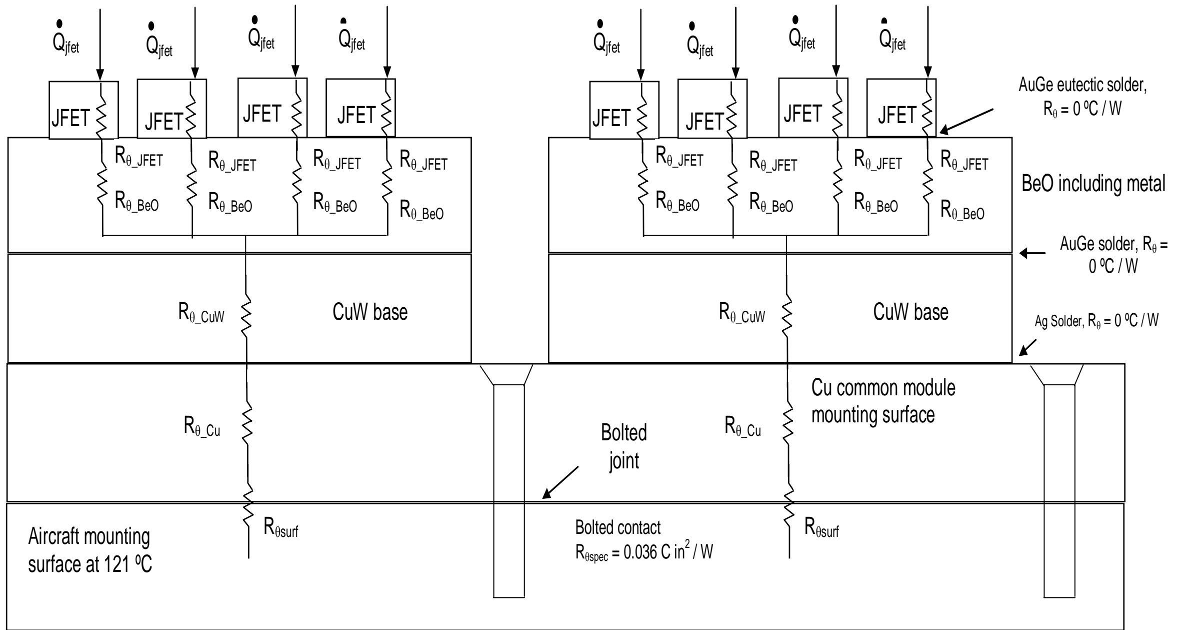


Figure 3.14 Multi Module Thermal Circuit

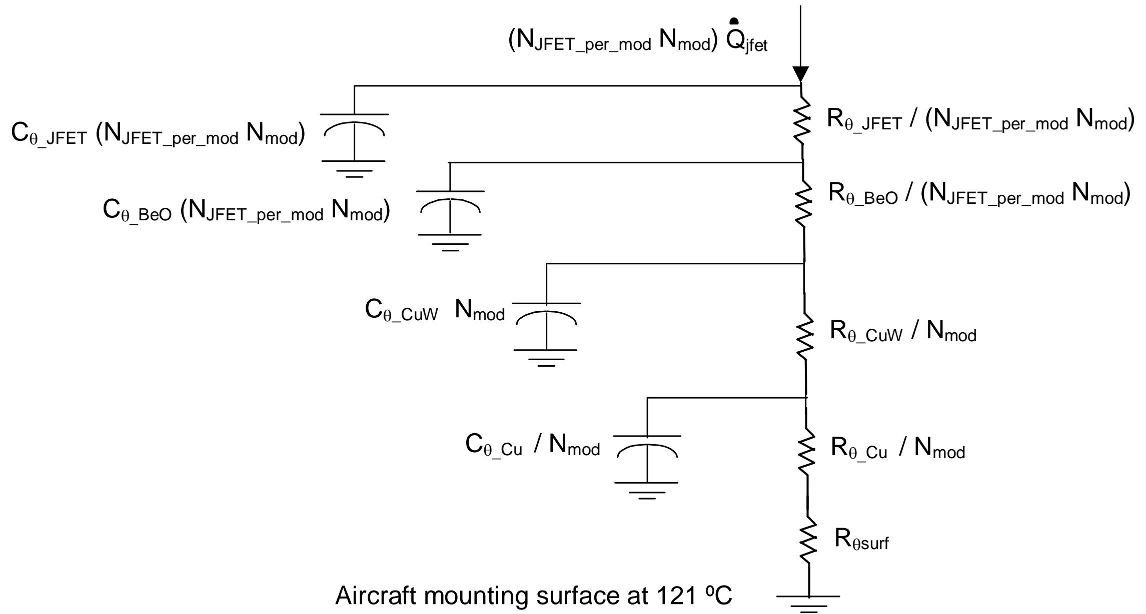


Figure 3.15 Multi Module Transient Thermal Circuit

The present concept for the SSPC switch module is shown in Figure 3.16. The module has eight chips in parallel ($N_{JFET_per_mod}$=8). The present concept for the SSPC

power switch, shown in Figure 3.17, consists of three SSPC modules in parallel (N_{mod}=3). All of these contribute to increasing the current carrying capability of the switch compared to a single module with one chip.

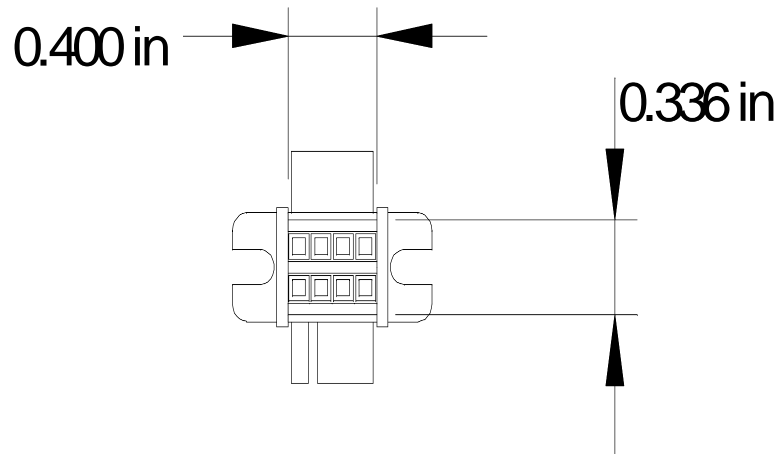


Figure 3.16 SSPC power switch module concept

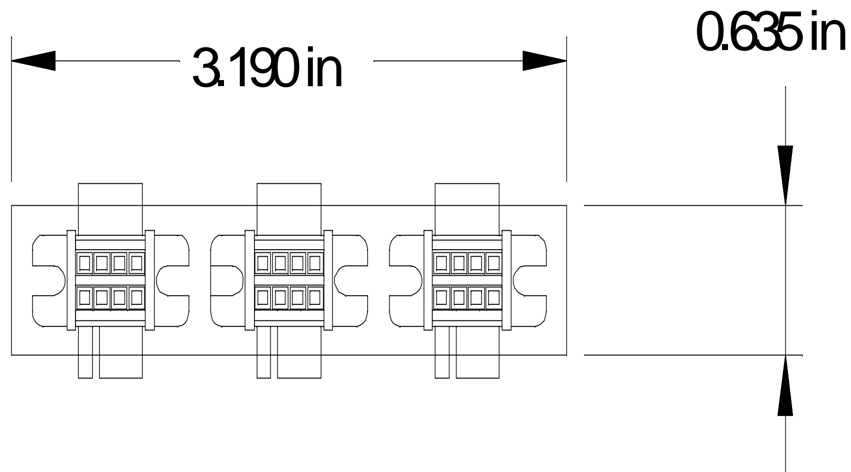


Figure 3.17 SSPC switch concept

3.3.1 Summary of SSPC Power Switch Thermal Model

Although the thermal resistance measurement method developed in section 3.2

can be applied to both Si and SiC devices, a thermal model of the SiC device developed to predict the thermal performance of the JFET switch during the fault current transient in order to predict the minimum number of JFET chips and modules that needed to be paralleled to meet the switch's requirements. Transient thermal experiments were then conducted to verify the model predictions and verify that the module fabrication was completed correctly. The transient thermal model was constructed using Spice to predict the transient thermal resistance and junction temperature versus time. The predicted transient thermal resistance was compared to experimental results to verify the calculated number of SiC JFETs that need to be put in parallel to meat SSPC trip curve requirement.

Currently, the SiC JFETs available for test do not have the BeO insulator, the CuW or multiple chips in a module. Rather the SiC devices tested consisted of a single SiC chip soldered directly to the case with one chip per module (package). Thus the thermal model of the experimental SiC devices can be simplified as shown in Figure 3.18.

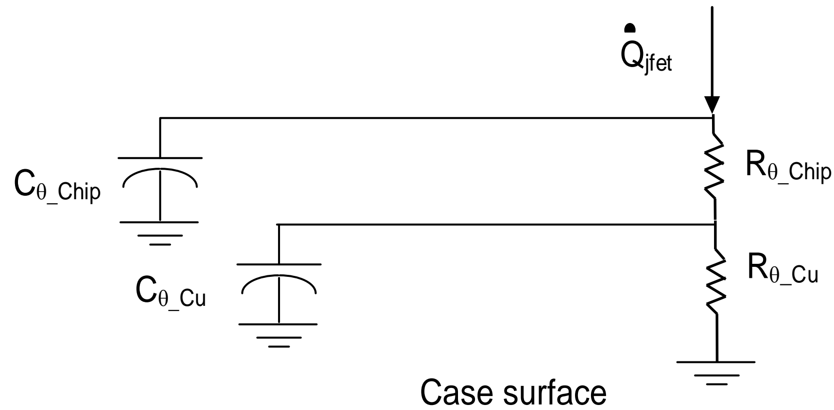


Figure 3.18 Single Module Transient Thermal Circuit

The value of SiC JFET chip's thermal resistance R_{θ_JFET} can be computed using

$$R_{\theta_chip} = \frac{th_{Chip}}{Kt_{SiC} \times Area_{Chip}} \tag{3.8}$$

where th_{Chip} is the thickness of the SiC chip, $Area_{Chip}$ is the area of the SiC chip, and Kt_{SiC} is thermal conductivity of SiC. The value of the copper package case R_{θ_Cu} can be

computed in a similar way.

Both the thermal capacitance of the chip (C_{θ_Chip}) and the thermal capacitance of the case (C_{θ_Cu}), which are key parameters that determine the transient thermal behavior of the device, must also be calculated. The value of C_{θ_Chip} can be computed using

$$C_{\theta_Chip} = Ct_{SiC} \times Area_{Chip} \times th_{chip} \tag{3.9}$$

and the value of C_{θ_Cu} can be computed using

$$C_{\theta_Cu} = Ct_{Cu} \times Area_{Cu} \times th_{Cu} \tag{3.10}$$

In Eq. 3.10 Ct_{Cu} is the heat capacity of copper which is the product of copper's mass density and specific heat capacity.

$$Ct_{Cu} = \rho_{Cu} \cdot Cp_{cu} = 3.21 \frac{J}{cm^3 \times K} \tag{3.11}$$

The numerical values of copper's mass density and specific heat capacity are

$$\rho_{Cu} = 8.23 \frac{g}{cm^3},\ Cp_{cu} = 0.38 \frac{J}{g \times K} \tag{3.12}$$

The area and thickness of the copper case can also be measured. The thermal capacitance of the Si chip, C_{θ_JFET} is computed in the same way. The details can be found in Appendix VIII.

Figure 3.19 shows the Spice thermal model that was developed for a SiC device under test. In the model the peak value of the current pulse is 6 A. The JFET's drain to source voltage is

$$V_{ds} = I_{ds} \times R_{on}(T) \tag{3.13}$$

which includes the fact that the on-resistance is a function of temperature. The power dissipated in the SiC JFET is

$$P = V_{ds} \cdot I_{ds} = I_{ds}^2 \cdot R_{on}(T_j{}^oC) = I_{ds}^2 \cdot R(T_{jo}) \left(\frac{T_j{}^oC}{T_{jo}} \right)^{\nu} \tag{3.14}$$

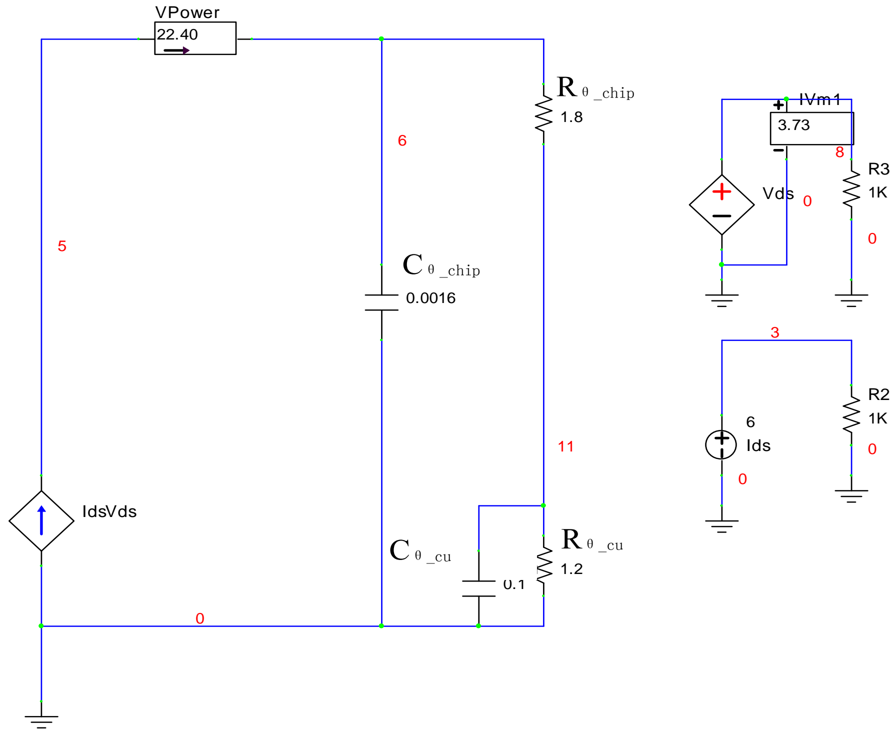


Figure 3.19 Spice thermal model of the SiC JFET with a constant 6A drain current

Figure 3.20 shows a typical simulation result, the lower waveform is the chip transient thermal impedance Z_{θ_Chip} and the upper waveform is the total transient thermal impedance Z_{θ_Tot}. The chip transient thermal impedance at a given instant of time is defined as the temperature rise from the bottom to the top of the SiC chip divided by the power dissipation in the chip at that instant of time. The total transient thermal impedance at a given instant of time is defined as the temperature rise from the bottom of the copper base plate to the top of the SiC chip divided by the power dissipation in the chip at that instant of time. The transient thermal impedance is what is specified by manufactures rather that the device thermal model parameters because it is easier to measure. The transient thermal impedance Z_{θ_Chip} reaches steady state faster than Z_{θ_Tot} because the SiC chip is much smaller and much thinner than the copper base plate the chip is mounted on so the thermal resistance R_{θ_Chip} is smaller than R_{θ_Cu} and thermal capacitance C_{θ_Chip} is also smaller than C_{θ_Cu}. Later in this chapter, the simulation results will be compared to experimental results.

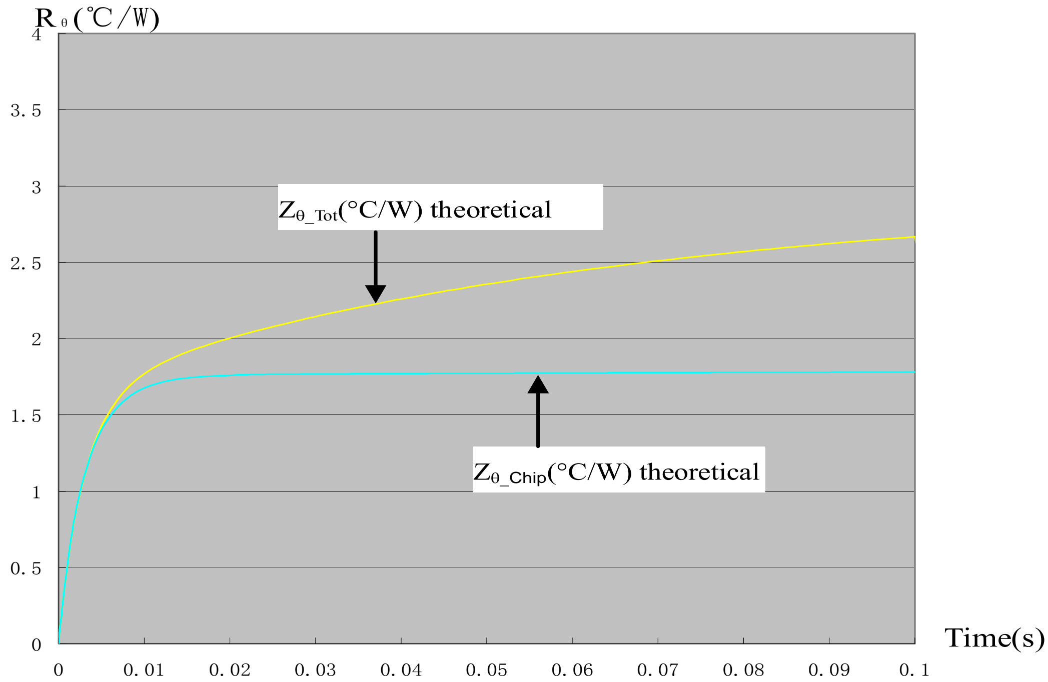


Figure 3.20 Computed transient thermal impedances versus time with 6A drain current under 0.1 second

The transient thermal model in Figures 3.18 and 3.19 along with the thermal circuit component values given in Eqs. 3.8 to 3.14 can be used to determine how many SiC JFETs should be put in parallel to meet the SSPC trip curve requirement in Figure 1.6 and the requirement that the maximum temperature rise from the case to the junction be less than or equal to 125℃.

For example, according to the trip curve, for a 500% rated current of 150 Ampere the length of time is the SSPC power switch is to remain on before it turns off is 40mS. The simulation circuits was modified as shown in Figure 3.21 for the case of 19 SiC JFET in parallel where the thermal resistances are divided by the number of SiC JFETs in parallel and the thermal capacitances are multiplied by the number of SiC JFET in parallel.

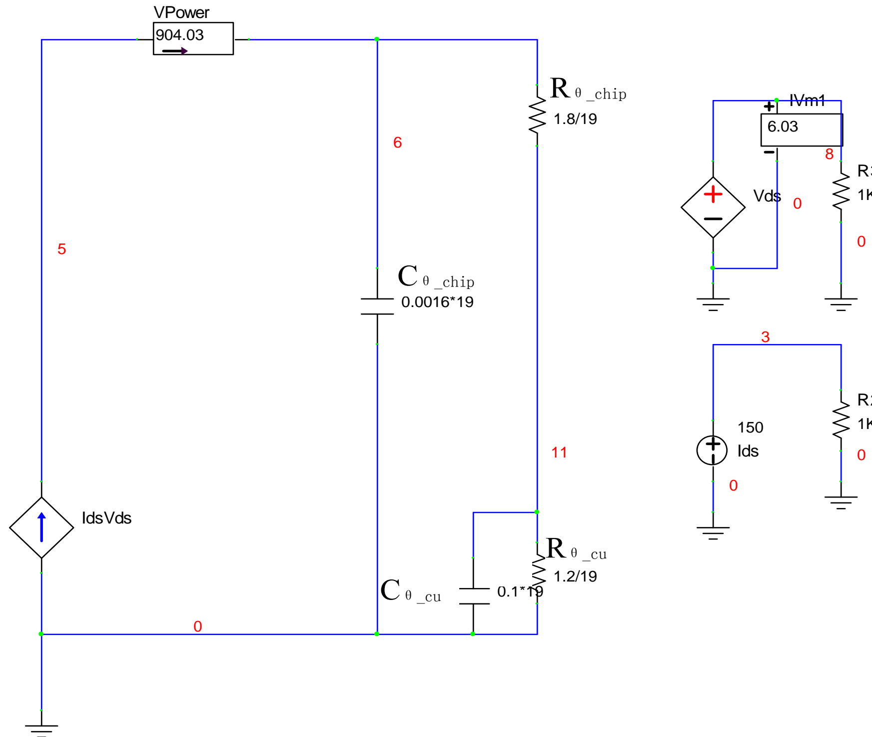


Figure 3.21 Thermal model circuit for predicting temperature rise for 19 individually packaged SiC JFET chips in parallel.

Figure 3.22 shows the temperature rise from the SiC JFET's junction to case obtained using the model for 19 individually packaged SiC JFET chips in parallel. Note that the first temperature increase is very rapid being completed in about 10ms. This is characteristic of the SiC chips time constant which is short due to the small size of the chip and the high thermal conductivity (low thermal reisistance) of SiC. The second rise in the junction temperature is much slower and characterist of the copper base plate the SiC chip is mounted on. From figure 3.22, nineteen of the individually packaged SiC JFETs are needed to be put in parallel to meet the trip curve requirement. If more SiC JFETs are put in parallel, the junction temperature will be lower and thus the system will be more reliable but the cost will increase, If less SiC JFETs are put in parallel, the temperature rise junction to case will exceed the 125℃ and thus result in a SiC power switch failure.

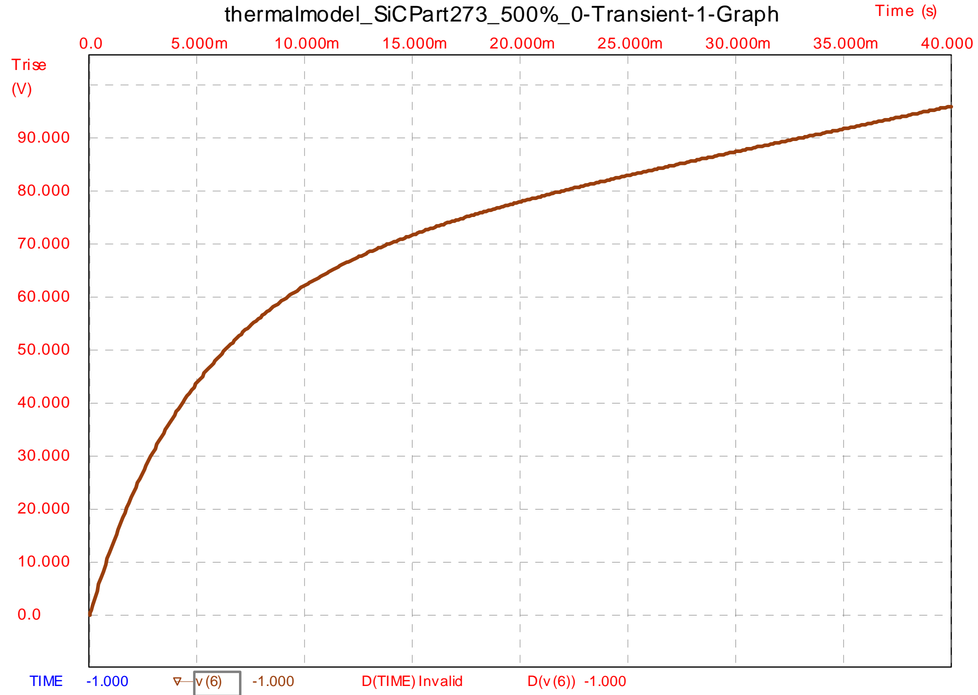


Figure 3.22 Temperature Rise Simulation Results For 500% rated current and 40mS

In the same way, a thermal model of multiple Si MOSFETs in parallel was built and used to determine the number of Si MOSFETs put in parallel to meet the SSPC trip curve requirement. The comparison of the SiC and Si results are shown in table 3.3. The ratio of the total required Si chip area to the total required SiC chip area is about 26.5, Thus a SiC device has superior performance compared to a Si device due to its much better material properties.

Table 3.3 Comparison between Si and SiC device.

Conditions			SiC device		Si device	
Isurge	Time	I	#Chips	Chip Area	#Chips	Chip Area
100%	infinite	30A	5	5mm2	2	2cm2
200%	200mS	60A	9	9mm2	2	2cm2
500%	40mS	150A	19	19mm2	5	5cm2
1000%	10mS	300A	34	34mm2	9	9cm2

3.3.2 Measurement of SiC JFET Thermal Resistance

As discussed in section 3.1, the method developed to measure the thermal

performance of a Si device can be used to measure thermal response of a SiC device too. For the Si device the on-resistance versus junction temperature data is available in manufacture's specification while for the SiC device, the on-resistance versus junction temperature data must be measure experimentally. Once the data has been measured it can be fitted to the same equation for the on-resistance versus temperature. Once the equation for the SiC JFET's on-resistance versus temperature is know the JFET's on-resistance can be used as a thermometer to measure its junction temperature.

In order to accurately measure the relationship between the on-resistance and junction temperature, the data must be taken with essentially no power dissipation in the device so the SiC JFET's junction and case temperatures are equal. Doing this the measured case temperature the on-resistance is measured at is equal to the junction temperature the on-resistance is measured at. The JFET is put in an oven at various temperatures and at each oven temperature its case temperature and on-resistance are measured to obtain a calibration curve for the variation of the SiC JFET's on resistance with temperature. Data was taken from room temperature to 200°C or to the oven's maximum temperature in 10°C steps. It is necessary to wait at least 10 minutes at each new temperature to insure that the thermocouple, case, and the junction have come into thermal equilibrium with each other and thus are at the same temperature. Now having the on-resistance versus its junction temperature data, Eq 3.6 can be fit to the data to find ν.

Figure 3.23 shows a plot of the measured SiC JFET on-resistance and the plot of the least square curve curve fit versus the junction temperature. Figure 3.24 shows the error between the two curves.

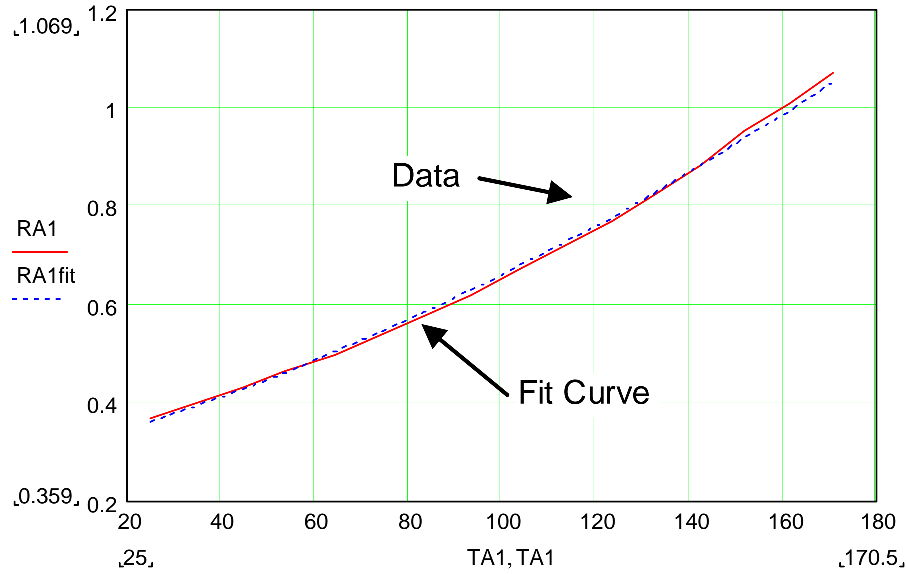


Figure 3.23 Measured SiC JFET on-resistance and curve fit plot versus junction temeprature

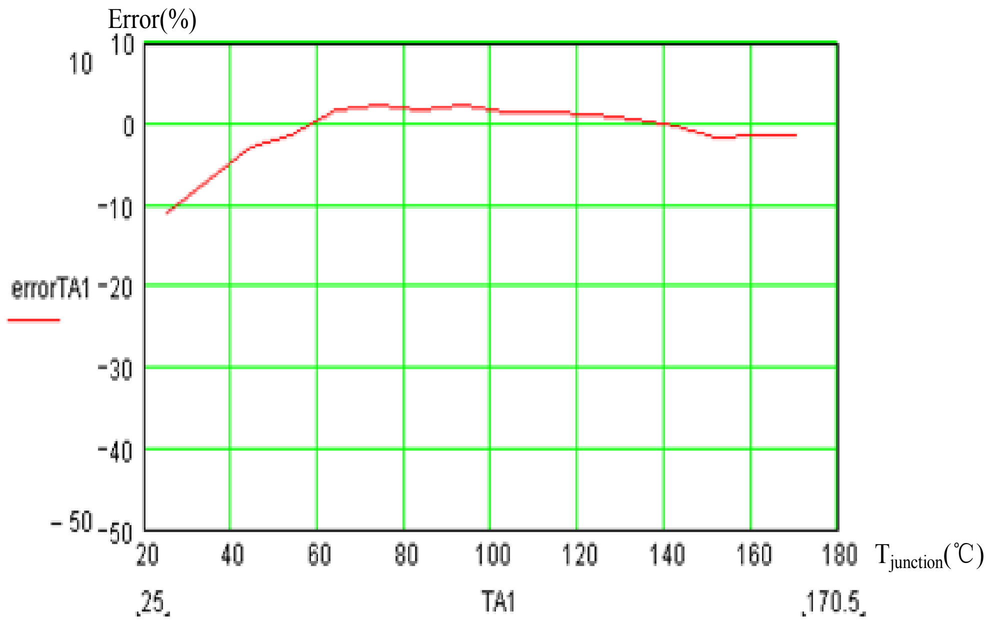


Figure 3.24 The error between the least square curve and the measured data.

The SiC JFET's transient thermal impedance is measured in the same manner as the Si MOSFETs transient thermal impedance was measured.

Figure 3.25 shows the experimental transient thermal impedance results obtained with current pulses with different durations and peak values. The upper ($Z_{\theta ja}$)

waveform is the transient thermal impedance from the junction to the air. As expected, it is higher and takes a long time to reach steady state.

Figure 3.24 shows the comparison between experimental results and simulation results for 6A constant current and under 0.1second. Noticed that it is impossible to only measure R_{θ_chip} alone but it is doable to measure R_{θ_Tot}

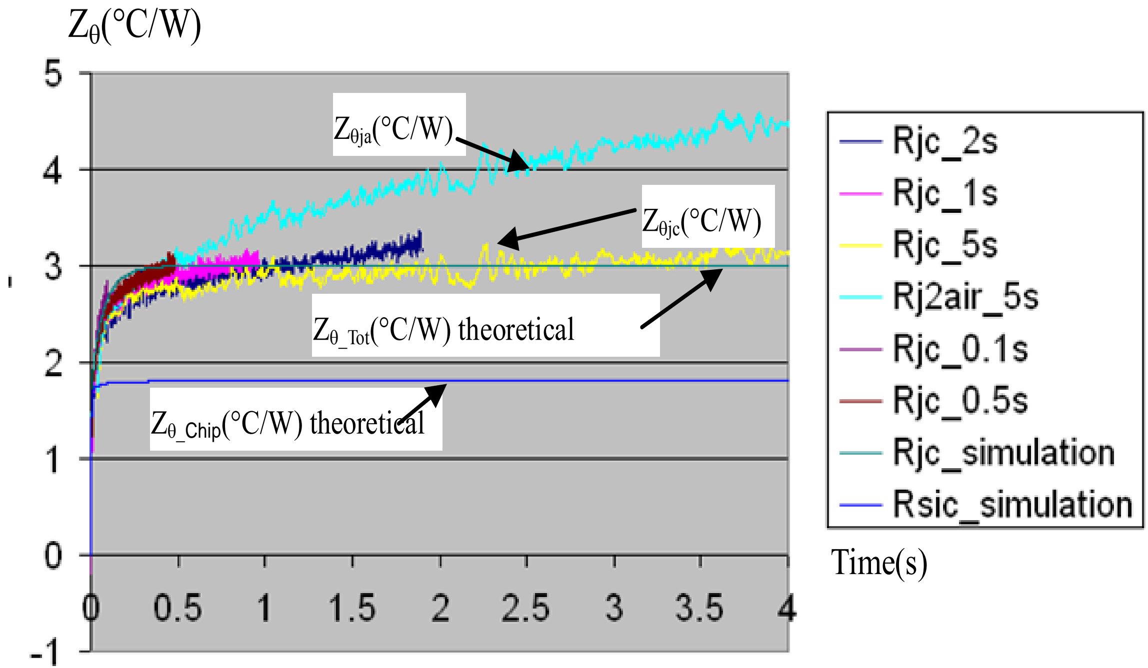


Figure 3.25 Measured transient thermal resistances with different time scales and compared to simulation results.

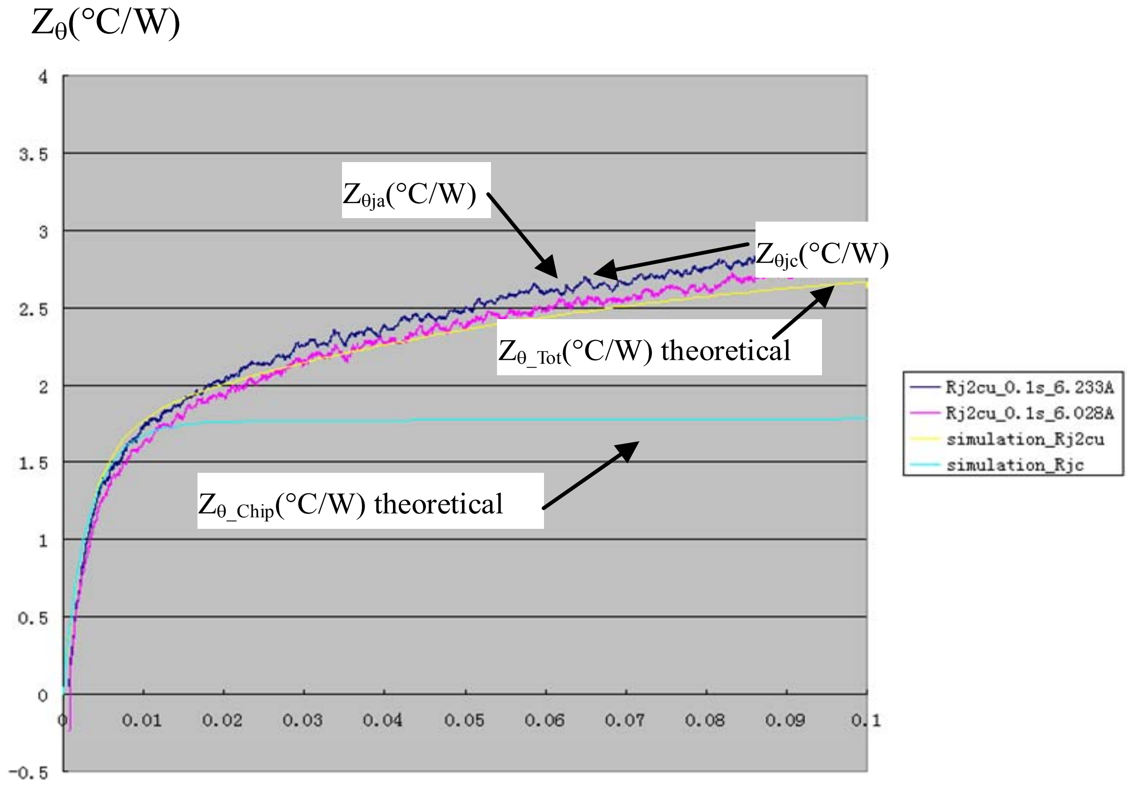


Figure 3.26 Measured transient thermal resistances under 0.1second and compared to simulation results.

According to simulation parameter, the time constants can be computed and compared to measured time constants shown in Figure 3.25. The details can be found in Appendix VIII. Table 3.4 shows the comparison of computed and measured time constants.

Table 3.4 The Comparison of computed and measured time constants.

	Computed time constant	Measured time constant
Chip time constant (Time)	14 ms	13 ms
Junction to case time constant (Time)	0.68 s	0.55 s

3.3.3 Summary of SiC JFETs ($9mm^2$ active area) power switch parameters

The SiC JFETs tested above had an active area of $1mm^2$. The largest SiC JFETs that can be built at this time with an acceptable yield have an active area of $9mm^2$. It is these larger devices that were chosen for the final SSPC design. Detailed design results for these devices are shown in this section. A specification for the $9mm^2$ SiC JFET chip was developed and is given in Appendix III.

Chapter4 Experimental Results

4.1 Printed Circuit Board Layout and Fabrication

The SSPC circuit design presented in Chapter 2 was verified by fabricating and testing the circuit. The SSPC circuit was broken into three units which were implemented in three printed circuit boards (PCBs). These three units are the Gate drive board, I^2T board and the Logic Section board. The fabricated, populated, and tested boards are shown in Figure. 4.1.

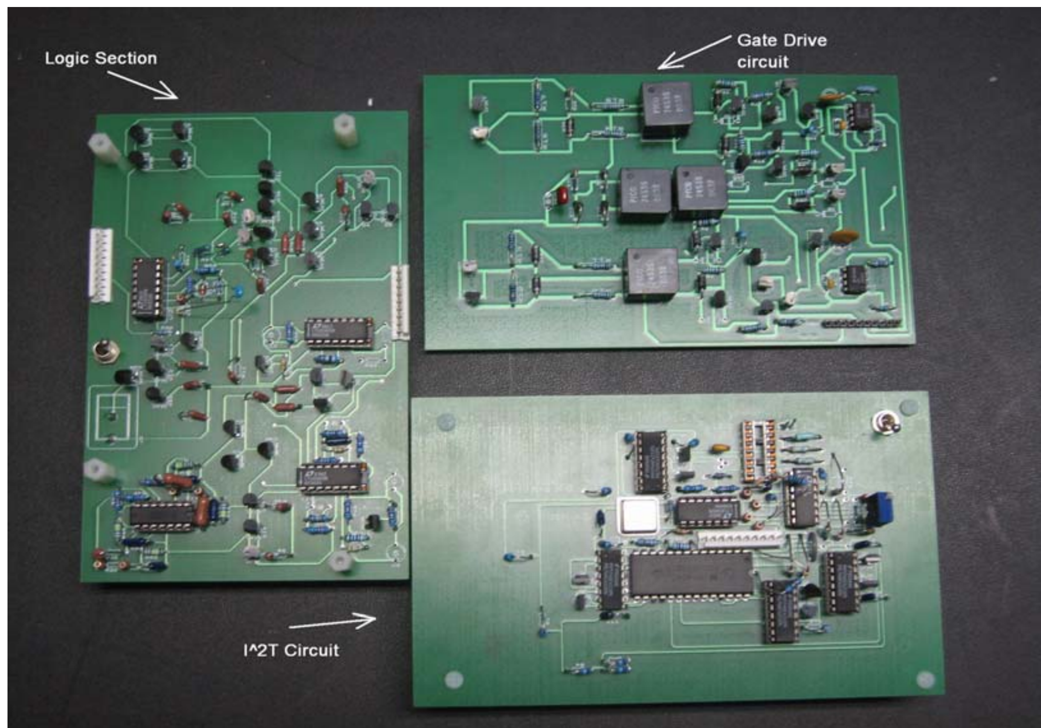


Figure 4.1 Three printed circuit boards developed for the SSPC

Figure 4.2 shows the integration of the three fabricated boards and a Si power MOSFET. The required logic power supply (plays the role of the aircraft 28V) is not shown but is connected to the breadboard using standard test leads.

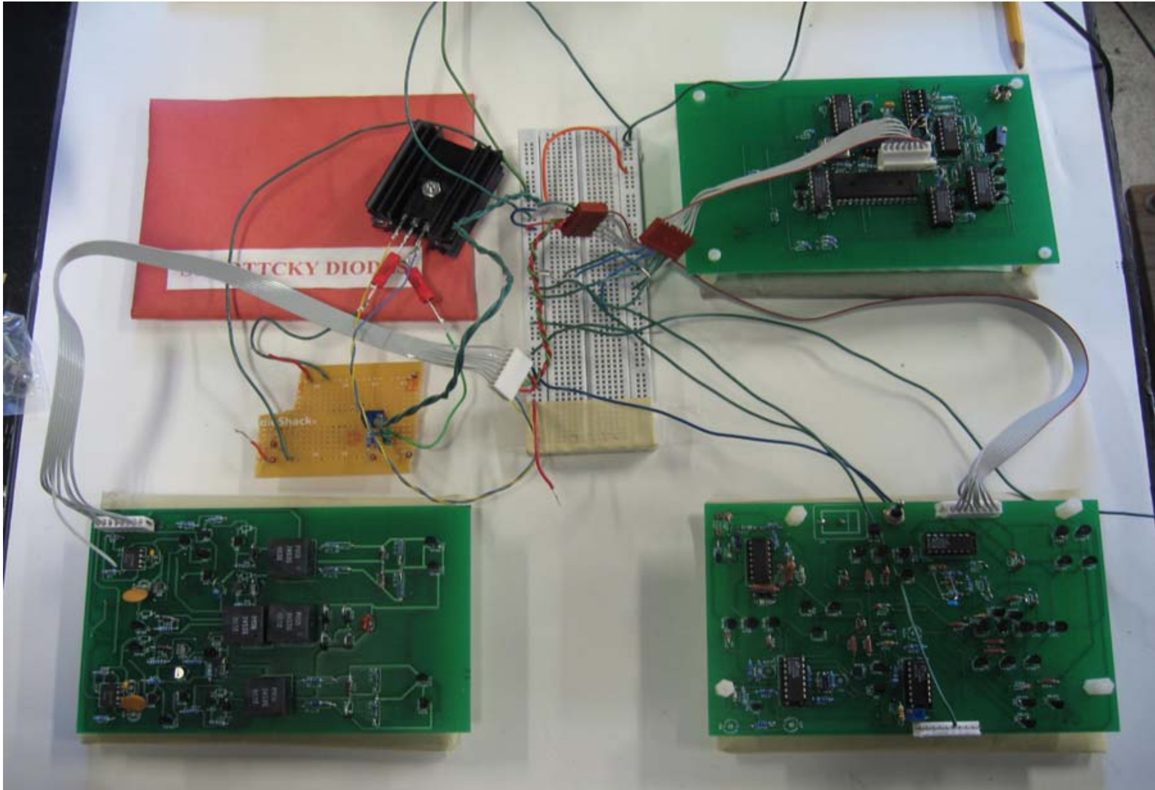


Figure 4.2 the Integration of the three fabricated boards with a Si MOSFET

4.2 Experimental results

As described in Chapter 2, the SSPC was designed for a 270VDC aircraft electrical system. For the SSPC design the highest current during a fault is 300A. In the experimental SSPC a power MOSFET was ultimately used for the power switch instead of the three SiC JFET modules in parallel that are required by the design. This is because the required SiC JFET modules are still being developed and were not available to test the SSPC system. After fabrication of the SSPC system was completed, a series of tests

were run and the test results were recorded. Both transient and steady state operation of the experimental SSPC have been evaluated. Performance results from the experimental system are presented in this chapter.

Figure 4.3 shows the measured logic input voltage from the SSPC switch status latch labeled Q and the gate to source voltage V_{GS} waveforms for the gate drive circuit. These experimental results can be, compared to the spice simulation results in Figure 2.7. The upper waveform is the input command signal (Q), when it is high; the lower waveform (V_{GS}) is zero, which means the JFET is turned on. When the upper waveform is low, the lower (V_{GS}) is negative 40 volts, which means the JFET is turned off.

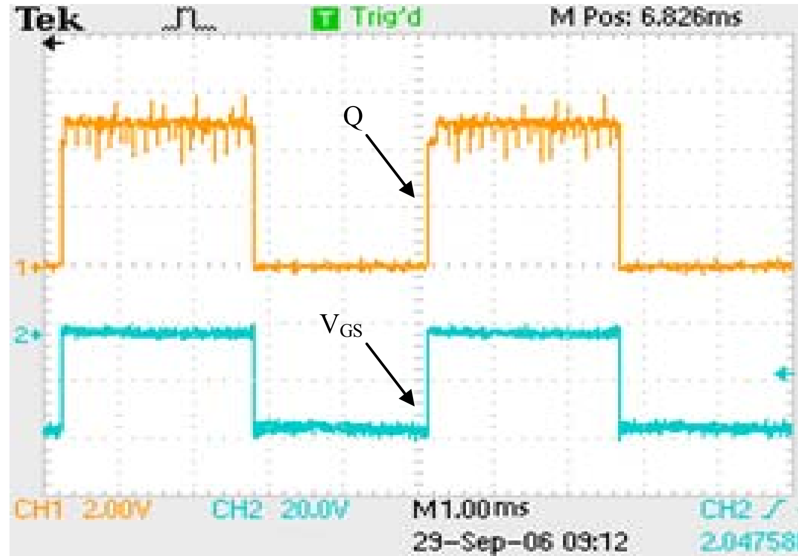


Figure 4.3 Experimental results for the SSPC gate drive circuit with C1 in the gate drive equal to10uF and C_{GS}=90nF. The upper waveform is the logic input and the lower waveform is the gate to source voltage

Figures 4.4a and 4.4b show the expanded V_{GS} waveform so that its rise and fall times can be observed and measured.

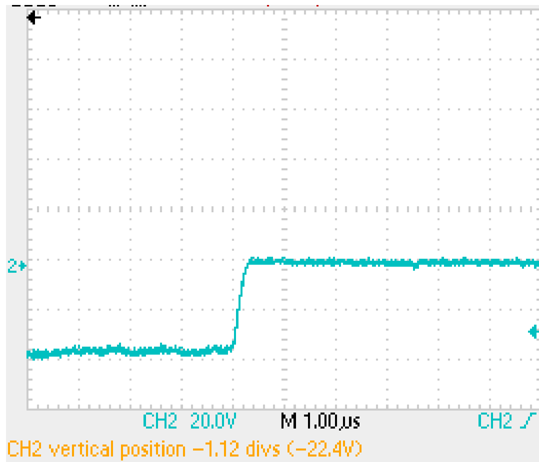


Figure 4.4a Rise time of V_{GS}, 1us/div.

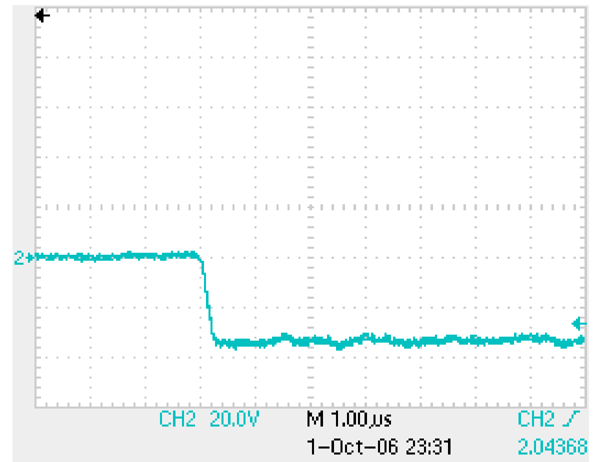


Figure 4.4b Fall time of V_{GS}, 1us/div

The rise and fall times are less than 1µs, which is much faster than required for the SSPC. Thus the switching time of the JFET can be set to the desired value with an appropriate gate resistor.

In Figures 4.5a and 4.5b, both gate drive input control signal (Q) and the corresponding output (V_{GS}) shown simultaneously to measure the delay time between them. The upper waveform is the input control signal (Q). When it is high, the SiC JFET device should be turned on; when it is low, the SiC JFET device should be turned off. As we can see, the delays between them are less than 1us at turn on and turn off. Thus the maximum delay for the SSPC to turn off once it is commanded to turn off is 10µs (gate drives clock period) plus 920ns or about 11µs. It was determined by simulation that the total switch turn off time needed to be about 56µs to insure that the switch did not generate an excessive ring up voltage turning off without a link capacitor and 20µH of aircraft wiring inductance.

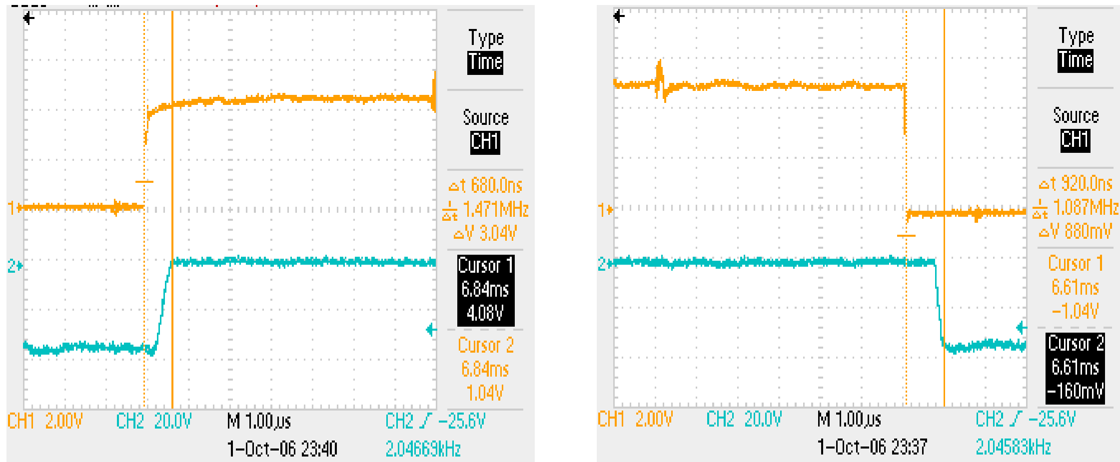


Figure 4.5a The delay is 680ns during rise time. Figure 4.5b The delay is 920ns during fall time.

Figure 4.6 shows the output of the integrator and the comparator the integrator's output goes into in the experimental I^2t circuit at rated current, 316% of rated current and 1000% of rated current. As required by the square of the current the time that it takes to trip the SSPC follows a square relationship and is 1 second, 0.1 second, 0.01 second respectively. This meets the trip curve requirement in Figure 4.7d. The comparator output (stepped curve) indicates that the SSPC tripped and turned off when the I^2t signal exceeded 4Vdc.

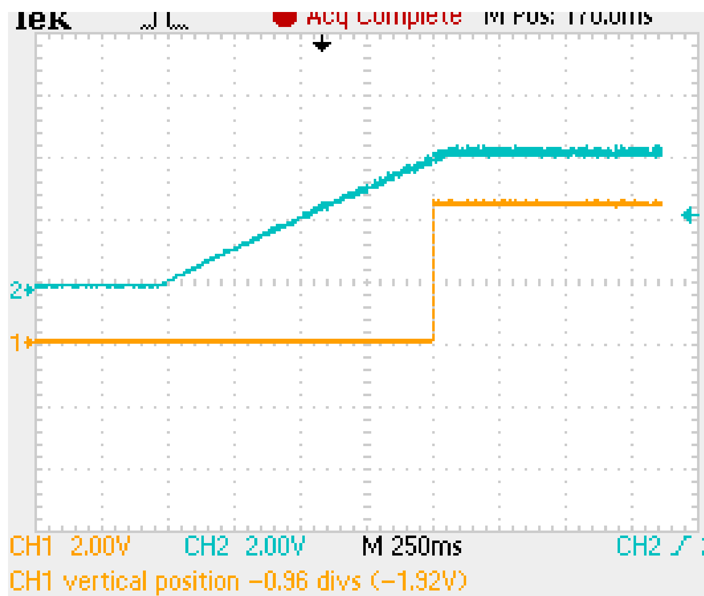


Figure 4.6 Measured integrator and comparator output at rated current

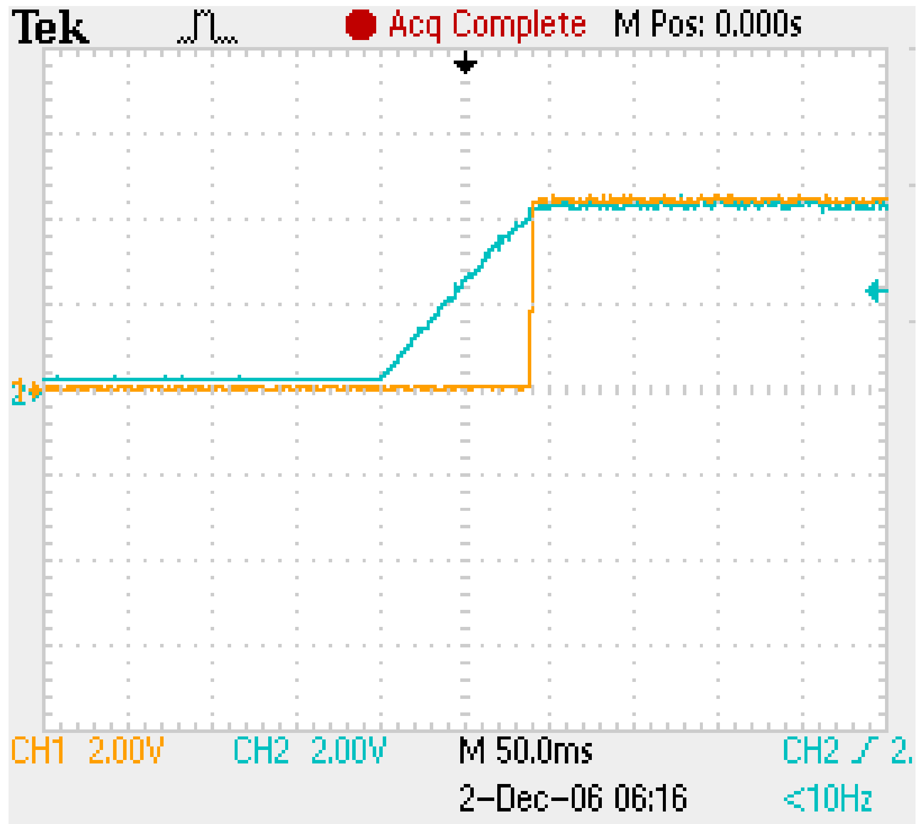


Figure 4.7 Measured integrator and comparator output at 316% rated current

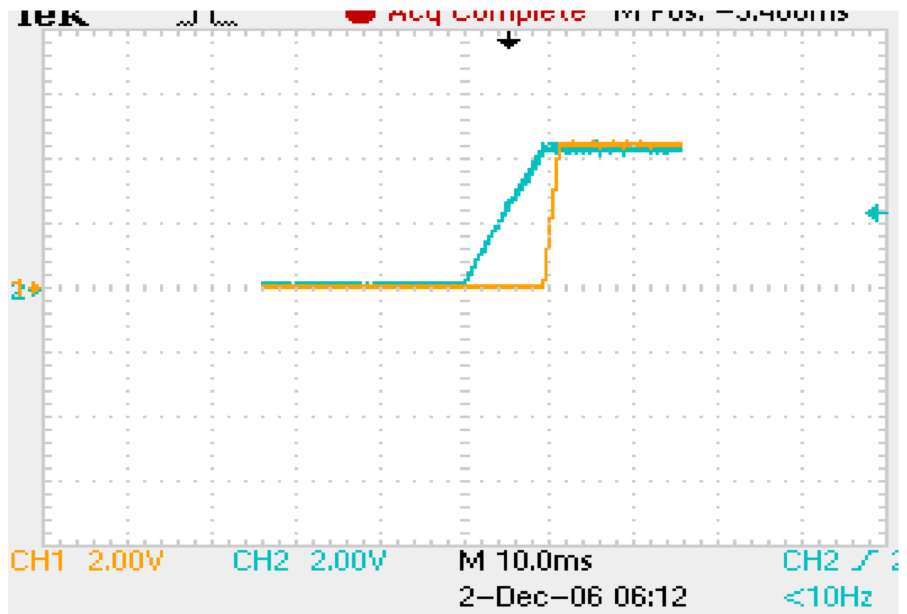


Figure 4.8 Measured integrator and comparator output at 1000% rated current

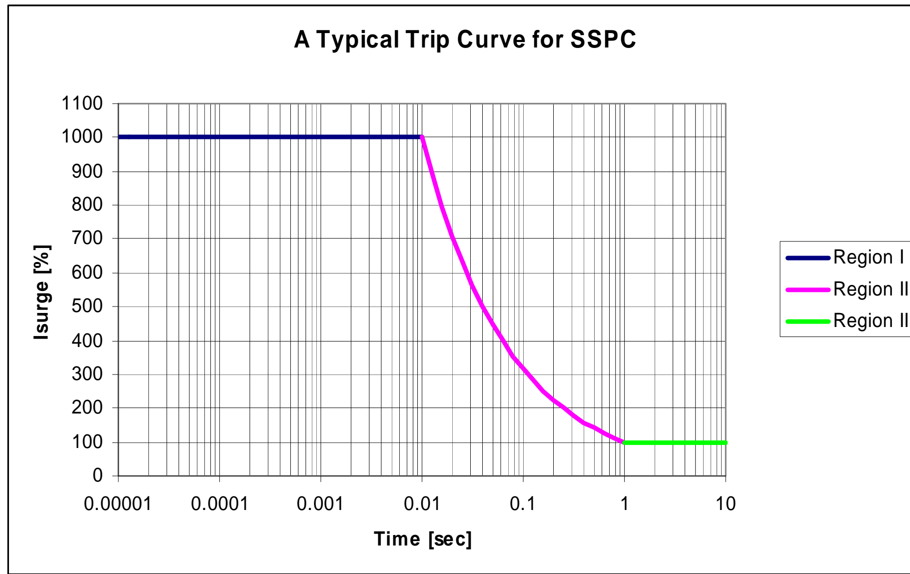


Figure 4.9 Specified SSPC trip curve.

Figure 4.10 shows the measured power MOSFET drain to source voltage V_{DS} during an over 200% over current transient. In this test the SSPC is reset 3 consecutive equally spaced times after it turns off due to an I^2t shutdown. Thus the MOSFET continues to heat up. Note that V_{DS} does not start from its value at room temperature. The MOSFET's junction temperature is increasing due to the over current and continues to increases after each SSPC reset., Thus the MOSFET's drain to source voltage V_{DS} also increases until it exceeds the maximum value. As discussed in Chapter 2, if input current is constant, V_{DS} will increase nearly proportional to the temperature and V_{DS} will approximately double from its room temperature value at the same current when the MOSFET's junction temperature increases from 25°C to 125°C, which is maximum operating temperature. The MOSFET's V_{DS} is sensed using a differential op-amp.

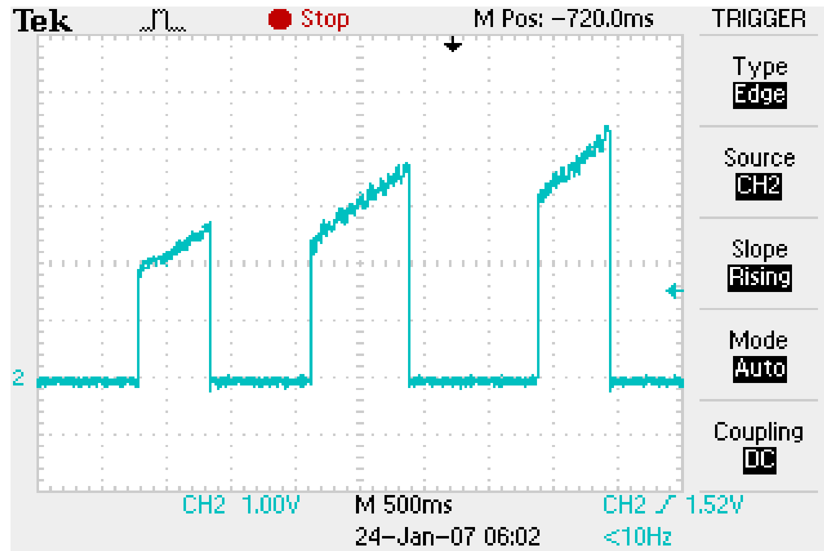


Figure 4.10 Measured V_{DS} showing it doubling as the MOSFET's junction temperature goes from 25°C to 125°C because the I^2t circuit shutdown is overridden by resetting the circuit 3 times.

As discussed in Chapter 2, the control section contains thermal shutdown, over-current shutdown, and R/S latch. The R/S latch stores the status of the JFET switch. Under normal operating conditions without a fault the reset (R), set (S), and Q are low, a logic zero.

First, before the SSPC connects the power to the load the SSPC is in off state and the SSPC is waiting for an on-command. At this time, R=0, S=1,Q=1, Qbar=0. To turn on the SSPC the set input is made low and an on-command is issued to cause a short duration high at R. This resets the R/S latch after which both R and S are equal zero. The Q output goes low and the SSPC switch is on. This turn-on process is shown in Figures 4.11 and 4.12

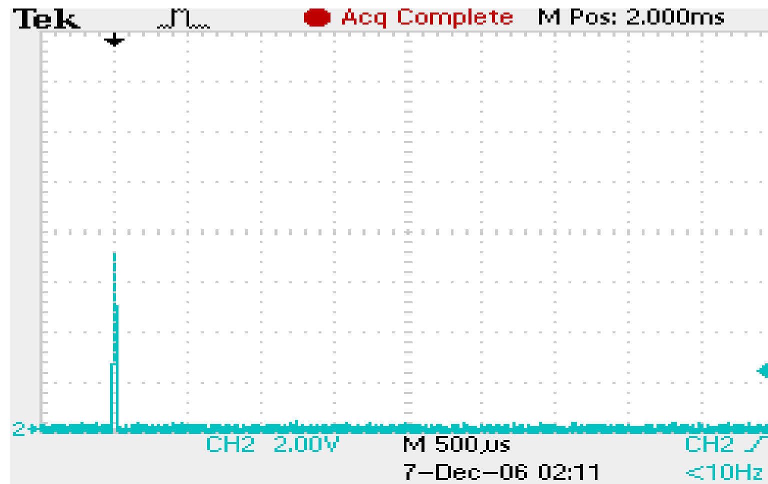


Figure 4.11 The reset spike appears at R when the on-command is issued

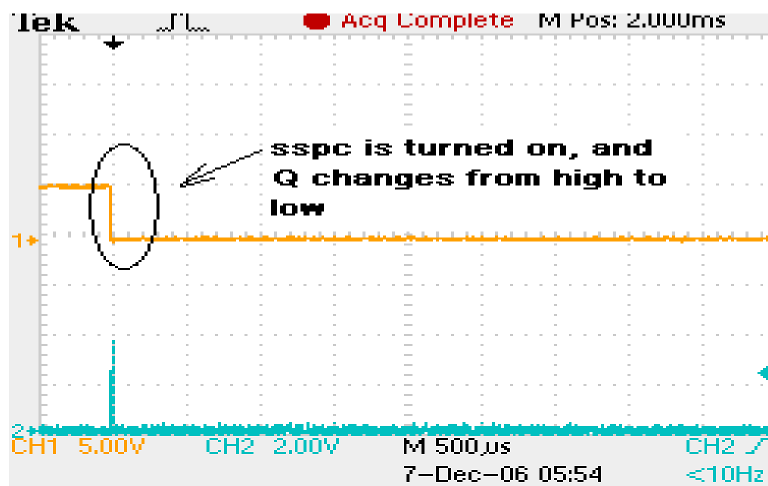


Figure 4.12 The SSPC is turned on due to the change of R

After the SSPC is turned on, R and S will remain low and the status of the R/S latch will not change until a fault condition appears, which can be caused by any condition among the over-current, over-temperature and over-I^2t. If a fault occurs the flip-flop's set input goes high so R=0, S=1, and thus Q goes high (Q=1, Qbar=0). When Q goes high it causes the SiC JFET switch to be turned off eliminating the fault current and causing the set input to the R/S latch to return to zero. The R/S latch Q output remains high (stores a fault occurred) and the SiC JFET switch remains off. Thus the set input remains high only long enough to turn the SiC JFET off as shown in Figure 4.13. Once the cause of the fault has been corrected the user can make the reset high with the set

input remaining low (S=0, R=1). The Q output goes low turning the SiC JFET switch back on.

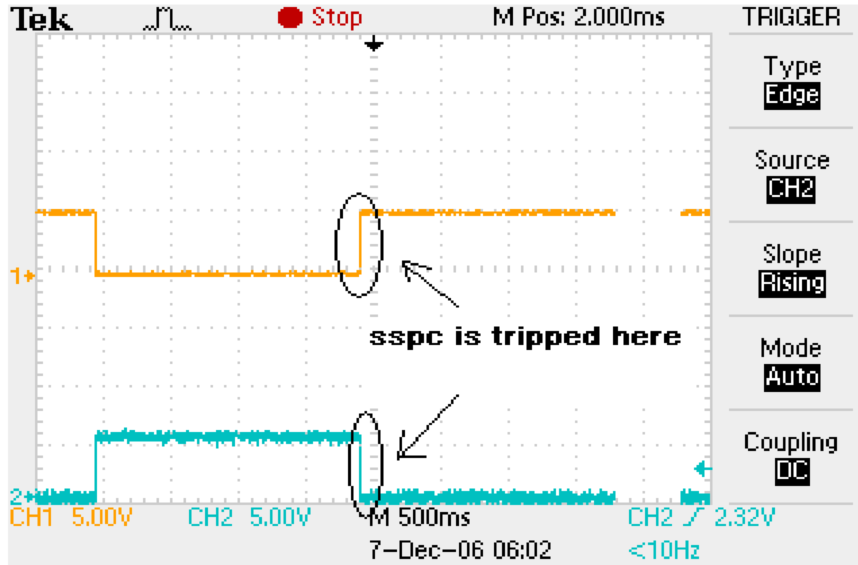


Figure 4.13 SSPC is turned off due to fault condition.

The R/S latch outputs Q and Qbar control the turn on/off of the SiC JFET's gate drive signal as described in the section on the gate drive.

4.3 Connecting wire inductance

The SSPC can be installed anywhere in the aircraft with the SSPC connected between the generator and the load by wire with a length up to 30 feet long. This wire has inductance often called stray inductance, which will generate induced voltages across the SSPC power switch when the SSPC turns off because the SSPC has neither a DC link capacitor or free-wheel diode. The inductance of 30 feet of wire is approximately equal to 20μH.

$$V_{g_stray} = L_{g_stray} \frac{di_{LA}}{dt}$$

Figure 4.14 shows the SSPC turn off simulation model. Here two 10 μH inductors are put in series (sum to 20μH) with SSPC power switch to simulate wire stray

inductance. The SSPC turn off simulation results are shown in Figure 4.15 and 4.16.

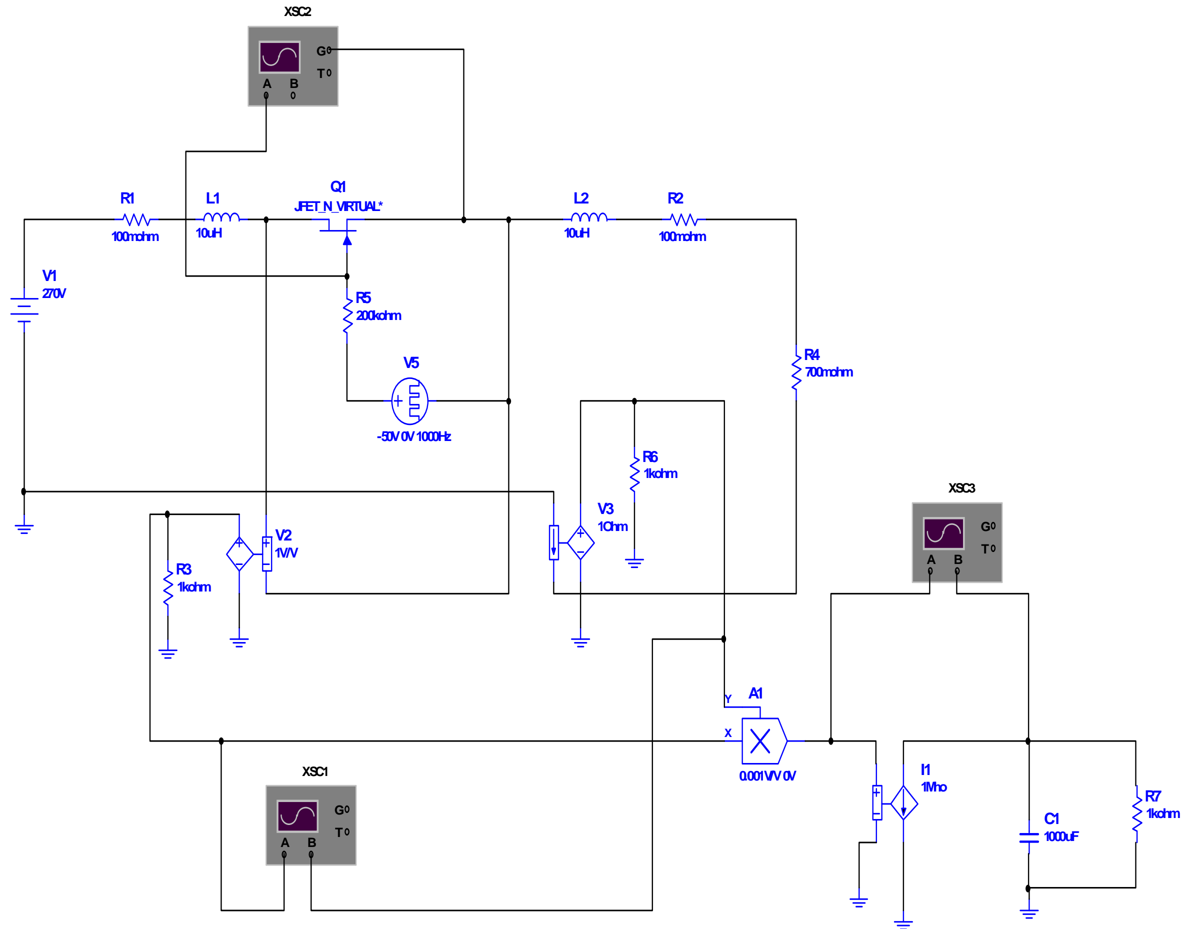


Figure 4.14 Stray inductance spice simulation model

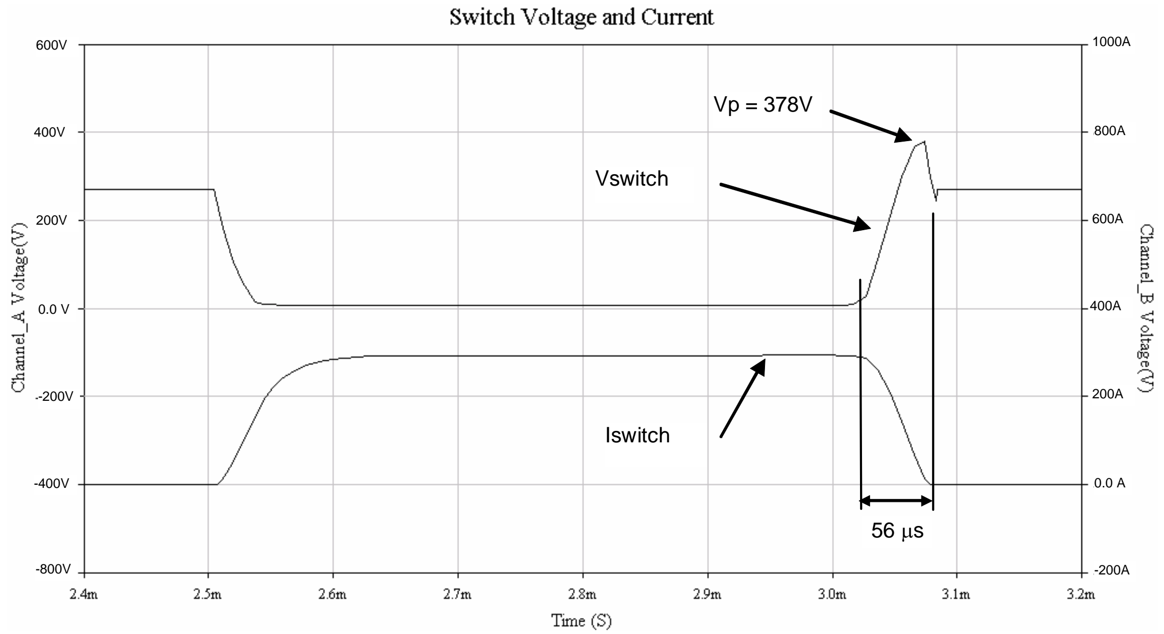


Figure 4.15 Voltage drop across the SiC JFET showing the voltage spike induced by the inductance of the wire connecting the SiC JFET to the power supply and load.

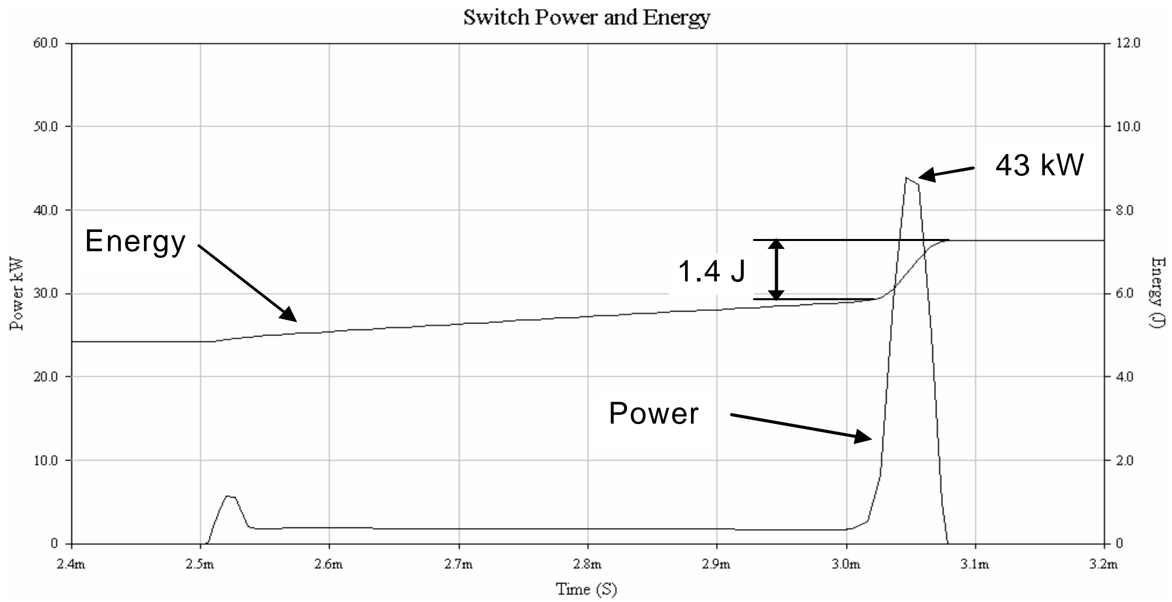


Figure 4.16 generated power and energy during the turn off of SSPC

Chapter5 Conclusions

5.1 Conclusions

The research done in this dissertation addresses the problem of replacing a conventional electromagnetic circuit breaker with a high voltage and current solid-state power controller (SSPC) to improve power management and fault protection in 270Vdc aircraft electrical power systems. The electrical aircraft power system distributes power to different loads and protects both itself and the loads. With SSPC protection, the power system is more reliable with improved fault handling capability. In particular a SSPC will provide current squared time protection (I^2t) for wiring and rapid fault protection for short circuit faults. To achieve a high voltage and current SSPC this research has investigated the use of SiC JFET technology for the main semiconductor switch. Prior research to investigate the use of SiC power semiconductors in this application was not found in the literature. The need for such SiC JFET technology is driven by the limited properties of Silicon material and the need to reduce the size of circuit breakers and complex cooling systems in electrical aircraft power systems. Methods for testing SiC JFET devices under transient thermal conditions unique to the SSPC application were developed and the experimental results were compared to simulation results of using a transient thermal circuit model. The transient thermal circuit model was analyzed using Spice and Mathcad. The SSPC circuit design was simulated using Multisim Spice. After simulation, printed circuit boards for the SSPC were laid out and built to test the SSPC circuit experimentally. This laboratory breadboard was tested with a Si power MOSFET at reduced current instead of using a SiC JFET device because the proposed SiC JFET is still being developed. However available reduced current SiC JFETs were tested under the transient thermal conditions of the SSPC to verify the SiC design conclusions.

The transient thermal experiments were undertaken first with Si MOSFETs because SiC JFETs are still experimental, expensive to purchase, and difficult to obtain while Si MOSFETs are low cost and common place. Thus Si devices were tested first to

develop the test methods for characterizing the SiC JFETs thermally. Also, the thermal performance of Si devices is available in their specification and this information can be used to verify the thermal models and measurement methods developed. Finally, once the experimental results showed that the modeling and the measurement methods were correct for the Si devices they were applied to the lower current SiC JFETs that were available and can be applied to the SiC JFETs required by the SSPC design once they becomes available. Compared with the conventional electromagnetic circuit breaker, this proposed SSPC will be more suited to the emerging high current, large scale 270Vdc aircraft electric power system applications.

5.2 Future Research

The results of this research point to a number of opportunities for increasing the current capability of the present experimental SSPC system. They include

1. Complete the development of the SiC JFET switch required by the completed SSPC design consisting of eight $9mm^2$ chips in parallel per module and three of these modules in parallel.

2. Complete transient thermal tests of the required SSPC SiC JFET modules verifying their design and fabrication method.

3. Complete traditional thermal cycle and life tests of the required SSPC SiC JFET modules.

4. The SSPC needs to be evaluated experimentally using the required SiC JFET switch.

5. The SSPC circuitry needs to be fabricated using high temperature components and evaluated by experimentally over the -55°C to 200℃ temperature range it will experience in use.

Appendices

Appendix I. Drain Current Sense Voltage Amplifier Common Mode Voltage Calculations

Design Inputs

$Ion := 30 \cdot amp$

$Imax := 300 \cdot amp$

$Vcommon := 270 \cdot volt$

$Vcommonmax := 330 \cdot volt$

$Vcommonmin := 200 \cdot volt$

Sense Resistor Specification

$Rsensei := 0.01 \cdot ohm$

Value of one sense resistor

$npar := 2$

number of sense resistors in parallel

$Pmax25c := 25 \cdot watt$

Maximum power rating at 25C

$Pmax200c := 0.2 \cdot Pmax25c$

Power rating at 200C is 20% of its 25C power rating

$Pmax200c = 5\,W$

Value of the composite sense resistor consisting of

$npar = 2$ Resistors in parallel.

$$Rsense := \frac{Rsensei}{npar}$$

$Rsense = 5 \times 10^{-3}\,\Omega$

Compute the power loss in the sense resistors

$$Psense_per_R := \frac{Ion^2 \cdot Rsense}{npar}$$

$Psense_per_R = 2.25\,W$

$$Psensemax_per_R := \frac{Imax^2 \cdot Rsense}{npar}$$

$Psensemax_per_R = 225\,W$

Compute the differential voltages

$Vdiff := Ion \cdot Rsense$

$Vdiff = 0.15\,V$

$Vdiffmax := Imax \cdot Rsense$

$Vdiffmax = 1.5\,V$

Output Constraints

$Voutmax := 7.5 \cdot volt$

$Vinmin := 0 \cdot volt$

$Vinmax := Voutmax$

$$Vcommono := \frac{Vinmax - Vinmin}{2} + Vinmin$$

$Vcommono = 3.75\,V$

Differential Gain Calculations

$$Gmaxdiffo := \frac{Voutmax}{Vdiffmax}$$

$Gmaxdiffo = 5$

Common Mode Gain Calculations

$$Gcommono := \frac{Vcommono}{Vcommon}$$

$Gcommono = 0.014$

Voltage Divider Design

$R1 := 500 \cdot 10^{3} \cdot ohm$

$$PR1 := \frac{Vcommonmax^{2}}{R1}$$

$PR1 = 0.218\,W$

$$R2 := \frac{R1 \cdot Gcommono}{1 - Gcommono}$$

$R2 = 7.042 \times 10^{3}\,\Omega$

Compute the gain of the amplifier

$$Gamp := \frac{Gmaxdiffo}{Gcommono}$$

$Gamp = 360$

$GBWP := 1.4 \cdot 10^{6} \cdot Hz$

$$BW := \frac{GBWP}{Gamp}$$

$BW = 3.889 \times 10^{3}\,Hz$

$\omega BW := 2 \cdot \pi \cdot BW$

$$\tau BW := \frac{1}{\omega BW}$$

$\tau BW = 4.093 \times 10^{-5}\,s$

Feedback Gain Calculations

$$Vth := \frac{Vdiffmax \cdot R2}{R1 + R2}$$

$Vth = 0.021\,V$

$$Rth := \frac{R1 \cdot R2}{R1 + R2}$$

$Rth = 6.944 \times 10^{3}\,\Omega$

$Rf := Gamp \cdot Rth$

$Rf = 2.5 \times 10^{6}\,\Omega$

Test Cases

1) Maximum common mode voltage and maximum differential voltage (300A)

$$Vth1 := \frac{Vdiffmax \cdot R2}{R1 + R2}$$

$Vth1 = 0.021\,V$

$$Vcommon1 := \frac{Vcommonmax \cdot R2}{R1 + R2}$$

$Vcommon1 = 4.583\,V$

$$Vout1 := Vth1 \cdot \frac{Rf}{Rth}$$

$Vout1 = 7.5\,V$

2) Minimum common mode voltage and minimum differential voltage (30A)

$$Vth2 := \frac{Vdiff \cdot R2}{R1 + R2}$$

$Vth2 = 2.083 \times 10^{-3}\,V$

$$Vcommon2 := \frac{Vcommonmin \cdot R2}{R1 + R2}$$

$Vcommon2 = 2.778\,V$

$$Vout2 := Vth2 \cdot \frac{Rf}{Rth}$$

$Vout2 = 0.75\,V$

The over current comparator is to trip when the current amplifier reaches 7.5V

Appendix II. VDS Sense Voltage Amplifier Common Mode Voltage Calculations

V_{DS} Sense Voltage Amplifier Common Mode Voltage Calculations

Design Inputs

$Ion := 30 \cdot amp$

$Imax := 300 \cdot amp$

$Vcommon := 270 \cdot volt$

$Vcommonmax := 330 \cdot volt$

$Vcommonmin := 200 \cdot volt$

$Ron25c := 5 \cdot 10^{-3} \cdot ohm$

$Ron225c := 10.5 \cdot 10^{-3} \cdot ohm$

$Vdiff25c := Ion \cdot Ron25c$

$Vdiff25c = 0.15\,V$

$Vdiff25cmax := Imax \cdot Ron25c$

$Vdiff25cmax = 1.5\,V$

$Vdiff225c := Ion \cdot Ron225c$

$Vdiff225c = 0.315\,V$

$Vdiff225cmax := Imax \cdot Ron225c$

$Vdiff225cmax = 3.15\,V$

Output Constraints

$Voutmax := 7.5 \cdot volt$

$Vinmin := 0 \cdot volt$

$Vinmax := Voutmax$

$$Vcommono := \frac{Vinmax - Vinmin}{2} + Vinmin$$

$Vcommono = 3.75\,V$

Differential Gain Calculations

$$Gmaxdiffo := \frac{Voutmax}{Vdiff225cmax}$$

$Gmaxdiffo = 2.381$

Common Mode Gain Calculations

$$Gcommono := \frac{Vcommono}{Vcommon}$$

$Gcommono = 0.014$

Voltage Divider Design

$R1 := 500 \cdot 10^{3} \cdot ohm$

$$PR1 := \frac{Vcommonmax^{2}}{R1}$$

$PR1 = 0.218\,W$

$$R2 := \frac{R1 \cdot Gcommono}{1 - Gcommono}$$

$R2 = 7.042 \times 10^{3}\,\Omega$

Compute the gain of the amplifier

$$Gamp := \frac{Gmaxdiffo}{Gcommono}$$

$Gamp = 171.429$

$GBWP := 1.4 \cdot 10^{6} \cdot Hz$

$$BW := \frac{GBWP}{Gamp}$$

$BW = 8.167 \times 10^{3}\,Hz$

$\omega BW := 2 \cdot \pi \cdot BW$

$$\tau BW := \frac{1}{\omega BW}$$

$\tau BW = 1.949 \times 10^{-5}\,s$

Feedback Gain Calculations

$$Vth := \frac{Vdiff225cmax \cdot R2}{R1 + R2}$$

$Vth = 0.044\,V$

$$Rth := \frac{R1 \cdot R2}{R1 + R2}$$

$Rth = 6.944 \times 10^{3}\,\Omega$

$Rf := Gamp \cdot Rth$

$Rf = 1.19 \times 10^{6}\,\Omega$

Test Cases

1) Maximum common mode voltage and maximum differential voltage (300A and Ron at 225C)

$$Vth1 := \frac{Vdiff225cmax \cdot R2}{R1 + R2}$$

$Vth1 = 0.044\,V$

$$Vcommon1 := \frac{Vcommonmax \cdot R2}{R1 + R2}$$

$Vcommon1 = 4.583\,V$

$Vout1 := Vth1 \cdot \frac{Rf}{Rth}$

$Vout1 = 7.5\,V$

2) Minimum common mode voltage and minimum differential voltage (30A times Ron at 25C)

$Vth2 := \frac{Vdiff25c \cdot R2}{R1 + R2}$

$Vth2 = 2.083 \times 10^{-3}\,V$

$Vcommon2 := \frac{Vcommonmin \cdot R2}{R1 + R2}$

$Vcommon2 = 2.778\,V$

$Vout2 := Vth2 \cdot \frac{Rf}{Rth}$

$Vout2 = 0.357\,V$

3) Maximum common mode voltage and over current differential voltage at 25C (300A times Ron at 25C)

$Vth3 := \frac{Vdiff25cmax \cdot R2}{R1 + R2}$

$Vth3 = 0.021\,V$

$Vcommon3 := \frac{Vcommonmax \cdot R2}{R1 + R2}$

$Vcommon3 = 4.583\,V$

$Vout3 := Vth3 \cdot \frac{Rf}{Rth}$

$Vout3 = 3.571\,V$

Common mode output

$Vthcommonmax := \frac{Vcommonmax \cdot R2}{R1 + R2}$

$Vthcommonmax = 4.583\,V$

$dbcommon := -95$

$Gcommon := 10^{\frac{dbcommon}{20}}$

$Gcommon = 1.778 \times 10^{-5}$

$Vcommonoutmax := Gcommon \cdot Vthcommonmax$

$Vcommonoutmax = 8.15 \times 10^{-5}\,V$

Appendix III. Specification for the 9mm2 SiC JFETSiC Chip Specification

The individual chips are square with dimensions 3.5mm X 3.5mm

The active area is 3.00mm X 3.00mm = 9mm^2

The chip thickness is 360µm +/- 30µm

350μm OD wire bond is feasible, 250 μm OD wire bonds were used previously

The maximum on-resistance of a single chip at various temperatures with V_{GS} = 0V and I_D = 10A is.

Ron @ 25ºC = 0.0962 Ω

Ron @ 200ºC = 0.204 Ω

Ron @ 225ºC = 0.222 Ω

The minimum single chip saturation current is I_{sat_min} = 28A at 225ºC with V_{GS} = 0V and V_{DS} = 30V

The minimum continuous single chip current @ 150ºC chip backside temperature, I_{cont} = 4.5A

The minimum non-repetitive 10ms single chip surge current @ 150ºC chip backside temperature, I_{surge} = 19A

The breakdown voltage over the temperature range from –55ºC < Tj <225ºC is greater than 600V

The pinch off voltage over the temperature range from –55ºC < Tj <225ºC, at V_{DS}=400V and a drain leakage current of Irss<0.4mA will be in the range 20V < $|V_{GS_pinch}|$ < 25V.

The metallization is

Backside – Au (Gold) (50nm Ti, 50nm Pt, 500nm Gold)

Top bonding metal is 3.2μm Al (Aluminum)

The passivation will be polyimide (no gel required).

Things to be measured at the wafer probe at room temperature and 225ºC. The 225ºC data can be on a sample of devices.

Breakdown voltage

Pinch off voltage

On resistance

8 Die Module

The 8 die module maximum on-resistance at various temperatures with V_{GS} = 0V and I_D = 80A is.

Ron @ 25ºC = 0.0120 Ω =12.0m Ω

Ron @ 200ºC = 0.0256 Ω =25.6m Ω

Ron @ 225ºC = 0.0278 Ω =27.8m Ω

The maximum continuous 8 die module current @ 150ºC chip backside temperature, I_{cont_mod} = 36.0A

Minimum non-repetitive 10ms 8 die module surge current @ 150ºC chip backside temperature, I_{surge_mod} = 152A

Minimum 8 die module saturation current is I_{sat_min} = 225A at 225ºC, V_{GS} = 0V, and V_{DS} = 30V

3 Module Switch

The 3 module switch maximum on-resistance at various temperatures with V_{GS} = 0V and I_D = 240A is

Ron @ 25ºC = 4.00m Ω

Ron @ 200ºC = 8.52m Ω

Ron @ 225ºC = 9.25m Ω

The maximum continuous 3 module switch current @ 150ºC chip backside temperature, I_{cont_mod} = 108A

The minimum non-repetitive 10ms 3 module switch surge current @ 150ºC chip backside temperature, I_{surge_mod} = 456A

The minimum 3 module switch saturation current is I_{sat_min} = 675A at 225ºC, V_{GS} = 0V, and V_{DS} = 30V

Appendix IV. ADC0808 A/D converter

The ADC0808 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique [11]. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register [11]. The 8-channel multiplexer can directly access any of 8-single-ended analog signals. The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs. The design of the ADC0808 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power [11].

A block diagram of the ADC0808 IC is shown in Figure A-1.

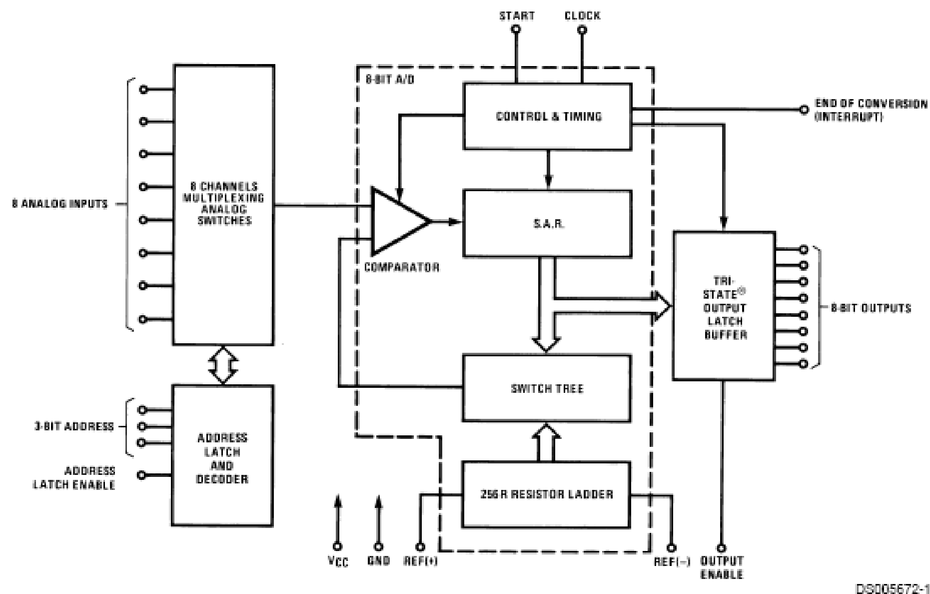


Figure A-1 Figure Block diagram of ADC0808 chip [11]

Multiplexer

The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table A-1 shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal [11].

Table A-1 Input states for the address lines [11]

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

Figure A-2 shows The ADC0808 circuit with external components as used in this dissertation.

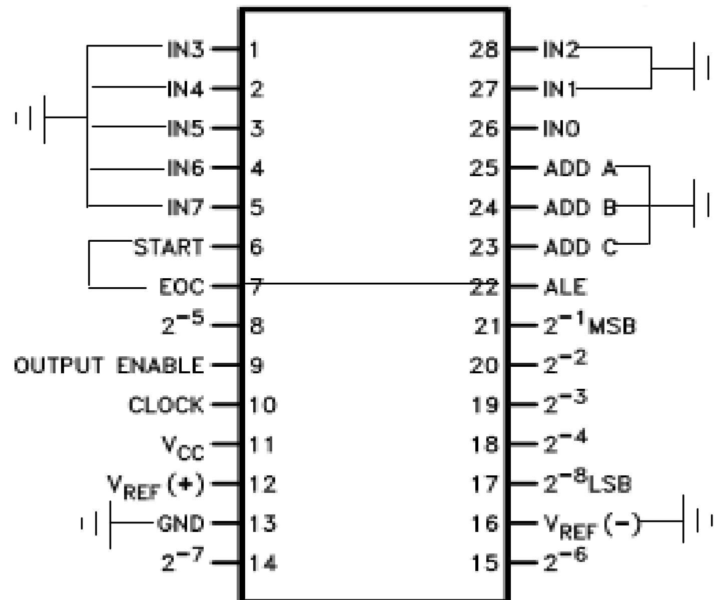


Figure A-2 The ADC0808 circuit schematic

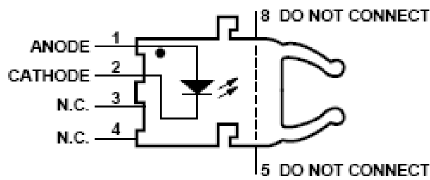
Appendix V. The Versatile Fiber Optic Connection HFBR-0501

The Versatile Link series is a complete family of fiber optic link components

for applications requiring a low cost solution. The HFBR-0501 series includes transmitters, receivers, connectors and cable specified for easy design. This series of components is ideal for solving problems with voltage isolation/insulation, EMI/RFI immunity or data security. The optical link design is simplified by the logic compatible receivers and complete specifications for each component. The key optical and electrical parameters of links configured with the HFBR-0501 family are fully guaranteed from 0ºto 70ºC [12].

Transmitters incorporate a 660 nm LED. Receivers include a monolithic dc coupled, digital IC receiver with open collector Schottky output transistor. A shield has been integrated into the receiver IC to provide additional, localized noise immunity. Internal optics have been optimized for use with 1 mm diameter plastic optical fiber. Versatile Link specifications incorporate all connector interface losses. Therefore, optical calculations for common link applications are simplified [12].

Figure A-3 and A-4 show the schematic of transmitter and receiver, which are connected by optic cable.

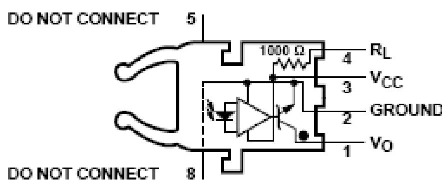


Pin #	Function
1	Anode
2	Cathode
3	Open
4	Open
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Figure A-3 HFBR-0501 transmitter schematic [12]

HFBR-25X1 Receiver



Pin #	Function
1	V_O
2	Ground
3	V_{CC}
4	R_L
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Figure A-4 HFBR-0501 receiver schematic [12]

Figure A-5 shows the typical HFBR-0501 5 Mb interface circuit

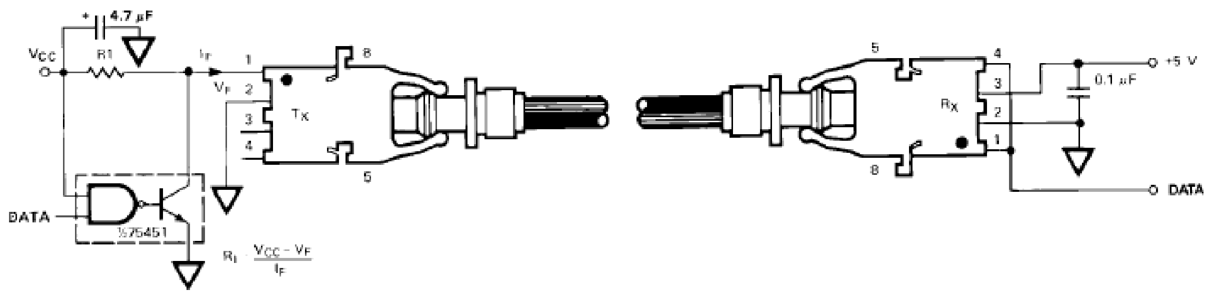


Figure A-5 typical HFBR-0501 5Mb interface circuit [12]

Appendix VI MM74HC4316 Quad Analog Switch with Level Translator

The MM74HC4316 devices are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology [13]. These switches have low "ON" resistance and low "OFF" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa [13]. Three supply pins are provided on the MM74HC4316 to implement a level translator which enables this circuit to operate with 0–6V logic levels and up to ±6V analog switch levels [13]. The MM74HC4316 also has a common enable input in addition to each switch's control which when HIGH will disable all switches to their OFF state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to VCC and ground [13].

Figure A-6 shows the MM74HC4316 connection diagram and Figure A-7 shows the truth table.

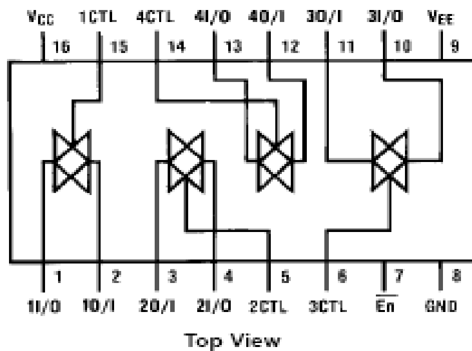


Figure A-6 MM74HC4316 connect diagram [13]

Inputs		Switch
$\overline{En}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"

Figure A-7 MM74HC4316 truth table [13]

Appendix VII. Dual retriggerable monostable multivibrator 74AHC123A

The 74AHC/AHCT123A are dual retriggerable monostable multivibrators with output pulse width control by three methods [14]. The basic pulse time is programmed by selection of an external resistor (REXT) and capacitor (CEXT). The external resistor and capacitor are normally connected as shown in Figure A-8 [14].

For $C_{ext} \geq 10$ nF the typical value of the pulse width t_w (ms) = R_{ext}(kW)*C_{ext} (nF).

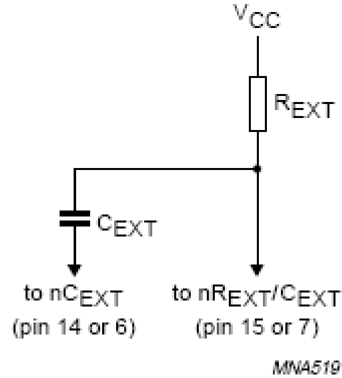


Figure A-8 Timing component connections [14].

Figure A-9 shows the pin configuration of 74AHC123A and Figure A-10 shows the function diagram

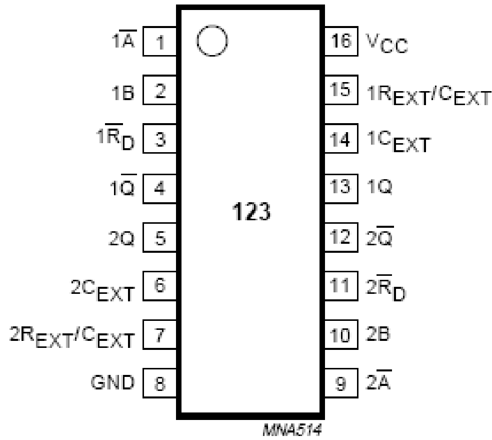


Figure A-9 Chip 74AHC123A pin configuration [14]

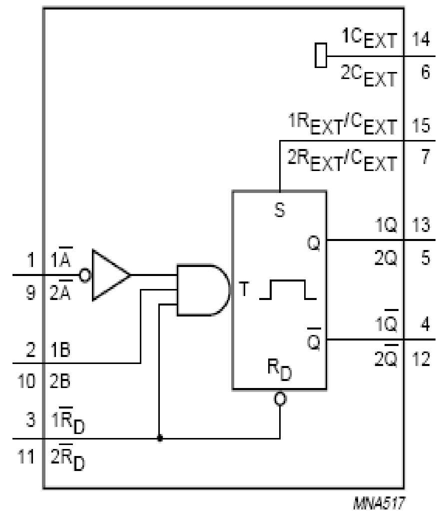


Figure A-10 Chip 74AHC123A function diagram [14]

Appendix VIII. Thermal capacitance computation

Copper

$KtCu := 401 \cdot \frac{watt}{m \cdot K}$ Thermal conductivity of Copper at presumably 25C. Thermal conductivity of a conductor is essentially constant

$CpCu := 389 \cdot \frac{joule}{kg \cdot K}$ Specific heat capacity of Copper at 25C. The specific heat of a material is essentially constant at temperatures above room temperature.

$\rho mCu := 8.96 \cdot 10^{3} \cdot \frac{kg}{m^{3}}$ Mass density of Copper at 25C. Mass density of a material is essentially a constant for temperatures of interest.

$CTCu := CpCu \cdot \rho mCu$ $CTCu = 3.485 \frac{joule}{K \cdot cm^{3}}$

$AreaCu := 0.5 \cdot 0.65 cm^{2}$ Area of the copper

$thCu := 0.1 cm$ thickness of the copper

$CtCu := CTCu \cdot thCu \cdot AreaCu$ Thermal capacitity of the copper

$CtCu = 0.113 \frac{joule}{K}$

$R\theta case := 1.2 \frac{K}{W}$ Thermal resistance of the case

Silicon Carbide

$KtSiC25 := 3.34 \cdot \frac{watt}{cm \cdot K}$ Thermal conductivity of SiC at 25C. Thermal conductivity of a SiC changes with temperature.

$Tj := 200 \cdot K$ $TKo := 273 \cdot K$

$$KtSiC(TC) := \frac{611}{TKo + TC - 115 \cdot K} \cdot \frac{W}{cm}$$

$KtSiC(25K) = 333.88 \frac{watt}{m \cdot K}$

$CpSiC := 700 \cdot \frac{joule}{K \cdot kg}$ Specific heat capacity of SiC

$\rho mSiC := 3.21 \cdot \frac{gm}{cm^{3}}$ Density of SiC

$CTSiC := CpSiC \cdot \rho mSiC$ $CTSiC = 2.247 \frac{joule}{K \cdot cm^{3}}$

$AreaSiC := 1.1 mm^{2}$ Area of the SiC chip

$thSiC := 0.065cm$ Thickness of the SiC chip

$CtSiC := CTSiC \cdot AreaSiC \cdot thSiC$ Thermal capacitance of the SiC chip

$CtSiC = 1.607 \times 10^{-3} \frac{joule}{K}$

$R\theta SiC := \frac{thSiC}{KtSiC(26K) \cdot AreaSiC}$ Thermal resistance of the SiC chip

$R\theta SiC = 1.779 \frac{K}{W}$

$\tau chip := 5 \cdot R\theta SiC \cdot CtSiC$ Computed Time Constant of SiC chip

$\tau chip = 0.014 s$

$\tau case := 5 \cdot R\theta case \cdot CtCu$ Computed Time Constant of the case

$\tau case = 0.68 s$

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