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Fabrication and Characterization of CIS/CdS and Cu2S/CdS Devices for Applications in Nano Structured Solar Cells

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Abstract of Thesis

Fabrication and Characterization of CIS/CdS and Cu_2S/CdS Devices for Applications in Nano Structured Solar Cells

Nano structured solar cells provide an opportunity for increased open circuit voltages and and short circuit currents in solar cells due to quantum confinement of the window and absorber materials and an increase in the optical path length for the incident light. In this study, both bulk and nano heterojunctions of CIS/CdS and Cu_2S/CdS devices have been fabricated and studied on plain glass substrates and inside porous alumina templates to compare their performance. The devices have also been characterized SEM, XRD and J-V measurements. The J-V curves have also been analyzed for series resistance, diode ideality factor and reverse saturation current density.

KEYWORDS: Nano structured solar cells, CIS/CdS, Cu_2S/CdS, porous alumina templates, heterojunction solar cells.

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August 05, 2005

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Fabrication and Characterization of CIS/CdS and Cu_2S/CdS Devices for Applications in Nano Structured Solar Cells

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The Graduate School
University of Kentucky
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Fabrication and Characterization of CIS/CdS and Cu_2S/CdS Devices for Applications in Nano Structured Solar Cells

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THESIS

A thesis submitted in partial fulfillment of the requirements for the degree of
Master of Science in the College of Engineering
at the University of Kentucky

By

Visweswaran Jayaraman

Lexington, KY

Director: Dr. Vijay P. Singh, Professor & Chair

Electrical and Computer Engineering

Lexington, KY

2005

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Chapter 1. Introduction

The present rate of energy consumption in the world is alarming in view of the rapid depletion of conventional energy resources. The known petroleum reserves in the world can provide about 70 Quads (1 Quad ~ 10^{18} Joules), and its cumulative production is about 1.6 Quads [40]. Assuming that there would be no increase in consumption over the years, it is quite apparent that we are heading towards an energy crisis. This could be averted only by a combination of energy conservation and renewable energy resource measures.

Renewable energy sources that could be developed involve, tapping the continuous natural energy flows (such as sunlight, ocean currents, waves, falling water and wind) or any other natural resource whose replenishment in nature is far greater than the projected human use. Of the wide possibilities of energy sources, solar energy is definitely one of the most attractive. Quoting Denis Hayes [1], "no country uses as much energy as is contained in the sunlight that strikes just its buildings."

The direct conversion of solar energy into electricity by a photovoltaic technology has a number of technological and social advantages over other energy technologies. The photovoltaic systems are quiet, require little or no maintenance, can be physically located near the load and are environmentally harmless in their operation. Hence it is one of the most attractive future technologies.

1.1 Thin film solar cells

Photovoltaic technology is based on the thin film form of the suitable photovoltaic material. Thin film devices are typically about 5 to 50 μm thick. Thin films can be

deposited over large areas in any predetermined shape and structure. When devices are fabricated over a large area, the numbers of interconnections are greatly reduced. This gives rise to array configurations and thus high packing densities could be achieved. The ease of production over large areas and the low-cost associated with the polycrystalline thin-film solar cells have satisfied commercial and military satellite requirements [40].

1.2 CIS/CdS thin film solar cells

Copper indium diselenide (CIS or $CuInSe_2$) is an established material for solar cell applications. Interest in $CuInSe_2$ dates back to the work of Wagner, et al., [2] who demonstrated a 12% conversion efficiency using single crystals. The extraordinarily high absorption coefficient of CIS makes thin-film devices practical, while an optical band gap of 1.05 eV is too low for optimum conversion efficiencies. Thin-film solar cells with a conversion efficiency of 6.6% were fabricated by Kazmerski et al., [3] by simultaneous evaporation from $CuInSe_2$ and Se sources. Interest in CIS for thin-film solar cells significantly increased with the results reported by R. A. Mickelsen, who demonstrated 10.6% efficient cells [4] fabricated by physical evaporation of the three elements onto Mo-coated substrates. The key to increase the open-circuit voltage and the photo-current of the device is to use to the wider bandgap window material. The optical bandgap of the absorber layer can be increased by the use of alloys in which Ga is substituted for In. This resulted in increased conversion efficiencies [4].

$CuInSe_2$ thin-film devices have been fabricated by several different methods. Physical vapor deposition (PVD) and selenization of the deposited metals have yielded high efficiency devices [5-8]. CIS device fabrication methods such as sputtering [9-10],

spray deposition [11], direct evaporation [12] and screen printing [13], have been less successful in yielding high-efficiency devices. Electrodeposition is considered as an alternative low cost method for CIS film preparation [14-16]. A. Kampmann et al., have demonstrated an efficiency of 1.5% [17] with single step electrodeposited CIS in superstrate configuration. CIS solar cells in the front wall configurations have yielded efficiencies of 9.4% [18]. High open circuit voltage of 420 mV and high short circuit current density of 25 $mA.cm^{-2}$ have been achieved by single step electrodeposition of CIS onto CdS-coated substrates [19]. Efficiencies as high as 8.8% have been reported on CIS solar cells made on Mo-coated glass substrates [20].

Recent studies have shown that the bandgap of a material can be increased by reducing its particle size [21]. For a heterojunction to yield high efficiencies, the n-type window material should have a wide bandgap so that maximum amount of light can be incident on the absorber and the p-type material should have a lower bandgap so that maximum absorption of the incident light can take place. An absorber material with a bandgap in the range of 1.1 eV to 1.5 eV would take advantage of the solar spectrum for maximum absorption of sunlight.

In this thesis, an attempt has been made to take advantage of the increased bandgap of nano CdS. Also the as-deposited CIS had nano feature sizes which would increase its bandgap from a low 1.02 eV. An increase in bandgap of the window material, along with a fine tuning of the bandgap of the absorber material closer to the solar absorption spectrum, is expected to give higher efficiencies for the solar cells. Back-wall heterojunctions have been made on ITO-coated glass with bulk CdS/bulk CIS and bulk CdS/nano CIS. Front wall heterojunctions have been made on Mo-coated glass with bulk

CdS/bulk CIS and nano CdS/bulk CIS. Nano crystalline CdS is fabricated by ultrasound technique and CIS is deposited by electrodeposition technique. The devices are characterized by SEM, XRD and I-V measurements.

1.3 Cu_2S/CdS thin film solar cells

Cu_2S possesses extremely favorable material characteristics, which make it suitable for large-scale photovoltaic applications. Cu_2S has a very good photovoltaic application in particular with CdS or ZnCdS. The Cu_2S/CdS thin film heterojunction solar cell has been the most extensively researched thin film photovoltaic system [22-25].

Cu_2S/CdS thin film solar cells have been fabricated by a variety of techniques including a combination of evaporation and chemiplating [26-27], all evaporation [28], a combination of spray pyrolysis and chemiplating [24] and sputtering [29]. Chemiplated Cu_2S/evaporated $Zn_xCd_{1-x}S$ (with anti-reflective coating) thin film solar cells on Zn/Cu substrates have exhibited the highest efficiencies [30]. These cells had a V_{oc} of 0.599 V, a J_{sc} of 18.5 $mA.cm^{-2}$, a fill- factor of 0.748 and an efficiency of 10.2%. Cu_2S/CdS (with anti-reflective coating) thin film solar cells, fabricated by chemiplating an evaporated CdS layer, had a conversion efficiency of 9.15% with V_{oc} = 0.516, J_{sc} = 21.8 mA/cm^{-2} and FF = 0.714 [27, 30]. Spray deposited cells had efficiencies of up to 5.3% over a 1-cm^2 area [24]. Spray deposited thin film cells in general exhibit lower efficiencies than the corresponding evaporated cells. Reactively sputtered Cu_2S/evaporated CdS thin film solar cells on Au coated glass substrates exhibited best efficiencies of about 4%. Lower efficiencies have been obtained on all sputter-deposited Cu_2S/ CdS cells. Cu_2S/CdS cells are generally prone to degradation over time as the copper ions start moving about.

Exposing the Cu_xS surface to strong oxidizer such as oxygen can cause a substantial degradation in device performance [31]. The Cd atoms were found to move rapidly to both the Cu_xS surface and the CdS-Cu_xS interface on exposure to air at room temperature [32]. The degradation of the Cu_2S/CdS cells, attributed to the formation of surface oxides, can be significantly prevented by replacing the ambient air with argon [33].

In this thesis Cu_2S/CdS solar cells have been fabricated by an all evaporation process. CdS and CuCl are successively evaporated onto ITO-coated glass substrate and the CuCl is converted into Cu_2S by annealing the device in vacuum. A thin layer of copper is evaporated on top of Cu_2S to correct its stoichiometry. A variety of contacts including copper, silver and a combination of chromium/lead have been evaporated to serve as top contacts for Cu_2S. The devices are electrically characterized by I-V measurements.

1.4 Nano-structured Cu_2S/CdS solar cells

A nano-structured solar cell has a nano-scale heterojunction between the n and p type materials forming the heterojunction. The nano confinement of a particle is found to increase its bandgap [21]. With the increased bandgap of the n-type material one can expect more of the incident light to pass through to the absorber. The nano confinement also increases the usually lower bandgap of the absorber material closer to the ideal solar spectrum absorption values. With the increased absorption of the solar energy it can be expected that the open circuit voltage of such devices would increase. The nano confinement of the absorber material would also give rise to multiple light reflections at their grain boundaries. This will increase the optical path length of the incident light and

thus create more electron-hole pairs. This leads to increased short circuit currents in the devices. With the increase in V_{oc} and J_{sc} for these devices the efficiencies are also expected to go up.

In this thesis an attempt has been made to fabricate nano-scale heterojunctions inside porous alumina templates. Until recently, porous alumina templates have been used as masks to fabricate ordered arrays of nano particles [34-37]. In this work a Cu_2S/CdS heterojunction has been fabricated inside the porous alumina template and the template has been used to hold the junction intact. CdS and CuCl have been thermally evaporated onto the porous alumina template. The Cu_2S/CdS heterojunction is formed inside the pore by annealing the alumina template in vacuum. A thin layer of copper is thermally evaporated onto Cu_2S to correct its stoichiometry. A combination of thermally evaporated chromium/lead has been used as the top contact for Cu_2S. ITO has been sputtered on the back side of the porous alumina template to act as ohmic contact to CdS. The devices are then electrically characterized by I-V measurements.

Chapter 2. Theory

2.1 Theory of Heterojunction Solar Cells

A heterojunction is formed between two semiconductors with different crystal structure, bandgap and other properties. Heterojunctions are classified as abrupt, graded, isotype and anisoptype. If the transition between one material to the other takes place over a distance of many lattice constants, the heterojunction is said to be graded. If the transition is characterized by a sharp change in interface, with a sudden change in properties within a very small distance, the junction is said to be abrupt. If a junction exhibits rectification, even if both the materials forming the heterojunction have the same type of doping, it is said to be isotype. If the doping is of the opposite type in the two materials, the junction is said to be anisotype. This section focuses on the narrow gap p-type, wide gap n-type abrupt heterojunction relevant to the CIS/CdS and Cu_2S/CdS systems.

2.1.1 Energy Band Diagram of a Heterojunction Solar Cell

When semiconductors of different bandgaps, work functions and electron affinities are brought together to form a junction, one can expect to see discontinuities in the energy bands as the Fermi levels line up at equilibrium. This is shown in Figure 2.1. The discontinuities in the valence band ΔE_v and the conduction band ΔE_c accommodate the difference in the bandgap between the two semiconductors ΔE_g. In an ideal case, ΔE_c would be the difference between the electron affinities, and ΔE_v would be found from $\Delta E_g - \Delta E_c$. This is known as the Anderson affinity rule [44].

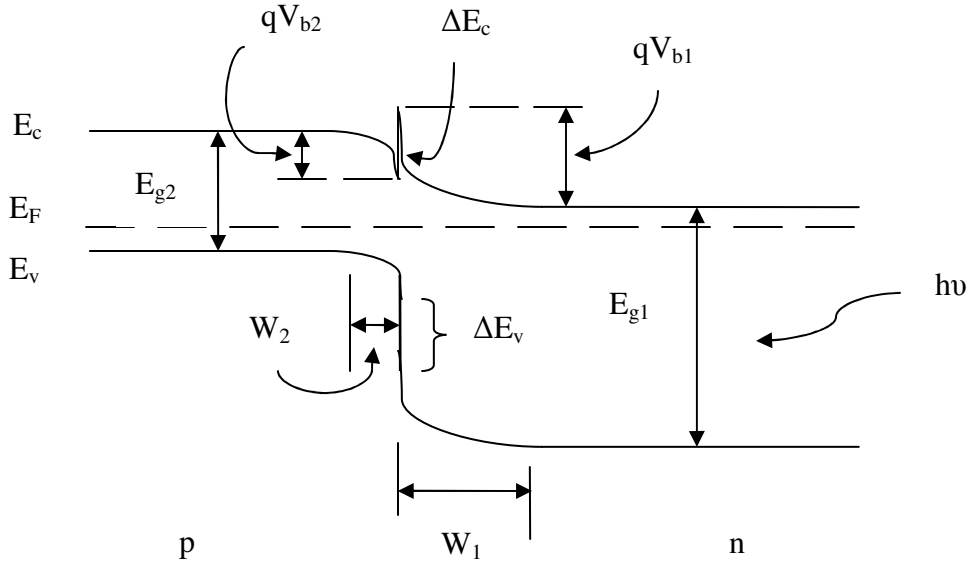

Figure 2.1 Energy band diagram of a heterojunction solar cell

Light with energy less than E_{g1} but greater than E_{g2} will pass through the n-type semiconductor, acting as the window material, and be absorbed by the p-type material. Absorption of light in the depletion region and within a diffusion length of the junction in the absorber will create carriers which will be collected. Light with energy greater than E_{g1} will be absorbed by the n-type material, and the carriers created in the depletion region and within a diffusion length of the junction will also be collected. The separation of the light-generated carriers across the junctions gives rise to the light- generated current I_L. The advantages of heterojunction solar cells over conventional p-n junction solar cells are [38],

1. enhanced short-wavelength response, if E_{g1} is large enough for the high-energy photons to be absorbed in the depletion of the p-type semiconductor;

2. lower series resistance, if the n-type semiconductor can be heavily doped without affecting its light transmission characteristics; and

3. high radiation tolerance, if the n-type semiconductor is thick in addition to being high in bandgap.

2.1.2 Equivalent Circuit of a Solar Cell

The equivalent circuit of a solar cell is shown below in Figure 2.2. The light-generated current I_L is represented by a constant current source.

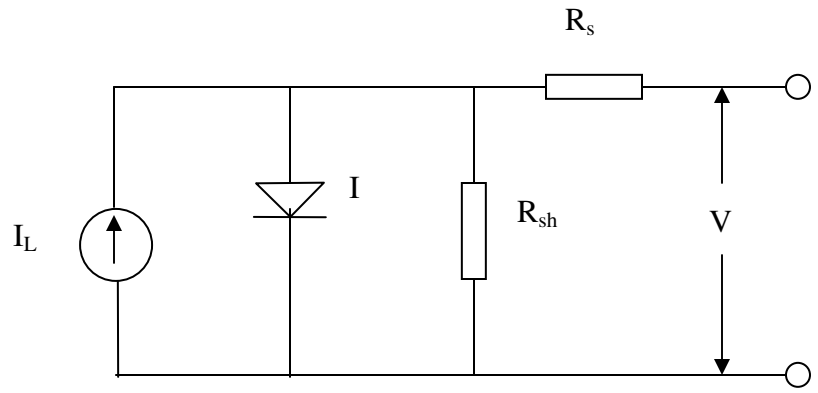

Figure 2.2 Equivalent circuit of a solar cell

Here, I_L is the light-generated current,

R_s is the series resistance associated with the device,

R_{sh} is the finite shunt resistance between the Cu_2S/CdS junction,

I is the current through the device, and

V is the voltage across the device.

The series resistance, R_s, arises due to the resistance associated with quasi neutral regions and the ohmic contacts of the n and p type material. The shunt resistance R_{sh}, arises due to the presence of shunting paths formed between Cu_2S and CdS layers during fabrication. Hence the total current I, flowing through the device can be written as,

$$I - \frac{(V - IR_s)}{R_{sh}} = I_0\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] - I_L \quad \text{.....(2.1)}$$

2.2 Photovoltaic Parameters

The short-circuit current, open-circuit voltage, power output, fill factor and efficiency of a solar cell are collectively called the photovoltaic parameters.

2.2.1 Short-Circuit Current

The short-circuit current I_{sc} is the current that flows through the junction under illumination at zero applied bias. In the ideal case (neglecting the effects of R_s and R_{sh} resistances) it is equal to the light-generated current I_L and proportional to the incident number of photons or the illumination intensity.

2.2.2 Open-Circuit Voltage

The open-circuit voltage is the voltage across the device at zero current through the device. Assuming a diffusion current dominated model for the junction, V_{oc} is given by,

$$V_{oc} = \frac{nkT}{q}\ln\left[\frac{I_{sc}}{I_0} + 1\right] \quad \text{.....(2.2)}$$

It appears from the above equation that large values of n would be desirable in obtaining high open-circuit voltages, but this is not the case, since high values of n are associated with high values of I_0. V_{oc} for a p-n junction is always higher for lower values of n (ideally n = 1).

2.2.3 Power Output

The output power is given by,

$$P = IV = I_0 V\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] - I_{sc}V \quad \text{.....(2.3)}$$

The condition for maximum power is obtained by setting $\partial P / \partial V = 0$;

this yields a current output at maximum power as

$$I_m = (I_{sc} + I_0)\frac{qV_m / nkT}{1 + qV_m / nkT} \quad \text{.....(2.4)}$$

and the voltage at maximum power point as,

$$\exp\left(\frac{qV_m}{nkT}\right)\left[1 + \left(\frac{qV_m}{nkT}\right)\right] = \left(\frac{I_{sc}}{I_0}\right) + 1 = \exp\left(\frac{qV_{oc}}{nkT}\right) \quad \text{.....(2.5)}$$

The maximum power output can be calculated as $P_m = I_m V_m$.

2.2.4 Fill Factor

The fill factor is defined as $V_m I_m / V_{oc} I_{sc}$. It is a measure of the squareness of the I-V curve. When the series and shunt resistance effects cannot be ignored, the two ratios V_m/V_{oc} and I_m/I_{sc} and the fill factor are all reduced.

2.2.5 Efficiency

The efficiency η of a solar cell is defined as the ratio of the maximum output power obtainable from the solar cell to the incident power.

$$\eta = V_m I_m / P_{in} \quad \text{.....(2.6)}$$

$$P_m = V_m I_m = V_{oc} I_{sc} FF$$

Therefore, the conversion efficiency of a solar cell is given by,

$$\eta = (V_{oc} I_{sc} FF / P_{in}) \times 100\% \quad \text{.....(2.7)}$$

When there are non-negligible series and shunt resistive effects, the V_{oc}, I_{sc} and FF are lowered. This leads to a reduction in the efficiency of the solar cell as can be seen from equation 2.7.

2.3 Energy Band Diagram of CIS/ CdS heterojunction

The energy band diagram of the CIS/CdS heterojunction is shown below in Figure 2.3.

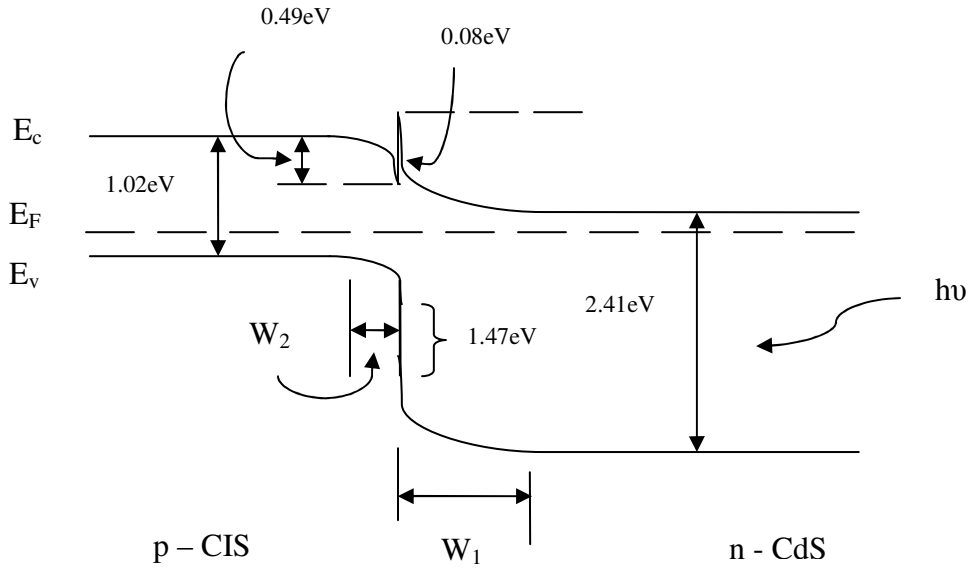

Figure 2.3 Energy band Diagram of CIS/CdS heterojunction

Light with energy less than 2.41 eV but greater than 1.02 eV will pass through the CdS layer, acting as the window material, and be absorbed by the CIS layer. Absorption of light in the depletion region and within a diffusion length of the junction in CIS will create carriers which will be collected. Light with energy greater than 2.41 eV will be absorbed by the CdS layer, and the carriers created in the depletion region and within a

diffusion length of the junction in CdS will also be collected. The separation of the light-generated carriers across the CdS/CIS junction gives rise to the light-generated current I_L.

2.4 Energy Band Diagram of Cu_2S/CdS heterojunction

The energy band diagram of the Cu_2S/CdS heterojunction is shown below in Figure 2.4.

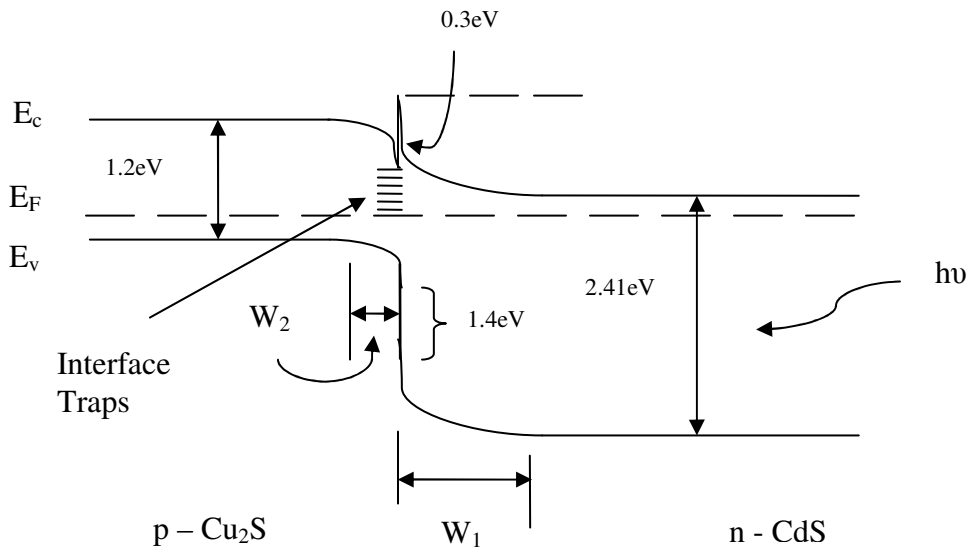

Figure 2.4 Energy band diagram of Cu_2S/ CdS heterojunction

Under illumination, most of the light is absorbed in the p-type Cu_2S layer. Thus the Cu_2S layer accounts for most of the light-generated carriers. Freshly prepared cells consist of uncompensated CdS and nearly stoichiometric Cu_2S. The space charge would thus be narrow and ionization of deep levels near the junction on illumination causes further narrowing. Tunneling to interface states occurs, lowering the effective barrier height and hence the V_{oc}. Heat treatment of the cell allows oxygen and/or copper to reach the space-charge region, forming compensating acceptor states in the CdS. This process

widens the space-charge region which restricts tunneling. With the increased barrier, an improvement in V_{oc} could be expected. A major factor affecting the photocurrent in Cu_2S solar cells is the high surface recombination velocity which results in most of the photo-generated carriers close to the surface to be captured. Surface recombination can be reduced by proper doping of the region closer to the surface, to produce a drift field to counteract the minority carrier diffusion to the surface [40].

Chapter 3. Experimental

3.1 Fabrication of CIS/CdS Devices

3.2 Device Structures

CIS/CdS devices were fabricated on two different kinds of substrates, namely molybdenum-coated glass and ITO (Indium Tin Oxide)-coated glass. The front wall heterostructures used molybdenum-coated glass as the substrate, and the back wall heterostructures used ITO-coated glass as the substrate. To compare the nano scale heterojunctions against bulk junctions, both types of junctions have been fabricated on molybdenum-coated glass and ITO-coated glass.

3.2.1 Devices configurations on ITO coated glass substrates

Figure 3.1 shows the device configuration for bulk heterojunctions made on ITO coated glass substrates.

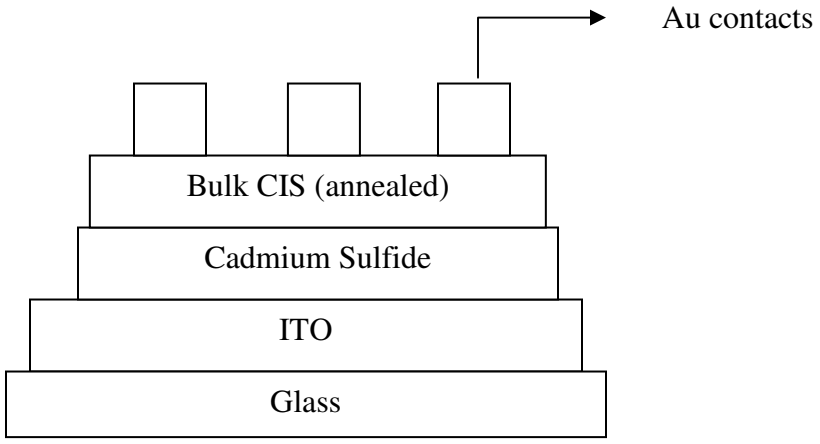

Figure 3.1 Back wall heterojunction (bulk CIS/CdS) on ITO-coated glass

The device configuration in Figure 3.2 shows a nano heterojunction made on ITO coated glass substrate. The deposited films of CIS had particle sizes in the range of 30 nm - 35 nm.

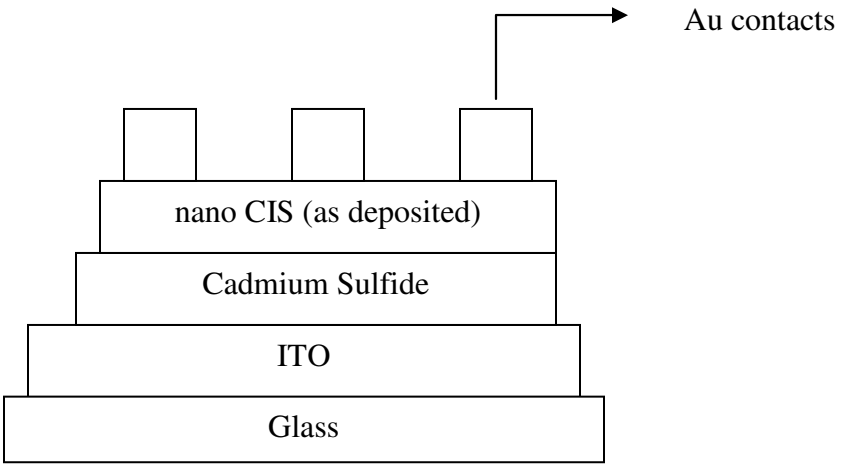

Figure 3.2 Back-wall heterojunction (nano CIS/ bulk CdS) on ITO coated glass

3.2.2 Device configurations on molybdenum coated glass

The front wall device configurations were studied with molybdenum-sputtered glass substrates. Figure 3.3 and Figure 3.4 illustrate the bulk and nano heterojunctions fabricated in the front-wall configuration. To fabricate the nano heterojunction, a thin layer of ultrasound-assisted CdS was deposited on top of thermally evaporated CdS.

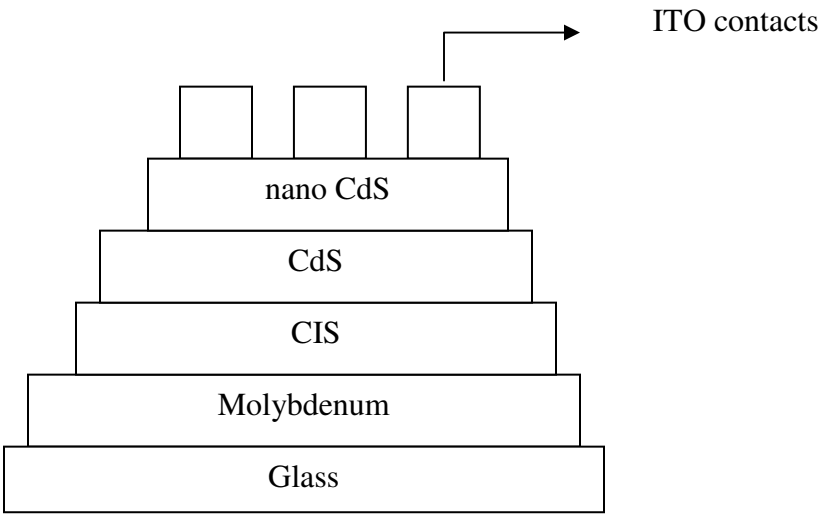

Figure 3.3 Front-wall heterojunction (bulk CIS/nano CdS) on Mo-coated glass

The front wall configuration for the bulk device is the same as shown in Figure 3.3, except without the nano CdS layer, and is shown in Figure 3.4.

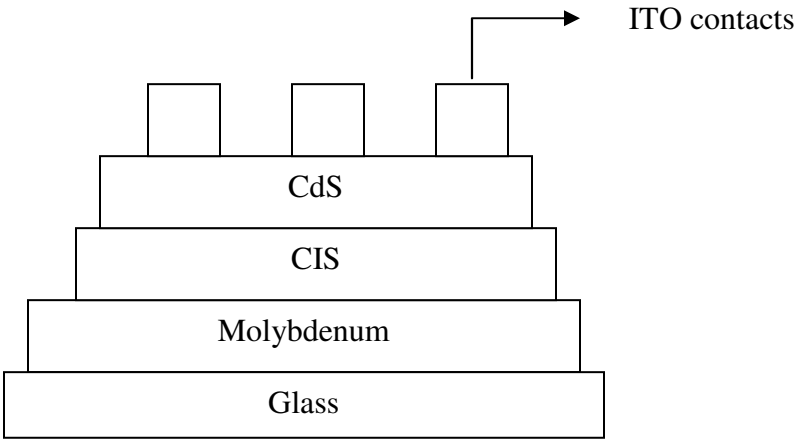

Figure 3.4 Front-wall heterojunction (bulk CIS/ CdS) on molybdenum-coated glass

3.3 Substrate Cleaning

Two types of substrates were used for the front-wall and back-wall heterojunctions. Glass was used as the substrate for the front wall configuration and ITO-coated glass was used as the substrate for the back-wall configuration. An identical cleaning process was adopted for both kinds of substrates.

The ITO-coated glass substrates had to be cleaned thoroughly prior to the fabrication of the devices. Cleaning was an important process in obtaining a smooth, contaminant-free semiconductor film. The substrates were initially cleaned with running de-ionized water and then placed in a beaker containing acetone. This beaker was then immersed in an ultrasound sonicator for 10 minutes. The substrates were then cleaned in running de-ionized water, immersed in a beaker containing methanol and sonicated for 10

minutes. The substrates were finally rinsed in de-ionized water and dried in a jet of flowing nitrogen.

3.4 Fabrication of back wall or superstrate heterojunction

The back wall configuration consists of glass/ITO/CdS/CIS/Au. The ITO-coated glass was cleaned with the substrate cleaning procedure detailed above in section 3.3.

3.4.1 Fabrication of the CdS layer

Cadmium sulfide was used as the n-type material for the pn heterojunction. CdS was fabricated by thermal evaporation. The cleaned ITO-coated glass substrate was mounted on a disc on the thermal evaporator. A portion of the substrate was masked with aluminum foil in order to provide contact to ITO. Cadmium sulfide powder was loaded into a molybdenum boat and covered with glass wool. The presence of the glass wool ensures that CdS evaporates in the form of very fine powder on the ITO-coated glass substrate, giving a more uniform deposition. After loading CdS, the vacuum chamber was closed and the thermal evaporator was allowed to pump down. Once the pressure inside the chamber went down to 4e-06 Torr, the molybdenum boat was heated by passing current through the two ends clipped to the evaporation source. This process heats up the CdS powder and starts the deposition of CdS onto ITO. A constant current was passed in order to maintain a uniform deposition rate. Once the thickness of the film reached close to 500 nm, the current source was turned off and the deposition was stopped. The vacuum chamber was allowed to cool down for one hour, then vacuum was broken by letting nitrogen into the chamber. The samples were then removed from the chamber and stored in an air-tight container.

3.4.2 Fabrication of Copper Indium Diselenide layer

A three-electrode electrochemical cell was used for the fabrication. The setup consisted of a three-electrode electrochemical cell connected to a potentiostat which was interfaced to a personal computer. The setup used for the electrodeposition is shown below in Figure 3.5.

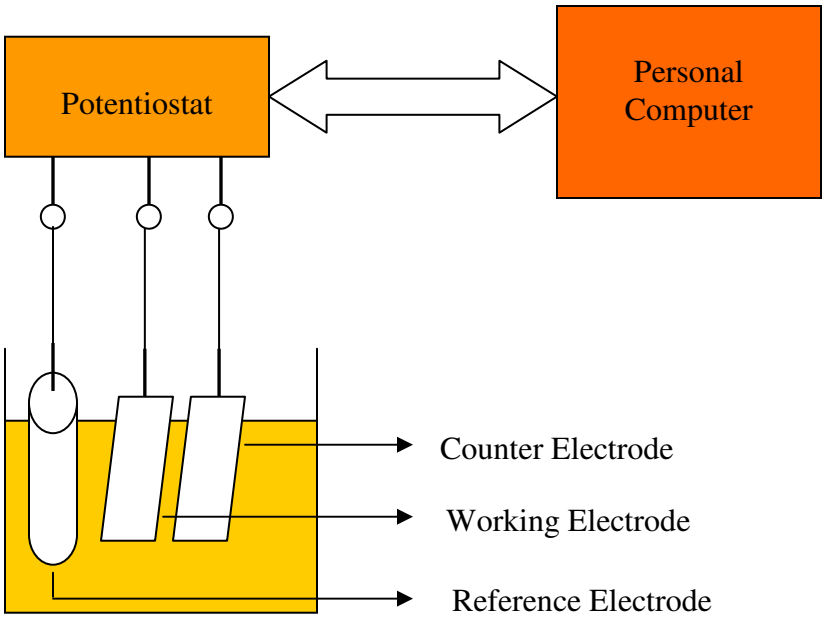

Figure 3.5 Three electrode electrodeposition setup

The electrodeposition of CIS was done potentiostatically in an electrochemical cell at room temperature, from a solution containing 1.0e-03 M Copper Sulfate, 1.7e-03 M Selenium Dioxide, 3.0e-03 M Indium Sulfate and 0.3 M Potassium Sulfate acting as the supporting electrolyte. The volume of the solution prepared was 200 mL. The pH of the solution was adjusted to 2.45 with dilute sulfuric acid. The solution was prepared with analytical grade chemicals from Sigma-Aldrich and de-ionized water. All depositions were carried out using a Princeton Applied Research 273A potentiostat at room temperature. ITO-coated glass and a platinum electrode were used as the working and

counter electrode respectively. The applied electrodeposition potential was -0.70 V vs. a Saturated Calomel Electrode (SCE). The computer controlled the duration of deposition that was desired. A small jet of nitrogen was passed on top of the solution throughout the duration of the deposition, to prevent the oxidation of the CIS film that formed. By varying the duration of deposition, films different thickness can be produced. The electrodeposition process yielded a layer of CIS with an average particle size of about 30 nm. Varying the applied potential can vary the relative ratios of Copper, Indium and Selenium.

3.4.3 Heat treatment of Copper Indium Diselenide

The heat treatment of CIS, as opposed to the as-deposited films, improves the crystallinity of the films. The heat treatment process lends CIS a chalcopyrite structure, which makes it a better photovoltaic material. The heat treatment was done in a cylindrical glass furnace with an inlet for nitrogen at one end and the sample at the other end. The partially completed device (glass/ITO/CdS/CIS) was inserted through the opening in the glass furnace and sealed with a cylindrical glass lid with an outlet for nitrogen. The glass chamber was first purged for 25 minutes with nitrogen to remove any residual oxygen. This is important since heating the chamber with residual oxygen would result in oxidizing the sample. The sample was annealed at 350^{o}C for one hour with nitrogen flowing through the chamber. The heating source was then switched off and the chamber was allowed to cool for about four hours. The sample was then removed and stored in an air-tight container.

3.4.4. Thermal evaporation of gold for the top contact

Gold is known to make an ohmic contact with CIS. Gold was deposited as the top contact for CIS by thermal evaporation. The device was covered with an aluminum mask with holes punched to as openings for the metal contact, then loaded into the vacuum chamber. Small strips of gold wire were placed on a tungsten filament for evaporation. Current was then passed through the filament to evaporate the gold wire onto the device. A thin film of gold approximately 150 nm thick was deposited. The chamber was allowed to cool down for one hour and the samples were removed. Two different kinds of junctions were made. The as-deposited CIS films formed a heterojunction with nano CIS and bulk CdS. The annealed devices formed a bulk heterojunction between CIS and CdS.

3.5 Fabrication of front wall heterojunction

The front wall configuration consists of glass/Mo/CIS/CdS/ITO. The glass substrate was cleaned with the substrate cleaning procedure detailed in section 3.3.

3.5.1 Sputtering of Molybdenum for back contact

Molybdenum was deposited onto the cleaned glass substrates through RF sputtering technique. The cleaned glass substrate was loaded into the load lock chamber of the sputtering machine and allowed to pump down. Once a low pressure was reached in the load lock chamber, the sample was transferred from the load lock chamber onto the main chamber and set in place. Plasma was fired between the target and the sample. The rate of deposition on the sample was fixed at 0.1 Å/sec and the process was allowed to run until a thickness of 500 nm was reached. The plasma was then switched off and the

chamber was allowed to cool down. The sample was transferred from the main chamber into the load lock chamber. The load chamber was vented to remove the sample.

3.5.2 Fabrication of the Copper Indium Diselenide layer

CIS was fabricated on molybdenum-sputtered glass substrates by two methods. In the first method, metallic sulfates were used in the electrolytic bath and in the second method, metallic chlorides were used in the bath.

3.5.2.1 Fabrication of Copper Indium Diselenide with metallic sulfates

The fabrication of CIS with metallic sulfates was carried out by the same method as detailed in section 3.4.2.

3.5.2.2 Fabrication of Copper Indium Diselenide with metallic chlorides

A three-electrode electrochemical cell was used for the fabrication. The setup consisted of a three-electrode electrochemical cell connected to a potentiostat which was interfaced to a personal computer. The setup used for the electrodeposition is shown in Figure 3.5. The electrodeposition of CIS was done potentiostatically in an electrochemical cell at room temperature from a solution containing 2.6e-03 M of Cuprous Chloride ($CuCl_2.2H_2O$), 9.6e-03 M Indium Chloride ($InCl_3$) and 5.5e-03 M Selenous Acid (H_2SeO_3), with 0.236 M Lithium Chloride (LiCl) acting as the supporting electrolyte. The bath was buffered using a pH = 3 pHydrion buffer, giving pH ~ 2.6. A platinum electrode was used as a counter electrode and a molybdenum-coated glass substrate was used as the working electrode. A saturated calomel electrode (SCE) was used as the reference electrode. All depositions were carried out using a Princeton Applied Research 273A potentiostat at room temperature from a stirred bath. Good CIS films were obtained when a multi-potential regime, of 20 minutes at -0.5 V vs. SCE

followed by 50 minutes at -0.6 V vs. SCE, was used. After the deposition the films were rinsed with distilled water and dried under flowing nitrogen. The film was then annealed in nitrogen at a temperature of about 450 ^{o}C for one hour.

3.5.3 Fabrication of Cadmium Sulfide

A cadmium sulfide layer of thickness 700 nm was then deposited onto the CIS by thermal evaporation as detailed in section 3.4.1.

3.5.4 Fabrication of nano CdS by ultrasound technique

A very thin layer of nano CdS was deposited onto thermally evaporated CdS by an ultrasound technique. The existence of this layer increased the bandgap of the window material [39]. CdS was deposited by chemical bath deposition technique. When the chemical bath is immersed in an ultrasound medium, the deposited CdS particles attain nano feature sizes [39].

A beaker was filled with 194.6 mL of water and 5.4 mL of Ammonium Hydroxide. To this 1.6 g of Cadmium Chloride and 2.1 g of Ammonium Chloride were added. The solution was stirred with a magnetic stirrer and heated simultaneously till it reached a temperature of 70 ^{o}C. Meanwhile water was heated in a beaker to a temperature of about 70 ^{o}C and poured into the ultrasound sonicator. When the temperature of the chemical bath reached 70 ^{o}C, 2.3 g of thiourea was added to it to begin the formation of cadmium sulfide. The chemical bath was then immersed in the sonicator and the partially completed device (glass/Mo/CIS) was immersed into the chemical bath for 5 minutes. CdS was deposited onto the substrate by ultrasound waves generated by the sonicator. The device was then rinsed with DI water and dried under flowing nitrogen.

3.5.5 Sputtering of ITO for top contact

ITO is known to make an ohmic contact with CdS. ITO contacts to CdS were established with sputtering. ITO was deposited on top of CdS covered with an Aluminum foil with small holes acting as openings for device contacts. The sputtering was carried out as detailed in section 3.5.1.

3.6 Fabrication of Cu_2S/CdS Devices

3.7 Device Structures

Devices with structures ITO/CdS/Cu_2S/Cu/Ag or Cu/Pb on a glass substrate and a porous alumina foil were fabricated. The two structures were fabricated in order to compare the performance of the solar cells on a flat substrate against those inside nano-porous templates.

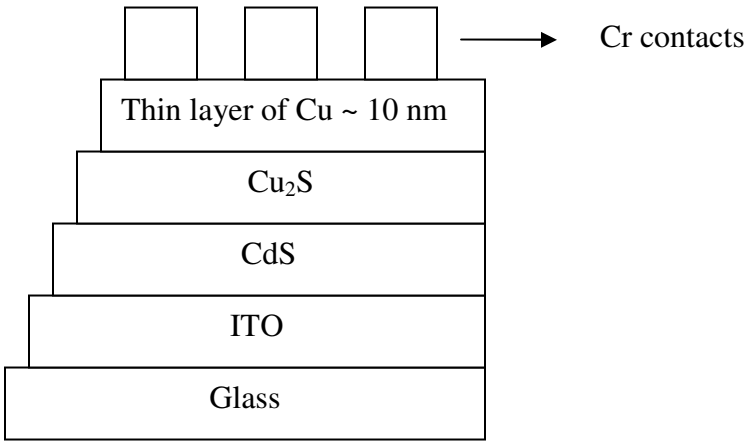

Figure 3.6 Structure of devices fabricated on glass substrate

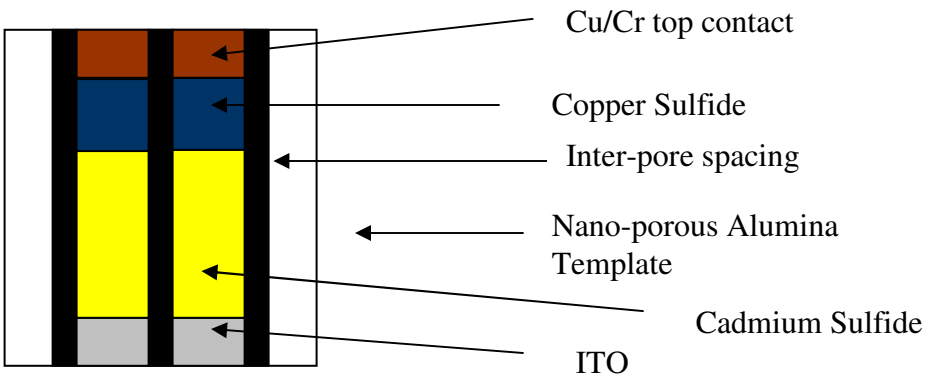

Figure 3.7 Structure of devices fabricated inside nano-porous alumina template

The two structures fabricated are shown in Figures 3.6 and 3.7. The Indium Tin Oxide (ITO)-coated glass substrates used for device fabrication were purchased from Delta Technologies, Limited, Stillwater, MN-55082. The glass substrate provides mechanical support to the devices, while the transparent conductive layer ITO acts as a bottom contact for the cadmium sulfide film.

3.8 Substrate Cleaning

ITO-coated glass substrates were used in the fabrication of the solar cells. The substrates were cleaned with the same procedure as detailed in section 3.3.

3.9 Fabrication of Cu_2S/CdS Devices on flat substrates

3.9.1 Fabrication of polycrystalline Cadmium Sulfide films

Polycrystalline films of CdS were fabricated on ITO-coated glass substrates by thermal evaporation of CdS powder. Evaporation grade CdS powder of 99.9% purity was purchased from AlfaAesar. The ITO-coated glass substrates were covered with aluminum

foil masks with square openings. This confines the CdS films to a square shaped area well away from the edges of the ITO coated glass substrate, thereby preventing the possibility of films grown on top of CdS shorting with ITO. Thermal evaporation is one of the physical vapor deposition techniques employed to obtain uniform films on flat substrates. The technique involves passing a high current through a filament or a boat containing the material to be deposited. The filament/boat has a higher melting point than the material to be deposited. The high current melts the source material and produces vapors which rise through the chamber and deposit on the substrates. A molybdenum boat was used to evaporate CdS. The molybdenum boat was half filled with CdS purchased from AlfaAesar and connected to the evaporation source. A ball of glass wool was paced on top of CdS to prevent it from jumping inside the boat. This also aids in uniform deposition of CdS on the substrates. A current of the order of 4A was passed through the molybdenum boat and the pressure in the chamber was maintained close to 4 e-06 Torr. The target substrates were clipped onto a disc at the top of the chamber. The disc was rotated at a constant speed to avoid shadowing effects and hence obtain a uniform film of the deposited material. When the current through the boat was increased the pressure inside the chamber increased due to the heating of the boat and the subsequent rise of vapors of CdS. Maintaining a low pressure inside the chamber was critical in obtaining uniform films. In the absence of a low pressure the vapors from the source material could get deflected and produce a non-uniform film on the substrates. Further more a good vacuum inside the chamber prevents the oxidation of the source material. Hence in order to maintain a low pressure inside the chamber, the current through the boat was slowly increased in steps. For every step increase in current through

the boat, the pressure inside the chamber was allowed to stabilize before any further increase in current could be made. Once the desired rate of CdS deposition was achieved, the current through the boat was kept constant. When the thickness monitor indicated the film thickness desired, the current through the boat was switched off. The chamber was then allowed to cool down before venting and subsequent removal of the substrates.

3.9.2 Annealing

The cadmium sulfide films deposited by thermal evaporation were subjected to an annealing treatment in a nitrogen atmosphere. Annealing is a process wherein the films are heated at a very high temperature in a quartz furnace tube in an atmosphere of a preferred gas. The annealing process helps in recrystallizing the CdS film and hence improves the film adhesion and grain size. Figure 3.8 shows the quartz furnace tube used for the purpose. The quartz furnace tube consisted of an inlet for nitrogen, attached to a nitrogen cylinder at one end and an outlet for nitrogen at the other end. The nitrogen outlet tube was kept immersed in a bottle containing water. The quartz tube had three zones namely, Zone 1, Zone 2, and Zone 3.

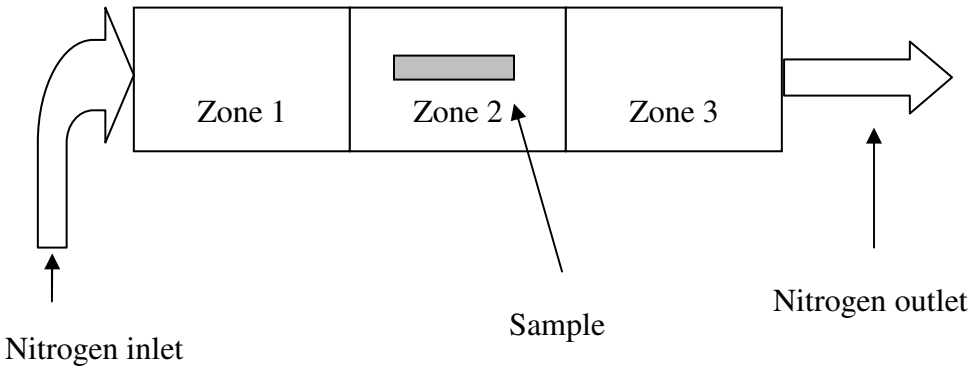

Figure 3.8 Quartz furnace tube used for annealing

The temperature at which the sample is to be annealed is best maintained in zone 2, hence the sample to be annealed was positioned at the center of zone 2. Prior to heating the sample, the quartz furnace tube was purged with flowing nitrogen for duration of 25 minutes to remove any oxygen present in the tube. This was an important step, as any resident oxygen in the chamber could oxidize the sample during heating. After purging, the sample was heated at a temperature of 450^{o}C for 90 minutes. The furnace was then switched off and allowed to cool down to room temperature. Finally the sample was removed from the quartz furnace tube.

3.9.3 Fabrication of Cuprous Chloride film

A uniform film of cuprous chloride (CuCl) was deposited on top of the annealed CdS film by thermal evaporation. Copper (I) chloride of 99.999% purity was purchased from AlfaAesar. The commercially bought Copper (I) chloride is green in color due to the exposure to atmospheric oxygen and needs to be bleached to turn it to its natural pale white color. In a preferred process, an amount of copper chloride was prepared to form a layer of one micron thick on the crystalline CdS layer. The CuCl was bleached in a dilute hydrochloric acid solution, typically about a 10% solution, and then rinsed in acetone. The powder was then placed in a molybdenum boat and loaded into the thermal evaporator. The pressure inside the thermal evaporator was maintained close to 4e-06 Torr. Aluminum foil masks with small circular holes were wrapped on top of the CdS films. This was done to make sure that the heterojunction was confined to a smaller area in order to get a realistic estimate of short circuit currents. The CdS films were loaded onto a circular disc at the top of the chamber. A current in the order of 2.5A was passed through the boat. The circular disc holding the substrates was rotated at a constant speed

in order to obtain uniform deposition. The thermal evaporation process was carried out as described in section 3.9.1.

3.9.4 Post heat treatment to convert CuCl into Cu_2S

The CuCl layer deposited has to react with the CdS layer in order to form Cu_xS. This was preferably done in the vacuum chamber following the CuCl deposition. The following reaction takes pace as a result of heating the substrates.

$$CdS + 2\,CuCl \longrightarrow Cu_2S + CdCl_2$$

The substrate temperature was heated to a temperature in the range of 190 ^oC – 200 ^oC with the help of a quartz lamp fitted inside the vacuum chamber. Once the temperature in the chamber stabilized around 190 ^oC, the substrates were heated for duration of 18 minutes. The heat source was then switched off and the chamber was allowed to cool down to 45^oC. The chamber was finally vented to remove the samples. The resulting thickness of Cu_xS was about 0.7 microns, a thickness sufficient enough to absorb the incident radiation.

3.9.5 Rinsing to remove residual chlorides

Prior to rinsing, the photovoltaic cells were measured for probe voltages with a multimeter in order to get a rough estimate of the open circuit voltage. Following the post heat treatment, the photovoltaic cells were rinsed in order to remove the residual chlorides and other reaction products. The photovoltaic cells were first immersed in a beaker containing de-ionized water for 15 seconds, then rinsed in running de-ionized water to wash away the residual $CdCl_2$ and other byproducts of the reaction. After the rinse, the samples were dried in flowing nitrogen and again measured for probe voltage.

The second probe voltage measurement would yield a higher open circuit voltage because the byproducts of the reaction had been removed.

3.9.6 Formation of Electrodes

The devices were fabricated on an ITO-coated glass substrate since it makes a good ohmic contact with CdS, and acts as a transparent bottom contact for the solar. The top metallic electrode for Cu_2S was vacuum evaporated. A combination of chromium and lead or gold can be used to make an ohmic contact with Cu_2S. The combination of chromium/lead was preferred over gold because of the high cost of gold. A 100 Å layer of copper was vacuum evaporated on top of Cu_2S layer to correct the stoichiometry of Cu_xS and also to make a good ohmic contact to it. An aluminum mask with very small circles of area 0.07 cm^2 was used for this purpose. The evaporation of copper was done at a slower rate in order to prevent the copper ions from hitting the Cu_2S with a high velocity and thereby diffusing into the CdS layer. A 50 nm chromium layer was deposited on top of the copper contact. Lead contacts, one micron thick were deposited on top of the chromium contacts in order to improve the currents in the solar cells. Another way of making contact to Cu_2S is by applying silver paste with a brush directly on top of it. Commercial silver paste bought from Structure Probe, Inc., West Chester, PA, was used for the purpose. Once applied, the silver paste dried to form an adherent, metallic and electrically conductive coating.

3.10 Fabrication of nano-structured CdS/Cu_2S Devices in a porous alumina template

The nano-structured CdS/Cu_2S junctions were made inside a nano-porous alumina template. An all evaporation process was employed in the fabrication of these devices. Well ordered porous alumina templates with a pore diameter of 30 nm and a pore depth of 4 microns were used for this purpose.

3.10.1 Deposition of CdS inside nano pores

The nano porous alumina templates were mounted on a cleaned glass slide with aluminum foil stirps tightly securing them in place. The slide was then loaded into the vacuum chamber for thermal evaporation of CdS. The samples were loaded close to the evaporation source, as it was believed that the shorter distance could force the CdS particles through the nano pores. The pressure inside the chamber was maintained at 6e-06 Torr. CdS of thickness 3.5 microns was evaporated onto the nano porous template. The chamber was allowed to cool down and the samples were removed.

3.10.2 Annealing of CdS on nano porous alumina template

CdS deposited by thermal evaporation was amorphous in nature and hence needed to be annealed in order to allow for crystal regrowth. The regrown crystals would be able to support the diffusion of copper ions from CuCl into CdS to form a layer cuprous sulfide. The nano porous alumina templates, partially filled with CdS, were mounted on a cleaned glass substrate with aluminum foil strips tightly securing them in place. The glass substrate was then placed in zone 2 of the furnace as shown in Fig 3.8, and the samples were annealed at 450^{o}C in a nitrogen atmosphere for 90 minutes. Finally the furnace was allowed to cool down and the samples were removed.

3.10.3 Sputtering of ITO for back contact to CdS

Gas plasma may be formed whenever the gas is exposed to an electric field. If the electric field is sufficiently strong enough, majority of the gas atoms will surrender an electron or two and become ionized. The resultant ionized gas and the liberated energetic electrons would comprise the gas plasma or plasma. The ionized gas atoms gain kinetic energy when they are accelerated through a high electric field. When accelerated, they will bombard a surface with sufficient force to dislodge an atom from a target material. The term sputtering refers to the process of dislodging atoms from a target material to coat a thin layer onto the surface of a material of interest.

On the nano-structured solar cells, the ITO layer should contact the CdS layer at the bottom of the nano porous template. The partially filled porous alumina templates were turned upside down and mounted on a cleaned glass substrate with aluminum foil strips tightly securing them in place. The glass substrate was placed inside the vacuum chamber and allowed to pump down. Once a low pressure of the order of 2e-06 Torr was reached, a flow of argon was induced in the chamber. The power source was switched on in order to create plasma. Once the plasma in the chamber stabilized, the flow of argon was reduced to decrease the pressure inside the chamber. The shutter was then opened to start the deposition on the porous alumina template. A 280 nm layer of ITO was deposited to contact CdS. The shutter was then closed and the plasma was switched off by cutting the power supply. The chamber was then vented to remove the sample.

3.10.4 Deposition of CuCl on nano porous alumina template

CuCl was deposited onto the nano porous alumina templates by thermal evaporation. Prior to thermal evaporation, CuCl was bleached in a dilute hydrochloric

acid solution, followed by an acetone rinse. The partially filled nano porous alumina templates were mounted on a cleaned glass substrate with aluminum foil strips tightly securing them in place. This was then loaded into the vacuum chamber for thermal evaporation of CuCl. The samples were loaded close to the evaporation source, as it was believed that the shorter distance could force the CuCl particles through the nano pores. The pressure inside the chamber was maintained at 6e-06 Torr. CuCl of thickness 3 microns was evaporated onto the nano porous alumina templates. The chamber was allowed to cool down and the samples were removed.

3.10.5 Post heat treatment to convert CuCl into Cu_2S

The samples were then annealed in vacuum, as described in section 3.9.4, in order to convert the CuCl into Cu_2S.

3.10.6 Rinsing to remove residual chlorides

The solar cells were rinsed in de-ionized water, as described in section 3.9.5, to remove the residual chlorides. The solar cells were measured for probe voltages prior to and after the rinse to obtain a rough estimate of the open circuit voltage.

3.10.7 Formation of electrodes

Chromium and lead or gold is known to make a good ohmic contact to Cu_2S. Prior to the fabrication of contacts, a 100 Å thick layer of copper was thermally evaporated on top of Cu_2S. This was expected to correct the stoichiometry of cuprous sulfide as it could be deficient in copper. A 50 nm thick layer of chromium and one micron layer of lead were successively evaporated on top of the thin copper layer to establish the top contacts for the solar cell.

3.11 Measurement of Device J-V Characteristic

The J-V measurement setup used for the measurement of the devices is shown below in Figure 3.9.

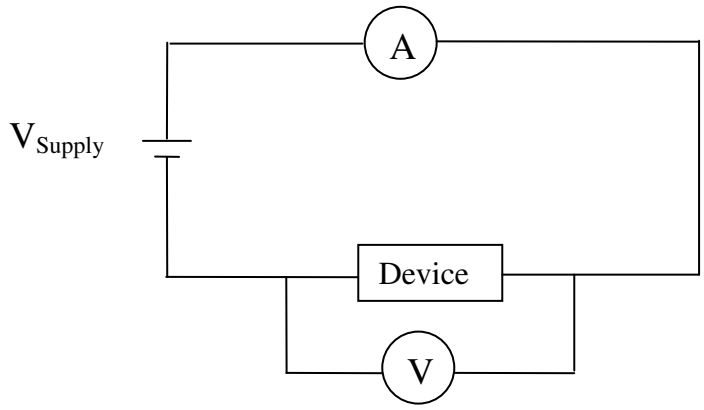

Figure 3.9 I-V measurement setup

V_{Supply} - Bipolar supply voltage

A – Ammeter to measure the current through the device

V – Voltmeter to measure the voltage across the device

Device – Device under test

The entire J-V setup shown in Fig 3.9 was controlled with a computer interface. Two Keithley multimeters were used as the voltmeter and the ammeter. The bipolar supply voltage, the voltmeter and ammeter were controlled by the computer interface running LabVIEW software. The DC voltage over which the device was to be swept, the time interval between each successive I and V measurements, and the destination folder in which the collected data is to be stored, are provided through the LabVIEW software interface. The electrical characteristics of the device under light were studied with a solar simulator. The solar simulator is shown in Figure 3.10.

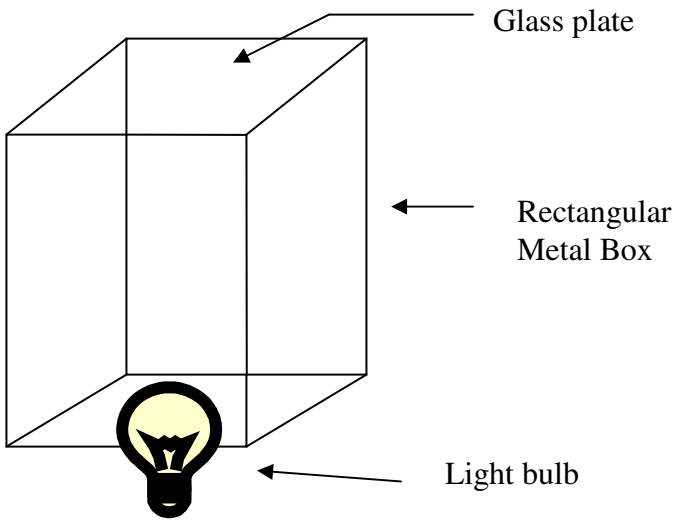

Figure 3.10 Solar simulator

The solar simulator consists of a rectangular box, open at the top and bottom. The bottom of the rectangular box is fitted with a light bulb to flash light onto the devices to be measured. The top of the box is covered with a flat square piece of glass on which to mount the devices to be measured and also to allow light coming from the bulb to be incident on the devices. The illumination from the bulb is a standard one sun. The corresponding incident power is 100 $mW.cm^{-2}$.

The J-V curve as generated by the Labview software consists of individual data points showing current vs. voltage across the device. Gaps between data points can be seen. This is shown in Figure 3.11 measured for a standard silicon solar cell under light and dark conditions.

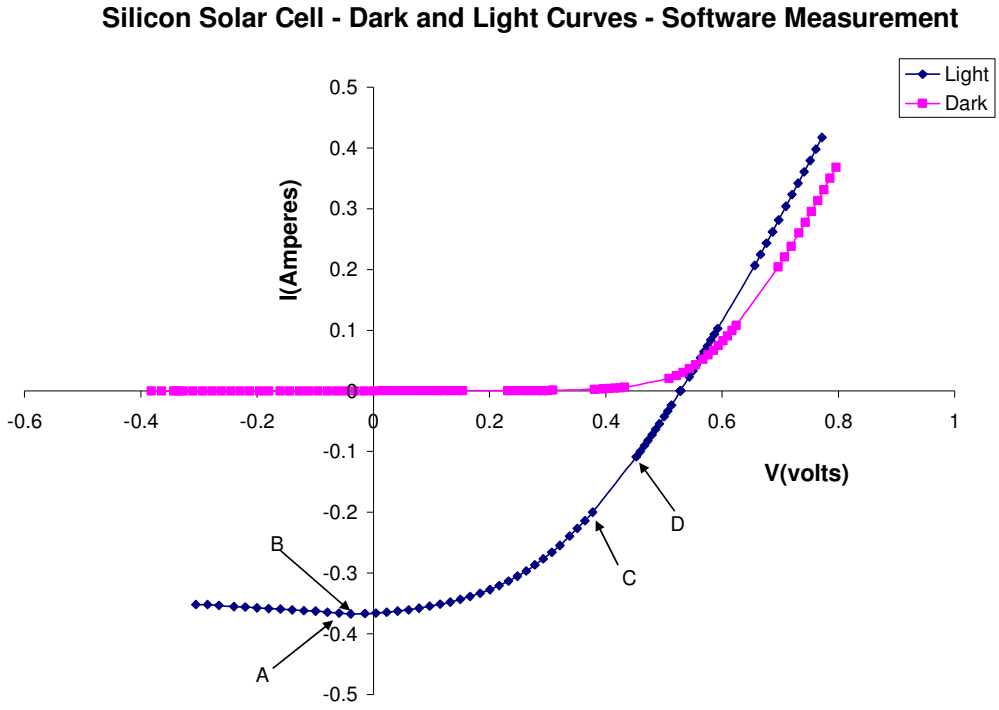

Figure 3.11 Silicon solar cell – Dark and Light – Software Measurement

To verify the validity of the software measurements, the silicon solar cell was measured manually and compared with the software measurements. The manual measurements made for the silicon solar cell is shown below in Figure 3.12. The manual measurements also had gaps between data points in them. It is possible that the presence of an external resistance in the circuit (caused by the resistance of the ammeter, voltmeter or the connecting wires) could be the reason for the missing points.

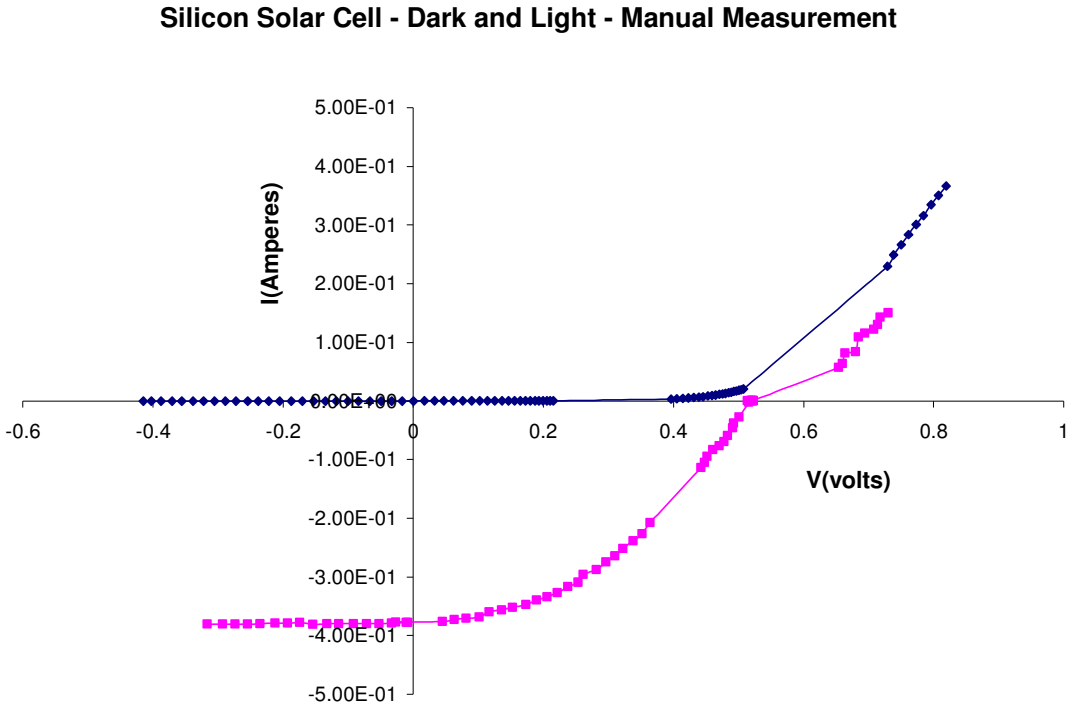

Figure 3.12 Silicon solar cell – Dark and Light – Manual Measurement

To confirm this, two consecutive points A and B were picked on the light curve (Figure 3.11) measured by the software, and the change in voltage and current were noted to calculate the value of the external resistance. The external resistance was calculated using the formula, $\Delta V_d = \Delta V_a - \Delta I.R_{ext}$, where ΔV_d is the change in voltage across the device, ΔV_a is the change in applied voltage and ΔI is the change in current for two consecutive points. For the points A and B the following values are found. ΔV_a = 20 mV, ΔV_d = 20.2 mV and ΔI = 0.0004 A. The value of R_{ext} is calculated to be 0.5 Ω. Points C and D are considered next. The corresponding values were ΔV_a = 20 mV, ΔV_d = 76 mV and ΔI = 92 mA. For points C and D, ΔV_d - ΔV_a is found to be 56 mV, and ΔIR_{ext} (92 mA * 0.5Ω) is found to be 46 mV. Thus there is a close agreement between the two values. If the external resistance had a very small value such as 0.01Ω, the difference between the

applied voltage and the voltage across the device for two consecutive points would only be 0.9 mV. Hence for a lower value of external resistance, many more points would be measured between C and D.

Chapter 4. Material Characterization

4.1 Characterization of CdS by SEM

CdS has been used in the fabrication of both CIS/CdS and Cu_2S/CdS solar cells. Ultrasound assisted nano CdS has been used in the fabrication of CIS solar cells and thermally evaporated CdS has been used in Cu_2S solar cells. The Figure 4.1 below shows the SEM image of nano crystalline CdS at a high magnification. The deposited film was uniform and had a particle size of 20 nm. The SEM image at high magnification (Figure 4.2) shows the uniformity of the film.

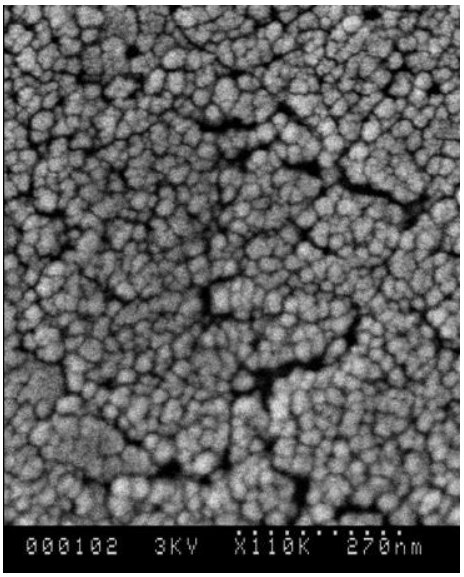

Figure 4.1 SEM image of nano crystalline CdS at high magnification

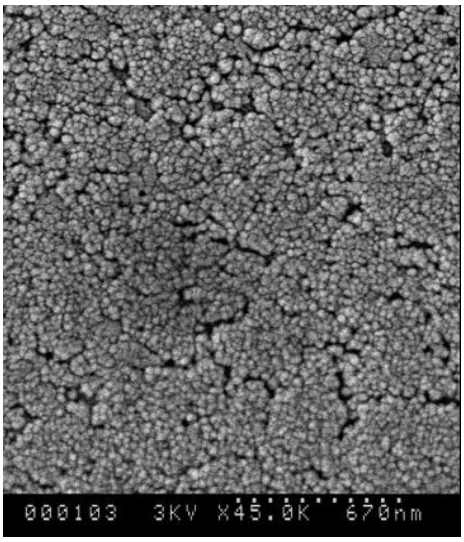

Figure 4.2 SEM image of nano crystalline CdS at low magnification

Figure 4.3 below shows the SEM image of thermally evaporated CdS. The film was uniform and the average particle size was about 80 nm.

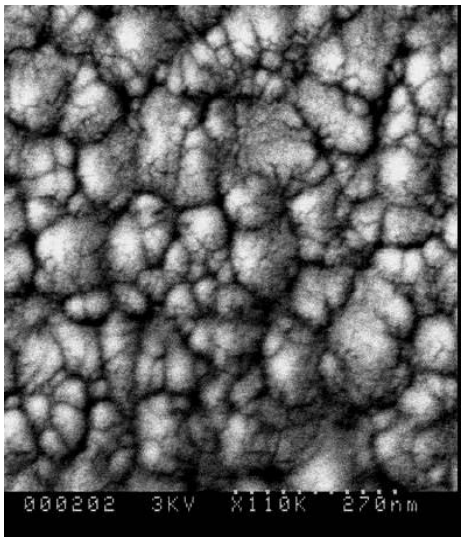

Figure 4.3 SEM image of thermally evaporated CdS at high magnification

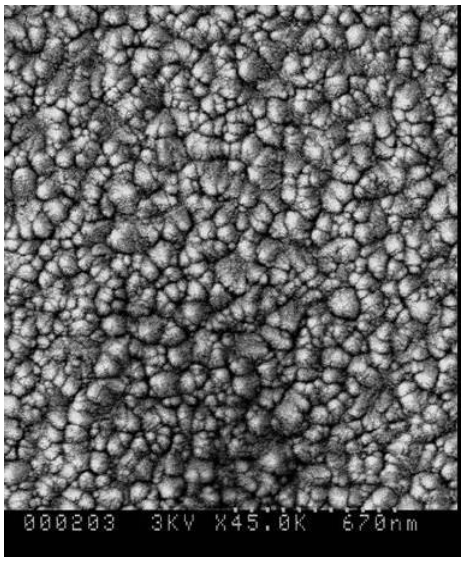

Figure 4.4 SEM image of thermally evaporated CdS at high magnification

4.2 Characterization of CdS by XRD

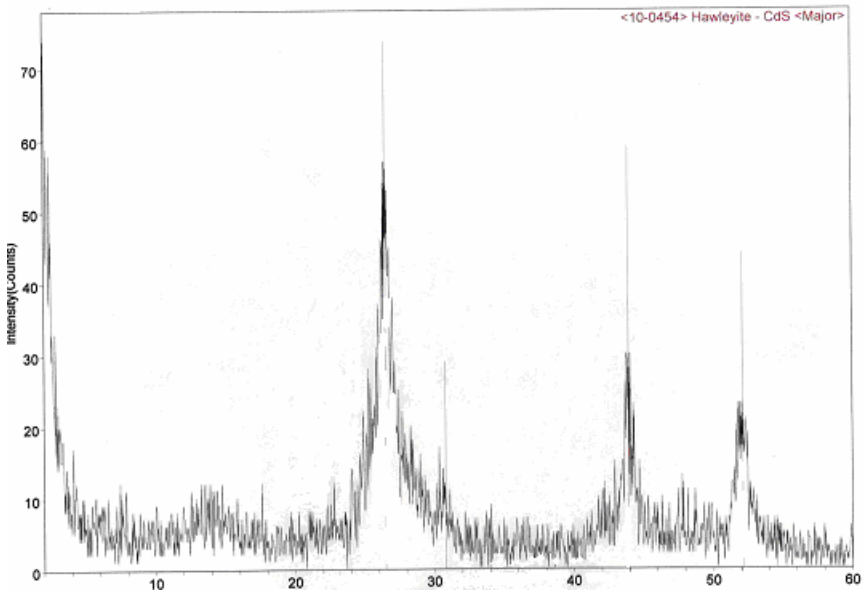

Figure 4.5 XRD of solution grown CdS powder

The X-ray diffraction pattern of the CdS powder prepared by solution growth method shows peaks at 2θ positions of 27°, 44° and 52° corresponding to the planes

(111), (220) and (311) respectively. The XRD pattern indicates a cubic phase for CdS as per the 10-0454 Hawleyite JCPDS.

4.3 Characterization of CIS by SEM

Figure 4.6 shows the SEM image of a CIS film deposited at -0.75 V vs. a saturated calomel electrode (SCE). Figure 4.7 shows the SEM image of the same sample at an even higher magnification. The CIS particles have an average size of about 20 nm to 25 nm. Figure 4.8 and 4.9 show the SEM image of a CIS sample deposited at -0.85 V vs. SCE at two different magnifications. It can be seen that the CIS particles have an average size of about 25 nm to 30 nm. The size of the CIS particle increase slightly with an increase in the applied voltage.

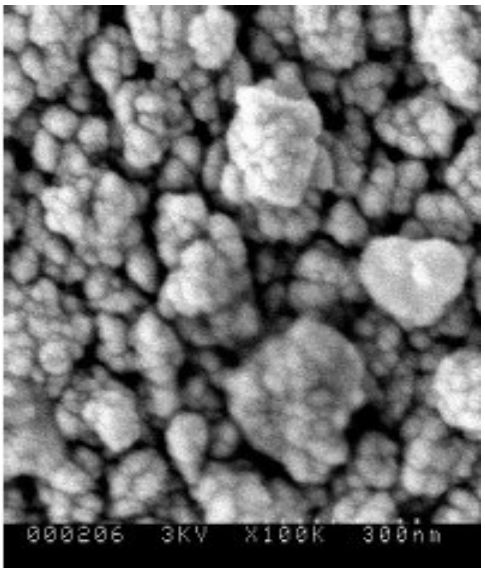

Figure 4.6 SEM image of CIS deposited at -0.75 V vs. SCE at lower magnification

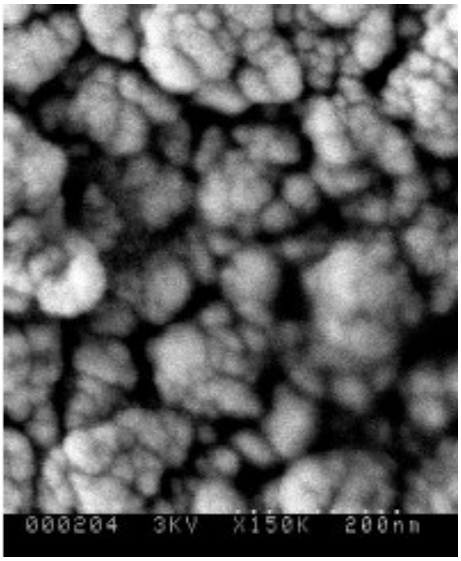

Figure 4.7 SEM image of CIS deposited at -0.75 V vs. SCE at higher magnification

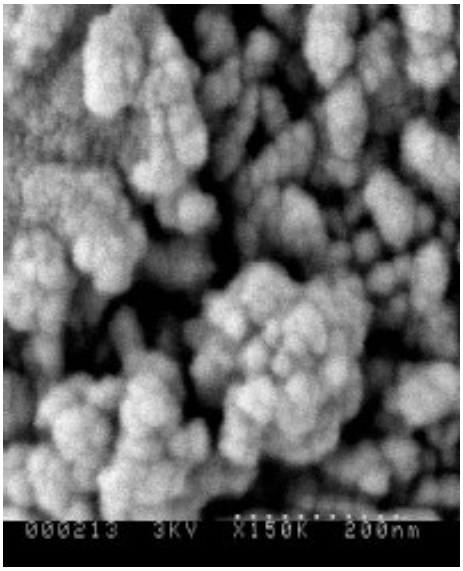

Figure 4.8 SEM image of CIS deposited at -0.85 V vs. SCE at lower magnification

Figure 4.10 shows the SEM image of a CIS film deposited at -0.75 V vs. SCE and annealed at 350^{o}C for one hour. The annealing process increases the particle sizes to about 60 nm. Also the crystallinity of the film improves with the annealing step.

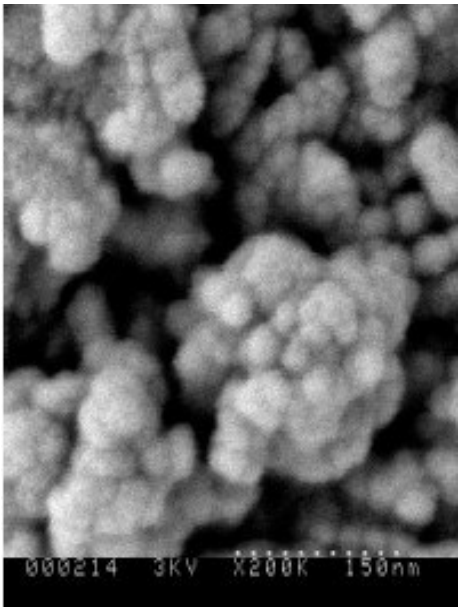

Figure 4.9 SEM image of CIS deposited at -0.85 V vs. SCE at higher magnification

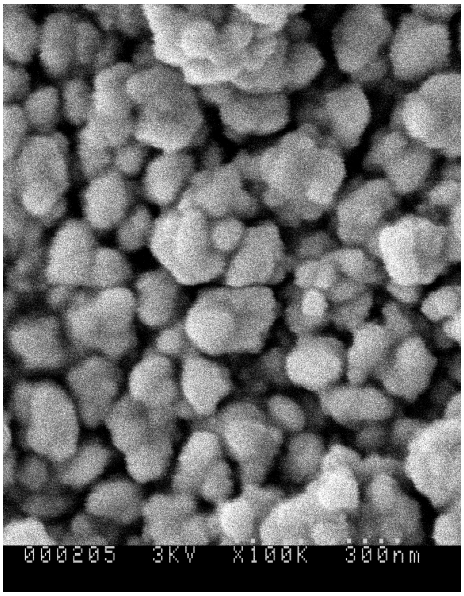

Figure 4.10 SEM image of CIS film annealed at 350^{o}C for one hour

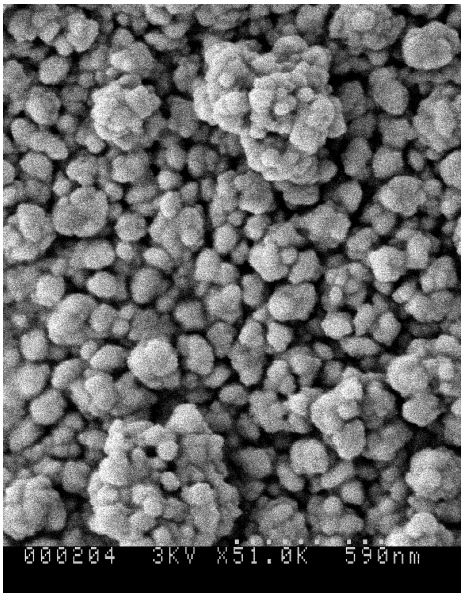

Figure 4.11 SEM image of CIS film annealed at 350^{o} C for one hour at a lower magnification

4.4 Characterization of CIS by XRD

Copper Indium Diselenide films made by electrodeposition, without the subsequent annealing step are called the as-deposited films and the ones that go through the annealing process are called annealed or crystalline films. X-ray Diffraction studies were conducted on both the as-deposited and annealed films. The CIS films on ITO coated glass were deposited at different potentials ranging from -0.6 V vs. SCE to -0.9V vs. SCE. Shown below are the XRD of CIS films (as-deposited and annealed) deposited at -0.6 V vs. SCE. Figure 4.12 shows the XRD of the as-deposited film and Figure 4.13 shows the XRD of the film annealed at 350^{o}C.

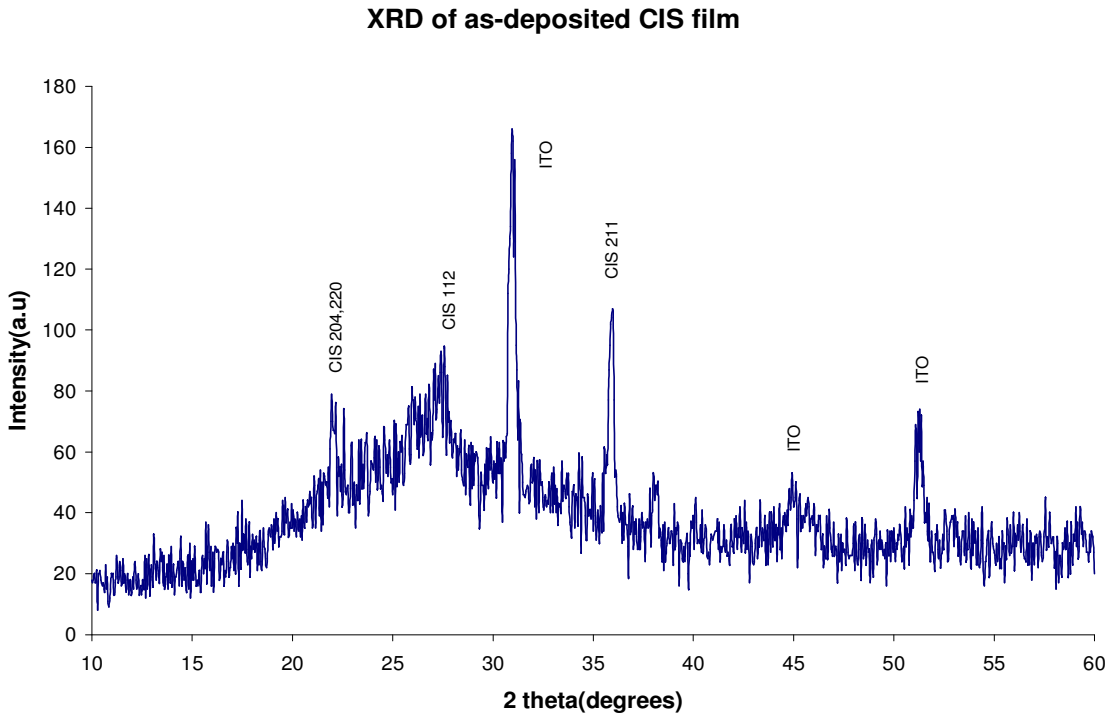

Figure 4.12 XRD of as-deposited CIS film

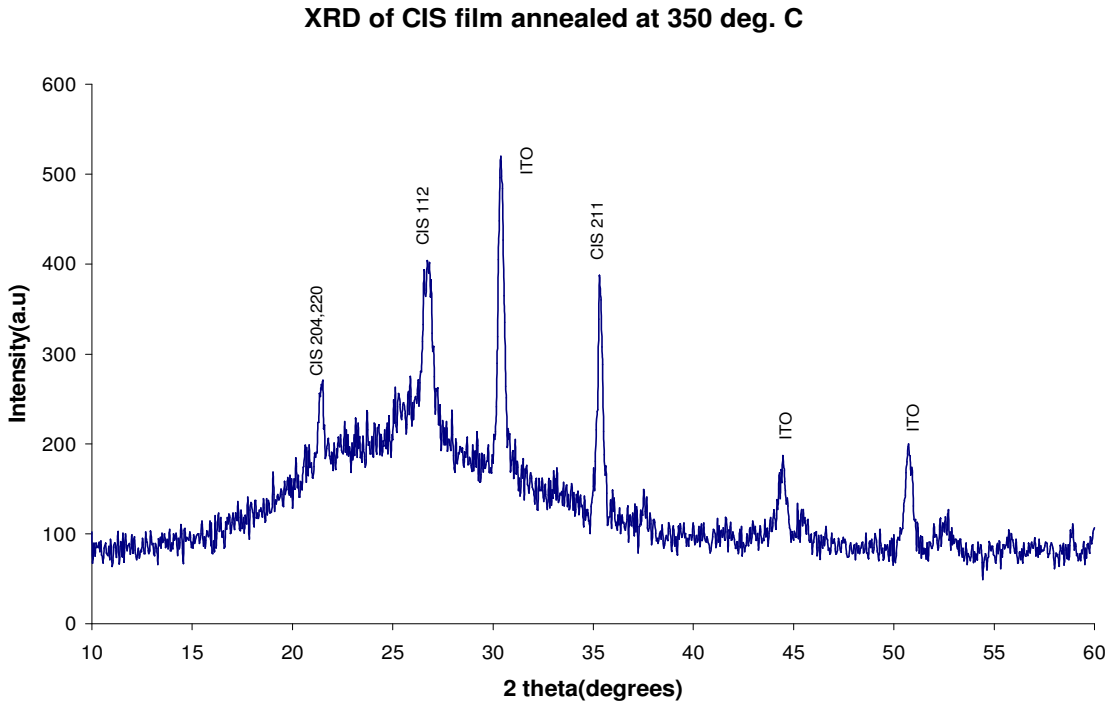

Figure 4.13 XRD of CIS film annealed at 350^{o}C

The as-deposited CIS films exhibited very weak and broad reflections due to the small crystallites found in them. The CIS films that underwent a heat treatment at 350^{o}C for one hour on the other hand exhibited strong and sharp reflections. CIS is clearly identified by the characteristic (112), (204, 220) and (211) reflections of the tetragonal structure. The presence of these peaks confirms the chalcopyrite structure of the CIS films. The other peaks in the XRD were found to correspond to tin oxide. In other words annealing improves the crystalline nature of the as-deposited films.

4.5 Characterization of Cu_2S by SEM

Figures 4.14 and 4.15 show the SEM image of copper sulfide at lower and higher magnifications respectively.

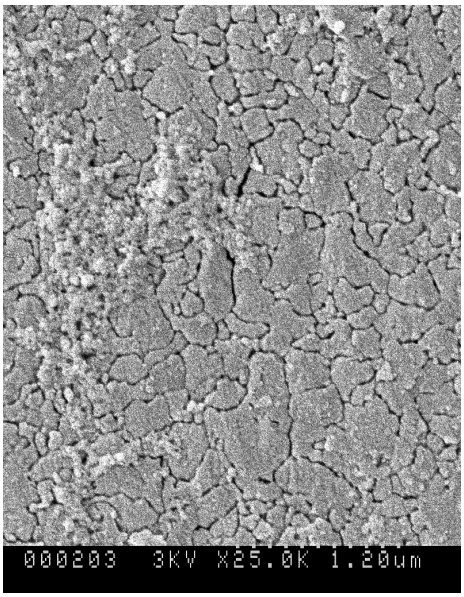

Figure 4.14 SEM image of Cu_2S at lower magnification

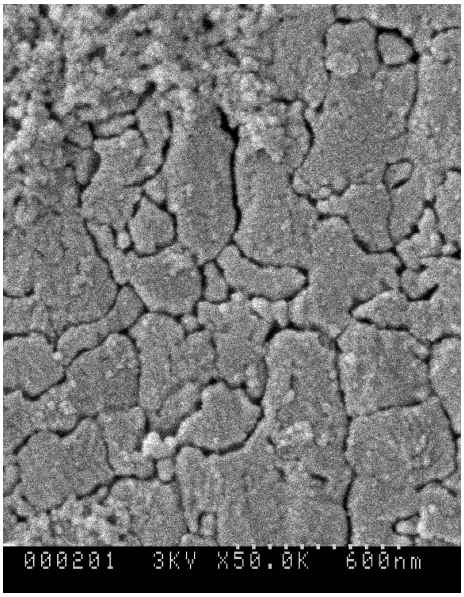

Figure 4.15 SEM image of Cu_2S at high magnification

From the SEM images of Cu_2S, it can be observed that there are micro-cracks in the film. The Cu_2S layer is formed by the reaction of the copper ions penetrating and reacting with the CdS layer. So the morphology of the Cu_2S layer is dictated by that of the CdS layer. After going through an annealing process at 450^{o}C for one hour, the CdS layer develops micro-cracks during recrystallization. Hence the Cu_2S layer would also have micro-cracks in it as shown in the SEM images above.

4.6 SEM images of porous alumina

Figure 4.16 shows the top view of a porous alumina film made from a two-step anodization process. A 0.3 M oxalic acid was used as the electrolyte. The SEM images show ordered pores of diameter 30 nm.

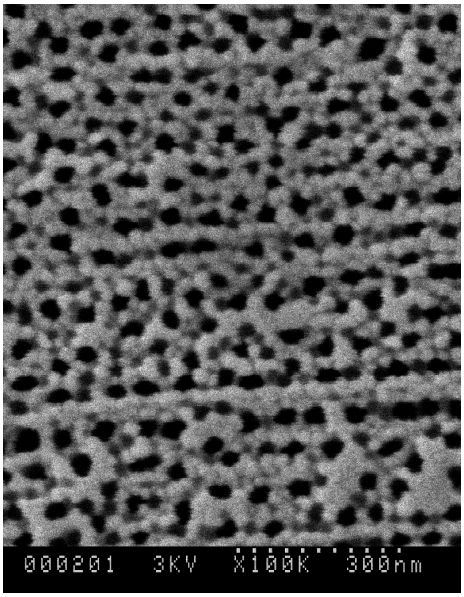

Figure 4.16 SEM image of top view of a porous alumina film – high magnification

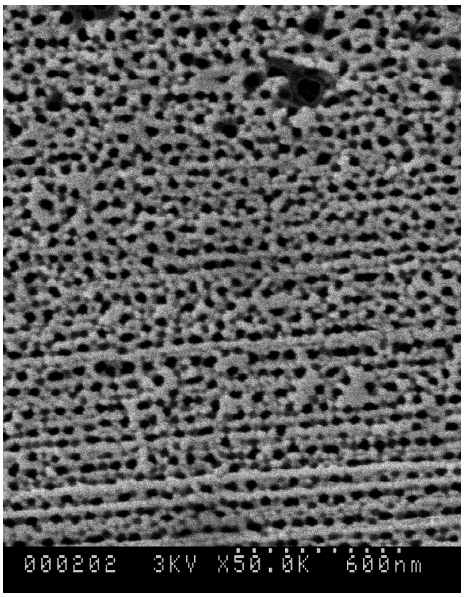

Figure 4.17 SEM image of top view of porous alumina film – low magnification

Figures 4.18 and 4.19 show the back side of the porous alumina film at lower and higher magnifications respectively. Figures 4.20 and 4.21 show the cross section of the porous alumina film at two different magnifications. It can be seen that the pores run through and through to the bottom. The porous alumina foil is approximately 4 microns thick.

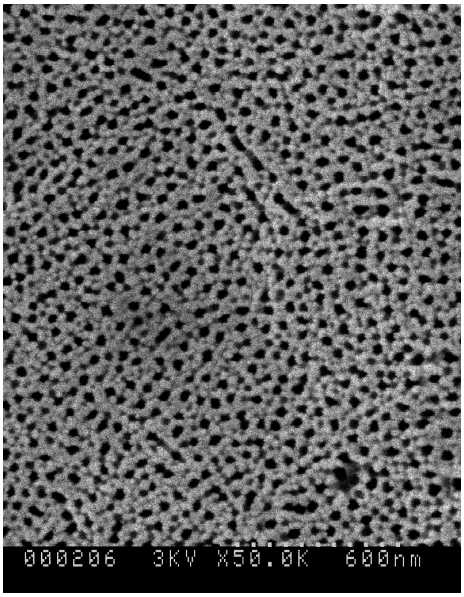

Figure 4.18 SEM image of back side of porous alumina – low magnification

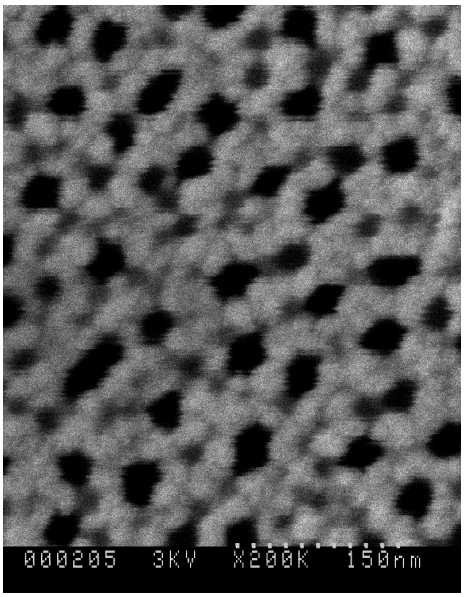

Figure 4.19 SEM image of back side of porous alumina – high magnification

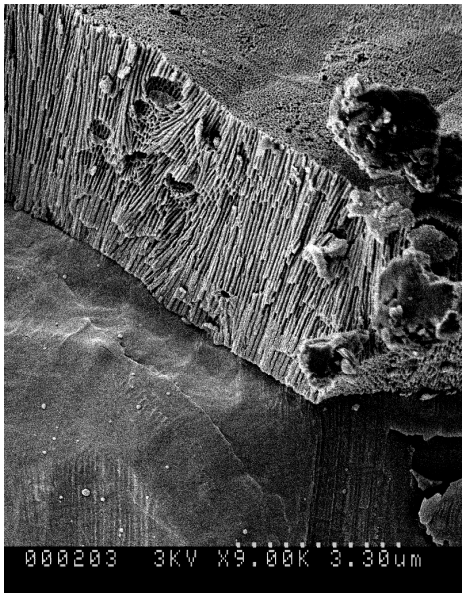

Figure 4.20 SEM of cross-section of porous alumina foil – low magnification

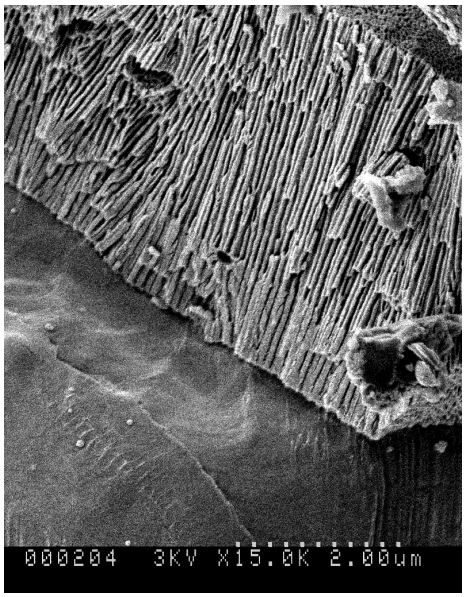

Figure 4.21 SEM of cross-section of porous alumina foil – high magnification

4.7 SEM images of porous alumina foil after deposition of CdS

Figures 4.22 and 4.23 show the SEM images of the top and bottom of the porous alumina foil after the deposition of CdS through it.

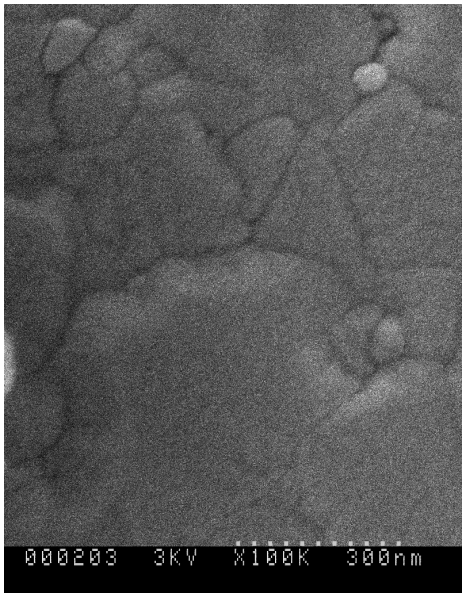

Figure 4.22 SEM image of top side of porous alumina film after CdS deposition

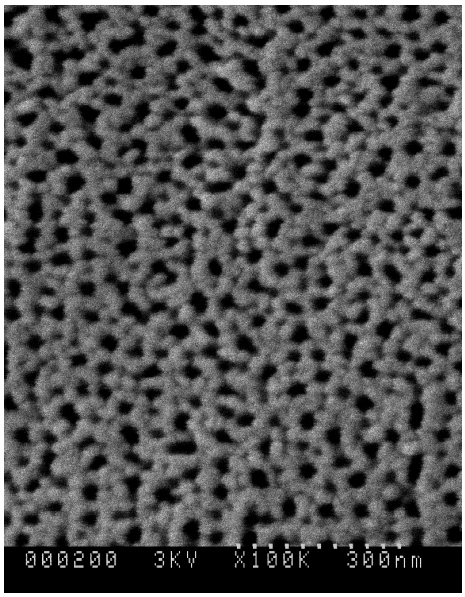

Figure 4.23 SEM image of back side of porous alumina film after CdS deposition

From these pictures it is clear that CdS is not going all the way through to the bottom of the pores. The CdS would get inside the pores and stop midway because of the high aspect ratio of the porous alumina film. Figure 4.24 below shows the back side of the porous alumina film after sputtering ITO through it. The thickness of the ITO film was about 560 nm.

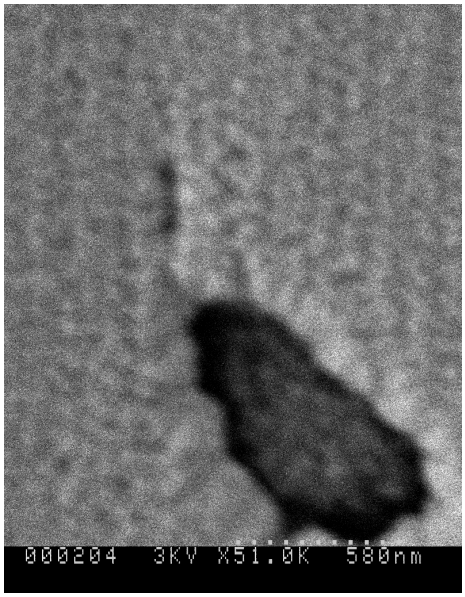

Figure 4.24 SEM image of back side of prous alumina foil after ITO sputtering

It can be seen from Figure 4.24 that ITO is going inside the pores and filling it.

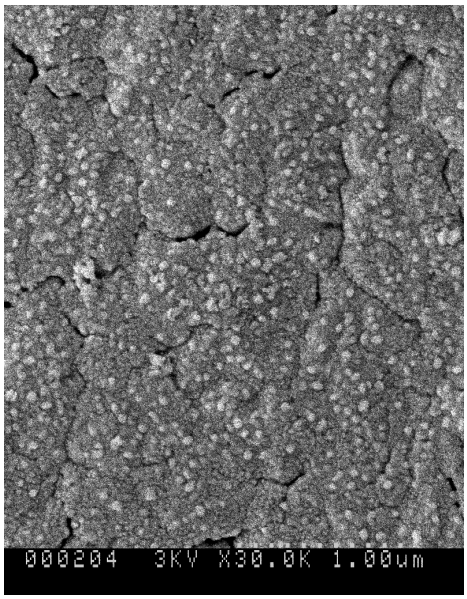

Figure 4.25 SEM image of Cu_2S on porous alumina template – low magnification

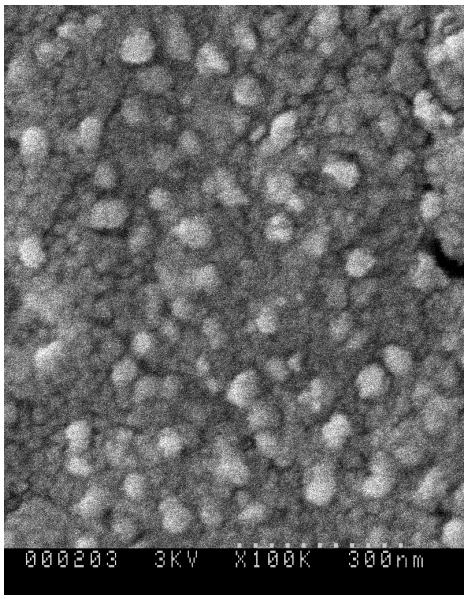

Figure 4.26 SEM image of Cu_2S on porous alumina template – high magnification

The sputtered ITO from the bottom and the 3.5 micron thick CdS evaporated from the top meet midway inside the porous template. CuCl of thickness 3 microns was evaporated on top of CdS. According to the reaction taking place between CdS and CuCl, three-fifths of the thickness of CuCl would be consumed in the formation of Cu_2S and rest would be converted into the reaction by-products. An identical thickness of CdS would be needed to support the growth of Cu_2S through it. Hence the ITO would fill the bottom half micron of the 4 micron thick pore and the 3.5 micron thick CdS would fill the pore and overflow. When 3 microns of CuCl is deposited on top of CdS and annealed in vacuum, 1.8 microns of Cu_2S would be formed. Thus 1.8 microns of CdS would be consumed in supporting the growth of Cu_2S through it. Hence the heterojunction would be formed inside the nano pore. From Figures 4.25 and 4.26 it can be seen that the Cu_2S particles are going through the pores. This represents a sharp contrast to the Cu_2S films formed on ITO-coated glass substrates (Figures 4.14 and 4.15).

Chapter 5. Results and Discussion for CIS/CdS Devices

5.1 J-V Characteristics

The J-V characteristic of the CIS/CdS heterojunction was obtained by applying a voltage across the junction and measuring the resulting current density. A positive voltage was applied to the gold dot and a negative voltage was applied to ITO. The J-V characteristics were measured for both the front-wall and back-wall heterostructures.

The n-type CdS and p-type CIS form a rectifying junction, whose behavior is similar to that of an abrupt p-n junction. The behavior of an abrupt p-n junction is governed by the ideal diode equation given below,

$$J = J_0[\exp(qV / nkT) - 1] \quad \text{.....(5.1)}$$

Where, J_0 – reverse saturation current density,

q – Charge of an electron = 1.6e-19 C,

V – Voltage applied to the abrupt p-n junction,

n – Diode ideality factor,

k – Boltzman constant = 1.38e-23 $J.K^{-1}$,

T – Absolute temperature in degree Kelvin.

From the ideal diode equation it can be deduced that,

* The drift and diffusion current components cancel each other when there is no applied bias (V = 0), resulting in no net current flow across the junction.

* When the applied voltage is positive (V > 0 i.e. forward bias), the barrier for majority carrier diffusion is lowered resulting in an exponential increase in current through the junction. The drift current remains unaltered.

* When the applied voltage is negative ($V < 0$ i.e. reverse bias), the barrier for majority carrier diffusion is increased resulting in a negligible diffusion current through the junction, while the drift current remains unchanged.

Most practical diodes have current transport mechanisms which deviate from that described by the ideal diode equation. These non-ideal currents arise as a result of generation and recombination of carriers in the depletion region, tunneling of carriers between states in the bandgap, and high-injection conditions which may arise even at a relatively small forward bias. The ideal diode equation has to be modified accordingly for these cases.

5.2 J-V Analysis

The J-V analysis of a curve involves the determination of diode parameters namely, diode ideality factor n, reverse saturation current density J_0 and the series resistance associated with the device. The sections below explain the estimation of these parameters from a given J-V curve.

5.2.1 Determination of Series Resistance, R_s

The J-V characteristics of a heterojunction diode become linear at high voltages and high currents due to the series resistance associated with it. The series resistance in the device arises due to the resistance offered by the quasi neutral region in the p and n type materials forming the heterojunction and the resistance of the ohmic contacts to the device. In such a case the voltage drop across the device is not just the drop across the p-n junction, but also includes the drop due to the series resistance, R_s. In order to get the value of the voltage drop across the diode junction, the drop due to the series resistance

has to be subtracted from the measured voltage drop. This makes sure that the J-V characteristic is corrected for series resistance and the current component only due to the diode behavior is extracted. Equation 5.1 modified for series resistance would be,

$$J = J_0\left[\exp\left(\frac{q(V - JR_s)}{nkT}\right) - 1\right] \quad \text{.....(5.2)}$$

where, R_s is the series resistance and the actual drop across the junction would be ($V - JR_s$). The series resistance can be mathematically determined from the J-V characteristic as explained below.

Differentiating equation 5.2 results in,

$$1 = J_o \frac{q}{nkT}\left(\frac{dV}{dJ} - R_s\right)\exp\left[\frac{q(V - JR_s)}{nkT}\right]$$

Now,
$$\frac{dV}{dJ} = \frac{nkT}{qJ_o}\exp\left[\frac{-q}{nkT}(V - JR_s)\right] + R_s \quad \text{.....(5.3)}$$

Ignoring the reverse saturation current density, J_0, equation 5.3 can be written as,

$$\frac{dV}{dJ} = \frac{nkT}{qJ} + R_s \quad \text{.....(5.4)}$$

When the junction is biased at a high voltage, the current through it would also be high. Thus the first term on the right side of equation 5.4 can be neglected. Hence at a higher bias voltage (and hence a higher J), the series resistance can be approximated as the slope of the J-V curve.

5.2.2 Determination of Ideality Factor and Reverse Saturation Current Density

This section explains the mathematical determination of ideality factor and the reverse saturation current density from the J-V characteristic. A plot of ln(J) Vs. V is needed in order to estimate n and J_0.

Obtaining the natural logarithm of equation 5.1,

$$\ln(J) = \ln(J_o) + \frac{qV}{nkT} \quad \text{.....(5.5)}$$

This represents the equation of a straight line, with q/nkT as its slope and (V, ln(J)) as the variables. Once the slope of the curve is known, the ideality factor can be easily computed, as the values of q, k and T are known already. The y-intercept of the line would give the value of $\ln(J_0)$, from which the reverse saturation current density can be calculated. The value of n gives a fair idea of the ideality of the device. For an ideal diode the value of n would be 1. In the case of practical diodes, the value of n deviates from 1 due to a various reasons such as, generation-recombination processes in the depletion region, high-injection conditions and tunneling of carriers between states in the bandgap.

5.2 J-V Characteristics of back-wall heterostructures

The back-wall heterostructure consists of glass/ITO/CdS/CIS/Au. In this structure a bulk-heterojunction and a heterojunction with nano CIS were fabricated to compare their performance. Figure 5.1 below shows the dark curve measured for device cis1_6 with nano CIS. The as-deposited CIS had particles of size 30 nm to 35 nm.

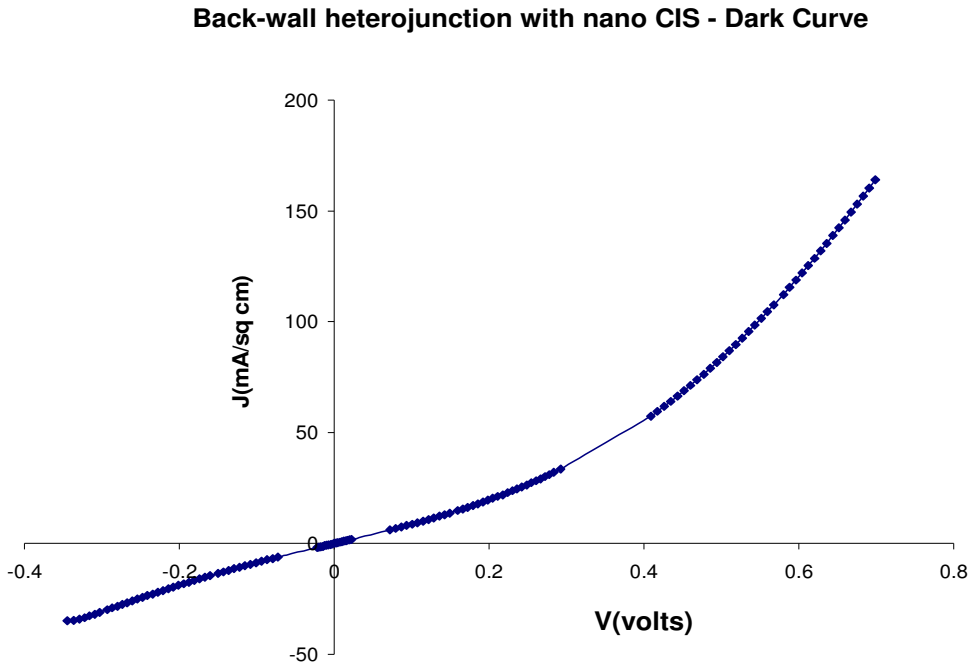

Figure 5.1 Back-wall heterojunction with nano CIS – Dark Curve

The J-V characteristic was obtained by sweeping the voltage from -0.4 V to 0.7 V and measuring the resulting current. The contacts for the cell were 0.07 cm^2 in area. The series resistance for the device was obtained by taking a slope of the curve at higher voltages as explained in section 5.2.1. The series resistance was found to be 2.14 $\Omega.cm^2$. The J-V characteristic was then corrected for series resistance by subtracting JR_s from V. A plot of V vs. J and ($V - JR_s$) vs. J is shown below in Figure 5.2. The diode ideality factor, n, and the reverse saturation current density J_0, were obtained by making a plot of ln(J) vs. V as explained in section 5.2.2. The ideality factor was found to be 8.9 and the diode had a reverse saturation current density of 9.03e-03 $A.cm^{-2}$. The ln(J) vs. V plot is shown in Figure 5.3.

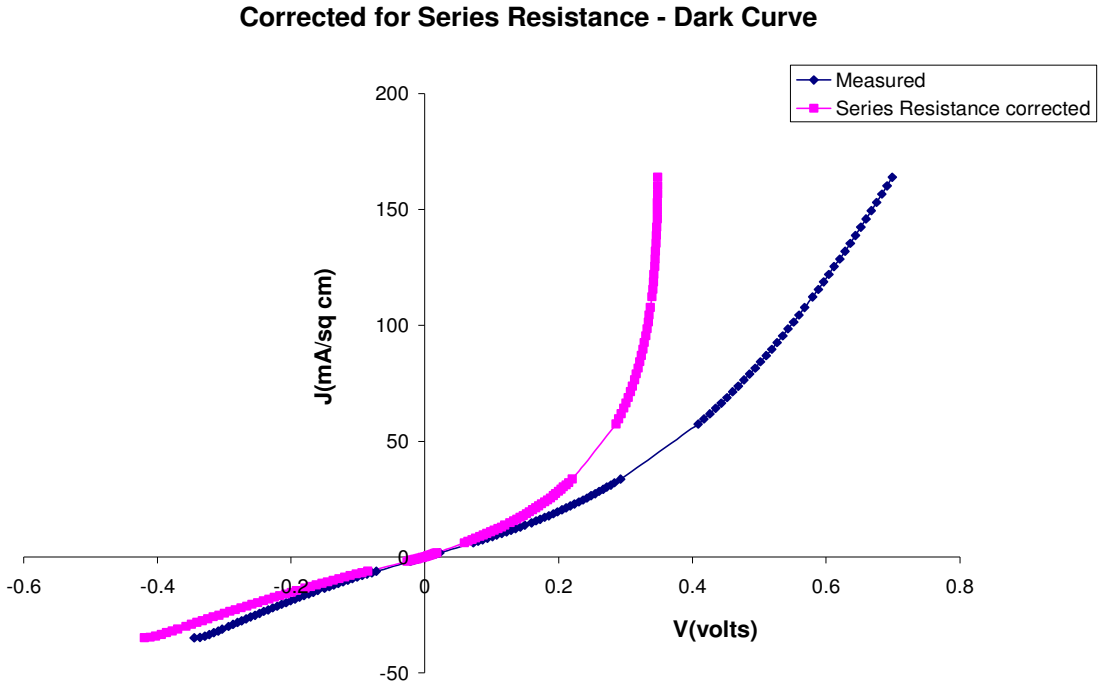

Figure 5.2 Corrected for series resistance - Dark Curve

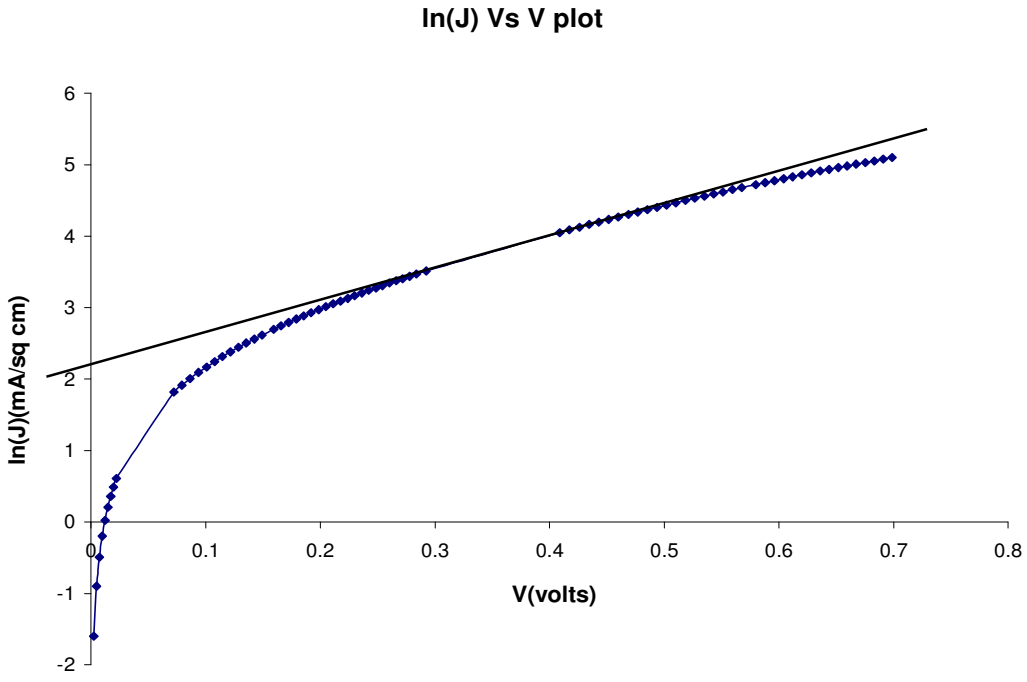

Figure 5.3 ln(J) vs. V plot for determining n and J_0

The dark curve, in Figure 5.1, shows a slope in the reverse bias. This is because of the availability of a shunting path between the top contact to the cell and the underlying CdS layer. The CIS layer has particle sizes in the range of 30 nm to 35 nm. These nano particles of CIS have a higher surface to volume ratio and hence it possible that gold could have seeped through the grain boundaries of CIS and contacted CdS. Also the existence of the physical shunting path is more reasonable considering the fact that there is a high reverse saturation current density of 9.03e-03 $A.cm^{-2}$.

Figure 5.4 shows the J-V characteristic for the device cis1_6 measured under light. The series resistance, ideality factor and reverse saturation density were computed as detailed in section 5.2.1 and 5.2.2. The light curve had a series resistance of 1.8 $\Omega.cm^2$, ideality factor of 12 and a reverse saturation current density of 36.6e-03 $A.cm^{-2}$.

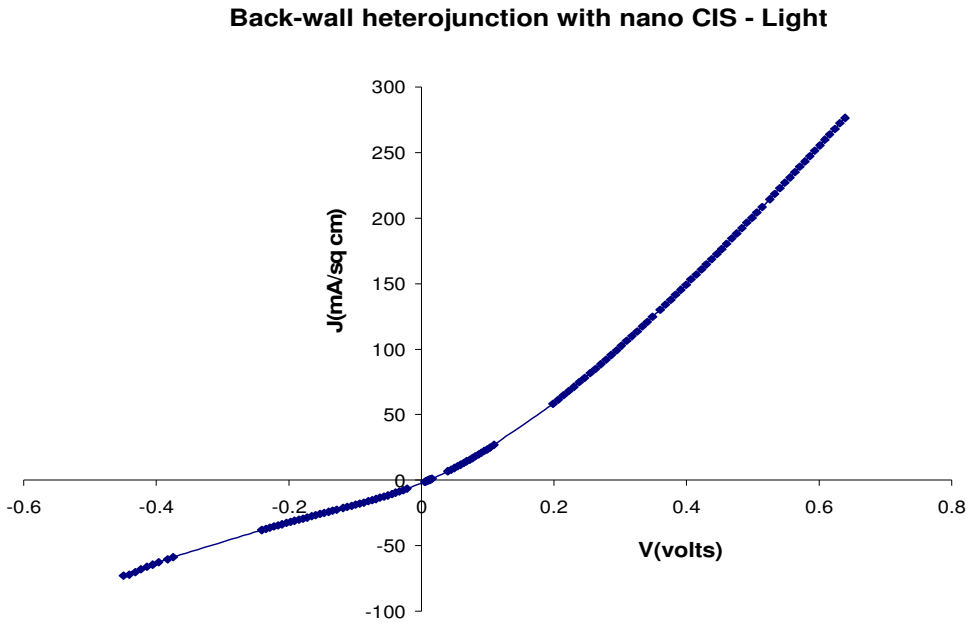

Figure 5.4 Back-wall heterojunction with nano CIS – Light Curve

Figure 5.5 and 5.6 show the series resistance corrected plot and ln(J) vs. V plot respectively.

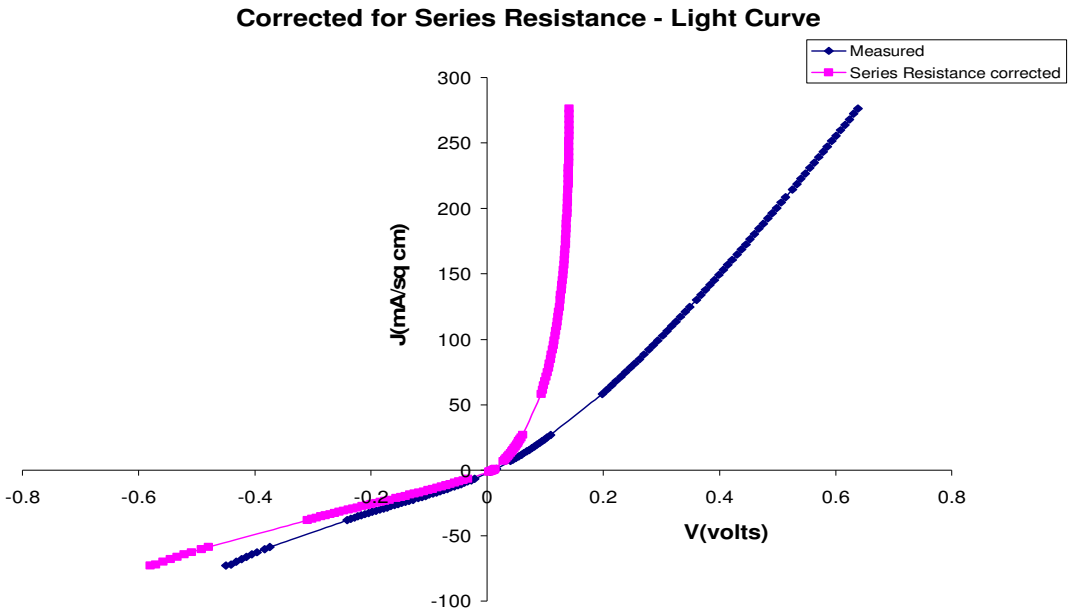

Figure 5.5 Corrected for series resistance – Light Curve

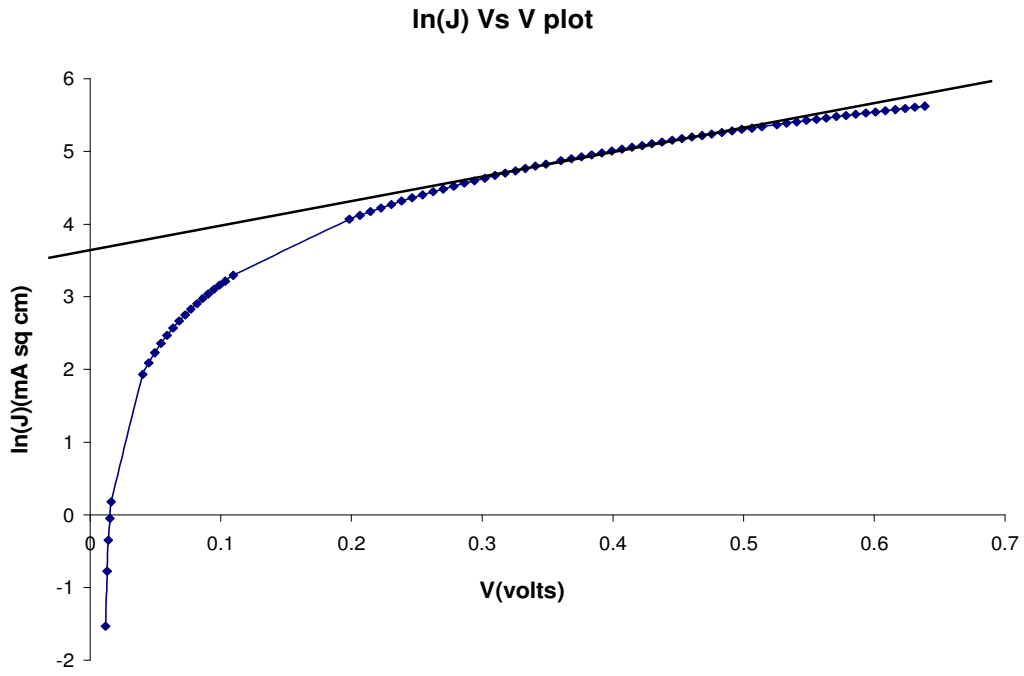

Figure 5.6 ln(J) vs. V plot for determination of n and J_0

Very high currents of the order of hundreds of $mA.cm^{-2}$ are observed for the heterojunctions with nano CIS. The diode ideality factors under dark and light are found to be 8.9 and 12 respectively. This indicates that the current transport in these devices cannot be explained with just the diffusion current dominated model. Several transport mechanisms may be operative at the interface. These would include diffusion current for the electrons and holes, recombination-generation currents in the depletion region, recombination through interface states at the junction, tunneling from band states to localized defect states in the bandgap and band-to-band tunneling. A proper junction between CIS and CdS will not be formed when the junction is not heat treated [19, 20]. A crucial reason for such high currents in these cells could be the presence of a shunting path between the gold top contact and CdS, provided by the nano grain boundaries of CIS. This is shown in Figure 5.7.

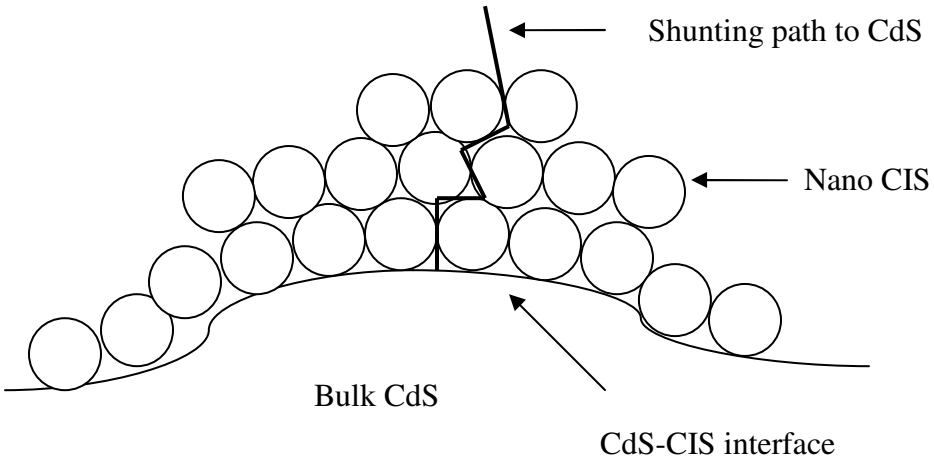

Figure 5.7 Shunting paths in back-wall devices with nano CIS

The nano particles have a high surface to volume ratio and so it is possible for the overlying gold contact to seep through the gaps between the nano grain boundaries and

contact the CdS, thereby creating a shunting path. This shunting path would give rise to higher currents in both the forward and reverse bias conditions of the diode. The light currents are higher than the dark currents indicating that the device is photoconductive. The cell however yields a very low open circuit voltage of 10 mV and a short circuit current density of 1.2 $mA.cm^{-2}$. The poor photovoltaic behavior is attributed to the as-deposited amorphous CIS which is not suitable for photovoltaic conversion. An annealing step adds crystallinty to the CIS layer and gives better opto-electronic properties to it [20].

Figure 5.8 below shows the J-V characteristic of a bulk-heterojunction of device, cis1ann_4, in dark.

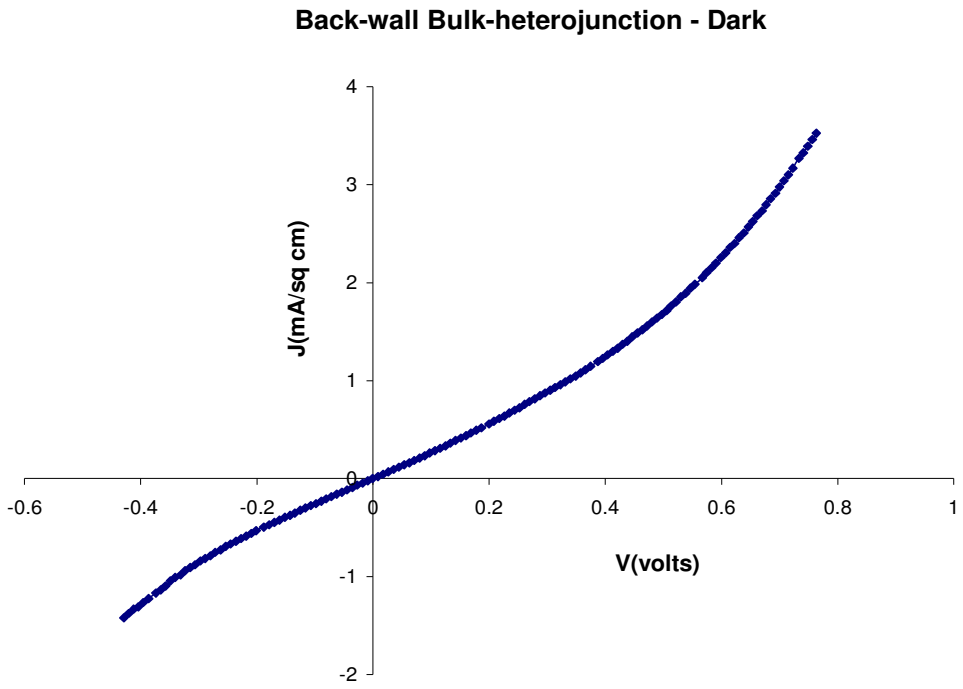

Figure 5.8 Back-wall bulk heterojunction – Dark Curve

The J-V characteristic was corrected for series resistance as detailed in section 5.2.1 and the corrected plot is shown below in Figure 5.9. The series resistance of the light curve

was found to be 111 $\Omega.cm^2$. The diode ideality factor and reverse saturation current density can be computed as detailed in section 5.2.2. The ln(J) vs. V plot for the device is shown in Figure 5.10. The diode ideality factor was found to be 10 and the reverse saturation current was 2.73e-04 $A.cm^{-2}$. The ohmic behavior in reverse bias could be due to the presence of shunting path between the CIS and CdS. The as deposited CdS layer could have pin holes in it which give rise to the shunting path. CIS is deposited in an acidic medium with a pH of 2.45. Dilute acids are known to etch off CdS. It is possible that the acidic medium could have partially etched off CdS thereby creating pin holes in the layer. These pin holes could short the CIS with the ITO layer resulting in increased currents through the junction.

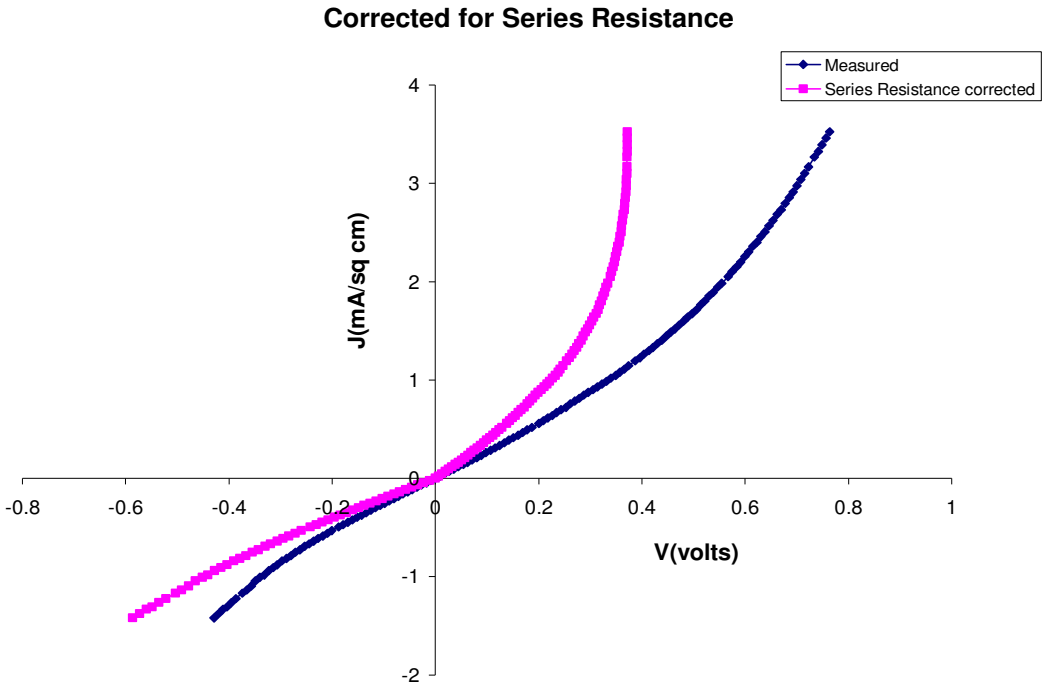

Figure 5.9 Corrected for series resistance – Dark Curve

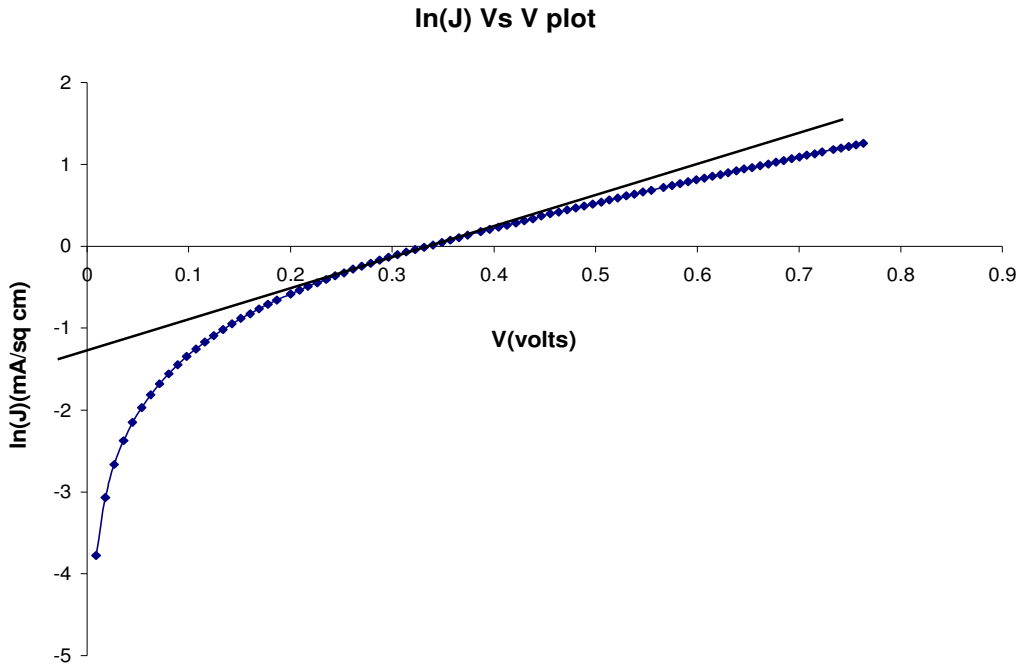

Figure 5.10 ln(J) vs. V plot for determination of n and J_0

The J-V characteristic of the back-wall bulk heterojunction in light is shown in Figure 5.11 below. The curve was analyzed for series resistance, ideality factor and reverse saturation current density as detailed in sections 5.2.1 and 5.2.2. The bulk device had an open circuit voltage of 98 mV and a short-circuit current density of 3 $mA.cm^{-2}$ under light. The series resistance corrected plot is shown Figure 5.12 and the ln(J) vs. V plot is shown in Figure 5.13. The series resistance was found to be 10.8 $\Omega.cm^2$. The diode ideality factor was 7.7 and the reverse saturation current density was 7.8e-04 $A.cm^{-2}$.

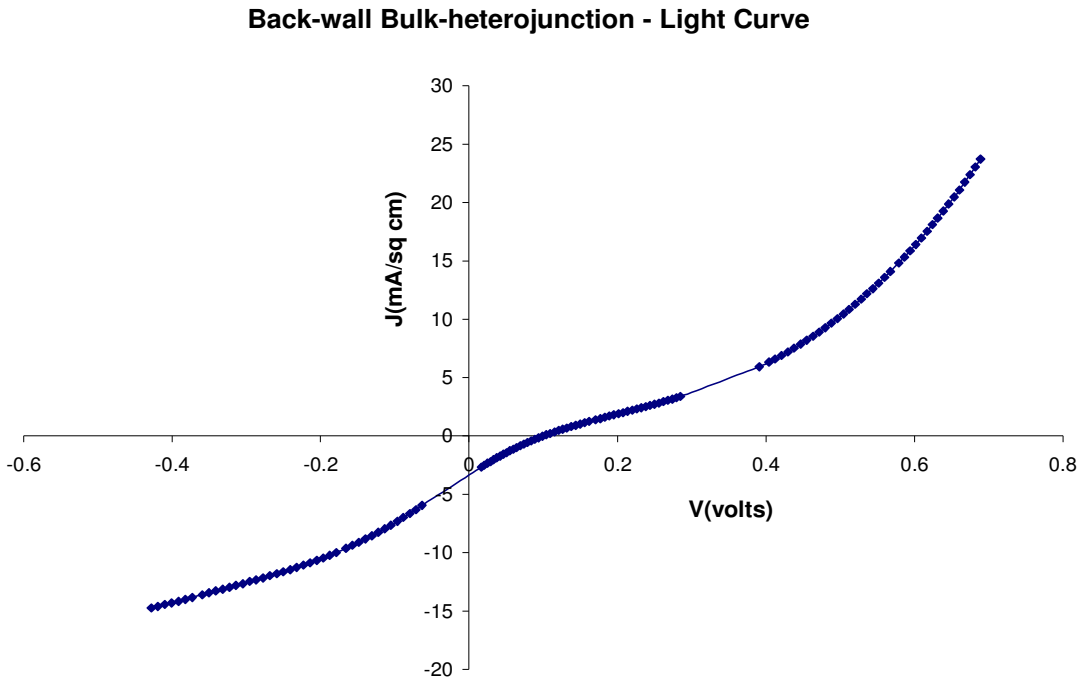

Figure 5.11 Back-wall bulk heterojunction – Light Curve

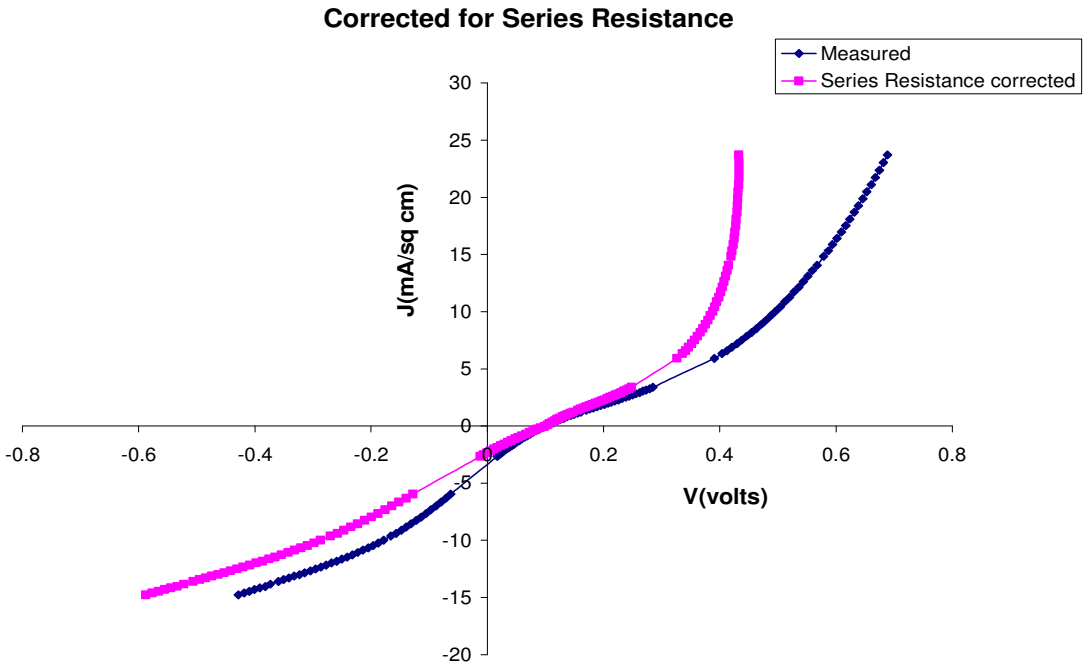

Figure 5.12 Corrected for series resistance – Light Curve

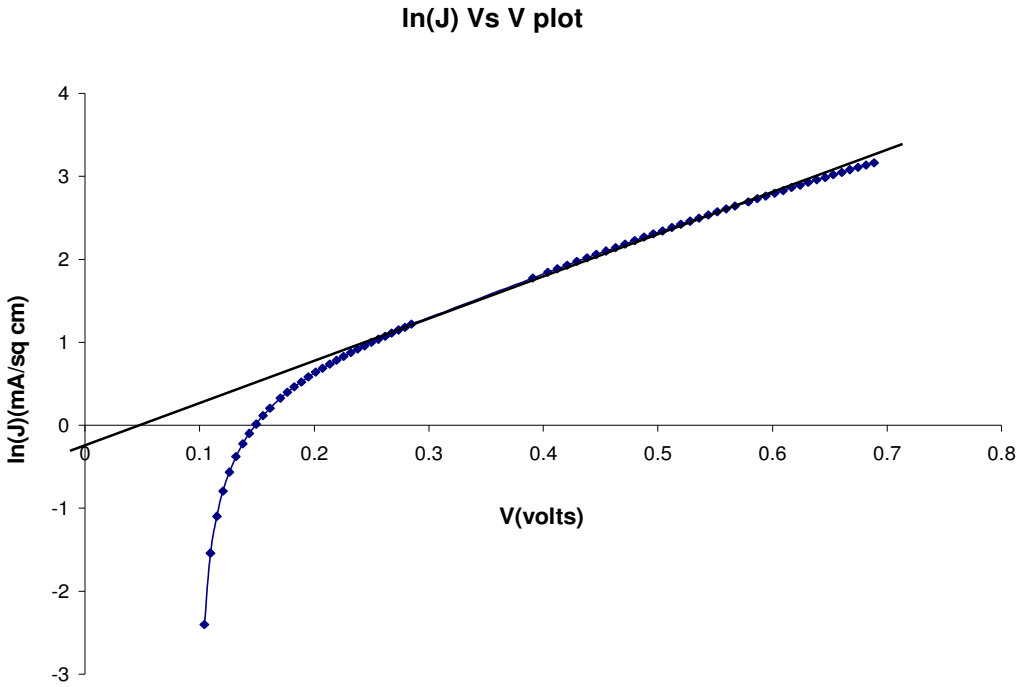

Figure 5.13 ln(J) vs. V plot for determination of n and J_0

The annealing treatment given to the CIS layer improves its crystallinity and gives it better opto-electronic properties. When the as-deposited CIS is annealed at 350^{o}C for one hour, the nano grain boundaries get cleaned up and become crystalline. The average particle size almost doubles from 30 nm to 60 nm. With the improved opto-electronic properties the bulk heterojunction yields an open circuit voltage of 98 mV and a J_{sc} of 3 mA.cm^{-2}. This can be seen from Figure 5.11.

5.3 J-V Characteristics of front-wall heterostructures

The front-wall heterostructure consists of glass/Mo/CIS/CdS/ITO. Heterostructures with both bulk and nano CdS were made to compare their performance. Shown in Figure 5.14 is the J-V characteristic of a bulk-heterojunction device,

mciscds13bulk_8. The series resistance was found to be 2870 $\Omega.cm^2$.

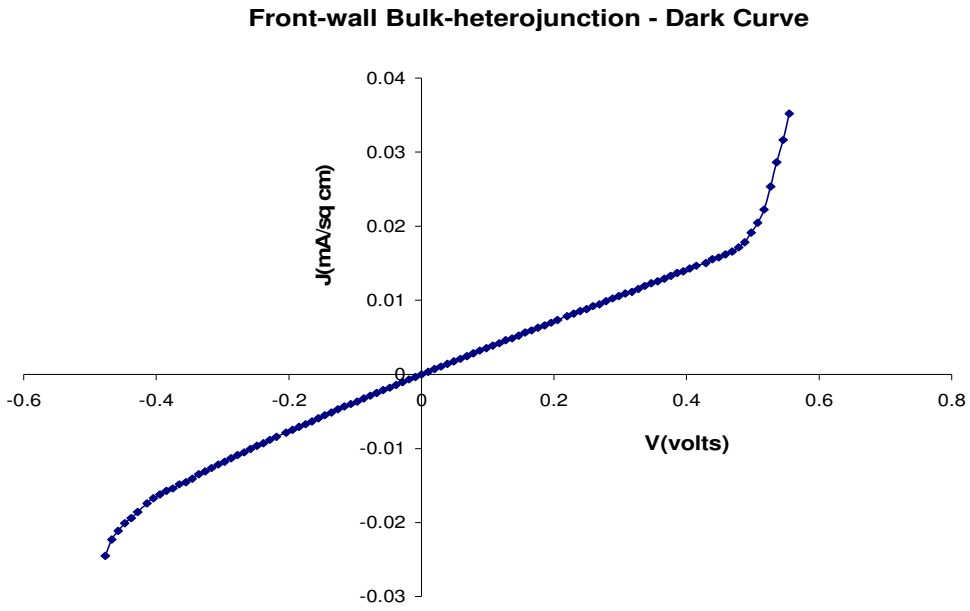

Figure 5.14 Front-wall bulk heterojunction – Dark Curve

The J-V characteristic under light for the device, mciscds13bulk_8, is shown below in Figure 5.15. The light current was higher than the dark current, proving that the device was photoconductive. But there was no significant photovoltaic behavior from the device.

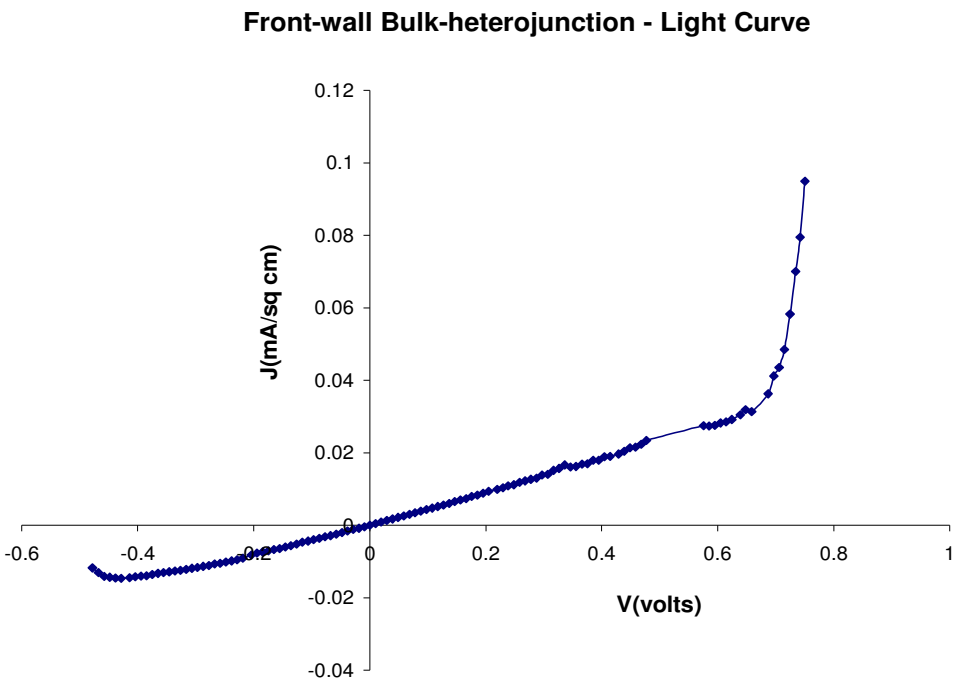

Figure 5.15 Front-wall bulk heterojunction – Light Curve

The front-wall heterostructures made on molybdenum have a high series resistance. There is a slope to the J-V curve in both the forward and the reverse bias conditions. This could be due to the presence of a shunting path between the CdS and CIS. Also there could be lattice mismatch between the CdS and CIS layers resulting in a weak rectifying junction between them. The light curve passes through the origin yielding no V_{oc} or J_{sc}. A selenization treatment could improve the photovoltaic behavior of CIS [17].

The front-wall devices were made with a thin layer of ultrasound-assisted CdS grown on top of thermally evaporated CdS. The nano CdS layer with its higher bandgap [39] is expected to assist in an increased light trapping at the junction. The J-V characteristic for the front-wall devices with nano CdS (device number mciscds9nano_24), under dark conditions, is shown in Figure 5.16.

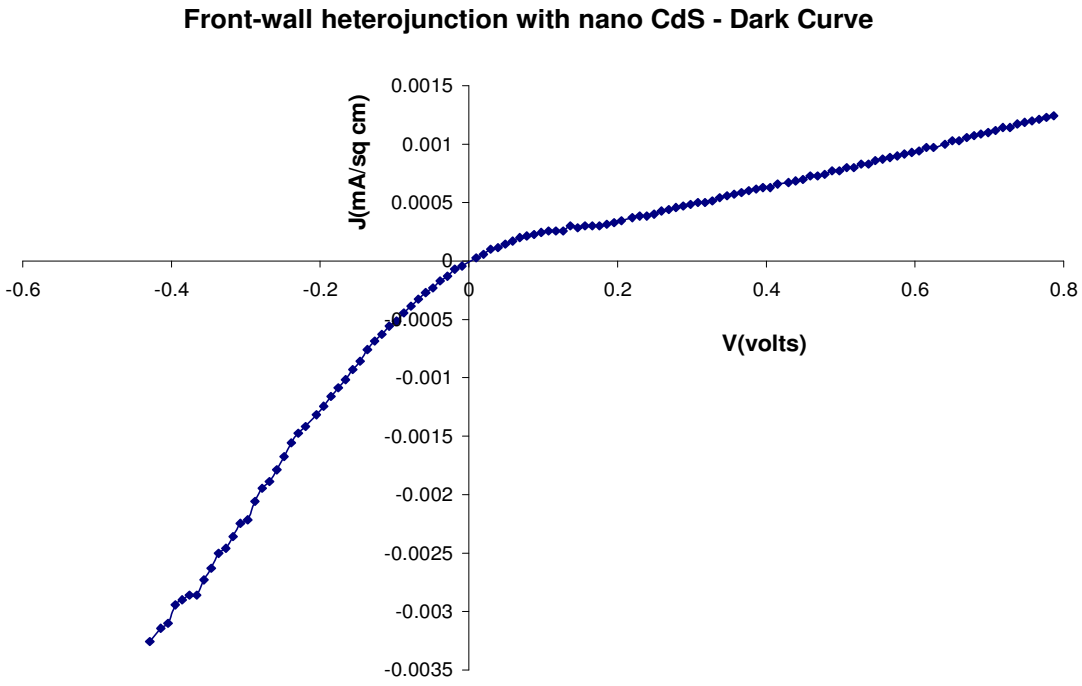

Figure 5.16 Front-wall heterojunction with nano CdS – Dark Curve

The series resistance for this device as calculated from the J-V curve is 6.26e05 $\Omega.cm^2$. The J-V characteristic for the device under light is shown in Figure 5.17.

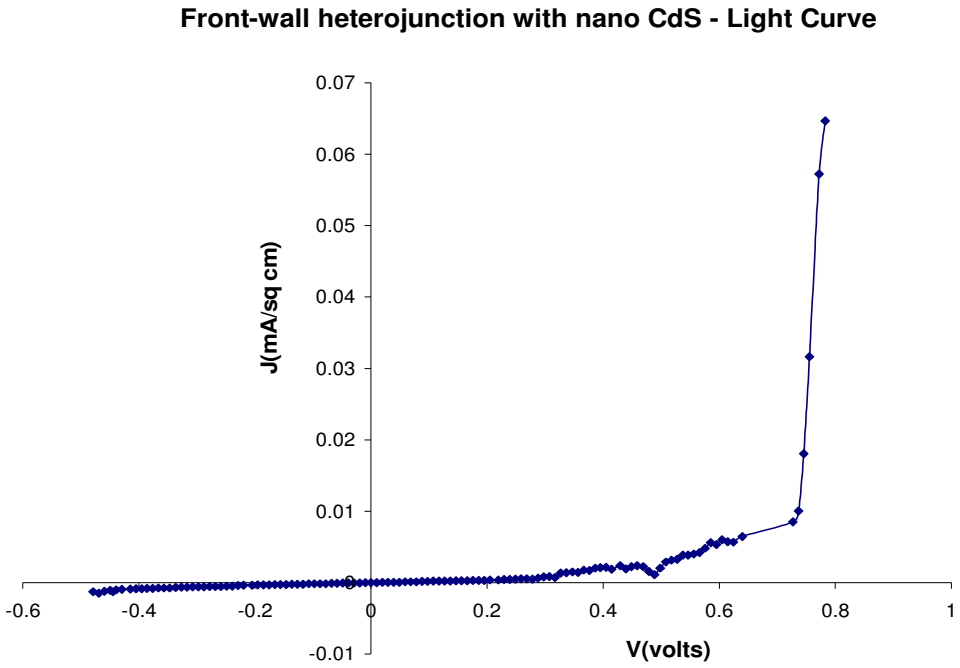

Figure 5.17 Front-wall heterojunction with nano CdS – Light Curve

The front-wall structures with nano CdS have a very high series resistance as can be seen from Figure 5.16. It is possible that a p-n junction is not formed properly in these devices. The fabrication of nano CIS on top of thermally evaporated CdS involves a chemical bath deposition done in an ultrasound medium. Chemical bath deposited CdS sticks best on ITO-coated glass. When the device is immersed in the bath, it is probable that the liquid medium washed off parts of the thermally evaporated CdS. In that case the CdS nano particles generated from the ultrasound medium do not have a crystalline CdS layer to grow on. This could be the explanation for the poor junction formation between CdS and CIS. The devices under light had high series resistance as well and there was no observable V_{oc} or J_{sc}. As shown in Figure 5.17 the light curve passes through the origin.

5.4 J-V Characteristics of Front-wall heterostructures with CIS made from metallic chlorides

Front-wall heterostructures were made on molybdenum substrates with CIS made from metallic chlorides, as detailed in section 3.5.2.2. J-V characteristic of a bulk front-wall heterojunction (device ciscds16_16) is shown below in Figure 5.18. The series resistance of the bulk heterojunction was found to be 1400 $\Omega.cm^2$. The series resistance corrected curve is shown in Figure 5.19. The diode ideality factor was 4 and the reverse saturation current density was 18.4e-06 $A.cm^{-2}$. The ln(J) vs. V plot for the determination of n and J_0 is shown in Figure 5.20.

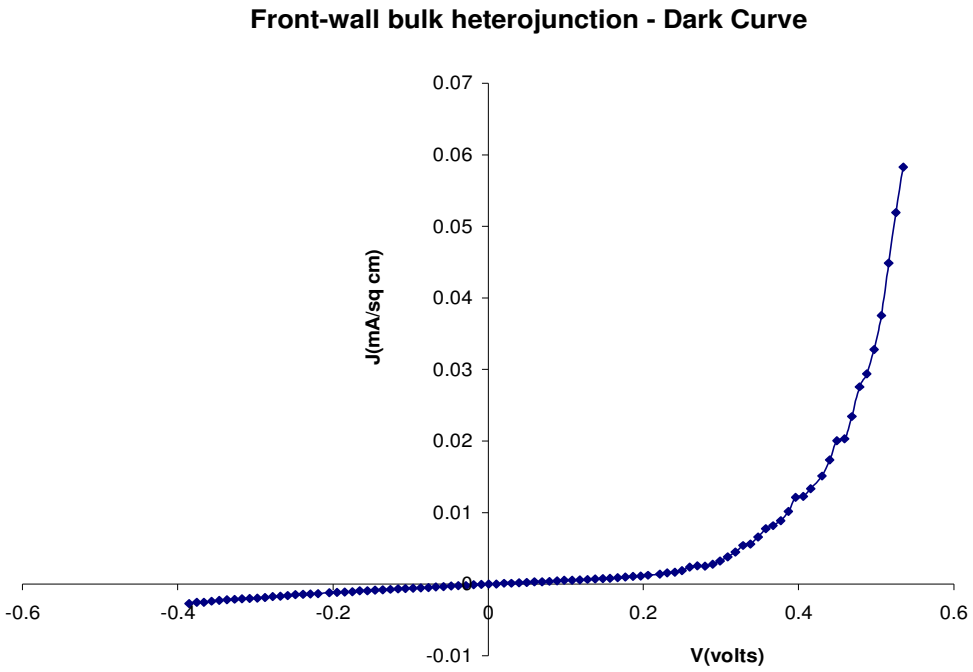

Figure 5.18 Front-wall bulk heterojunction – Dark Curve

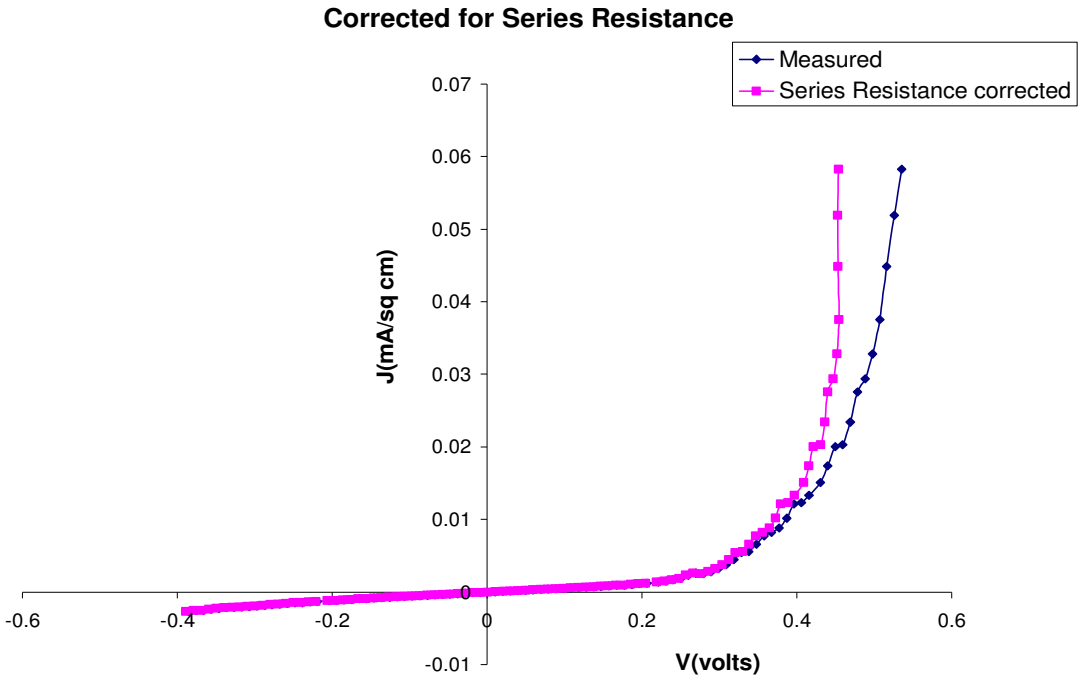

Figure 5.19 Corrected for series resistance – Dark Curve

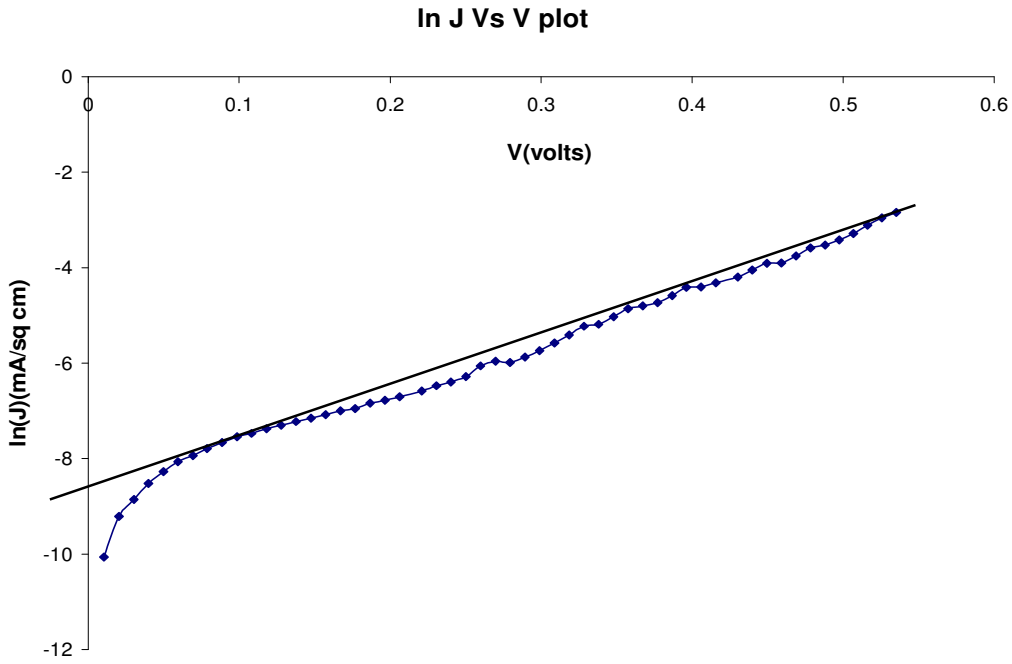

Figure 5.20 ln(J) vs. V plot for determination of n and J_0

The front-wall heterojunctions had a high series resistance as calculated from the J-V characteristic. The slope of the curve, in Figure 5.18, in the reverse bias condition is very small indicating that the device has a very high shunt resistance. With a high shunt resistance one can expect a reasonably good p-n junction between the CdS and CIS layers. However the devices did not display a photovoltaic behavior. There was no observable V_{oc} or J_{sc} from these devices. A selenization treatment of the as-deposited CIS films made from metallic chlorides could improve their opto-electronic properties.

The front-wall heterojunctions with nano CdS had a thin layer of nano CdS grown on top of thermally evaporated CdS. The dark curve for such a device (cisncds17_8) is shown in Figure 5.21.

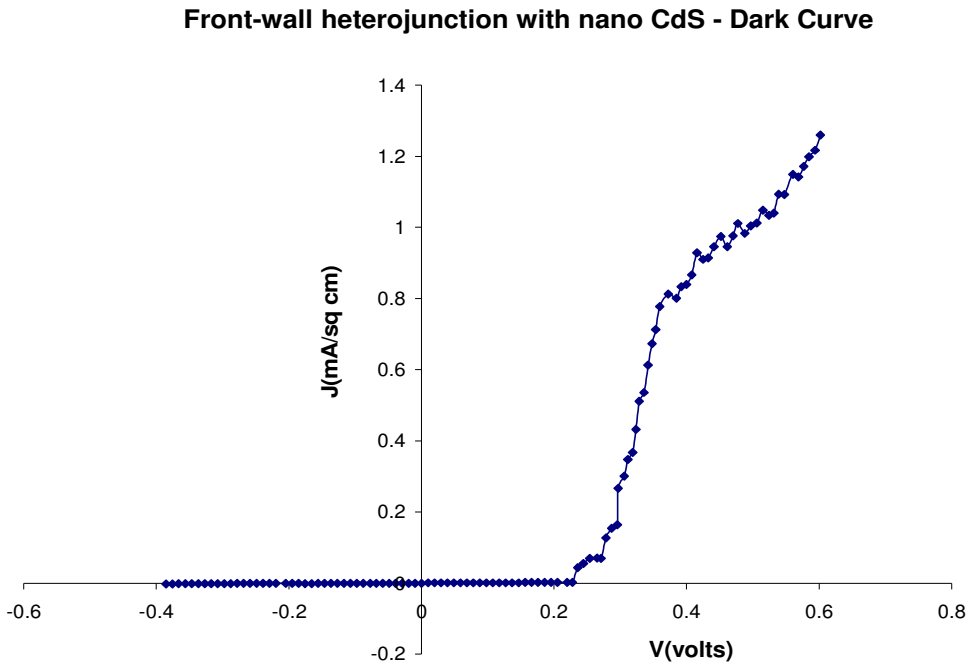

Figure 5.21 Front-wall heterojunction with nano CdS – Dark Curve

From the J-V characteristic it is clear that a good p-n junction does not exist between the CdS and CIS layers. The wet process, involving the deposition of nano CdS

on top of thermally evaporated CdS, could have washed off parts of thermally evaporated CdS leaving behind a poor p-n junction between CdS and CIS.

The best result obtained on the back-wall solar cells was 98 mV of V_{oc} and 3 $mA.cm^{-2}$ of J_{sc}. The back-wall solar cells with nano CdS had a V_{oc} of 10 mV and a J_{sc} of 1.2 $mA.cm^{-2}$. The front-wall solar cells however did not exhibit a photovoltaic behavior. Overall, not very encouraging results were obtained on the CIS/CdS devices in both the front-wall and back-wall configurations. Hence an attempt was made to fabricate Cu_2S/CdS devices on both ITO-coated glass substrates and inside nano-porous alumina templates to study the bulk and nano heterojunctions.

Chapter 6. Results and Discussion for Cu_2S/CdS Devices

6.1 J-V Characteristics

The J-V characteristics of the Cu_2S/CdS solar cells were obtained by applying a voltage across the device and measuring the resulting current with the help of an I-V measurement setup. The I-V measurement setup consisted of two Keithley meters acting as voltmeter and ammeter and a bipolar power supply interfaced to a computer via GPIB cables. Labview software was used to control the setup.

Devices of the structure, ITO/CdS/Cu_2S/Cu/(Ag or Cr/Pb), were made on ITO-coated glass substrates and inside porous alumina templates to compare the performance of bulk and nano heterojunctions.

6.2 J-V Characteristics of Cu_2S/CdS devices with copper top contact

The bulk heterojunction was fabricated on ITO-coated glass substrates with an 80 nm thick copper layer acting as the ohmic contact to Cu_2S. The CdS layer was 8 microns thick and the CuCl layer was 1 micron thick. Vacuum anneal of the device would convert 60% of CuCl into Cu_2S, forming 0.6 microns of Cu_2S. Correspondingly 0.6 microns of CdS would be consumed in supporting the growth of Cu_2S through it. The device would have 7.3 microns of CdS and 0.6 microns of Cu_2S. The dark curve for the junction is shown below in Figure 6.1. The series resistance was calculated from the J-V characteristic as described in section 5.2.1, and was found to be 17 $\Omega.cm^2$. The diode ideality factor and reverse saturation current density were calculated from the J-V characteristic as described in section 5.2.2. The value of n was 2.7 and J_0 was found to be 5.52e-06 $A.cm^{-2}$. Since the value of n is close to 2, it can be concluded the current

transport in this device is recombination current dominated [40]. The dark curve corrected for series resistance is shown in Figure 6.2.

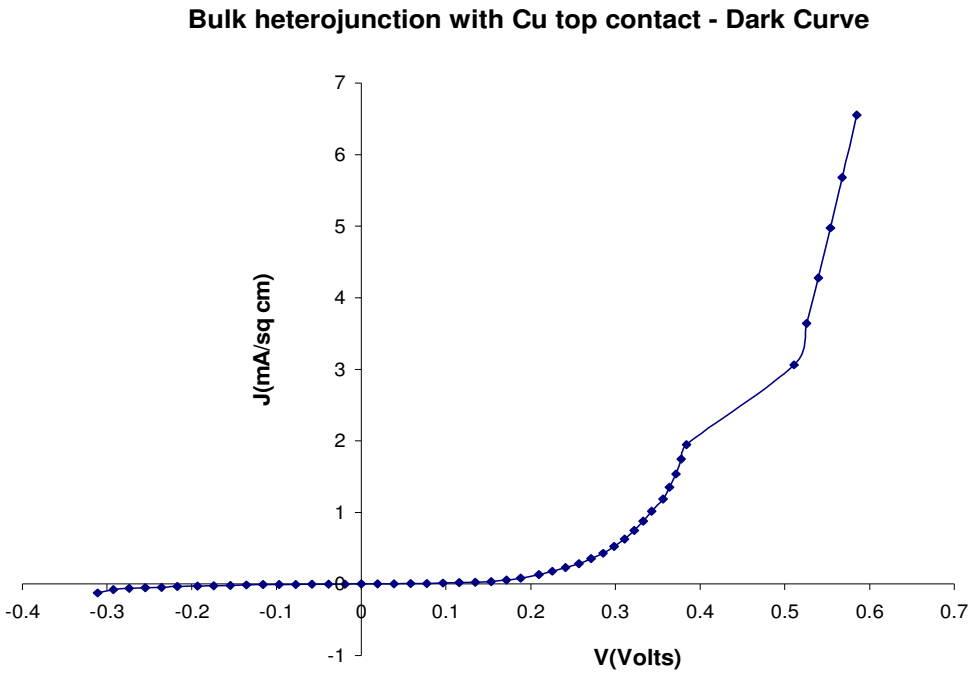

Figure 6.1 Bulk heterojunction with Cu top contact – Dark Curve

From Figure 6.1 it can be seen that the device is series resistance dominated once the voltage drop across the junction exceeds 0.4 V. This is reasonable since the CdS layer is 7.3 microns thick and is known to be resistive in nature. The series resistance here would be due to the sum of the resistances between CdS/ITO, Cu_2S/Cu, quasi neutral regions in the CdS and Cu_2S layers. From the curve it can be seen that the reverse saturation current is low. This can be attributed to a high shunt resistance between the CdS and Cu_2S layers. This is reasonable since the thickness of the CdS layer is 7.3 microns and it would be difficult for the Cu_2S layer to seep all the way through it to be able to cause a finite shunt resistance.

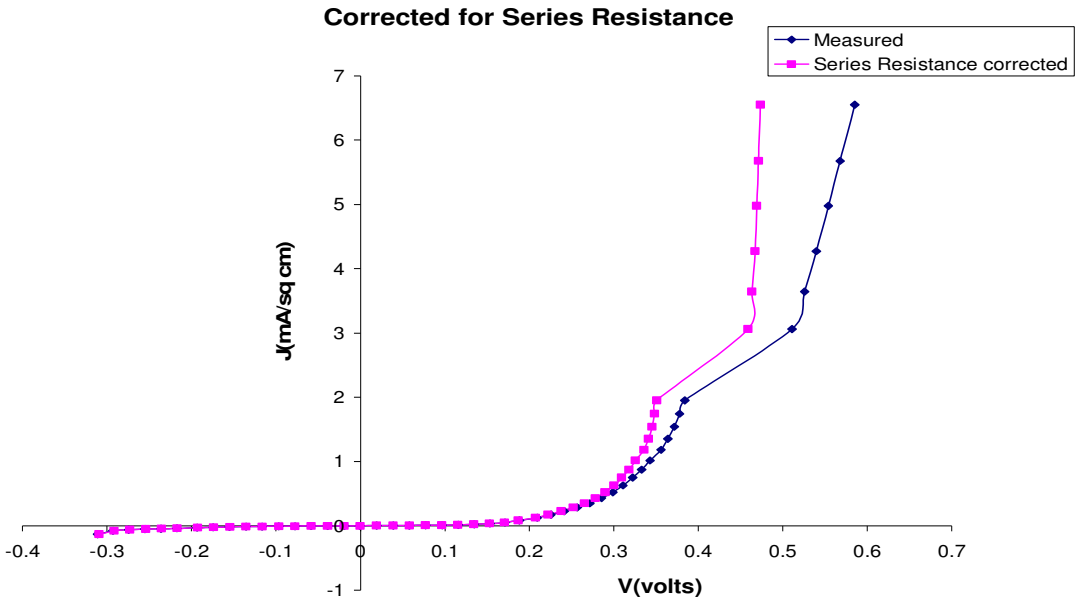

Figure 6.2 Corrected for series resistance – Dark Curve

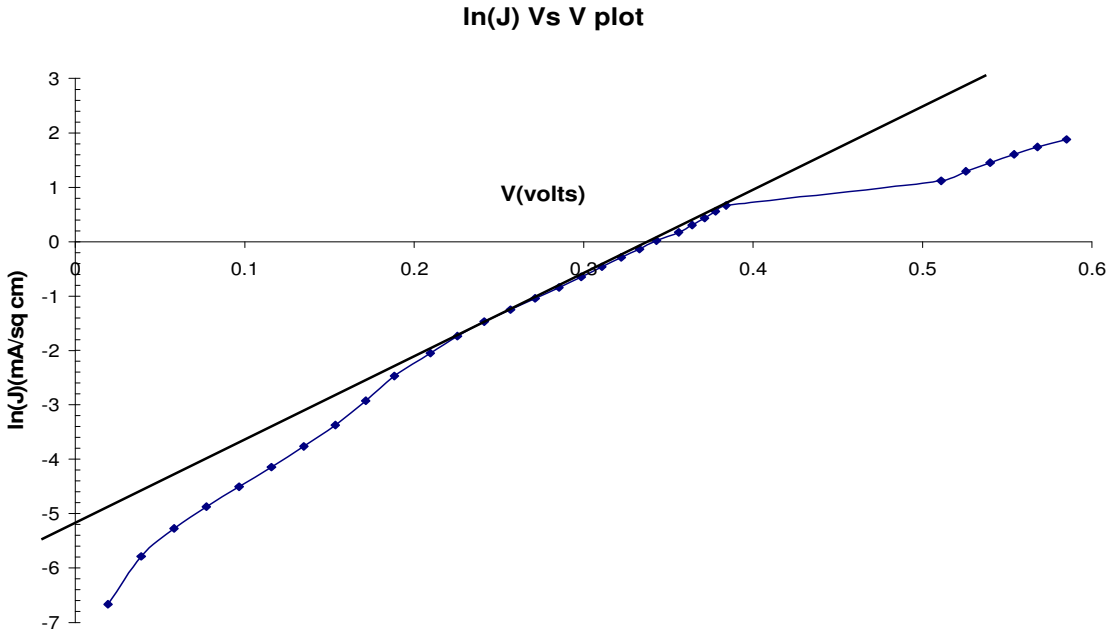

Figure 6.3 ln(J) vs. V plot for determination of n and J_0

The junction was then illuminated to study its light behavior. Figure 6.4 shows the J-V characteristic of the junction under light.

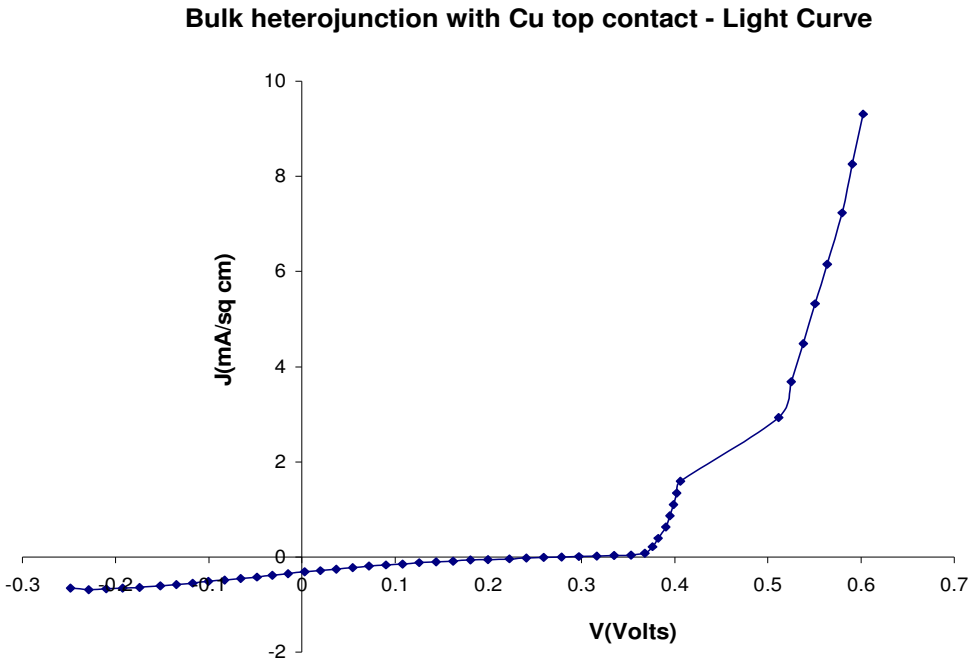

Figure 6.4 Bulk heterojunction with Cu top contact – Light Curve

Photovoltaic parameters namely, J_{sc}, V_{oc}, power delivered and fill factor, were computed from the J-V light curve through a matlab code [Refer Appendix]. The cell had a V_{oc} of 280 mV, J_{sc} of 0.32 mA.cm^{-2}. The power delivered was 0.0376 mW.cm^{-2} and the fill factor was 0.4185. The cell had an efficiency of 0.04%. The cell has a low V_{oc} and J_{sc}, which can be attributed a high series resistance contributed by the thick CdS layer. The low J_{sc} could also be due to a high surface recombination velocity which causes more than 50% of the photogenerated carriers close to the surface to be captured. Surface recombination is known to affect the photogenerated current for Cu_2S/CdS solar cells [41].

6.3 J-V Characteristics of Cu_2S/CdS devices with silver top contact

The bulk heterojunction was fabricated on ITO-coated glass substrates. CdS of thickness 8 microns and CuCl of thickness 1 micron were thermally evaporated on ITO. Annealing the devices in vacuum resulted in 7.3 microns of CdS and 0.6 microns of Cu_2S. Silver paste was applied on top of Cu_2S to form the ohmic contact. The dark curve for the device is shown in Figure 6.5.

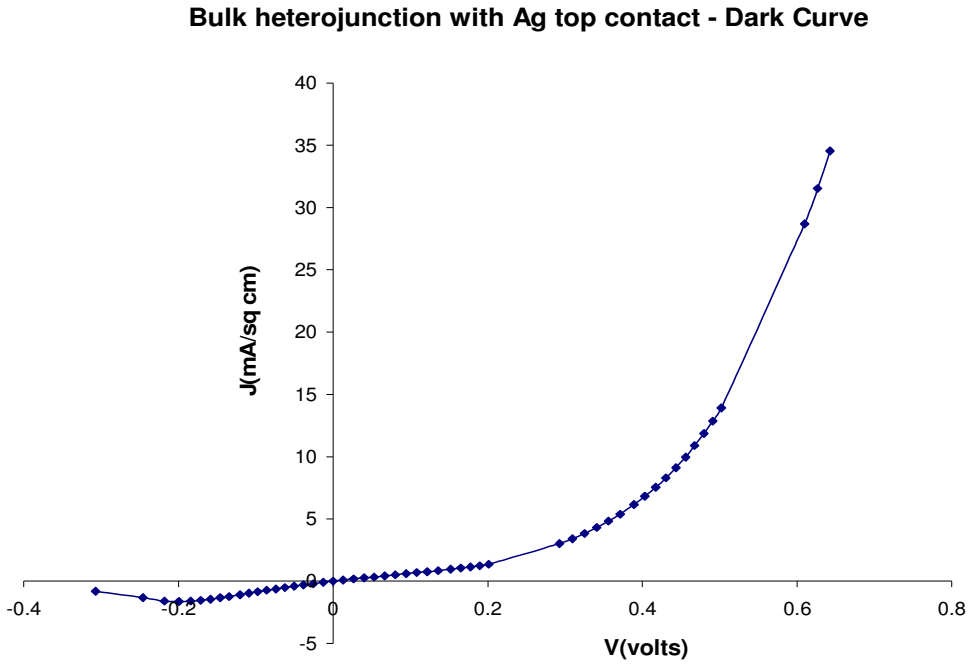

Figure 6.5 Bulk heterojunction with Ag top contact – Dark Curve

The curve was corrected for series resistance and the plot is shown in Figure 6.6 below. The series resistance was found to be 5.6 $\Omega.cm^2$. Figure 6.6 shows the ln(J) vs. V plot used to obtain the diode ideality factor and reverse saturation current density. The value of n was found to be 5.3 and J_0 was found to be 3e-04 $A.cm^{-2}$. The high value of n indicates that the current transport in the device cannot be explained with a simple diffusion current dominated model. The current transport could be a combination of

diffusion currents, recombination-generation currents, tunneling from band states to localized defect centers and band-to-band tunneling. This is reasonable since the heterojunction formed between CdS and Cu_2S has problems of lattice mismatch and difference in electron affinities. The lattice mismatch also gives rise to deep interface states at the junction between CdS and Cu_2S which could act as recombination centers [40].

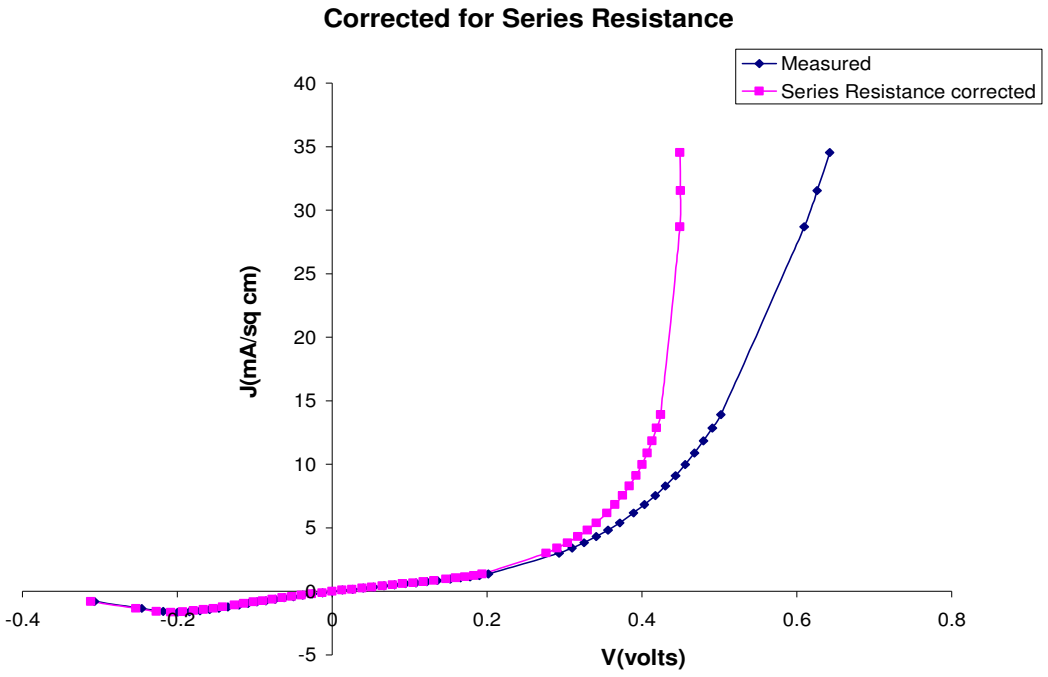

Figure 6.6 Corrected for series resistance – Dark Curve

Figure 6.7 shows the light curve for the device. The curve was analyzed with a matlab code to determine the precise values of V_{oc}, J_{sc}, power delivered and fill factor. The V_{oc} was 302 mV and J_{sc} was 21.8 mA.cm^{-2}. The power delivered was 3.54 mW.cm^{-2} and the fill factor was 0.536. The cell had an efficiency of 3.54%.

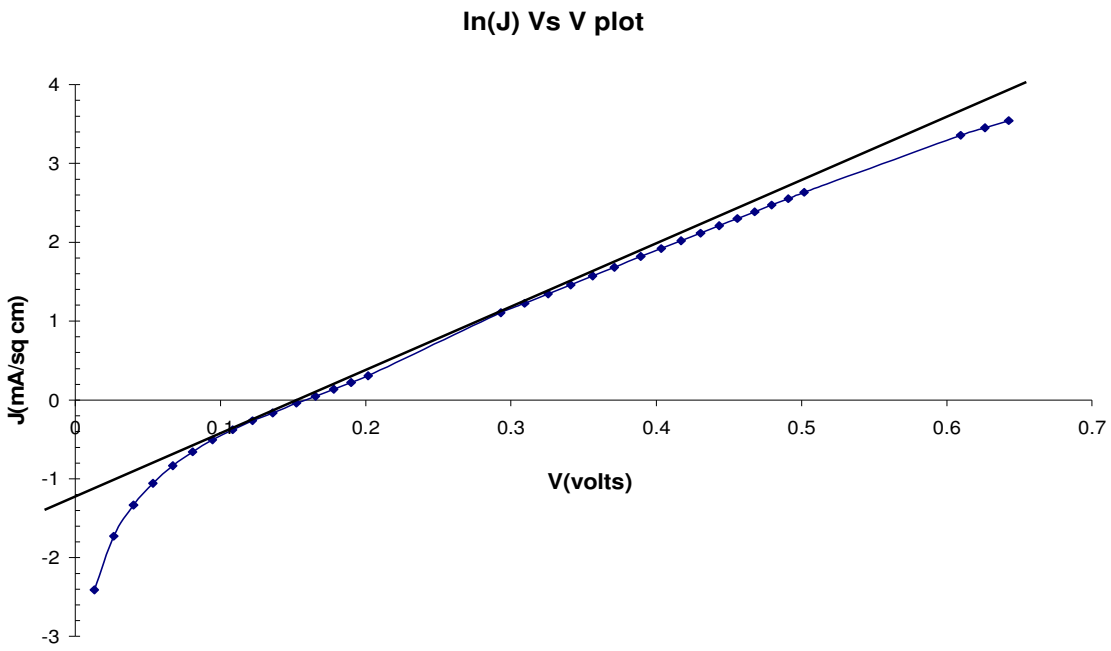

Figure 6.6 ln(J) vs. V plot for determination of n and J_0

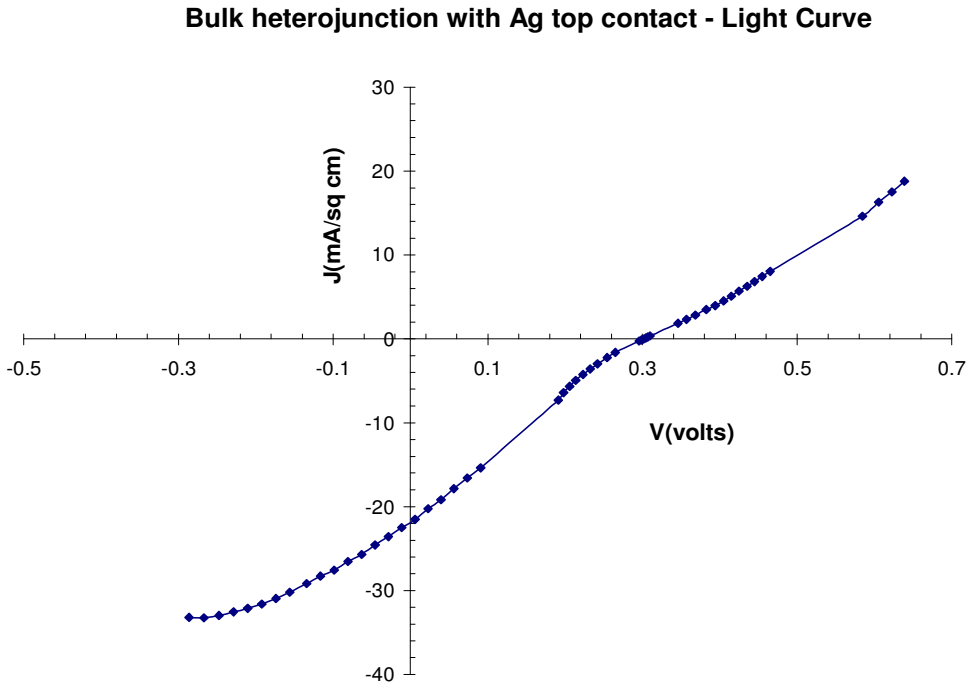

Figure 6.7 Bulk heterojunction with Ag top contact – Light Curve

The light current is higher than the dark current as can be seen from the dark and light curves. Photoconductivity of the device accounts for this increase in light current. A change in conductivity, $\Delta\sigma$, upon illumination, called photoconductivity results when light absorption increases the values of dark-free carrier densities n and p, and/or the dark mobilities μ_n and μ_p. Hence,

$$\Delta\sigma = e(\Delta n\mu_n + \Delta p\mu_p) \quad \text{.....(6.1)}$$

$$\Delta\sigma = e(n\Delta\mu_n + p\Delta\mu_p) \quad \text{.....(6.2)}$$

The change in mobility upon illumination could occur if the material is inhomogeneous, in which case the n and p type material are not uniform throughout. It is possible that a material could have high conductivity regions separated by narrow low conductivity regions in the dark. The low conductivity regions would act as barriers to the flow of current between the high conductivity regions, thus limiting conductivity. When light is absorbed in these low conductivity regions, the resistance of these barriers would be reduced and the flow of current through the material would be much greater than that in the dark.

From the light curve one can observe that there is a slope to it in the third and the fourth quadrant. This can be attributed to the finite shunt resistance between CdS and Cu_2S. Figure 6.8 below shows a zoomed in view of the Cu_2S/CdS junction.

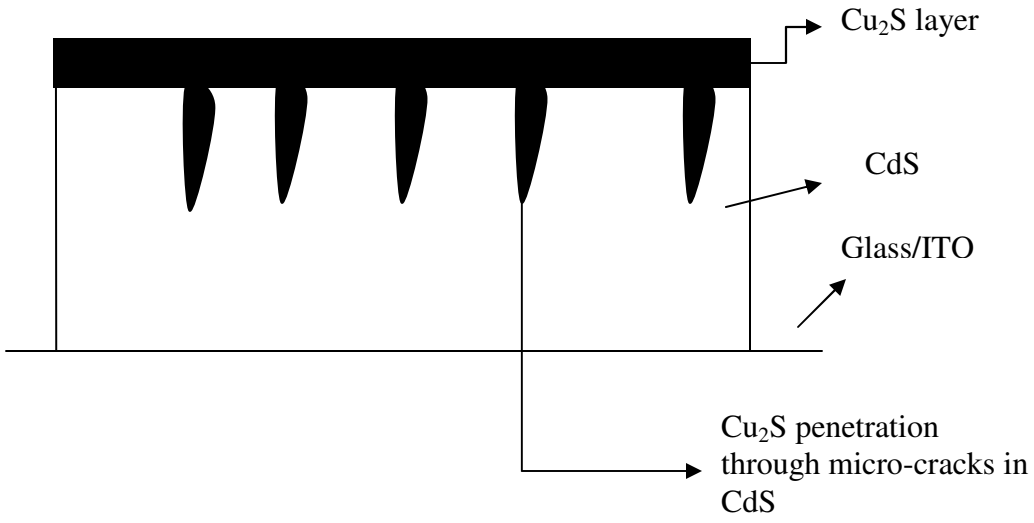

Figure 6.8 Shunting paths between Cu_2S and CdS

Cu_2S could penetrate through the grain boundaries and micro cracks in the CdS film and thus create shunting paths in it [42, 43]. These shunting paths give rise to very small shunt resistances which result in the current through the device to be dependent on voltage, in reverse bias. The light behavior of the device (in Figure 6.7) suffers from a very small shunt resistance. Because of the slope to the curve in the fourth quadrant, the V_{oc} obtainable from the device also decreases. A heat treatment of the device could cause the thin layers of Cu_2S to disappear from the grain boundaries, thus eliminating the shunting paths [40]. The device also exhibits a very high series resistance in the forward bias. Thus the presence of both, a very high series resistance and a very low shunting resistance lead to a reduction in the fill factor for the solar cell. The highest open circuit voltage obtained with a silver contact was 453 mV. Devices with high open circuit voltages were able to be fabricated reproducibly.

6.4 J-V Characteristics of Cu_2S/CdS devices with chromium/lead top contact

Bulk heterojunctions of Cu_2S/CdS were fabricated on ITO coated glass substrates. CdS of thickness 4 microns and CuCl of thickness 0.5 micron were evaporated to form the junction. The vacuum anneal would yield a Cu_2S thickness of 300 nm and a CdS thickness of 3.7 microns. Chromium was evaporated as the top ohmic contact for Cu_2S and a one micron thick layer of lead was evaporated on top of chromium to improve its conductivity. The dark curve for the device is shown below in Figure 6.9.

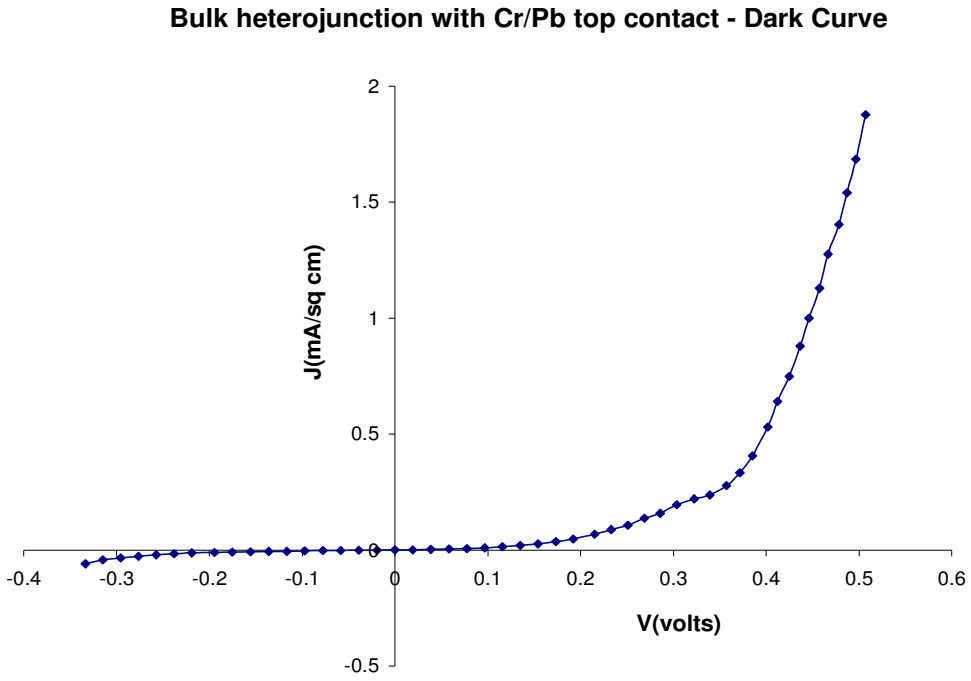

Figure 6.9 Bulk heterojunction with Cr/Pb top contact – Dark Curve

The curve was corrected for series resistance and the corrected plot is shown in Figure 6.10. The series resistance was found to be 54 $\Omega.cm^2$. From the reverse biased mode of operation it is clear that there is a high shunt resistance. The ln(J) vs. V plot used to compute the diode ideality factor and the reverse saturation current density is shown in Figure 6.11.

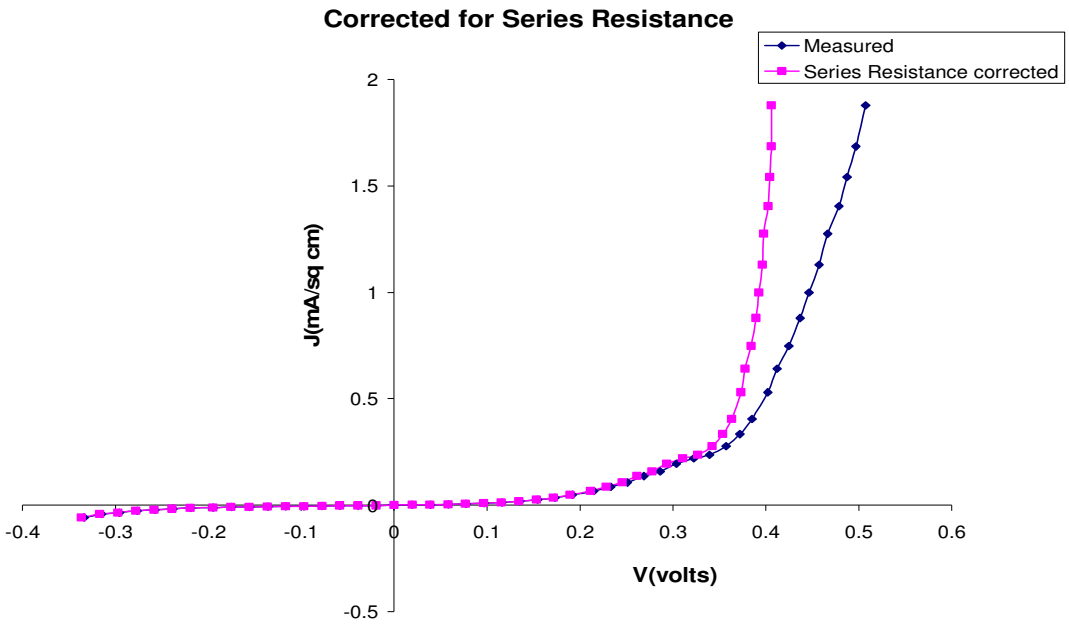

Figure 6.10 Corrected for series resistance – Dark Curve

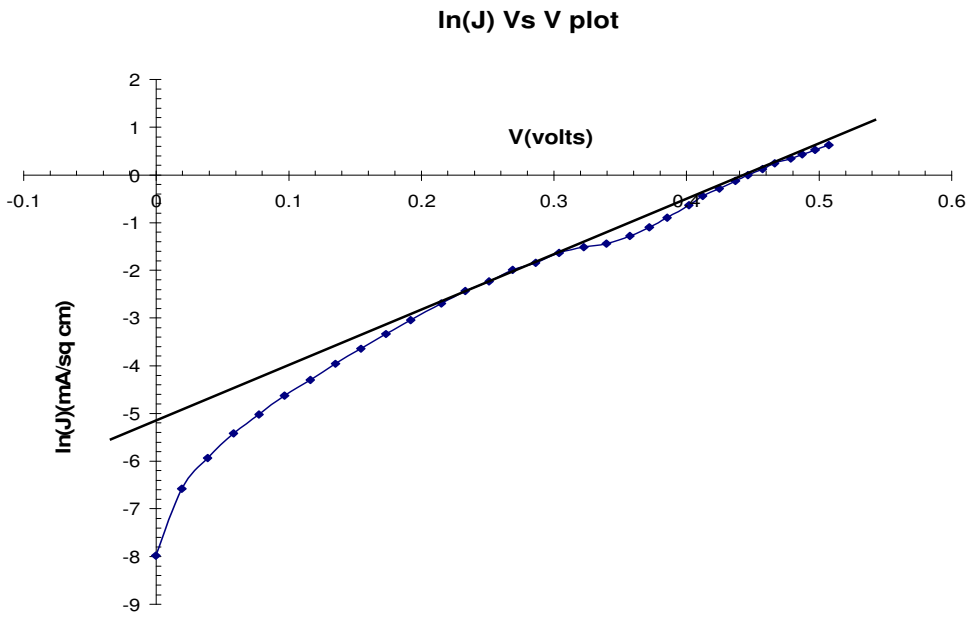

Figure 6.11 ln(J) vs. V plot for determination of n and J_0

The diode ideality factor was found to be 3.4 and J_0 was found to be 6.09e-06 $A.cm^{-2}$. The light curve for the device is shown in Figure 6.12. The J-V data for the

device was analyzed with a matlab code to calculate the precise values of V_{oc}, J_{sc}, power delivered and fill factor. The cell yielded a V_{oc} of 445 mV and a J_{sc} of 20.3 mA.cm^{-2}. The power delivered was -5.73 mW.cm^{-2} and the fill factor was 0.635. The cell had an efficiency of 5.73%.

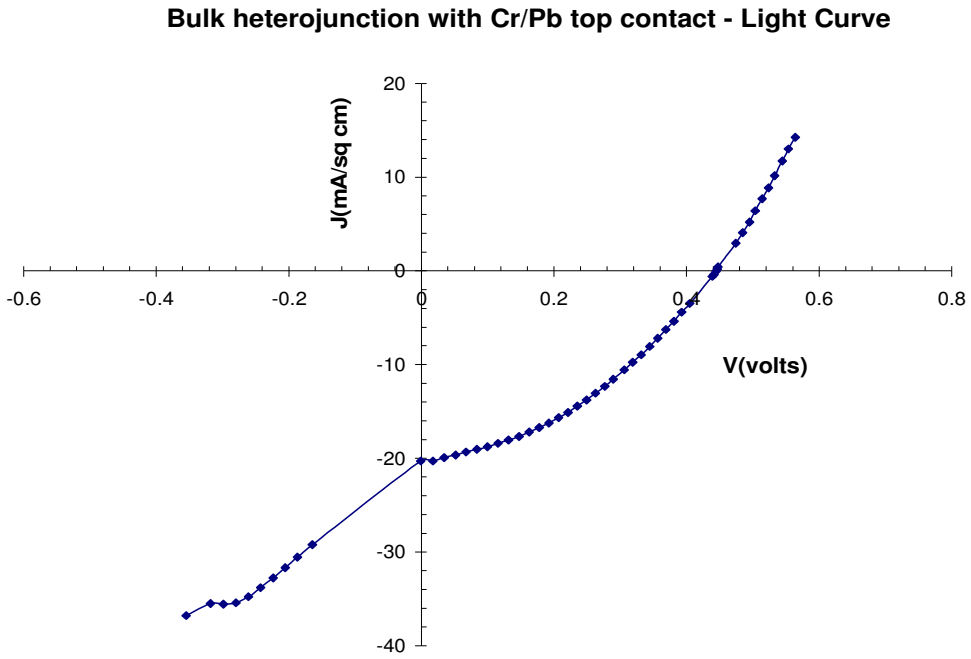

Figure 6.12 Bulk heterojunction with Cr/Pb top contact – Light Curve

The light current is much higher than the dark current because of the photoconductive effect explained in section 6.3. The slope in the third quadrant indicates the presence of a low shunt resistance between CdS and Cu_2S. The photovoltaic behavior of the device in the power quadrant is affected by presence of both series and shunt resistances as can be seen from the light curve. The presence of the series resistance tends to reduce the short circuit current density and the presence of a low shunt resistance tends to reduce the open circuit voltage. The presence of both R_s and R_{sh} reduce the fill factor of the device.

Chromium/lead contacts yielded the best results for the Cu_2S/CdS solar cells in comparison to the silver and copper top contacts. The highest open circuit voltage obtained on the cells with a chromium/lead contact was 464 mV and the corresponding short circuit current density was 21.5 $mA.cm^{-2}$. The cell had a fill factor of 0.69 and an efficiency of 6.9%.

6.5 J-V Characteristics of Cu_2S/CdS devices fabricated inside nano-porous alumina templates

Nano structured heterojunction solar cells were fabricated inside porous alumina templates by an all evaporation process. 3.5 microns of CdS and 3 microns of CuCl were evaporated on the porous alumina templates. This resulted in 1.8 microns of Cu_2S and 1.7 microns of CdS inside the pores which are roughly 4 microns in depth. Since the 3.5 microns thick CdS layer supports the growth of Cu_2S inside it, the heterojunction would be formed inside the nano pore. The dark curve for this device is shown below in Figure 6.13. The curve was corrected for series resistance and the corrected plot is shown in Figure 6.14. The series resistance was found to be 1323 $\Omega.cm^2$. Such a huge value for the series resistance indicates that the device suffers from a very poor ohmic contact. The ln(J) vs. V plot used to obtain the diode ideality factor and the reverse saturation current density is shown in Figure 6.15. The value of n was found to be 4.7 and J_0 was found to be 2.25e-07 A/cm^{-2}.

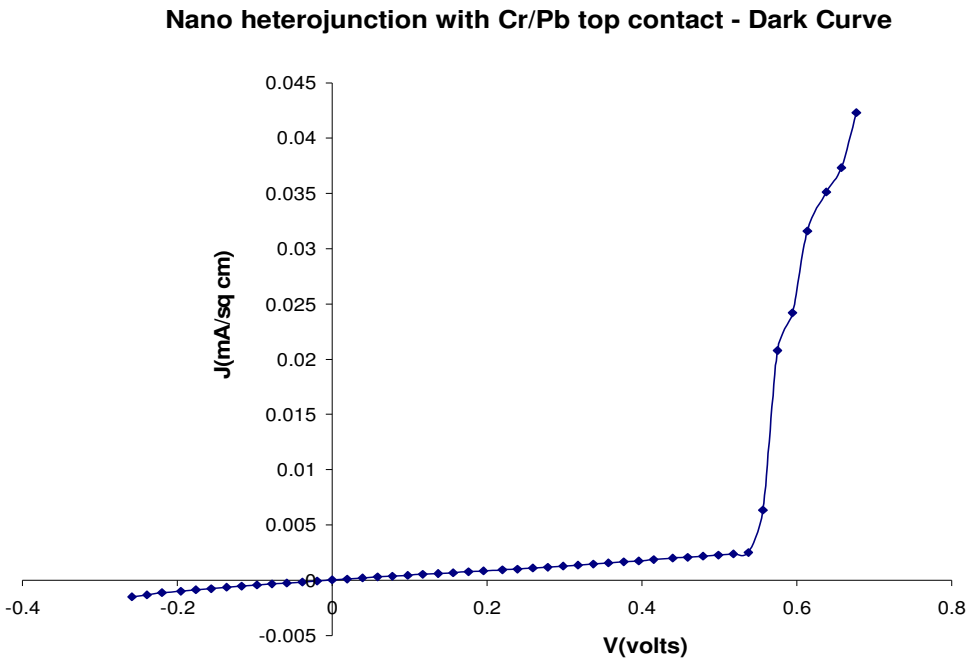

Figure 6.13 Nano heterojunction with Cr/Pb top contact – Dark Curve

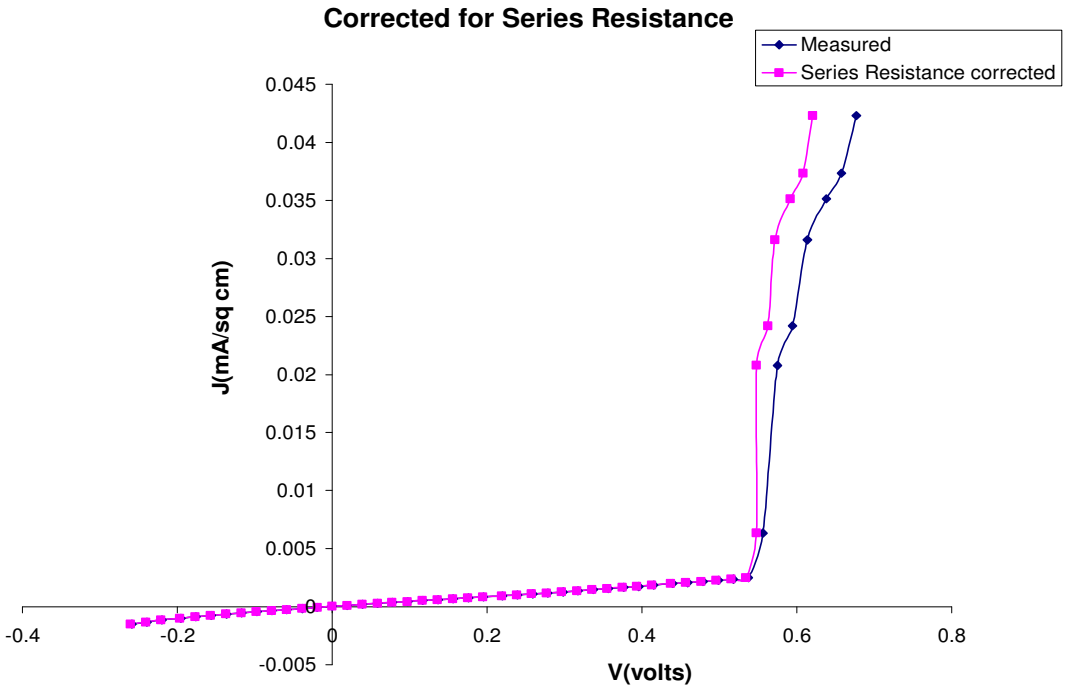

Figure 6.14 Corrected for Series Resistance – Dark Curve

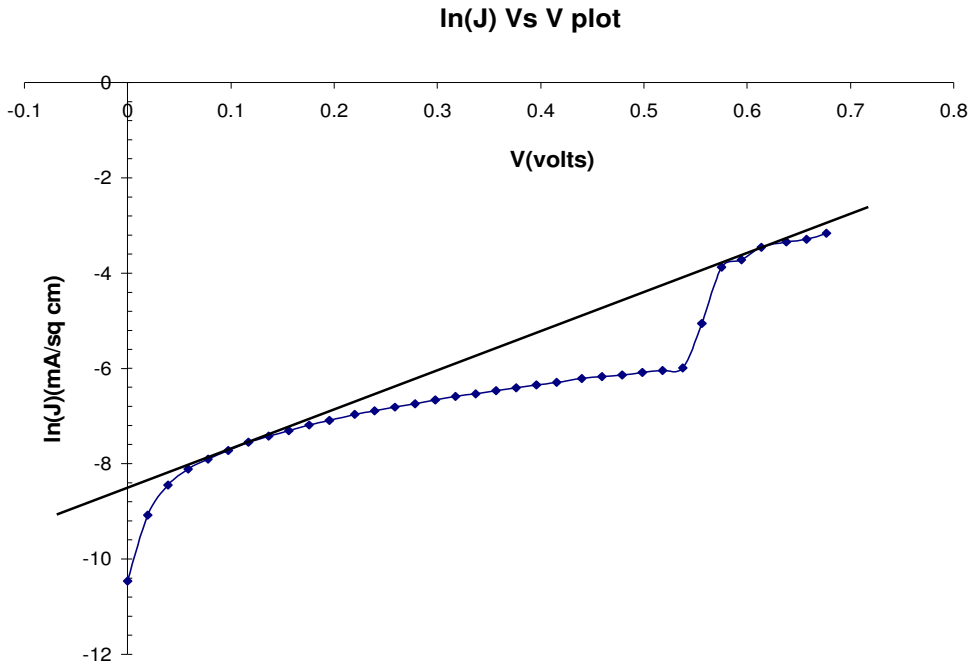

Figure 6.15 ln(J) vs. V plot for determination of n and J_0

The light curve for the device is shown in Figure 6.16. The curve was analyzed with a matlab code to determine the precise values of V_{oc}, J_{sc}, power delivered and fill factor. The nano heterojunction solar cell yielded a V_{oc} of 367 mV and a J_{sc} of 0.0178 $mA.cm^{-2}$. The power delivered by the cell was 0.0034 $mW.cm^{-2}$ and the fill factor was 0.526. The cell had an efficiency of 0.0034%. The bulk and the nano heterojunctions have comparable open circuit voltages, but they differ only in the magnitudes of the light-generated currents. The bulk devices have light-generated currents of the order of tens of milliamperes while the nano scale heterojunctions have currents of the order of tens of microamperes. One of the major reasons for the poor photovoltaic behavior (caused by poor light-generated currents) of the nano scale heterojunctions, is the presence of poor ohmic contacts to the CdS layer. Figure 6.17 shows the cross section of the nano scale heterojunction formed inside the porous alumina template.

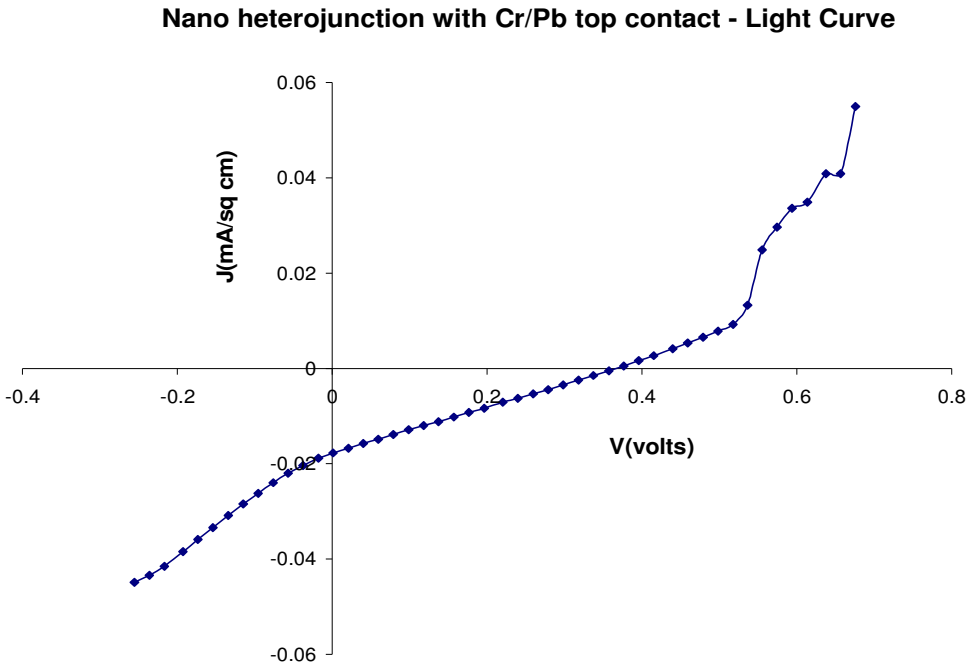

Figure 6.16 Nano heterojunction with Cr/Pb top contact – Light Curve

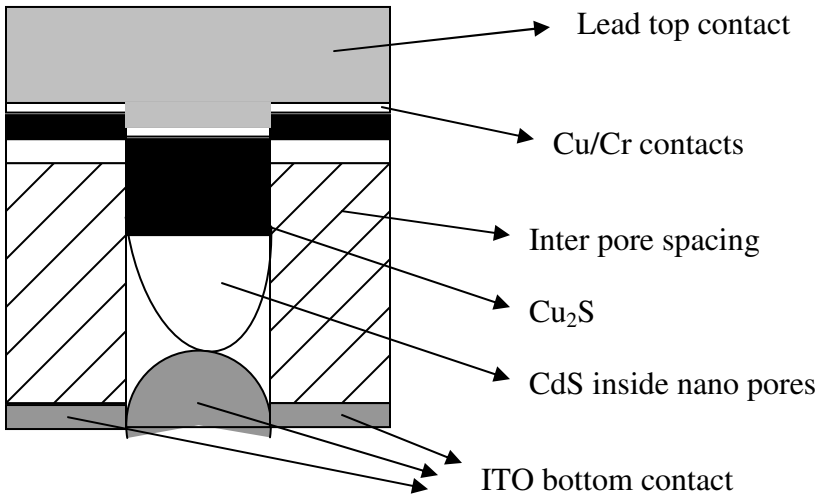

Figure 6.17 Cross-section of Cu_2S/CdS junction inside nano porous alumina

SEM pictures of the back side of the porous alumina film do not show CdS in it. Hence CdS must not be filling the pores completely. It could get stuck somewhere in the middle. The high aspect ratio between the pore depth and diameter would be the major reason for CdS filling the pore partially. When ITO is sputtered from the other side of the foil, it is possible that the contact formed could be a poor one as shown in Figure 6.17. Such a poor contact between CdS and ITO could give rise to a large series resistance. There could also be additional shunt resistive paths between Cu_2S and CdS inside the pore, as Cu_2S could seep through the nano grain boundaries of CdS. Thus the solar cell under illumination could be approximated by the circuit shown in Figure 2.2. I_L, R_s, R_{sh} and I_{diode} are the light current, series resistance, shunt resistance and diode current respectively. It is very clear that a high series resistance would lower the light generated current. Also the presence of a low shunt resistive path between Cu_2S and CdS would give rise to a larger reverse saturation current I_0. Now considering the expression for open circuit voltage given below,

$$V_{OC} = \frac{nkT}{q} \ln\left[\frac{I_L}{I_0} + 1\right] \quad \text{.....(6.3)}$$

it is clear that an increase in I_0 and a decrease in I_L would lead to a reduction in the open circuit voltage obtainable from the device. This could be the explanation for the low open circuit voltages observed on the nano heterojunctions. Thus it can be concluded that both the light and dark behavior of the junction are series resistance (and to some extent shunt resistance) limited. The reduction in light current and hence the decrease in V_{oc} reduce the power delivered by the cell. The reduction in the power delivered also reduces the fill factor and hence the efficiency of the cell.

Device	Expected V_{oc}	Observed V_{oc}
Cu_2S/CdS – Bulk junction	600 mV	464 mV
Cu_2S/CdS – Nano junction	800 mV	367 mV

Table 6.1

Table 6.1 shows the observed and expected values of the open circuit voltage for the bulk and nano Cu_2S/CdS heterojunctions. The V_{oc} expected in the bulk heterojunctions are reduced from the observed values due to the presence of a finite shunt resistance. With the nano heterojunctions an increase in the bangap of the window material is expected. The bandgap of CdS could be expected to increase from 2.45 eV to 3 eV, because of quantum confinement. The bandgap of Cu_2S could be expected to increase from 1.2 eV to 1.5 eV, which is the ideal bandgap for an absorber material to take full advantage of the solar spectrum. Since the bandgap of CdTe is also 1.5 eV, the nano Cu_2S/CdS heterojunctions are expected to match the highest open circuit voltage observed in the CdTe/CdS solar cells which is 800 mV. But such high open circuit voltages were not observed in the nano Cu_2S/CdS heterojunctions. The performance of these cells was greatly limited by series resistances arising out of poor contacts to the window material. These cells can be improved by reducing the thickness of the porous alumina foil. The reduction in the thickness of the foil reduces the aspect ratio. This would make it easier for the CdS to get through the pore depth completely. With CdS having gone all the way through the pore, better ohmic contacts can be made to it. The improved ohmic contacts would reduce the series resistance associated with the cell

considerably and hence improve the J_{sc}, V_{oc} and fill factors for the cell. More experiments need to be done to optimize the thickness of the porous alumina films and to improve the open circuit voltage of the cells.

Chapter 7. Conclusion

CIS/CdS heterojunction solar cells were fabricated on both ITO-coated and molybdenum-coated glass slides. The back-wall heterojunction solar cells with nano CIS yielded an open-circuit voltage of 10 mV and a short-circuit current density of 1.2 $mA.cm^{-2}$. The back-wall bulk heterojunctions yielded an open-circuit voltage of 98 mV and a short-circuit density of 3 $mA.cm^{-2}$. The annealing step that the bulk devices went through, improved their crystallinity and the photovoltaic property of the CIS films. The high currents in the devices with nano CIS was attributed to availability of a shunting path between the top contact and the CdS layer via the nano grain boundaries of CIS. The front-wall heterojunction with bulk and nano CdS did not yield any appreciable V_{oc} or J_{sc}. A selenization treatment of the as-deposited CIS films could improve the photovoltaic behavior of the device.

Cu_2S/CdS heterojunction solar cells have been fabricated on ITO-coated glass slides and inside nano porous alumina templates. The bulk heterojunctions were fabricated with three different top metallic contacts to Cu_2S. The cells with a copper top contact had a V_{oc} of 280 mV, a J_{sc} 0.32 $mA.cm^{-2}$ and an efficiency of 0.04%. The cells with silver top contact had a V_{oc} of 302 mV, a J_{sc} of 21.8 $mA.cm^{-2}$ and an efficiency of 3.54%. The highest V_{oc} obtained on cells with silver top contact was 453 mV. The cells with chromium/lead top contact had a V_{oc} of 445 mV, a J_{sc} was 20.3 $mA.cm^{-2}$ and an efficiency of 5.73%. A highest V_{oc} of 464 mV was obtained on the Copper sulfide solar cells with a chromium/lead top contact.

Nano structured Cu_2S/CdS solar cells were fabricated inside nano porous alumina templates by an all evaporation process. The nano solar cell had a V_{oc} of 367 mV , a J_{sc} of

0.0178 $mA.cm^{-2}$ and an efficiency of 0.0034%. The very low efficiencies of the nano solar cells were attributed to a very high series resistance arising out of the poor contacts to CdS. The high series resistance reduces the light current and since the V_{oc} depends logarithmically on the light-generated current, it suffers a little.

The efficiency of the nano solar cells can be greatly improved by fabricating the solar cells inside a much thinner porous alumina foil. Fabrication of thin porous alumina foils will reduce the aspect ratio and make it easier to force CdS through the pores. With CdS having gone all the way down to the bottom of the pore, a better contact between CdS and ITO could be expected. This would improve the light currents and open-circuit voltages and hence yield better efficiencies by taking advantage of the nano confinement of the CdS and Cu_2S and the improvement in the optical path length for the incident light.

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Appendix

Matlab Code used to determine the values of J_{sc}, V_{oc}, power delivered and fill factor

```
% Procedure for calculating open-circuit voltage, short-circuit
current,
% power delivered and fill factor:
%
% The x and y interecept are calculated as follows:
% 1. The 'x' values are read through in order to see where it changes
sign;
% these two points are x1 and x2; it's corresponding y values are y1
and
% y2.
% 2. The slope of the line is calculated as m = (y2-y1)/(x2-x1)
% 3. The constant 'c' in the equation y = mx+c is evaluated as c =
% y1-(m*x1)
% 4. The short circuit current density is 'c'.
% 5. Similarly, the value of open-circuit voltage is calculated as -c/m
% 6. The power delivered by the solar cell is calculated by summing the
% values of -jsc.delta_V over the interval (0,Voc)
% 7. The fill factor is calculated as Power delivered/(jsc*voc)

% Locate the data files

t1 = load('c:\solar\CrPbLnano.txt');

% Reading values of the data files into matlab arrays

x = t1(:,1);

y = t1(:,2);

plot(x,y)

% Computing short-circuit current density

for i=1:size(x)
    if (x(i)<0 & x(i+1)>0)
        x1 = x(i);
        x2 = x(i+1);
        y1 = y(i);
        y2 = y(i+1);
    end
end

m = (y2-y1)/(x2-x1);

c = y1-(m*x1);

jsc = c

% Computing open-circuit voltage
```

```
for i = 1:size(x)
    if (y(i)<0 & y(i+1)>0)
        x3 = x(i);
        x4 = x(i+1);
        y3 = y(i);
        y4 = y(i+1);
    end
end

m = (y4-y3)/(x4-x3);

c = y3-(m*x3);

voc = -c/m

% Computing power delivered by the cell

p=0;

for i=1:size(x)
    if (x(i)>=0 & x(i)<=x3)
        p = p+y(i)*(x(i+1)-x(i));
    end
end

p

% Computing fill factor

ff = p/(jsc * voc)
```

Vita

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