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SYNTHESIS AND CHARACTERIZATION OF P-TYPE COPPER INDIUM DISELENIDE (CIS) NANOWIRES EMBEDDED IN POROUS ALUMINA TEMPLATES

Sri Harsha Moturu

University of Kentucky, harsha.moturu@uky.edu

ABSTRACT OF THESIS

Synthesis and Characterization of P-type Copper Indium Diselenide (CIS) Nanowires embedded in Porous Alumina templates

This work focuses on a simple template assisted approach for fabricating I-III-VI semiconductor nanowire arrays. Vertically aligned nanowires of p-CIS of controllable diameter and thickness are electrodeposited, from an acidic electrolyte solution, inside porous aluminum templates using a three electrode set up with saturated calomel electrode as the reference. AAO template over ITO-glass was used as starting template for the device fabrication. The deposited CIS is annealed at different temperatures in a reducing environment (95% Ar+ 5% H_2) for 30 minutes. X-ray diffraction of the nanowires showed nanocrystalline cubic phase structures with a strong orientation in the <112> direction. The effective bandgap of the deposited CIS nanowires determined using the Near Infrared (NIR) Spectrometer was found to be 1.07eV. The type of CIS electrodeposited inside the porous alumina template is determined to be p-type from the Schottky diode obtained with ITO-CIS-Au structure. Schottky diodes were characterized and analyzed at room temperature.

KEYWORDS: Schottky diode, Copper Indium Diselenide (CIS), Nanowires, Anodic Aluminum Oxide (AAO), Electrodeposition.

Sri Harsha Moturu

March 4th 2011

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By

Sri Harsha Moturu

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(Dr. Vijay P Singh)

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(Dr. Stephen Gedney)

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(Date)

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SYNTHESIS AND CHARACTERIZATION OF P-TYPE COPPER INDIUM DISELENIDE (CIS) NANOWIRES EMBEDDED IN POROUS ALUMINA TEMPLATES

THESIS

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical & Computer Engineering in the College of Engineering at the University of Kentucky

By

Sri Harsha Moturu
Lexington, Kentucky
Director: Dr. Vijay P. Singh, Professor
Electrical and Computer Engineering
Lexington, Kentucky
2011

DEDICATION

To Parents, sister and all my family members

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1. Introduction:

For the past fifty years the hope that one could make electricity from the sun, which on a bright, sunny day yields nearly 1000W of energy per sq.mt of the earth's surface, lingered around. The Photovoltaic effect was discovered by Edmund Becquerel in 1839 and the first solar cell with enough efficiency for commercial applications was a diffused silicon p-n junction, developed by Bell Labs researchers Chapin, Fuller, and Pearson in 1954 [1]. The continued improvements in the research area will make the solar energy economically viable. The imminent exhaustion of fossil fuels on the planet combined with the spiraling cost of conventional fuels led many to think solar cells are the future.

1.1 Thin film based Solar cells:

Thin-film solar cell manufacturers begin building their solar cells by depositing several layers of a light-absorbing material, a semiconductor, onto a substrate -- coated glass, metal or plastic. The materials used as semiconductors don't have to be thick because they absorb energy from the sun very efficiently. As a result, thin film solar cells with their low cost, wide range of applications, durability and high efficiencies provide a number of benefits in converting solar energy to electricity. Promising advances in non-silicon thin-film PV technologies are beginning to overcome the issues associated with amorphous silicon.

In order to reduce the cost of manufacturing solar cells based on silicon wafers, researchers have moved from crystalline silicon to p-n junction solar cells to thin film hetero junction based solar cells. The advantages of hetero-junction solar cells over

conventional p-n junction solar cells include: Enhanced short-wavelength spectral response because most photons are absorbed inside the depletion region of the second semiconductor, thus surface recombination of high-energy photon generated electron hole pairs is greatly decreased; lower series resistance because the first semiconductor can be heavily doped without causing the lifetime of minority carriers short; high radiation tolerance. CIGS and CdTe based hetero junction solar cells are the most promising among non-silicon based solar cells. There are a lot of similarities in both of these solar cells. These two materials are the absorber layers in the two respective cells. Both CIGS and CdTe cells use a transparent conducting oxide for one of the conducting layers, and both use cadmium sulfide (CdS) as the high band gap window layer.

1.1.1 CIS Based Solar Cells:

Copper Indium Diselenide (CIS) with a high efficiency of 19% [3] at present is one thin film material with a high scope of improvements. CIS thin films with a bandgap of 1.05eV has a very high absorption coefficient ($>10^5 cm^{-1}$) [4] and a large minority carrier diffusion length suitable for photovoltaic applications, which makes it a very popular thin film material. CIS can be deposited by a number of techniques such as: atmospheric pressure chemical vapor deposition, electrodeposition, closed space vapor transport, co-evaporation from elemental sources, selenization, evaporation from compound sources, sputtering and spray pyrolysis [5]. The method of deposition chosen in this research is the electrochemical deposition because of its large scale production, simple nature and the absence of vacuum making it a highly cost efficient method. A CdS/CIS solar cell can be viewed as n-π-p device with one or more bulk trap levels in the layer and interface states at the CIS-CdS heterojunction [13]. These traps and interface

states cause a drop in open circuit voltage. Such traps, interface states can be reduced if we have better lattice matching [6]. Stoichiometry plays a major role in developing CIS thin films where by a slight change in potential is enough to change the semiconducting material from p to n-type as the Cu to In ratio varies. These compositions must be potentiostatically controlled since a small change in stoichiometry results in a huge difference in the carrier density due to intrinsic defects [7].

1.1.2 Nanostructured Solar cells:

Nanostructured based solar cell layers in thin film solar cells offer three significant advantages,

(i) Varying the size of nanowires (quantum confinement) by modifying the desired design value, the energy band gap of several layers is kept constant.

(ii) The effective optical path for absorption is much larger than the actual film thickness due to the presence of scattering.

(iii) The recombination losses are greatly reduced by light generated electrons and holes, which transport over a very short path.

To fabricate large periodic arrays of semiconductor nanostructures that will allow, viz. (i) Flexible usage of various substrate materials, (ii) Compatibility with standard fabrication techniques, (iii) Variation of both size and composition, requires large scale production that has very high stability, device designs, which can attain high efficiency, the ability to produce effective results in large areas, both uniform and self-ordered films. In the above mentioned context of nanostructured solar cells, these fabrication issues are subjugated. Another major aspect of improving solar cell efficiency is by improving the charge

transport of free carriers and the concept of light harvesting is overcome by the properties of nanostructured solar cells [8] [9].

1.2 Goals and Objectives:

Goal of our research is the continued investigation of nanostructured device designs for improving the performance of CdS-CIS solar cells. In the past, CIS nanowires were fabricated inside the pores of anodized aluminum oxide (AAO) in our group by Phok et al [20] and by Liang Shi et al [11] at the University of Science and Technology, Hefei, China. Another technique used in the past to synthesize CIS nanowires consisted of vapor liquid solution (VLS) growth using gold (Au) catalyst [12].

In the past work on CIS nanowires, substrate material has been aluminum because freestanding AAO membranes were used for electro depositing CIS nanowires. On the other hand, research work in this thesis has focused on using indium tin oxide (ITO) substrate instead of aluminum. Advantage of ITO over aluminum is that ITO is a transparent conductor and therefore allows for more flexibility in choosing an appropriate device design for the solar cell. To our knowledge, this is the first time that CIS nanowires have been formed on an ITO substrate. Objectives of our research include,

1. Fabrication of CIS nanowires on ITO substrates.
2. Material characterization of above films by SEM, XRD and Spectral Absorption.
3. Formation of ohmic and Schottky diode contacts to CIS nanowires.
4. Analysis of above Schottky diodes.

This work advances the understanding of CIS nanowire growth processes and film characteristics and thus lays groundwork for the development of CIS based solar cells of more than 20% power conversion efficiency. Chapter two describes the basic theory behind Metal-Semiconductor junctions and their characteristics. The third chapter discusses the experimental details of the CIS-Al and CIS-Au device fabrication and the forth chapter describes the results and discusses the observations made. The last chapter summarizes the thesis with the conclusions drawn and presents suggestions for future research work.

2. Theory:

2.1 Metal Semiconductor Junction:

Metal-semiconductor junction is a type of junction in which a metal comes in close contact with a semiconductor material. Similar to a p-n junction, it has rectifying properties. Although our knowledge of Metal-Semiconductor contacts can be traced as far back as early work by Braun (1874), it was not until 1938 that both Schottky and Mott independently suggested a model for the rectification mechanism [14]. They pointed out that the observed direction of rectification could be explained by supposing that electrons passed over a potential barrier through the normal process of drift and diffusion.

A metal-semiconductor is a junction formed by the intimate contact of a metal and a semiconductor having non equal work functions. These can be classified as ohmic or rectifying, depending on the relative work function difference between the metal and semiconductor and type of the semiconductor used (p-type or n-type). An ohmic contact is like a typical resistor thus providing a means to connect the semiconductor directly to the outside world with some loss due to the resistance where rectifying contact exhibits diode behavior with a turn-on voltage and diode ideality factor. The only fundamental difference between a metal-semiconductor Schottky diode to that of a conventional p-n junction diode is that the majority carriers in the semiconductor dominate the current incase of metal-semiconductor junction. It can be viewed as a one sided abrupt (e.g., p+ - n) junction.

In a material, the work function is defined as the energy difference between the vacuum level and the Fermi level and is denoted by $q\Phi_m$ or (Φ volts) for a metal and is equal to q

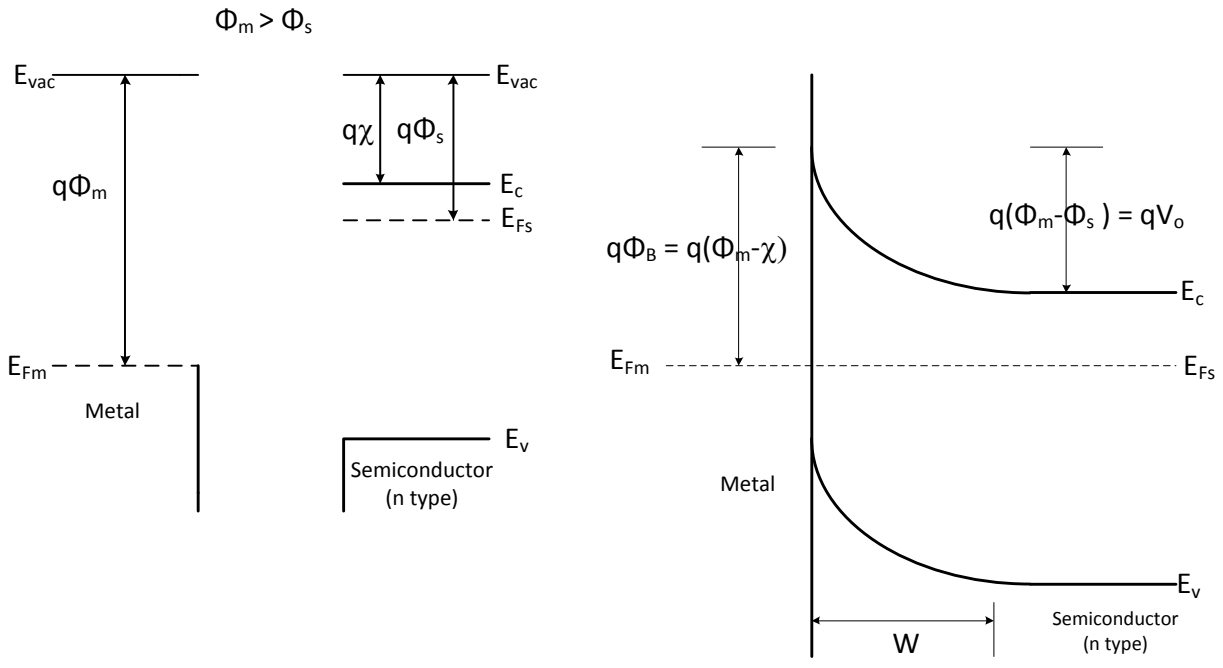
(χ+ Vn) or $q\Phi_s$ for a semiconductor where $q\chi$ is the electron affinity measured from the bottom of the conduction band E_c to vacuum level, and qV_n is the energy difference between E_c and the Fermi level. In a metal semiconductor junction the charge will flow from the semiconductor to the metal and thermal equilibrium is established.

The current flow across the metal-semiconductor contacts can take five paths [15] [16]. These are: (i) quantum-mechanical tunneling current through the barrier, the dominant process for contact with a heavily doped semiconductor, (ii) thermionic emission current from the semiconductor over the potential barrier into the metal, the dominant process for Schottky diodes with moderately doped semiconductor operated at a moderate temperature like 300K, (iii) injection current from the metal to the semiconductor, (iv) recombination current in the space-charge region and (v) recombination current via interface states.

2.1.1 Schottky Contacts:

A Schottky contact refers to the contact between a metal and a semiconductor that hinders the flow of carriers in and out of the semiconductor. When negative charges (electrons) are brought near the metal surface, positive charges are induced in the metal. When the applied electric field is coupled with the force induced to carry an electron into vaccum, the effective work function is somewhat reduced. Such lowering of the barrier is referred to as Schottky effect and the rectifying contacts are referred to as Schottky barrier diodes. The largest differences between a Schottky barrier and a regular p–n junction diode are its typically lower junction voltage, and decreased (almost nonexistent) depletion width in the metal.

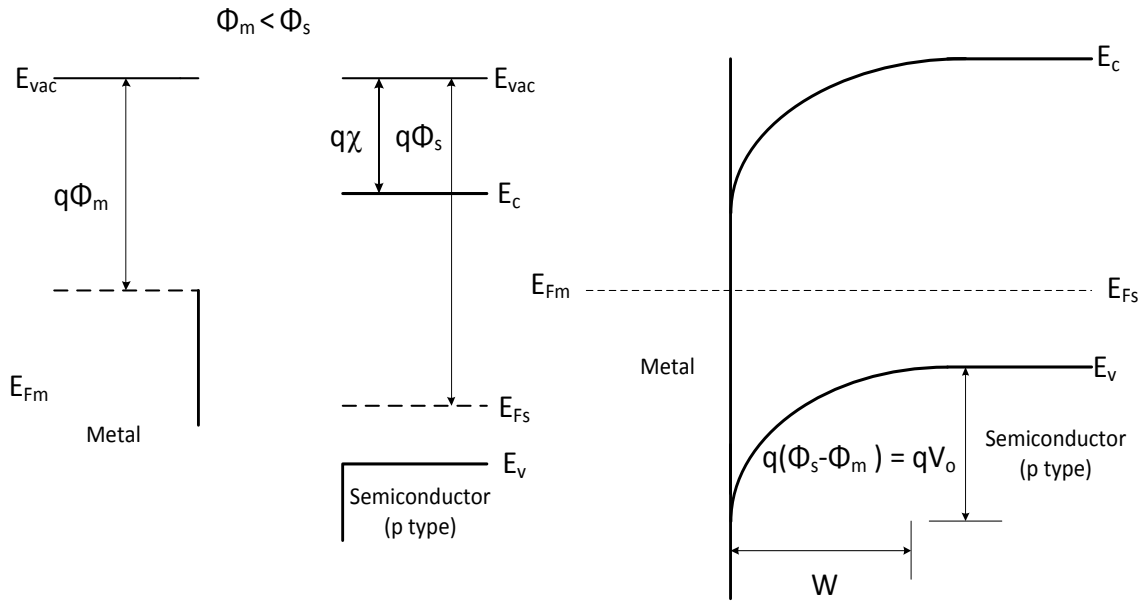
When $\Phi_m > \Phi_s$, the n-type semiconductor Fermi level is initially higher than that of the metal before contact is made as shown in the figure below. The Fermi levels on both sides line up and relative to the Fermi level in the metal, the Fermi level in the semiconductor is lowered by an amount equal to the difference between the two work functions. In order to align the Fermi levels, the electrostatic potential of the semiconductor must be raised relative to that of metal. In the Figure 1, after a contact has been made, a depletion region W is formed near the junction on the n-type semiconductor side. The positive charge on the n type side due to uncompensated donor ions within W equals the net negative charge accumulated on the metal.



(a) (b)

Figure 1: A Schottky barrier between a metal and a n-type semiconductor with $\Phi_m > \Phi_s$; (a) band diagrams before joining; (b) equilibrium band diagram for the junction

At equilibrium, a contact potential of V_o is formed at the junction. This potential prevents further electron diffusion from the semiconductor conduction band into the metal. The contact potential is given by the difference in the work function potentials $\Phi_m - \Phi_s$. The potential barrier height, Φ_B, for electron injection from the metal into the semiconductor conduction band is $\Phi_m - \chi$, where $q\chi$ is the electron affinity measured from the vacuum level to the semiconductor conduction band edge. By applying either forward or reverse-bias voltage, the equilibrium potential difference V_o can be decreased or increased as in the p-n junction.



(a) (b)

Figure 2: A Schottky barrier between a metal and a p-type semiconductor with $\Phi_m < \Phi_s$; (a) band diagrams before joining; (b) equilibrium band diagram for the junction

Figure 2 describes the energy band diagram for a Schottky barrier on a metal - p-type semiconductor with $\Phi_m < \Phi_s$. In this case the fermi level of the metal is higher than that

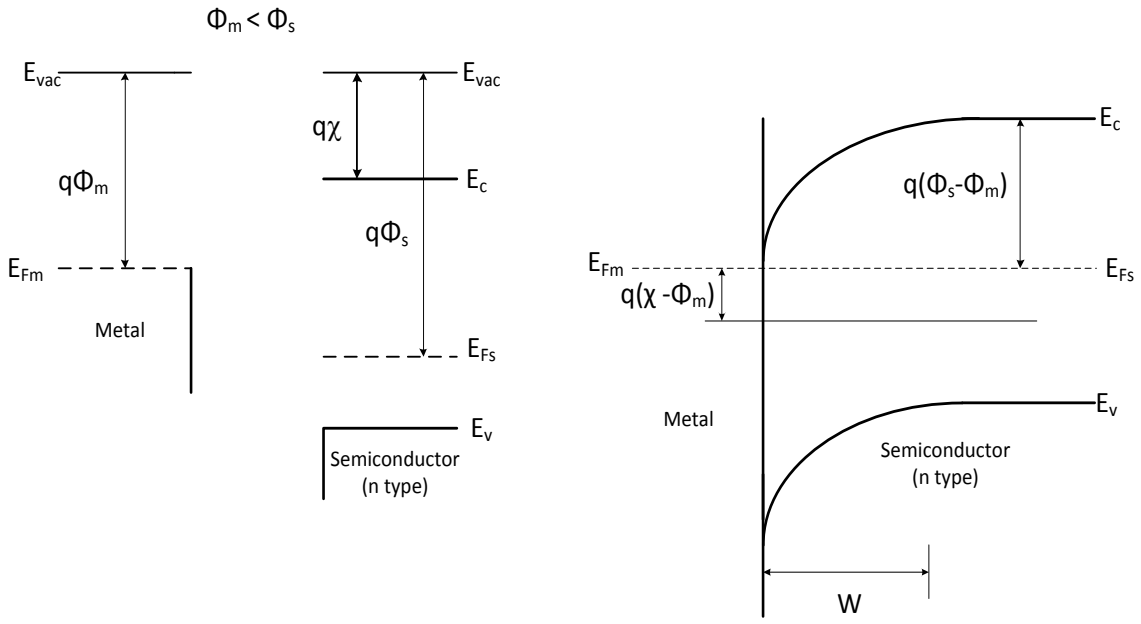
of p-type semiconductor before the contact has been made. Aligning fermi levels at equilibrium requires a positive charge on the metal side and a negative charge on the p-type semiconductor side of the junction. In the p-type semiconductor of the above figure, a depletion width of W is formed near the junction after the contact has been made. The negative charge due to ionized acceptors within W matches the positive charge on the metal. The potential barrier V_o prevents further hole diffusion from the semiconductor into the metal and is equal to the difference in the work function of the semiconductor and metal (Φ_s - Φ_m). The potential can be raised or lowered by applying voltage across the junction just like in the metal - n type semiconductor junction.

2.1.2 Ohmic Contact:

An ohmic contact refers to the contact between a metal and a semiconductor to allow carriers to flow in and out of the semiconductor. An ideal ohmic contact must be capable of delivering the required current with no voltage drop between the semiconductor and the metal. In reality, an ohmic contact must have a contact resistance as low as possible and should be negligible when compared to the bulk resistance of the semiconductor.

Metal-semiconductor contacts are said to be ohmic when the charge induced in the semiconductor in aligning the fermi levels is provided by the majority carriers. For example in the case of metal - n type semiconductor junction, the fermi levels are aligned at equilibrium by transferring electrons from the metal to the semiconductor. This transferring of electrons raises the electron energy levels in the n type semiconductor relative to the metal at equilibrium. With $\Phi_m < \Phi_s$, the barrier to the electron flow

between the metal and the semiconductor is very small and easily overcome by a small voltage. Thus the junction effectively acts as a linear resistor. Conversely for a p type semiconductor, $\Phi_m > \Phi_s$ results in easy hole flow across the junction. Energy band diagram of such a junction is illustrated in the figure 3 and 4.



(a) (b)

Figure 3: An Ohmic contact between a metal and an n-type semiconductor with $\Phi_m < \Phi_s$; (a) band diagrams before joining; (b) equilibrium band diagram for the junction

In most practical ohmic contacts the metal layers usually contain a suitable dopant species - donor or acceptor atoms. A heat treatment is used to drive the dopant into the semiconductor to form an n++ or p++ layer thus creating a tunneling metal-

semiconductor junction required for enhanced ohmic behavior. The quality of an ohmic contact is ultimately assessed by determining its specific contact series resistance.

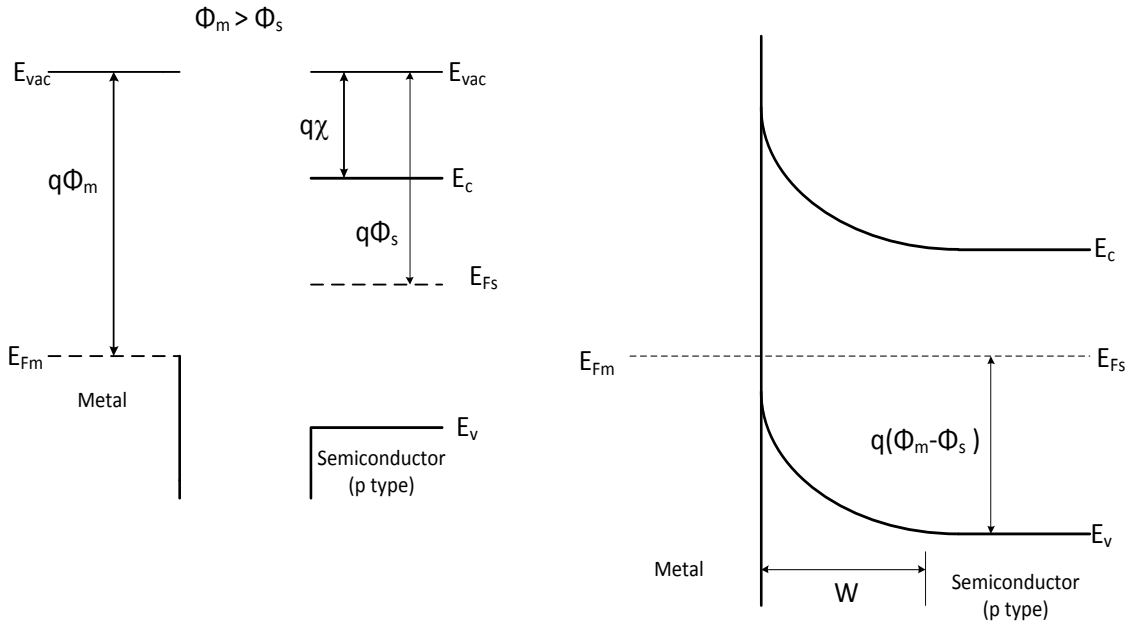


Figure 4: An Ohmic contact between a metal and a p-type semiconductor with $\Phi_m > \Phi_s$; (a) band diagrams before joining; (b) equilibrium band diagram for the junction

2.2 Schottky Diode Characteristics:

Schottky contact or rectifying contact behaves the same way as a p-n junction diode. I-V characteristics of a metal-semiconductor junction are similar to that of p-n junction diode. Thus the diode equation should hold good for I-V characteristics of metal semiconductor Schottky junction.

The diode equation is given by

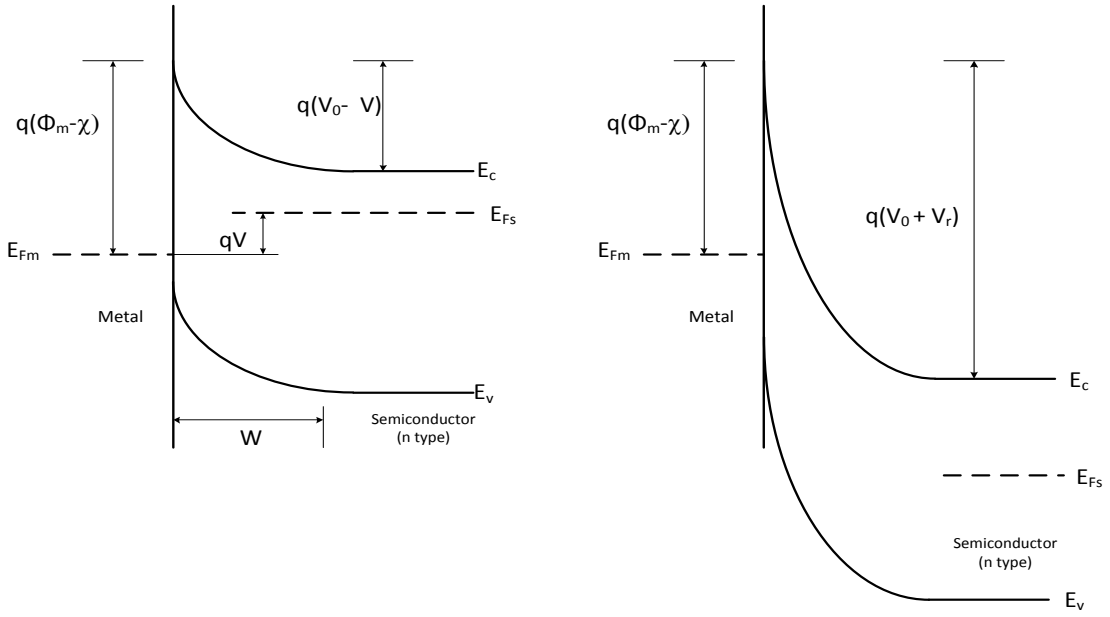
$$\boldsymbol{I = I_0\,(e^{\frac{qV}{kT}} - 1)}$$

where *Io* is the reverse saturation current, q is the charge of an electron, *V* is the applied voltage, *k* is the Boltzmann's constant and *T* is the temperature.

The reverse saturation current, *Io*, is given by

$$\boldsymbol{I_0 = ABT^2(e^{-\frac{q\phi B}{kT}})}$$

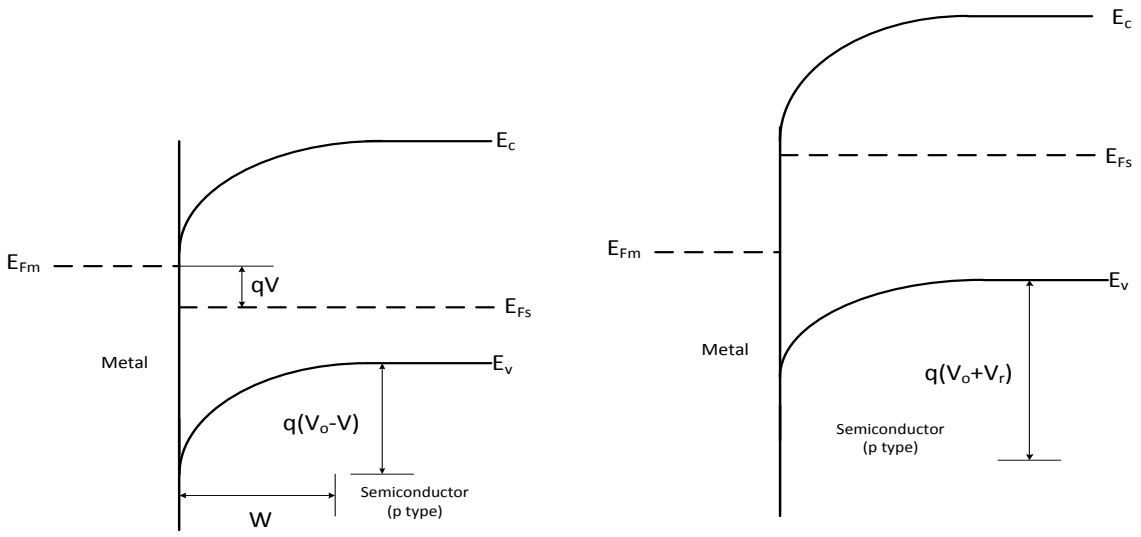
where B is effective Richardson constant.



(a) (b)

Figure 5: Biasing a Schottky barrier in an n-type Schottky diode; (a) Forward bias, (b) Reverse bias

When a forward-bias voltage V is applied to the Schottky barrier of Figure 1, the contact potential is reduced from V_o to V_o-V as shown in Figure 5. As a result, electrons in the semiconductor conduction band can diffuse across the depletion region into the metal thus increasing the forward current through the junction. Conversely on applying a reverse bias voltage V_r, the contact potential increases from V_o to V_o+V_r, and electron flow from semiconductor to metal becomes negligible. Here, the forward current is due to the injection of majority carriers from the semiconductor into the metal. The absence of minority carrier injection and the associated storage delay time is an important feature of Schottky barrier diodes. Their high-frequency properties and switching speed are therefore generally better than typical p-n junctions.



(a) (b)

Figure 6: Biasing a Schottky barrier in a p-type Schottky diode; (a) Forward bias, (b) Reverse bias

[*Note: Most of the theory in section 2.1 and 2.2 has been taken from reference 17 and 18*]

2.3 Device Structure:

The device structure that was performed is as shown in the figure below.

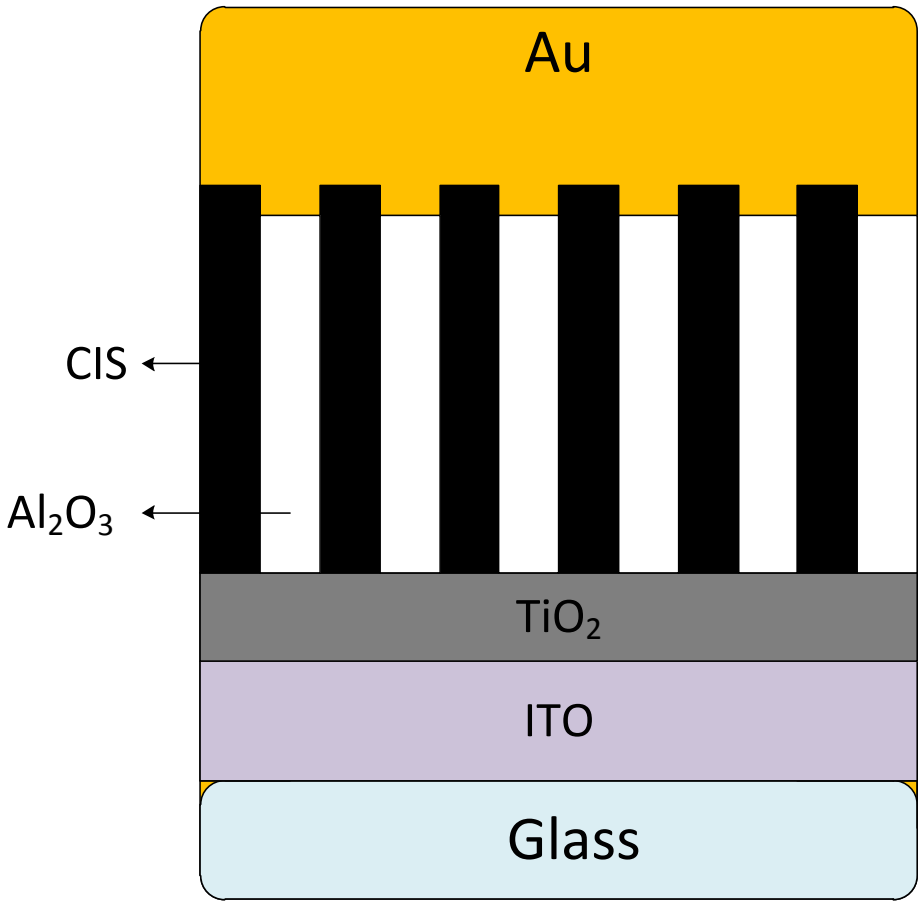


Figure 7: Cross section of CIS nanowires based Schottky diode with Au on top as contact (ohmic) and ITO as Schottky contact to CIS wire at the bottom

Here Gold (Au) and Indium Tin Oxide (ITO) act as cathode and anode respectively. Copper Indium Diselenide (CIS) nanowires (1.5µm) stand on top of the ITO substrate, with a thin layer (5 nm -10 nm) of TiO_2 in between. Alumina (Al_2O_3) acts as a wall separating nanowires from each other.

3. Experimental Procedure:

The device was fabricated first by preparing the template used by preparing anodized aluminum oxide (AAO) over ITO-glass followed by electro deposition of CIS using three electrode process and finally evaporating aluminum and gold as top contact to verify that the CIS deposited was of p-type.

3.1 Fabrication of AAO on ITO substrates:

Glass substrates pre-coated with 150 nm thick conductive, transparent ITO anode were purchased and cut to the following dimensions of 1" x 0.5" in size with a sheet resistance of about 4-8 ohms/square. These substrates are first sonicated using an ultrasonic bath in acetone for 2 minutes in ultrasonictor model 50HT of VWR and then rinsed with isopropyl alcohol (IPA) followed by DI water. A thin layer of Titanium (Ti) of about 5nm is sputtered to aid in the adhesion of Aluminum (Al) on ITO. Aluminum is then vacuum evaporated using Torr International E-Beam Evaporation at a low chamber pressure of ~5.0E-6 with a thickness varying from 1μm to 1.5μm. The obtained samples were subject to a one step anodization processes at 50V to obtain highly ordered alumina pores.

3.2 Anodization:

The procedure for fabricating anodized aluminum oxide typically consists of an electro chemical cell with the aluminum substrate as anode, platinum plate (1" x 1") as cathode and a magnetic stirrer. The cell is placed on a stirring instrument and the solution is constantly stirred during anodization. Stirring the electro chemical solution is a critical step in obtaining ordered pore arrays. The rate of rotation was approximately 45-60 rpm.

The temperature of the electrolyte is maintained at 5° C. The aluminum substrate and platinum plate are then placed into the reaction cell, with alligator clips securing them. The clips themselves are placed a few millimeters above the surface of the electrochemical solution. The electro chemical solution used is 0.3 M oxalic acid ($C_2H_2O_4$). In this case potentiostatic anodization is used to produce optimum results.

During anodization, the potential was set to 50V and maximum current to 1A, cathode was given to platinum plate and anode was given to the substrate. As the rate of potentio-static alumina formation decreases (due to less aluminum) the current decreases until it reaches a lower peak value. Anodization was carried out till the current reaches a constant low value of about 1mA. At this point most of the aluminum is anodized and the current rises rapidly suggesting that it is contact with the TiO_2 layer. However the electrolyte should be a very strong acid if it were to anodize the TiO_2.

The anodized substrate is then rinsed with DI water and dried in Nitrogen. Without any aluminum the substrate looks transparent with a very slight hue. The AAO layer also grows with a small layer of oxide at the interface of the Al and Al_2O_3.

3.3 Etching:

As discussed above after anodization an oxide layer at the interface of Al and Al_2O_3 is formed, which acts as a barrier layer at the bottom, hindering the growth of CIS nanowires. This barrier layer is dissolved away by dipping the substrate in 5% phosphoric acid (H_3PO_4) for 50-60 minutes leaving the pores open on each side. The substrate is then again rinsed with DI water and dried in Nitrogen.

After the wet etching process, any remaining excessive barrier layers are removed by Reactive Ion etching (RIE). Reactive ion etching (RIE) is an etching technology, which uses chemically reactive plasma to remove material deposited on the substrate. The plasma is generated under low pressure (vacuum) by an electromagnetic field. High-energy ions from the plasma bombard the surface of the sample and react with it. The plasma generated helps in removing the Al_2O_3 present at the bottom of pores. After RIE, the sample is dipped in 5% H_3PO_4 to completely remove the oxide layers in the substrate thus making it free of any existing barrier layers. Though the etching might seem a small process, it is a very crucial step in fabricating an ideal solar cell of high efficiencies [19].

3.4 Fabrication of p-CIS Nanowires:

CIS nanowires are electro deposited by using a three-electrode deposition as shown in Figure 8 in which a 1”x1” platinum electrode was used as the counter electrode. AAO substrate serves as the working electrode and Saturated Calomel Electrode acts as the reference electrode. The electrolytic solution consists of 1.5 mM Copper sulfate hydrate, 2mM Indium sulfate hydrate, 3.5mM Seleneous acid, Lithium chloride and Potassium hydrogen phthalate [20] [21]. After the solids are completely dissolved, the solution is then added to a standard beaker of 200 ml. The solution is thoroughly stirred till all the solids are completely dissolved and the pH of the solution is adjusted to 2.8 by adding a few drops of dilute HCl to the electrolyte. Electrodeposition of p-CIS and n-CIS was carried out at 800 mV and 2.5V respectively against the reference electrode. The temperature of the electrolyte was maintained at room temperature during the whole process of electro deposition.

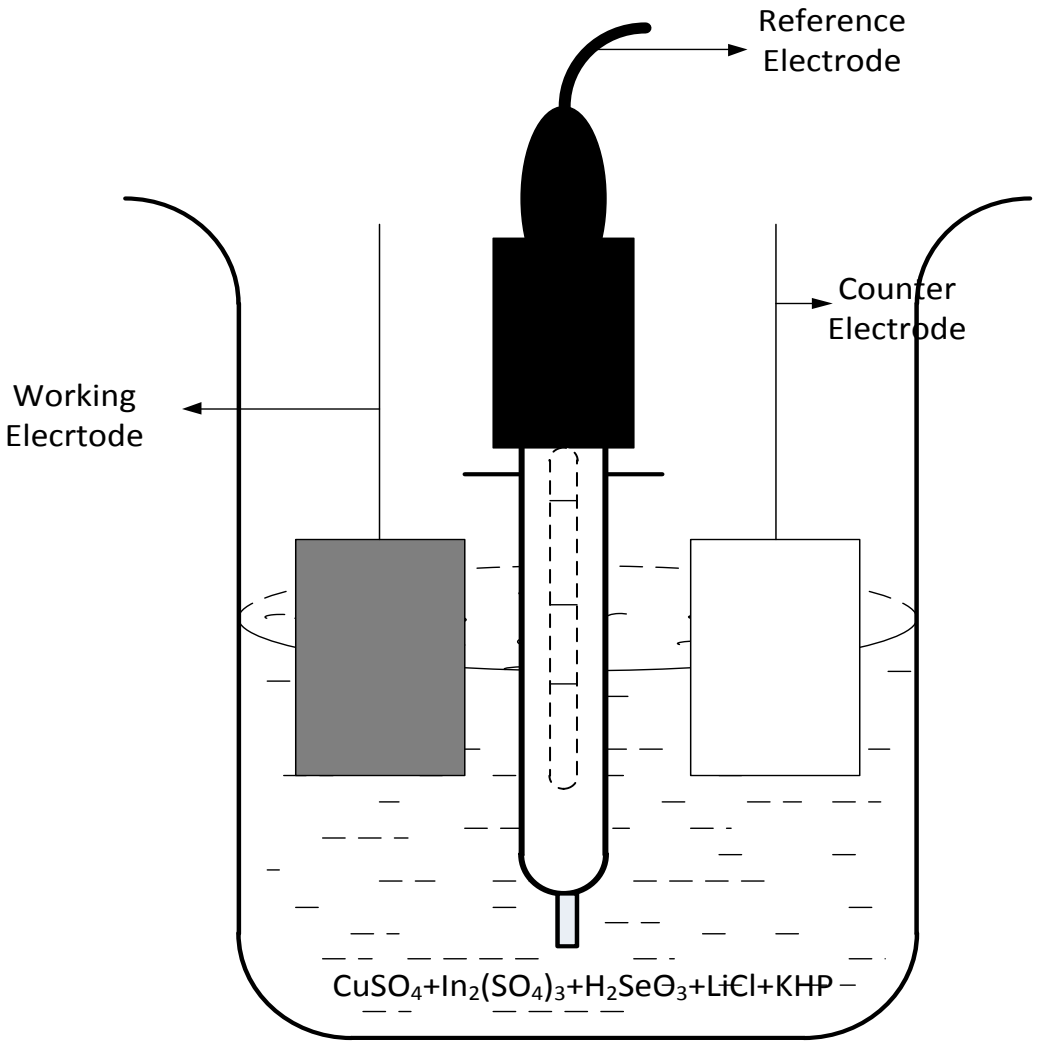


Figure 8: Electrodeposition setup for three Electrode process

The deposited CIS nanowires are annealed in a reducing environment (95% Ar + 5% H_2) for 30 minutes at 250°C and 350°C to increase the crystallinity of nanowires.

3.5 E-beam evaporation of Gold and Aluminum for contacts:

For depositing Au and Al as contacts on the samples, a Torr International E-Beam evaporator was used. The substrate was first masked with Al foil in the form of dots of

crossectional area of 0.07cm^2. The masked substrates are placed inside a vacuum chamber, in which a source of the material to be deposited is placed in a graphite crucible. The density, Z factor, tooling and sense average are set to the respective values of the material used for deposition. An electron beam (E-beam) is aimed at the source material causing local heating. The source material is heated to the point that it liquefies, starts to boil and evaporates. The vacuum is essential to allow the atoms to evaporate freely in the chamber, and subsequently condense on all surfaces.

3.6 Material Characterization:

Characterization of a device is a very essential process in determining the characteristics of the material deposited and a crucial step. Material characterizations of the CIS nanowires are performed with the techniques of X-ray Diffraction (Bruker-AXS D8 DISCOVER Diffractometer), optical absorption spectroscopy (Cary-50 v3.0 UV-Visual Spectrophotometer), near IR (infrared) spectroscopy and scanning electron microscopy (Hitachi S-900 field emission SEM).

3.6.1 Scanning Electron Microscopy:

A scanning electron microscope (SEM) is a type of electron microscope that images a sample by scanning it with a high-energy beam of electrons in a horizontal scan pattern. The electrons interact with the atoms that make up the sample producing signals that contain both qualitative and quantitative information of the sample being studied. A Hitachi FESEM (Model S-900) with a maximum magnification power of 800kX at an accelerating potential of 3kV was used for characterization purposes for this thesis work.

For the SEM analysis, a small section of the CIS template was cut and placed on a copper stub with a double sided carbon tape as the backing. A thin layer of gold-palladium alloy was then sputtered on to this sample to increase the conductivity of the sample. This step helps in obtaining good quality SEM micrographs. SEM technique was used to confirm the diameter and length of the CIS nanowires in AAO matrix on the ITO substrate.

3.6.2 X-ray Diffraction:

X-ray scattering techniques are a family of non-destructive analytical techniques which reveal information about the crystallographic structure, chemical composition, and physical properties of materials and thin films. With a diffraction pattern an investigator can identify an unknown mineral or characterize the atomic-scale structure of an already identified mineral. There exists systematic X-ray diffraction data for thousands of mineral species. Much of these data are gathered together and published by the International Centre for Diffraction Data. When certain geometric requirements are met, X-rays scattered from a crystalline solid can constructively interfere, producing a diffracted beam. The principle behind X-ray diffraction is Bragg's law ($\lambda=2d\sin\theta$) [22]. These techniques are based on observing the scattered intensity of an X-ray beam hitting a sample as a function of incident and scattered angle, polarization, and wavelength or energy. A Bruker-AXS D8 DISCOVER Diffractometer was used to obtain the X-ray diffraction spectra of all the samples fabricated.

An ITO substrate with deposited CIS nanowires is aligned vertically with respect to the X-ray source and the detector. After alignment, automated proprietary software was used to obtain the diffraction spectrum for 2θ angle ranging from 20° to 60° of angles of

incidence with a step scan of 2°. Patterns thus obtained were cross-referenced with the spectra in the reference database software for suitable match and identification of compounds present in the sample. XRD was also performed on the same piece of template to find out the preferential crystal orientation of the CIS nanowires.

3.6.3 Ultraviolet-Visual Absorption Spectroscopy:

A material's absorption spectrum is the fraction of incident radiation absorbed by the material over a range of frequencies. The absorption spectrum is primarily determined by the atomic and molecular composition of the material. Radiation is more likely to be absorbed at frequencies that match the energy difference between two quantum mechanical states of the molecules. The energy associated with the quantum mechanical change primarily determines the frequency of the absorption line but the frequency can be shifted by several types of interactions such as electric and magnetic fields and neighboring molecules. The energy associated with a given segment of the spectrum is proportional to its frequency and the energy carried by a photon of a given wavelength of radiation is given as $E=hv$ [23]. A Cary-50 v3.0 UV-Visual Spectrophotometer was used to obtain the absorption spectrum of the samples fabricated. UV-Vis spectroscopy was performed on a piece of AAO template filled with CIS nanowires. A bare AAO template on ITO substrate was used as a baseline for this measurement.

3.6.4 Near Infrared (NIR) Spectroscopy:

Near-infrared spectroscopy (NIRS) is a spectroscopic method that uses the near-infrared region of the electromagnetic spectrum (from about 800 nm to 2500 nm). Just as

in the UV-Vis range the absorption spectrum is dependent more on the atomic composition of the material and less on the molecular composition owing to quantum mechanics present in the substrate. As a result, the molar absorptivity in the near IR region is typically quite small. One advantage is that NIR can typically penetrate much farther into a sample than mid infrared radiation [24]. NIR spectroscopy was performed on the same piece of AAO template that was used in calculating the bandgap in the UV-Vis range.

3.6.5 J-V Characterization:

Current density-voltage (JV) measurements are the major accomplishment of any characterization procedure as they are one of the most established techniques in determining the type of semiconductor deposited on the substrate. The JV plots give us a rough graphical representation of how the currents are flowing as a function of applied potential in dark and as well as under illumination. They also give us valuable information regarding series resistance (R_s), shunt resistance (R_{sh}), diode ideality factor (η), diode saturation current (I_o), short circuit current (I_{sc}), open circuit voltage (V_{oc}), maximum power point (P_m), fill factor and conversion efficiency [25]. The equipment for measuring JV consisted of a Kepco programmable bipolar operational amplifier/power supply (Model BOP 36-12M) and two Keithley digital multimeters employed as voltmeters (Model 2001 and 2000) interfaced with a common lab PC using an application software developed in-house with LabVIEW Student Edition 7.0 provided by National Instruments. The supply voltages are varied from -2V to +2V in steps of 0.05V. Electrical characterization was performed on a template filled with CIS nanowires with Gold, Aluminum and Graphite contacts on the top surface.

4 Results and Discussion:

4.1 Electrodeposition of CIS inside AAO template over an ITO-glass:

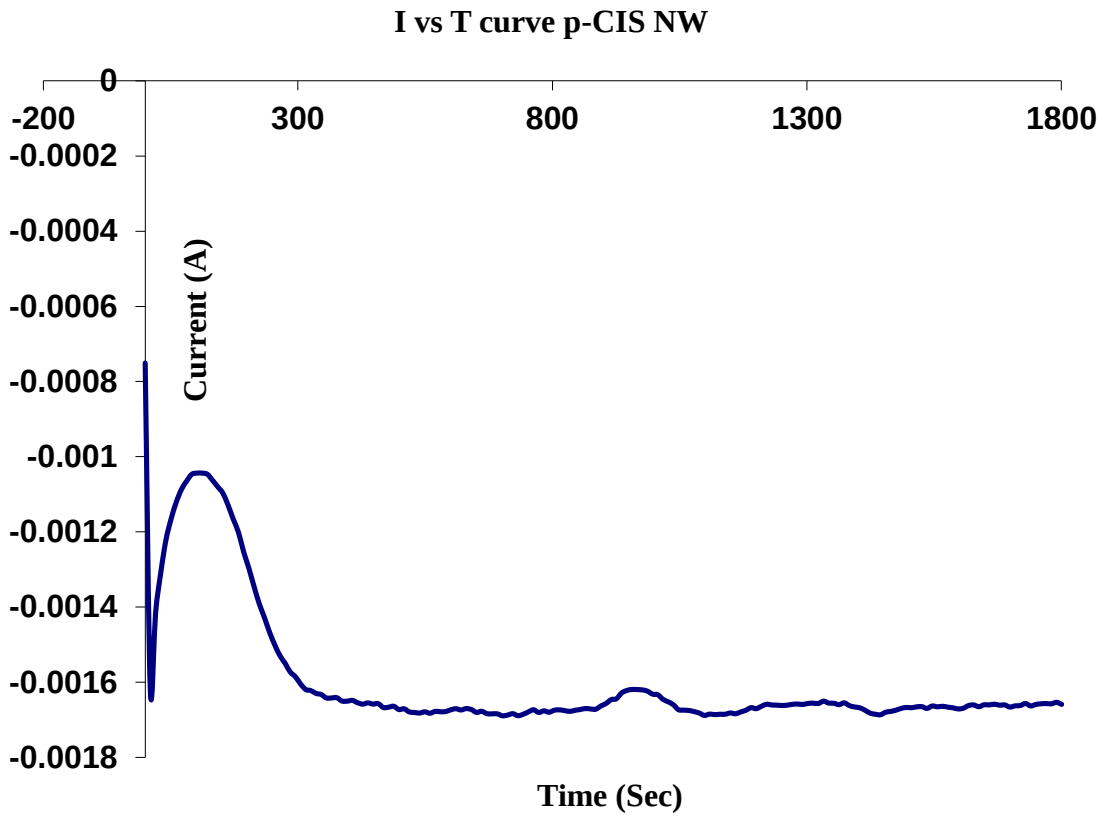


Figure 9: Current-Time plot against working electrode with respect to counter electrode during Electrodeposition of p-CIS Nanowires

The base templates with AAO pores were about 1.5μm long and 50-60nm in diameter. It was observed that at a higher potential greater than 1200 mV, indium rich compounds were formed, which results in the formation of n-CIS materials and at lower potentials less than 1200mV, copper rich compounds were formed, which results in the formation of p-CIS materials. N.B. Chaure et al. [7] reported an extensive study of the various reactions taking place with respect the deposition potential.

Figure 9 shows the current vs. time graph against the working electrode with respect to the counter electrode. We observe from the graph that the current suddenly hikes up when the time reaches 1200 seconds, this could be the result of pores being filled completely to the top surface.

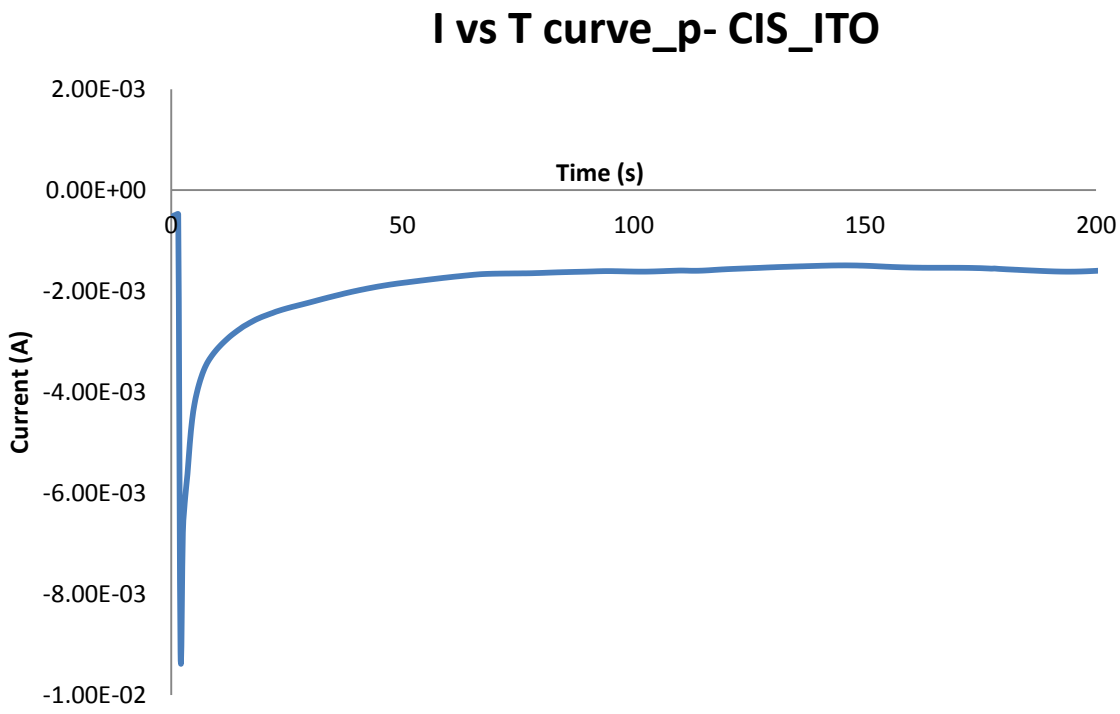


Figure 10: Current-Time plot against working electrode with respect to counter electrode during Electrodeposition of p-CIS on ITO

Figure 10 and 11 show the same current vs. time graph for p-CIS on a planar surface for a potential of 0.8V and n-CIS for a potential of 2.5V respectively. The rate of deposition is approximately 75nm/min. Bhattacharya et al [26] pioneered deposition of CIS on a thin film, which consists of three primary steps:

$$2Cu + Se + 4e^- \longrightarrow CuSe \quad (1)$$

$$3Se + 2In \longrightarrow In_2Se_3 \quad (2)$$

$$In_2Se_3 + Cu_2Se \longrightarrow CuInSe_2 \quad (3)$$

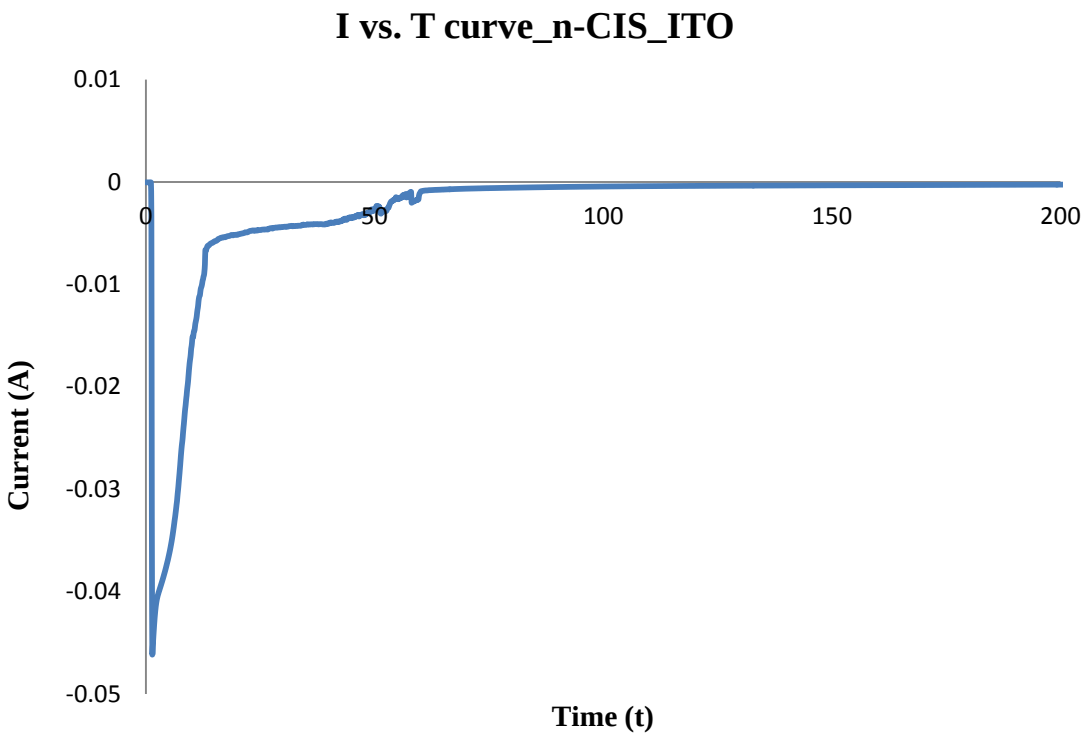


Figure 11: Current-Time plot against working electrode with respect to counter electrode during Electrodeposition of n-CIS on ITO

4.2 Characterization of CIS using Scanning Electron Microscope (SEM):

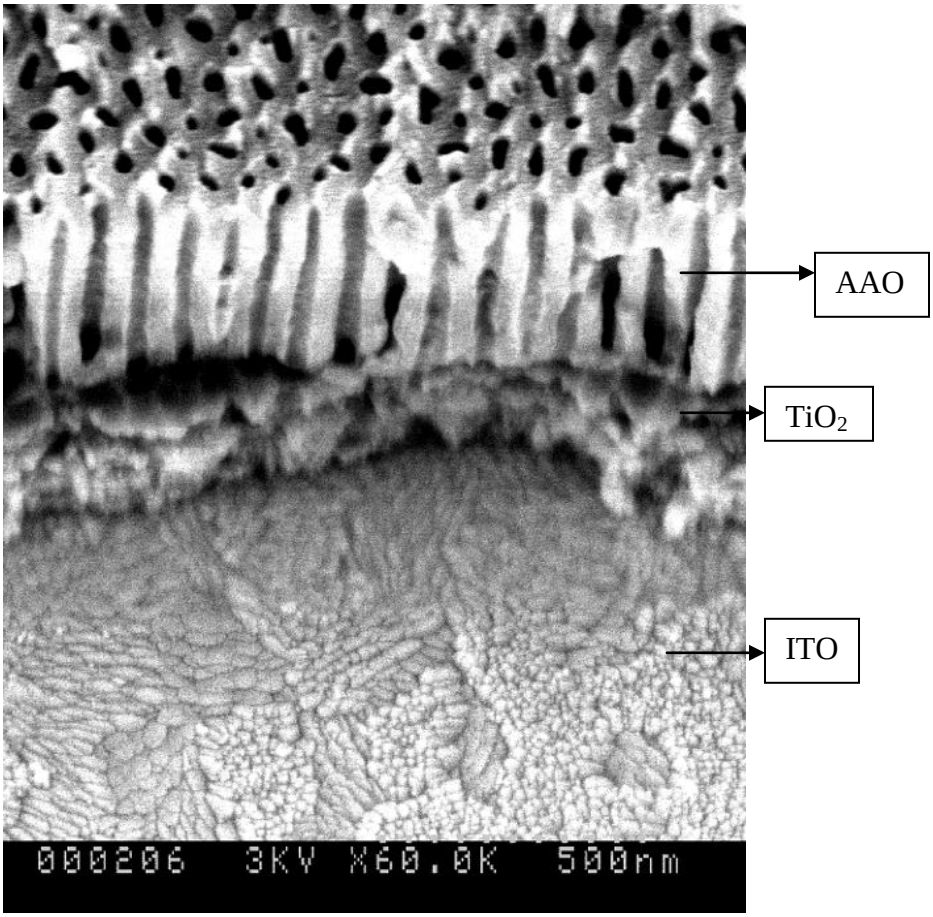
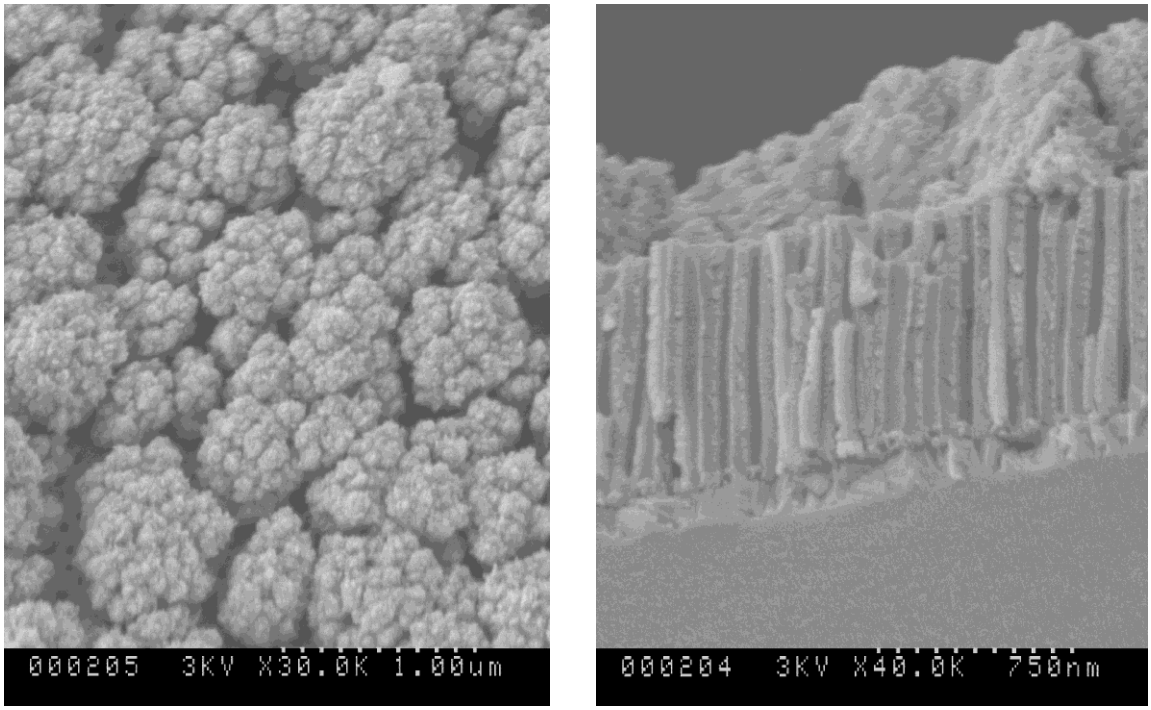


Figure 12: Cross section of an AAO template over ITO glass

Figure 12 gives a typical cross sectional view of an AAO template on an ITO glass. The template reveals layers of Glass, ITO and TiO2 along with AAO hexagonal pores of diameter 50-60nm range for a template anodized at 50V at room temperature standing on top. As we can see the pores are uniformly distributed.

Near stoichiometric CIS nanowires were formed at a potential of 800 mV across the reference voltage. This is applied across the working electrode (substrate) and reference electrode (Saturated Calomel Electrode).



(a) **(b)**

Figure 13: SEM Micrographs of CIS Nanowires (a) Top layer (bulk) (b) Cross-sectional view.

From Figure 13, one can observe the CIS nanowires grow from the bottom of the pore. Figure 13(a) depicts the amount of bulk CIS present at the top of the template. Figure 13(b) shows the partially filled nanowires on the AAO template. The unfilled portions of AAO pores seen in Figure 13(b) are thought to have lost their CIS nanowires due to the stress produced during the process of breaking the device and mounting it on the stub for electron microscopy.

4.3 X-Ray Diffraction (XRD) Characteristics:

XRD analyses were performed in the Bragg-Bretano geometry with two-theta angle ranging from 20° - 60° with a step scan of 2°.

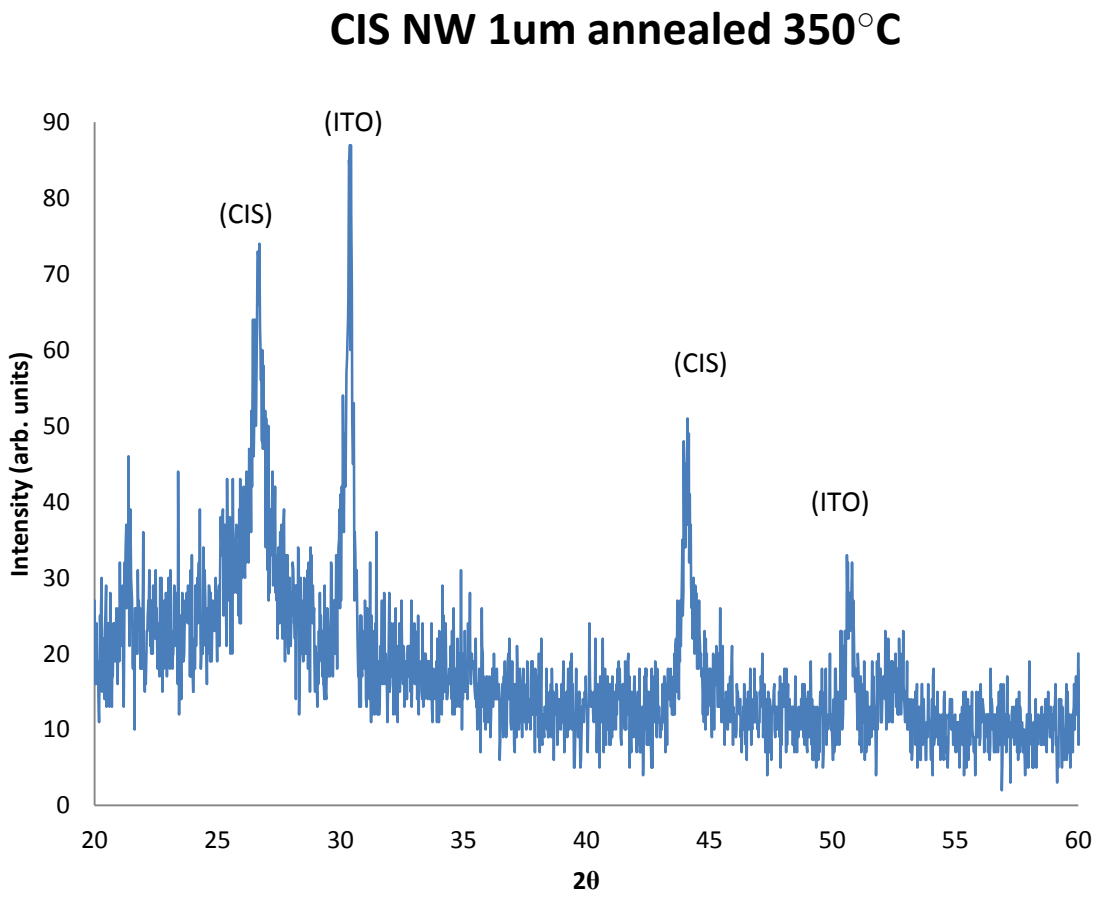


Figure 14: X-ray Diffraction pattern of electrodeposited CIS nanowires in AAO template on a glass-ITO substrate at 350°C

Figure 14 and 15 show the XRD patterns of CIS films after annealing at 350°C and 250°C for 30 minutes in an inert atmosphere, respectively. From the XRD pattern of the

embedded CIS nanowires we infer having a strong diffraction peak at 2θ = 26.6° and 44.2°, which corresponds to diffraction from <112> and <220> planes respectively [27].

As shown in figure 14 we observe that CIS when annealed at 350°C has a preferential growth of higher intensity at 26.6° in <112> direction when compared to that annealed at 250°C, which has higher intensity at 44.2°. This clearly indicates that annealing, when done at the optimum temperature of 350°C helps improve the crystalline nature of the CIS nanowires and their preferential growth in <112> direction at 26.6°. Similarly, both the figures also show reflection of ITO peaks at 30.3° and 50.7°.

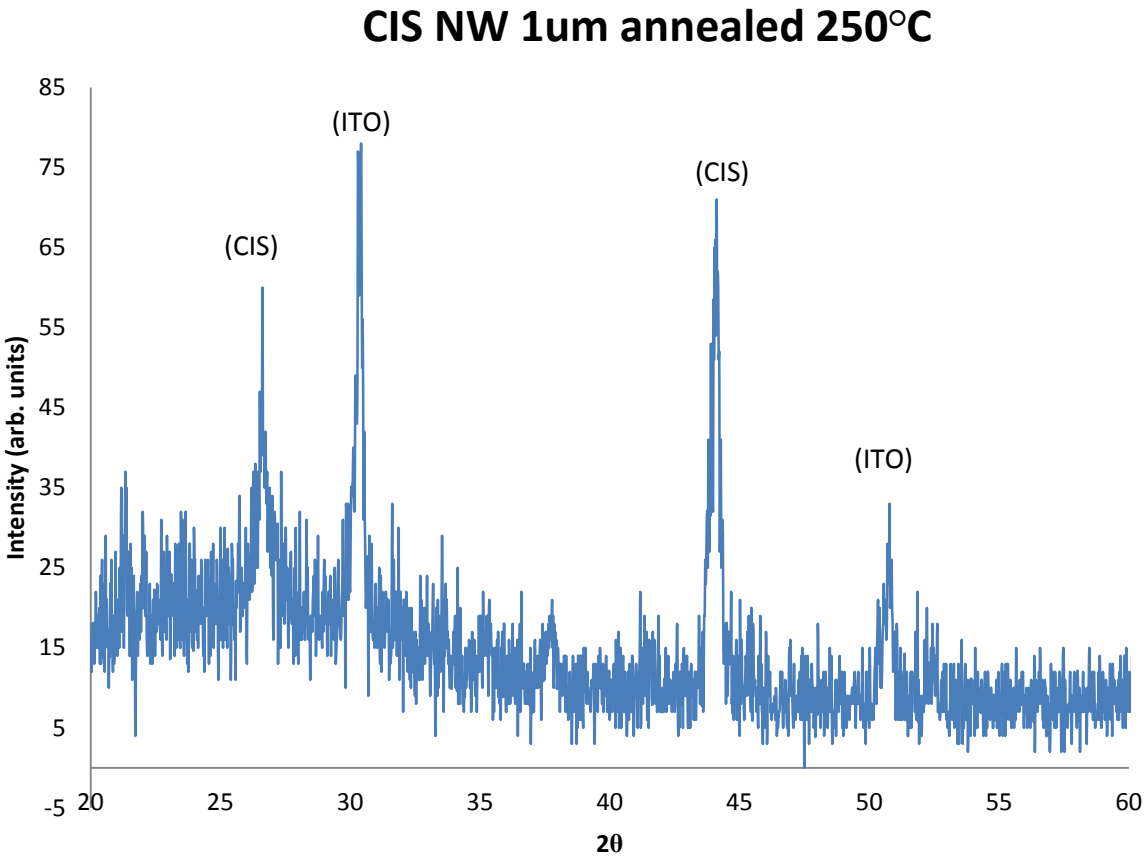


Figure 15: X-ray Diffraction pattern of electrodeposited CIS nanowires in AAO template on a glass-ITO substrate at 250°C

4.4 Optical Absorption & Near Infrared (NIR) Spectroscopy:

The absorption spectrum of CIS nanowires embedded in AAO on ITO substrate before and after annealing is compared with the ITO-AAO template of 1.5μm thickness, which is taken as the baseline for identifying the absorption spectra. Due to the presence of quantum confinement inside the sample, absorption spectrum cannot be calculated in the UV-visible region for which reason Near IR spectrum is considered.

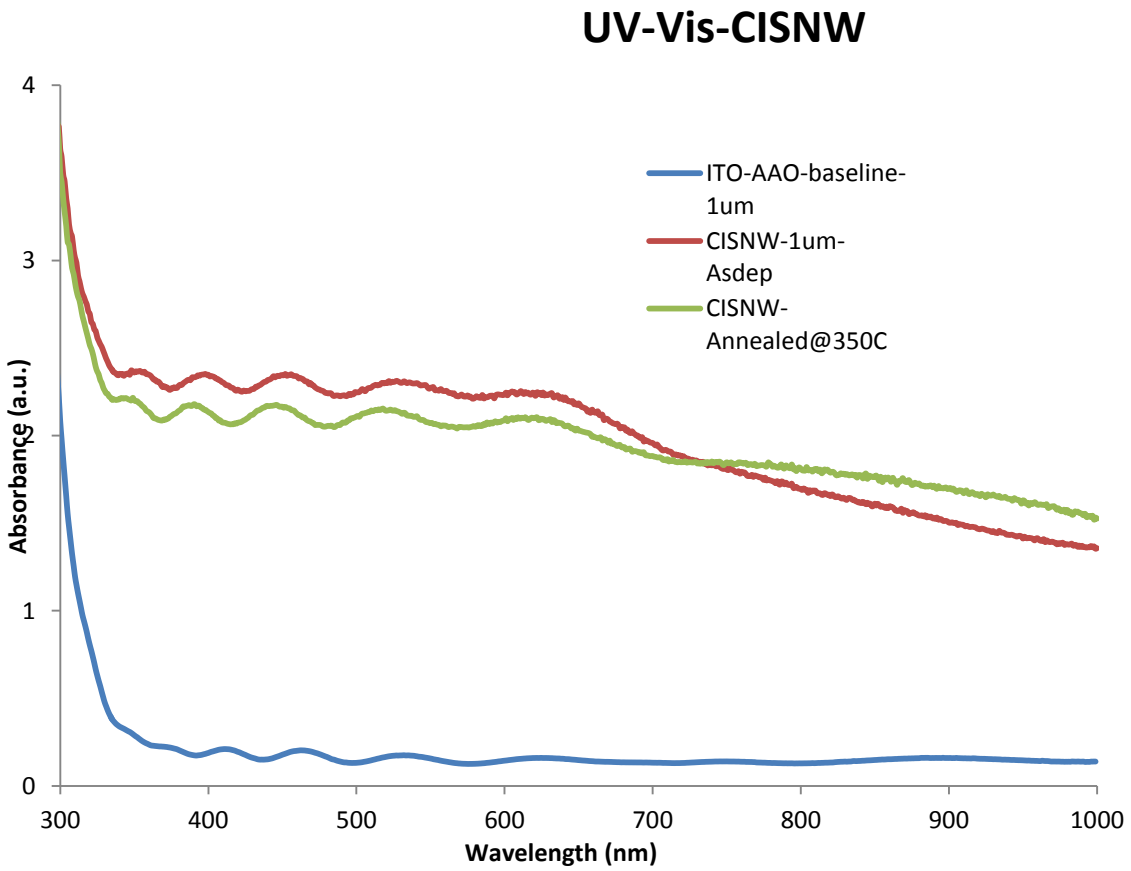


Figure 16: Optical absorption spectra of electrodeposited CIS nanowires embedded in an AAO template on a glass-ITO substrate

Figure 17 shows the absorption spectrum of CIS nanowires inside an AAO template in the infrared region ranging from 800-2500nm. Due to the experimental confinement present in the optical component, the range over which the readings were taken are restricted to 1100-2500nm. From the figure 17, we observe that the absorption edge is at 1150nm for a sample annealed at 350°C, which when used to calculate the effective band gap, yields an absorption spectrum of 1.07eV as compared to 1.05eV [28] for an ideal CIS solar cell.

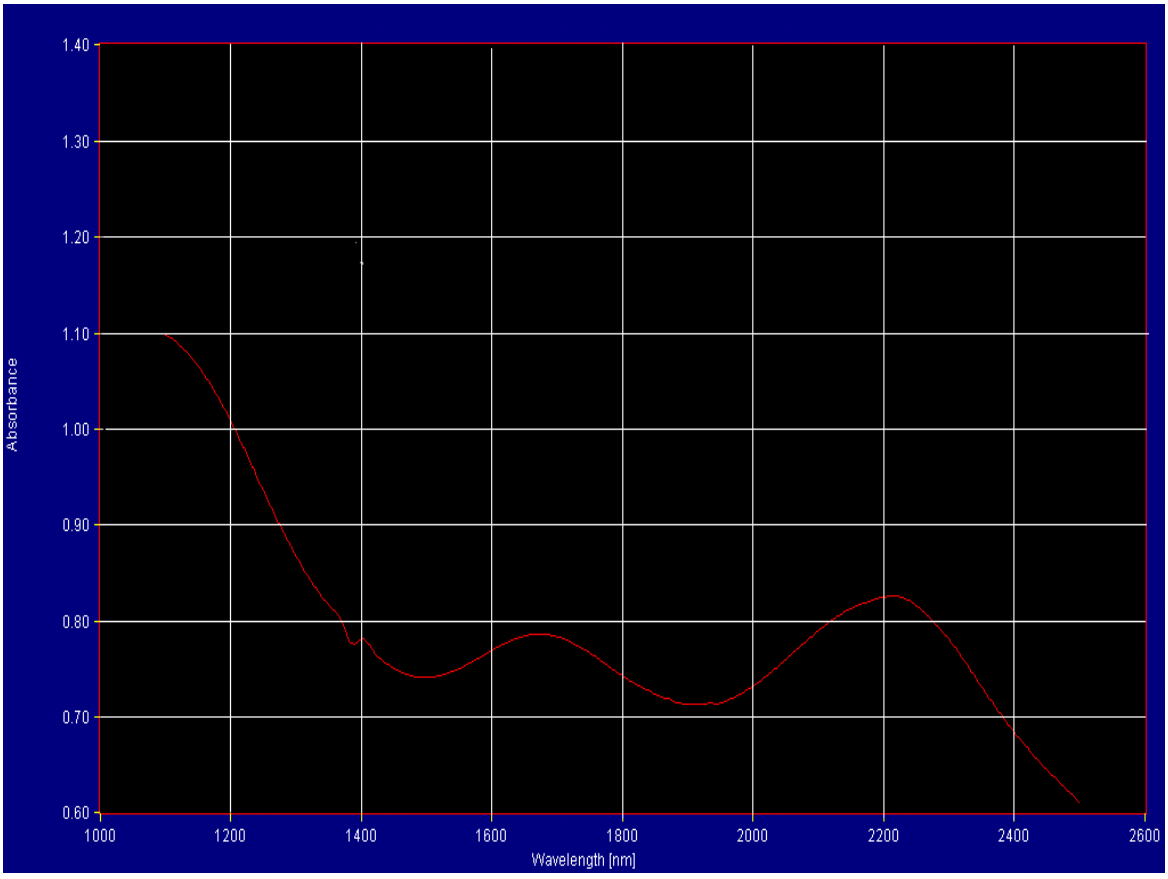


Figure 17: Near Infrared spectroscopy of CIS nanowires inside an AAO template

4.5 JV Characteristics:

The current density (J) vs. voltage (V) characteristics is determined in the dark and under "one sun" illumination, of a 0.07 cm^2 area ITO-CIS inside an AAO template. Aluminum, Graphite and Gold served as the top contact to CIS.

After comparisons with different materials as top contact, we conclude that the semiconductor deposited inside the AAO template is of p-type. Both Schottky diode and Ohmic contact behaviors are exhibited when metals with different work functions, both greater and lower than the semiconductor, are deposited on the top.

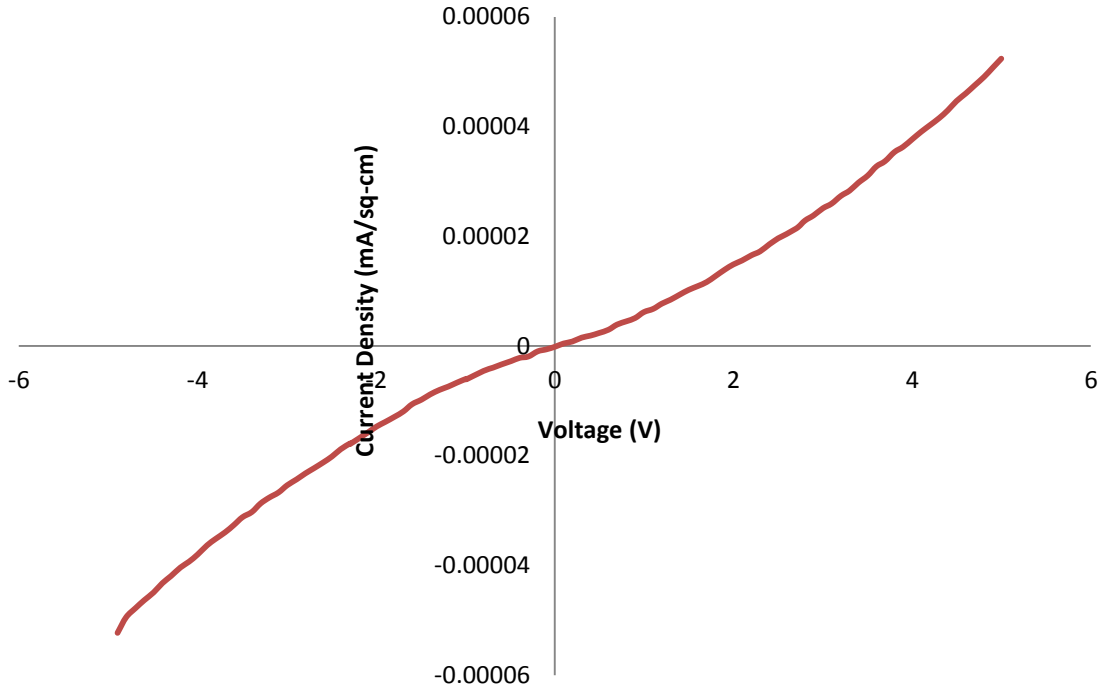


Figure 18: JV Characteristics of ITO-CIS-Al inside an AAO template

Figure 18 shows the current density-voltage characteristics of a ITO-CIS-Al schottky diode. In the case of ITO-CIS-Al schottky on AAO templates we observe that the currents were very low and there is a lift off voltage present beyond 5V. Also the current densities are similar both in dark and under illumination and hence the curves overlap each other, the low currents could be attributed to the fact that the nanowires are not in proper contact to the metal on top due to pin hole diffusion and hence this may not be used to determine the type of CIS material.

Figure 19 shows that the current density-voltage characteristics in the case of ITO-CIS-Graphite schottky diode has higher currents and that Graphite with a work function of 5.0eV [29] makes an Ohmic contact with CIS thus strengthning the fact that the CIS deposited is of p-type.

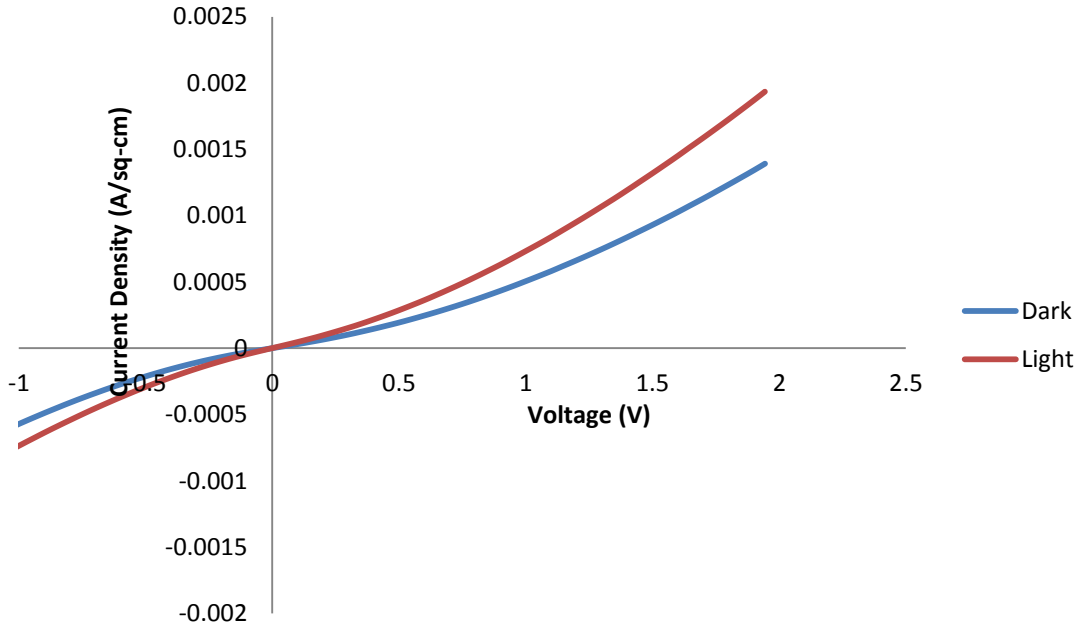


Figure 19: JV Characteristics of ITO-CIS-Graphite inside an AAO template

4.5.1 Calculation of Jo and Series Resistance of CIS-Graphite Schottky:

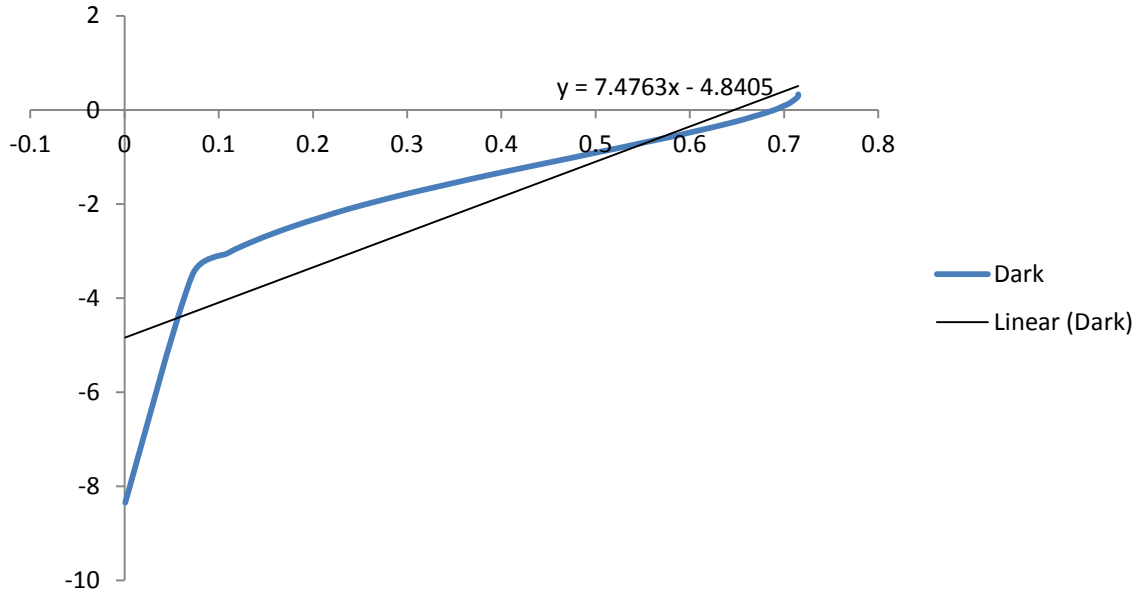


Figure 20: Plot of Ln (J) vs. V of CIS-Graphite Schottky diode under dark

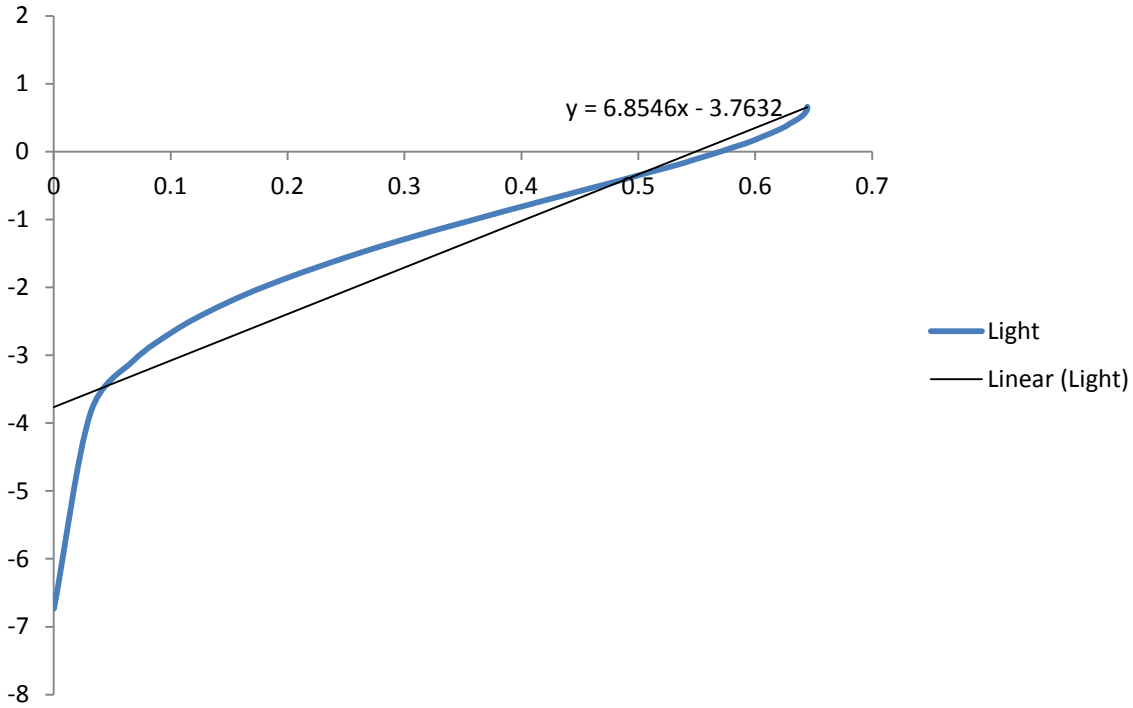


Figure 21: Plot of Ln (J) vs. V of CIS-Graphite Schottky diode under light

Photo conductance was exhibited by the device but no photo voltaic effect was observed. Diode analysis was performed for these devices and the values of the effective reverse saturation current (J_o) and the effective diode ideality factor (A) were calculated to fit the equation,

$$J= J_0 [(exp(qV/(AkT))-1]$$

Table 1: Diode parameters for ITO-CIS-Graphite Schottky diode

Illumination	**Series Resistance (R_s) (Ohms)**	**Effective Jo ($\mu A/cm^2$)**	**Diode Ideality factor (η)**
Dark	882.994	11.3	5.2
Light	671.294	23.2	5.6

From the above obtained values we observe that the measured values of Diode Ideality factor are greater than 2.0, which indicates that the dominant mechanism of electron transport across the junction is likely to be interface state recombination or tunneling, or combination of both.

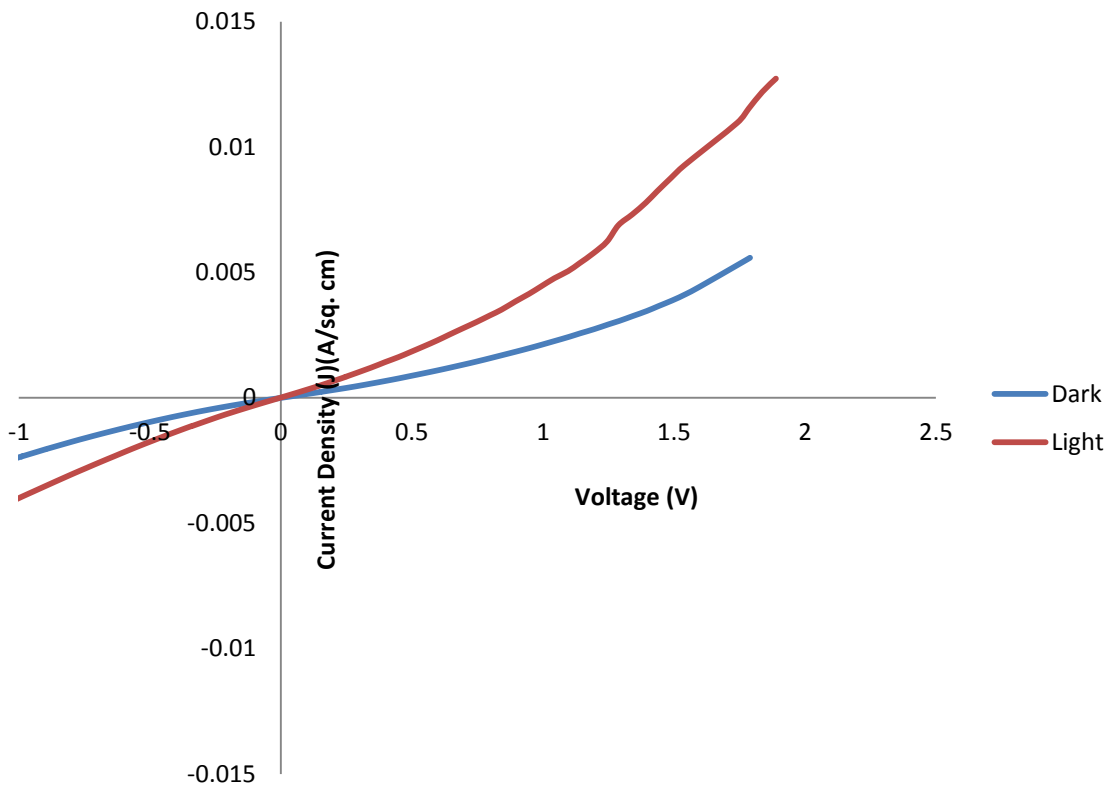


Figure 22: JV Characteristics of ITO-CIS-Au inside an AAO template

Figure 22 shows the Current density (J) vs. Voltage (V) characteristics for ITO-CIS-Au diode. Just as in the case of ITO-CIS-Graphite paste, Au too has a higher work function of 5.1eV [30] compared to that of CIS thus making an Ohmic contact with p-type CIS. With Au being a proper metal contact deposited using e-beam evaporation technique, we observe the currents being much higher when Au is deposited on top as opposed to Graphite paste. The fact that graphite paste also consists of polymers decreases its contact resistance with the CIS nanowires and hence may not be the most feasible option available.

4.5.2 Calculation of Jo and Series Resistance of CIS-Au:

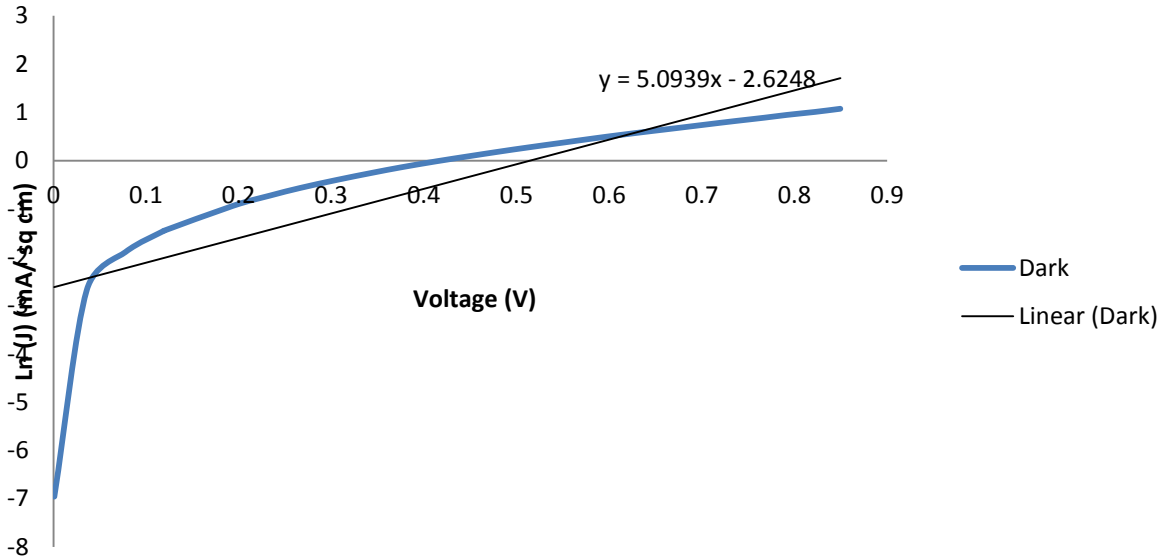


Figure 23: Plot of Ln (J) vs. V of CIS-Au diode under dark

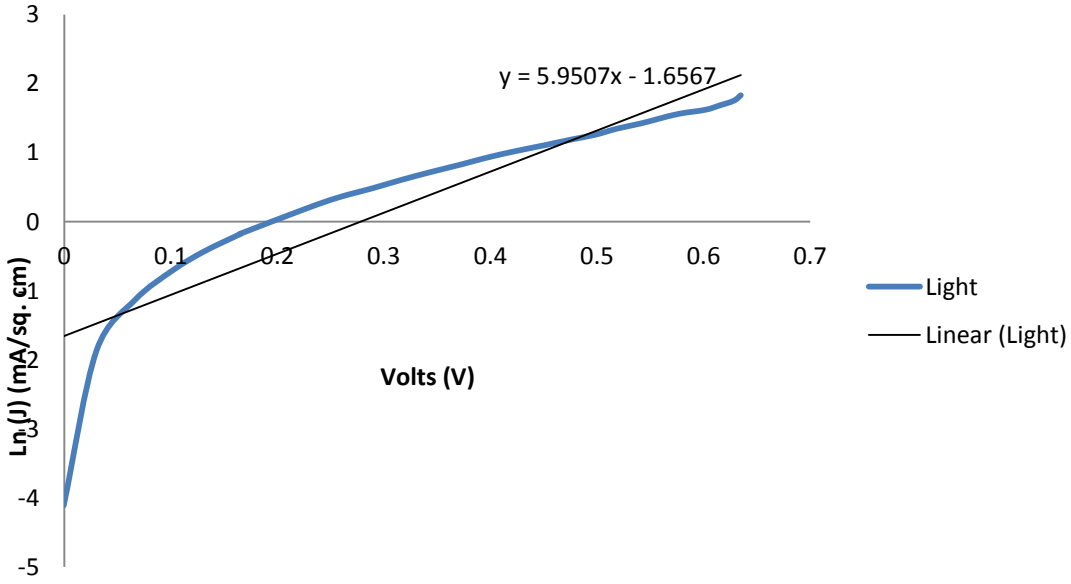


Figure 24: Plot of Ln (J) vs. V of CIS-Au diode under light

Photo conductance was exhibited by the device but no photo voltaic effect was observed. Diode analysis was performed for these devices and the values of the effective reverse saturation current (J_o) and the effective diode ideality factor (A) were calculated to fit the equation,

$$J= J_0 [(exp(qV/(AkT))-1]$$

Table 2: Diode parameters for ITO-CIS-Au Schottky diode

Illumination	**Series Resistance (R_s) (Ohms)**	**Effective Jo ($\mu A/cm^2$)**	**Diode Ideality factor (η)**
Dark	136.288	72.4	7.58
Light	97.836	190.7	6.49

In all the cases discussed above, it can be seen that the device current is higher under illumination when compared to their corresponding dark currents owing to photo conductance of CIS. This can be attributed to the fact that under illumination more carriers get excited; hence, more current.

Similarly as in the case of ITO-CIS-Graphite Schottky diode we observe that the measured diode ideality factor is greater than 2.0 owing to tunneling or interface state

recombinnations. Also the effective current densities are higher under illumination owing to photo conductance.

4.6 Calculation of Resistivity (ρ) of deposited CIS nanowires:

As discussed above, gold deposited by means of electron-beam evaporation technique has more ideal diode parameters as that compared to graphite paste; hence, the values considered in calculation of resistivity are that of gold Schottky diode.

The Sputtered Gold dots have an area of 0.07 cm^2. From the SEM images we can find the pore density to be approximately 1.3E09 pores/cm^2. The diameters of the nanopores were approximately 60nm. So the area of each wire would be 2.286E-11 cm^2. Assuming 25% porosity we have,

Area of the gold dot= 0.07 cm^2;

Length of the pore = 1500 nm;

Radius of the pore= 30 nm;

Area of the pore = $\pi * R^2$= 3.14 * 30E-9 * 30E-9 = 2.286E-11 cm^2;

Pore density = 1.3E9 pores/cm^2;

Porosity= 25%;

Number of CIS Nanowires in contact with gold dot= area of dot * pore density * porosity = 0.07 cm^2 * 1.3E9 * 0.25 = 2.275E7 nanowires;

Area of CIS nanowires contact to the metal = Area of the pore * number of CIS nanowires

= 2.286 E-11 * 2.275E7 = 5.2007 E-4 cm^2;

We know that resistivity (ρ) = Resistance * Area/ Length

Substituting series resistance, area of the CIS nanowires contact, length of the pore in the above equation, we get

ρ = 472.5Ωcm.

Our results are consistent with the size dependent resistivity values reported by Yong Shi et al [31] on CIS films. Resistivity of CIS film was strongly dependent on the grain size in their work, which range from 400nm to 100nm having respective resistivity's of 0.58Ωcm to 516.4Ωcm for CIS annealed at different temperatures. In our case, the particle size does not increase with annealing temperature but instead is limited by the template pore size, which is in the 30nm range.

4.7 Device Operation:

Alumina acts as a wall separating nanowires from each other. ITO substrate at the bottom makes a Schottky contact to p-type CIS nanowires, while gold makes an ohmic contact with p-type CIS nanowires at the top. CIS nanowires, which act like a p-type semiconductor, has an electron affinity of 4.48eV and an energy band gap of 1.07eV (obtained value). Aluminum has a work function of about 4.06eV and gold has a work function of around 5.1eV [30]. The work function of the metal (i.e., Al) is less than that of semiconductor ($\Phi_m < \Phi_s$), which is of p-type makes a Schottky contact. Also the work

function of the metal (i.e, Au) is greater than that of semiconductor ($\Phi_m > \Phi_s$), which is of p-type makes an ohmic contact. Figure 25 shows the energy level diagram for CIS-Al (p-type) Schottky junction. The difference in the work function provides an electric field at the Al-CIS interface [32].

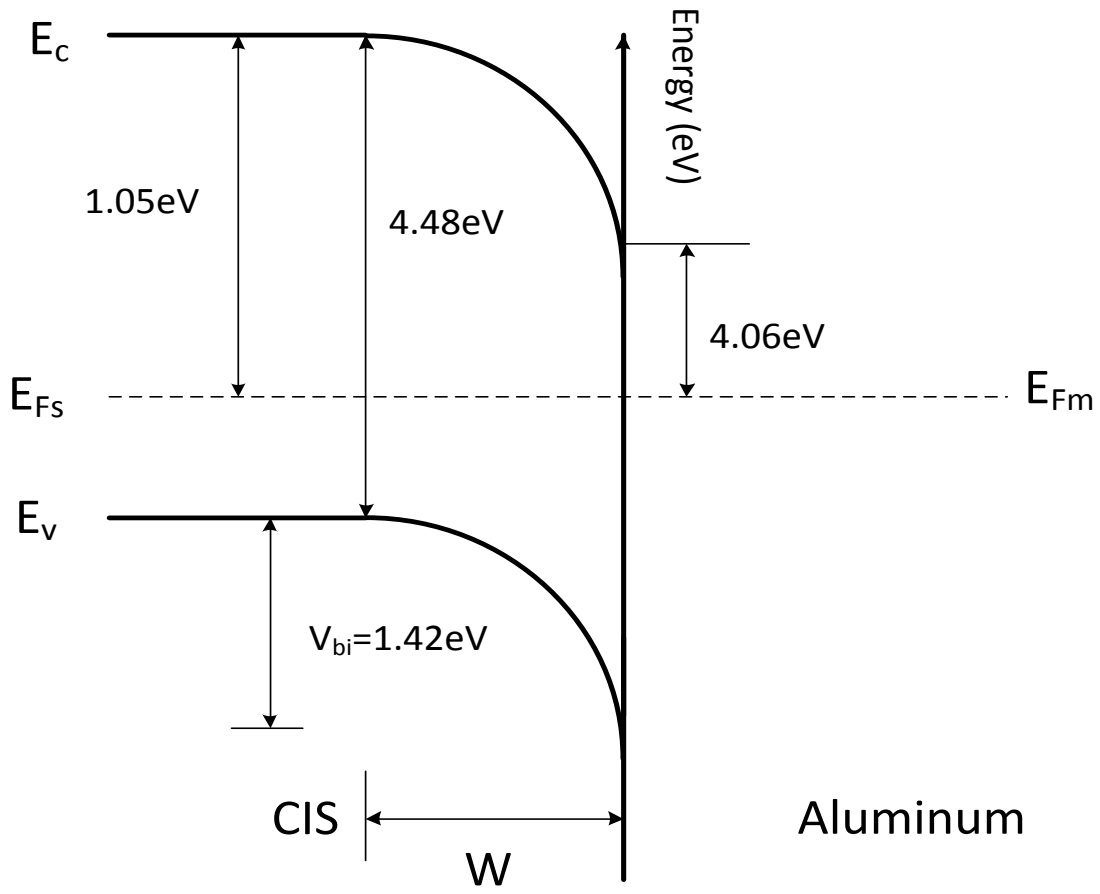


Figure 25: Energy level diagram of CIS-Al junction

5 Conclusions and Suggestions for Future Work

The template-directed electrode position method was utilized to electrodeposit p-CIS nanowires inside an AAO template. The AAO on ITO/glass substrate was chosen because of its stability and transmittance of light. The XRD pattern of the embedded p-CIS nanowires annealed at 350°C for thirty minutes showed better crystallization with a strong preference of <112> orientation at 26.6 degrees. The UV-Vis and NIR spectroscopy results showed that the band gap of the p-CIS nanowires was 1.05eV. The JV analysis of the ITO-CIS-Au Schottky junction yielded reverse saturation current density values of J_o = 72.4μA/cm^2 and A = 7.58 in the dark, and J_o = 190.7 μA/cm^2 and A = 6.5 under one sun illumination, respectively. The resistance (R_s) of the CIS nanowires of 1500 nm length and 55 nm diameter was calculated as 136.2 and 97.8 Ω in dark and under one sun illumination, respectively. From the Schottky diode behavior of the ITO-CIS-Au junctions, it was deduced that these CIS nanowires were p-type.

It is suggested that future work be focused on electro-depositing CdS (or n-type CIS) nanowires on ITO prior to the deposition of CIS nanowires or bulk CIS. CdS (or n-type CIS) nanowires would act as the window layer in the n-CdS/p-CIS heterojunction solar cell or in the n-CIS/p-CIS homojunction solar cell. Such devices will have higher efficiency due to improved lattice matching (in case of n-CIS window layer) and reduced losses due to interface states. Also decreasing the diameter of the pores to approx. 4 nm would improve the efficiency of the solar cell due to quantum confinement.

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Vita

Sri Harsha Moturu was born on January 21st, 1986 in Vijayawada, Andhra Pradesh, India. He received the Bachelors of Engineering degree in Electronics and Communication Engineering from Anna University, Chennai, Tamilnadu, India, in 2007. His research is to fabricate Copper Indium Diselenide (CIS) nanowires on an Anodized Alumina Oxide (AAO) substrate. In 2007 he began to study in department of Electrical Engineering at University of Kentucky.