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Electric field driven memristive behavior at the Schottky interface of Nb-doped SrTiO₃

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Computing inspired by the human brain requires a massive parallel architecture of low-power consuming elements of which the internal state can be changed. SrTiO₃ is a complex oxide that offers rich electronic properties; here, Schottky contacts on Nb-doped SrTiO₃ are demonstrated as memristive elements for neuromorphic computing. The electric field at the Schottky interface alters the conductivity of these devices in an analog fashion, which is important for mimicking synaptic plasticity. Promising power consumption and endurance characteristics are observed. The resistance states are shown to emulate the forgetting process of the brain. A charge trapping model is proposed to explain the switching behavior. *Published by AIP Publishing.* https://doi.org/10.1063/1.5037965

I. INTRODUCTION

Modern day computers rely heavily on the *von Neumann*[1] architecture, and while for many tasks this computing approach works well, it cannot compete with the speed, low power consumption, and adaptability of the human brain for certain functions, such as performing cognitive tasks. This has led to a need for alternative architectures inspired by the performance of the brain.[2–6] In such neuromorphic architectures, memory and processing operations are ideally co-located in devices that are highly connected, capable of computing in parallel yielding an analog output while consuming low power.[2,3,5–7] In order to mimic such performance of the brain, multi-level storage devices and a high storage density are needed.[4,6–9] The exact required device performance specifications, including switching speed and retention, strongly depend on the biological functionality that is required from the neural network.[2,3,5,6] For example, the processes of learning and forgetting in the human brain are governed by the modulation of the strengths of paths connecting neurons, known as synaptic weights, as a result of action potentials.[4,7,10,11] This *synaptic plasticity* behavior can be emulated by memristors:[12] two-terminal devices of which the microscopic internal state can be modified and measured as a change in the conductance. Consequently, these devices can be used to emulate synapses for neuromorphic computing.[4,8,10,11] These memristors should have sizes on the order of nanometers and should offer low power consuming resistive switching in order to be able to build a highly connected parallel architecture.[5] These features make these devices very computationally efficient as well as fault tolerant; connections that do not work can be bypassed through alternative paths.

In many material systems where memristive behavior has been demonstrated, resistive switching is absent in the as-fabricated device and an electroforming process, during which the device is subjected to a high bias, is needed to induce the switching.[2,10,13,14] The details of the forming process are well discussed in the literature but pose a limitation on the operation of memristors at low powers due to the requirement of the high forming voltage. Additionally, a lack of control over the forming process can increase device-to-device variations and reduce device performance.[2,9,10,15] In this context, interface driven memristive effects such as that found in Schottky interfaces between Nb-doped SrTiO₃ (Nb:STO) and metals, without the need of a forming process, are an important consideration.[11,14,16–23] Recently, there has been a growing interest in understanding the rich and intricate properties of complex oxide interfaces and their application in superconductivity, magnetism, and multiferroics.[24–27] The Schottky interface of Nb:STO offers rich electronic properties that have been shown to be useful both for memristor and spintronics applications.[28–31] An important parameter is the non-linear variation of the large dielectric permittivity (ϵ_r) with temperature and electric field.[32] The tuning of the potential profile of the conduction band of Nb:STO with electric field and temperature gives rise to charge transport characteristics that are unique and are not observed in conventional semiconductors like Si, GaAs, and Ge.

In this paper, the use of Ni/Nb:SrTiO₃ Schottky junctions for potential applications in neuromorphic memristors is evaluated. Here, relatively large structures for Ni contact pillars ($100 \times 200 \, \mu m^2$) on Nb:STO are used; the simplistic structure of these pillars, however, lends itself well to the required down-scaling. In the first part of this work, the possibility of multi-level switching is demonstrated by gradually sweeping the applied voltage. By changing the magnitude of the reverse bias *reset* voltage, the devices can be switched to higher resistance states so that multi-level storage can be realized. From this, important information about the resistance switching mechanisms is also inferred. The second part of this work focused on how the resistance state can be changed by applying voltage pulses. This is of importance for emulating synaptic behavior, where resistance changes are brought about by the spiking behavior of neurons.[11] The reliability of the devices, with respect to retention and endurance, was investigated by performing repeat cycles of resistance switching.

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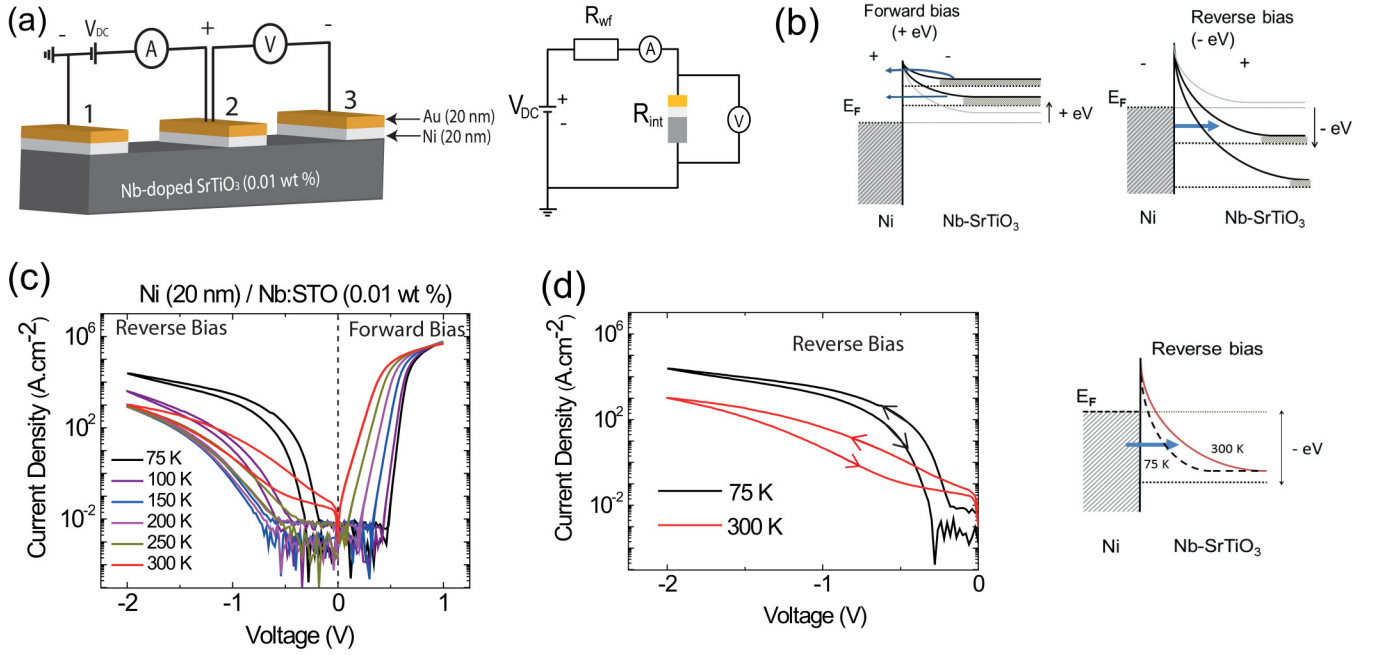
FIG. 1. (a) Three terminal (3T) device geometry where a voltage (V_{DC}) is sourced between central contact 2 and a grounded reference contact 1, giving rise to a potential drop between contact 2 and reference contact 3. The measurement scheme used is 4-probe, and the junction voltage (resistance R_{int}) is measured, decoupled from the resistances due to the leads and the semiconductor channel (R_{wf}). (b) Potential profiles for different polarities of V_{DC}: positive (forward bias) and negative (reverse bias) across the Schottky interface of Nb:STO with Ni at room temperature. (c) Temperature dependent I-V characteristics for a contact ($100 \times 200 \, \mu m^2$) where the current density is plotted with junction voltage. (d) Increase in the reverse bias current on decreasing temperature, as shown by the crossover of the reverse current between 75 K and 300 K. The potential profile shows narrowing of the conduction band in STO at 75 K resulting in increasing current due to enhanced tunneling.

II. EXPERIMENTAL DETAILS AND RESULTS

Devices were fabricated on n-type doped (001) SrTiO$_3$ single crystalline substrates with 0.01 wt% Nb doping, obtained from Crystec GmbH. To remove the SrO sublattice from the top surface and obtain TiO$_2$ termination, the substrates were treated with buffered hydrofluoric acid and deionized water. This was followed by the immediate deposition of 20 nm of Ni, capped with 20 nm of Au by electron beam evaporation at a base pressure of 10^{-6} Torr. Three terminal (3T) geometry meso-structures were fabricated by UV lithography and Ar-ion etching. A typical device geometry is shown in Fig. 1(a). In order to investigate the Schottky contact of Ni on Nb:STO, current-voltage (I-V) measurements were performed in a 4-probe, three terminal (3T) geometry using a Keithley 2410. In this geometry, a dc-voltage (V_{DC}) is sourced between a central contact 2 and a grounded reference contact 1 [shown in Fig. 1(a)], giving rise to a potential drop between contact 2 and reference contact 3. The dc-current is measured between contact 2 and source contact 1. This geometry ensures that the potential drop (V) is caused solely by the interface resistance (R_{int}) of contact 2 and eliminates series resistances from the leads, semiconducting channel (R_{wf}), and the two reference contacts. Isolating the effect of a single Schottky interface gives a better understanding of the transport mechanisms that are controlled by the electric field across the interface with Nb:STO. The temperature-dependent I-V characteristics of a junction of $100 \times 200 \, \mu m^2$ are shown in Fig. 1(c). At each temperature, the current density is plotted with respect to V, following a sweep from $0 \, V \rightarrow +1 \, V \rightarrow 0 \, V \rightarrow -2 \, V \rightarrow 0 \, V$. The I-V

characteristics clearly show the existence of a Schottky barrier at the Ni/Nb:STO interface. Transport in forward bias is governed by thermionic emission. Upon increasing the voltage, the conduction band of Nb:STO is raised with respect to the Fermi level (E_F) of Ni, as shown in Fig. 1(b), resulting in a decrease in the width of the depletion region and the built-in electric field. At low temperatures, there is less thermal energy available for electrons to overcome the barrier, and consequently, larger voltages are required for transport compared to higher temperatures. Current density, J, can be described by

$$J(V) = A^* T^2 e^{-\frac{q\phi_B}{k_B T}} \left(e^{\frac{qV}{nk_B T}} - 1 \right), \tag{1}$$

where A^* is the Richardson constant, q the electron charge, ϕ_B the Schottky barrier height, k_B the Boltzmann constant, n the ideality factor, V the applied voltage, and T the temperature.

In reverse bias (negative V_{DC}), a strong response of the dielectric permittivity of STO (ε_r) to the increasing built-in electric field results in a steeper bending of the conduction band of STO as shown in Fig. 1(b). This decrease in the effective barrier width at E_F promotes tunneling, allowing current to flow in the reverse bias regime. The reverse current increases upon lowering the temperature as illustrated in Fig. 1(d) where 75 K and 300 K are compared. Upon reducing temperature, ϵ_r increases and becomes more sensitive to electric fields, resulting in a significant narrowing of the conduction band potential and allowing for enhanced tunneling.[33,34] In summary, the charge transport is
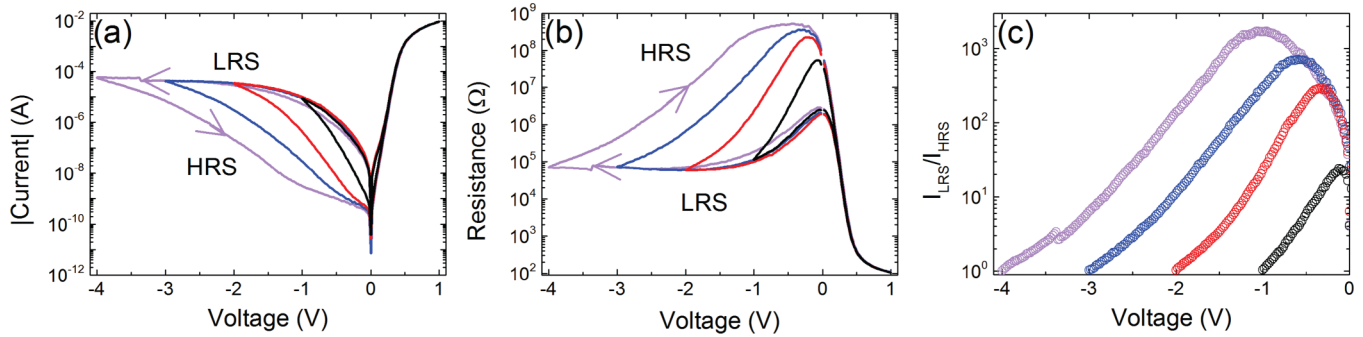
FIG. 2. (a) Room temperature I-V characteristics of the device obtained by performing repeat cycles in which the voltage was swept between $+1\,V$ and a varying $[-1\,V$ (black), $-2\,V$ (red), $-3\,V$ (blue), and $-4\,V$ (purple)] reverse bias voltage. Each subsequent cycle was done after a delay time of $300\,s$ at $+1\,V$. The upper branch of each cycle is the low resistance state (LRS) and the lower branches are the high resistance states (HRSs). (b) Resistances calculated from the cycles performed in (a); the lower branches are the trace directions and the upper branches are the retrace directions. (c) Ratios of the HRS (lower branch) and LRS (upper branch) resistance values calculated from (a).

governed by thermionic emission of charge carriers in the forward bias regime and by temperature independent field emission in reverse bias.

The reverse bias hysteretic response of the resistance embodies the colossal electroresistance (CER) effect. The Schottky interface of Nb:STO is replete with trapped charge states in the form of oxygen vacancies that occupy energy levels about 0.5 to 1 eV below the conduction band.[35–37] Their accessibility to electrons flowing into the conduction band in Nb:STO is enhanced by the increasing electric field, giving rise to the CER effect. This switching is bipolar: the resistance will increase in reverse bias and decrease in forward bias.

To demonstrate multi-level resistance switching, the bias voltage was swept from $+1\,V \rightarrow -V_{reset} \rightarrow +1\,V$. The *set* voltage ($+1V$) and time ($300\,s$), to switch to a low resistance state (LRS), was kept constant, while the *reset* voltage (V_{reset}) was varied ($-1\,V$, $-2\,V$, $-3\,V$, and $-4\,V$) to *reset* to different high resistance states (HRSs). The results of this are shown in Fig. 2(a) and illustrate that by changing the *reset* voltage, states of increasingly higher resistance can be attained. The resistance values corresponding to every part of the loops are explicitly plotted in Fig. 2(b). The resistance of the LRS does not change significantly by changing the bias, while the resistance of the HRS peaks at a low bias value and thereafter decreases until reaching the resistance value of the LRS at the maximum *reset* voltage. This is mimicked in Fig. 2(c), where the ratio of the resistance of the HRS over the LRS is extracted at every reverse bias value.

The room temperature endurance and cycle-to-cycle resistance variations were understood by performing 100 subsequent cycles between $+1\,V$ and $-4\,V$ and back, shown in Fig. 3. The first 99 cycles were done with a *set* time of $120\,s$ at $+1\,V$ between cycles. The last cycle was performed after a 1 h *set* time at $+1\,V$. There is minimal variation in the HRS between cycles, while the resistance of the LRS increases upon cycling. This indicates that the $120\,s$ used to *set* the device is insufficiently long to completely restore the LRS. These data show that the device is able to repeatedly switch its resistive state over at least 100 consecutive cycles without showing any degradation in device performance.

The retention of the LRS and HRS was investigated by setting the respective states in two ways. Firstly, by the

voltage sequence shown in the bottom panel of Fig. 4(a): here the LRS was *set* by sweeping $0\,V \rightarrow +1\,V \rightarrow 0\,V$ with a *set* time of $120\,s$ at $+1\,V$. This was followed by a negative bias read pulse of $-1\,V$. The device was subsequently *set* to a HRS by sweeping $0\,V \rightarrow -4\,V \rightarrow 0\,V$, and another read pulse was applied. Secondly, the LRS and HRS were *set* by applying short pulses of $0.9\,s$ of $+1\,V$ and $-4\,V$, respectively, depicted in Fig. 4(b). In both cases, the sequences were repeated five times.

The two sets of results demonstrate that the resistance of the HRS does not significantly change either over time or between cycles. The differences in the LRSs resulting from the two setting methods on the other hand clearly show deviations. When a short pulse is used to *set* the LRS, the resulting resistance difference between the LRS and HRS is smaller than when a longer pulse is used to *set* this state. Over time, the resistance of the LRS becomes higher, and for the short pulse setting method, the high and low resistance states reach similar resistance values more rapidly.
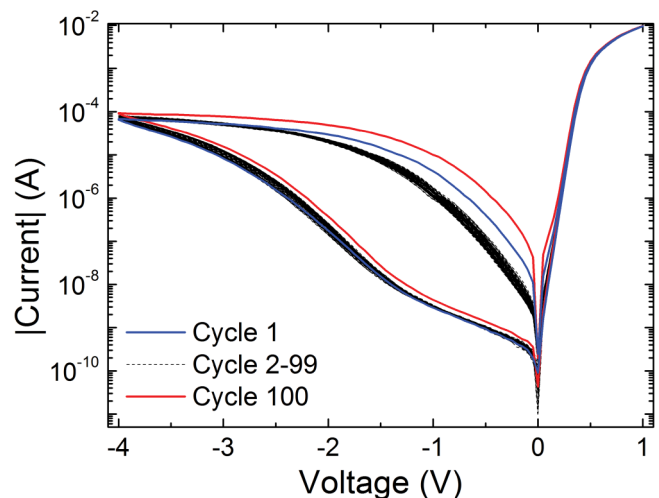

FIG. 3. Endurance characteristics of the device over 100 subsequent switching cycles. The first (blue) to 99th cycle were performed following a sequence where, after a $120\,s$ wait time at $+1\,V$, the voltage was swept from $+1\,V$ to $-4\,V$ and back to $+1\,V$. The black lines show cycle 2-99. Cycle 100 (red) was obtained after a 1 h *set* time at $+1\,V$.
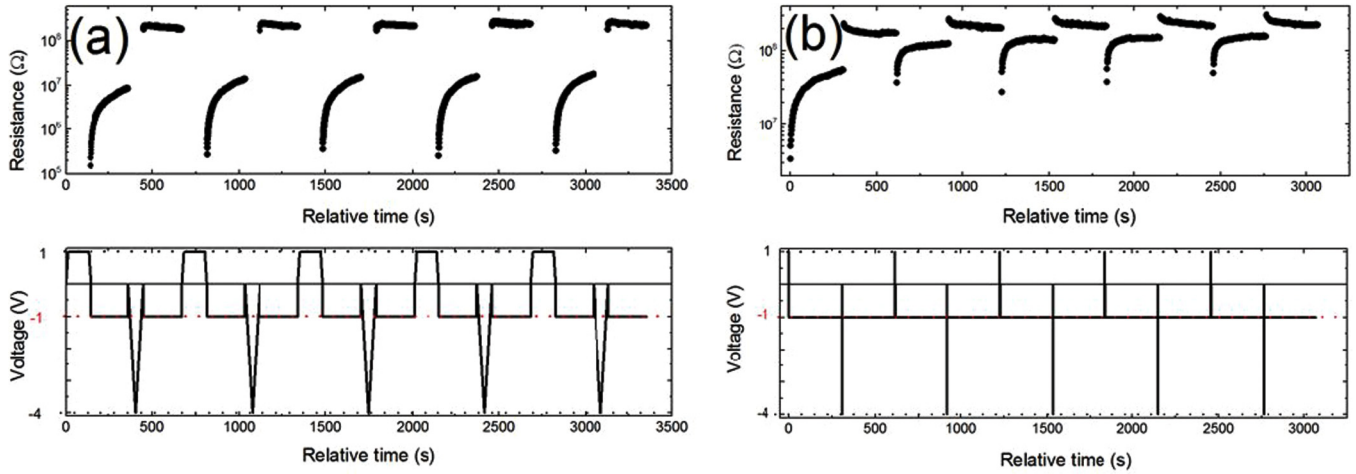
FIG. 4. Retention characteristics of the LRS and HRS upon repeatedly switching between the two states by (a) voltage sweeps and (b) voltage pulses.

III. DISCUSSION

Stable bipolar resistive switching was present in the as-fabricated device without the requirement of an electroforming process. This indicates that the nature of the switching is not mediated by the formation of local filamentary paths, as is seen in many oxides that are initially insulating. The Schottky nature of the transport characteristics is evident from the temperature dependence of the charge-transport measurements shown in Fig. 1(c). The importance of the existence of the Schottky barrier in realising switching is evident from junctions where no proper Schottky contact was established; these show an absence of hysteresis, even with large voltage sweeps, up to −10 V (Figs. S1 and S2 in the supplementary material). Both these observations confirm the interfacial origin of the resistive switching.[11,18–20]

Estimations of the barrier heights in the LRS and HRS, realized using a *set* voltage of +1 V and a *reset* voltage of −4 V, were made by fitting (1) in the forward bias regime (Fig. S3 in the supplementary material). This gives a value of 0.72 ± 0.01 eV for the LRS and 0.76 ± 0.01 eV for the HRS. The height of the barrier is smaller in the LRS than in the HRS, allowing for an increase in the number of electrons able to overcome the barrier in the forward bias regime, where charge transport is governed by thermionic emission [see Fig. 1(b)].

Resistive switching is the result of a change in the charge at the interface from a more negative to a more positive value between the HRS and LRS. In the literature, both the redistribution of oxygen vacancies and the trapping and de-trapping of electrons at the interface under electric fields have been linked to this change.[11,16,20,38] After switching, it is observed that both the LRS and HRS asymptotically approaches a stable value over time: the resistance of the LRS becomes higher, while the resistance of the HRS becomes lower. In both cases, the resistance R over time t could be fit using the Curie-von Schweidler equation $R \propto t^n$[16] with rate related exponents, n, for the LRS and HRS of 0.685 and −0.244, respectively (see Fig. 5). This change is associated with capacitive charging and is typically observed in high-κ materials due to the trapping of charges under bias.[11,16,18,23]

Under the influence of a reverse bias voltage, the mobile electrons are trapped at defects and oxygen vacancy sites which result in a reduction in the positive charge at the interface. Consequently, the barrier becomes higher and wider resulting in a switch to the HRS. When electrons become de-trapped from the interface, the charge in this region becomes more positive, resulting in a reduction of the height and width of the Schottky barrier giving the LRS. When switching from the HRS to LRS, charges are de-trapped, and more trap states are available at the interface. Over time, negative charges will again become trapped in these states resulting in a progressive increase in the resistance of the LRS. Fig. 2(a) shows that the hysteresis in the forward bias direction (governed by thermionic emission) is less significant than in the reverse direction (governed by tunneling) which suggests that the resistive switching does not originate purely from changes in the profile of the barrier.

Trap-assisted tunneling may also contribute to transport, and when the trap states become filled, these paths become blocked so that tunneling is suppressed.[38] When the reverse bias reset voltage is increased, the strength of the electric
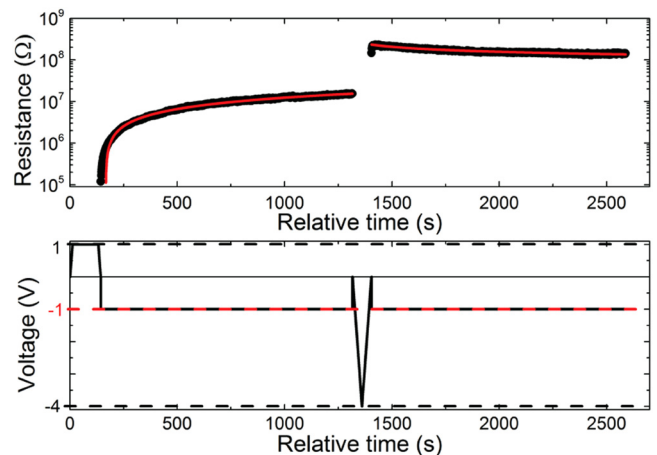

FIG. 5. Fits (shown in red) of the Curie-von Schweidler equation to LRS and HRS after setting the respective states with voltage sweeps between 0 V and +1 V and −4 V. The extrapolation of these fits was used to estimate the retention time.

field across the interface increases. Additionally, with a larger reverse bias, transport is dominated by electrons tunneling from states further below the Fermi level in the metal to the semiconductor side. Consequently, a larger range of interfacial states is available in which they can become trapped, resulting in an increase in the resistance of the HRS obtained upon increasing the *reset* voltage.

Figure 4 demonstrates that there is very little variation in the HRS after repeat cycles, and there is no difference in the value realized by the sweeps and pulses. The LRS state, on the other hand, is affected more significantly, and the resistance achieved with a longer setting process is noticeably lower and reproducible upon cycling. These observations are in accordance with the increasing resistance of the LRS upon cycling (Fig. 3) and indicate that the setting process is slower than the resetting. While, within the time the states were monitored, the difference in the resistance states remained substantial, the progressive change of the LRS (HRS) toward a state of higher (lower) resistance could indicate that over time both will tend to a steady state of intermediate resistance. By extrapolating the Curie-von Schweidler fits from Fig. 5, an estimate of 12 400 s (~3.5 h) is obtained for this retention time. A similar analysis was done for the measurement performed using pulses to *set* the states, and here a retention time of 4150 s (~1 h) is estimated (Fig. S4 in the supplementary material). This kind of relaxation is typically observed in systems where the switching mechanism is related to charge trapping and de-trapping.[38]

Figure 4 alludes to a temporal dependence on the setting process to realize the LRS. The two different methods for setting the LRS can be used to mimic learning and forgetting in short-term memory: when a relatively long stimulus (a positive bias voltage) is used to *set* the device to a state of low resistance and the resistance is monitored immediately after, there is a significant decrease in resistance with respect to before the stimulus. Over time, this state will approach a state more similar to before the stimulus.[9,11] If, on the other hand, a shorter pulse is used to *set* the LRS, the state of the device is less significantly affected. Like before, directly after presenting the stimulus the resistance state will be the lowest, but in this case, the device will tend to a state reminiscent of its state before the stimulus much faster. This can be compared to the fading of memory as time passes: less significant events (in this case, a shorter pulse) will be forgotten faster.

From Fig. 2(a), it is clear that multi-level switching can readily be achieved by changing the magnitude of the *reset* voltage. In this way, a plethora of resistance states can be defined at a single low bias read voltage. The gradual, rather than digital, nature of the resistance change not only mimics the analog nature of synapses, but also allows for a large storage. The small amount of current flowing in the reverse bias regime gives rise to very large resistance values [plotted in Fig. 2(b)] both in the LRS (~10^5 Ω) and in the HRSs (up to ~10^8 Ω). In addition to high resistance values, the resistance ratios between the HRS and LRS are also large [see Fig. 2(c)]: using −1 V as a read voltage, a maximum ratio of ~10^3 can be obtained. The power (*P*) consumption of this device is shown in Fig. 6 and estimated from every point of the I-V plot in Fig. 2(a) using $P = IV$. From the graph, it is
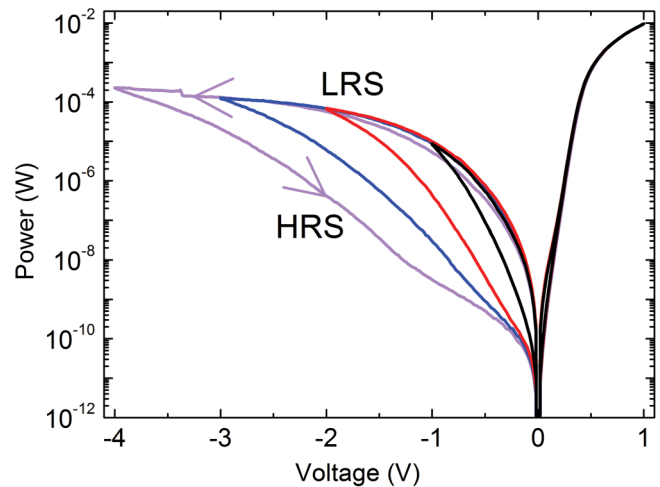

FIG. 6. Estimation of power consumption during series of I-V cycles shown in Fig. 2(a).

seen that using a read voltage of −1 V, between 10^{-9} W and 10^{-5} W is required to read four distinct states, when they have been "trained" in different cycles.

IV. CONCLUSION

Bipolar resistive switching at the Schottky interface of Ni and Nb-doped $SrTiO_3$ has been investigated. Measurements have been conducted to specifically address characteristics important for neuromorphic computing, including endurance upon repeat cycles, retention, power consumption, and multi-level switching. By changing the *reset* voltage, multi-level switching was demonstrated between highly resistive states with resistance variations up to three orders of magnitude. Read powers in the nW regime were realized with junctions of relatively large area. The power consumption of a junction is expected to decrease when it is scaled down to the nanometer regime. The resistive switching showed no permanent degradation during a sequence of 100 switching cycles and showed no signs of fatigue over subsequent measurements. Time was identified as an important parameter governing the setting of the LRS. The retention time of the LRS was seen to increase upon increasing the time of a presented voltage stimulus in a fashion similar to the processes of learning and forgetting in the human brain.

SUPPLEMENTARY MATERIAL

See supplementary material for measurements performed on other junctions and fits used to estimate Schottky barrier heights and ideality factors.

ACKNOWLEDGMENTS

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