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Tunable doping in PbS nanocrystal field-effect transistors using surface molecular dipoles

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We study the effect of self-assembled monolayer (SAM) treatment of the SiO_2 dielectric on the electrical characteristics of PbS transistors. Using SAMs, we observe threshold voltage shifts in the electron transport, allowing us to tune the electrical properties of the devices depending on the SAM molecule used. Moreover, the use of a specific SAM improves the charge carrier mobility in the devices by a factor of three, which is attributed to the reduced interface traps due to passivated silanol on the SiO_2 surface. These reduced traps confirm that the voltage shifts are not caused by the trap states induced by the SAMs. © *2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* [http://dx.doi.org/10.1063/1.4966208]

The need for electronic devices, which can be produced at low cost and with low energy consumption, has led to an increasing attention to solution-processed materials. One of the most promising classes of these materials is colloidal nanocrystals (CNCs) due to their size-tunable band gap, simple synthesis, and easy control.[1–9] Because of their interest for solar cell fabrication and the high quality of the synthesized material, PbS NCs are one of the most intensively studied semiconductors in colloidal form. Many efforts have also been made to utilize PbS CNCs for field-effect transistors (FETs).[10–16] The FETs based on this material offer ambipolar transport,[10–12,14–17] which is prospective for light-emitting device applications.[18–20] However, their use is still challenging because of the limited charge carrier mobility determined by the high density of charge carrier traps in the active material. As interfacial devices, dangling bonds on the oxide gate dielectric further hamper the charge carrier mobility in FETs based on this material.[12] This, in turn, becomes an obstacle to understand the charge carrier transport in this material, which is essential to broaden their applicability.

Increasing carrier concentration through doping is used to improve film conductivity as well as charge carrier mobility in different types of semiconductors. This effort has been widely performed in organic FETs, whereas doping in colloidal nanocrystals is generally attempted by exploiting different ligands.[3,7,8,10,13–16,21–27] Heavy doping in lead chalcogenide nanocrystals using donor molecules, such as cobaltocene ($CoCp_2$), has also been investigated.[28] Doping with these donor molecules has enabled strong n-type transport in electronic devices. However, these heavily doped PbS

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NCs resulted in FET devices that always turned-on with consequent low current modulation, which is an undesirable property for an electronic device application. Therefore, light doping of the active material is preferred.

Molecular dipoles, well known as self-assembled monolayers (SAMs), have been widely used to achieve light doping in organic FETs. This light doping is a consequence of the energy level bending due to the modulation of interfacial carrier concentration induced by the SAM molecules. Due to this modulation, the molecules affect the threshold voltage of devices, allowing the control of charge carrier density as well as the device operation.[29–33] In addition, the use of SAMs can modify the surface properties of the oxide gate dielectric, which influence the morphology of the deposited films. Furthermore, these SAMs are able to passivate the dangling bonds on the surface of the oxide dielectric, thus reducing the interface traps, leading to improved charge carrier mobility.[29] Therefore, using SAM treatments as a doping strategy in FETs is very promising to realize high performance devices with controllable operation. These effects have so far been widely studied in organic semiconductors, while the investigation of SAMs in PbS CNCs FETs is still limited. This leaves many unsolved questions about the possibility to improve the performance as well as to influence the electrical characteristics of the CNC FETs using SAMs.

In this letter, we present a study on the effect of SAM surface treatment of the SiO_2 gate dielectric on the electrical characteristics of PbS NC-FETs. Upon the application of SAMs, we observed threshold voltage shifts indicating electron or hole doping introduced by the molecular dipole on the dielectric surface. We observed obvious relationship between the threshold voltage of the devices and the doping concentration induced by the SAM molecules, giving us the opportunity to tune the FET properties towards n- or p-type depending on the SAM molecules. The use of SAMs also allows reducing the density of traps in the device by passivating the dielectric interface, leading to improved electron mobility up to a factor of three. This light doping strategy through SAM treatment is promising in controlling the electrical characteristics and improving charge carrier mobility in PbS NCs FET devices.

To fabricate PbS NC-FETs, we used a heavily n-doped silicon substrate covered by a thermally grown 200 nm thick SiO_2 layer. Before use, the substrates were cleaned with acetone and isopropanol for 10 min, respectively. The substrates were then dried at 120 °C to remove the residual solvents. Six different SAM molecules, namely, hexamethyldisilazane/HMDS, hereinafter referred to as (A), *n*-octyltriethoxysilane/OTS (B), trimethoxy(2-phenylethyl)silane/PEMS (C), trichlorophenetylsilane/β-PTS (D), 3-(mercaptopropyl)trimethoxysilane/MPMS (E), and dodecyltrichlorosilane/DTS (F) were used to functionalize the SiO_2 surface. The molecular structures of the SAMs are shown in Fig. 1(a). The treatment with SAM A was done by soaking the substrates in SAM A for 1 min followed by spin coating at 1000 rpm for 1 min (drying). For the treatment

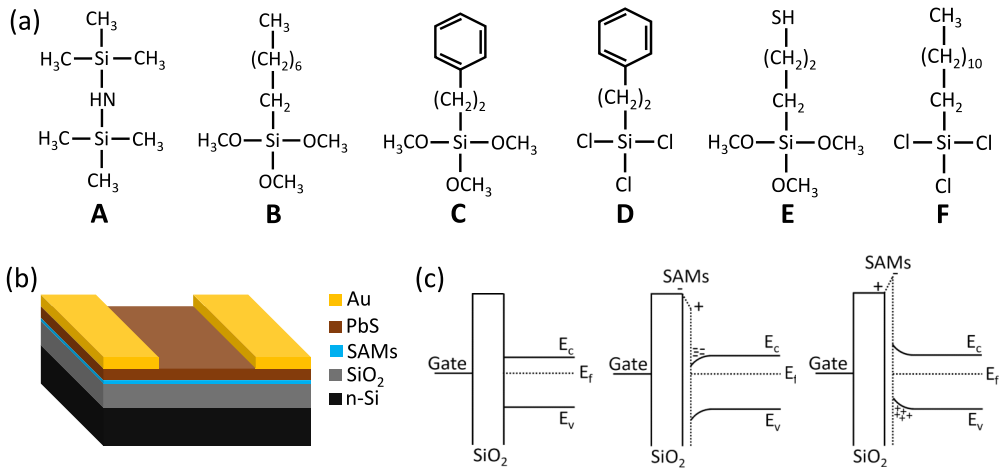

FIG. 1. (a) Molecular structure of the SAMs. (b) Configuration of PbS FETs. (c) Schematic of energy band diagrams for PbS FETs with untreated SiO_2 (left) and SAM-treated SiO_2 (middle and right) at zero gate voltage.

with SAM B-E, the substrates were immersed in the corresponding SAM solution (20 μl of SAM molecules in 10 ml of toluene) for 48 h. The last SAM F treatment was done using vapor deposition at atmospheric pressure obtained by placing the SAM inside a Teflon container at 120 °C for 3 h. To remove the excess of unbound SAM molecules, the substrates were cleaned with acetone and isopropanol for 5 min, respectively. Finally, the substrates were dried at 120 °C to remove the residual solvents as well as to promote a stronger bonding between the SAM molecules and the SiO_2 surface. The deposition of PbS NC films (diameter of 3.6 nm) from 10 mg/ml of oleic acid stabilized-NC solution in chloroform on the previously SAM-treated substrates was done using spin casting. To improve the conductivity of the films, the long-alkyl chain ligands were exchanged by shorter organic molecules, namely, 1,2-ethanedithiol (EDT), with a concentration of 1% (v/v) in acetonitrile. The film deposition as well as the ligand exchange (LE) was done using layer-by-layer (LbL) spin coating method repeated for five times to ensure the complete LE process, similarly to what has been previously reported.[12] After each LE step, we cleaned the samples with acetonitrile to favor the removal of the exchanged native oleic acid ligands. The devices were then annealed at 120 °C for 20 min to remove residual solvents. Finally, Au with thickness of 50 nm was evaporated as a source-drain electrode defining the channel length and width of 50 μm and 2 mm, respectively. All the device fabrication was performed in an N_2-filled glove box.

To ensure that the SAM molecules influence the semiconductor/insulator interfaces only, we used a top contact device structure as shown in Fig. 1(b). In this way, we minimize the effect of SAMs on the work function of the source-drain electrodes. The insertion of the SAM layer between the semiconductor and the dielectric films does not significantly change the total series capacitance due to higher capacitance of the SAM layer than that of the SiO_2 gate dielectric. After the deposition of the semiconductor film on the SiO_2 dielectric, the Fermi level of the semiconductor is aligned with the work function (Fermi level) of gate electrode as described in Fig. 1(c). The treatment of the SiO_2 surface with SAMs introduces dipoles at the surface which allow the bending of the energy levels of the semiconductor up or down, leading to hole or electron accumulation depending on the polarity of the SAMs as displayed in Fig. 1(c). This accumulation of carriers without applying a gate voltage appears as a carrier doping in the devices, which therefore influences the electrical characteristics of the devices.

As first, AFM measurements on the PbS films were performed to verify the effect of the SAMs on the PbS morphology. Because the first PbS layer has direct contact with the SAM-treated SiO_2 surfaces, the AFM images were only taken for this first layer (see supplementary material). We found that the use of SAMs on the SiO_2 surface generally promotes a better particle organization as demonstrated by the improved surface roughness in all films, with the exception of the DTS-treated surfaces. These results are in line with our previous report using PbS NCs capped with 3-mercaptopropionic acid (3MPA) ligands.[12]

To investigate the effect of the SAM surface treatment of the gate insulator on the electrical characteristics of PbS NC-FETs, we first performed the electrical characterization of the devices without any surface treatment in an N_2-filled glove box. The transfer characteristics of the PbS NC-FETs in the n-channel operation without surface treatment are shown in Fig. 2(a). The devices

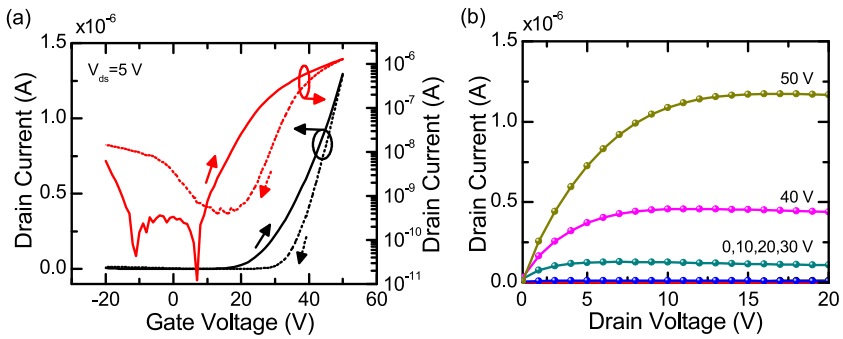

FIG. 2. (a) $I_D - V_G$ transfer characteristics and (b) $I_D - V_D$ output characteristics of pristine PbS FETs.

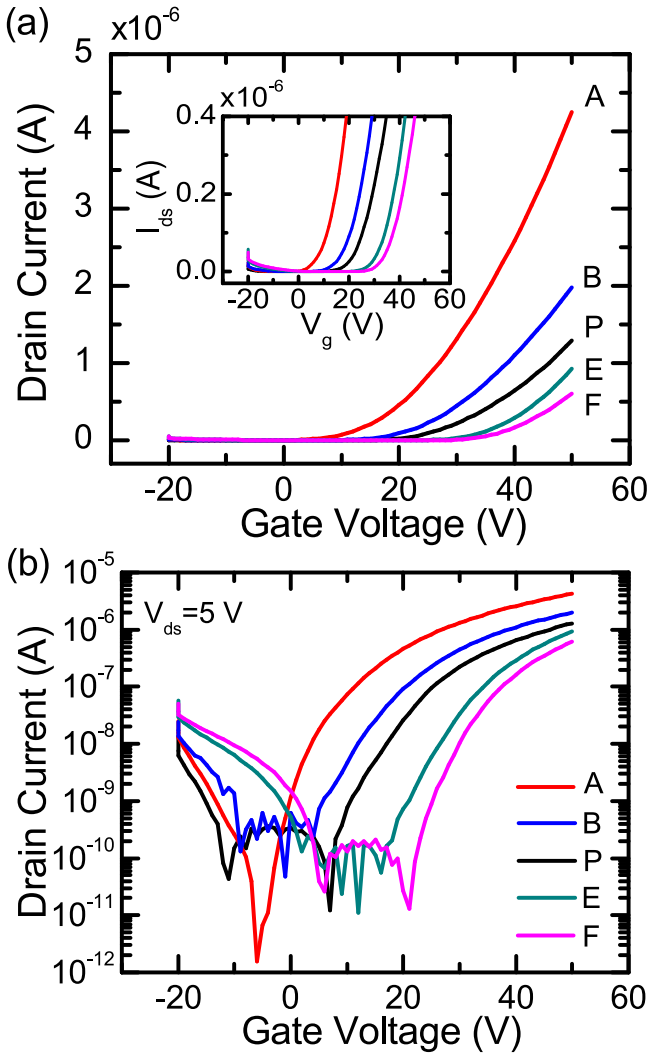

FIG. 3. $I_D - V_G$ transfer characteristics of PbS FETs after various SAM surface treatments on the SiO_2 surface in (a) linear and (b) semi-logarithmic scales.

show pronounced n-type properties with a extracted linear electron mobility of 0.02 $cm^2\ V^{-1}\ s^{-1}$ and a high current modulation of 10^4. The electron mobility is calculated from the forward sweep of the transfer curve, which means that the extracted values do not overestimate the real value of the mobility. In the semi-logarithmic profile of the transfer characteristics, we also observed slight hole current. Here we will focus on the electron transport properties to investigate the effect of the SAM surface treatment of the SiO_2 gate dielectric, since the hole current in the devices is much lower than the electron current. The hole transport in the devices is also influenced by the stoichiometry of the CNCs and by the much higher hole trap density with respect to the electron trap density, which may result in the uncertainty of the doping effect.[12] We then calculated the threshold voltage of the devices as one of the main parameters to investigate the effect of doping using the SAM surface treatment. To extract the threshold voltage (V_{th}) we used following equation for the linear region:

$$I_{ds} = \frac{\mu_{lin} C_{ox} W V_{ds}}{L}\left(V_g - V_{th} - \frac{V_{ds}}{2}\right), \tag{1}$$

where μ_{lin}, W, and L are the linear mobility, the channel width, and channel length, respectively. The SiO_2 gate dielectric with thickness of 200 nm defines the oxide capacitance (C_{ox}) of 17.3 nF/cm^2. By estimating the intercept of the current voltage curve in the x-axis, the threshold

voltage of the devices is calculated to be 29 V. To confirm that the devices are in linear regime at the applied source-drain voltage (V_{ds}), the output characteristics of the devices are displayed in Fig. 2(b). From the measurements, it is clear that the devices show both clear linear and saturation regime with no indication of contact limitation.

The transfer characteristics of PbS NC-FETs in the linear scale on different SAM-treated SiO_2 surfaces are shown in Fig. 3(a). The characteristics of the devices fabricated on pristine SiO_2 are shown in black line and indicated by "P". Using the SAM treated substrates, we are able to improve as well as tune the source-drain current of the devices. The treatment of the SiO_2 gate insulator using SAM A shows the highest current and the highest mobility among the tested SAMs. In addition, the SAM surface treatment of the SiO_2 gate dielectric influences the threshold voltage characteristics of the devices. The inset of Fig. 3(a) shows the effect of the SAM surface treatment on the threshold voltage of the devices. By the application of SAM A and B, the threshold voltages are shifted towards more negative values indicating electron doping (relative to the devices fabricated on the pristine SiO_2 surface). This negatively shifted threshold voltages are also observed in devices treated with SAM C (see supplementary material). Instead, the threshold voltage shifts towards more positive voltages when the substrate is treated with SAM D, E, and F. The transfer curves of devices treated with SAM D are shown in the supplementary material. Importantly, we observed similar behavior in more than 3 devices for each SAM which confirms the reproducibility. According to these results, the SAM treatment strategy allows us to tune the electrical characteristics of PbS NC-FETs through electron or hole doping, depending on the SAM molecules utilized.

At this point, it is interesting to quantify the doping strength induced by the SAM molecules, which corresponds to the concentration of electron and hole doping in devices. To estimate this electron and hole doping, we can refer to the semi-logarithmic profile of the device transfer characteristics. Fig. 3(b) shows in semi-logarithmic scale the transfer characteristics of PbS NC-FETs fabricated on different SAM-treated SiO_2 surfaces. We observed an obvious variation of the on-voltage (V_{on}) of devices using different SAM treatments. The V_{on} can be calculated from the gate voltage where the source-drain current starts increasing exponentially. This voltage enables us to calculate the electron and hole doping concentrations in the devices after the SAM surface treatment using the equation $N_{SAMs} = C_{ox}\Delta V_{on}/e$, where ΔV_{on} is the shift of on-voltage by SAM treatment.[29] Table I shows the doping concentration of electron and hole in devices with different SAM treatments of the SiO_2 gate dielectric. A negative value of the doping concentration corresponds to electron doping, while a positive value indicates hole doping. Furthermore, the doping concentration is also related to the dipole moments induced by the SAM molecules. The dipole moments and their direction are given in Table I and supplementary material. The negative dipole moments correspond to their downward direction, which favors more electron doping, thus negative doping concentration. Meanwhile, upward direction is shown by their positive values, which promote hole doping. Interestingly, we observed a peculiar result with SAM B in which electron doping is resulted by a positive dipole moment. In addition, we also did not find a monotonic trend between the magnitude of dipole moment and the number of carrier concentration at a specific type of carrier doping. These results can be attributed to the arrangement of the SAM molecules on the SiO_2 surface. It is important to note that the arrangement of the SAMs as well as their orientation on

TABLE I. Charge carrier doping concentration and the density of interface traps on different SAM treatments.

SAMs	Molecules	N_{SAMs} (10^{12} cm^{-2})	Dipole moment (D)	D_{it} (10^{12} eV^{-1} cm^{-2})
P	Pristine	...	...	11.6
A	Hexamethyldisilazane	−1.1	−0.98	4.9
B	*n*-octyltriethoxysilane	−0.54	3.03	10.2
C	Trimethoxy(2-phenylethyl)silane	−0.33	−1.74	9.0
D	Trichlorophenetylsilane	0.76	0.41	9.8
E	3-(mercaptopropyl)trimethoxysilane	0.97	1.21	10
F	Dodecyltrichlorosilane	1.5	0.91	7.4

the SiO_2 surface is very crucial to determine the effective magnitude of dipole moments as well as the type of charge carrier doping.

As we compare Figs. 3(a) and 3(b), the variation in the V_{on}, thus in doping concentrations, is interestingly followed by the threshold voltage shift in the same direction. It further shows that the

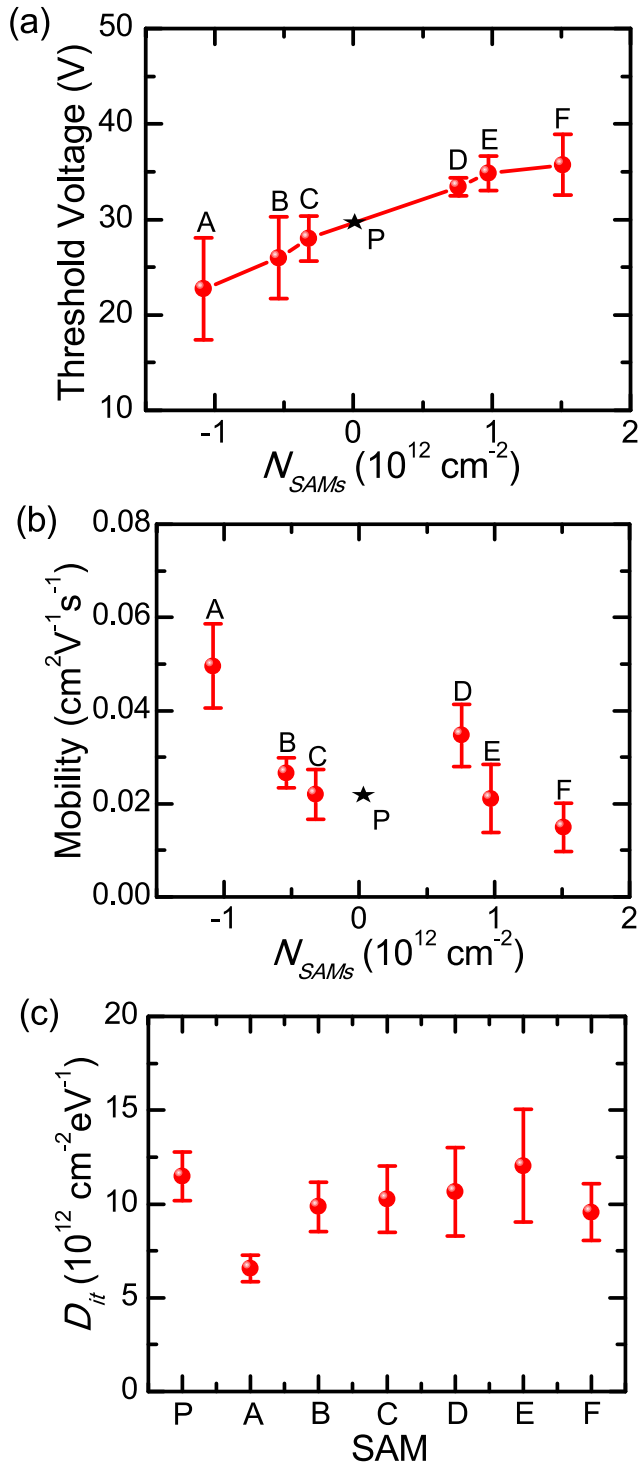

FIG. 4. The characteristics of (a) threshold voltage for electron accumulation and, (b) electron mobility as a function of doping density induced by SAMs. (c) The density of deep traps in PbS FETs with various SAM-treated SiO_2 surfaces.

charges induced by the SAM molecules are at the origin of the shifted transfer characteristics. To confirm this, we investigate the relationship between the threshold voltage of the devices and the doping concentrations of SAMs as shown in Fig. 4(a). Obviously, the SAM doping concentrations display a linear relationship with the threshold voltage of the devices. The deposition of the SAM thin layer builds a series capacitance with respect to the capacitance of the oxide gate dielectrics which induces a threshold voltage shift that can be described as follows:

$$\Delta V_{th} = \frac{C_i + C_{SAMs}}{C_i C_{SAMs}} e N_{SAMs} \approx \frac{e N_{SAMs}}{C_i}. \tag{2}$$

According to Eq. (2), the inverse gradient of the curve in Fig. 4(a) corresponds to the capacitance of the SiO_2 gate dielectrics. From Fig. 4(a), we calculated the gradient of the curve to be 5.2×10^{-12} V cm^2, which corresponds to the gate dielectric capacitance of 31.1 nF/cm^2. This calculated value of the capacitance shows a substantial deviation from the one of the actual gate dielectrics used in the devices, 17.3 nF/cm^2. This deviation may come from an underestimation of the calculated V_{th}, particularly in the devices with the characteristics shifted towards the right direction, as we refer to Fig. 3(a). The V_{th} value can be extracted at different charge carrier densities, which may result in the error in V_{th} extraction.

This doping strategy using SAMs also allows influencing the charge carrier mobility in the devices. Fig. 4(b) displays the electron mobility in the linear regime obtained using different SAM surface treatments. The electron mobility increases with the increase of the electron doping concentration. We also observed that the electron mobility tends to decrease as the hole doping concentration increases with the exception of the devices treated with SAM D. In this condition, holes in the devices reduce the film conductivity, which results in the decrease of electron mobility. This could be explained with the recombination of holes and electrons, which gives rise to light emission.[34,35] In organic FETs, organosilanes have been indicated to induce additional traps further reducing the charge carrier mobility.[29,33] Therefore, to confirm that the decrease of electron mobility is caused by hole doping and not by the additional traps, we quantify the trap density (D_{it}) in our devices using following equation:

$$D_{it} = \left(S \frac{e}{k_B T \ln 10} - 1 \right) \frac{C_i}{e^2}, \tag{3}$$

where S, e, and k_B are the subthreshold swing, the elementary charge, and the Boltzmann constant, respectively. The density of traps in the devices using different surface treatment is shown in Fig. 4(c) and Table I. The use of SAMs on the SiO_2 gate dielectric reduces the density of electron traps in the devices, which is in agreement with the fact that the SAM molecules passivate the dangling bonds on the SiO_2 surface. Therefore, the use of SAMs does not induce additional traps in our devices, confirming that the decrease of the electron mobility, particularly in the devices treated with SAM E and F, originates from an increase of the hole current. Furthermore, we observed the reduction of the density of traps by almost a factor of three using SAM A, which may also contribute to the highest electron mobility in these devices. Importantly, the improvement of the carrier mobility in our devices is not as high as in the case of organic single crystals such as rubrene. In rubrene transistors, the trap density in the material is very low. Hence, small doping level induced by the SAM molecules will have a great impact on the mobility of the charge carriers. Meanwhile, the trap density in PbS FETs is rather high (1.2×10^{13} eV^{-1} cm^{-2}). Because of this high trap density, the improvement of the mobility in the devices is very reasonable considering the doping level given by the SAMs.

In conclusion, we have performed experiments to unravel the effect of SAM treatment of the SiO_2 gate dielectrics on the electrical characteristics of PbS NC-FETs. The use of SAM results in the threshold voltage shifts by inducing electron and hole doping in the devices. We found a clear relationship between the threshold voltages and the doping concentration induced by SAMs, allowing us to tune the electrical characteristics of PbS NC-FETs. The use of SAMs is also able to improve electron mobility by a factor of three, which is attributed to higher electron doping as well as lower interface traps than in devices fabricated on untreated SiO_2 surfaces. Hole doping results in

a decrease of the electron concentration, probably due to the recombination of the electron and hole population.

See supplementary material for the AFM images of the semiconducting films, further details of the transfer characteristics, and schematic of dipole moments at the dielectric interface.

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