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# A multi-dimensional model of passive MESFETS for use in non-linear microwave signal processing

Roger Dorval
*New Jersey Institute of Technology*

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# ABSTRACT

## A MULTI-DIMENSIONAL MODEL OF PASSIVE MESFETS FOR USE IN NON-LINEAR MICROWAVE SIGNAL PROCESSING

by
Roger Dorval

A multi-dimensional model which accurately predicts device non-linearities over frequency and power has been developed for MESFETs used in a passive configuration in microwave signal processing applications.

Historically, MESFETs have been used in linear control applications as passive microwave switches and attenuators. More recently, MESFETs operated as passive elements have been employed as power-sensitive non-linear transfer function generators to produce limiters, phase shifters, and linearizers. These devices offer simplicity, high performance, and the opportunity for application in MMIC technology.

This thesis deals with a mapping of passive MESFET non-linear characteristics, and provides insight into the causes of non-linearity in MESFETs when operated as control elements at near zero drain voltage. Five unique operating modes are identified, and discussed in terms of their equivalent circuit models.

This work also deals with computer aided model extraction and non-linear simulation of MESFET characteristics, and presents a multi-dimensional lumped element model which accurately predicts device non-linearity over a wide range of power (-35 to > 10 dBm) and frequency (.1 to > 18 GHz). The application of this model to the design of a traveling wave tube amplifier (TWTA) linearizer is demonstrated. The model allows linearized TWTA transfer characteristics and two-tone carrier-to-intermodulation (C/I) performance to be predicted using standard CAD software.

# A MULTI-DIMENSIONAL MODEL OF PASSIVE MESFETS FOR USE IN NON-LINEAR MICROWAVE SIGNAL PROCESSING

by
Roger Dorval

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## APPROVAL PAGE

# A MULTI-DIMENSIONAL MODEL OF PASSIVE MESFETS FOR USE IN NON-LINEAR MICROWAVE SIGNAL PROCESSING

**Roger Dorval**

Dr. Allen Katz, Thesis Adviser — Date
Professor of Electrical Engineering, Trenton State College

Dr. Gerald Whitman, Faculty Thesis Adviser — Date
Professor of Electrical Engineering, NJIT

Dr. Edip Niver, Committee Member — Date
Professor of Electrical Engineering, NJIT

# BIOGRAPHICAL SKETCH

**Author:** Roger Dorval

**Degree:** Master of Science in Electrical E Engineering

**Date:** May 1994

**Undergraduate and Graduate Education:**

- Master of Science in Electrical Engineering,
  New Jersey Institute of Technology, Newark, NJ, 1994
- Bachelor of Science in Electrical Engineering Technology,
  Trenton State College, Trenton, NJ, 1991

**Major:** Electrical Engineering

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# CHAPTER 1

## INTRODUCTION

The ability to generate non-linear transfer functions (Power-in vs. Power-out) which can be tailored to desired magnitude and phase characteristics is important in many RF/ microwave applications. Principle among these applications are linearizers and limiters. Linearizers are used to reduce multi-tone intermodulation distortion caused by the non-linearities of active RF/microwave components such as amplifiers. Limiters are used to limit, or diminish, the maximum signal levels produced by RF/microwave systems and in some instances are required to provide a shaped response [1]. Non-linear transfer characteristics are also employed in microwave signal processing applications for the production of logarithmic amplifiers and similar devices.

Non-linear transfer functions have been commonly generated by driving amplifiers into their saturation region, or by making use of the change in impedance of diodes with power level. Neither of these methods allow the resultant gain and phase transfer characteristics to be readily modified so as to match a desired transfer response. Diodes, in particular, can display gross changes in characteristics as frequency is varied. The ability to maintain a specific transfer characteristic over a wide band of frequency is essential in many non-linear signal processing applications.

Non-linear components have been used in both transmissive and reflective networks. Each configuration has unique characteristics and between the two, a variety of non-linear characteristics can be generated. A transmissive and a reflective network is illustrated in Figures 1a and 1b, respectively, where the impedance, $Z_{nl}$, represents the non-linear component.

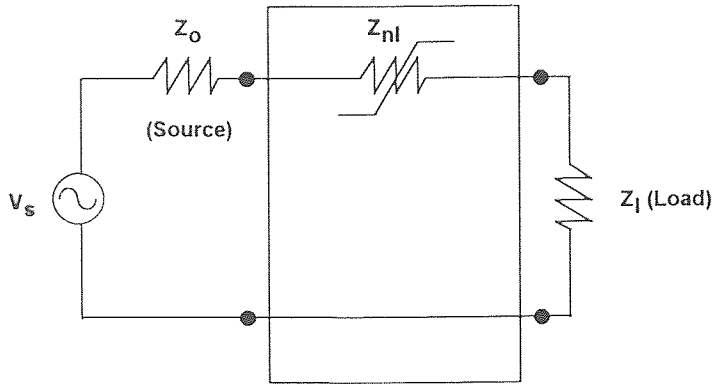


**Figure 1a** Transmissive Network

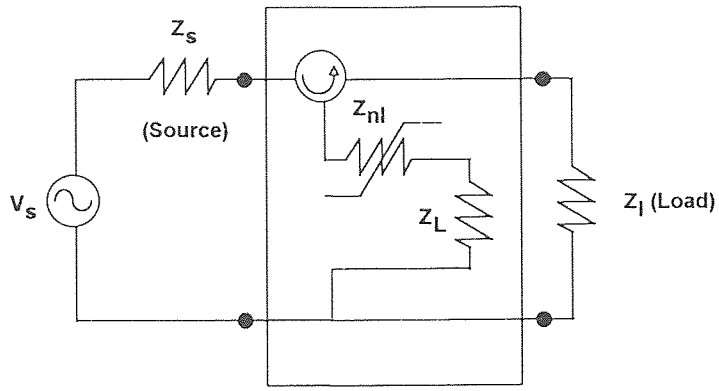


**Figure 1b** Reflective Network

The equation for transducer gain can be determined for each of the above networks using network analysis techniques. The simplified transmissive case is shown in Figure 1a. The network transducer gain, $S_{21}$, for a matched load (i.e. $Z_l = Z_o$), is related to the non-linear impedance, $Z_{nl}$, by Equation 1.

$$S_{21} = \frac{2Z_o}{Z_{nl} + 2Z_o} \tag{1}$$

If $|Z_{nl}| >> |Z_o|$, then $|S_{21}|$ becomes inversely related to $|Z_{nl}|$.

For the reflective case shown in Figure 1b, assuming an ideal circulator and a matched load, the transducer gain is given by Equation 2, where $\Gamma_n$ is the reflection coefficient of $Z_{nl} + Z_L$.

$$S_{21} = \Gamma_n = \frac{Z_{nl} + Z_L - Z_o}{Z_{nl} + Z_L + Z_o} \tag{2}$$

Using flow graph theory, $S_{21}$ can be related to the S-parameters of the $Z_{nl}$ network ($S_{nl}$) and $\Gamma_L$, the reflection coefficient of the internal impedance $Z_L$. This relation is given in Equation 3.

$$S_{21} = S_{nl11} + \frac{S_{nl21} S_{nl12} \Gamma_L}{1 - \Gamma_L S_{nl22}} \tag{3}$$

When $Z_L$ is totally reflective (i.e. $|\Gamma_L| = 1$), and $|S_{nl22}| << 1$, then the transducer gain is given by Equation 4.

$$S_{21} = S_{nl21} S_{nl12} \angle\Theta + S_{nl11} \tag{4}$$

Where $\theta$ is the angle associated with $\Gamma_L$. If $|S_{nl11}| << |S_{nl21}|$ and the network is bilateral, then Equation 5 holds true.

$$S_{21} = (S_{nl21})^2 \tag{5}$$

Under these conditions the transmissive characteristics of $Z_{nl}$ also establish its reflective characteristics. When $|S_{nl11}|$ is comparable to $|S_{nl21}|$, the angle of $\Gamma_L$ becomes critical, and a variety of reflective transfer characteristics can be established as a result of the addition or subtraction of $S_{nl21}$ and $S_{nl11}$.

# CHAPTER 2

## PASSIVE FET NON-LINEAR ELEMENT

GaAs MESFETs connected in a common gate configuration and operated as passive elements, with the drain and source at the same dc potential, are commonly used in microwave control applications to produce linear components such as switches and attenuators. In these control applications, the gate of the MESFET is connected to a high impedance, typically greater than 5 KΩ, and non-linearities in the power transfer characteristics are undesirable. When a MESFET is operated as a non-linear element (NLE), the gate is usually connected to ground through a relatively low impedance. The FET is operated essentially as a passive element with the impedance of the drain-to-source channel controlled by the gate field. Negligible dc power is consumed when operated in this way, since there is no drain-source supply. A basic NLE network is illustrated in Figure 2.

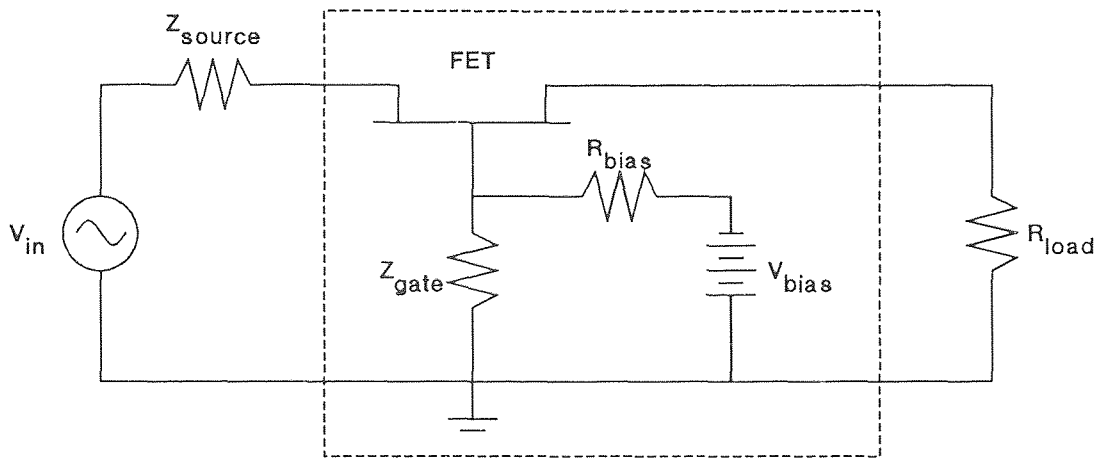


**Figure 2** Basic FET Non-Linear Element (NLE)

It was discovered that a GaAs MESFET, when connected as an NLE, can display both a significant change in input impedance, $S_{11}$, and transducer gain, $S_{21}$, with varying power level [2]. In the case of passive MMIC switches/attenuators, a change of input impedance or insertion loss with power level is undesirable. Where such changes have been observed, they have been reported as occurring at power levels greater than 10 dBm and attention has focused on minimizing these effects [3]. For the NLE, the onset of changes in input impedance and insertion loss has been observed at input powers below -25 dBm. This change can be readily tailored to produce a wide variety of responses in both magnitude and phase and is relatively insensitive to frequency variation. In general, $S_{11}$ is less sensitive to power level than $S_{21}$, however, a variety of input reflection coefficient responses are available by appropriate selection of $\Gamma_L$ as given by Equation 4. Input and output match as well as reverse and through transmission gain have almost identical characteristics, meaning the NLE acts as a bilateral, or symmetrical, network. NLE non-linear characteristics have been successfully employed to produce superior high power amplifier (HPA) linearizers, limiters, level sensitive switches, and other related devices [1,2].

The impedance properties of FET NLEs have been found to be easily altered by varying the gate parameters of the basic NLE network shown in Figure 2. Most important of these gate controls are the dc bias voltage and the RF impedance between the gate and ground. Depending on parameter values, it is possible to obtain an $S_{21}$ transfer function whose magnitude becomes either larger or smaller and whose phase angle either increases or decreases with increasing input power. A typical NLE transfer response usable for a linearizer is shown in Figures 3 and 4 as a function of frequency and input power, respectively.

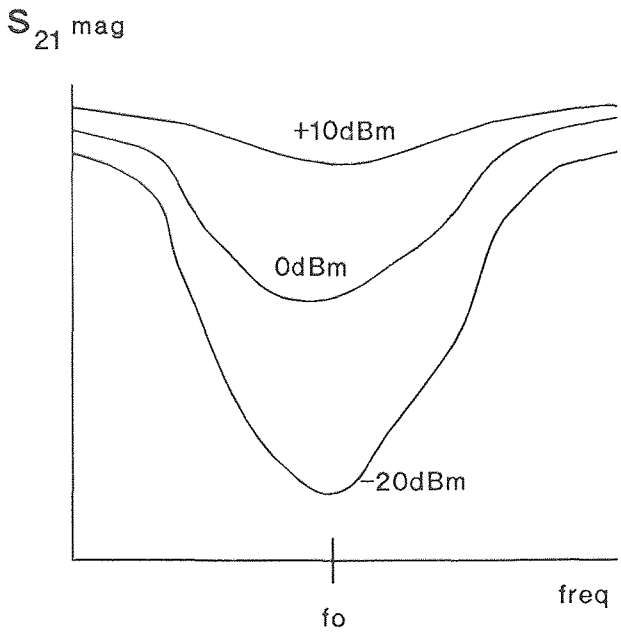


**Figure 3a** Typical NLE Gain Transfer Characteristics Versus Frequency

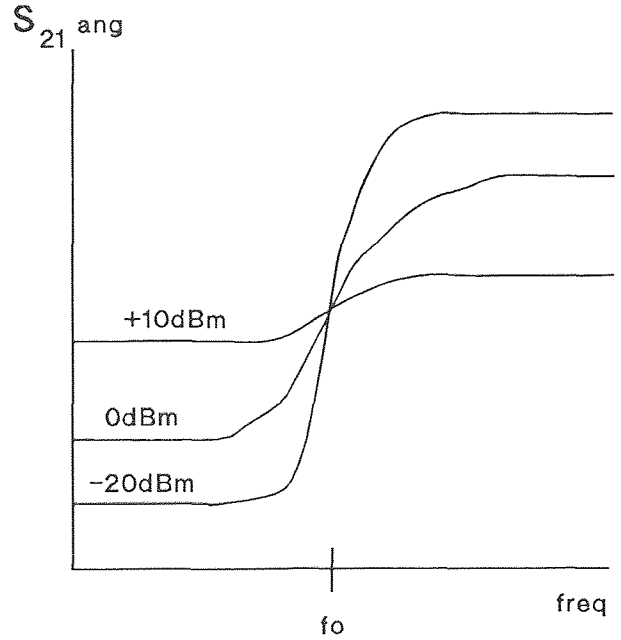


**Figure 3b** Typical NLE Phase Transfer Characteristics Versus Frequency

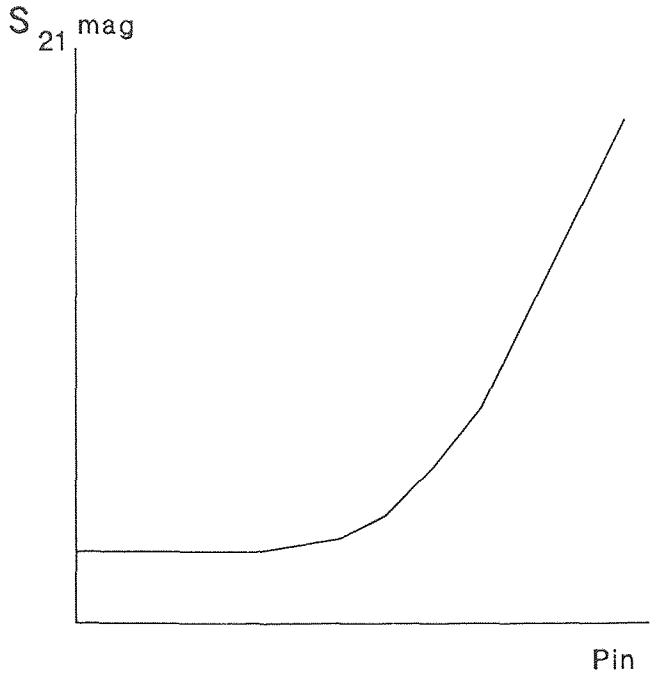


**Figure 4a** Typical NLE Gain Transfer Characteristics Versus Input Power

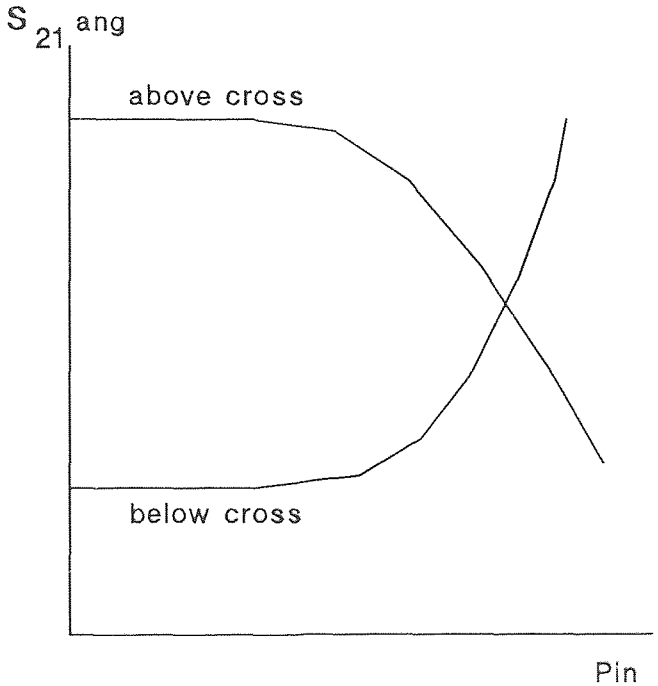


**Figure 4b** Typical NLE Phase Transfer Characteristics Versus Input Power

Figure 3a shows a null in the magnitude versus frequency characteristics of the forward transmission gain, $S_{21}$. As shown in the figure, the depth of the null decreases with increasing power level. This change corresponds to gain expansion, as illustrated in Figure 4a. Such a characteristic can be used to compensate for the non-linearity of an amplifier in the compression region near saturation. Coinciding in frequency with this null in the magnitude response is a phase crossing, as illustrated in Figure 3b. Below this crossing point, phase increases with increasing power level, and above this point, phase decreases with increasing power level. The change in phase with input power level is illustrated in Figure 4b. The useful bandwidth of this type of response is limited on the low frequency side by the point of transition from gain expansion to gain compression and on the high frequency side by the transition from an increasing phase angle to a decreasing phase angle with power level.

The location of the null center, the point of phase cross in frequency, and the shape of the magnitude and phase versus power characteristics are affected by input and output matching, external gate circuitry, and gate bias level. A desired non-linear response can be achieved by proper selection of these parameters.

# CHAPTER 3

# NLE MODES OF OPERATION

## 3.1 Operational Modes

Five distinct modes of FET NLE operation which are relatively insensitive to MESFET type and frequency band (up to at least 18 GHz) have been identified. These operational modes are established by the gate bias voltage. Each mode is defined in terms of a null in the magnitude response of the forward transmission gain of the NLE swept over frequency. The location of the null in frequency, the depth of the null, and the sensitivity to power level, depend on the gate bias voltage and impedance. A packaged MESFET, with its gate grounded, will produce a transmission null in the multi-GHz frequency range. The null of a chip device will be significantly higher in frequency. As the NLE is driven harder these nulls tend to disappear as previously illustrated in Figure 3. This action produces the expanding magnitude transfer response, shown in Figure 4. The phase characteristics are mode dependent and will also be affected by frequency and external gate circuitry.

## 3.2 Mode #1

The first mode identified, referred to as mode #1, occurs for gate voltages ranging from approximately +1 volt to -2 volts. The precise voltage range depends on MESFET type and, in the positive range of voltage, depends on the size of the gate isolation resistor, since the gate diode draws current when biased positive. At higher power levels, the dc gate current increases. This self biasing action may help to explain some of the NLE's non-linear characteristics. As gate voltage is reduced, the location of the null moves higher in frequency.

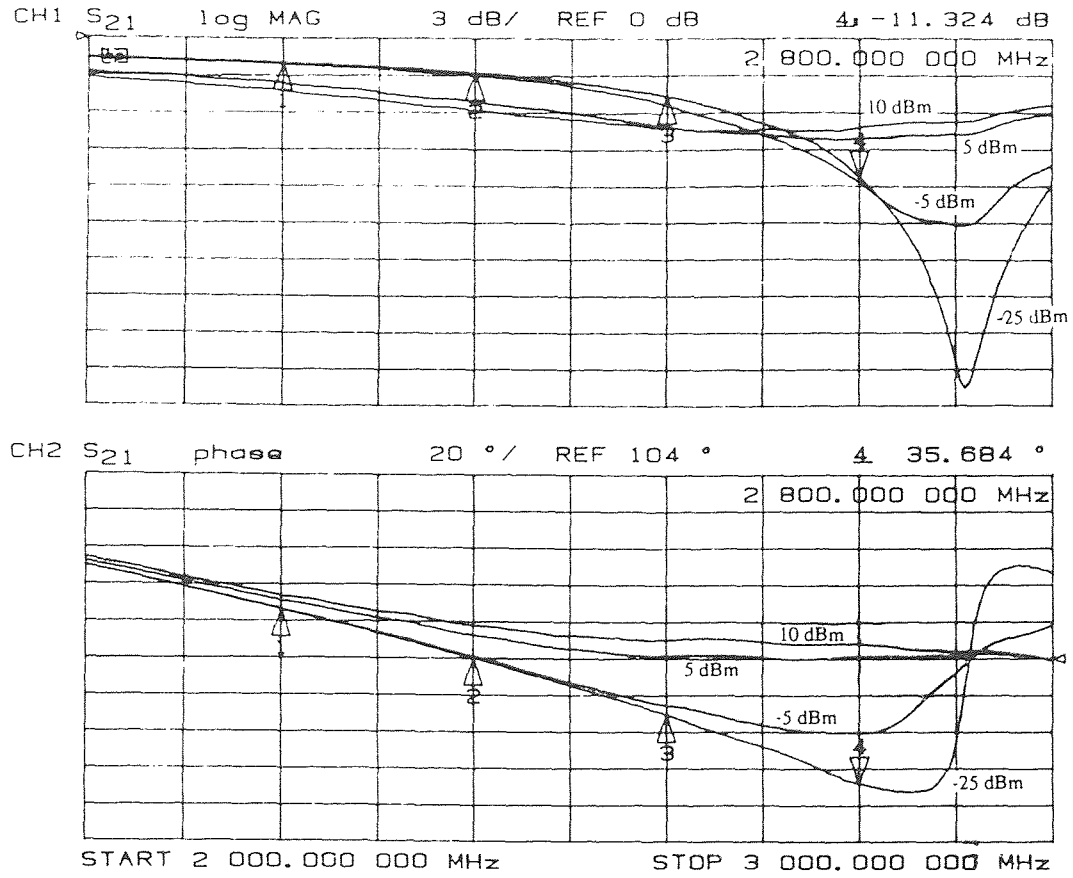


**Figure 5** Typical Gain and Phase Response of Mode #1

The response of a typical mode #1 null is illustrated in Figure 5. The response is that of an NE710 GaAs FET with a small inductance connecting the gate to ground through a dc blocking capacitor. A gain expansion, or reduction in loss, of greater than 12 dB and a phase angle change of more than 60 degrees can be achieved for a change in input level of 20 dB. Gain compression, which occurs at frequencies below the null, is limited to about 5 dB over the same power range. A point of zero phase change with power occurs at the frequency coinciding with the bottom of the null. Phase angle increases with increasing power at frequencies below this point, and phase angle decreases with increasing power at higher frequencies.

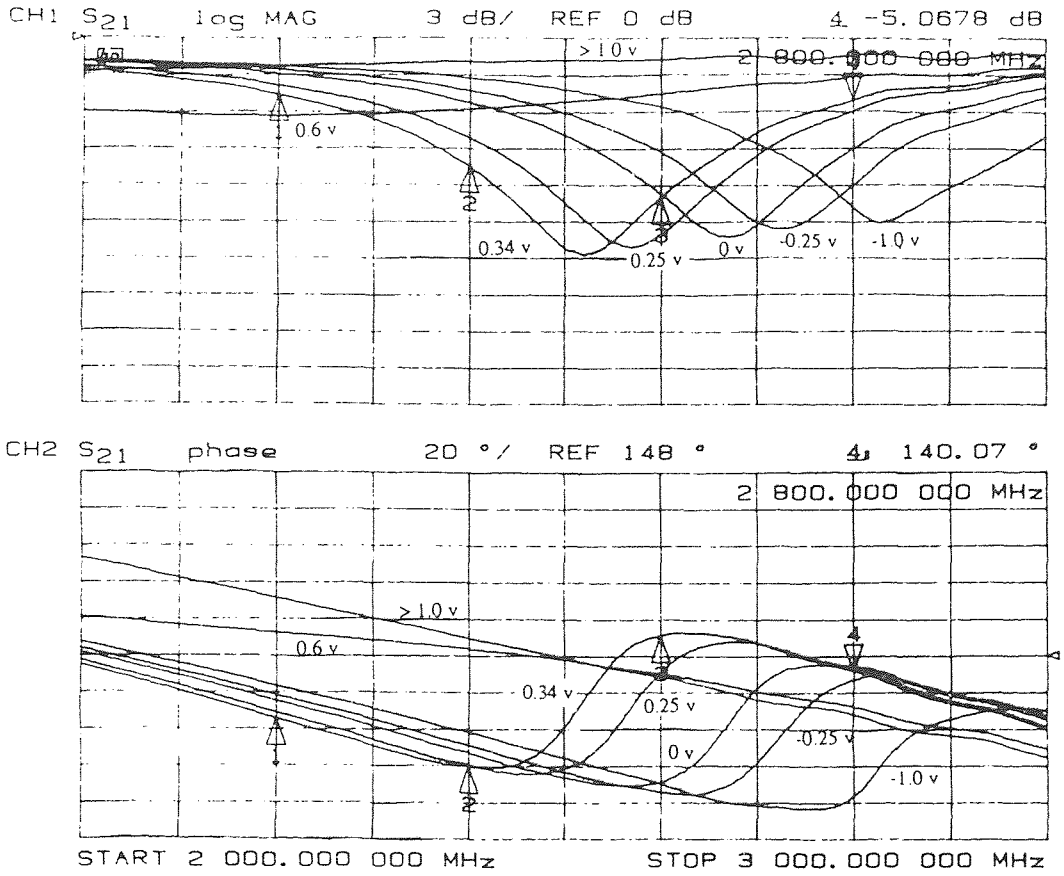


**Figure 6** Effect of Gate Bias on Mode #1 Null Versus Frequency

Figure 6 illustrates the effect of gate bias on the location of the null in frequency. The bias is varied from +0.6 volts to -1.0 volts. As the bias becomes more negative, the center of the null moves higher in frequency while the depth and shape of the null remain fairly constant. The corresponding phase cross associated with the null also moves higher in frequency as would be expected, and also maintains a fairly constant shape over the entire range of voltage. The ability to move the null frequency by varying the gate reactance is illustrated in Figure 7.

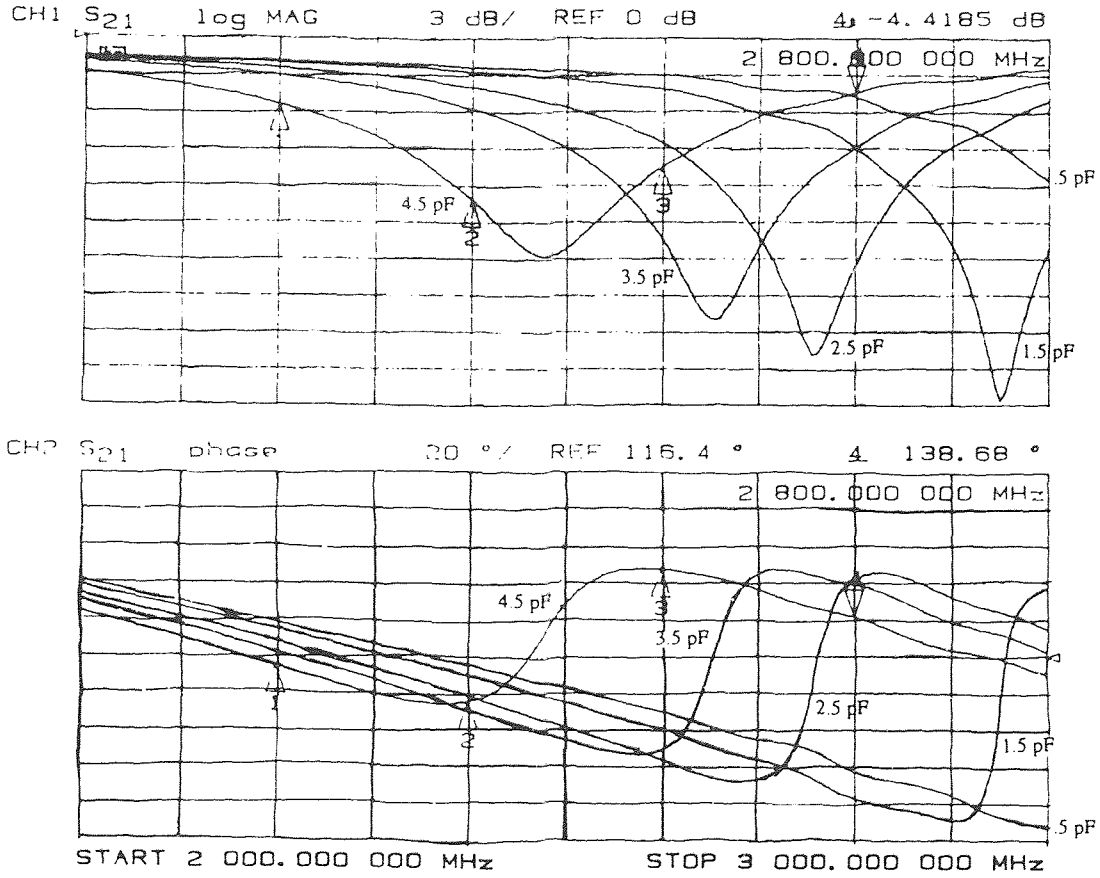


**Figure 7** Effect of Gate Reactance on Mode #1 Null Versus Frequency

Figure 7 shows the effect of varying the capacitance of a trimmer in the gate of an NLE from 4.5 pF to 0.5 pF with a small inductor of about 2 nH in series. The resistance of the source and drain dc return paths have negligible effect on this mode. The useful bandwidth of mode #1, for transmissive linearizer applications, is limited on the low side by the point of transition from expansion to compression and on the high side by the transition from an increasing phase angle to decreasing phase angle with power level.

The $S_{11}$ characteristics of mode #1 display an improvement in match over a broadband with increasing power level. By symmetry, the same holds true for $S_{22}$ characteristics. The magnitude of $S_{11}$ decreases by about 5 dB with increasing power as shown in Figure 8.

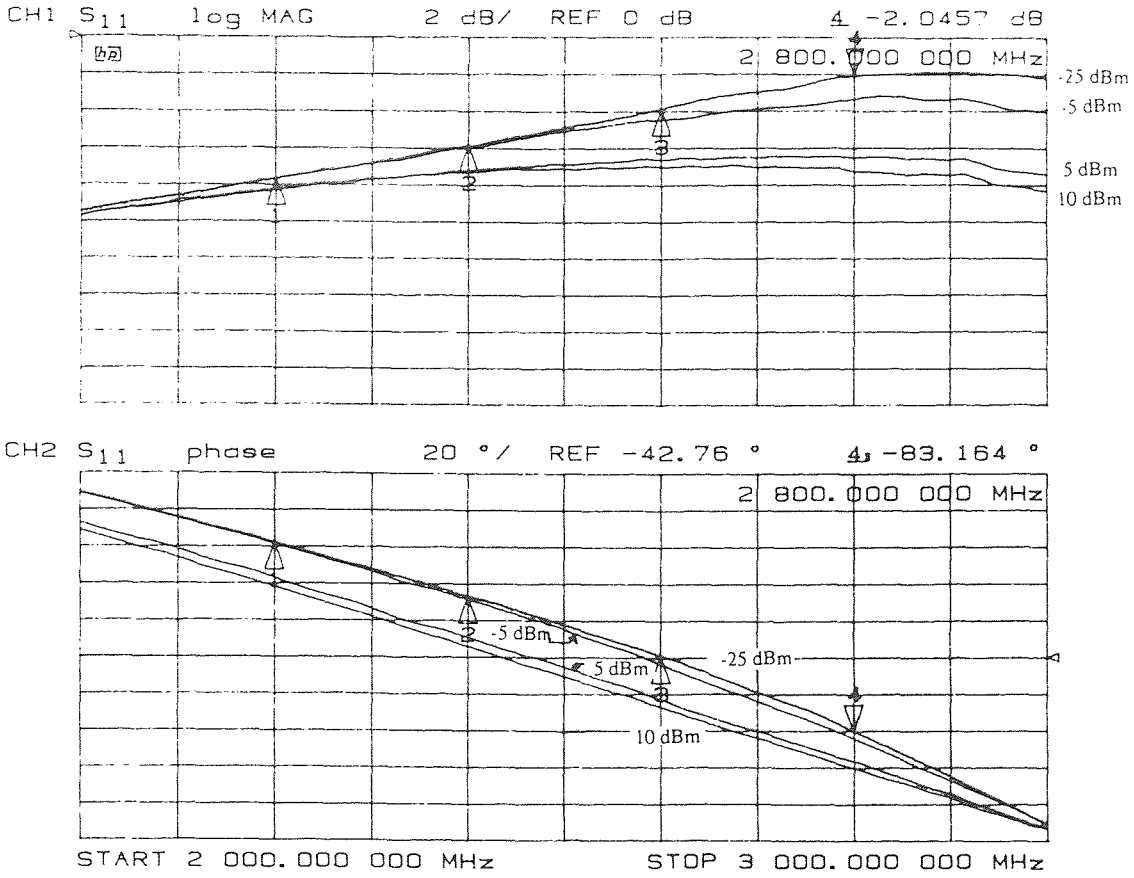


**Figure 8** Typical $S_{11}$ Characteristics of Mode #1

The phase angle of $S_{11}$ becomes negative with greater power level below the null center, and more positive above the center. This response can be altered greatly by terminating the NLE in a non-$Z_0$ load, and in this manner be tailored for use in reflective circuit applications as predicted by Equation 3.

### 3.3 Mode #2

A second operational mode, mode #2, occurs at a more negative gate voltage than mode #1 and over a relatively narrow voltage window of about 0.2 volts, just before the pinchoff voltage level. The attributes of this null are similar to, but more complex than those of mode #1, and depend on the gate bias ground return path at the source and drain terminals. Typically as the gate voltage is reduced, the center of this null moves lower in fre-

quency. If dc return paths are provided at both the input and output ports, the frequency point of zero phase angle change with power level takes place at or near the center of the transmission null. The phase angle decreases with increasing power level below the null center frequency, and increases with increasing power above this point. This facet as well as the change of null frequency with gate voltage are the opposite of mode #1.

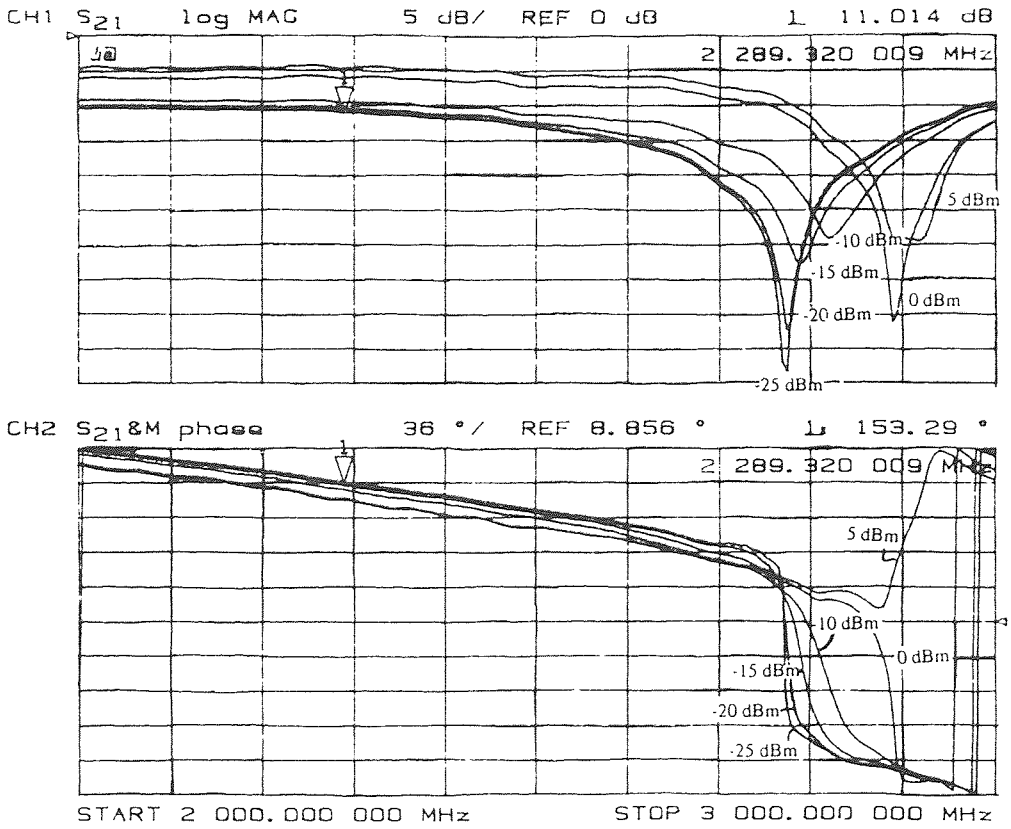


**Figure 9** Typical Gain and Phase Response of Mode #2

Mode #2 provides a very deep null, typically greater than 20 dB, and is the most sensitive to power level as demonstrated in Figure 9. A dynamic gain expansion of greater than 15 dB with a maximum slope on the order of 1 dB/dB can be achieved with a single FET. The point of maximum attenuation is usually associated with a large and steep change in phase. A mode #2 null can be also tuned to act as a limiter and produce a

deeper null with increased power. Greater than 20 dB of limiting can be achieved with a single mode #2 NLE. This property is illustrated in Figure 9 as well.

The $S_{11}$ characteristics of mode #2 normally display a broad null whose depth decreases, and phase angle increases, with increased power level as shown in Figure 10.

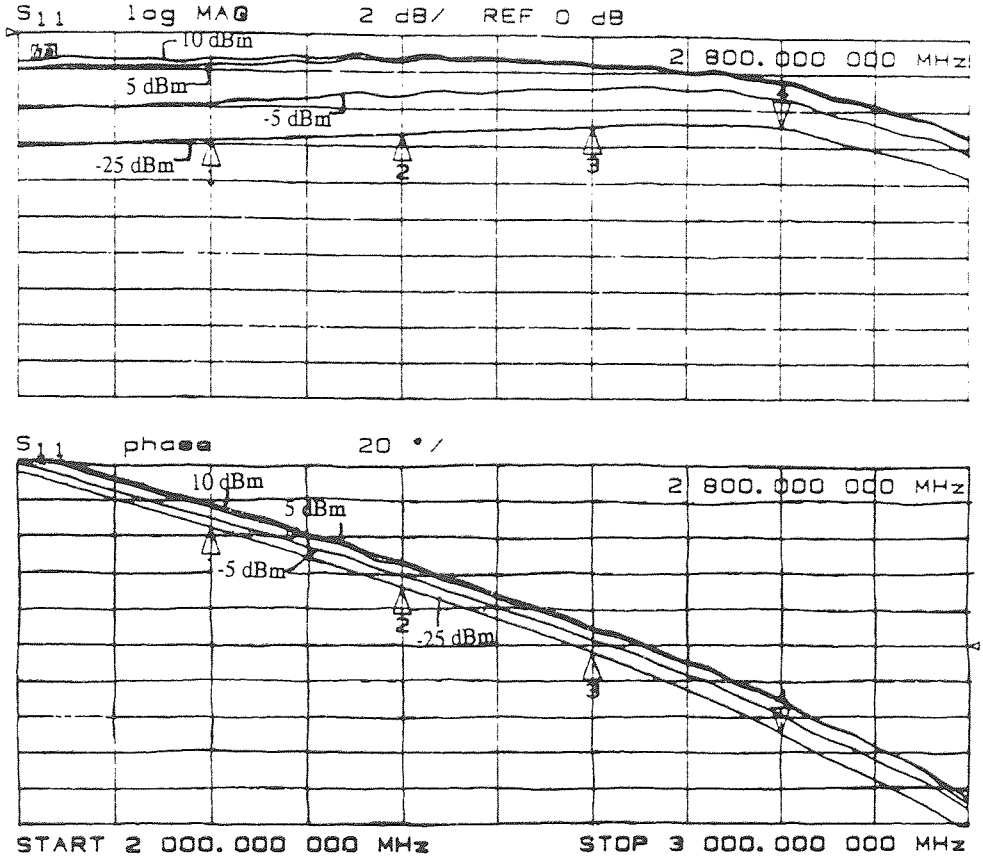


**Figure 10** Typical $S_{11}$ Characteristics of Mode #2

### 3.4 Mode #3

Decreasing the gate voltage further, typically Vg < -2.7 volts, produces a broad, deep null at frequencies less than 3 MHz, which is referred to as mode #3. At frequencies above 3 MHz, there is little sensitivity to power in either the magnitude or phase response of the forward transmission gain. A typical mode #3 response is shown in Figure 11.

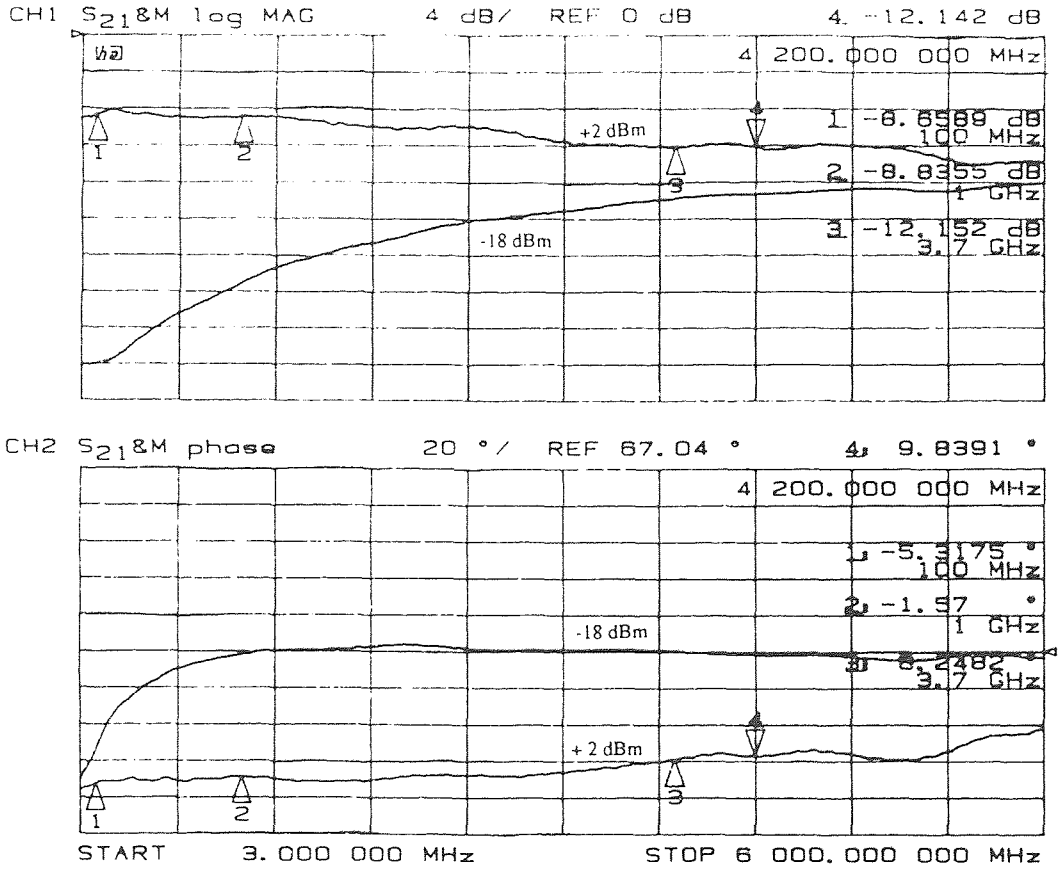


**Figure 11** Typical Gain and Phase Response of Mode #3

The above response was obtained from the same network used to produce the mode #1 and mode #2 response shown in Figures 5-10. However, for mode #3 operation, the gate impedance was reduced to move any residual mode #1 or mode #2 nulls above the frequency range shown.

Mode #3 can provide more than 10 dB of gain expansion with a maximum gain slope approaching 1 dB/dB, but only a phase angle change that decreases with increasing power level and which is relatively insensitive to the value of gate impedance. This mode is particularly useful for HF and VHF/UHF linearizer applications.

Mode #3 $S_{11}$ response displays a broad band increase in return loss of about 5 dB with increasing power. A small phase change, primarily in the negative direction, is seen with increasing power level. These characteristics are illustrated in Figure 12.

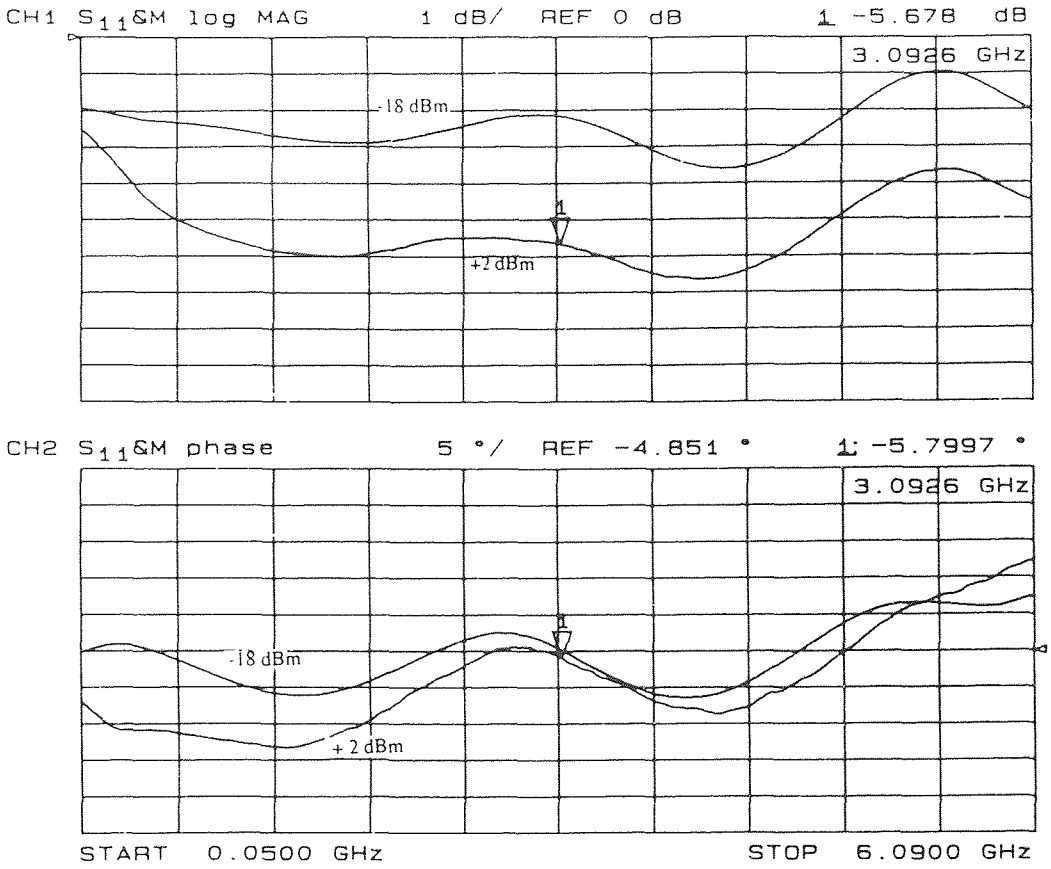


**Figure 12** Typical $S_{11}$ Characteristics of Mode #3

### 3.5 Broad-Band Mode

Setting the gate voltage to a level somewhere between the more negative end of mode #2 and the beginning of mode #3, yields a multiple decade broad-band mode. Uniform non-linear magnitude and phase characteristics are obtainable over several GHz range. A typical broad-band mode response is illustrated in Figure 13.

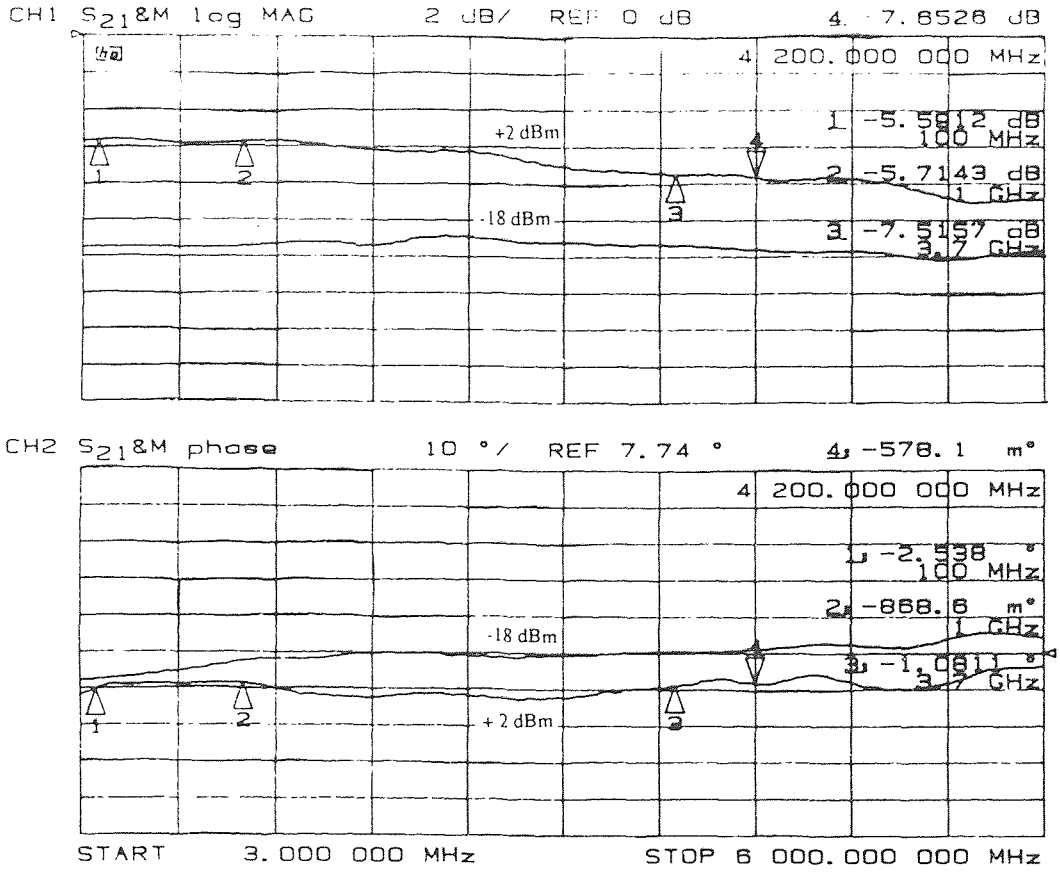


**Figure 13** Typical Gain and Phase Response of the Broad-Band Mode

Although the gain expansion and phase change with power of this mode are less than that provided by mode #1, #2, or #3 , they are still sufficient (> 6 dB) for many applications. One limitation of this mode as well as mode #3, is that the phase angle displays only a decrease with increasing power. The characteristics of the input reflection coefficient, $S_{11}$, shown by this mode are almost identical to those of mode #3, shown in Figure 12.

### 3.6 Mode #4

One additional mode, mode #4, has been classified. This mode occurs for a gate bias more positive than that of a mode #1. A typical mode #4 response is shown in Figure 14.

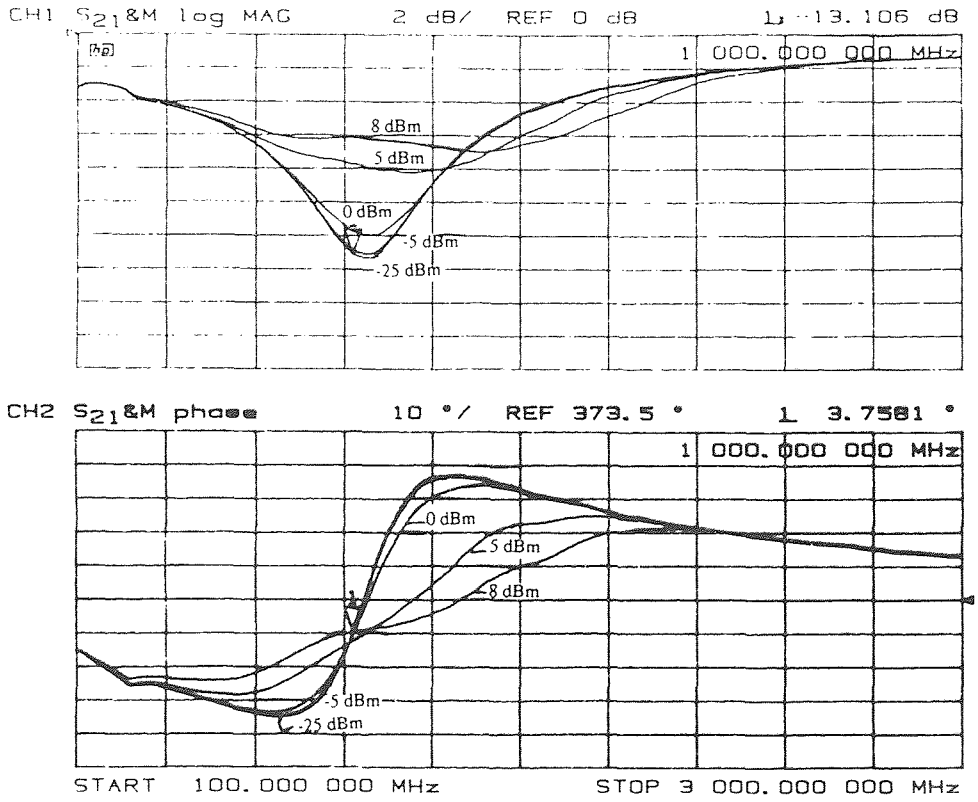


**Figure 14** Typical Gain and Phase Response of Mode #4

Mode #4 has characteristics very similar to mode #1 but the null occurs at a lower frequency for a given gate reactance. There is also considerable dc gate current because of the high forward gate bias. The decrease in phase angle with power level, which occurs above the null center frequency is commonly more pronounced than the increase in phase angle which occurs below the null center frequency.

The $S_{11}$ characteristics of mode #4 are similar to mode #1 in magnitude, but display a phase angle which increases with applied power. This is the reverse of a mode #1 null.

# CHAPTER 4

# STATIC MODELING OF NLE MODES

## 4.1 General Static NLE Model

The operational mode characteristics described in Chapter 3 can be predicted using cold FET models [4,5]. Most device modeling is usually done for devices operating as active components in a common source configuration. The cold FET models are used to simulate the passive characteristics of devices (i.e. Vds = 0) and, as presented here, apply to a common gate configuration as opposed to common source configuration. A modified cold FET model is shown below in Figure 15. The behavior of the various NLE modes is modeled closely by a symmetrical Tee network consisting of the elements, $Z_S$ and $Z_m$, as shown in the Figure.

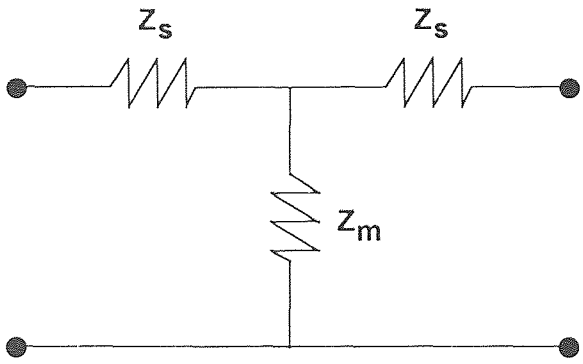


**Figure 15** Symmetrical Tee Equivalent Network of a Passive MESFET

The impedances, $Z_S$ and $Z_m$, can be related to the S-parameters for the two-port network by Equations 6 and 7, as derived through network analysis techniques.

$$S_{11} = S_{22} = \frac{Z_s^{\,2} + 2Z_sZ_m - Z_o^{\,2}}{Z_s^{\,2} + 2Z_sZ_o + 2Z_sZ_m + 2Z_mZ_o + Z_o^{\,2}} \tag{6}$$

and

$$S_{21} = S_{12} = (1 + S_{11})\frac{Z_mZ_o}{Z_s^{\,2} + Z_sZ_o + 2Z_sZ_m + Z_mZ_o} \tag{7}$$

### 4.2 Mode #1 Model

In the case of mode #1, $Z_S$ is the fixed resistance, $R_{cg}$ (5 Ω fits the sample data shown in Figure 3). $Z_m$ consists of the power sensitive resistance, $R_g$, in series with a capacitor, $C_g$ (.6 pF), internal to the MESFET, and a series external inductor, $L_G$ (5.2 nH), connected between the gate and ground. This model is shown in Figure 16.

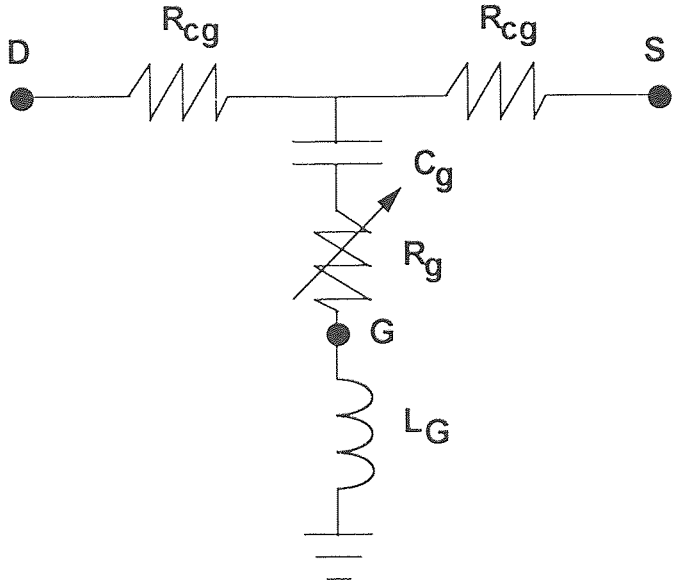


**Figure 16** Equivalent Circuit for Mode #1. $L_G$ is external to the MESFET.

The parameters, $R_{cg}$ and $C_g$, correspond to the physical resistance of the gate channel and the gate diode capacitance established by the gate bias voltage. They are both insensitive to variation in power level. The resistance, $R_g$, represents the internal gate resistance. An excellent match to mode #1 typical characteristics is obtained when $R_g$ is increased from 1 Ω at low power level (Pin < -20 dBm) to about 30 Ω at high power (5 - 10 dBm). These characteristics are shown in Figures 17a and 17b.

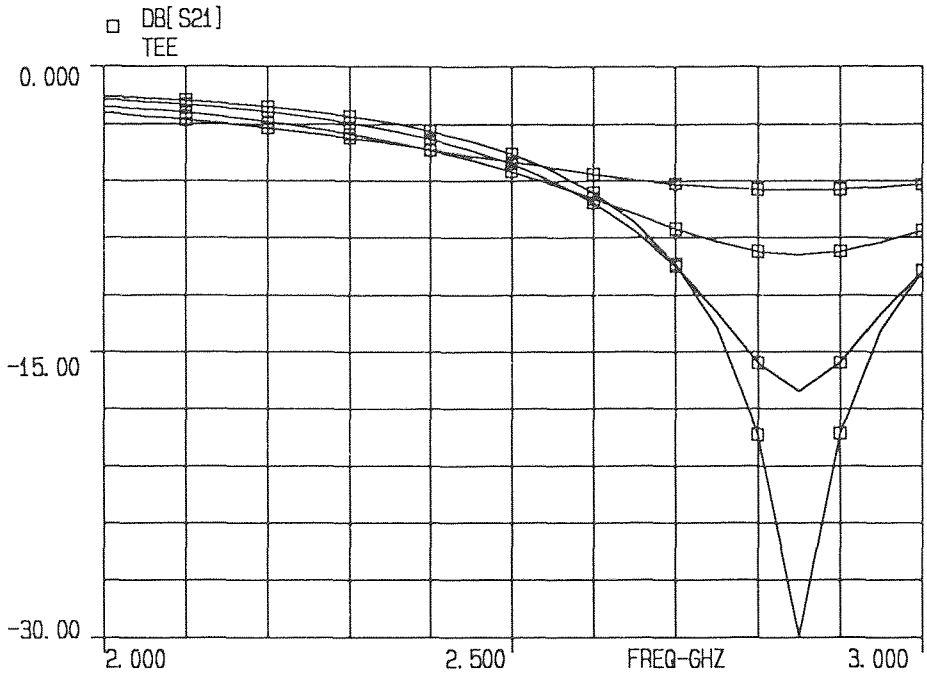


**Figure 17a** Gain Response of Mode #1 Equivalent Circuit. Rg = 1 Ω to 30 Ω.

The modeled response shows the characteristic null which decreases in depth with increasing power level. The model also predicts the change from gain expansion to gain compression with increasing power as frequency is reduced. Likewise, the model predicts the phase cross corresponding in frequency to the center of the magnitude null. The model shows positive phase shift below the cross and negative phase shift above the cross.

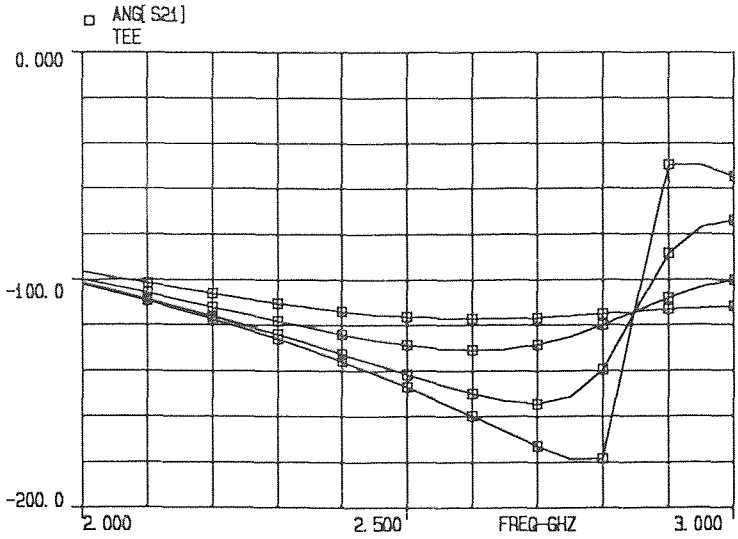


**Figure 17b** Phase Response of Mode #1 Equivalent Circuit. $R_g$ = 1 Ω to 30 Ω.

### 4.3 Mode #3 Model

As the MESFET's negative gate bias is increased, the value of $R_{cg}$ increases and becomes sensitive to power level. Because of the lower conductance of the gate channel, the shunt channel to gate capacitances, $C_{cg}$, become significant. The variation of $R_{cg}$ with power can be used to model mode #3 behavior. For this case, $Z_S$ is the parallel combination of $R_{cg}$ and $C_{cg}$ as shown in Figure 18 and given by Equation 8.

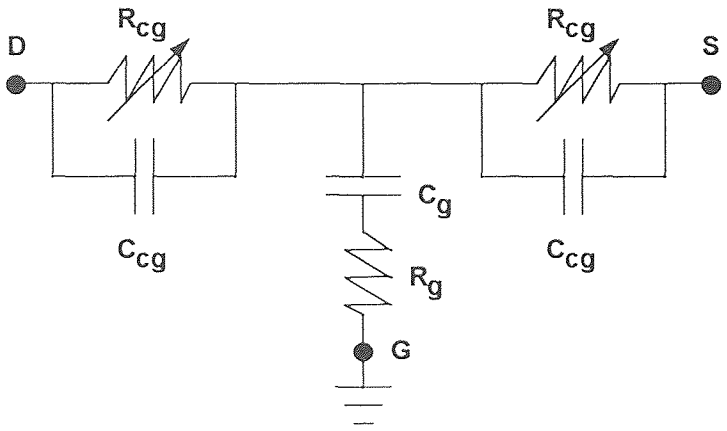


**Figure 18** Equivalent Circuit for Mode #3

$$Z_s = \frac{R_{cg}}{1 + j\omega R_{cg} C_{cg}} \tag{8}$$

A value of about 0.15 pF for $C_{cg}$, and 1 Ω for Rg, is need to model the $S_{21}$ magnitude and phase response shown in Figure 13. The value of the gate capacitor, Cg, reduces to about 0.2 pF. A change in $R_{cg}$ from about 3000 Ω, to simulate low power response, to 100 Ω, to simulate high power response, produces the characteristics shown in Figures 19a and 19b.

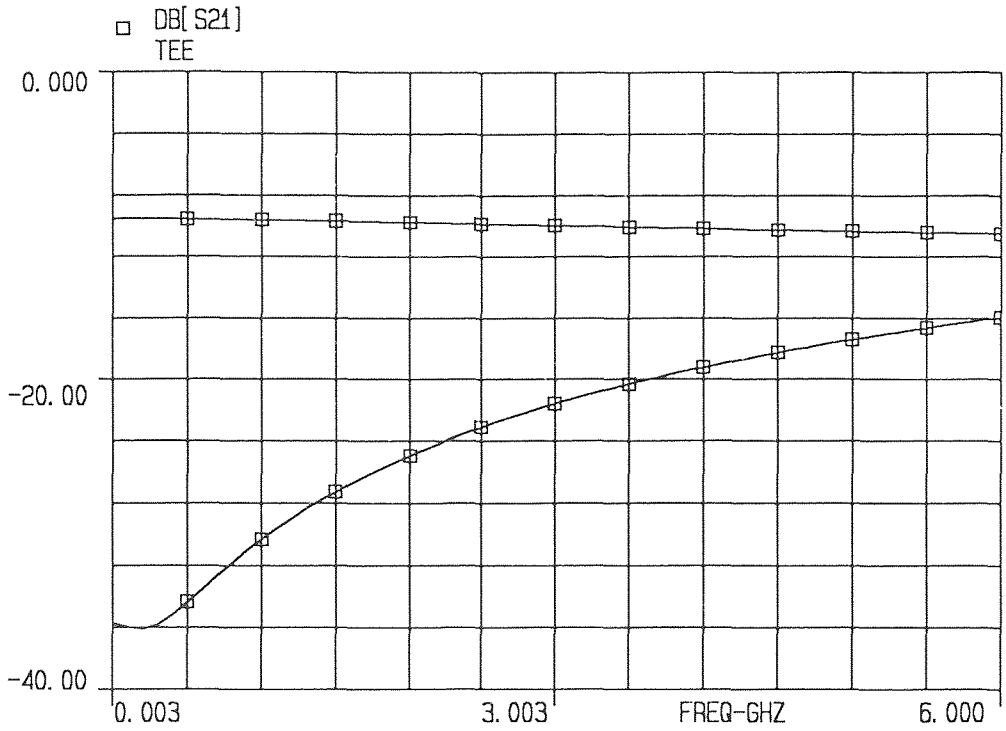


**Figure 19a** Gain Response of Mode #3 Equivalent Circuit. $R_{cg}$ = 3000 Ω to 100 Ω.

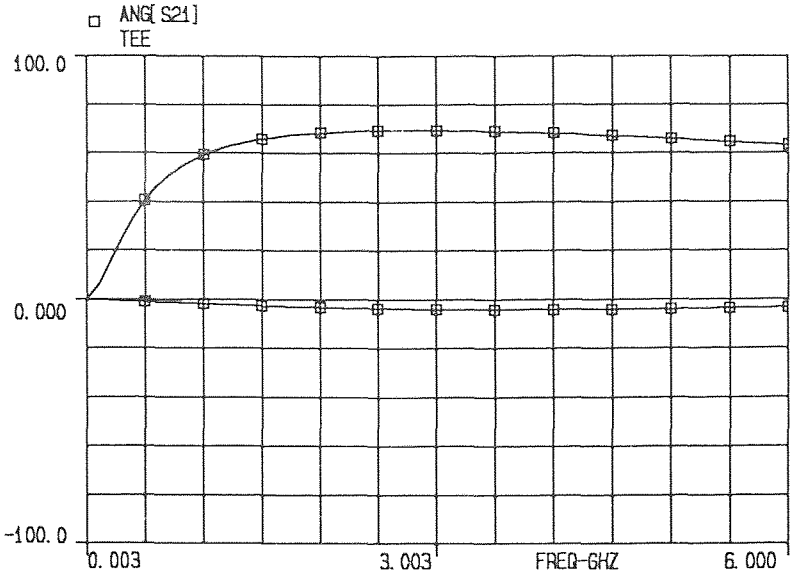


**Figure 19b** Phase Response of Mode #3 Equivalent Circuit. $R_{cg}$ = 3000 Ω to 100 Ω.

For the mode #3 equivalent circuit, the impedance $Z_m$, consists of $R_g$ in series with $C_g$. Variation of $R_g$, up to 500 Ω, has negligible effect on the mode #3 null. The ratio of $C_g$ to $C_{cg}$ does effect the shape of the response. $L_g$ is not required since it does not effect the near dc null of mode #3. If $L_g$ is added to the circuit $Z_m$ is as described in Equation 9.

$$Z_m = R_g + \frac{1}{j\omega C_g} + j\omega L_G \tag{9}$$

Both mode #1 and mode #3 nulls will be present under these conditions, and each will be independently controlled by the respective power sensitive resistance, $R_g$ and $R_{cg}$. In the transition frequency range between these nulls, the magnitude of the forward transmission gain is relatively insensitive to gate bias voltage level, while the phase angle varies considerably. This property can be utilized to produce an exceedingly simple, voltage controlled phase shifter [6].

### 4.4 Broad-Band Mode Model

The broad-band mode characteristics can be modeled by the same Tee equivalent circuit as that of mode #3, which is shown in Figure 18. For the broad-band mode, however, the required value of $R_{cg}$ spans the range from 130 Ω to 50 Ω, to simulate increasing power. This result is expected as a consequence of the lower dc bias voltage. $C_{cg}$ is also reduced to a value of 0.13 pF. The corresponding broad-band mode response is shown in Figures 20a and 20b.

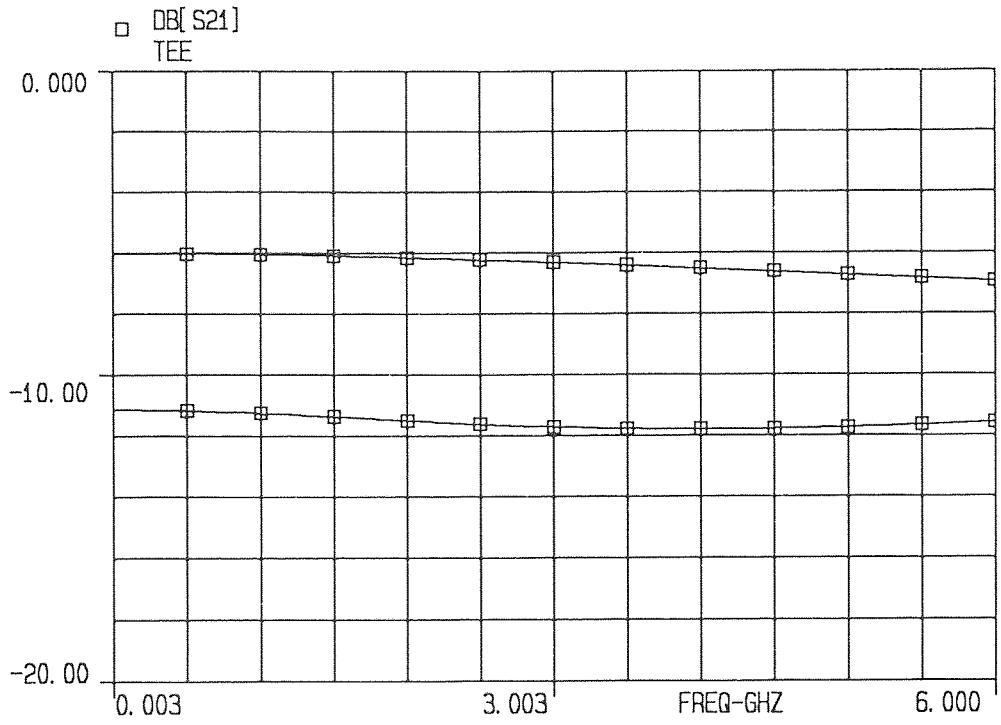


**Figure 20a** Gain Response of Broad-Band Mode Equivalent circuit.
$R_{cg}$ = 130 Ω to 50 Ω.

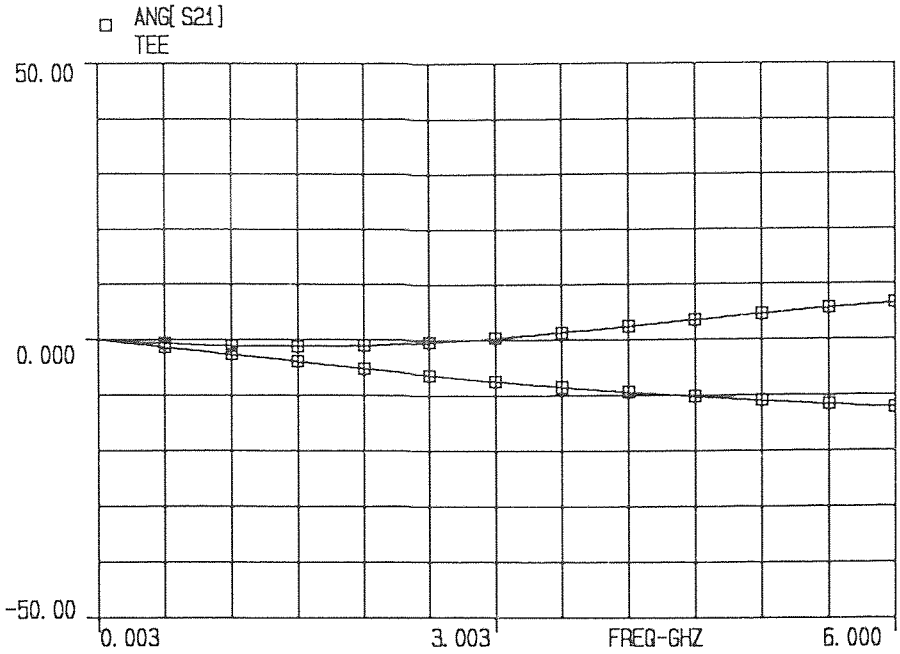


**Figure 20b** Phase Response of Broad-Band Mode Equivalent circuit. $R_{cg}$ = 130 Ω to 50 Ω.

### 4.5 Mode #2 Model

A model for the mode #2 response is shown in Figure 21. A bridged Tee network with a restricted range of values is required to produce the unique phase characteristics associated with this mode. Too large or too small of an element value will transform the descending phase step, shown in Figure 9, to an ascending phase step, and mode #1 characteristics will result. Mode #1 nulls are observed on both sides of the narrow band of bias voltages which produce mode #2 nulls. The response provided by the mode #2 model is shown in Figures 22a and 22b.

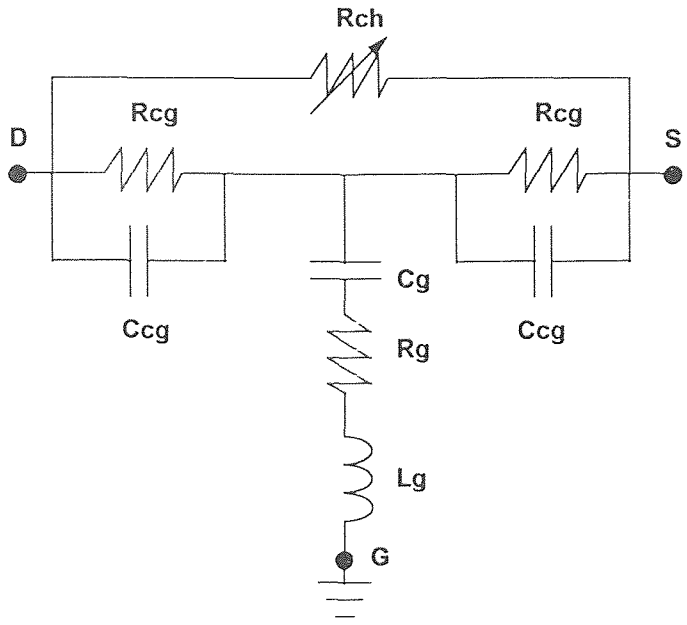


**Figure 21** Equivalent Circuit for Mode #2. $R_{ch}$ affects Null Depth and Frequency.

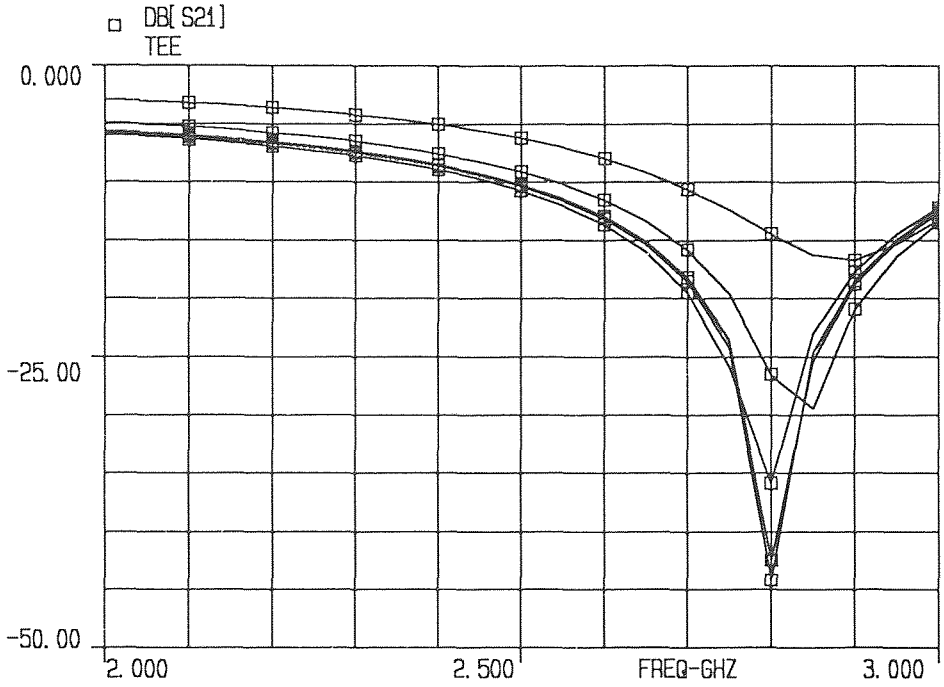


**Figure 22a** Gain Response of Mode #2 Equivalent Circuit. $R_{ch}$ = 70 Ω to 30 Ω.

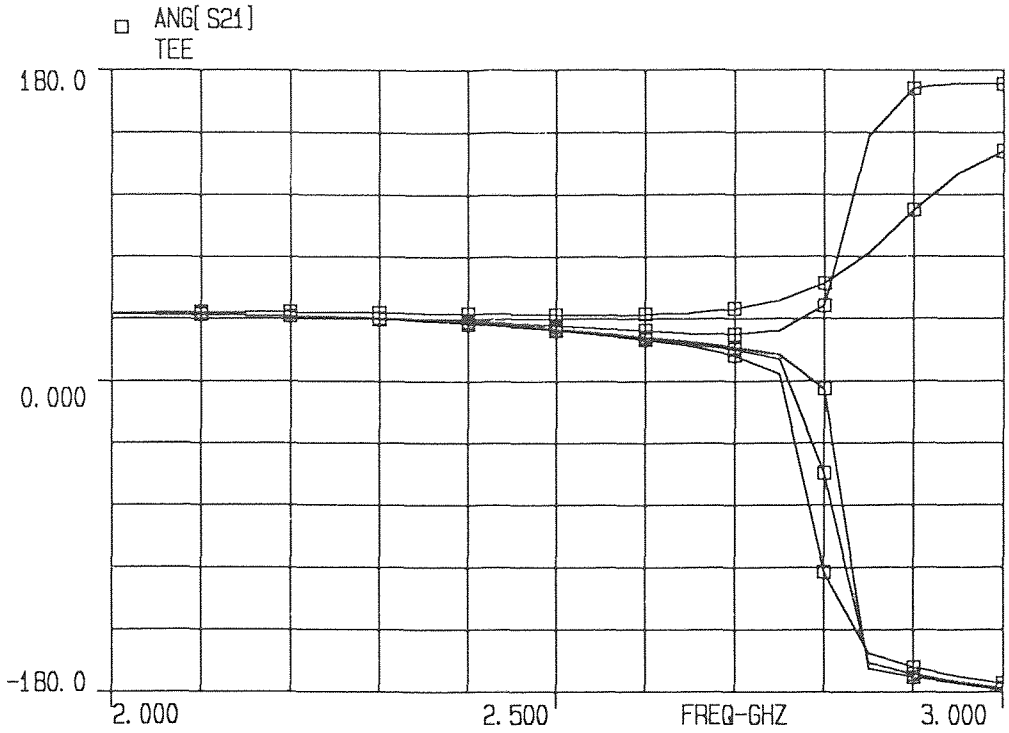


**Figure 22b** Phase Response of Mode #2 Equivalent Circuit. $R_{ch}$ = 70 Ω to 30 Ω.

Only a change in $R_{ch}$ is required to simulate the observed mode #2 magnitude and phase response. An equivalent Tee network can be created consisting of complex, reactive elements. The network whose response is depicted in Figure 22, requires the resistance, $R_{cg}$, with a value of 250 Ω, and the resistance, $R_{ch}$, which varies from 70 Ω to 20 Ω as power is increased. The equivalent real part of the impedance $Z_s$ ranges from 30.7 Ω to 9.6 Ω. These values fit the mode #2 bias conditions which lie between those of mode #1 where $R_{cg}$ = 5 Ω and the Broad-band Mode where $R_{cg}$ = 130 Ω to 50 Ω. The complex impedances $Z_s$ and $Z_m$ are given by Equations 10 and 11 respectively where $Z_{m'}$ in Equation 11 is given by Equation 12, and is the part of the $Z_m$ term resulting from the bridge elements.

$$Z_s = \frac{R_{ch} R_{cg}}{R_{ch} + 2R_{cg} + j\omega R_{cg} R_{ch} C_{cg}} \tag{10}$$

$$Z_m = Z_{m'} + R_g + \frac{1}{j\omega C_g} + j\omega L_G \tag{11}$$

$$Z_{m'} = \frac{R_{cg}^{\ 2}}{R_{ch} + 2R_{cg} - (\omega R_{cg} C_{cg})^2 R_{ch} + j\omega(2R_{cg} R_{ch} C_{cg} + R_{cg}^{\ 2} C_{cg})} \tag{12}$$

The above expression for $Z_m$ includes Rg (4.5 ohms), $C_g$ (.5 pF), and an external $L_G$ (.45 nH) needed to match the mode #2 response. The $Z_{m'}$ expression shows why a change in $R_{ch}$ not only effects the mode #2 null depth but also its location in frequency. It also explains why mode #2 can be used to produce high-Q notch filters. If,

$$(\omega R_{cg} C_{cg})^2 R_{ch} > R_{ch} + 2R_{cg} \tag{13}$$

the real part of $Z_m$, as given by Equation 11, is negative. By proper choice of component values and bias voltage, it is possible to cancel $R_g$ and any losses of $L_g$ and $C_g$ to produce an extremely high-Q trap. Notch depths in excess of 50 dB are easily achieved as illustrated in Figure 23.

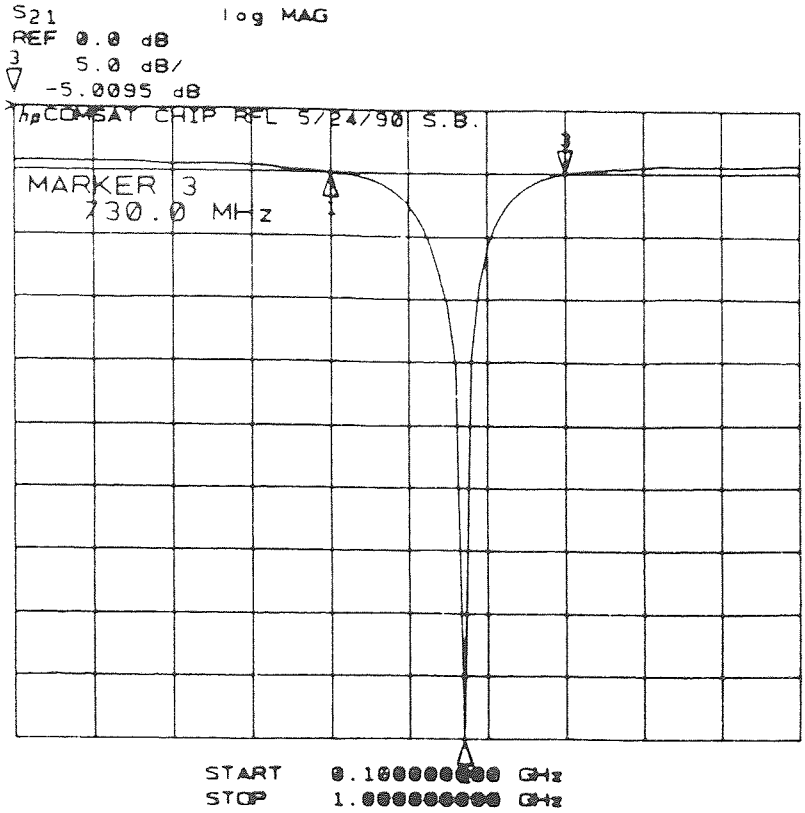


**Figure 23** Single NLE Used as a Notch Filter

One limitation of this techniques is the NLE's non-linear characteristic. NLE notch filters should be limited to low power applications (Pin < -10 to -20 dBm) to avoid distortion.

### 4.6 Mode #4 Model

The equivalent circuit for mode #4 characteristics is shown in Figure 24. This circuit is very similar to the mode #1 circuit. One difference is the absence of $C_g$. As a consequence of the high forward bias current, the FET is virtually a resistive element, and $C_g$ disappears. The function of $C_g$ is replaced by an external capacitor $C_G$ which is a 10 pF dc blocking capacitor. This change accounts for the drop in frequency displayed by the mode #4 null.

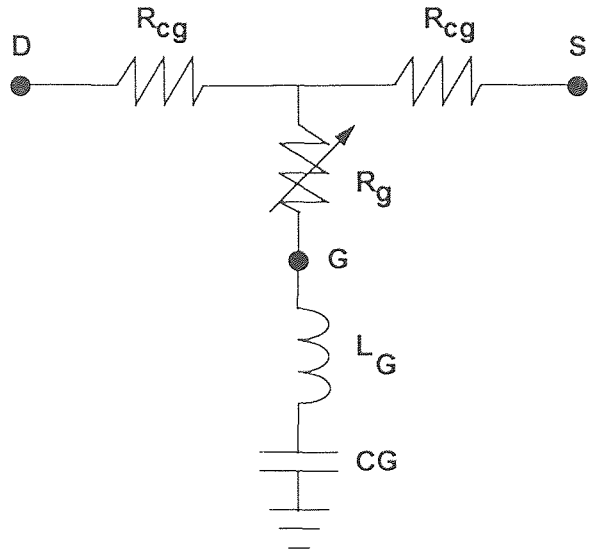


**Figure 24** Equivalent Circuit for Mode #4. Both $L_G$ and $C_G$ are External to the FET.

The response produced by the above mode #4 equivalent circuit is illustrated below in Figures 25a and 25b.

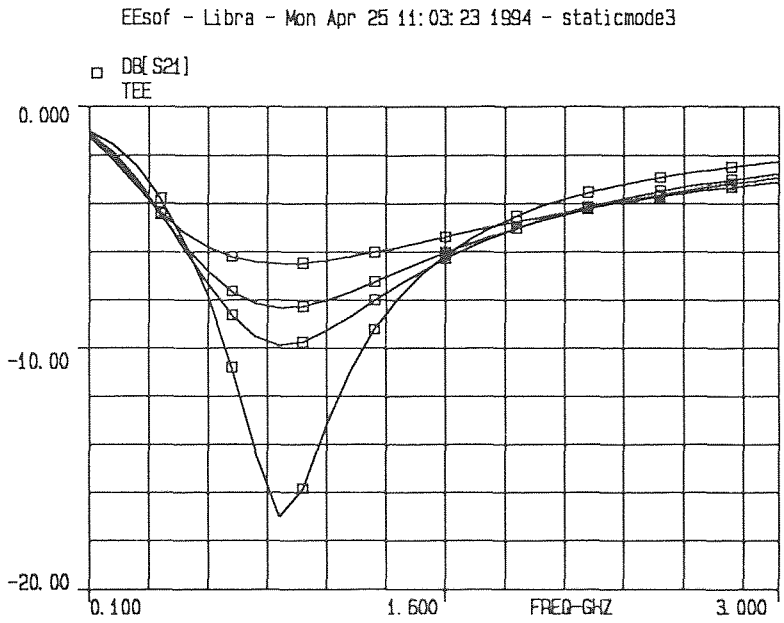


**Figure 25a** Gain Response of Mode #4 Equivalent Circuit. Rg = 5 Ω to 30 Ω.

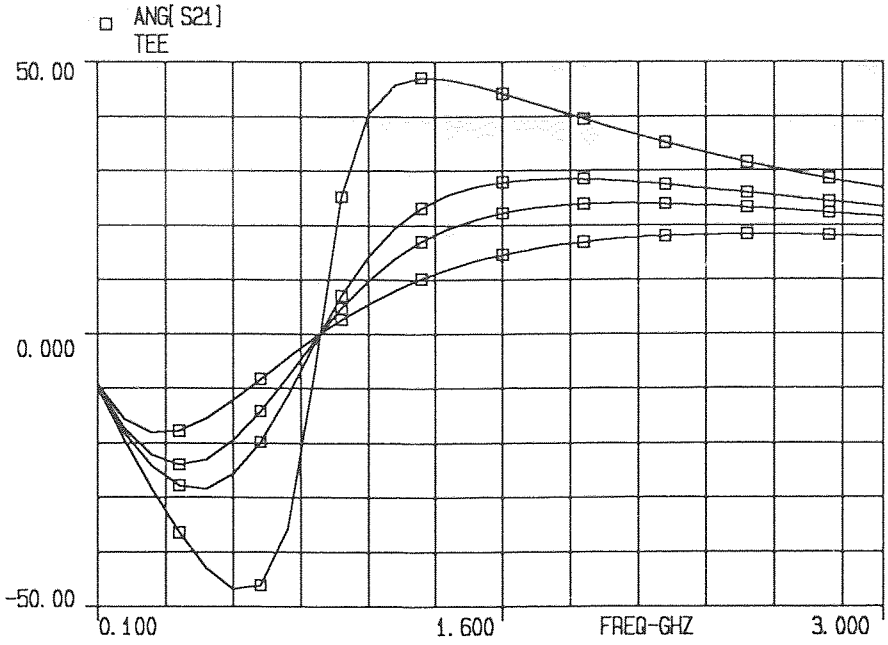


**Figure 25b** Phase Response of Mode #4 Equivalent Circuit. Rg = 5 Ω to 30 Ω.

# CHAPTER 5

# DYNAMIC NLE MODEL

## 5.1 Model Development

An accurate dynamic model is essential to conform the response of a device to a specific application. Unfortunately, most existing non-linear GaAs MESFET models were formulated for active, common source, applications, and give poor results when applied to the NLE in a passive common gate configuration [4]. Some specialized passive models have been developed [7,8]. However, these models are primarily for FET switches, and focus on the ON and OFF states in the linear region of operation. They provide little insight into MESFET characteristics in the transition region between these end states. This is the region of most importance in NLE applications.

To solve this problem, a model was developed which accurately predicts passive MESFET characteristics over a wide dynamic range of frequency, power level, and bias voltage. This model is based on a modified Curtice model with a non-linear diode element acting as the non-linear channel resistance [4]. Harmonic balance microwave circuit simulation software is used for the analysis of circuit component values.

The S-parameters of the device to be modeled are obtained over a desired range of frequency and input power, for a variety of bias levels using a network analyzer, automated test equipment, and specially designed calibration fixtures. Circuit optimization is then used to match the component values of an initial static model to the measured S-parameter data. This is done in a manner similar to the equivalent circuit modeling presented in Chapter 4. The static model is converted to a dynamic model by insertion of the non-linear diode element, and run under a harmonic balance analysis. The diode is reversed biased and operates in the reverse saturation region. Diode parameters such as junction capacitance and reverse saturation current control the change in characteristics with power

level. These parameters are altered to match the device's non-linear gain response. Once congruent gain characteristics are obtained, the phase characteristics should also match, with little or no adjustment of the diode. The general, dynamic model of a MESFET connected as an NLE, is shown in Figure 26.

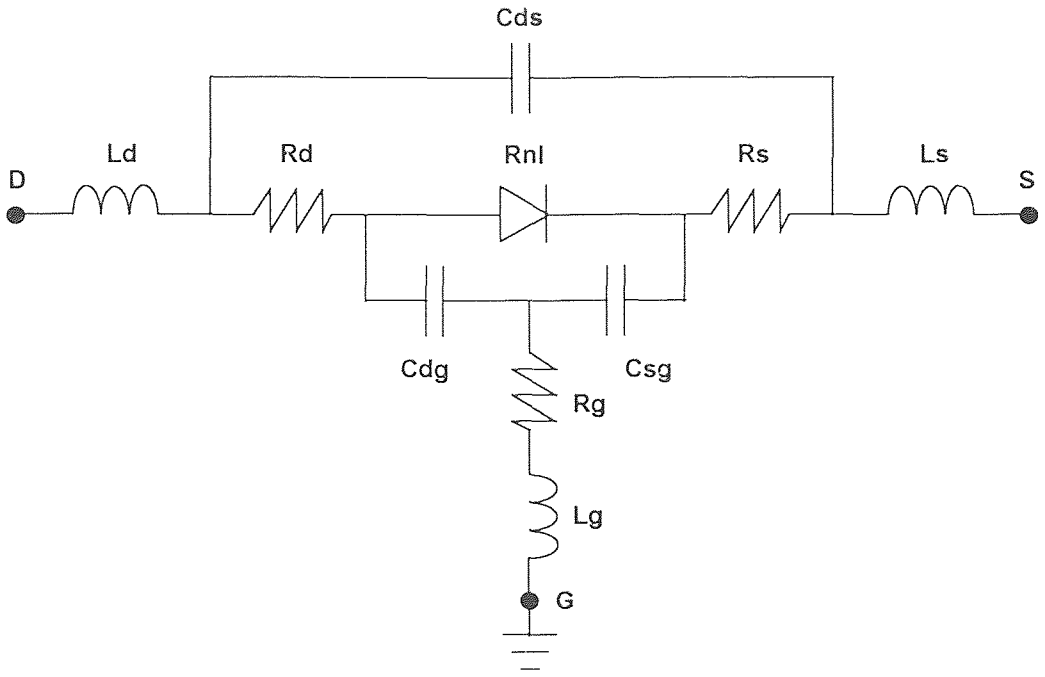


**Figure 26** Dynamic Model of NE710 NLE Using a Non-Linear Diode Element

The S-parameter equations for the equivalent circuit model shown in Figure 26 are given in Equation A-21. A detailed derivation and definition of terms is provided in Appendix I. The Libra model schematic representation and circuit file description for the basic FET NLE component are discussed in Appendix II.

$$S11 := \frac{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND + (NA - ND - (Zo + Xs - Xd)\cdot(NC))\cdot Zo}{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND + (NA + ND + 2\cdot D3 + (Zo + Xs + Xd)\cdot(NC))\cdot Zo}$$

$$S12 := \frac{2\cdot Zo\cdot D4}{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND + (NA + ND + 2\cdot D3 + (Zo + Xs + Xd)\cdot(NC))\cdot Zo}$$

$$S21 := \frac{2\cdot Zo\cdot D4}{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND + (NA + ND + 2\cdot D3 + (Zo + Xs + Xd)\cdot(NC))\cdot Zo}$$

$$S22 := \frac{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND - (NA - ND + (Zo + Xd - Xs)\cdot NC)\cdot Zo}{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND + (NA + ND + 2\cdot D3 + (Zo + Xs + Xd)\cdot(NC))\cdot Zo}$$

[A1-21]

## 5.2 NLE Modeling Results

The dynamic model simulates gate bias control, and the effect of external component variation on the NLE frequency and power transfer characteristics. The following data illustrates the effect of gate bias control in the model. The complete dynamic model shown in Figure 26 was used to simulate the typical performance characteristics of mode #1, #2, and #3 operation of an NLE. Figures 27, 28 and 29 illustrate these results. These results correspond to the equivalent circuit modeling results shown in Figures 17, 22, and 19, and to the measured data shown in Figures 5, 9, and 11, respectively. As illustrated by the figures, the single dynamic model simulates the magnitude and phase characteristics of three of the five operating modes previously modeled by three separate static models.

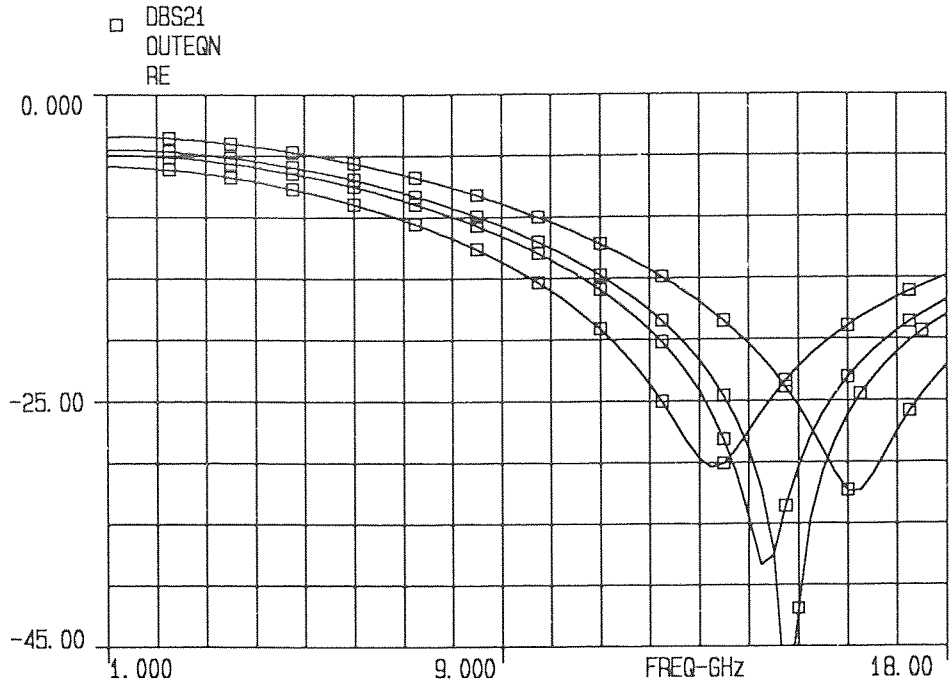


**Figure 27a** Simulated Mode #2 Gain Response

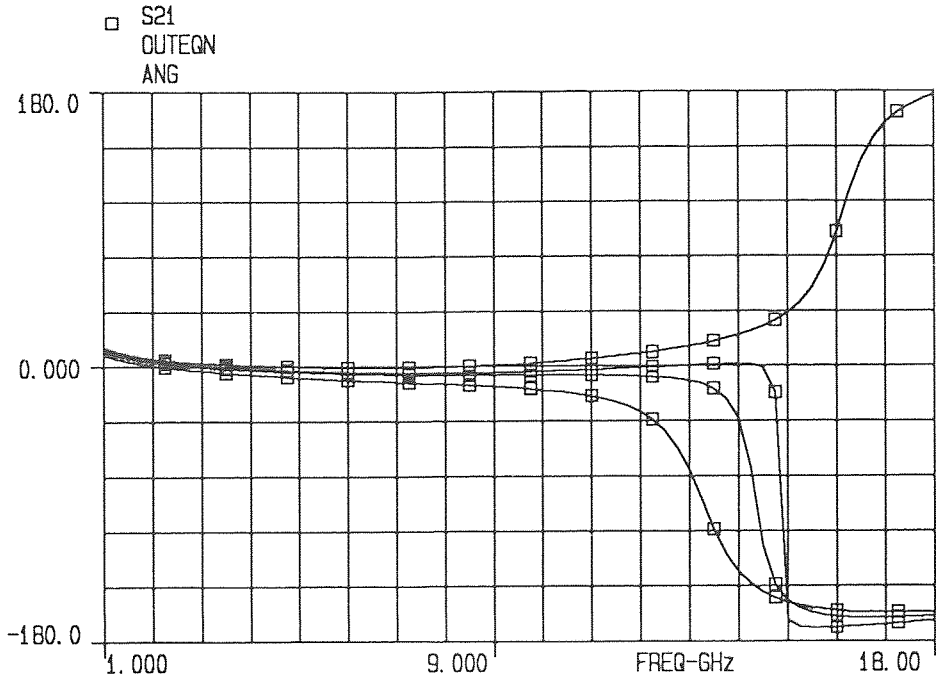


**Figure 27b** Simulated Mode #2 Phase Response

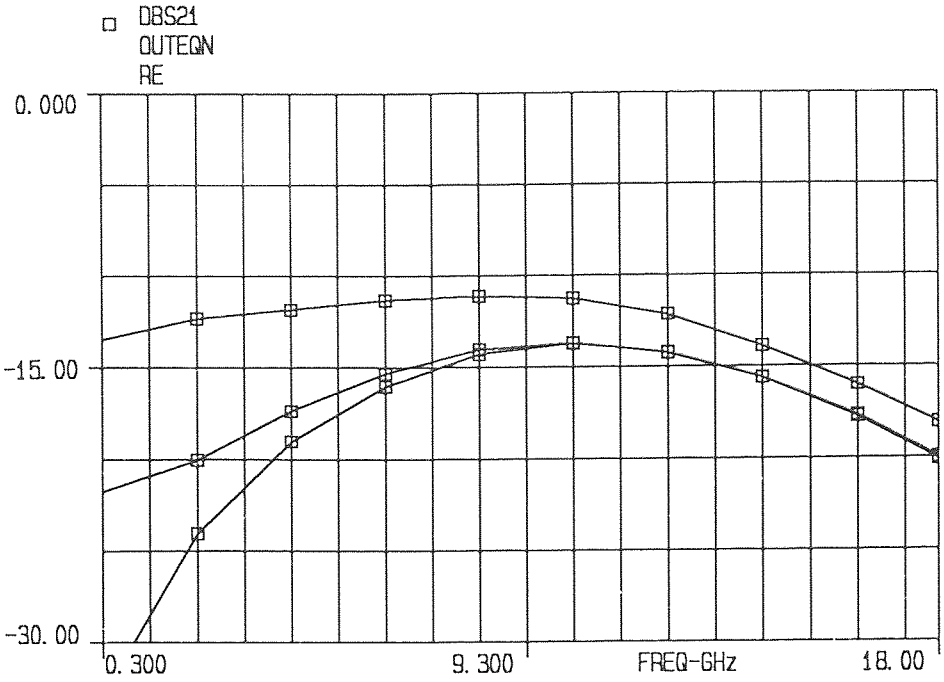


**Figure 28a** Simulated Mode #3 Gain Response

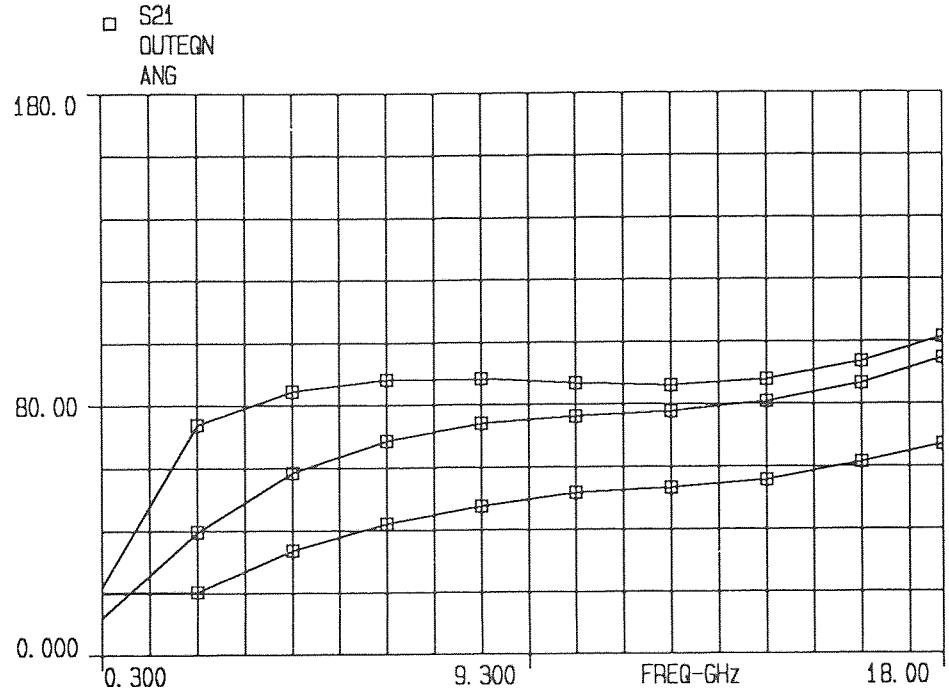


**Figure 28b** Simulated Mode #3 Phase Response

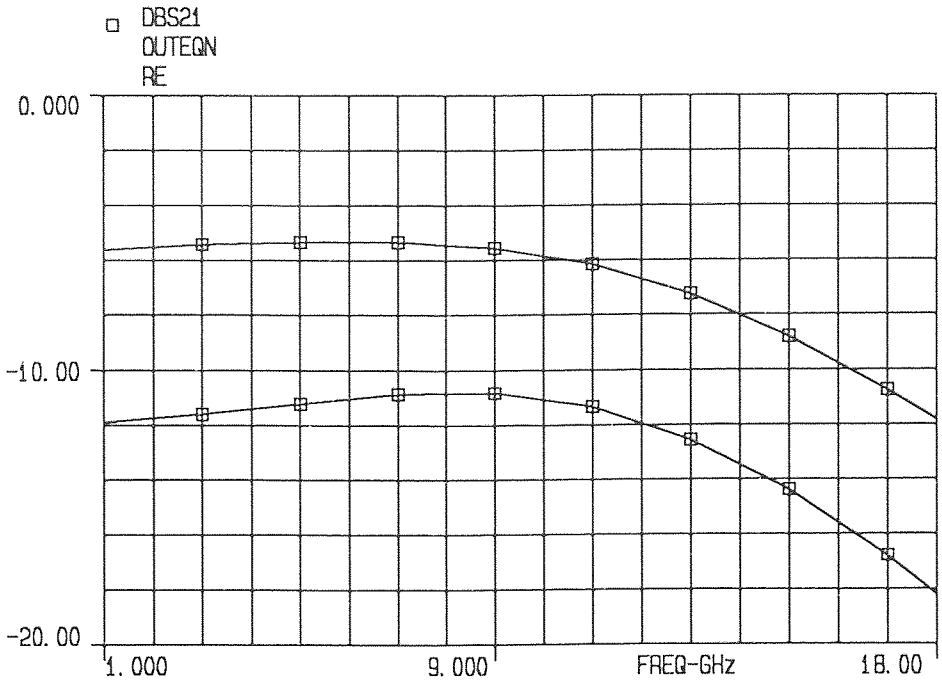


**Figure 29a** Simulated Broad-Band Mode Gain Response

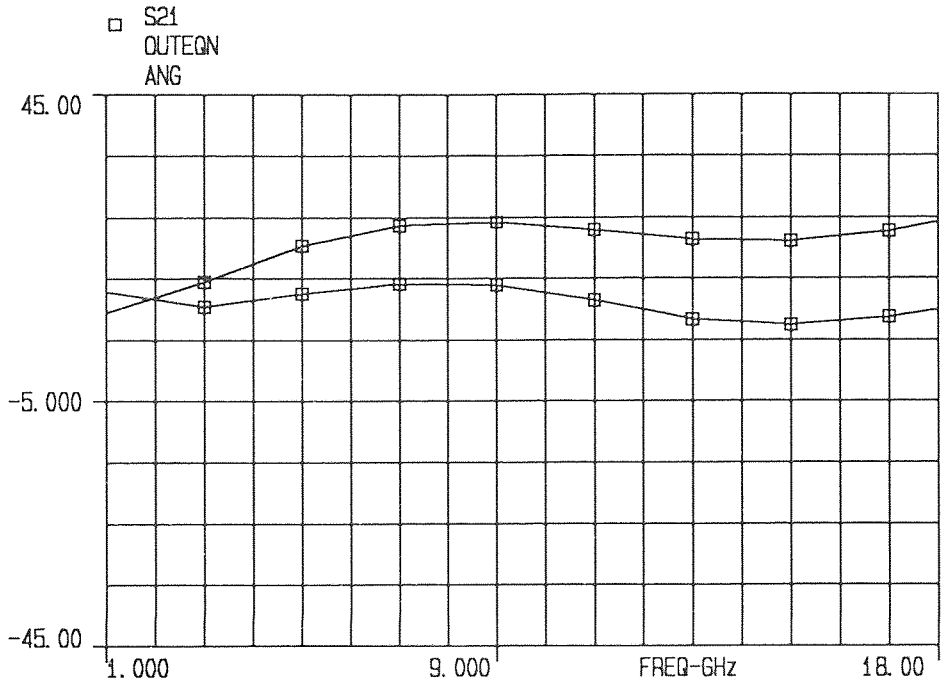


**Figure 29b** Simulated Broad-Band Mode Phase Response

Figure 27a illustrates the deep null in the gain response associated with mode #2 corresponding to gate voltages just before the pinch-off voltage level. The simulated phase response for mode #2 is shown in Figure 27b. A gate bias of 1.2 volts corresponds to the data shown in this figure.

The broad null in gain response at low frequency associated with mode #3 is shown in Figure 28a. Figure 28b illustrates the negative phase shift with increasing power level associated with this mode. The modeled response occurs for gate voltages above 1.5 volts.

The broad-band mode gain response shown in Figure 29a was obtained with a gate bias of 1.3 volts which falls between the voltage levels of modes #2 and #3. The corresponding phase characteristics are given in Figure 29b.

The above results show the validity of simulated gate bias control in the model. Each of the mode #2, and #3, and the broad-band mode characteristics associated with a region of gate bias were simulated using the gate bias control in the model. The model, however, does not take into account the drastic physical changes in gate structure that take place during the forward bias conditions of mode #1 or the reverse breakdown region associated with mode #4. Further modifications to the model would be needed to take these effects into account.

### 5.3 NE710 Modeling Results

The mode of operation most useful for linearization is the broad-band mode. The ability of the model to accurately simulate the actual power and frequency response characteristics of an NE710 MESFET operating in this mode is illustrated in Figures 30 and 31. The data was taken and the model was generated for the NE710 MESFET as described in section 5.1. A comparison of actual measured S-parameter data and the simulated results is given in the figures.

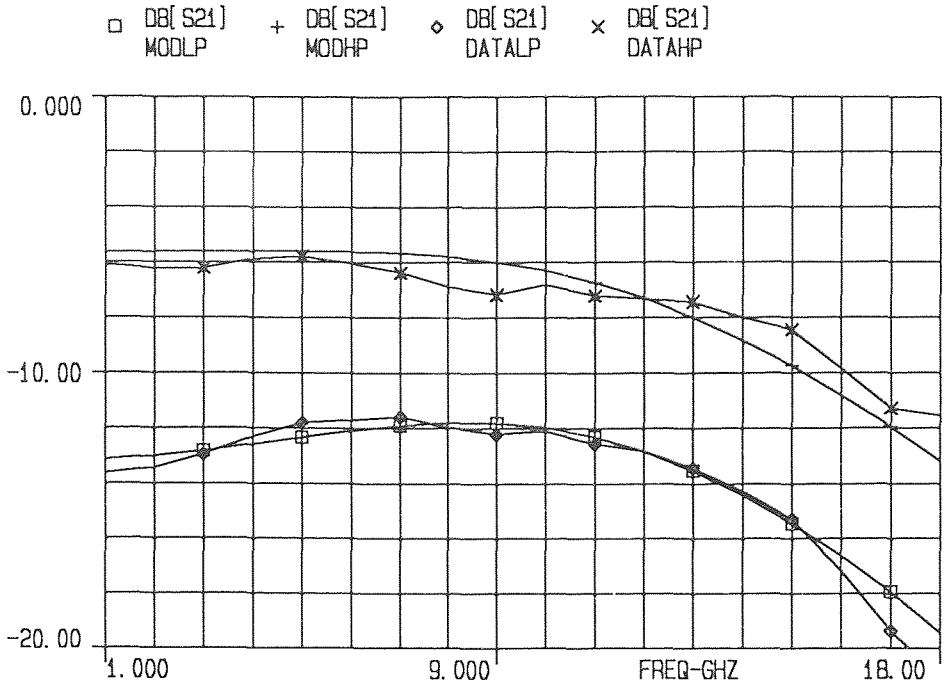


**Figure 30a** Comparison of Measured and Simulated Gain Response Over Frequency

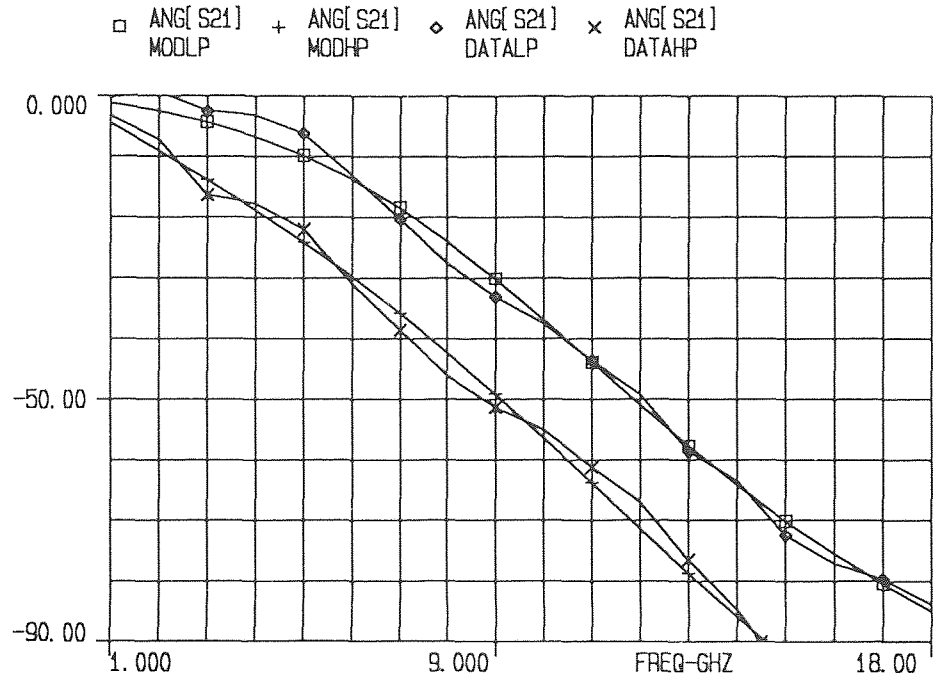


**Figure 30b** Comparison of Measured and Simulated Phase Response Over Frequency

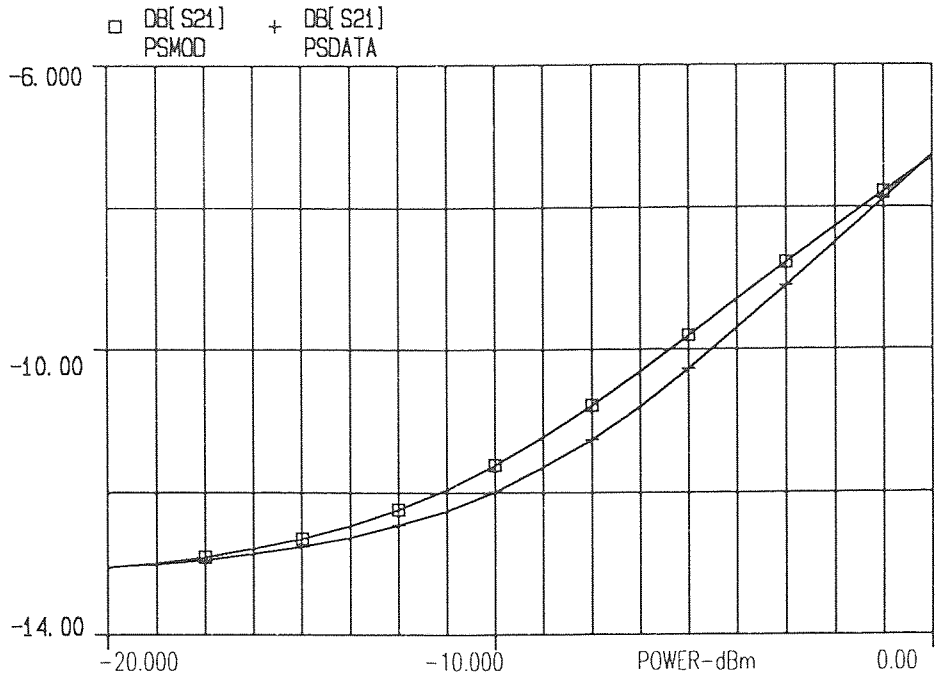


**Figure 31a** Comparison of Measured and Simulated Gain Response Over Power

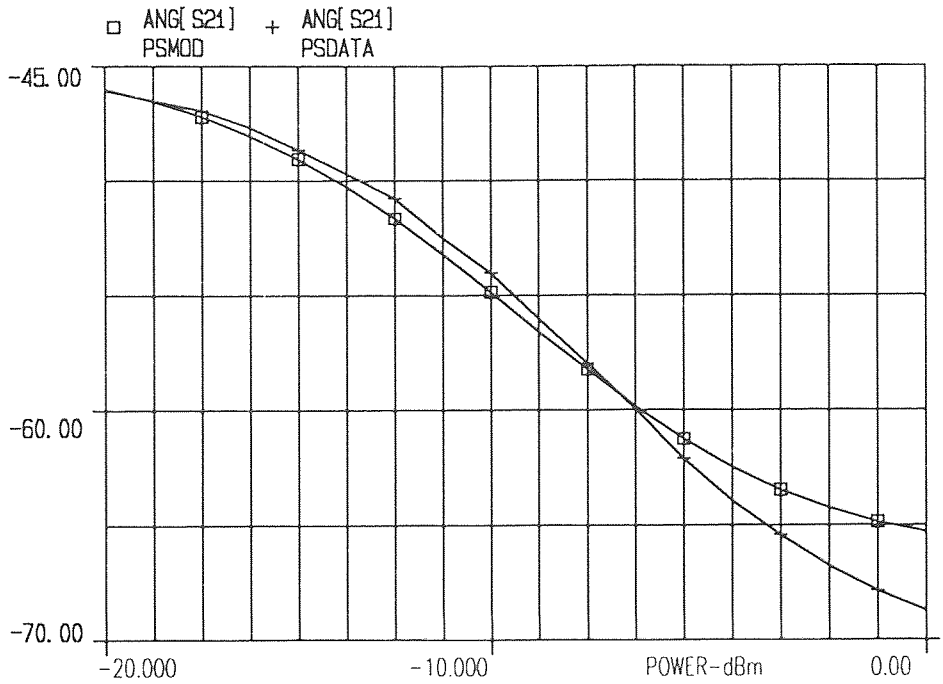


**Figure 31b** Comparison of Measured and Simulated Phase Response Over Power

The simulated and measured magnitude and phase characteristics of an NE710 MESFET chip connected as an NLE and biased for broad-band mode operation are illustrated in Figures 30a and 30b. The data is shown over frequency, at -20 dBm input power and 0 dBm input power. At the low power level, the NLE is insensitive to changes in drive level, while at the high power level, the change in NLE loss is approximately 6 dB, about that needed to compensate for the non-linearity of an amplifier near saturation. The null associated with this mode occurs above the frequency range of interest and thus facilitates a wide band response. Figures 31a and 31b show a comparison of the simulated and measured response of the same device as a function of input power at 12 GHz. The figures illustrate the expanding magnitude and phase transfer characteristics of the forward transmission gain as input power is increased.

# CHAPTER 6

# NLE TWTA LINEARIZER DESIGN

## 6.1 TWTA Linearizer

Non-linearities are inherent in all amplifier transfer characteristics (power in vs. power out) in both magnitude and phase. These non-linearities produce intermodulation distortion for multi-carrier input signals and increased bit error rate and spectral spreading for single carrier digitally modulated signals.

As discussed earlier, some of the identified NLE modes are beneficial for the design of linearizers, others are more applicable to limiters. The NLE has been applied in both reflective and transmissive networks to produce linearizers which cover the full C and Ku satellite bands. The passive FET non-linear element has proven particularly successful as a broad-band linearizer for compensation of such non-linearities for TWTAs, and GaAs FET and BJT solid state amplifiers. For TWTAs, NLE linearizers provide a reduction in inter-modulation distortion products of more than 10 dB at the 2.5 dB output power back-off point. Multiple-decade bandwidth is also possible for linearizers using FET NLEs.

## 6.2 TWTA Linearizer Design

The above model was used to design a linearizer for a Ku-band TWTA. TWTAs require a phase response which increases with power level. This characteristic is opposite to that produced by the basic NLE network. Positive phase shift with increasing power can be achieved by the NLE through appropriate design of the gate impedance and the NLE embedding network. This can be done while maintaining the gain expansion and bandwidth characteristics typical of the basic NLE operating in the broad-band mode.

For the design, the entire linearizer/TWTA system was simulated. This included the linearizer, the TWTA, and variable gain blocks at the input and output of the

linearizer. These are used to align the expansion of the linearizer relative to the TWTA saturation point. S-parameter data of the TWTA magnitude and phase transfer response as a function of input power were obtained using an automated test system. This S-parameter data was converted to equation form using an exponential series expansion as given by Equations 14 and 15, for output power and phase respectively.

$$Gain = A + BP_{in} + CP_{in}^{2} + DP_{in}^{3} + EP_{in}^{4} + FP_{in}^{5} + GP_{in}^{6} + HP_{in}^{7} \qquad (14)$$

$$Phase = I + JP_{in} + KP_{in}^{2} + LP_{in}^{3} + MP_{in}^{4} + NP_{in}^{5} + OP_{in}^{6} \qquad (15)$$

These equations were then combined with a linearizer circuit embedding the NE710 dynamic model, and analyzed using the same harmonic balance software used to develop the NLE model. The linearizer circuit components were adjusted to provide maximally flat phase and optimal gain response defined as a 1 dB compression point as close to saturation as possible with less than 0.5 dB overshoot. The two-tone, third order carrier-to-intermodulation ratio (C/I) performance was then calculated using these results. The resulting linearizer gain and phase characteristics as a function of input power level are shown in Figures 33a and 33b. The combined linearizer/TWTA transfer response is shown in Figures 34a-34c, and the overall C/I as a function of output backoff is shown in Figure 35.

### 6.3 TWTA Linearizer Modeling Results

To verify the design, a linearizer was fabricated using the component values predicted by the dynamic model and evaluated for transfer characteristics and C/I performance. These results are also shown in Figures 33-35, and confirm the value and accuracy of the NLE model. Figures 32a and 32b show the gain and phase compression of the uncompensated TWTA as saturation is approached. Figures 33a and 33b show the simulated and measured gain and phase expansion characteristics of the TWTA linearizer. The combined

linearizer/TWTA measured and simulated gain and phase characteristics, output power, and C/I performance are illustrated in Figures 34 and 35.

The linearizer, when mated with the test TWTA, increased the C/I performance to greater than 30 dB for 3 dB and greater output backoff levels. The worst case phase variation from far backoff to saturation was reduced from 40 degrees to less than 5 degrees, and the am/pm conversion coefficient (Kp) was reduced to less than 1 degree/dB. Also, the separation of the 1 dB compression point from saturation was reduced from greater than 8 dB to less than 2 dB. This performance was maintained over a bandwidth of greater than 500 MHz.

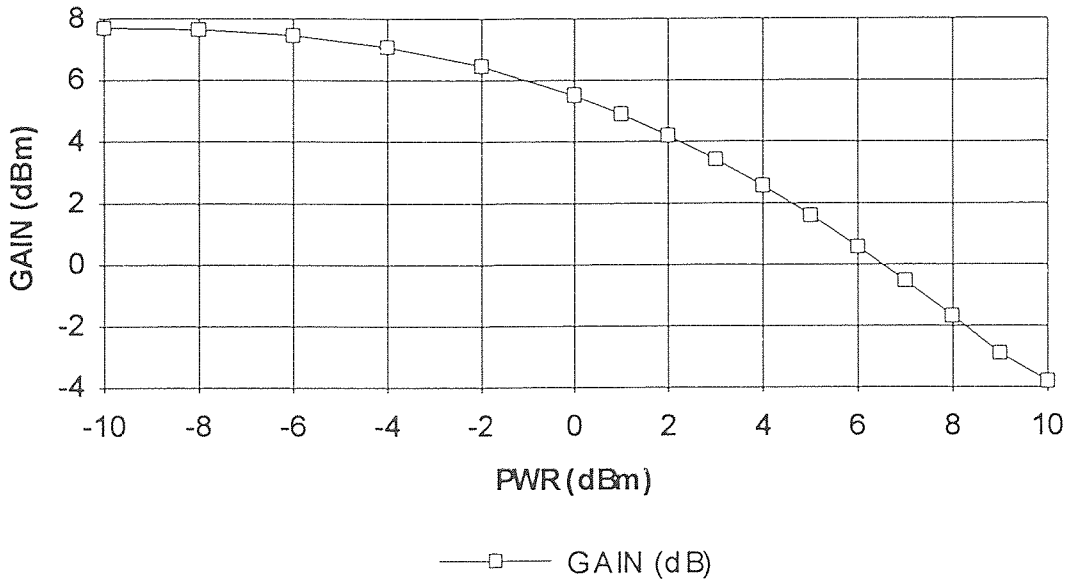


**Figure 32a** TWTA Gain Compression

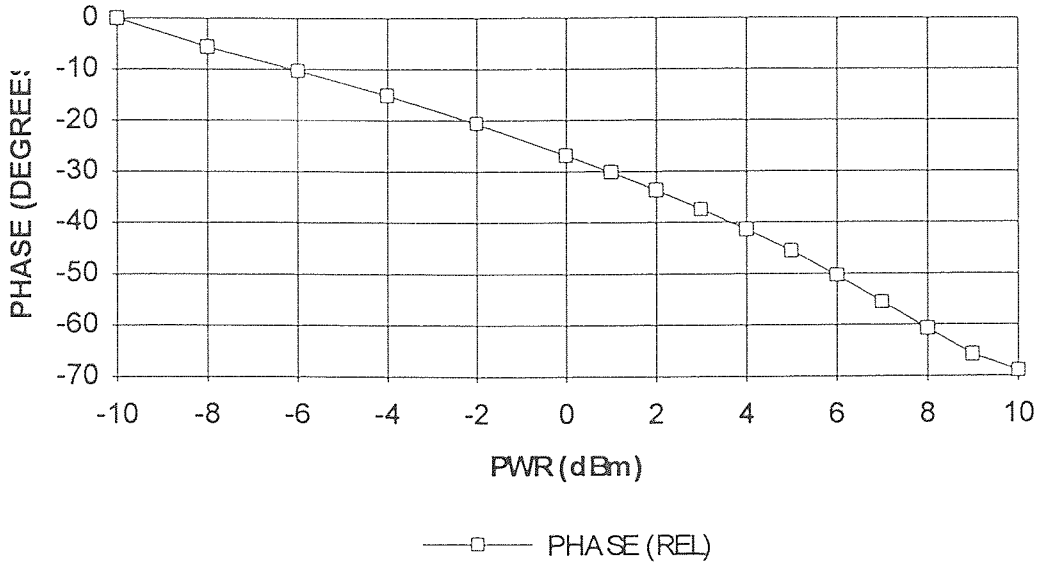


**Figure 32b** TWTA Phase Compression

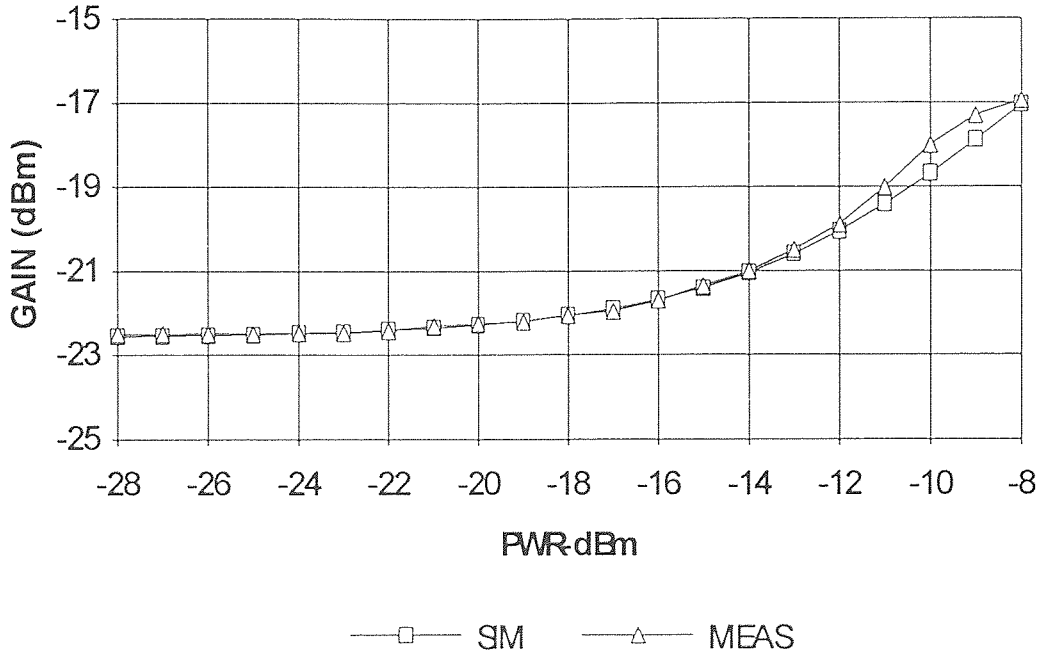


**Figure 33a** NE710 TWTA Linearizer Measured and Simulated Gain Transfer Response

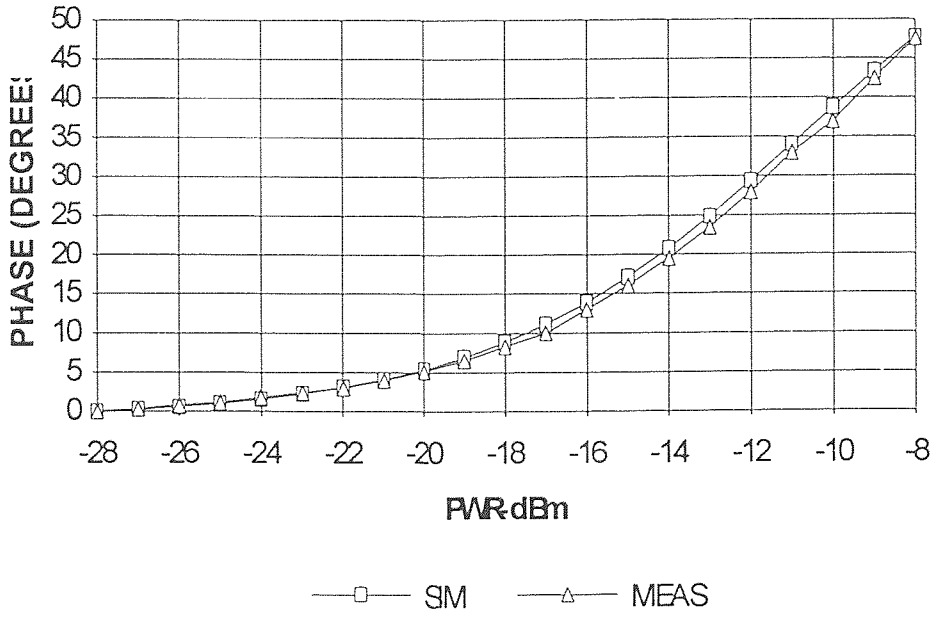


**Figure 33b** NE710 TWTA Linearizer Measured and Simulated Phase Transfer Response

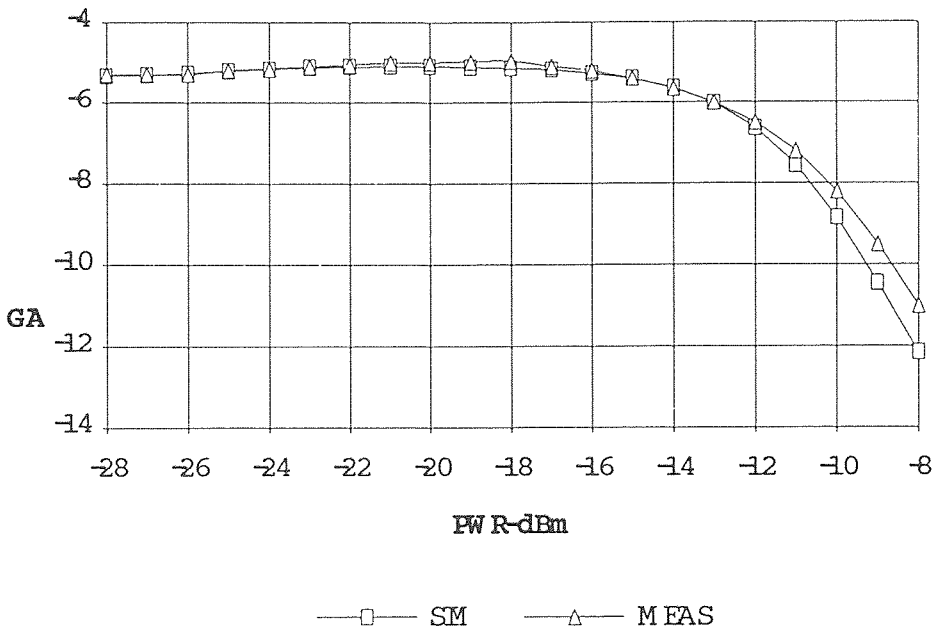


**Figure 34a** Comparison of Combined Linearizer/TWTA Measured and Simulated Gain Performance Over Power

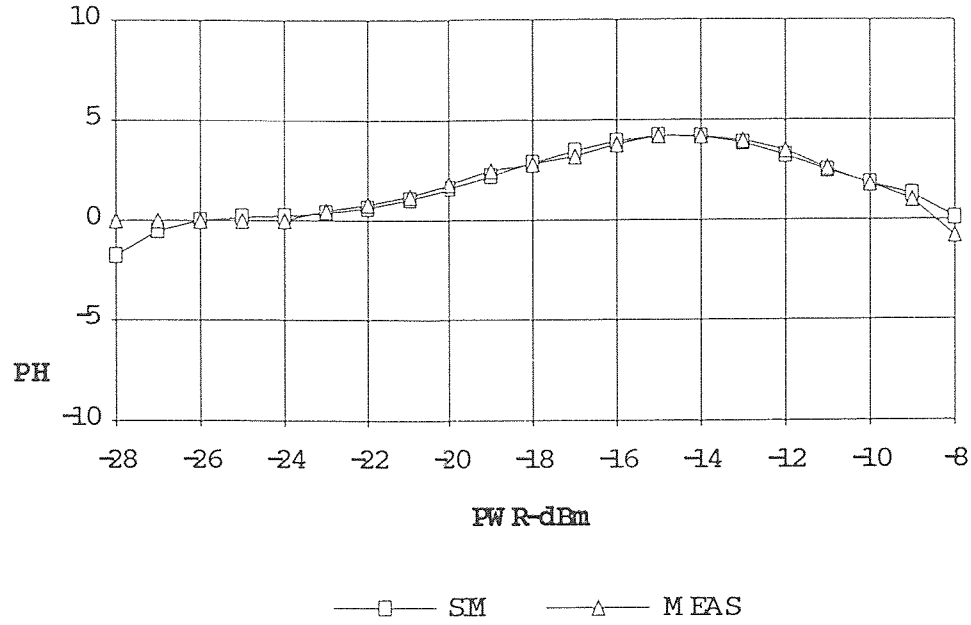


**Figure 34b** Comparison of Combined Linearizer/TWTA Measured and Simulated Phase Performance Over Power

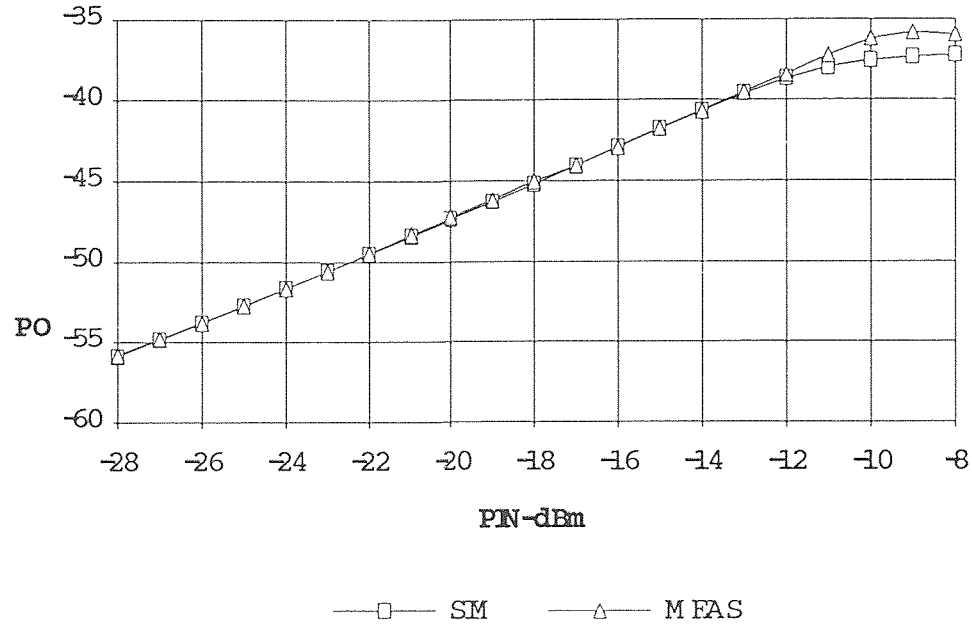


**Figure 34c** Comparison of Combined Linearizer/TWTA Measured and Simulated Output Power Versus Input Power

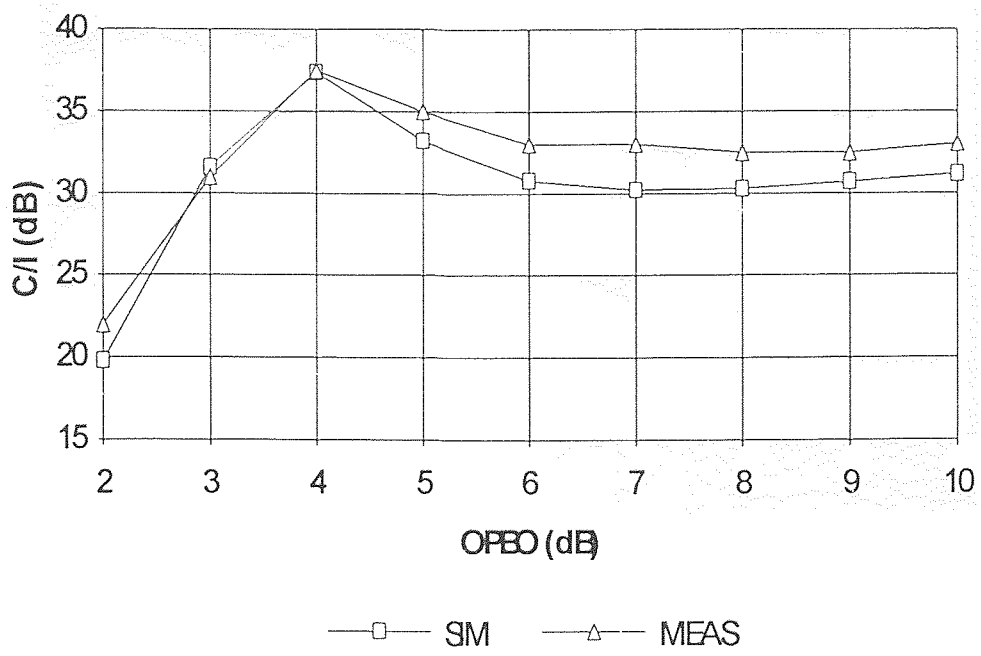


**Figure 35** Comparison of Combined Linearizer/TWTA Measured and Simulated C/I Performance as a Function of Output Backoff

# CHAPTER 7

# CONCLUSION

Information has been provided on the non-linear characteristics of MESFET NLEs when used in non-linear control applications. FET NLEs offer significant advantages in terms of circuit simplicity, bandwidth, temperature stability and control of transfer characteristics over other non-linear transfer function generators. Because of the passive nature of FET NLEs, negligible dc power is consumed which offers the potential for high reliability. The value of FET NLEs has been demonstrated in a variety of linearizer and limiter applications. These devices can be fabricated with minimum size and weight while providing features as remote commandability, wide bandwidth, implementation in MMIC technology, and outstanding performance.

Five, bias dependent, operating modes valuable in the production of non-linear control elements have been identified. Four of these modes are associated with power sensitive nulls in the transmission response. The fifth mode provides a very wide band transmission response while maintaining power sensitivity. Simple equivalent circuit models were developed for each of these modes. These models require only a single resistive element to be varied to simulate the NLE's change in response with power and were shown to closely match the measured characteristics of NLEs.

A general model which accurately predicts the dynamic characteristics of an NLE linearizer was presented. This model accurately forecasts the effects of external circuitry and gate bias control on linearizer transfer characteristics. Excellent agreement between simulated and measured performance has been shown, when used in the design of a linearizer for a TWTA at Ku band. Use of the model has enabled the system gain and phase transfer response, output power, and C/I performance of a linearizer/TWTA combination to be predicted in advance of fabricating the linearizer.

# APPENDIX 1

## DERIVATION OF MODEL S-PARAMETERS

In order to derive the S-parameter equations for the NLE dynamic model, the equivalent circuit was broken into smaller two-port networks. The network parameters for each sub-network were then derived. These parameters were then combined using two-port network analysis techniques to derive the equations for the entire equivalent circuit.

The first sub-network evaluated was the tee network in the gate circuit as shown in Figure A1-1.

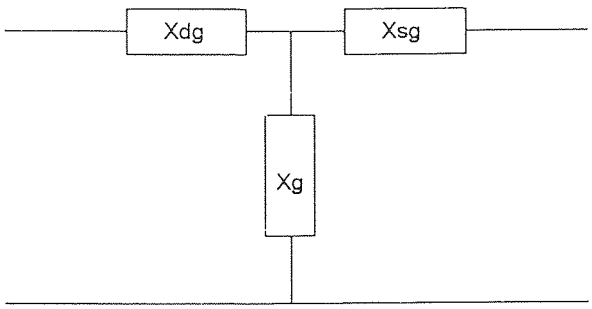


**Figure A1-1** Tee Sub-Network of NLE Equivalent Circuit

The Z-parameters for the above tee network are given in Equation A1-1, and where obtained using the Z-parameter defining equations for a tee network.

$$Z11 := Xdg + Xg \qquad Z12 := Xg$$

$$Z21 := Xg \qquad Z22 := Xsg + Xg \qquad \text{[A1-1]}$$

The tee network in Figure A1-1 is in parallel with the series network Rnl as shown in Figure A1-2. Since Y-parameters add in parallel, the above Z-parameters are converted to Y-parameters as given in Equation A1-2 [10].

$$Y11 := \frac{Xsg + Xg}{DEN1} \qquad Y12 := \frac{-Xg}{DEN1}$$

$$Y21 := \frac{-Xg}{DEN1} \qquad Y22 := \frac{(Xdg + Xg)}{DEN1} \qquad \text{[A1-2]}$$

where:

$$DEN1 := Xdg \cdot Xsg + Xg \cdot (Xdg + Xsg) \qquad \text{[A1-3]}$$

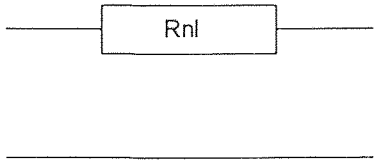


**Figure A1-2** Series Network Containing the Non-Linear Resistance, Rnl

The Y-parameters for the series network Rnl are as given in Equation A1-4.

$$Y11 := \frac{1}{Rnl} \qquad Y12 := -\frac{1}{Rnl}$$

$$Y21 := -\frac{1}{Rnl} \qquad Y22 := \frac{1}{Rnl} \qquad \text{[A1-4]}$$

The combined network is shown in Figure A1-3.

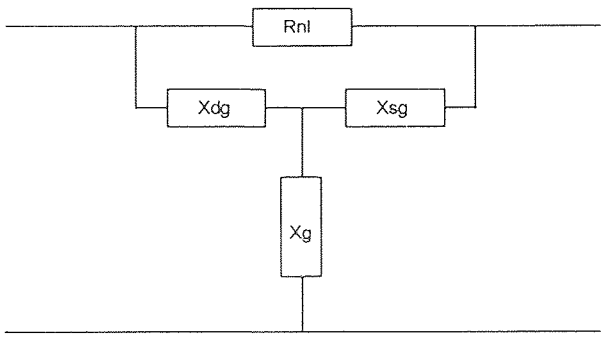


**Figure A1-3** Parallel Combination of Tee and Series Sub-Networks

The resulting Y-parameters are obtained from direct matrix addition of the Y-parameters for the tee and series sub-networks and are as given in Equation A1-5

$$Y11 := \frac{1}{Rnl} + \frac{(Xsg + Xg)}{(Xdg \cdot Xsg + Xdg \cdot Xg + Xg \cdot Xsg)} \qquad Y12 := -\frac{1}{Rnl} + \frac{-Xg}{(Xdg \cdot Xsg + Xdg \cdot Xg + Xg \cdot Xsg)}$$

$$Y21 := -\frac{1}{Rnl} + \frac{-Xg}{(Xdg \cdot Xsg + Xdg \cdot Xg + Xg \cdot Xsg)} \qquad Y22 := \frac{1}{Rnl} + \frac{(Xdg + Xg)}{(Xdg \cdot Xsg + Xdg \cdot Xg + Xg \cdot Xsg)} \qquad [A1\text{-}5]$$

In order to combine these results with the network parameters of the series resistance Rd, the above Y-parameters are converted to ABCD parameters as given in Equation A1-6.

$$A := \frac{DEN2 + Rnl \cdot Xdg}{DEN2} \qquad B := Rnl \cdot \frac{DEN1}{DEN2}$$

$$C := \frac{(Xdg + Xsg + Rnl)}{DEN2} \qquad D := \frac{DEN2 + Rnl \cdot Xsg}{DEN2} \qquad [A1\text{-}6]$$

where:

$$DEN2 := Xdg \cdot Xsg + Xg \cdot (Xdg + Xsg + Rnl) \qquad [A1\text{-}7]$$

The series two port network, Rd, is shown in Figure A1-4 and the resulting ABCD parameters are given in Equation A1-8.

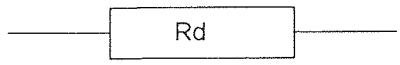


**Figure A1-4** Series Network, Rd

$$A := 1 \qquad B := Rd$$
$$C := 0 \qquad D := 1 \qquad \text{[A1-8]}$$

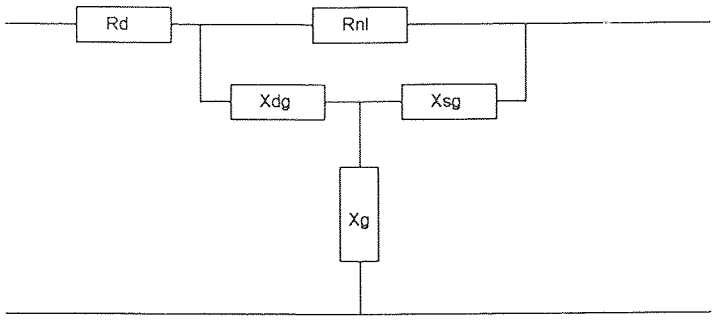


**Figure A1-5** Combination with Series Network, Rd

The resulting parameters for the series combination of the above two-port networks is obtained by matrix multiplication of the ABCD parameter. The results are given below in Equation A1-9.

$$A := \frac{(DEN2 + Rnl \cdot Xdg + Rd \cdot Xdg + Rd \cdot Xsg + Rd \cdot Rnl)}{DEN2} \qquad B := \frac{(Rnl \cdot DEN1 + Rd \cdot DEN2 + Rd \cdot Xsg \cdot Rnl)}{DEN2}$$

$$C := \frac{(Xdg + Xsg + Rnl)}{DEN2} \qquad D := \frac{DEN2 + Rnl \cdot Xsg}{DEN2} \qquad \text{[A1-9]}$$

The next step is to combine the series resistance, Rs, with the above ABCD parameters. The ABCD parameters for the series network RS shown in Figure A1-6 are given in Equation A1-10.

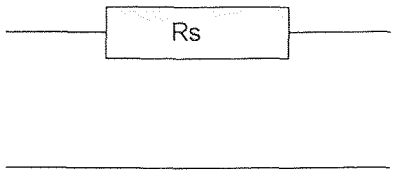


**Figure A1-6** Series Network, Rs

$$A := 1 \qquad B := Rs$$

$$C := 0 \qquad D := 1 \qquad \text{[A1-10]}$$

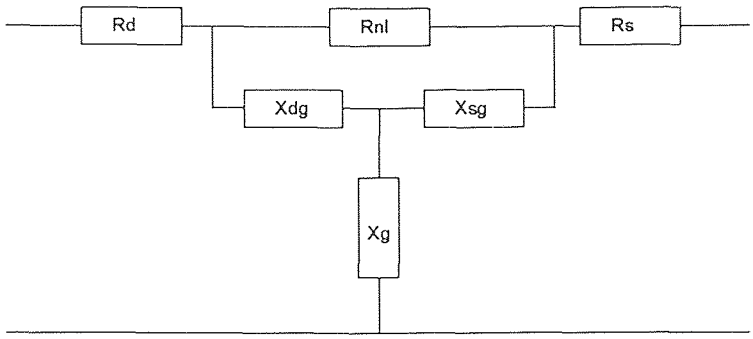


**Figure A1-7** Combination with Series Network, Rs

The resulting network is shown above in Figure A1-7. As before, the S-parameters of the combined network are found through matrix multiplication of the ABCD parameter matrices as given in Equation A1-11.

$$A := \frac{(DEN2 + Rnl \cdot Xdg + Rd \cdot Xdg + Rd \cdot Xsg + Rd \cdot Rnl)}{DEN2}$$

$$B := \frac{(Rs \cdot (Xdg \cdot (Rnl + Rd) + Rd \cdot (Xsg + Rnl)) + Rnl \cdot (DEN1 + Rd \cdot Xsg))}{DEN2} + Rd + Rs$$

$$C := \frac{(Xdg + Xsg + Rnl)}{DEN2}$$

$$D := \frac{Rs \cdot (Xdg + Xsg + Rnl) + Xsg \cdot Rnl}{DEN2} + 1 \qquad \text{[A1-11]}$$

The ABCD parameters are then converted to Y-parameters to be combined in parallel with the series reactance Xds. The converted parameters are given in Equation A1-12.

$$Y11 := \frac{(Rs \cdot (Xdg + Xsg) + Rnl \cdot (Rs + Xsg) + DEN2)}{DEN3} \qquad Y12 := \frac{-DEN2}{DEN3}$$

$$Y21 := \frac{-DEN2}{DEN3} \qquad Y22 := \frac{(Rd \cdot (Xdg + Xsg) + Rnl \cdot (Rd + Xdg) + DEN2)}{DEN3} \qquad \text{[A1-12]}$$

where:

$$DEN3 := DEN2(Rd + Rs) + Rnl \cdot (Rs \cdot Xdg + Rd \cdot Xsg) + Rd \cdot Rs \cdot (Xdg + Xsg + Rnl) + Rnl \cdot DEN1 \qquad \text{[A1-13]}$$

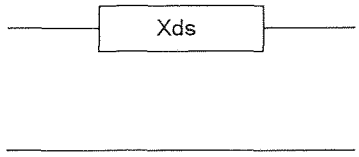


**Figure A1-8** Series Network, Xds

The series reactive network to be combined in parallel with the previous result is shown in Figure A1-8. The corresponding Y-parameters are given in Equation A1-14.

$$Y11 := \frac{1}{Xds} \qquad Y12 := -\frac{1}{Xds}$$

$$Y21 := -\frac{1}{Xds} \qquad Y22 := \frac{1}{Xds} \qquad \text{[A1-14]}$$

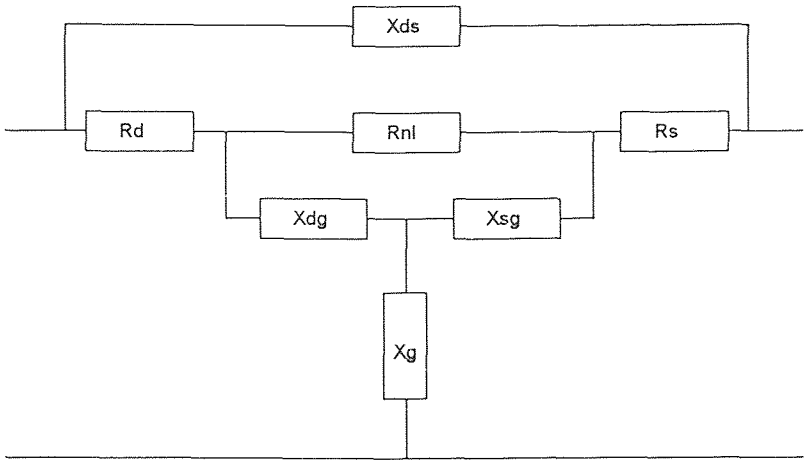


**Figure A1-9** Parallel Combination with Series Network, Xds

The resulting two-port network is shown above in Figure A1-9. The S-parameters for this network are obtain by matrix addition of the Y-parameters for the two individual networks as given in Equations A1-12 and A1-14. These results are given in Equations A1-15.

$$Y11 := \frac{1}{Xds} + \frac{(Rs\cdot(Xdg + Xsg) + Rnl\cdot(Rs + Xsg) + DEN2)}{DEN3} \qquad Y12 := -\frac{1}{Xds} + \frac{-DEN2}{DEN3}$$

$$Y21 := -\frac{1}{Xds} + \frac{-DEN2}{DEN3} \qquad Y22 := \frac{1}{Xds} + \frac{(Rd\cdot(Xdg + Xsg) + Rnl\cdot(Rd + Xdg) + DEN2)}{DEN3}$$

[A1-15]

The above Y-parameters are then converted to the ABCD parameters given by Equation A1-16. These ABCD parameters are combined with the series reactive network, Xd, shown in Figure A-10.

$$A := \frac{DEN3 + NUMA1}{DEN4} \qquad B := Xds \cdot \frac{DEN3}{DEN4}$$

$$C := \frac{NUMC1}{DEN4} \qquad D := \frac{DEN3 + NUMD1}{DEN4} \qquad \text{[A1-16]}$$

where:

$$DEN4 := DEN3 + Xds \cdot DEN2$$

$$NUMA1 := (Rd \cdot (Xdg + Xsg) + Rnl \cdot (Rd + Xdg) + DEN2) \cdot Xds$$

$$NUMC1 := (Rd + Rs + Xds) \cdot (Xdg + Xsg) + Rnl \cdot (Rd + Rs + Xdg + Xsg + Xds)$$

$$NUMD1 := ((Rs \cdot (Xdg + Xsg) + Rnl \cdot (Rs + Xsg) + DEN2) \cdot Xds) \qquad \text{[A1-17]}$$

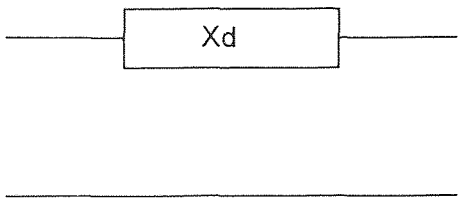


**Figure A1-10** Series Network, Xd.

The ABCD parameters for the network in Figure A1-10 are given by Equation A1-18.

$$A := 1 \qquad B := Xd$$

$$C := 0 \qquad D := 1 \qquad \text{[A1-18]}$$

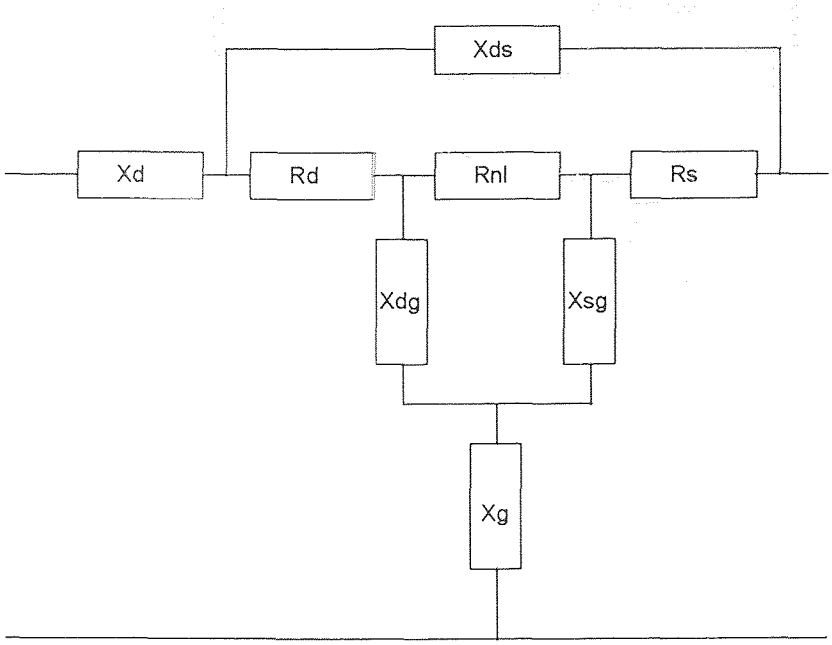


**Figure A1-11** Combination with Series Network, Xd

The resulting ABCD parameters for the combined network shown in Figure A1-11 are given in Equation A1-19.

$$A := \frac{(DEN3 + NUMA1 + Xd \cdot NUMC1)}{DEN4} \qquad B := \frac{(DEN3\,(Xds + Xd) + Xd \cdot NUMD1)}{DEN4}$$

$$C := \frac{NUMC1}{DEN4} \qquad D := \frac{DEN3 + NUMD1}{DEN4} \qquad \text{[A1-19]}$$

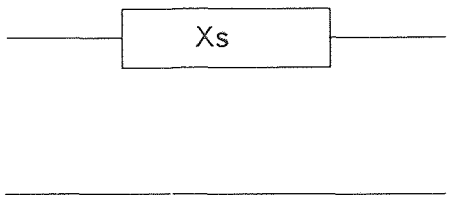


**Figure A1-12** Series Network, Xs

The final step is the series cascading of the previous result, Figure A1-11, with the reactive two-port network Xs shown in Figure A1-12. The ABCD parameters for this network are as follows in Equation A1-20. The resulting two-port network and the corresponding ABCD parameters are given in Figure A1-13 and Equation A1-21 respectively.

$$A := 1 \qquad B := Xs$$

$$C := 0 \qquad D := 1 \qquad \text{[A1-20]}$$

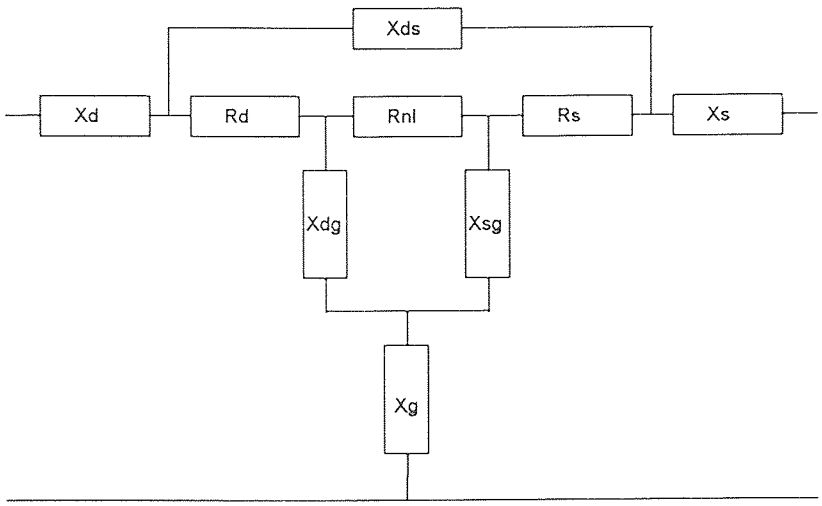


**Figure A1-13** Two-Port Representation of Complete NLE Model

$$S11 := \frac{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND + (NA - ND - (Zo + Xs - Xd)\cdot(NC))\cdot Zo}{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND + (NA + ND + 2\cdot D3 + (Zo + Xs + Xd)\cdot(NC))\cdot Zo}$$

$$S12 := \frac{2\cdot Zo\cdot D4}{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND + (NA + ND + 2\cdot D3 + (Zo + Xs + Xd)\cdot(NC))\cdot Zo}$$

$$S21 := \frac{2\cdot Zo\cdot D4}{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND + (NA + ND + 2\cdot D3 + (Zo + Xs + Xd)\cdot(NC))\cdot Zo}$$

$$S22 := \frac{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND - (NA - ND + (Zo + Xd - Xs)\cdot NC)\cdot Zo}{Xs\cdot(D3 + NA + Xd\cdot NC) + D3\cdot(Xds + Xd) + Xd\cdot ND + (NA + ND + 2\cdot D3 + (Zo + Xs + Xd)\cdot(NC))\cdot Zo}$$

[A1-21]

# APPENDIX II

## LIBRA MODEL CIRCUIT FILE

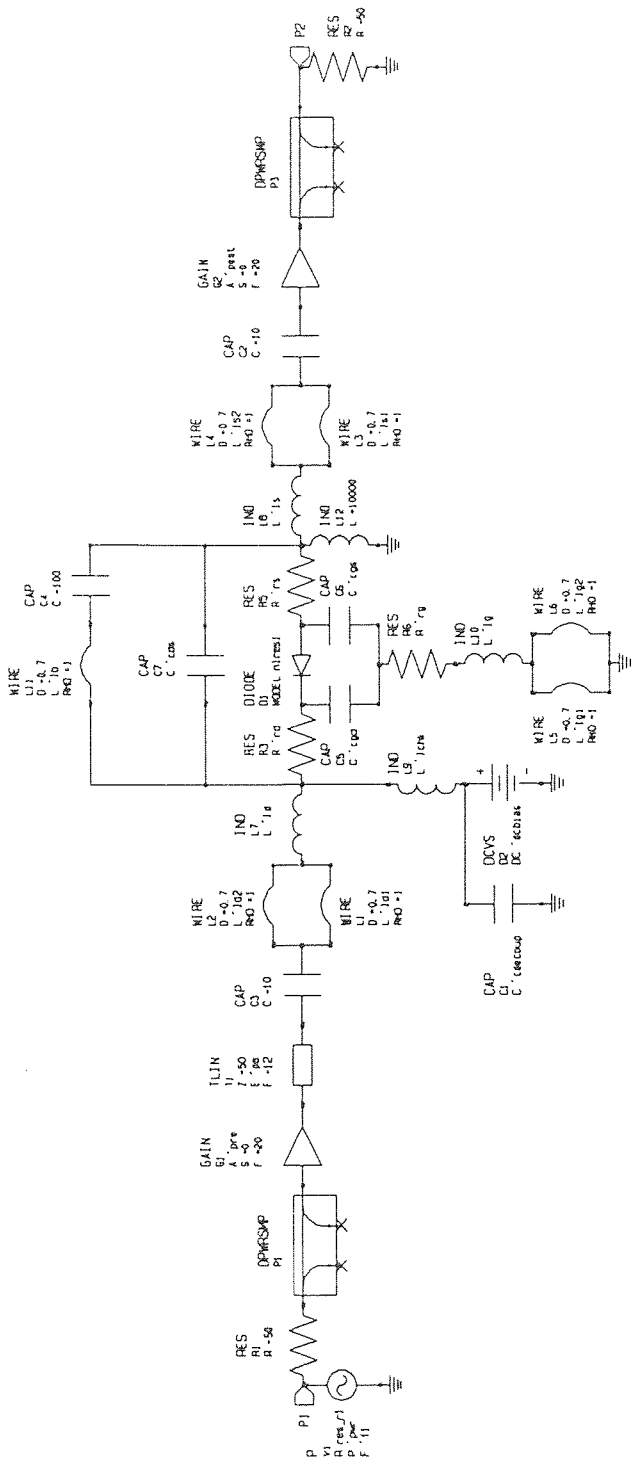

**Figure AII-1** Libra Model Schematic Representation

The Libra model circuit schematic is shown in Figure AII-1. The figure illustrates the components necessary to simulate the entire linearizer/TWTA system. The model takes into account the physical layout of the device in a fixture including input and output dc blocking capacitors and the bond wires connecting the transmission line to the device. The directional coupler elements are used to detect the incident and reflected signals from which the transducer gains and reflection coefficients are calculated. The dc power supply is used to simulate gate bias control.

When the basic NLE dynamic model is embedded within a linearizer/TWTA combination, the gain block elements are necessary to control the level into the linearizer and the gain between the linearizer and the TWTA. This allows the gain and phase expansion of the linearizer to be aligned with the corresponding gain and phase compression of the TWTA.

In order to obtain the linearizer/TWTA system output, the calculated S-parameters of the linearizer/gain block combination are input into a power series expansion of the TWTA gain and phase response. This enables the system gain and phase response to be determined. These calculations are all done in the equation block contained in the Libra circuit file included in this appendix.

```
ACADEMY (TM) Ver. 3.500.104.1  Cfg. (210 N202 5 0 8953 1 0 D0F)
bbmode.ckt

DIM
FREQ      GHZ
RES       OH
COND      /OH
IND       NH
CAP       PF
LNG       MIL
TIME      PS
ANG       DEG
VOL       V
CUR       A
PWR       DBM

VAR
dcbias = 1.28
is1 #0 .25 .1
n1 #0 1.95 10
rsd #0 -.4 10
tt #0 1E-12 1e-10
cgd #0 .048030 1
cgs #0 .265174 1
ld #0 .000112 1
ls #0 .512426 1
lg #0 .069777 1
rg #0 1.912534 10
cds #0 .043509 1
pa = -75
lchk = 10000
cdecoup = 10
rd #0 4 10
rs #0 .05 10
ld1 = 0
ld2 = 0
ls1 = 0
ls2 = 0
lg1 = 0
lg2 = 0


EQN
```

CKT

RES_R3 7 2 R^rd
RES_R5 3 10 R^rs
CAP_C5 2 5 C^cgd
CAP_C6 3 5 C^cgs
RES_R6 5 16 R^rg
CAP_C7 7 10 C^cds
TLIN_T1 1 12 Z=50.0000000000 E^pa F=12.0000000000
WIRE_L1 4 22 D=0.70000000000 L^ld1 RHO=1.00000000000 AF? CO? A1? A2?
WIRE_L2 4 22 D=0.70000000000 L^ld2 RHO=1.00000000000 AF? CO? A1? A2?
WIRE_L3 21 15 D=0.70000000000 L^ls1 RHO=1.00000000000 AF? CO? A1? A2?
WIRE_L4 21 15 D=0.70000000000 L^ls2 RHO=1.00000000000 AF? CO? A1? A2?
WIRE_L5 19 0 D=0.70000000000 L^lg1 RHO=1.00000000000 AF? CO? A1? A2?
WIRE_L6 19 0 D=0.70000000000 L^lg2 RHO=1.00000000000 AF? CO? A1? A2?
DPWRSMP_P1 6 1 8 9
DIODE_D1 3 2 [MODEL=nlres1]
CAP_C1 17 0 C^cdecoup
DPWRSMP_P3 13 11 18 20
IND_L7 22 7 L^ld
IND_L8 10 21 L^ls
IND_L10 16 19 L^lg
CAP_C2 15 13 C=10.0000000000
CAP_C3 12 4 C=10
IND_L12 10 0 L=10000.0000000
DEF2P 6 11 MODE3
TERM

PROC

MODEL

nlres1 d is^is1 n^n1 rs^rsd tt^tt

SOURCE
MODE3 RES_R1 14 6 R=50.0000000000
MODE3 RES_R2 11 0 R=50.0000000000
MODE3 P_V1 14 0 R=res_r1 P^pwr F^f1
MODE3 VS_D2 17 0 DC^dcbias
MODE3 IND_L9 17 7 L^lchk

DCTR

```
FREQ
NH=3

SWEEP 1 18 2
!STEP 12.2

POWER

STEP -20,0
!SWEEP -20 0 2

FILEOUT

mode3 hb pdspar ./freq

OUTVAR

pa1 = mode3 spw_pa1 8 r=match h1=1
pb1 = mode3 spw_pb1 9 r=match h1=1
pa2 = mode3 spw_pa2 18 r=match h1=1
pb2 = mode3 spw_pb2 13 r=match h1=1

vd1 = mode3 vfc 3 2 h1=1
id1 = mode3 ifc diode_d1 h1=1

OUTEQN

s21 = pb2/pa1
dbs21 = 20*log(mag(s21))

s11 = pb1/pa1
dbs11 = 20*log(mag(s11))

s12 = pb1/pa2
dbs12 = 20*log(mag(s12))

s22 = pb2/pa2
dbs22 = 20*log(mag(s22))

res1 = vd1/id1
```

```
OUT

outeqn re[dbs21] gr1
outeqn ang[s21] gr2

outeqn re[dbs11] gr3
outeqn ang[s11] gr4

outeqn re[res1] gr5


GRID

freq 1 18 1
!power -20 0 2

!gr1 -14 -6 1
gr1 0 -20 2
!gr2 -45 -75 5
gr2 -45 45 10
gr3 0 -20 2
gr4 0 -90 10
gr5 0 450 50

HBCNTL

OPT

YIELD

TOL
```

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