Fall 2018

ECE 353 - Computer Architecture and Organization

John Carpinelli

ECE 353-001: Computer Architecture and Organization (3-0-3)

Instructor: John Carpinelli, 315 ECEC, (973) 596-3536
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Office hours: Wednesdays and Fridays 10:00-11:25; or by appointment
Meeting times: Wednesdays and Fridays 8:30-9:55, ECEC 115

Text: *Computer Systems Organization and Architecture*, Addison-Wesley, John D. Carpinelli, Boston, MA, 2001, ISBN # 0-201-61253-4.

Description: This course emphasizes the hardware design of computer systems. Topics include register transfer logic, central processing unit design, microprogramming, ALU design, pipelining, vector processing, micro-coded arithmetic algorithms, I/O organization, memory organization and multiprocessing.

Course Outcomes:

1) The student will be able to design the instruction set architecture for a processor to meet specific computer requirements.
2) The student will be able to evaluate the tradeoffs in the design of an instruction set architecture and the processor that implements it.
3) The student will be able to design a system to meet a given specification using register transfer language.
4) The student will be able to design a basic CPU given the instruction set architecture using either hardwired or microcoded control.
5) The students will be able to design a hierarchical memory system to meet a given specification.
6) The student will be able to design an I/O system to meet a given specification.

Student Outcomes:

(a) an ability to apply knowledge of mathematics, science, and engineering (CLO2, 3)
(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability (CLO 1)
(e) an ability to identify, formulate, and solve engineering problems (CLO 2, 3, 4, 5, 6)

Course Schedule:

Week	Topic
1	Instruction Set Architectures
2	Basic Computer Organization
3,4	Register Transfer Languages
4,5	CPU Design - Hardwired Control***, Test #1***
6,7	Microsequencers Control Unit Design
8,9	Computer Arithmetic, ***Test #2***
10,11	Memory Organization
11,12	I/O Organization
13	RISC Processing, ***Test #3***
14	Parallel Processing

Grading Policy:		
	Homeworks/Quizzes	10%
	3 Tests @ 15/20/25%	60%
	Final Exam	30%

Honor Code: The NJIT Honor Code will be upheld, and any violations will be referred to the Dean of Students for disciplinary action.