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Correlation of drain breakdown with excess noise and other surface-related phenomena in enhancement MOSFETS

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CORRELATION OF DRAIN BREAKDOWN WITH EXCESS NOISE AND OTHER SURFACE-RELATED PHENOMENA IN ENHANCEMENT MOSFETS

BY

JERRY J. RIJ

A THESIS

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FOR

DEPARTMENT OF ELECTRICAL ENGINEERING
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ABSTRACT

An investigation of semiconductor surface-related phenomena has been undertaken to correlate 1/F noise with drain breakdown in p-channel enhancement MOSFET's. Increases in the intensity of drain current fluctuations at 10 Hz and at 1 KHz, particularly at the higher frequency, was observed following accelerated life-testing for threshold voltage drift. It was concluded that mobile ions near the oxide-semiconductor interface produce a sharp increase in fast surface states and that these states may be regarded as fast trapping centers. It was also found that the 1/F noise intensity consistently peaked at the threshold of drain breakdown and that it steadily decreased with further increases in drain current. Of all the transistors tested, those with relatively low noise intensity were found to exhibit sharper breakdown characteristics and higher breakdown voltages while those transistors with high noise showed soft breakdown characteristics. It was therefore concluded that low noise MOS transistors are superior to those with relatively high noise and that the 1/F noise - drain current characteristics may be used in nondestructive testing to determine the approximate drain breakdown voltage.

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A	Area of gate metalization in cm^2
$\mathring{A}$	Angstrom unit, 10^{-10} meters, 10^{-8} cm
B	Bandwidth in cycles per second, hertz, Hz
c	Capture rate probability
c_s	Capture rate probability at the $Si-SiO_2$ interface
C_B	Impurity concentration in the substrate per cm^3
C_O	Capacitance of the oxide layer in Farads/cm^2
C_S	Capacitance of the semiconductor space-charge region in Farads/cm^2
E	Surface-state energy in electron volts, eV
E_B	Barrier potential to be exceeded in the tunneling mechanism of holes
E_C	Conduction-band energy level
E_F	Fermi energy level
E_V	Valence-band energy level
$\mathcal{E}_T$	Transverse electric field in the channel depletion region between the expop (extrapolated pinch-off point) and the drain-to-substrate junction
F, f	Frequency in cycles per second
f_T	Quasi-Fermi function of surface states
f_{TP}	$1 - f_T$
G	The rate that surface states of energy E located at a distance x into the oxide layer gain holes
G_M	Transconductance in $ohms^{-1}$, mhos
g_{dSAT}	Small-signal saturation drain conductance in $ohms^{-1}$
$\hbar$	Planck's constant, 4.136×10^{-15} eV·second

$\overline{i^2}$	Mean squared noise current with drain shorted in mA^2/cycle
I_D	Drain current
I_{DSAT}	Saturation drain current
I_{DSAT}^*	Saturation drain current when $V_D = V_{DSAT}$
I_{DSS}	Drain leakage current when the gate is returned to the source, the source and substrate are common, and the drain-to-source voltage is 10 volts
J	Current density
k	Boltzmann's constant, 8.617×10^{-5} eV.°K^{-1}
K	Material constant
K_o	Relative permittivity of SiO_2, 3.54×10^{-13} Farad/cm
K_s	Relative permittivity of silicon
kT	Energy level, 0.0258eV at T = 300°K
ℓ	Length of diffusion of surface states from the Si-SiO_2 interface
L	Effective channel length (in the direction of current flow)
ΔL	Length by which the conducting channel is shortened when V_{DS} exceeds V_{DSAT}
m^*	Effective mass of a hole, 9.108×10^{-31} Kg
N_A	Acceptor doping density per cm^3
N_D	Donor doping density per cm^3
$N_T(E)$	Surface-state density of free holes and electrons in cm^{-3}.eV^{-1}
n_{si}	Free electron concentration at the surface when the Fermi level is at the surface-state level
n_{so}	Steady-state value of n_{si}
$n_\tau(\varepsilon)$	Empty surface states at energy E located at a distance x from the Si-SiO_2 interface
P^+	Heavy p-type diffusion (10^{18} to 10^{20} cm^{-3})

p_s	HOLE DENSITY IN THE INVERTED CHANNEL IN $CM^{-3}.eV^{-1}$
p_{s1}	FREE HOLE CONCENTRATION AT THE SURFACE WHEN THE FERMI LEVEL IS AT THE SURFACE-STATE LEVEL
p_{s0}	STEADY-STATE VALUE OF p_{s1}
Q_{SS}	SURFACE-STATE CHARGE IN COULOMBS
q	MAGNITUDE OF ELECTRONIC CHARGE, 1.602×10^{-19} COUL
R	RESISTANCE IN OHMS
$\mathcal{R}$	RATE THAT SURFACE STATES OF ENERGY E LOCATED AT A DISTANCE X INTO THE OXIDE LAYER LOSE HOLES
$S_{i(\omega)}$	SHORT-CIRCUIT DRAIN CURRENT NOISE SPECTRAL INTENSITY (DRAIN CURRENT FLUCTUATIONS IN MOSFET's)
$S_{p_T(\omega)}$	SPECTRAL INTENSITY OF THE TRAPPED HOLE DENSITY FLUCTUATION
T	TEMPERATURE IN DEGREES KELVIN, °K
v	VOLUME
V_D	DRAIN VOLTAGE
V_{DS}	DRAIN-TO-SOURCE VOLTAGE
V_{DSAT}	DRAIN VOLTAGE WHICH CAUSES CHANNEL PINCH-OFF
V_{FB}	FLAT-BAND VOLTAGE NECESSARY TO COUNTER BALANCE THE WORK FUNCTION DIFFERENCE BETWEEN THE METAL-OXIDE BARRIER ENERGY AND THE SILICON-OXIDE BARRIER IN AN MOS TRANSISTOR
V_G	GATE VOLTAGE
V_G'	EFFECTIVE GATE VOLTAGE
V_{GS}	GATE-TO-SOURCE VOLTAGE
V_{GSUB}	GATE-TO-SUBSTRATE VOLTAGE
V_T	THRESHOLD VOLTAGE
x	DISTANCE FROM THE $Si-SiO_2$ INTERFACE
x_0	THICKNESS OF THE OXIDE LAYER
z	PARABOLIC RATE CONSTANT FOR GROWTH OF SiO_2

α	CAPTURE RATE TIME CONSTANT
β	GAIN TERM
$\gamma, \eta, \theta, \lambda$	EXPONENTS OF R, f, J, V IN BELL'S GENERAL EQUATION FOR FREQUENCY-DEPENDENT NOISE
δ	INFINITESIMALLY SMALL INCREMENT
ϵ_o	PERMITTIVITY OF FREE SPACE, 8.86×10^{-14} FARAD/CM
ξ, ξ	FIELD FRINGING FACTORS EXPERIMENTALLY FOUND TO BE 0.2 AND 0.6, RESPECTIVELY
μ_n	MOBILITY OF ELECTRONS IN CM^2/VOLT·SECOND
μ_p	MOBILITY OF HOLES IN CM^2/VOLT·SECOND
π	PI, 3.1415926
ρ	RESISTIVITY
s	SHAPE FACTOR, EG. CROSS-SECTION/UNIT LENGTH
τ	TIME CONSTANT FOR SURFACE-STATE CHARGE DENSITY FLUCTUATION
τ_s	TIME CONSTANT FOR SURFACE STATES LOCATED RIGHT AT THE $Si-SiO_2$ INTERFACE
ϕ	ELECTROSTATIC POTENTIAL WITH REFERENCE TO THE BULK SEMICONDUCTOR MATERIAL
ϕ_F	ELECTROSTATIC POTENTIAL AT THE FERMI LEVEL; THE AMOUNT BY WHICH THE FERMI LEVEL IS DISPLACED FROM THE INTRINSIC LEVEL OR THE CENTER OF THE GAP (AS MEASURED IN THE BULK)
ϕ_s	ELECTROSTATIC POTENTIAL AT THE SURFACE; THE AMOUNT BY WHICH THE INTRINSIC FERMI LEVEL, AT THE SURFACE, HAS BEEN CHANGED WITH RESPECT TO THE FERMI LEVEL
χ	GENERAL CONSTANT IN THE SIMPLIFICATION OF BELL'S EQUATION FOR 1/F NOISE
ω	ANGULAR FREQUENCY IN RADIANS PER SECOND

CHAPTER 1

INTRODUCTION AND THEORY OF MOSFET OPERATION

1.1 Introduction to Basic MOS Devices

The basic metal-oxide-semiconductor field-effect transistor (MOSFET) is composed of two heavily-doped regions, the source and drain, diffused into a semiconductor substrate and separated by a channel. An insulated metal gate above the channel modulates majority carrier conduction from the source to the drain by field effects.

Two types of devices are commercially available: the p-channel MOSFET (in which holes are the majority carriers) and the n-channel MOSFET (in which the majority carriers are electrons). In addition, there are two common modes of operation: the enhancement-mode (in which the device is normally off and channel conduction is enhanced by the appropriate gate voltage) and the depletion-mode (in which the channel normally conducts and a gate voltage depletes it of majority carriers). Until recently, it was customary to produce primarily either p-channel enhancement- or n-channel depletion-mode MOS transistors. However, complimentary MOS integrated circuits consisting of pairs of both p- and n-channel transistors on a single chip are replacing a large portion of the bipolar devices in use today.

1.2 Theory of MOSFET Operation

Modulation of channel conduction. Figure 1-1 shows the geometric construction of a P-channel enhancement-mode MOS transistor properly biased for channel conduction. Such devices require a sufficiently negative gate voltage before the channel becomes inverted. This then forms a P type conducting path between the source and the drain, the conductivity of which is enhanced with increasingly negative gate bias. N-channel enhancement MOSFET's have N^+ source and drain regions and require a drain and gate bias of opposite polarity to those of P-channel MOS transistors in order to operate. Depletion-mode devices have a built-in conducting channel beneath the oxide of the same type of material used for their respective drain and source regions.

Figure 1-2A is a lateral view taken in the channel between the source and drain of a P-channel enhancement MOSFET. V_{GS} is the gate bias applied between the gate and source terminals. With the source and substrate at an electrical ground, there are three gate bias conditions of interest.

Figure 1-2B illustrates the semiconductor energy bands and characteristic "band bending" when the applied V_{GS} is greater than zero. An abrupt difference is assumed between the oxide (SiO_2) and the semiconductor substrate. The energy

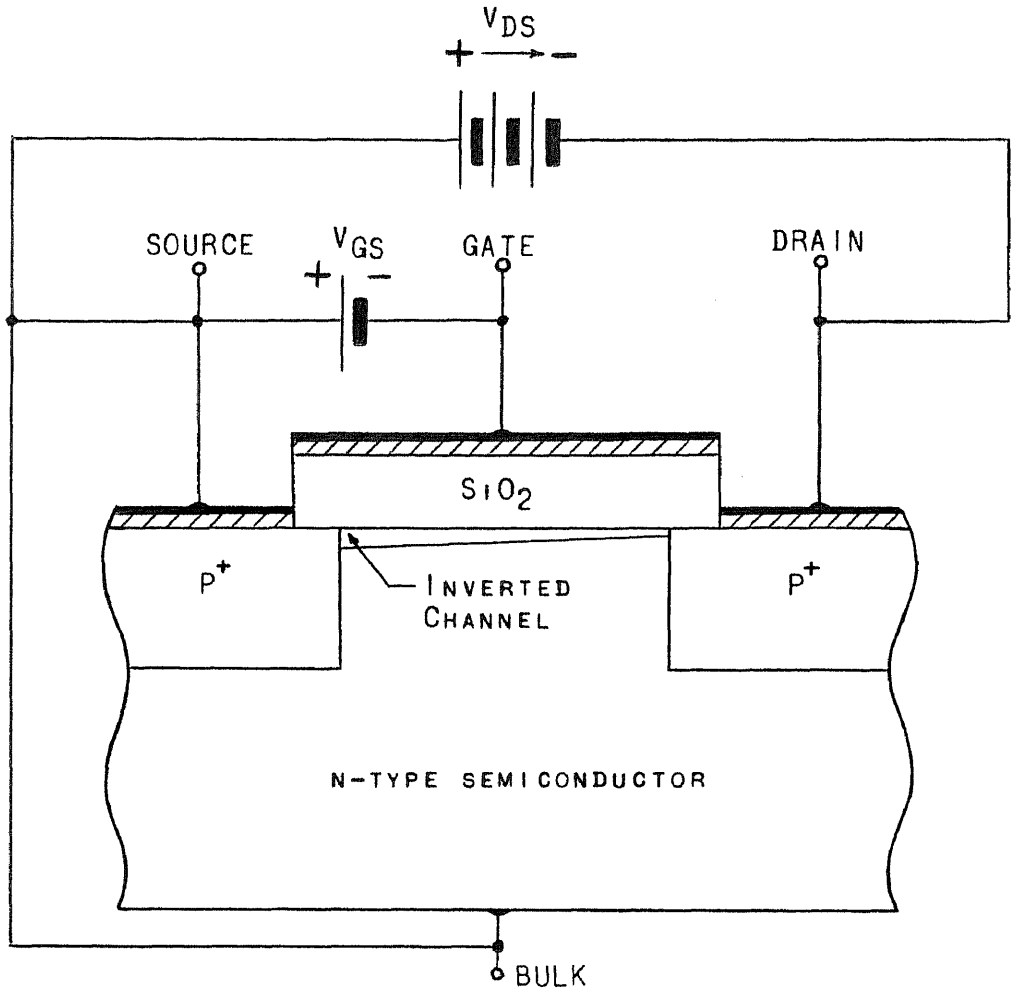

FIGURE 1-1. GEOMETRICAL CONSTRUCTION OF A P-CHANNEL ENHANCEMENT MOSFET BIASED FOR CHANNEL CONDUCTION. SUCH DEVICES HAVE ISOLATED P^+ SOURCE AND DRAIN DIFFUSIONS WITHIN AN N-TYPE SEMICONDUCTOR SUBSTRATE. AN OXIDE LAYER, USUALLY SiO_2, INSULATES THE GATE FROM THE SUBSTRATE AND PASSIVATES THE SURFACE OF THE DRAIN AND SOURCE P-N JUNCTIONS. TERMINALS ARE PROVIDED FOR THE DRAIN, GATE, AND SOURCE AND, IN SOME CASES, A SEPARATE TERMINAL FROM THE SUBSTRATE BULK MAY ALSO BE EXTERNALLY AVAILABLE. OTHERWISE, THE SUBSTRATE IS CONNECTED INTERNALLY TO THE SOURCE AND THE DEVICE IS THEN USUALLY INTENDED TO BE OPERATED WITH ONLY ONE OF THE P^+ REGIONS AS THE DRAIN.

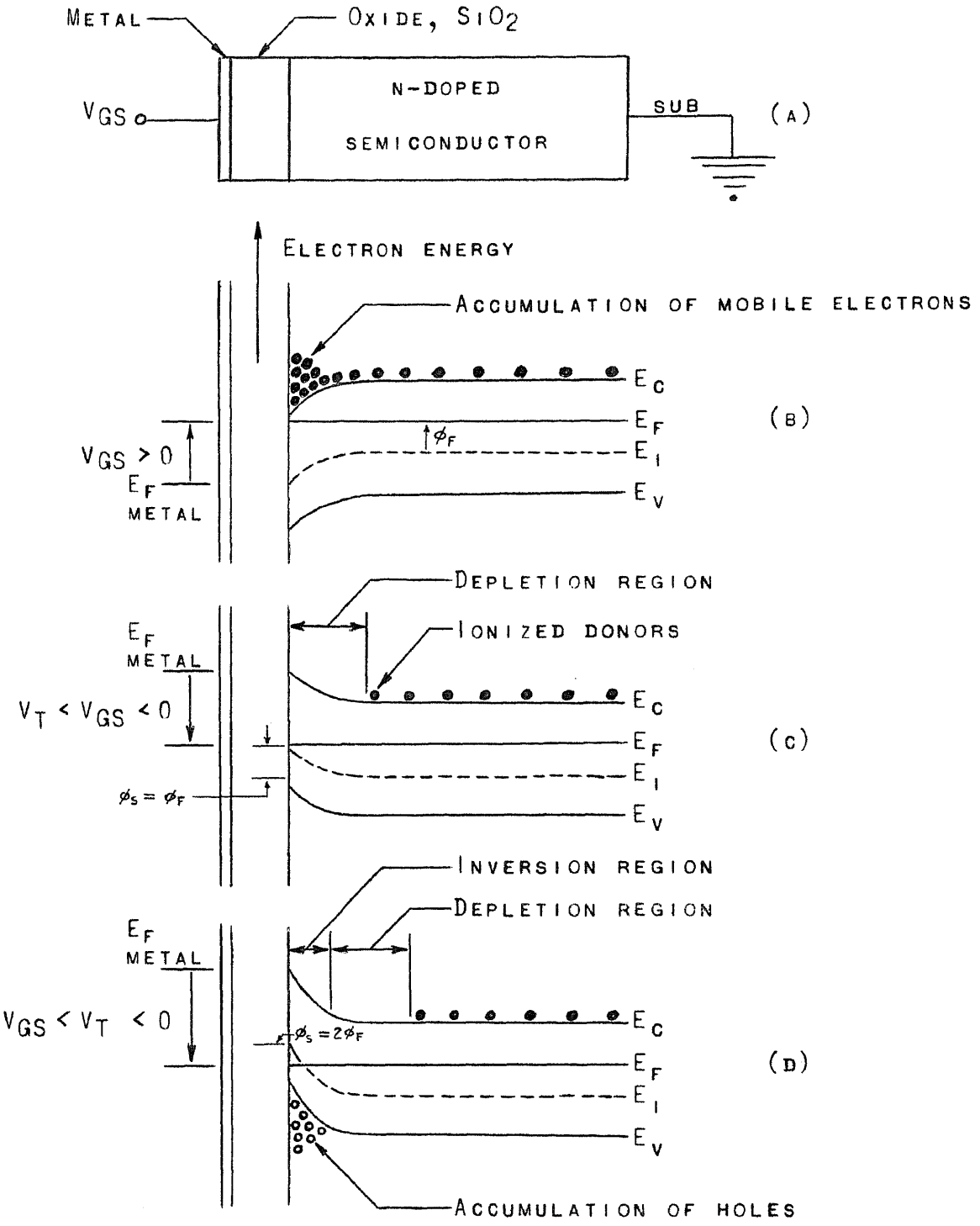

FIGURE 1-2. ENERGY BAND-BENDING NEAR THE SEMICONDUCTOR SURFACE UNDER THREE CONDITIONS OF GATE BIAS FOR A P-CHANNEL ENHANCEMENT MOSFET[1]. (B) POSITIVE V_{GS} RESULTS IN AN ELECTRON ACCUMULATION BENEATH THE OXIDE; (C) SMALL $|-V_{GS}|$ RESULTS IN DEPLETION REGION; AND (D) LARGER $|-V_{GS}|$ CAUSES SURFACE INVERSION AND AN ACCUMULATION OF HOLES.

BANDS ARE IDENTIFIED AS FOLLOWS:

E_C ELECTRON ENERGY AT THE EDGE OF THE CONDUCTION BAND

E_F ELECTRON ENERGY AT THE FERMI LEVEL, DEFINED AS THE ENERGY LEVEL AT WHICH "THE PROBABILITY OF OCCUPATION OF AN ENERGY STATE BY AN ELECTRON IS EXACTLY ONE-HALF."[2]

E_i ELECTRON ENERGY AT THE INTRINSIC FERMI LEVEL, THE FERMI LEVEL IN AN INTRINSIC SEMICONDUCTOR

E_V ELECTRON ENERGY AT THE EDGE OF THE VALENCE BAND.

A POSITIVE GATE BIAS LOWERS THE ENERGY LEVEL ASSOCIATED WITH THE SURFACE STATES DOWN NEAR THE FERMI LEVEL IN THE SEMICONDUCTOR MATERIAL. THE PROBABILITY OF THE STATES BEING OCCUPIED BY AN ELECTRON IS GREATLY INCREASED AND AN ELECTRON ACCUMULATION RESULTS BENEATH THE OXIDE.

FIGURE 1-2C SHOWS THE EFFECT OF APPLYING A SMALL NEGATIVE GATE BIAS. AS THE STATES ARE ELEVATED, THEIR PROBABILITY OF OCCUPATION BY ELECTRONS IS DECREASED. THE CHANNEL NEAR THE OXIDE BECOMES DEPLETED OF ELECTRONS. THIS RESULTS IN A DEPLETION REGION WHICH CONSISTS OF MOSTLY BOUND IONS OF IMPURITY ATOMS.

WHEN THE GATE BIAS IS SUFFICIENTLY NEGATIVE, THE PROBABILITY OF OCCUPATION APPROCHES ZERO. ENOUGH ELECTRONS ARE THEN DISPLACED FROM THE SEMICONDUCTOR SURFACE (HEREAFTER REFERRED TO SIMPLY AS THE SURFACE) THAT THEY BECOME THE MINORITY CARRIERS, WHILE HOLES BECOME DOMINANT. FIGURE 1-2D

SHOWS A NET ACCUMULATION OF HOLES IN THE SUBSTRATE DIRECTLY BENEATH THE OXIDE. WHEREAS THE CHANNEL WAS HITHERTO COMPOSED OF N-DOPED SILICON, THE SURFACE IS NOW WITHIN AN INVERSION REGION, THEREBY ALLOWING A HOLE CURRENT TO FLOW FROM THE SOURCE TO THE DRAIN WHEN THE DRAIN IS BIASED AT A POTENTIAL NEGATIVE WITH RESPECT TO THE SOURCE.

THE NEGATIVE GATE VOLTAGE WHICH PERMITS A CURRENT OF TEN MICROAMPERES TO FLOW WITH AN APPLIED $-V_{DS}$ EQUAL TO $-V_{GS}$ IS DEFINED TO BE THE THRESHOLD VOLTAGE, V_T. IT IS SO-NAMED BECAUSE IT IS AT THIS POTENTIAL THAT THE SURFACE IS AT THE THRESHOLD OF INVERSION.

IT IS EVIDENT THAT THE DEPTH, AND SO THE CONDUCTANCE, OF THE CONDUCTING CHANNEL MAY BE EASILY MODULATED BY VARIATIONS IN THE APPLIED GATE VOLTAGE. THE MOS TRANSISTOR ACQUIRES ITS PROPERTY OF AMPLIFICATION FROM THE FACT THAT A RELATIVELY SMALL VARIATION IN V_{GS} INDUCES A LARGE VARIATION IN DRAIN CURRENT.

OPERATION BEYOND CHANNEL PINCH-OFF. FIGURE 1-3A SHOWS A CROSS-SECTION OF A P-CHANNEL ENHANCEMENT-MODE TRANSISTOR WITH GATE VOLTAGE LARGE ENOUGH TO ESTABLISH A CONDUCTING CHANNEL BETWEEN THE SOURCE AND DRAIN. IN THE COMMON—SOURCE CONFIGURATION IT IS CUSTOMARY TO GROUND THE SOURCE AND SUBSTRATE BULK AND APPLY A NEGATIVE VOLTAGE TO THE DRAIN. A SMALL $|-V_{DS}|$ RESULTS IN THE BIAS CONDITION FORMERLY ILLUSTRATED IN FIGURES 1-1 AND 1-2D ABOVE.

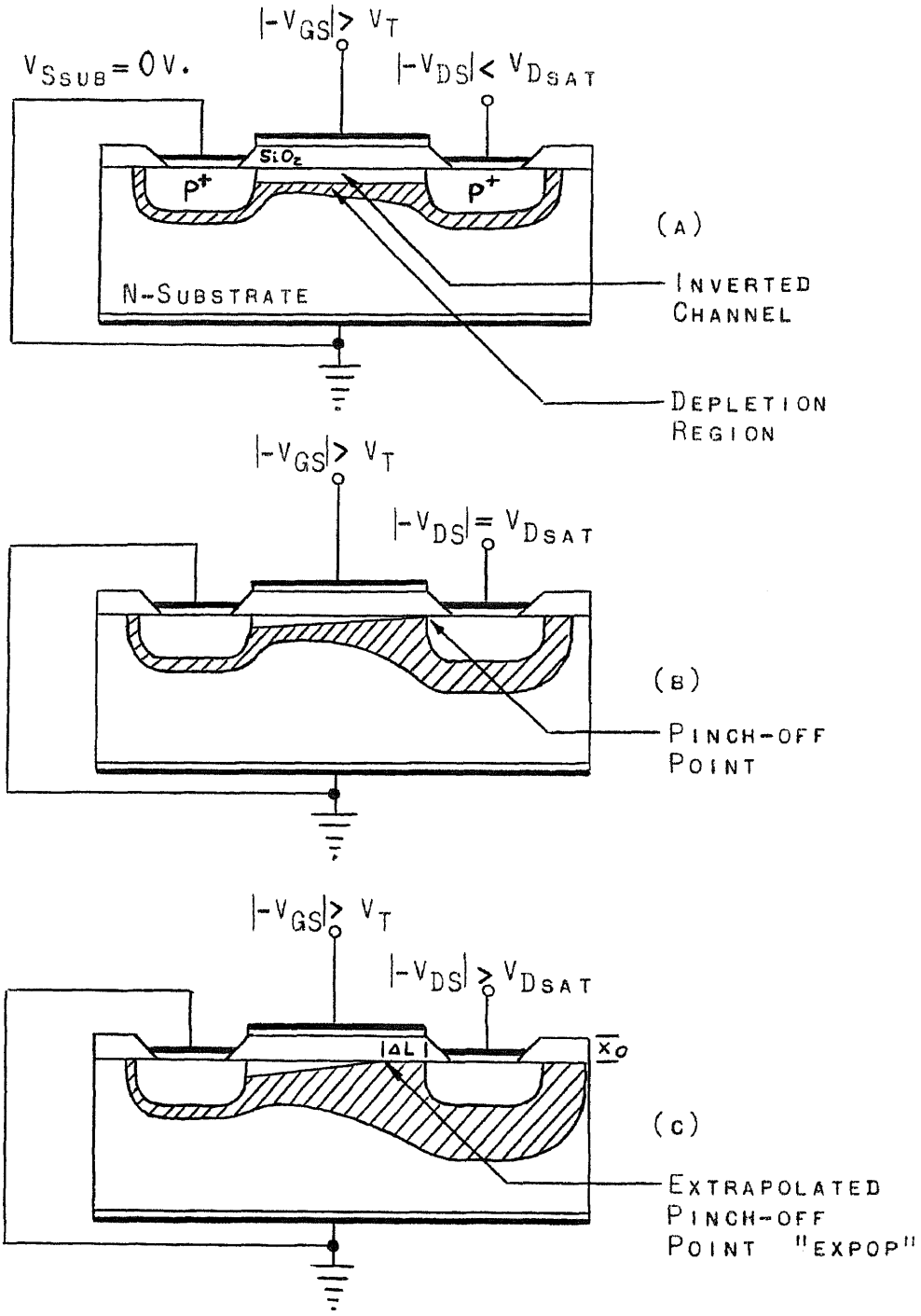

FIGURE 1-3. EFFECTS OF INCREASING $|-V_{DS}|$ ON THE INVERSION REGION OF A P-CHANNEL ENHANCEMENT MOSFET. (A) CONDITION WITH SMALL $|-V_{DS}|$; (B) PINCH-OFF CONDITION; AND (C) CONDITION BEYOND CHANNEL PINCH-OFF.

SINCE BOTH THE DRAIN AND SOURCE REGIONS ARE OF P^+ TYPE SILICON (N_A BETWEEN 10^{18} AND 10^{20} CM^{-3}) IN AN N-DOPED SEMICONDUCTOR SUBSTRATE ($N_D \simeq 10^{15}$ CM^{-3}), THERE IS A NATURAL RECOMBINATION PROCESS AS ELECTRONS FILL HOLES NEAR THE P-N JUNCTIONS. WITH THE DRAIN AND SOURCE HEAVILY DOPED, RECOMBINATION EXTENDS MUCH FURTHER INTO THE SUBSTRATE THAN INTO EITHER THE SOURCE OR THE DRAIN. THIS RESULTS IN A SPACE-CHARGE DEPLETION REGION AROUND THE SOURCE AND DRAIN JUNCTIONS. FURTHERMORE, SINCE THE SUBSTRATE IS ELECTRICALLY CONNECTED TO THE SOURCE, ANY APPLIED $-V_{DS}$ REVERSE BIASES THE DRAIN-TO-SUBSTRATE P-N JUNCTION, THEREBY FURTHER INCREASING THE WIDTH OF THAT PARTICULAR DEPLETION REGION.[3]

IF $|-V_{DS}|$ IS SMALL COMPARED TO $|-V_{GS}|$, THERE IS A LINEAR DROP IN POTENTIAL ALONG THE CHANNEL AS HOLE CURRENT PROCEEDS FROM THE SOURCE TO THE DRAIN. IN THIS CONDITION, THE DRAIN CURRENT $-I_D$ (NEGATIVE TO INDICATE THAT THE MAJORITY CARRIERS ARE HOLES) IS LINEARLY PROPORTIONAL TO $|-V_{DS}|$ AND THE TRANSISTOR IS SAID TO BE OPERATING IN THE LINEAR PORTION OF ITS I-V (CURRENT-VOLTAGE) CHARACTERISTICS.

IT IS EVIDENT THAT AS $|-V_{DS}|$ IS INCREASED, THE DIFFERENCE IN POTENTIAL BETWEEN THE GATE AND DRAIN TERMINALS IS LESSENED. SINCE THE INVERSION REGION IS DEPENDENT UPON THE ELECTRIC FIELD ACROSS THE OXIDE, WHICH IS A FUNCTION OF THE POTENTIAL DIFFERENCE ACROSS EACH DIFFERENTIAL ELEMENT OF THE OXIDE ALONG THE CHANNEL, THE WIDTH OF THE INVERSION REGION IS

DIRECTLY PROPORTIONAL TO THE ELECTRIC FIELD INTENSITY IN THAT PORTION OF THE OXIDE DIRECTLY ABOVE IT. CONSEQUENTLY, AS $|-V_{DS}|$ INCREASES, THE FIELD IN THE OXIDE AT THE DRAIN-END OF THE CHANNEL DECREASES. EVENTUALLY, IF $|-V_{DS}|$ IS MADE HIGH ENOUGH, THE FIELD INTENSITY IS UNABLE TO SUPPORT CHANNEL INVERSION NEAR THE DRAIN-TO-SUBSTRATE JUNCTION.[4] FIGURE 1-3B ILLUSTRATES THIS EFFECT AT THE ONSET OF CHANNEL PINCH-OFF, A CONDITION MARKED BY ESSENTIALLY ZERO CHANNEL DEPTH AT THE DRAIN-END.*

FIGURE 1-3C SHOWS THE EFFECT OF FURTHER INCREASING $|-V_{DS}|$. THE LENGTH OF THE INVERTED CHANNEL DECREASES BY AN AMOUNT ΔL AND THE EXPOP (EXTRAPOLATED PINCH-OFF POINT AT THE TIP OF THE INVERSION REGION) RECEDES TOWARD THE SOURCE. IF THE RESISTIVITY OF THE INVERTED REGION IS AVERAGED OVER ITS ENTIRE LENGTH, ANY SHORTENING YIELDS A DECREASE IN CHANNEL RESISTANCE AND A CORRESPONDING INCREASE IN DRAIN CURRENT.

IF IT IS ASSUMED THAT A DIFFERENTIAL INCREASE IN DRAIN VOLTAGE BEYOND THAT REQUIRED FOR SATURATION IS ACCOMPANIED BY A DIFFERENTIAL INCREASE IN DRAIN CURRENT DUE ENTIRELY TO A DIFFERENTIAL REDUCTION IN CHANNEL LENGTH, THEN THE INSTAN-

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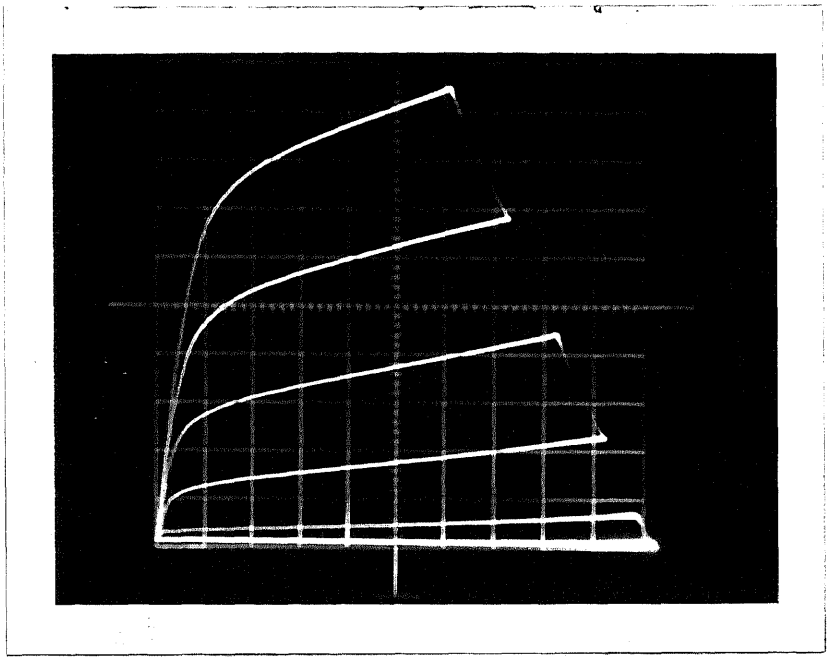
*ACTUALLY, THE CHANNEL DEPTH MUST BE SOME FINITE DIMENSION IN ORDER FOR DRAIN CURRENT TO FLOW. "ZERO CHANNEL DEPTH" IS AN APPROXIMATION USED FOR THE CONVIENCE OF DEFINING THE CHANNEL PINCH-OFF CONDITION. REFER TO SOURCES 1969-2 AND 1965-6 IN THE BIBLIOGRAPHY FOR A MORE DETAILED EXPLANATION OF THE SATURATION PHENOMENA.

DRAIN CURRENT, $-I_D$, 2MA/DIVISION



DRAIN VOLTAGE, $-V_{DS}$, 5 VOLTS/DIVISION

GATE VOLTAGE IN ONE VOLT INCREMENTS
STARTING FROM $V_{GS} = -6$ VOLTS

FIGURE 1-4. PHOTOGRAPH SHOWING THE CURRENT-VOLTAGE CHARACTERISTICS OF A TYPICAL P - CHANNEL ENHANCEMENT MOSFET. THE CURVES WERE TAKEN FROM A TETRONIX TYPE 527 TRANSISTOR CURVE TRACER WITH A SLIGHT MODIFICATION WHICH ALLOWED FOR VARIATIONS IN APPLIED GATE VOLTAGE.

TANEOUS SLOPE OF THE I-V CHARACTERISTICS IN THE SATURATION REGION YIELDS THE SMALL-SIGNAL SATURATION DRAIN CONDUCTANCE. THIS QUANTITY MAY BE EXPRESSED BY THE FOLLOWING:[5]

$$g_{d\,SAT} = \frac{\partial I_{DSAT}}{\partial V_D} = \frac{\partial I_{DSAT}}{\partial L} \cdot \frac{\partial L}{\partial V_D} \qquad 1\text{-}1$$

FIGURE 1-4 SHOWS THE I-V CHARACTERISTICS OF A TYPICAL P-CHANNEL ENHANCEMENT MOSFET. THE LINEAR AND SATURATION REGIONS ARE LABELED. IT IS EVIDENT THAT CHANNEL SHORTENING YIELDS A FINITE OUTPUT RESISTANCE FOR MOS TRANSISTORS.

1.3 Previous Investigations of the Saturation Phenomenon

FROHMAN-BENTCHKOWSKY AND GROVE[6] AND OTHERS[7,8] HAVE STUDIED MOSFET SATURATION CONDUCTANCE IN TERMS OF DEVICE PARAMETERS. APPENDIX A REVIEWS THE ANALYTICAL ANALYSIS OF THE EFFECTS OF OXIDE THICKNESS, ELECTRIC FIELD INTENSITY AND ASSOCIATED FRINGING EFFECTS, AND THE SEMICONDUCTOR IMPURITY CONCENTRATION ON DRAIN CONDUCTANCE. IN GENERAL, THE SATURATION DRAIN CONDUCTANCE CAN BE EXPECTED TO INCREASE WITH BOTH INCREASED OXIDE THICKNESS (SEE EQUATION A-12) AND DECREASED IMPURITY CONCENTRATION (SEE EQUATION A-9) IN THE SUBSTRATE.[9]

DEVICES WHICH EXHIBIT ABNORMALLY HIGH DRAIN CONDUCTANCE IN THE SATURATION REGION CAN THEREFORE ALSO BE EXPECTED TO HAVE A THICKER OXIDE LAYER, A LOWER SUBSTRATE IMPURITY CONCENTRATION, OR BOTH. THIS INVESTIGATION SUGGESTS THAT THE SATURATION DRAIN CONDUCTANCE IS ALSO A FUNCTION OF THE SURFACE-

STATE DENSITY AT THE OXIDE-SEMICONDUCTOR INTERFACE.

REDDI AND SAH[10] HAVE SHOWN THAT THE DRAIN-TO-SOURCE VOLTAGE REQUIRED FOR PINCH-OFF DECREASES WITH BOTH INCREASING OXIDE THICKNESS AND HIGHER BULK DOPING. SINCE SMALL INCREASES IN THE NUMBER OF IMPURITIES USED TO DOPE THE SUBSTRATE YIELD GREAT INCREASES IN THE NUMBER OF FREE CARRIERS ACCORDING TO THE FAMILIAR EQUATION,[11]

$$n p = n_i^2 = K^2 T^3 \exp(-E_G/kT) \qquad 1\text{-}2$$

WHERE $E_G = E_C - E_V$ = FORBIDDEN GAP IN eV

k = BOLTZMANN'S CONSTANT

K = MATERIAL CONSTANT, 3.87×10^{22} FOR SILICON AND 1.76×10^{22} FOR GERMANIUM AT 25°C

n = CONCENTRATION OF ELECTRONS PER cm^3

p = CONCENTRATION OF HOLES PER cm^3

T = TEMPERATURE IN °K,

IT IS REASONABLE TO EXPECT THAT A LARGER GATE BIAS IS NECESSARY TO DEPLETE, AND FINALLY INVERT THE CHANNEL WHEN THE SUBSTRATE IMPURITY CONCENTRATION IS HIGH.

FIGURE 1-5 ILLUSTRATES A P-CHANNEL ENHANCEMENT MOSFET DRAWN TO SCALE. THE CONTOURS OF THE DEPLETION REGIONS AND THE VARIOUS DIMENSIONS APPROXIMATE THEORETICAL BOUNDARIES BASED ON CUSTOMARY IMPURITY DOPING CONCENTRATIONS AND APPLIED TERMINAL VOLTAGES. SINCE THE WIDTH OF THE INVERSION REGION IS TYPICALLY LESS THAN 100Å, CHANNEL INVERSION AND DRAIN CONDUCTANCE ARE BOTH ESSENTIALLY SURFACE EFFECTS. THEREFORE,

THE CHARACTERISTICS OF THE OXIDE-SEMICONDUCTOR INTERFACE LARGELY DETERMINE THE OBSERVED PROPERTIES OF MOS TRANSISTORS.

SUCCEEDING CHAPTERS DISCUSS THE $Si-SiO_2$ INTERFACE IN MORE DETAIL. CORRELATIONS ARE MADE BETWEEN SURFACE-STATE DENSITY, SEMICONDUCTOR IMPURITY CONCENTRATION, AND BOTH THE EXCESS NOISE AND SATURATION DRAIN CONDUCTANCE PHENOMENA AND HOW THEY RELATE TO THE TYPE AND EXTENT OF DRAIN BREAKDOWN IN ENHANCEMENT-MODE MOS TRANSISTORS.

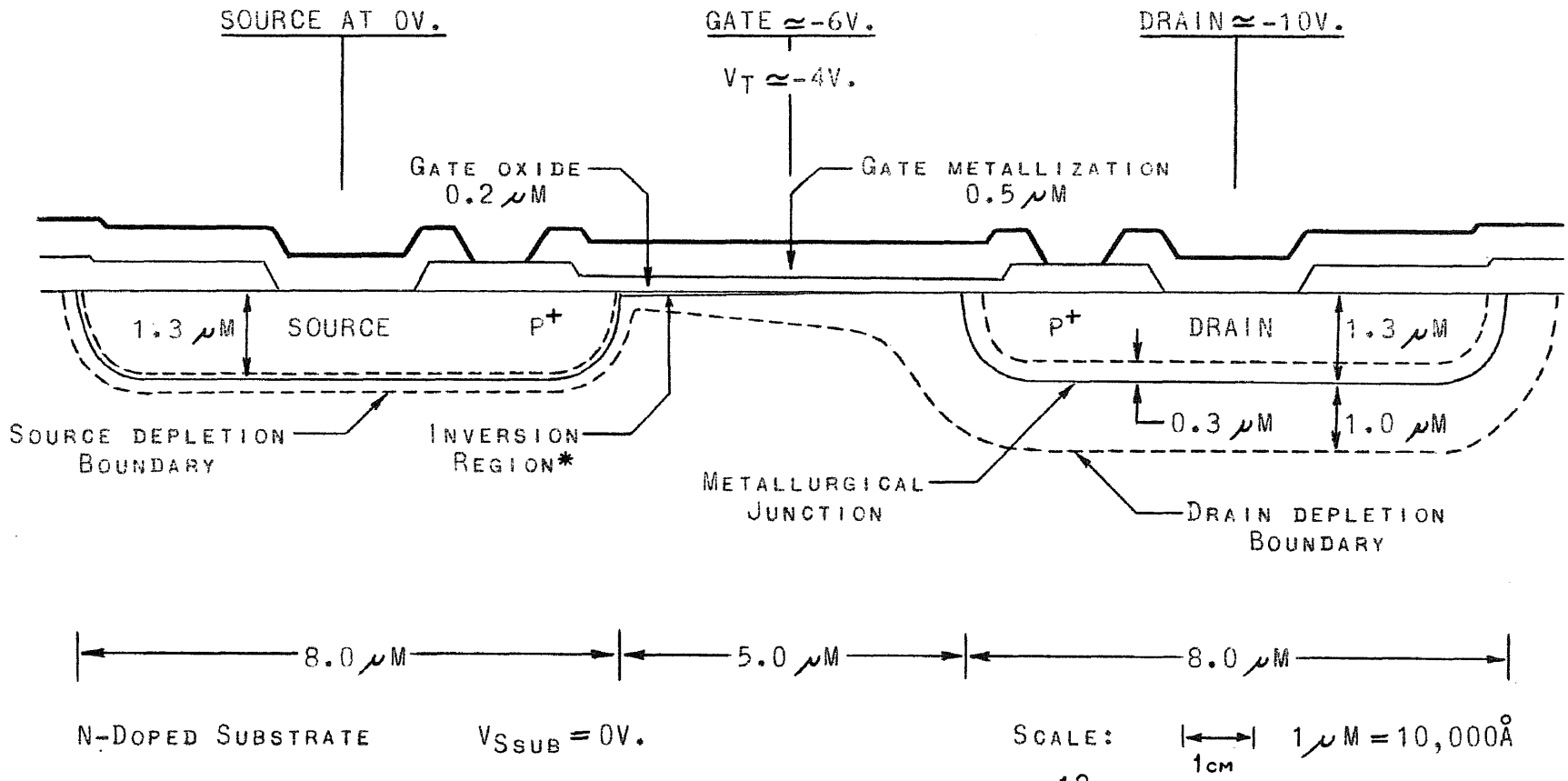


FIGURE 1-5. SCALE DRAWING OF A P-CHANNEL ENHANCEMENT MOSFET[12]
*THE INVERSION REGION IS NOT DRAWN TO SCALE

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[4]Op. Cit., Gosling et al, p. 39.

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[8]J. A. Guerst, "Theory of Insulated-Gate Field-Effect Transistors Near and Beyond Pinch-Off," Solid-State Electronics(GB) (1966), pp. 129-42. Ref. 1966-5.

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CHAPTER 2

FABRICATION AND PROPERTIES OF THE $Si-SiO_2$ INTERFACE

2.1 Introduction

Many operating characteristics of MOS field-effect transistors, particularly those which function in the enhancement mode, may be traced directly to the properties of the silicon-silicon dioxide interface. The following discussions qualitatively investigate these properties and review the mechanisms by which the insulating layer is grown on silicon. Experimental evidence is offered to explain threshold voltage drift in terms of a redistribution of mobile impurity ions within the oxide. The magnitude of such drift is correlated with the intensity of drain current fluctuations and it is shown that transistors which exhibit high noise also tend to show high threshold voltage drift. Measurements of I_{DSS} confirmed that there is no meaningful correlation between leakage at the drain p-n junction and threshold voltage drift.

2.2 Background Information

Growth and oxidation of silicon. Crystal defects may be introduced during the growth of n- or p-doped monocrystaline silicon. Crystal defects may be thermally stress-induced near the liquid-solid interface. During epitaxial growth, vapor-phase reduction of silicon-tetrachloride introduces defects as the temperature of growth is

REDUCED.

THE OVERALL REVERSIBLE CHEMICAL REACTION[1]

$$SiCl_4 + 2H_2 \rightleftharpoons Si_{(SOLID)} + 4HCl \qquad 2\text{-}1$$

SHOWS THAT HYDROCHLORIC ACID CONTAINED IN THE CARRIER GAS ENTERING THE REACTOR MAY RESULT IN REMOVAL RATHER THAN GROWTH OF SILICON.

THE COMPETING REACTION[2]

$$SiCl_4 + Si_{(SOLID)} \rightleftharpoons 2SiCl_2 \qquad 2\text{-}2$$

SUGGESTS THAT "IF THE [SILANE] CONCENTRATION IS TOO HIGH, ETCHING OF THE SILICON WILL TAKE PLACE EVEN IN THE ABSENCE OF A SIGNIFICANT CONCENTRATION OF HCL."[3] SUCH ETCHING DESTROYS MONO-CRYSTALLINE SURFACE PERIODICITY DUE TO LOSS OF SURFACE ATOMS. HIGH TEMPERATURES DURING THE GROWTH PROCESS ENABLES NEIGHBORING ATOMS TO EASILY MIGRATE TO REDUCE THE ENERGY LEVEL AT STRESS POINTS CAUSED BY VACANCIES. THIS INDUCES EVEN MORE LATTICE DEFORMATION WHICH MAY LEAVE THE SUBSTRATE WITH AN EXCESS OF HIGH ENERGY STATES AS A RESULT OF WEAK OR MISSING COORDINATIVE BONDS NEAR THE SEMICONDUCTOR SURFACE. IN CONTRAST WITH RELATIVELY RIGID TETRAHEDRONS OF NEAR PERFECT CRYSTALLINE SILICON, THE HIGH ENERGY STATES MAY FACILITATE HIGHER DIFFUSIVITY OF IMPURITIES INTO THE SUBSTRATE.

THERMAL OXIDATION OF SILICON MAY PROCEED BY EITHER OF TWO REACTIONS DEPENDING ON THE NATURE OF THE OXIDATION PROCESS USED:[4]

DRY $$Si_{(SOLID)} + O_2 \rightleftharpoons SiO_{2(SOLID)} \qquad 2\text{-}3$$

WET $$Si_{(SOLID)} + H_2O \rightleftharpoons SiO_{2(SOLID)} + 2H_2 \qquad 2\text{-}4$$

IT HAS BEEN SHOWN THAT SOME OF THE SURFACE EPITAXIAL SILICON IS CONSUMED DURING OXIDATION:

> "FROM THE DENSITIES AND MOLECULAR WEIGHTS OF SILICON DIOXIDE, A LAYER OF SILICON .45 X_O THICK IS CONSUMED [WHERE X_O IS THE NET OXIDE THICKNESS]. IT HAS BEEN DEMONSTRATED BY THE USE OF RADIOACTIVE TRACERS THAT OXIDATION PROCEEDS BY AN INWARD MOTION OF THE OXIDIZING SPECIES THROUGH THE OXIDE LAYER RATHER THAN BY THE OPPOSITE PROCESS OF THE OUTWARD MOTION OF SILICON TO THE OUTER SURFACE OF THE OXIDE."[5]

ACCORDINGLY, THE OXIDIZING SPECIES MUST UNDERGO THREE CONSECUTIVE STEPS DURING OXIDATION:[6]

1. THEY MUST BE TRANSPORTED FROM THE BULK OF THE GAS TO THE GAS-OXIDE INTERFACE;
2. THEY MUST DIFFUSE ACROSS THE OXIDE LAYER ALREADY PRESENT; AND
3. THEY MUST REACT AT THE SILICON SURFACE.

IT IS NOW CLEAR THAT OXIDE-MASKING STEPS DURING PRODUCTION OF MOS DEVICES INDUCE CRYSTAL STRESS WHEN THE OXIDIZING SPECIES MAKE THEIR WAY THROUGH EXISTING LAYERS OF OXIDE AND THE SEMICONDUCTOR BENEATH THEM. OTHER IONIC

IMPURITIES SUCH AS SODIUM AND HYDROGEN MAY REACT WITH THE SILICON AND SILICON DIOXIDE AT THE $Si-SiO_2$ INTERFACE AND INTRODUCE A LARGE NUMBER OF STATES WITH ENERGY LEVELS WITHIN THE FORBIDDEN GAP. SUCH STATES ARE CALLED <u>SURFACE STATES</u> AND WILL BE SHOWN TO PLAY A VITAL PART IN NOISE PHENOMENA ASSOCIATED WITH MOS TRANSISTORS.

IT IS A WELL KNOWN FACT THAT "IN EQUILIBRIUM, THE CONCENTRATION OF A SPECIES WITHIN A SOLID IS PROPORTIONAL TO THE PARTIAL PRESSURE OF THE SPECIES IN THE SURROUNDING GAS."[7] EXPERIMENTAL DATA UNDER WIDELY RANGING CONDITIONS OF TEMPERATURE, PARTIAL PRESSURE OF OXIDENTS, AND USING EITHER OXYGEN OR WATER VAPOR AS THE OXIDIZING SPECIES CONFIRM THAT FOR LARGE TIMES T, THE THICKNESS OF THE OXIDE FILM MAY BE EXPRESSED AS[8]

$$x_o^2 \simeq \bar{z} \cdot T \qquad 2\text{-}5$$

HERE $\bar{z}$ IS A PARABOLIC RATE CONSTANT FOR THE PROCESS AND IS PROPORTIONAL TO THE PARTIAL PRESSURE OF THE OXIDENT IN THE GAS AND RELATED TO BOTH THE DIFFUSIVITY AND CONCENTRATION OF THE OXIDIZING SPECIES IN THE OXIDE LAYER.

EXPERIMENTAL INVESTIGATIONS HAVE INDICATED THAT "FOR OXIDATION BOTH WITH OXYGEN AND WITH WATER VAPOR, THE OXIDIZING SPECIES MOVING THROUGH THE OXIDE LAYER ARE APPARENTLY <u>MOLECULAR</u>."[9] AT LEAST ONE THEORY OF 1/F NOISE[10] MAKES USE OF A "SLOW RELAXATION" IN THE TRANSISTION FROM MOLECULAR

CHEMISORBED WATER TO LARGER CHEMISORBED COMPLEXES.*

PROPERTIES OF THE $Si-SiO_2$ INTERFACE. THE SILICON-SILICON DIOXIDE INTERFACE IN MOS TRANSISTORS MAY BE CHARACTERIZED BY FIXED SURFACE-STATE CHARGE IN THE OXIDE, SPACE CHARGES WITHIN THE INSULATING LAYER DUE TO MOBILE IMPURITY IONS AND TRAPS IONIZED THERMALLY OR BY RADIATION, AND SURFACE STATES. EACH OF THESE PHENOMENA ARE TREATED INDIVIDUALLY IN THE FOLLOWING DISCUSSIONS.

1. FIXED SURFACE-STATE CHARGE. IT IS THEORIZED THAT THE UNEXPECTED EXISTENCE OF A FIXED SURFACE-STATE CHARGE, Q_{SS}, LOCATED AT OR NEAR THE $Si-SiO_2$ INTERFACE IS ATTRIBUTED TO EXCESS UNREACTED IONIC SILICON PRESENT IN THE OXIDE DURING THE OXIDATION PROCESS. THE CHARACTERISTICS OF THIS CHARGE HAVE BEEN EXTENSIVELY INVESTIGATED BY DEAL ET AL[11] AND HAVE BEEN SUMMARIZED BY GROVE:[12]

> IT IS FIXED AND CAN BE NEITHER CHARGED NOR DISCHARGED OVER A WIDE VARIATION OF BENDING OF THE SILICON ENERGY BANDS.
>
> IT IS NOT AFFECTED UNDER CONDITIONS LEADING TO SODIUM MIGRATION IN THE OXIDE.
>
> IT IS LOCATED WITHIN APPROXIMATELY 200Å OF THE $Si-SiO_2$ INTERFACE.
>
> THE CHARGE DENSITY IS NOT AFFECTED BY EITHER THE OXIDE THICKNESS OR THE TYPE AND CONCENTRATION OF IMPURITY PRESENT.

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*O. JANTSCH[13] AND REVESZ[14] HAVE SHOWN THAT THE "SLOW RELAXATION" RESULTS IN A "MODULATION OF SURFACE RECOMBINATION" WHICH PRODUCES DRAIN CURRENT FLUCTUATIONS IN MOSFETS.

THE CHARGE IS A FUNCTION OF THE OXIDATION AND ANNEALING CONDITIONS AS WELL AS THE ORIENTATION OF THE SILICON CRYSTAL.

THE FIXED SURFACE-STATE CHARGE RESULTS IN A "PARALLEL TRANSLATION OF THE CAPACITANCE-VOLTAGE CHARACTERISTICS ALONG THE VOLTAGE AXIS."[15] IT ALSO INCREASES THE EFFECTIVE GATE VOLTAGE BY[16]

$$V_G' = V_G + Q_{SS}/C_O \qquad 2\text{-}6$$

AND DECREASES THE FLAT-BAND VOLTAGE ACCORDING TO[17]

$$V_{FB} = \Phi_{MS} - Q_{SS}\left(\frac{x_O}{K_O \epsilon_O}\right) \qquad 2\text{-}7$$

WHERE V_{FB} IS DUE TO THE DIFFERENCE IN WORK FUNCTIONS BETWEEN THE METAL AND THE SEMICONDUCTOR MATERIAL AND Φ_{MS} IS THE METAL-SEMICONDUCTOR WORK FUNCTION DIFFERENCE WITHOUT THE INFLUENCE OF Q_{SS}.

2. SPACE CHARGES DUE TO IONIC CONTAMINATION. A MAJOR PROBLEM WITH EARLY MOS DEVICES HAS BEEN TRACED TO SODIUM CONTAMINATION AND IONIC DRIFT UNDER THE INFLUENCE OF AN ELECTRIC FIELD. THIS CAUSES A "REARRANGEMENT OF IONIC SPACE-CHARGE DISTRIBUTION IN THE OXIDE."[18]

FIGURE 2-1 PRESENTS A MODEL OF THE SILICON-SILICON DIOXIDE INTERFACE WITH BIAS APPLIED AT ELEVATED TEMPERATURES. FIGURE 2-1A SHOWS THE APPLICATION OF A $-V_{G\,SUB}$ AND THE INDUCED CHARGES AT THE METAL-GATE AND SUBSTRATE-METAL

INTERFACES. THE DIAGRAM SHOWS POSITIVE SODIUM ATOMS, REPELLED BY THE INDUCED OXIDE CHARGE AND HAVING SUFFICIENT THERMAL ENERGY TO MIGRATE TOWARD THE SUBSTRATE, DRIFTING TOWARD THE $Si-SiO_2$ INTERFACE. THIS CAUSES MOBILE ELECTRONS IN THE N-DOPED SUBSTRATE TO DRIFT TOWARD THE OXIDE AND CHANNEL REGION IN P-CHANNEL ENHANCEMENT MOSFET's.

FIGURE 2-1B ILLUSTRATES THE FOUR RESIDUAL SPACE CHARGES WHICH REMAIN IF THE DRIFT PROCESS IS ALLOWED TO CONTINUE OVER A LONG PERIOD OF TIME. THE RESULT IS THE SAME AS IF A POSITIVE VOLTAGE IS APPLIED TO THE GATE AS WAS SHOWN IN FIGURE 1-2B. THE CHANNEL APPEARS TO BE MORE HEAVILY N-DOPED THAN BEFORE IONIC DRIFT. THE NEGATIVE GATE VOLTAGE REQUIRED FOR SURFACE INVERSION, V_T, MUST NOW BE INCREASED, THEREBY ACCOUNTING FOR APPARENT NEGATIVE THRESHOLD DRIFT.

3. SPACE CHARGES DUE TO IONIZED TRAPS. EXPOSURE OF SILICON DIOXIDE FILMS TO X-RAY, GAMMA RAY, AND LOW-AND HIGH-ENERGY IRRADIATION RESULTS IN THE FORMATION OF ELECTRON-HOLE PAIRS. WHEN IN THE PRESENCE OF AN ELECTRIC FIELD, THE ELECTRONS AND HOLES SEPARATE.[19]

CONSIDER THE MODEL IN FIGURE 2-1 AGAIN. IF A $-V_{GS}$ IS APPLIED AND, INSTEAD OF HEAT THE DEVICE IS BROUGHT INTO CONTACT WITH X-RADIATION, OPTICALLY EXCITED ELECTRONS DRIFT TOWARD THE OXIDE AND HOLES DRIFT TOWARD THE SEMICONDUCTOR. SINCE THE MOBILITY OF ELECTRONS IN SILICON DIOXIDE IS VERY

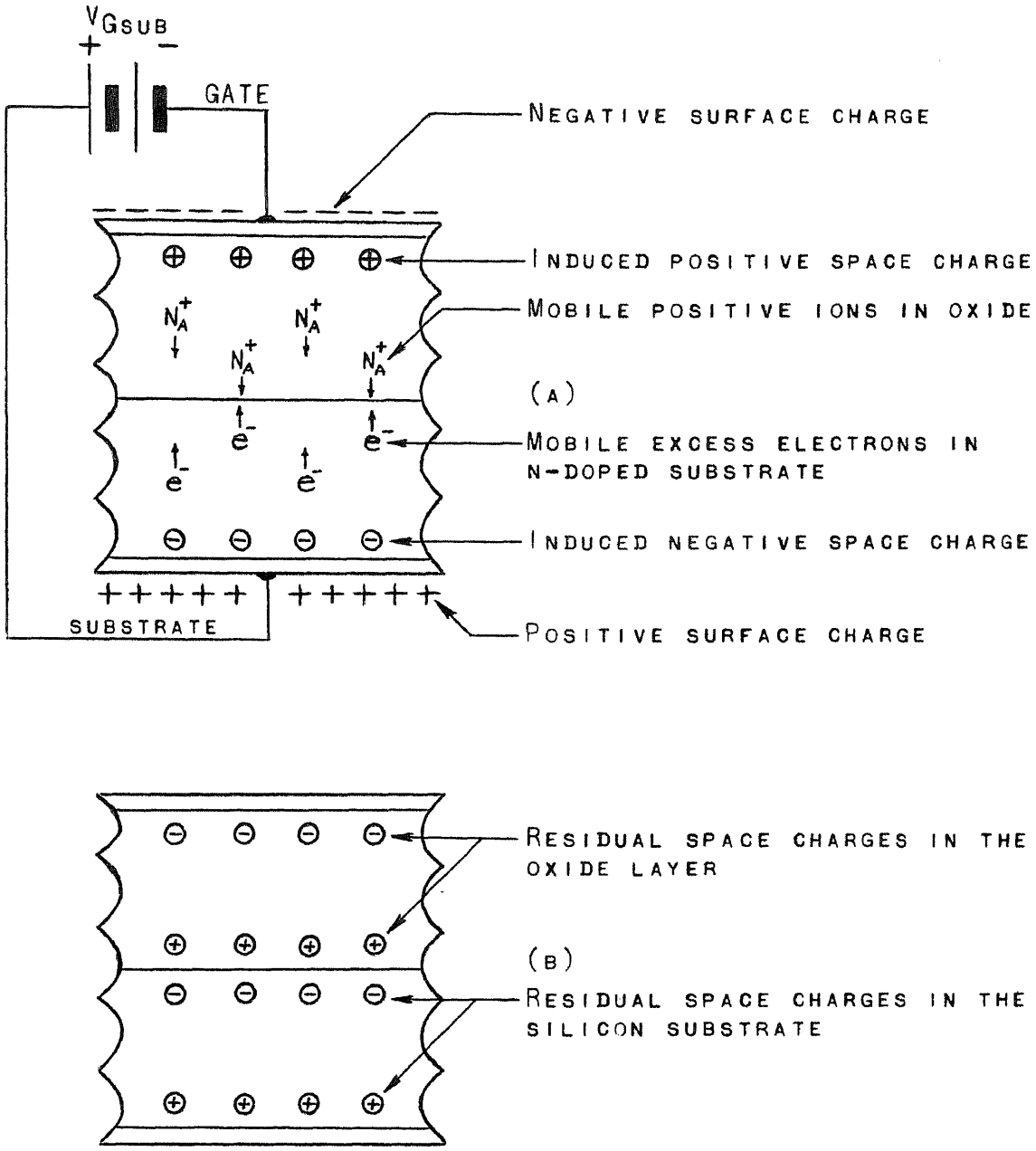

FIGURE 2-1. MODEL OF THE $Si-SiO_2$ INTERFACE IN A P-CHANNEL ENHANCENENT MOSFET SHOWING THE RESULTS OF IONIC DRIFT IN THE OXIDE UNDER THE INFLUENCE OF AN ELECTRIC FIELD. (A) SODIUM IONS ARE ATTRACTED TOWARD THE SEMICONDUCTOR WHILE MOBILE ELECTRONS IN THE N-DOPED SUBSTRATE DRIFT TOWARD THE OXIDE. (B) RESIDUAL SPACE-CHARGES IN THE OXIDE AND IN THE SEMICONDUCTOR MATERIAL. THE APPARANT HIGHER DOPING IN THE CHANNEL REGION CAUSES A NEGATIVE SHIFT IN THE THRESHOLD VOLTAGE, THE GATE VOLTAGE REQUIRED TO INVERT THE SEMICONDUCTOR SURFACE.

LOW, MAJORITY CARRIERS IN THE N-DOPED SUBSTRATE CANNOT RECOMBINE IN THE BULK INSULATOR AT THE $Si-SiO_2$ INTERFACE. THEREFORE, THERE IS A BUILD-UP OF SPACE CHARGE IN THE OXIDE AS HOLES ARE TRAPPED NEXT TO THE SUBSTRATE.

CONTINUED IRRADIATION IN THE PRESENCE OF AN ELECTRIC FIELD CAUSES A LARGER FRACTION OF THE TOTAL APPLIED GATE VOLTAGE TO BE DROPPED ACROSS THE SPACE CHARGE REGION, THEREBY FURTHER INCREASING THE ELECTRIC FIELD ACROSS THE SPACE-CHARGE REGION DUE TO THE ACCUMULATION OF HOLES. IF THE PROCESS IS ALLOWED TO CONTINUE, THE FIELD IN THE REST OF THE OXIDE GRADUALLY APPROACHES ZERO AND A STEADY-STATE HIGHLY LOCALIZED ELECTRIC FIELD CONDITION IS BROUGHT ABOUT IN THE OXIDE AT THE SILICON-SILICON DIOXIDE INTERFACE.[20]

4. FAST SURFACE STATES. FIGURE 1-2 ILLUSTRATED THE ENERGY BAND BENDING WHICH TAKES PLACE IN THE SEMICONDUCTOR NEAR THE $Si-SiO_2$ INTERFACE WHEN THE GATE IS HELD AT SOME POSITIVE OR NEGATIVE POTENTIAL WITH RESPECT TO THE SUBSTRATE. DUE TO A DISRUPTION OF THE PERIODICITY OF THE SEMICONDUCTOR SURFACE DURING OXIDATION, THERE ARE MANY SURFACE ENERGY STATES WITHIN THE FORBIDDEN GAP. CONSEQUENTLY, VARIATIONS IN THE ENERGY BANDS RELATIVE TO THE FERMI LEVEL AFFECT THE "PROBABILITY OF OCCUPATION OF THOSE STATES."[21]

BY DEFINITION, "THOSE STATES WHOSE CHARGE CAN BE READILY EXCHANGED WITH THE SEMICONDUCTOR ARE CALLED SURFACE

STATES."[22] THE PRESENCE OR ABSENCE OF ELECTRONS IN SUCH STATES IS A FUNCTION OF THE SURFACE POTENTIAL WHICH IS ITSELF A FUNCTION OF THE APPLIED GATE VOLTAGE.*

2.3 Previous Experimental Investigations

REVESZ[23] HAS INVESTIGATED THE $Si-SiO_2$ INTERFACE IN ENHANCEMENT MOSFET'S AND HAS SHOWN THAT THE SILICON SURFACE STATE IS A DONOR, THAT IS, POSITIVELY IONIZED SILICON PROVIDES AN EXCESS OF DONOR ELECTRONS. DURING OXIDATION IN OXYGEN AT RELATIVELY HIGH TEMPERATURES IT IS THEORIZED THAT O^- AND O^{--} CONSUME ELECTRONS AS THEY DIFFUSE INTO THE SILICON SUBSTRATE. REVESZ HAS CONCLUDED THAT OXIDATION IN WATER VAPOR INVOLVES SIGNIFICANTLY MORE SURFACE STATES THAN DOES OXIDATION IN OXYGEN ALONE AND THAT THE OXIDATION RATE IS INCREASED WHILE THE DENSITY OF FREE STATES IS REDUCED.[24]

IT IS WELL KNOWN THAT STATES HAVE A MUCH GREATER PROBABILITY OF EXISTING AT DISLOCATIONS AND BOUNDARY IMPERFECTIONS THAN ANYWHERE ELSE AND THAT THEY GIVE RISE TO THE FIXED SURFACE-STATE CHARGE PHENOMENON IN THE OXIDE. IT HAS BEEN THEORIZED THAT DONOR ELECTRONS PRESENT IN THIS MANNER ACT AS RECOMBINATION CENTERS, ENABLE THE DIFFUSION OF SUCH

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*SURFACE-STATE FLUCTUATIONS RESULTING IN VARIATIONS IN SURFACE POTENTIAL MODULATE CHANNEL CONDUCTANCE WHICH IN TURN CAUSES VARIATIONS IN DRAIN CURRENT. THESE DRAIN CURRENT FLUCTUATIONS MAY BE OBSERVED AS NOISE.

IMPURITIES AS HIGHLY MOBILE SODIUM ION, Na^{+}, HYDROGEN ION, H^{+}, AND OTHER ACCEPTORS WHICH MAY BE PRESENT.[25]

WHEN THE SEMICONDUCTOR SURFACE OF A P-CHANNEL ENHANCEMENT MOSFET IS INVERTED, THE FREE HOLE CONCENTRATION IS VERY LARGE WHILE THE FREE ELECTRON DENSITY IS NEGLIGIBLE. SINCE IONIZED SILICON, Si^{+3} AND Si^{+4}, IS ALSO AN ACCEPTOR, IT HAS BEEN THEORIZED THAT THE SURFACE STATES IN P-CHANNEL DEVICES ARE ALMOST EXCLUSIVELY FAST TRAPPING CENTERS IN THE CONDUCTION CHANNEL.*

2.4 Investigation of Threshold Voltage Drift

Experimental method. IN ORDER TO QUANTITATIVELY INVESTIGATE THE MAGNITUDE OF THRESHOLD VOLTAGE DRIFT DUE TO IONIC CONTAMINATION IN THE INSULATING LAYER AND IN ORDER TO CORRELATE SUCH DRIFT WITH EXCESS NOISE AND OTHER SURFACE-RELATED PHENOMENA, LIFE-TESTING OF SEVERAL ENHANCEMENT MOSFET'S WAS UNDERTAKEN.

A LARGE NUMBER OF MEDIUM CONDUCTANCE P-CHANNEL FIELD-EFFECT TRANSISTORS WERE OBTAINED.** THESE DEVICES WERE

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*SUCH OTHER CHEMISORBED SPECIES AS H_2O^{+} MAY ALSO BE CONSIDERED FAST TRAPPING CENTERS. O. JANTSCH CLAIMS THEY FIGURE PROMINENTLY IN THE PRODUCTION OF EXCESS NOISE IN MOS TRANSISTORS. SEE REFERENCE 1967-8 FOR MORE DETAILS.

**THE DEVICES WERE MANUFACTURED BY AMERICAN MICRO-SYSTEMS, INC. OF SANTA CLARA, CALIFORNIA AND WERE PART OF JOINT RELIABILITY STUDIES UNDERTAKEN BY NEWARK COLLEGE OF ENGINEERING AND PICATINNY ARSENAL DURING THE YEARS 1968-72.

PURPORTED TO BE DESIGNED PRIMARILY FOR "LINEAR WIDEBAND AMPLIFIERS AND HIGH SPEED SWITCHING AND COMMUTATING APPLICATIONS." THEY FEATURED A HIGH GAIN-BANDWIDTH PRODUCT, TYPICALLY 195MHz, AND A THRESHOLD VOLTAGE RANGE OF FROM -3.5 TO -5.5V. TWO CONFIGURATIONS AND THREE TYPES WERE AVAILABLE: TYPE DD07P UNITS HAD A BUILT-IN ZENER DIODE VOLTAGE LIMITER BETWEEN THE GATE AND THE SUBSTRATE WHILE TYPES DD08P AND DD08K HAD NO SUCH GATE PROTECTION. ALL WERE FOUR LEAD TRANSISTORS (ONE LEAD FOR THE DRAIN, GATE, SOURCE AND SUBSTRATE BULK) AND HERMETICALLY SEALED IN ORDINARY TO-72 METAL CANS. THERE WERE NO SIGNIFICANT DIFFERENCES IN THE CONSTRUCTION OF THE THREE TYPES OF MOSFET's.

TWENTY DEVICES, TEN EACH OF TYPES DD07P AND DD08K, WERE SELECTED FOR LIFE-TESTING FOR THRESHOLD VOLTAGE DRIFT ON THE BASIS OF THEIR LOW FREQUENCY NOISE INTENSITY.* ACCORDINGLY, FIVE HIGH- AND FIVE LOW-NOISE UNITS WERE SELECTED FROM EACH OF THE TWO TYPES.

TEFLON SOCKETS WERE USED TO CONNECT ALL TRANSISTORS WITH COMMON DRAIN, SOURCE, AND SUBSTRATE. ALL TYPE DD07P DEVICES WERE BIASED WITH $V_{GS} = -25V.$ AND ALL TYPE DD08K UNITS HAD -50V. ON THE GATE. THE COMPLETE ASSEMBLY WAS WIRED INSIDE AN OVEN LATTER MAINTAINED AT 130±5°C FOR 500 HOURS.

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*NOISE MEASUREMENTS WERE MADE AT 10Hz. AND AT 1KHz., BOTH WITH A BANDWIDTH OF 1 CYCLE. THE NOISE MEASUREMENTS ARE DETAILED IN SECTION 3.5.

Experimental results and discussion. Appendix C lists the percentage negative threshold voltage drift, $\%\Delta V_T$, for all twenty units tested. Type DD07P transistors exhibited ranges of drift of from 1.75 to 2.66 percent and from 3.16 to 7.15 percent for low- and high-noise units, respectively. Ranges of 6.88 to 9.11 and 11.5 to 23.6 percent drift were observed for the low- and high- noise type DD08K units.

It is apparant that threshold voltage drift is directly proportional to the electric field across the oxide, as evidenced by the higher percent drift for those units which were biased at the higher gate voltage. Statistical analysis confirmed that the type DD08K units exhibited substantial ΔV_T while drift in the DD07P transistors was very small.*

Of particular importance was the fact that higher threshold voltage drift was observed in the high noise units than in those with low noise intensity. It was therefore concluded that there is a definite correlation between 1/F noise and threshold voltage drift and that, for p-channel enhancement MOSFET's, ionic drift in the oxide definitely affects the semiconductor surface.

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*Previous investigations showed that the type DD08K devices exhibited unusually high ΔV_T. It was therefore of particular importance that such high drift units also be included in this investigation.

**Chapter 3 shows that 1/F noise is a surface-related phenomena and that ionic drift increases the surface-state density.

APPENDIX E DESCRIBES THE PROCEDURES USED TO MEASURE THE SHORT-CIRCUIT DRAIN LEAKAGE CURRENT (WITH ZERO GATE BIAS) AND LISTS THE RESULTS OBTAINED BOTH BEFORE AND AFTER LIFE-TESTING FOR THRESHOLD VOLTAGE DRIFT. IT WAS FOUND THAT THE LEAKAGE CURRENT INCREASED BY A FACTOR OF FROM THREE TO FOUR BUT THAT THIS WAS INSUFFICIENT TO CONCLUDE THAT A SIGNIFICANT AMOUNT OF DRAIN JUNCTION DEGRADATION HAD TAKEN PLACE AFTER 500 HOURS OF BIAS AT 130±5°C.

FURTHERMORE, SINCE THERE WAS NO SIGNIFICANT DIFFERENCE BETWEEN THE AMOUNT BY WHICH I_{DSS} INCREASED FOR UNITS HAVING EITHER RELATIVELY HIGH OR RELATIVELY LOW NOISE, IT WAS CONCLUDED THAT DRAIN LEAKAGE WAS NOT A FACTOR WHICH RESULTS IN THE PRODUCTION OF DRAIN CURRENT FLUCTUATIONS. ALSO, SINCE THE INCREASE IN LEAKAGE FOR TRANSISTORS WHICH SHOWED APPRECIABLE THRESHOLD VOLTAGE DRIFT WAS SIMILAR TO THAT FOR UNITS WHICH EXHIBITED ONLY A SMALL AMOUNT OF DRIFT, IT WAS CONCLUDED THAT THERE IS NO CORRELATION BETWEEN I_{DSS} AND THRESHOLD VOLTAGE DRIFT AND THE MECHANISM OF IONIC DRIFT AT THE $Si-SiO_2$ INTERFACE WHICH PRODUCES THE DRIFT.

REFERENCES

[1]A. S. Grove, Physics and Technology of semiconductor Devices (New York, 1967), p. 8. Ref. 1967-7.

[2]Ibid., p. 9.

[3]Ibid., p. 9.

[4]Ibid., p. 22.

[5]Ibid., p. 23.

[6]Ibid., p. 24.

[7]Ibid., pp. 24-25.

[8]Ibid., p. 27.

[9]Ibid., p. 28.

[10]O. Jantsch, "A Theory of 1/F Noise at Semiconductor Surfaces," Solid-State Electronics(GB) (1968), pp. 267-72. Ref. 1968-8.

[11]B. E. Deal, E.H. Snow, and A.S. Grove, "Properties of the Silicon—Silicon Dioxide System," Semiconductor Products and Solid State Technology (1966), pp. 25-33. Ref. 1966-4.

[12]Op. Cit., Grove, p. 342.

[13]Op. Cit., O. Jantsch, p. 268.

[14]Akos G. Reves7, "The Defect Structure of Grown Silicon Dioxide Films," IEEE Transactions on Electron Devices (1964), pp. 97-101. Ref. 1964-3.

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[16]D. Frohman-Bentchkowsky and A. S. Grove, "Conductance of MOS Transistors in Saturation," IEEE Transactions on Electron Devices (1969), p. 110. Ref. 1969-2.

[17]Op. Cit., Grove, p. 345.

[18]Ibid., p. 338.

[19]Ibid., p. 340.

[20]Ibid., pp. 341-2.

[21] Ibid., p. 282.

[22] Ibid., p. 283.

[23] Op. Cit., Revesz, p. 98.

[24] Ibid., p. 98.

[25] Op. Cit., O. Jantsch, p. 268.

CHAPTER 3

THE SURFACE-STATE RELATED NOISE PHENOMENA IN MOS TRANSISTORS

3.1 Introduction

In the absence of externally applied power, virtually all resistive elements may be thought of as noise generators. However, MOS transistors are unique in that they produce an exceptionally high intensity of excess noise when power is applied. This noise has been shown to be directly proportional to current density and inversely proportional to the frequency at which it is detected.[1] Furthermore, numerous investigations have shown that this "1/F" noise is strongly dependent upon the general surface conditions at the silicon-silicon dioxide interface in MOS transistors and on the surface state density in particular.

The following discussions present a brief background on the major types of electrical noise with particular emphasis on low frequency excess noise intensity and its use in an analysis of component reliability. Experimental results are then presented which qualitatively correlate surface-state related 1/F noise intensity with the surface-state density, semiconductor impurity concentration, and observed differences in saturation drain conductance between high- and low-noise enhancement MOSFET's.

3.2 Basic Noise Theory

Electrical noise may be defined as spurious, unwanted signals which are random in nature and which tend to be aperiodic. Noise may be named for its apparant cause and effect (ie. thermal excitation, random recombination, or random collisions) or by its frequency domain (eg. low-frequency noise). Accordingly, there are three major types of noise commonly found in electrical components, each of which is discussed individually below.

Thermal (Johnson) Noise. The random velocities of carriers between collisions constitutes currents which cause a fluctuating voltage to appear across the terminals of any resistance R. For MOS transistors, the Nyquist relation[2]

$$\overline{v}^2 = 4kTR\Delta f \qquad 3\text{-}1$$

expresses the mean-squared noise voltage in terms of the total drain-to-source resistance, the absolute temperature, and the bandwidth in cycles per second.

The spectral intensity of thermal noise is "white," that is, its magnitude is practically uniform with respect to frequency. Consequently, the larger the included bandwidth, the greater will be the intensity of noise measured. All practical electronic components possess a finite resistance which contributes thermal noise.

Shot Noise. Direct currents in semiconductor materials are by way of a continuous process of dissociation and recombination in a spasmodic "jerky" fashion. This results in instantaneous current fluctuations, the mean-squared value of which is given by[3]

$$\overline{i}^2 = 2qI\Delta f \qquad 3\text{-}2$$

where I is the direct current measured, q is the carrier charge, and Δf is the included bandwidth.

Previous investigations[4,5,6] have shown that shot noise is essentially white for low frequencies. It may be considered independent of frequency over the range of interest for MOSFET operation.

Excess (1/F, Modulation, Flicker) Noise. The origin of excess noise is "thought to lie in semiconductor crystal imperfections and surface effects."[7] By passivating silicon devices with silicon dioxide to reduce the role of surface states, defects are necessarily introduced at the $Si\text{-}SiO_2$ interface. The presence of fast surface states at the semiconductor surface leads to a fluctuation of surface charge in MOS transistors and may produce surface-state related noise which may be observed in either one or both the gate and the drain circuit in MOSFET's. Bell[8] has proposed two mechanisms which result in observed excess noise in MOS devices:

1. Gate noise* due to fluctuations in total surface charge as carriers move to and from the oxide, and

2. Drain current fluctuations** resulting from variations in channel conductance as a result of variations in V_{GS} due to the charge fluctuations which produce gate noise.

Bell offers the following generalized expression for frequency-dependent noise:[9]

$$\frac{V^2 B}{R} = K(J^{\theta} R^{\gamma} v^{\lambda} s/f^{\eta})B \qquad 3\text{-}3$$

where B = Bandwidth in cycles per second

J = Current density

K = Material constant

R = Resistance in ohms

s = Shape factor

v = Volume

$\eta + \gamma = 2$ to balance the equation in time

$\theta = 2$ to balance the equation in charge

---

*For any ΔQ into the oxide from the semiconductor, there must be a ΔQ of opposite polarity onto the gate and vice versa. This leads to gate charge fluctuation which is observed as a noise voltage in the gate circuit.

**Variations of charge between the depletion region, the inversion region, and the surface states alters the instantaneous value of V_{GS}. Recall from section 1.2 that the channel conductance, and therefore the drain current, is easily modulated by variations in gate voltage. Hence the observed drain current fluctuations in MOS transistors.

THE GENERAL EXPRESSION MAY BE SIMPLIFIED TO[10]

$$\frac{V^2 B}{R} = K(J^2 R^{2-\eta} v^{1-\varkappa} s/f)B \qquad 3\text{-}4$$

WHERE $\varkappa = (\eta - 1)/3$. FOR AN EXACT 1/F SPECTRUM, LET $\eta = 1$, $1-\varkappa = 1$, $2-\eta = 1$, AND LET S BE AN AREA/UNIT LENGTH. THEN THE PRODUCT R·S IS IN UNITS OF RESISTIVITY, ρ.

THE NOISE POWER DENSITY FOR A 1/F SPECTRAL INTENSITY (IN WHICH B IS ONE CYCLE AT AN ANGULAR FREQUENCY OF ω) MAY BE STATED AS[11]

$$P_{N(\omega)} = K(J^2 \rho v/f)d\omega \qquad 3\text{-}5$$

WHICH IS DIRECTLY PROPORTIONAL TO THE DC POWER APPLIED (AND THE CURRENT DENSITY SQUARED) AND INVERSELY PROPORTIONAL TO FREQUENCY.*

3.3 Previous Studies of the Excess Noise Spectral Intensity

SURFACE-STATE RELATED 1/F NOISE HAS BEEN ATTRIBUTED TO A MODULATION OF SURFACE RECOMBINATION. THIS REASONING IS BASED ON McWHORTER'S[12] THEORY OF TRAPPING CENTERS AT THE SILICON-SILICON DIOXIDE INTERFACE:

> 1. THE INTRODUCTION OF TRAPPING CENTERS INTO THE SEMICONDUCTOR MATERIAL RESULTS IN A "DIRECT CHANGE IN CURRENT DUE TO A CHANGE IN THE NUMBER OF FREE CARRIERS AND AN INDIRECT CHANGE IN CURRENT DUE TO A CHANGE IN THE NUMBER OF TRAPPED CARRIERS."[13]

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*1/F NOISE IS USUALLY MASKED BY THERMAL NOISE AT ALL FREQUENCIES ABOVE 20KHz AND THEREFORE MUST BE OBSERVED AT RELATIVELY LOW FREQUENCIES FOR TRUE 1/F DEPENDENCE.

2. The random occupancy of surface states by Brownian motion "modulates the surface potential, which causes a fluctuation in surface recombination velocity and a modulation of the free carrier density in the space-charge region near the silicon surface."[14]

3. Since the drift of charged carriers constitutes a diffusion current, any fluctuation in the free carrier density necessarily indicates a "fluctuation in diffusion current."[15]

The 1/F noise can then be explained by "conduction channel charge density fluctuation caused by the modulation of surface potential due to the random occupancy of surface states"[16] which supports the theory of drain current fluctuations put forth by Bell.

Since the life-time of the fast surface states is typically about 10^{-9} second, the recombination noise produced is of very high frequency. The observed low-frequency noise must therefore be a modulation of surface recombination.[17]

Heiman and Warfield[18] have estimated that surface states are located within about 20Å from the the $Si-SiO_2$ interface. Since the oxide thickness in MOS transistors is typically 600-2000Å (and since the oxide thickness must be orders of magnitude greater than the inversion layer), the resident distance of surface states is negligibly small and the 1/F noise may be considered a surface phenomenon.

HSU[19] HAS ANALYTICALLY PREDICTED THE NOISE SPECTRAL INTENSITY OF LOW-FREQUENCY EXCESS NOISE IN P-CHANNEL ENHANCEMENT MOSFET'S AND A REVIEW OF HIS DERIVATION IS INCLUDED IN APPENDIX B. THE SPECTRAL INTENSITY OF THE SHORT-CIRCUIT DRAIN CURRENT FLUCTUATIONS IS GIVEN BY[20]

$$S_{i(\omega)} = \left[\frac{g_{GM}}{AC_O}\right]^2 \frac{4kTAN_T(E)\tau_s}{\alpha}(e^{\alpha\ell}-1) \qquad 3\text{-}6A$$

FOR $\omega\tau_s e^{\alpha\ell} \ll 1$

$$S_{i(\omega)} = \left[\frac{g_{GM}}{AC_O}\right]^2 \frac{kTAN_T(E)}{\alpha f} \qquad 3\text{-}6B$$

FOR $\omega\tau_s \ll 1 \ll \omega\tau_s e^{\alpha\ell}$

$$S_{i(\omega)} = \left[\frac{g_{GM}}{AC_O}\right]^2 \frac{4kTAN_T(E)}{\alpha\omega^2\tau_s}(1-e^{-\alpha\ell}) \qquad 3\text{-}6C$$

FOR $1 \ll \omega\tau_s$

WHERE A = EFFECTIVE AREA OF THE GATE IN CM^2

$C_O = \frac{K_O\epsilon_O}{x_O}$ IS THE OXIDE CAPACITANCE

$G_M = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D = \text{CONSTANT}}$ IS THE MOST TRANSCONDUCTANCE

k = BOLTZMANN'S CONSTANT

ℓ = ASSUMED TO BE 20Å

$N_T(E)$ = DENSITY OF TRAPPED SURFACE STATES PER UNIT VOLUME PER UNIT ENERGY (CM^{-3}/EV)

T = ABSOLUTE TEMPERATURE IN °K

τ_s = TIME CONSTANT OF SURFACE STATES LOCATED AT THE $SI\text{-}SiO_2$ INTERFACE.

ω = ANGULAR FREQUENCY IN RAD/SEC.

AND WHERE α IS EXPERIMENTALLY DETERMINED TO BE 2×10^8 CM^{-1} AND $\exp(\alpha \ell) = 10^{17.21}$

FROM THE ABOVE EXPRESSIONS IT IS APPARANT THAT VERY LOW FREQUENCY NOISE IS INDEPENDENT OF FREQUENCY, A TRUE 1/F SPECTRAL INTENSITY IS FOUND ONLY WITHIN THE RANGE OF $(2\pi\gamma_s e^{\alpha\ell})^{-1}$ TO $(2\pi\gamma_s)^{-1}$ (A RANGE THEORETICALLY PREDICTED TO BE ABOUT 17 ORDERS OF MAGNITUDE), AND THAT NOISE AT HIGHER FREQUENCIES HAS A $1/F^2$ DEPENDENCE.

OF PARTICULAR INTEREST IS THE DEPENDENCE OF NOISE INTENSITY ON THE SURFACE-STATE DENSITY. SINCE ONLY THOSE STATES "WITHIN $\pm 2kT$ FROM THE SURFACE-STATE FERMI LEVEL CONTRIBUTE NOISE TO THE DEVICE, IF THE SURFACE STATES ARE ARBITRARILY DISTRIBUTED IN ENERGY, THE VALUE $N_T(E)$ REPRESENTS THE SURFACE-STATE DENSITY WITHIN $\pm 2kT$ OF THE FERMI LEVEL."[22] PROCESSES WHICH INTRODUCE STATES INTO THIS RANGE OF ENERGY THEREFORE RESULT IN AN INCREASE IN THE NUMBER OF SURFACE STATES AND MAY BE OBSERVED BY AN INCREASE IN NOISE INTENSITY.

3.4 Electrical Noise and Component Reliability

AN EXCEPTIONALLY HIGH NOISE INTENSITY MAY BE REGARDED AS AN INDICATION OF SOME ABNORMALITY IN AN ELECTRICAL DEVICE. THOSE DEVICES EXHIBITING HIGH NOISE CHARACTERISTICS MAY THEREFORE BE CLASSIFIED AS POTENTIAL RELIABILITY RISKS. NOISE MEASUREMENTS ARE THEREFORE A RELIABILITY TOOL USED TO COMPARE DEVICES WITH AN ACCEPTED STANDARD.

Any mechanism which "focuses" or "funnels" a significant amount of current through a small cross-section results in a high localized current density and accompanying localized heating in a device. Defects in the crystal structure at P-N junctions, cracks, flaws, or inclusions in the semiconductor material may lead to "current funneling" and high 1/F noise intensity.[23]

Since enhancement MOSFET's conduct through a relatively narrow inversion region at the semiconductor surface, all drain current is concentrated within an extremely limited portion of the channel. At even moderate current levels, such devices possess an inherently high current density near the $Si-SiO_2$ interface (where inclusions such as SiO_2 molecules are present) and consequently exhibit much higher 1/F noise intensity than bipolar transistors.

Therefore, unusually high noise units may be eliminated from production batches in anticipation of a correspondingly high failure rate probability due to high current density. Furthermore, the relative 1/F noise intensity should be an excellent indicator of surface conditions present in each device and the surface-state density in particular. This reasoning was applied to all analyises of noise phenemena encountered in this research and was one of the reasons it was thought that noise measurements would be beneficial in a study of breakdown in enhancemnent MOSFET's.

3.5 Noise Measurements Undertaken

Description of Equipment. Noise measurements were performed using the Quan-Tech Model 327 Diode Noise Analyzer. Figure 3-1 shows the internal connection block diagram and external gate supply of such an instrument modified for use with p-channel enhancement MOSFET's.

The device consisted of a built-in variable DC supply, a shielded test jig and socket, current-limiting resistors, a broadband amplifier for amplifying the noise voltage across a single, selected, fixed resistor, two active filters resonant at ten hertz and one kilohertz with a bandwidth of one cycle each, and analog outputs which read at the appropriate frequency in rms volts.

Nickel-cadmium batteries were used to bias the gate of each MOSFET under test in order to minimize noise introduced into the gate circuit which might in turn cause undesireable drain current fluctuations.

All noise measurements were conducted within a shielded room at a temperature of about 25°C and not more than 30% humidity.

Experimental Method. The p-channel MOSFET's under test were individually connected with source and substrate to the main power supply positive terminal, drain to the negative terminal, and gate to the external variable supply.

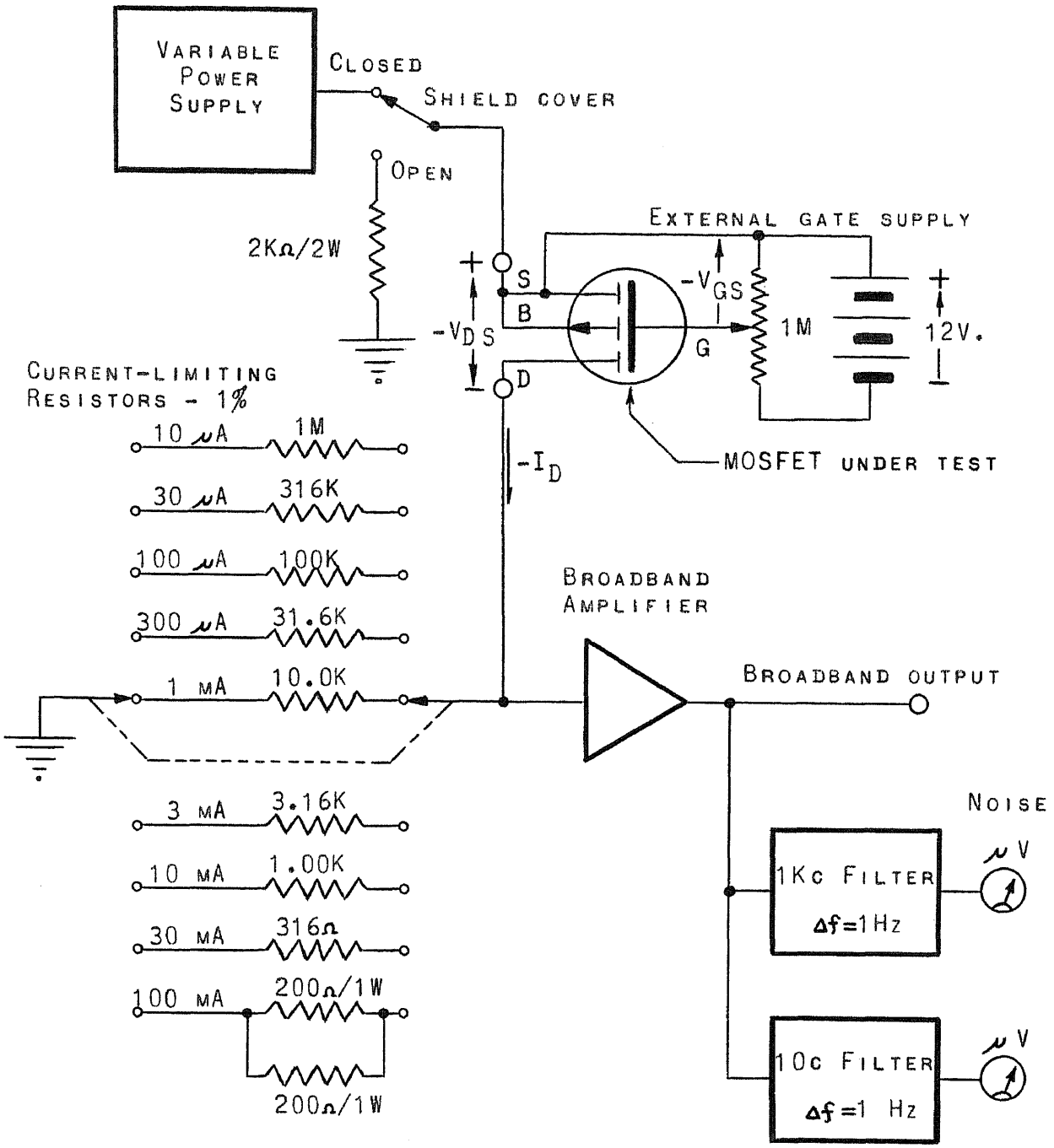

FIGURE 3-1. CONNECTION BLOCK DIAGRAM OF THE QUAN-TECH MODEL 327 DIODE NOISE ANALYZER MODIFIED FOR MEASURING NOISE VOLTAGES OF P-CHANNEL ENHANCEMENT MOS TRANSISTORS.[24]

THE MAIN DC SUPPLY AND THE CURRENT-LIMITING RESISTORS PROVIDED CONTINUOUS VARIATION OF EITHER $-V_{DS}$ OR $-I_D$. WITH USE OF THE EXTERNAL GATE SUPPLY, NOISE VOLTAGES* COULD BE OBTAINED ANYWHERE ON THE MOSFET I-V CHARACTERISTICS.

APPROXIMATELY 80 TRANSISTORS WERE SELECTED FROM A LARGE BATCH OF P-CHANNEL MOSFET'S.** ALL DEVICES WERE FIRST SCREENED FOR PROPER OPERATION UP TO AND SLIGHTLY BEYOND THE THRESHOLD OF DRAIN BREAKDOWN. THEN, 25 TRANSISTORS OF EACH TYPE WERE SELECTED FOR ACTUAL NOISE MEASUREMENTS.

NOISE VOLTAGES WERE OBTAINED AT 10Hz AND AT 1KHz WITH ALL UNITS BIASED AT A CONSTANT V_{GS} OF -5.5 VOLTS AND FOUR DIFFERENT VALUES OF DRAIN VOLTAGE: -3V., -10V.. -20V., AND AT -25V. THIS PERMITTED NOISE VOLTAGES TO BE MADE IN BOTH THE LINEAR AND SATURATION REGIONS OF OPERATION FOR EACH UNIT. THE DATA PROVIDED A PROFILE OF THE MEAN NOISE VOLTAGE AND STANDARD DEVIATION AS A FUNCTION OF DRAIN VOLTAGE FOR EACH TYPE OF TRANSISTOR.

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*ACTUAL DRAIN CURRENT FLUCTUATIONS WERE COMPUTED FROM THE MEASURED NOISE VOLTAGES BY DIVIDING THE OBSERVED QUANTITY BY THE KNOWN, FIXED RESISTANCE ACROSS WHICH IT APPEARED. THE NOISE INTENSITY (OF DRAIN CURRENT FLUCTUATIONS) WAS THEN THE SQUARE OF THE CALCULATED NOISE CURRENT AT A SPECIFIED OPERATING POINT.

**SECTION 2.4 DESCRIBED THE TYPES DD07P, DD08P, AND DD08K P-CHANNEL ENHANCEMENT MOSFET'S USED IN THIS RESEARCH. THOSE DEVICES ON WHICH NOISE MEASUREMENTS WERE MADE WERE SELECTED AT RANDOM FROM A BATCH ESTIMATED TO BE OVER 300 UNITS.

Using the built-in voltmeter and ammeter on the Quan-Tech noise measuring instrument, saturation drain conductance measurements were made at an operating point of -5.5V. on the gate and V_{DS} = -20V. The relative noise voltage at 10Hz was correlated with the drain conductance for each individual transistor.

On the basis of the relative noise intensity at ten cycles, the five highest and five lowest noise transistors of types DD07P and DD08K were selected for life-testing for threshold voltage drift. Noise voltage versus drain current measurements at constant gate voltage were made before and after 500 hours of bias* at 130 ± 5°C.

Noise voltage versus drain current characteristics at several gate voltages were plotted for three high- and three low-noise transistors of type DD07P. A curve tracer was used to visually verify the plotted I-V characteristics.

All noise, current, and voltage measurements were checked and rechecked to ensure accurate readings. A Fluke Model 8000A Digital Voltmeter was used to determine the precise threshold voltage for each transistor as well as for purposes of double checking the voltage readings on the Quan-Tech instrument.

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*Type DD07P units were biased at V_{GS} = -25V. while type DD08K units were biased at V_{GS} = -50V. The drain, source, and substrate bulk were common for both types of devices.

3.6 Experimental Results and Discussion

Comparison of noise intensities. Figure 3-2 represents the noise voltage profile of three sets of devices as a function of drain voltage before life-testing for threshold voltage drift. Figure 3-2a shows the mean and standard deviation of noise voltages at ten cycles while figure 3-2b gives the corresponding information at one-thousand cycles.*

It was not the intention of this research to establish the exact frequency dependence of excess noise in MOS transistors. This has been done before and is readily available in the literature.[25,26,27] Rather, it may be concluded that the low frequency excess noise intensity was found to be approximately inversely proportional to the frequency at which it was measured BEFORE threshold voltage drift. The 1/F noise theory developed earlier therefore applies to all subsequent discussions regarding the noise intensity of the devices tested.

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*The figures represent rms noise voltage in microvolts at two frequencies. Comparisons of mean noise intensities between any two types of devices or between two frequencies for the same device must reflect the ratio of the squares of the noise voltage readings used. Example: Compare the mean noise intensity of type DD08P at 10Hz and $V_{DS}=-3V$. and at the same drain voltage and 1KHz. In the first case the mean noise voltage was $10\times10^{-6}V$. and in the second it was approximately $0.82\times10^{-6}V$. The ratio of the square of the first reading to that of the second shows that the noise intensity at ten cycles was in fact more that 100 times that at one kilohertz.

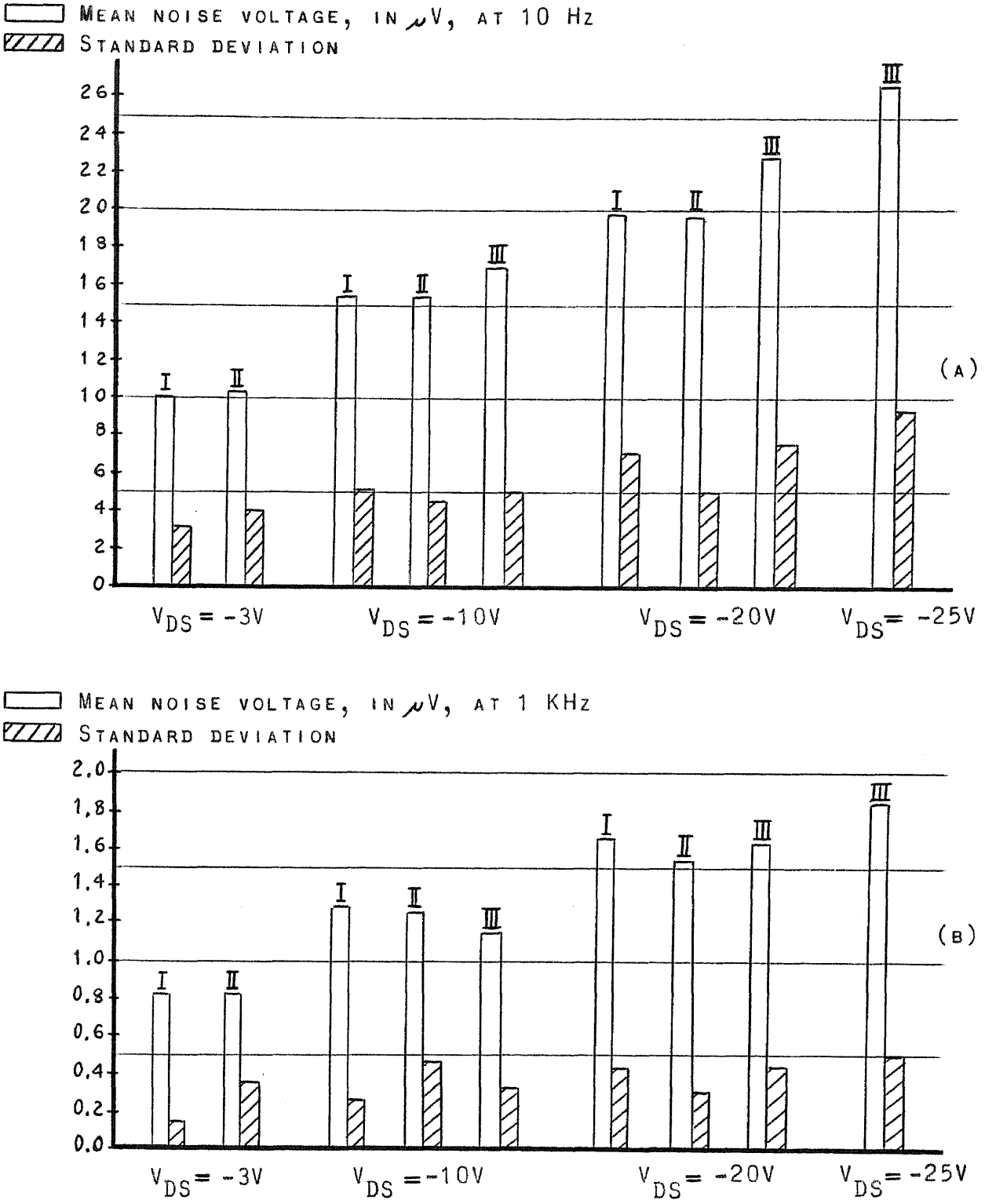

FIGURE 3-2. COMPARISON OF MEAN EXCESS NOISE VOLTAGE FOR THREE TYPES OF P-CHANNEL ENHANCEMENT MOSFET'S. MEASUREMENTS WERE MADE AT FOUR DRAIN VOLTAGES WITH CONSTANT V_{GS} OF -5.5V. TYPE I: DD08P TYPE II: DD08K TYPE III: DD07P

As expected, the noise voltage was found to increase with increasing drain voltage when the gate was held at a constant potential. Increasing V_{DS} in this manner also increases the drain current which flows in a channel of fairly constant dimensions. The approximate 1/F frequency dependence was found to hold for both the linear and saturation regions of operation.

Figures 3-3 through 3-5 compare mean noise voltage at 10Hz with saturation drain conductance at $V_{DS}=-10V.$ and $V_{GS}=-5.5V.$ for the three types of units tested. Two observations are immediately apparant:

1. There was a wide range of relative noise intensity within each group of MOSFET's, and

2. In every case, those units having a high noise intensity showed a correspondingly higher saturation drain conductance than did the low-noise units.

Two theories are offered to explain the correlation between 1/F noise intensity and saturation drain conductance.

1. Variations of semiconductor impurity concentration.

Recall from section 1.2 that high saturation drain conductance is synonymous with relatively thick oxide layers and/or low substrate impurity concentrations. Under the condition of uniform oxidation with low surface-state den-

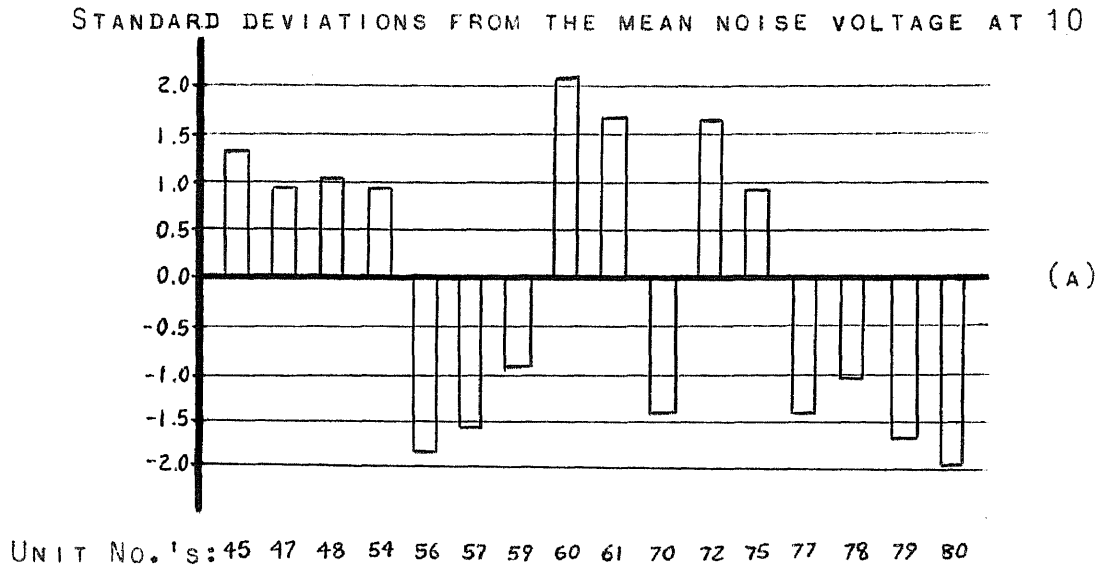

FIGURE 3-3. COMPARISON OF NOISE VOLTAGE AT 10Hz WITH SATURATION DRAIN CONDUCTANCE FOR SELECTED UNITS OF TYPE DD07P MOSFET's. $V_{DS} = -20$ VOLTS AND $V_{GS} = -5.5$ VOLTS.

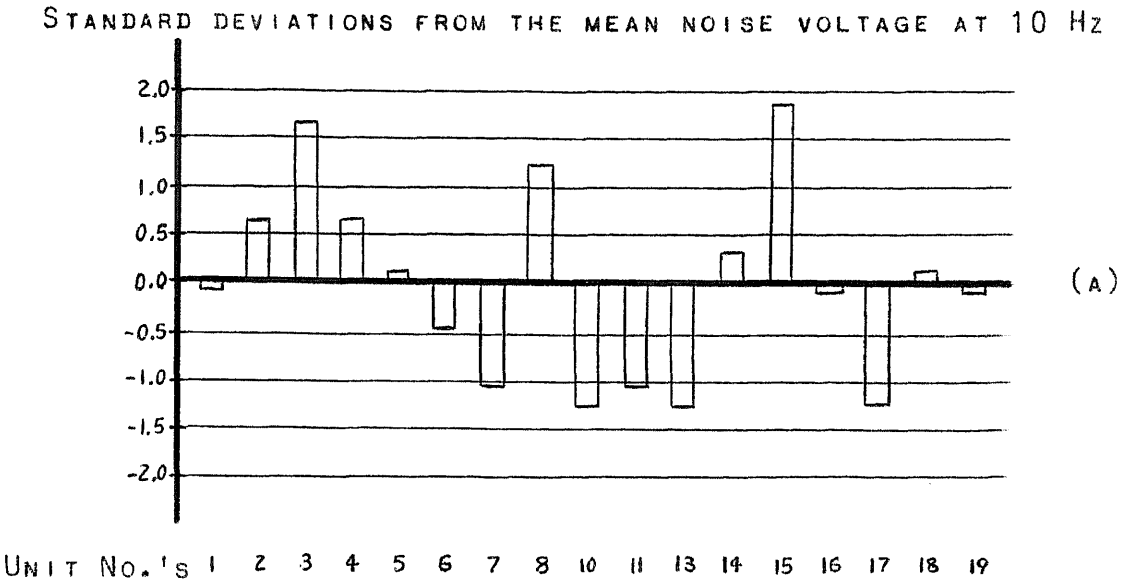

FIGURE 3-4. COMPARISON OF NOISE VOLTAGE AT 10Hz WITH SATURATION DRAIN CONDUCTANCE FOR SELECTED UNITS OF TYPE DD08P MOSFET's. $V_{DS} = -20$ VOLTS AND $V_{GS} = -5.5$ VOLTS.

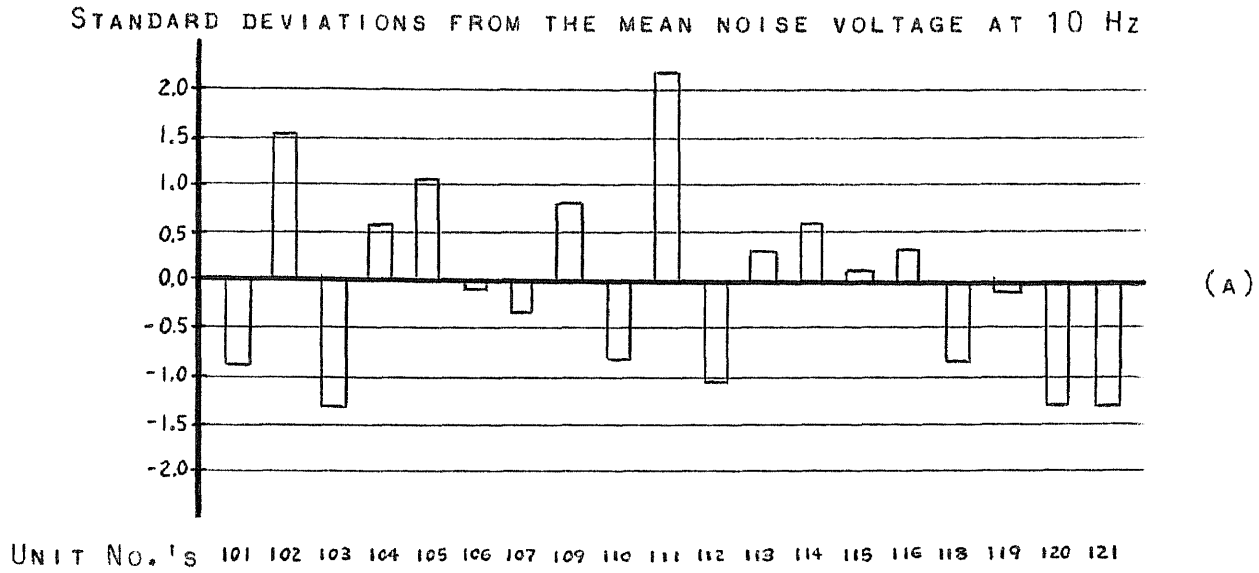

FIGURE 3-5. COMPARISON OF NOISE VOLTAGE AT 10Hz WITH SATURATION DRAIN CONDUCTANCE FOR SELECTED UNITS OF TYPE DD08K MOSFET's. V_{DS} = -20VOLTS AND V_{GS} = -5.5VOLTS.

SITY, THE DRAIN CONDUCTANCE IS SIMPLY A FUNCTION OF THE RELATIVE BULK DOPING CONCENTRATION. IT THEREFORE FOLLOWS THAT, WITH CONSTANT GATE VOLTAGE AND OPERATION IN THE SATURATION REGION AT CONSTANT DRAIN VOLTAGE, A RELATIVELY HIGH DRAIN CONDUCTANCE IS INDICATIVE OF A LOW SEMICONDUCTOR IMPURITY CONCENTRATION.

SINCE THE DRAIN CURRENT IN THE SATURATION REGION IS DEPENDENT UPON THE AMOUNT BY WHICH THE EXPOP RECEDES TOWARD THE SOURCE (WHICH IS ITSELF A FUNCTION OF TH BULK DOPING CONCENTRATION), THE RELATIVE CURRENT DENSITY IN THE TRANSISTOR IS DIRECTLY RELATED TO BOTH THE SEMICONDUCTOR IMPURITY CONCENTRATION AND THE SATURATION DRAIN CONDUCTANCE.

THEREFORE, A HIGH CURRENT DENSITY, GIVING A HIGH 1/F NOISE INTENSITY, IS A DIRECT CONSEQUENCE OF RELATIVELY LOW BULK DOPING IN THE SUBSTRATE. NOISE MEASUREMENTS ARE THEREFORE USEFUL IN AN ANALYSIS OF DOPING PROFILES FOR MOS TRANSISTORS. HOWEVER, THE VARIATION IN NOISE INTENSITY MAY BE EXPECTED TO BE RELATIVELY SMALL DUE TO THE SMALL VARIATION SEMICONDUCTOR DOPING LEVELS BETWEEN UNITS OF THE SAME BATCH.

2. HIGH SURFACE-STATE DENSITY. RECALL FROM SECTION 3.3 THAT 1/F NOISE INTENSITY IS DIRECTLY PROPORTIONAL TO THE SURFACE-STATE DENSITY WITHIN AN MOS DEVICE. IT THEREFORE FOLLOWS THAT, WITH CONSTANT SEMICONDUCTOR IMPURITY

CONCENTRATION AND OPERATING POINT, THOSE UNITS HAVING A RELATIVELY HIGH 1/F NOISE INTENSITY MAY ALSO BE EXPECTED TO POSSESS A HIGH DENSITY OF SURFACE STATES.

MEASUREMENTS OF I_{DSS} CONFIRMED THAT HIGH DRAIN-DIODE LEAKAGE WAS NOT A FACTOR IN THOSE UNITS HAVING AN ABNORMALLY HIGH DRAIN CONDUCTANCE AND THEREFORE SUCH CONDUCTANCE MUST NECESSARILY BE A SEMICONDUCTOR SURFACE EFFECT. IT IS THEN REASONABLE TO SUSPECT THAT SURFACE STATES CONTRIBUTE TO SURFACE CONDUCTION AND THAT SURFACE-STATE RELATED 1/F NOISE INTENSITY IS THEREFORE HIGHER IN THOSE TRANSISTORS HAVING HIGH SATURATION DRAIN CONDUCTANCE.

SECTION 2.4 PROPOSED THAT THE MAJORITY OF FAST SURFACE STATES IN P-CHANNEL ENHANCEMENT MOSFET'S ARE TRAPPING CENTERS, THAT IS HOLES NEAR THE $Si-SiO_2$ INTERFACE. SINCE THE OXIDIZING SPECIES CONSUME ELECTRONS DURING DIFFUSION INTO THE SILICON, IT IS PLAUSIBLE TO EXPECT THAT A LOW SEMICONDUCTOR IMPURITY CONCENTRATION RESULTS IN A GREAT MANY MORE TRAPPING CENTERS THAN WOULD BE THE CASE WITH HIGH BULK DOPING. THE DENSITY OF FAST TRAPPING CENTERS IN P-CHANNEL DEVICES WOULD THEN BE AN INVERSE FUNCTION OF THE IMPURITY CONCENTRATION IN THE SUBSTRATE. THEREFORE, BOTH THEORIES 1 AND 2 ARE RELATED AND THE RELATIVE 1/F NOISE INTENSITY MAY BE AN INDICATION OF BOTH THE DOPING LEVEL AND THE SURFACE-STATE DENSITY. FURTHERMORE, THE SATURATION DRAIN CONDUCTANCE MIGHT BE PROPORTIONAL TO

THE SURFACE-STATE DENSITY AS WELL.

Noise voltage and threshold voltage drift. The noise voltages versus drain current at constant gate voltage for the twenty units life-tested for threshold voltage drift are listed in Appendix D. All units increased in noise intensity following 500 hours of bias at an elevated temperature. Of particular importance is the apparant loss of 1/F frequency dependence due to unusually high increases in noise voltages at 1KHz. It was concluded that ionic drift at the silicon-silicon dioxide interface probably resulted in a high density of shallow traps at the semiconductor surface. It is believed that such traps have time constants which are much shorter than the time constants of other trapping centers and that modulation of surface recombination utilizing shallow traps accounts for the greatly increased noise intensity at the higher frequency.

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CHAPTER 4

CORRELATION OF 1/F NOISE WITH DRAIN BREAKDOWN

4.1 Introduction

Drain breakdown in MOS transistors is shown to be a composite of impact ionization in the channel and gate-controlled drain-diode breakdown at the drain-to-substrate p-n junction. The semiconductor impurity concentration, the surface-state density, the saturation drain conductance, and the applied gate voltage are critical factors influencing when and to what extent drain breakdown occurs at high drain voltages. Low frequency excess noise measurements were conducted on several high- and low-noise transistors at various stages of breakdown and the experimental results were correlated with semiconductor surface effects.

4.2 Theory of Electrical Breakdown at P-N Junctions

The cumulative drain breakdown phenomena in enhancement MOSFET's is essentially an extension of breakdown theory at any reverse-biased p-n junction. Two types of breakdown in semiconductor devices are discussed below.

Avalanche breakdown. Under the influence of a high electric field, ionization of semiconductor materials results in the creation of electron-hole pairs. When the electrons gain sufficient kinetic energy while being accelerated in the electric field, their collisions with the

CRYSTAL LATTICE FRACTURE Si-Si BONDS. EACH SUCH COLLISION PRODUCES SEVERAL ADDITIONAL ELECTRON-HOLE PAIRS WHICH IN TURN MAY RESULT IN MORE COLLISIONS AND EVEN FURTHER IONIZATION. SUCH IMPACT IONIZATION RESULTING IN RAPID MULTIPLICATION OF AVAILABLE CARRIERS HAS BEEN TERMED AVALANCHE BREAKDOWN.[1]

ZENER BREAKDOWN. A VERY HIGH ELECTRIC FIELD ACROSS THE SPACE-CHARGE REGION OF A REVERSE-BIASED P-N JUNCTION DISTORTS AND "TEARS APART" COVALENT Si-Si BONDS. ELECTRON-HOLE PAIRS ARE THEN IMMEDIATELY ELEVATED TO THE CONDUCTION BAND. SUCH PENETRATION OF THE FORBIDDEN GAP IS REFERRED TO AS TUNNELING AND LEADS TO THE SO-CALLED ZENER BREAKDOWN EFFECT.[2]

THE ELECTRIC FIELD REQUIRED FOR TUNNELING IN SILICON IS ON THE ORDER OF 10^6 VOLTS/CM. ZENER BREAKDOWN IS THEREFORE USUALLY PRECEEDED BY AVALANCHE BREAKDOWN WHICH OCCURS AT A LOWER ELECTRIC FIELD POTENTIAL. THE TWO TYPES OF BREAKDOWN ARE NOT TOTALLY INDEPENDENT AND ONE MAY BE RESPONSIBLE FOR THE ONSET OF THE OTHER.[3]

4.3 Previous Investigation of Drain Breakdown

CHANNEL IMPACT IONIZATION. COBBOLD[4] HAS SHOWN THAT CHANNEL BREAKDOWN IN MOS TRANSISTORS IS CHARACTERIZED BY HIGH SATURATION DRAIN CONDUCTANCE AND A GRADUAL INCREASE IN DRAIN CURRENT AT HIGH DRAIN VOLTAGES WHEN THE CHANNEL IS STRONGLY INVERTED.

RECALL THAT AS THE EXPOP RECEDES TOWARD THE SOURCE WHEN THE DRAIN VOLTAGE IS INCREASED FOLLOWING THE ONSET OF CHANNEL PINCH-OFF, THAT PROTION OF THE CHANNEL BETWEEN THE EXPOP AND THE DRAIN JUNCTION BECOMES A SPACE-CHARGE DEPLETION REGION. IMPACT IONIZATION OCCURS WITHIN THIS DEPLETION REGION WHEN THE TRANSVERSE ELECTRIC FIELD* REACHES A CRITICAL VALUE. COBBOLD HAS FOUND THAT SOFT DRAIN BREAKDOWN IN MOS TRANSISTORS IS ACCOMPANYIED BY AVALANCHE MULTIPLICATION AT THE DRAIN-END OF THE CHANNEL WHERE THE ELECTRIC FIELD IS THE STRONGEST.[5]

KRESSEL[6] HAS INVESTIGATED THE EFFECT OF INCLUSIONS IN SEMICONDUCTORS HAVING DIELECTRIC CONSTANTS DIFFERENT FROM THE MEDIUM IN WHICH THEY ARE IMMERSED. IN PARTICULAR, HE HAS FOUND THAT

> "IN THE CASE OF A SPHERICAL PRECIPITATE SUCH AS SiO_2 IN Si, IT MAY READILY BE SHOWN THAT THE MAXIMUM ELECTRIC FIELD AT THE SURFACE OF THE SPHERE IS APPROXIMATELY 1.5 TIMES LARGER THAN THE AVERAGE FIELD IN THE SURROUNDING MEDIUM."[7]

IT HAS LONG BEEN RECOGNIZED THAT INCLUSIONS IN SEMICONDUCTOR MATERIALS CONTRIBUTES TO ELECTRICAL BREAKDOWN AT P-N JUNCTIONS BY IMPOSING UNUSUALLY HIGH LOCALIZED ELECTRIC FIELDS WHICH ARE ALSO REGIONS OF HIGH CURRENT DENSITY.

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*A COMPLETE EXPRESSION FOR THE TRANSVERSE ELECTRIC FIELD MAY BE FOUND IN APPENDIX A, EQUATION A-5. FURTHER INFORMATION AND A DERIVATION OF THIS EXPRESSION MAY BE FOUND IN REFERENCE 1969-2.

DRAIN-DIODE BREAKDOWN. COBBOLD[8] HAS SHOWN THAT DRAIN-DIODE BREAKDOWN IN MOS TRANSISTORS IS CHARACTERIZED BY RELATIVELY SHARP INCREASES IN DRAIN CURRENT WITH INCREASING V_{DS}. THIS HARD DRAIN BREAKDOWN PHENOMENON HAS BEEN FOUND TO BE A FUNCTION OF THE POTENTIAL DIFFERENCE BETWEEN THE DRAIN AND GATE TERMINALS AND IS THEREFORE GATE-CONTROLLED. THIS FORM OF DRAIN BREAKDOWN HAS BEEN OBSERVED TO BE PARTICULARLY PREVALENT IN ENHANCEMENT-MODE DEVICES WHICH ARE BIASED AT OR BELOW CUTOFF AND THAT IT BECOMES LESS APPARANT AS THE CHANNEL IS INVERTED.[9]

FIGURE 4-1 ILLUSTRATES THE MECHANISM BY WHICH GATE-CONTROLLED DRAIN-DIODE BREAKDOWN TAKES PLACE IN AN N-CHANNEL MOSFET. WHEN THE GATE VOLTAGE IS INSUFFICIENT TO ESTABLISH A CONDUCTING CHANNEL, THE TRANSISTOR IS SAID TO BE IN CUTOFF. WITH THE SOURCE AND SUBSTRATE GROUNDED AND THE DRAIN AT A POSITIVE POTENTIAL, A SPACE-CHARGE DEPLETION REGION EXISTS AROUND THE DRAIN JUNCTION. THE POTENTIAL DIFFERENCE BETWEEN THE DRAIN AND GATE TERMINALS AND BETWEEN THE DRAIN AND SUBSTRATE CAUSES AN ELECTRIC FIELD TO EXIST IN BOTH THE OXIDE AND IN THE DRAIN DEPLETION REGION.

SINCE THE DEPLETION REGION IS NARROWEST NEAR THE SEMICONDUCTOR SURFACE, THE ELECTRIC FIELD IN THIS CORNER REGION IS THE STRONGEST, AS INDICATED BY THE DENSITY OF THE ELECTRIC FIELD LINES. FURTHERMORE, SINCE THE DEPLETION REGION EXTENDS ALONG AND DIRECTLY BENEATH THE OXIDE, THE DEPLETION

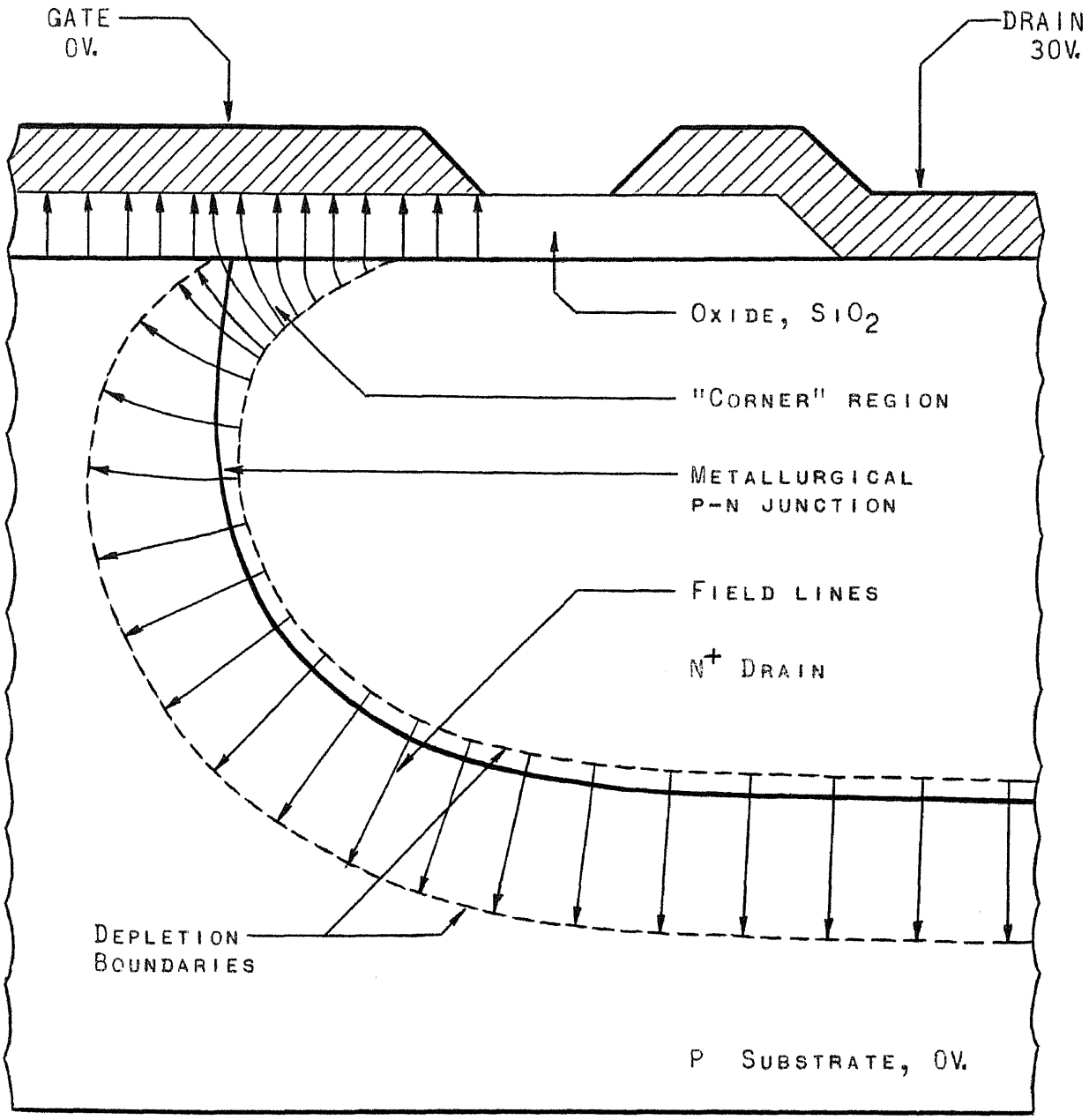

FIGURE 4-1. DRAIN-PORTION OF AN N-CHANNEL ENHANCEMENT MOSFET SHOWING THE MECHANISM OF DRAIN-DIODE BREAKDOWN IN THE "CORNER" REGION.

REGION FIELD LINES JOIN WITH AND REINFORCE THE FIELD LINES IN THE INSULATOR. THIS RESULTS IN A VERY HIGH FIELD INTENSITY IN THE CORNER REGION AND BRINGS ABOUT IMPACT IONIZATION AND AVALANCHE DRAIN-DIODE BREAKDOWN.[10]

4.4 Investigation of Drain Breakdown Under Conditions of Strong Channel Inversion in Enhancement MOS Transistors

Experimental Method. In order to evaluate the extent to which soft drain breakdown occurs and in order to correlate it with other surface-related phenomena in P-channel enhancement MOSFET's, drain breakdown characteristics of both relatively high- and low-noise transistors were obtained.

Using the Quan-Tech Model 327 Diode Noise Analyzer, drain breakdown and noise voltage versus drain current characteristics were plotted for each unit life-tested for threshold voltage drift. I-V characteristics were plotted up to and slightly beyond the threshold of drain breakdown.*

Noise voltage versus drain current at several gate voltages was plotted in order to determine the effects of

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*Drain breakdown was arbitrarily defined as occurring when the instantaneous saturation drain conductance reached approximately 100 micromhos. This limit was imposed in order to ensure that no unit exceeded its rated power dissipation level during the accompanying noise measurements. All noise measurements made at high drain voltages were accomplished in the shortest time interval possible without sacrificing accuracy. Due to the configuration of the noise measuring instrument, it was impossible to use any kind of heat sink.

VARIATIONS IN CHANNEL DEPTH AND ELECTRIC FIELD INTENSITY ON BOTH THE NOISE INTENSITY AND THE AMOUNT OF BREAKDOWN WHICH TOOK PLACE.

A CURVE TRACER WAS USED TO VISUALLY INVESTIGATE THE EFFECTS OF VARYING V_{GS} WHEN THE DEVICES WERE OPERATED AT A DRAIN VOLTAGE PRODUCING DRAIN BREAKDOWN.

ANALYSIS OF BREAKDOWN CHARACTERISTICS. DIFFERENCES BETWEEN THE DRAIN BREAKDOWN CHARACTERISTICS OF HIGH- AND LOW-NOISE TRANSISTORS IS MOST EASILY SEEN BY COMPARING THE HIGH VOLTAGE I-V CHARACTERISTICS OF SEVERAL DEVICES BIASED AT THE SAME GATE VOLTAGE.

FIGURE 4-2 ILLUSTRATES THE CHARACTERISTICS OF FIVE HIGH- AND FIVE LOW-NOISE TYPE DD07P MOSFET's. ALTHOUGH ALL OF THE TRANSISTORS EXHIBITED VARIOUS DEGREES OF SOFT DRAIN BREAKDOWN AT $V_{GS} = -5.5$ VOLTS, THREE OBSERVATIONS ARE IMMEDIATELY APPARANT:

1. ALL HIGH NOISE UNITS SHOWED CONSIDERABLY HIGHER SATURATION DRAIN CONDUCTANCE THAN DID THE UNITS HAVING A LOW NOISE INTENSITY;

2. THE BREAKDOWN CHARACTERISTICS OF THE HIGH NOISE TRANSISTORS ARE VERY SOFT COMPARED TO THOSE WITH LOW NOISE; AND

3. SOME HIGH NOISE UNITS APPEAR TO REACH THE THRESHOLD OF DRAIN BREAKDOWN AT A DRAIN VOLTAGE ONLY ABOUT HALF

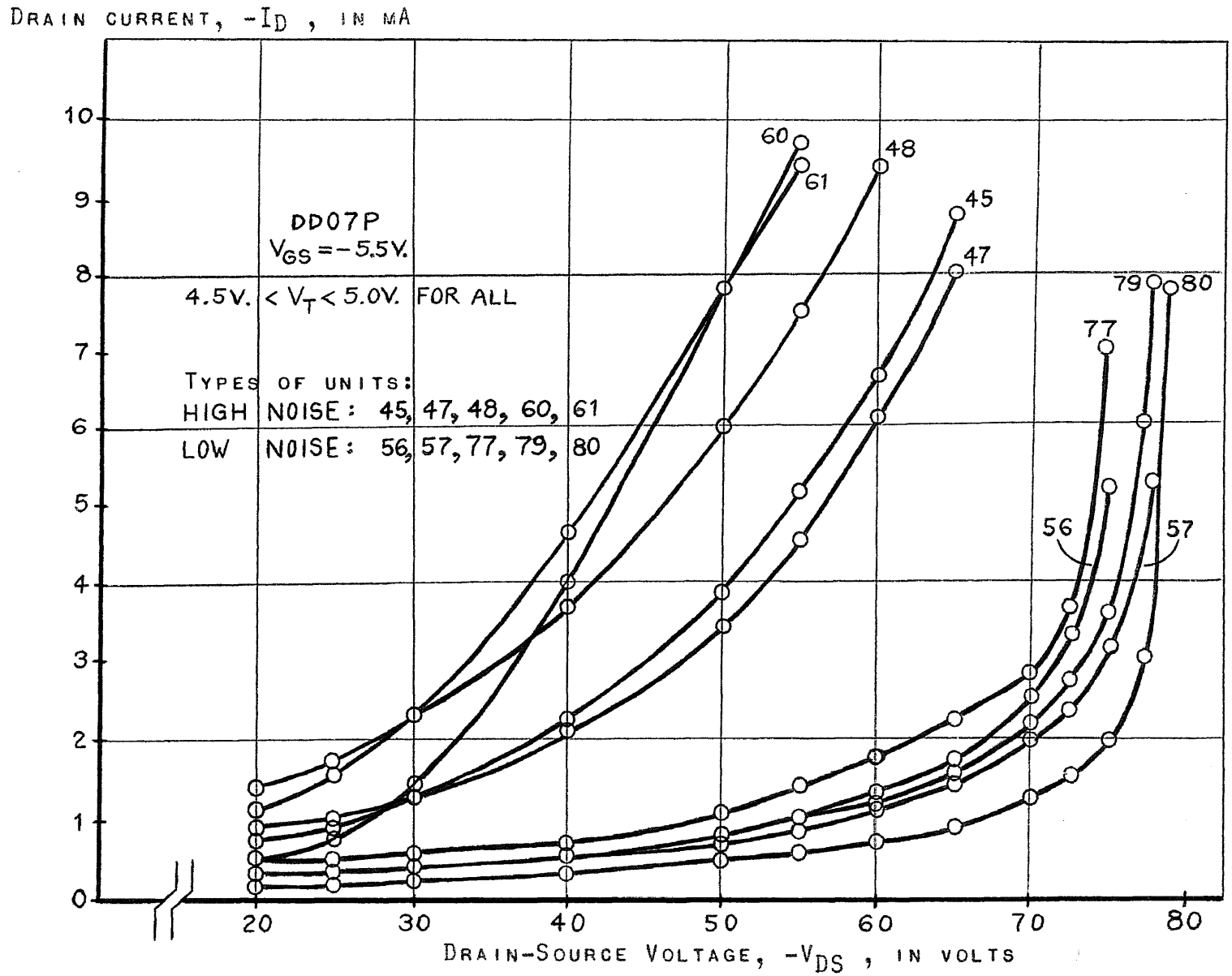


FIGURE 4-2. DRAIN BREAKDOWN CHARACTERISTICS OF FIVE HIGH- AND FIVE LOW-NOISE TYPE DD07P MOSFET's.

OF THAT REQUIRED BY THEIR LOW NOISE COUNTERPARTS.

RECALL THAT DRAIN LEAKAGE MEASUREMENTS CONDUCTED WITH ZERO GATE BIAS CONFIRMED THAT SATURATION DRAIN CONDUCTANCE WAS A STRICTLY SURFACE EFFECT. SINCE THE MAGNITUDE OF I_{DSS} WAS APPROXIMATELY THE SAME FOR BOTH HIGH- AND LOW-NOISE UNITS, IT MAY BE CONCLUDED THAT DRAIN-DIODE LEAKAGE WAS NOT A FACTOR INFLUENCING THE EXTENT OF DRAIN BREAKDOWN OBSERVED. RATHER, IT MAY BE STATED THAT AVALANCHE MULTIPLICATION IN THE CHANNEL--PRIMARILY IN THE DEPLETION REGION BETWEEN THE EXPOP AND THE DRAIN JUNCTION--WAS THE DOMINANT BREAKDOWN MECHANISM WHEN THE TRANSISTORS WERE BIASED WITH STRONGLY INVERTED CHANNELS.

SINCE THE RELATIVE INTENSITY OF 1/F NOISE IS RELATED TO THE SURFACE-STATE DENSITY, NOISE MEASUREMENTS AT CONSTANT DRAIN CURRENT AND GATE VOLTAGE APPEAR TO BE EXCELLENT INDICATORS OF THE EXPECTED "SOFTNESS" OF DRAIN BREAKDOWN. UNIT-TO UNIT VARIATIONS IN THE CHANNEL SEMICONDUCTOR IMPURITY CONCENTRATION AND/OR SURFACE-STATE DENSITY (BOTH OF WHICH HAVE BEEN SHOWN TO BE RELATED TO THE SATURATION DRAIN CONDUCTANCE) MAY BE RESPONSIBLE FOR THE GREAT DIFFERENCES IN DRAIN CHARACTERISTICS BETWEEN TRANSISTORS WITH RELATIVELY HIGH NOISE AND THOSE WITH RELATIVELY LOW NOISE INTENSITY.

APPENDIX D LISTS NOISE VOLTAGES VERSUS DRAIN CURRENT FOR ALL TRANSISTORS LIFE-TESTED FOR THRESHOLD VOLTAGE DRIFT AND GIVES CORRESPONDING DRAIN VOLTAGES FOR I-V CHARACTERISTICS.

Correlation of 1/F noise with drain breakdown. Figures 4-3 and 4-4 show the noise voltage-drain current characteristics at constant gate voltage for three low- and three high-noise DD07P MOSFET's, respectively. By comparing these curves with the drain characteristics shown in figure 4-2, it is possible to make four observations:

1. There is an approximate 1/F frequency dependence for the noise voltage over the full range of each I-V characteristic;

2. The noise characteristics are definitely peaked, increasing with the onset of drain breakdown and decreasing with further increases in drain current;

3. The peak noise voltage is lowest in the low noise transistors and occurs at a lower drain current but correspondingly higher drain voltage than for those units having a high noise intensity; and

4. The saturation drain conductance at the threshold of drain breakdown is approximately identical for each unit at the drain current for which its respective noise voltage is a maximum.

The first observation indicates that 1/F noise theory is appropriate, even after drain breakdown has resulted in substantial drain current. However, the peaking and steady decrease in noise voltage following drain breakdown was not

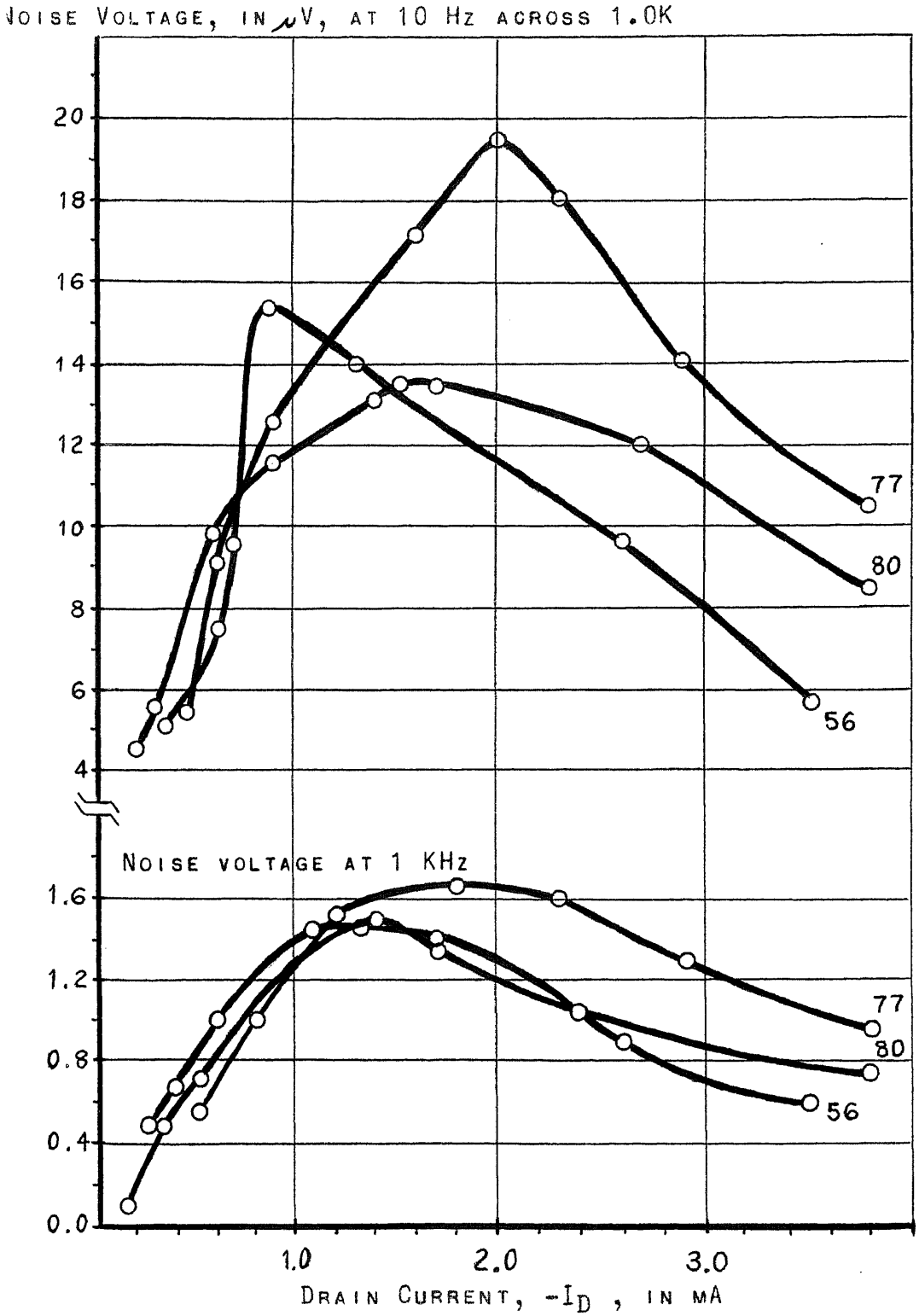


Figure 4-3. Noise voltage-drain current characteristics for three low noise type DD07P MOSFET's. V_{GS} =-5.5V. and V_{DS} ranged from -20 to -78V.

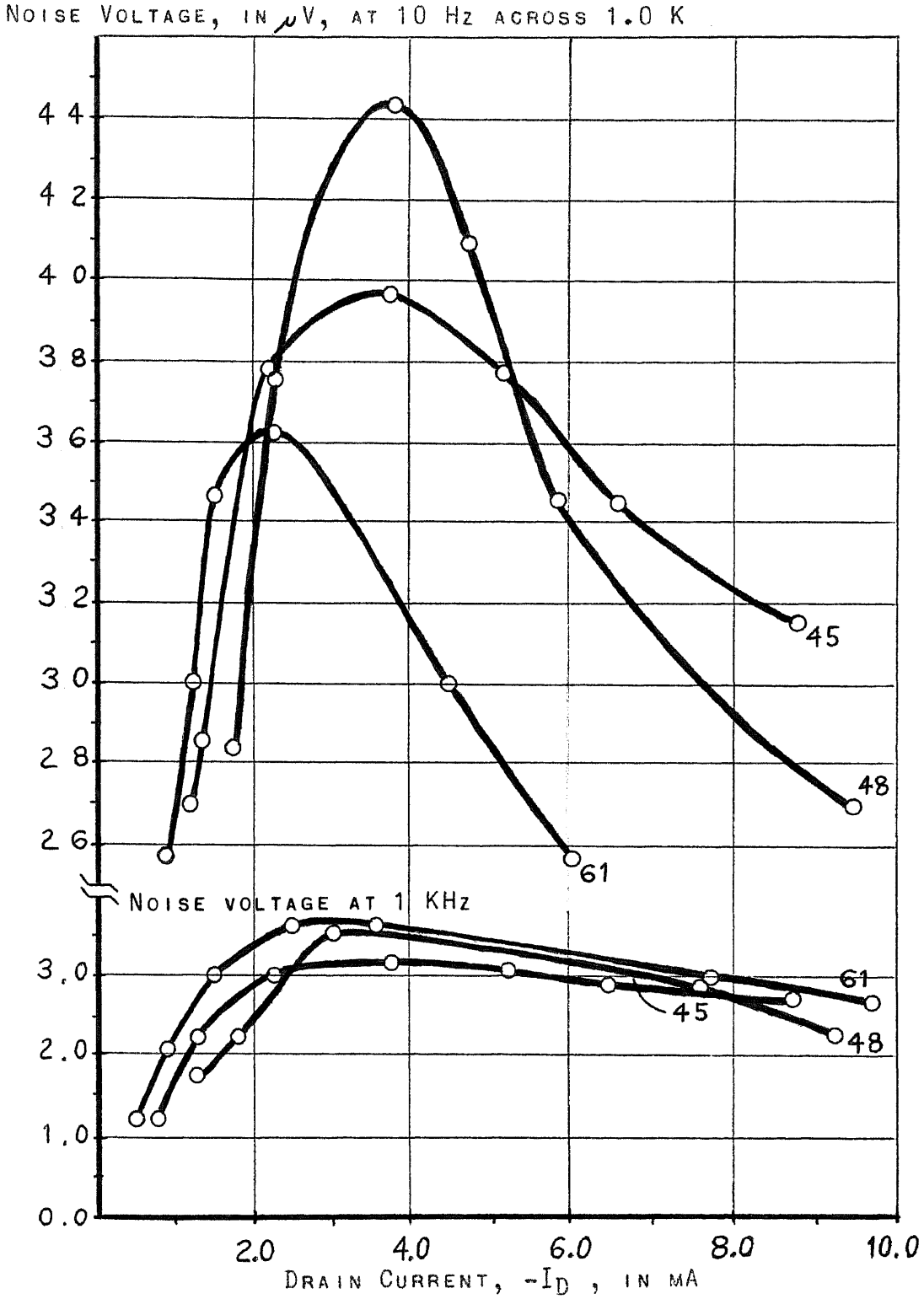


FIGURE 4-4. NOISE VOLTAGE-DRAIN CURRENT CHARACTERISTICS FOR THREE HIGH NOISE TYPE DD07P MOSFET's. V_{GS} = -5.5 V. AND V_{DS} RANGED FROM -20 TO -65V.

EXPECTED, PARTICULARLY IN VIEW OF THE FACT THAT THE NOISE INTENSITY DECREASES WHILE THE DRAIN CURRENT RISES ALMOST EXPONENTIALLY WITH FURTHER INCREASES IN DRAIN VOLTAGE.

THE RAPID INCREASE IN NOISE VOLTAGE AT THE ONSET OF DRAIN BREAKDOWN MAY BE EXPLAINED ON THE BASIS OF THE RELATIONSHIP BETWEEN 1/F NOISE AND CURRENT DENSITY. BY INCREASING $|-V_{DS}|$ WITH CONSTANT GATE VOLTAGE, THE EXPOP RECEDES TOWARD THE SOURCE, THEREBY PERMITTING INCREASED DRAIN CURRENT. WHEN THE DRAIN VOLTAGE IS SUFFICIENTLY LARGE, THE TRANSVERSE ELECTRIC FIELD IN THE CHANNEL DEPLETION REGION CAUSES IMPACT IONIZATION RESULTING IN AVALANCHE BREAKDOWN. INCREASED DRAIN CURRENT WITHIN A RELATIVELY CONSTANT CROSS-SECTION OF THE CHANNEL (DUE TO THE CONSTANT GATE VOLTAGE) RESULTS IN INCREASED CURRENT DENSITY AND CORRESPONDINGLY INCREASED 1/F NOISE INTENSITY.

AS THE DRAIN VOLTAGE IS FURTHER INCREASED, IONIZATION TAKES PLACE FURTHER ALONG THE DRAIN P-N JUNCTION. AS BREAKDOWN PROGRESSES, THE EFFECTIVE CROSS-SECTION THROUGH WHICH CARRIERS ARE INJECTED INTO THE DRAIN INCREASES. THIS LOWERS THE CURRENT DENSITY AND THE NOISE INTENSITY DECREASES PROPORTIONATELY.

FIGURE 4-5 SHOWS THE NOISE VOLTAGE-DRAIN CURRENT CHARACTERISTICS AT SEVERAL GATE VOLTAGES FOR A SINGLE HIGH NOISE TYPE DD07P MOSFET. IT IS EVIDENT THAT THE PEAK NOISE INTENSITY IS PROPORTIONAL TO THE APPLIED GATE VOLTAGE AND THAT

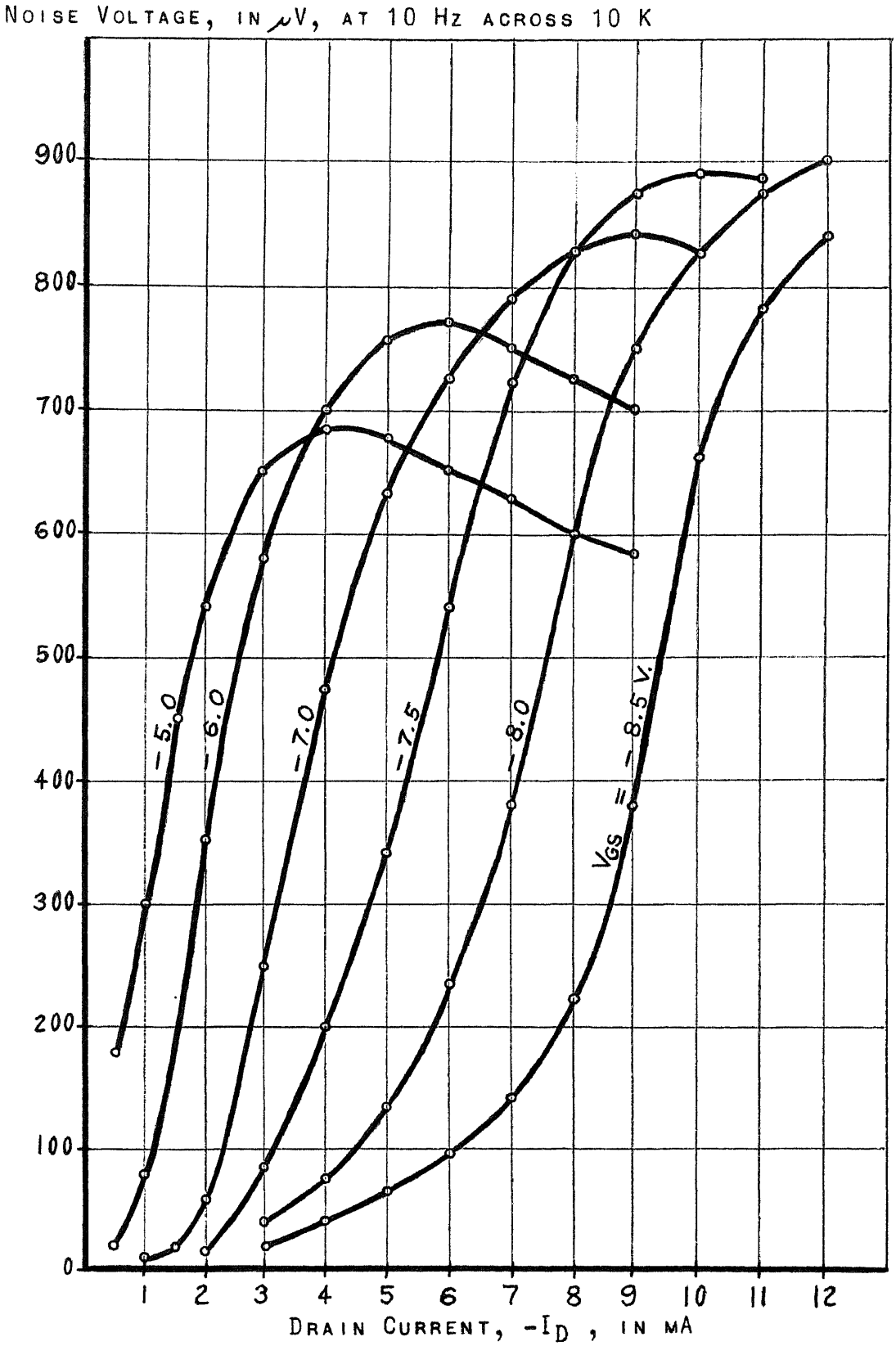


FIGURE 4-5. NOISE VOLTAGE-DRAIN CURRENT CHARACTERISTICS AT SEVERAL GATE VOLTAGES FOR A SINGLE HIGH NOISE TYPE DD07P MOSFET. UNIT NO. 61.

THE PEAKS OCCUR AT SUCCESSIVELY HIGHER VALUES OF DRAIN CURRENT WITH INCREASING $|-V_{GS}|$. THIS IS IN EXCELLENT AGREEMENT WITH THE FINDINGS OF HSU[11] WHO STATES THAT "LOW FREQUENCY NOISE INCREASES MONOTONICALLY WITH NEGATIVE GATE BIAS ON P-CHANNEL ENHANCEMENT MOSFET'S"[12] AT THE SAME DRAIN VOLTAGE, INDICATING THAT "THE SURFACE-STATE DENSITY INCREASES TOWARD THE EDGE OF THE VALENCE BAND."[13] IT WAS ALSO FOUND THAT THE SURFACE-STATE DENSITY INCREASED WITH INCREASED SURFACE POTENTIAL. THEREFORE, 1/F NOISE MEASUREMENTS AT CONSTANT DRAIN CURRENT SHOULD INDICATE THE RELATIVE SURFACE-STATE DENSITY AS A FUNCTION OF GATE BIAS.

THE THIRD OBSERVATION--DIFFERENCES IN THE MAGNITUDE OF THE PEAK NOISE VOLTAGE BETWEEN THE LOW NOISE TRANSISTORS AND THOSE HAVING HIGH NOISE INTENSITY--MAY BE TRACED TO DIFFERENCES IN SURFACE-STATE DENSITY BETWEEN THE VARIOUS DEVICES. SINCE 1/F NOISE IS DIRECTLY PROPORTIONAL TO SURFACE-STATE DENSITY, IT FOLLOWS THAT THOSE UNITS HAVING A RELATIVELY LOW NOISE INTENSITY ALSO POSSESS FEWER SURFACE STATES THAN HIGH NOISE TRANSISTORS.

THE FOURTH OBSERVATION INDICATES THAT EXCESS NOISE MEASUREMENTS MAY BE USED WITH SOME DEGREE OF ACCURACY TO DETERMINE THE APPROXIMATE BREAKDOWN VOLTAGE OF AN MOS TRANSISTOR WITHOUT ACTUALLY BREAKING DOWN THE DEVICE. SUCH NONDESTRUCTIVE TESTING COULD PROVE INVALUABLE WHEN IT IS DESIRED TO KNOW THE BREAKDOWN VOLTAGE OF A DEVICE OR THAT

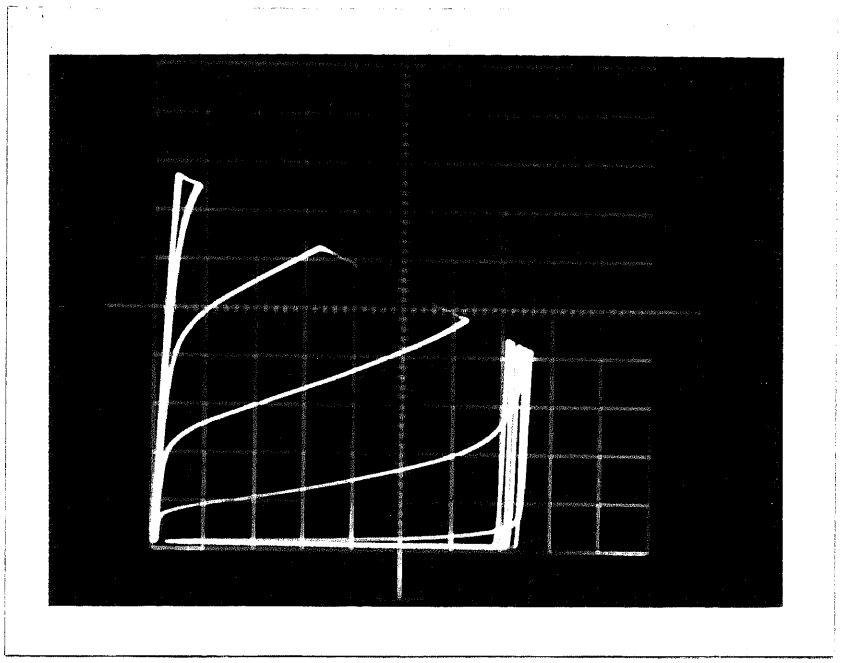
AN ENTIRE MOS INTEGRATED CIRCUIT. THE RELATIVE PEAK VOLTAGE THAT CAN BE SAFELY HANDLED BY A DEVICE COULD BE DETERMINED WITHOUT EXHAUSTIVE MEASUREMENTS WHICH, IF NOT DONE PROPERLY, COULD SUBJECT THE CHIP TO UNUSUALLY HIGH LEVELS OF POWER DISSIPATION.

4.5 Investigation of Gate-Controlled Drain-Diode Breakdown Under Cutoff Conditions

Experimental method. Drain breakdown characteristics at several gate voltages extending down below cutoff were plotted for transistors having relatively high- and relatively low-noise intensity. The Quan-Tech Model 327 Diode Noise Analyzer was used to obtain I-V curves for the type DD07P transistors which had undergone 500 hours of bias at $130 \pm 5°C$. Gate voltages ranged from $V_{GS} = -8.5$ to $+1$ volt. In addition, a curve tracer was used to visually investigate drain-diode breakdown and to obtain pictures showing extremes in this phenomena between high and low noise transistors.

Experimental results and discussion. Figures 4-6 and 4-7 illustrate the dramatic difference in drain breakdown characteristics between p-channel transistors having relatively high- and low-noise intensity. Figure 4-6 shows the typical moderate saturation drain conductance and soft channel breakdown at intermediate and highly negative gate voltages and the increasingly harder drain-diode breakdown at

DRAIN CURRENT, $-I_D$, 2MA/DIVISION

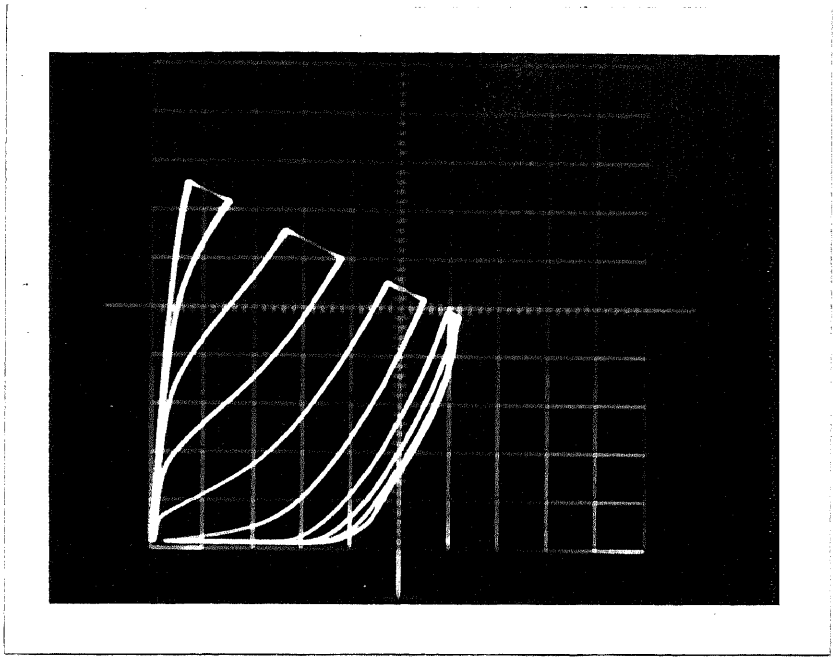


DRAIN VOLTAGE, $-V_{DS}$, 10 VOLTS/DIVISION

GATE VOLTAGE IN ONE VOLT INCREMENTS
STARTING FROM $-V_{GS} = 0$ VOLTS

FIGURE 4-6. PHOTOGRAPH SHOWING THE CURRENT-VOLTAGE DRAIN BREAKDOWN CHARACTERISTICS OF A RELATIVELY LOW NOISE P-CHANNEL ENHANCEMENT MOSFET. HARD DRAIN - DIODE BREAKDOWN IS EVIDENT AT LOW $|-V_{GS}|$ AND $-V_{DS} = 70$ VOLTS.

DRAIN CURRENT, $-I_D$, 2MA/DIVISION



DRAIN VOLTAGE, $-V_{DS}$, 10 VOLTS/DIVISION

GATE VOLTAGE IN ONE VOLT INCREMENTS
STARTING FROM $-V_{GS} = 0$ VOLTS

FIGURE 4-7. PHOTOGRAPH SHOWING THE CURRENT-VOLTAGE DRAIN BREAKDOWN CHARACTERISTICS OF A RELATIVELY HIGH NOISE P-CHANNEL ENHANCEMENT MOSFET. UNUSUALLY HIGH SATURATION DRAIN CONDUCTANCE AND VERY SOFT BREAKDOWN INDICATES THAT CHANNEL PUNCH-THROUGH HAS OCCURED.

LOW GATE VOLTAGES FOR A VERY LOW NOISE DEVICE. FIGURE 4-7 SHOWS THE CHARACTERISTICS OF A TECHNICALLY POOR, HIGH NOISE MOS TRANSISTOR.

IT IS EVIDENT THAT INCREASING THE MAGNITUDE OF THE GATE VOLTAGE LESSENS THE POTENTIAL DIFFERENCE BETWEEN THE DRAIN AND GATE TERMINALS, THEREBY REDUCING THE ELECTRIC FIELD INTENSITY IN THE CORNER REGION AND SOFTENING THE BREAKDOWN CHARACTERISTICS. ON THE OTHER HAND, AS THE GATE VOLTAGE IS BROUGHT TO ZERO, OR EVEN MADE POSITIVE,* THE ELECTRIC FIELD AT THE SEMICONDUCTOR SURFACE NEAR THE DRAIN JUNCTION IS GREATLY INCREASED AND THE BREAKDOWN CHARACTERISTICS BECOME VERY SHARP.

THE VERY HIGH SATURATION DRAIN CONDUCTANCE (WHICH GIVES THE CURVES IN FIGURE 4-7 THE APPEARANCE OF TRIODE CHARACTERISTICS) FOUND IN THE RELATIVELY HIGH NOISE TRANSISTOR IS INDICATIVE OF <u>DRAIN PUNCH-THROUGH</u>, WHEREBY THE CHANNEL DEPLETION REGION EXTENDS FROM THE DRAIN TO THE SOURCE AND THE DRAIN CURRENT IS SPACE-CHARGE LIMITED. FROHMAN-BENTCHKOWSKY AND GROVE[14] HAVE INVESTIGATED THE MECHANISMS BY WHICH MOS TRANSISTORS BREAKDOWN BY THE PUNCH-THROUGH PHENOMENON. THEY HAVE CONCLUDED THAT IT IS CHARACTERISTIC OF DEVICES HAVING SHORT CHANNEL LENGTHS AND/OR UNUSUALLY LOW BULK DOPING.

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*THE DD07P MOSFET'S POSSESSED ZENER DIODE VOLTAGE LIMITING BETWEEN THE GATE AND SOURCE. APPLICATION OF A POSITIVE GATE VOLTAGE GREATER THAN 1V. WOULD HAVE DRAWN TOO MUCH CURRENT THROUGH THIS DIODE, CAUSING EXCESSIVE HEATING.

HOWEVER, UNDER THE ASSUMPTION THAT BOTH THE SEMICONDUCTOR IMPURITY CONCENTRATION AND CHANNEL LENGTH WERE NEARLY IDENTICAL FOR BOTH THE HIGH AND LOW NOISE TRANSISTORS, AND ON THE BASIS OF THE EARLIER CORRELATION BETWEEN 1/F NOISE AND SURFACE-STATE DENSITY, THERE IS STRONG EVIDENCE TO SUGGEST THAT CONDITIONS AT THE SILICON-SILICON DIOXIDE INTERFACE ARE IMPORTANT DETERMINING FACTORS IN THE TYPE OF DRAIN BREAKDOWN WHICH OCCURS UNDER A GIVEN BIAS CONDITION. SINCE SATURATION DRAIN CONDUCTANCE AND 1/F NOISE ARE BOTH SURFACE-RELATED, IT WAS CONCLUDED THAT THE RELATIVE NOISE INTENSITY WAS INDICATIVE OF EITHER SOFT OR HARD DRAIN BREAKDOWN.

IT IS CUSTOMARY TO DESIGN HIGH FREQUENCY TRANSISTORS (INCLUDING THE TYPES DD07P, DD08P, AND DD08K MOSFET'S USED IN THIS RESEARCH) WITH RELATIVELY SHORT CHANNELS. THEREFORE, 1/F NOISE MEASUREMENTS MAY BE USEFUL IN "WEEDING OUT" DEVICES HAVING BREAKDOWN CHARACTERISTICS SIMILAR TO THOSE OF FIGURE 4-7.

REFERENCES

[1]A. S. Grove, Physics and Technology of Semiconductor Devices (New York, 1967), p. 191. Ref. 1967-7.

[2]Ibid., p. 159.

[3]Ibid., p. 164.

[4]Richard S. Cobbold, Theory and Application of Field-Effect Transistors (New York, 1970), p. 265. Ref. 1970-2.

[5]Ibid., p. 266.

[6]H. Kressel, "A Review of the Effect of Imperfections on the Electrical Breakdown of P-N Junctions," RCA Review (1967), p. 179. Ref. 1967-9.

[7]Ibid., p. 187.

[8]Op. Cit., Cobbold, p. 267.

[9]Ibid., p. 267.

[10]Ibid., p. 267.

[11]S. T. Hsu, "Surface State Related 1/F Noise in MOS Transistors," Solid-State Electronics(GB) (1970), pp. 1451-1459. Ref. 1970-4.

[12]Ibid., p. 1457.

[13]Ibid., p. 1457.

[14]D. Frohman-Bentchkowsky and Grove, "Conductance of MOS Transistors in Saturation," IEEE Transactions on Electron Devices (1969), p. 111. Ref. 1969-2.

CHAPTER 5

CONCLUSIONS AND DISCUSSION OF RESULTS

THIS INVESTIGATION HAS FOUND A DEFINITE CORRELATION BETWEEN EXCESS NOISE INTENSITY AND DRAIN BREAKDOWN IN P-CHANNEL ENHANCEMENT-MODE MOS FIELD-EFFECT TRANSISTORS. IN PARTICULAR, IT WAS FOUND THAT TRANSISTORS HAVING RELATIVELY LOW NOISE INTENSITY EXHIBITED SHARPER BREAKDOWN CHARACTERISTICS AT HIGHER DRAIN VOLTAGES THAN DEVICES HAVING HIGH NOISE. IT IS BELIEVED THAT THE SURFACE-STATE DENSITY IS RELATED TO THE SEMICONDUCTOR IMPURITY CONCENTRATION AND THAT TRANSISTORS HAVING LOW BULK DOPING AND/OR HIGH SURFACE-STATE DENSITY MAY BE EXPECTED TO EXHIBIT HIGH SATURATION DRAIN CONDUCTANCE AND SOFT BREAKDOWN CHARACTERISTICS. FINALLY, IT WAS CONCLUDED THAT 1/F NOISE MEASUREMENTS MAY BE USED IN NONDESTRUCTIVE TESTING TO DETERMINE THE APPROXIMATE BREAKDOWN VOLTAGE OF INDIVIDUAL DEVICES OR ENTIRE MOS INTEGRATED CIRCUITS.

PREVIOUS INVESTIGATIONS HAVE TRACED THE ORIGIN OF 1/F NOISE TO MODULATION OF SURFACE RECOMBINATION AND HAVE SHOWN THAT THE NOISE INTENSITY IS DIRECTLY PROPORTIONAL TO BOTH THE SURFACE-STATE DENSITY AND THE CURRENT DENSITY. MEASUREMENTS OF DRAIN CURRENT FLUCTUATIONS AT 10Hz AND AT 1KHz WERE FOUND TO BE CONSISTENT WITH 1/F NOISE THEORY. THE FREQUENCY DEPENDENCE WAS FOUND TO EXIST OVER A WIDE RANGE OF OPERATING CONDITIONS, INCLUDING AT THE ONSET AND FOLLOW-

ING DRAIN BREAKDOWN. THEREFORE, 1/F NOISE THEORY WAS APPLIED IN THIS INVESTIGATION.

RESULTS FROM LIFE-TESTING FOR THRESHOLD VOLTAGE DRIFT WERE CONSISTENT WITH ACCEPTED THEORY OF IONIC DRIFT IN THE OXIDE. EXCESS NOISE INTENSITY, PARTICULARLY AT 1KHz, SHOWED A SUBSTANTIAL INCREASE FOLLOWING NEGATIVE GATE BIAS AT $130 \pm 5°C$ FOR 500 HOURS. THIS WAS INDICATIVE OF INCREASED SURFACE-STATE DENSITY AND CONFIRMS THAT CATIONS AT THE $Si-SiO_2$ INTERFACE CONTRIBUTE TO AN INCREASE IN THE NUMBER OF FAST TRAPPING STATES. IT WAS CONCLUDED THAT IONIC DRIFT NEAR THE SEMICONDUCTOR SURFACE RESULTED IN A LARGE NUMBER OF SHALLOW TRAPS, THE FAST TIME CONSTANTS OF WHICH ACCOUNTED FOR AN UNUSUALLY HIGH INCREASE IN NOISE INTENSITY AT HIGHER FREQUENCIES.

IT IS WELL KNOWN THAT SATURATION DRAIN CONDUCTANCE IS DIRECTLY PROPORTIONAL TO THE OXIDE THICKNESS AND INDIRECTLY PROPORTIONAL TO THE SEMICONDUCTOR IMPURITY CONCENTRATION. CURRENT-VOLTAGE CHARACTERISTICS OF SEVERAL TRANSISTORS SHOWED THAT HIGH DRAIN CONDUCTANCE CORRESPONDED TO HIGH 1/F NOISE INTENSITY. THIS ESTABLISHED A CORRELATION BETWEEN DRAIN CONDUCTANCE, SURFACE-STATE DENSITY, AND THE LEVEL OF BULK DOPING.

SINCE THERE WAS NO CORRELATION BETWEEN I_{DSS} AND OBSERVED DIFFERENCES BETWEEN TRANSISTORS HAVING RELATIVELY HIGH AND LOW NOISE, IT WAS CONCLUDED THAT HIGH SATURATION DRAIN CON-

DUCTANCE IS STRICTLY A SURFACE EFFECT AND THAT THE RELATIVE 1/F NOISE INTENSITY MAY BE USED TO CORRELATE DRAIN CONDUCTANCE WITH THE SURFACE-STATE DENSITY.

IT WAS FOUND THAT TRANSISTORS HAVING RELATIVELY HIGH EXCESS NOISE CONSISTENTLY EXHIBITED SOFT DRAIN BREAKDOWN AND HIGH DRAIN CONDUCTANCE WHILE BREAKDOWN IN RELATIVELY LOW NOISE DEVICES UNDER SIMILAR BIAS CONDITIONS WAS ALWAYS SIGNIFICANTLY MORE ABRUPT AND WAS FOUND TO OCCUR AT UP TO TWICE THE DRAIN VOLTAGE.

IN A FEW EXTREME CASES, VERY HIGH NOISE TRANSISTORS BIASED IN CUTOFF SHOWED BREAKDOWN CHARACTERISTICS WHICH WERE INDICATIVE OF PUNCH-THROUGH. IT WAS CONCLUDED THAT DRAIN BREAKDOWN IS RELATED TO THE SEMICONDUCTOR IMPURITY CONCENTRATION AND THE SURFACE-STATE DENSITY AND THAT LOW BULK DOPING AND/OR AN UNUSUALLY HIGH DENSITY OF SURFACE STATES FACILITATES EXPOP RECESSION TOWARD THE SOURCE WHEN THE TRANSISTOR IS OPERATED IN SATURATION.

OF PARTICULAR SIGNIFICANCE WAS THE FACT THAT THE NOISE INTENSITY CONSISTENTLY PEAKED AT THE THRESHOLD OF DRAIN BREAKDOWN AND STEADILY DECREASED WITH INCREASING DRAIN CURRENT. SINCE THE NOISE INTENSITY IS DIRECTLY PROPORTIONAL TO THE CURRENT DENSITY WITHIN THE DEVICE, IT WAS REASONED THAT THE EFFECTIVE CHANNEL DEPTH AT THE DRAIN JUNCTION INCREASES AS IONIZATION PROGRESSES FOLLOWING THE ONSET OF DRAIN BREAKDOWN. THIS MAY BE EXPLOITED IN NON-

DESTRUCTIVE TESTING OF MOS DEVICES, INCLUDING ENTIRE MOS INTEGRATED CIRCUITS, BY MEASURING THE RELATIVE 1/F NOISE INTENSITY TO DETERMINE THE APPROXIMATE DRAIN BREAKDOWN VOLTAGE WITHOUT ACTUALLY BREAKING DOWN THE DEVICE.

IN CONCLUSION, AN EXCEPTIONALLY HIGH 1/F NOISE INTENSITY IS INDICATIVE OF A HIGH SURFACE-STATE DENSITY AND/OR LOW SEMICONDUCTOR IMPURITY CONCENTRATION. MOS TRANSISTORS HAVING RELATIVELY LOW NOISE INTENSITY MAY BE EXPECTED TO EXHIBIT LOW SATURATION DRAIN CONDUCTANCE AND SHARP DRAIN BREAKDOWN CHARACTERISTICS AT HIGHER DRAIN VOLTAGES THAN HIGH NOISE DEVICES.

APPENDIX A

THE INFLUENCE OF DEVICE PARAMETERS ON THE MOS SATURATION DRAIN CONDUCTANCE

FROHMAN-BENTCHKOWSKY AND GROVE[1] AND OTHERS[2,3] HAVE INVESTIGATED THE DRAIN CONDUCTANCE OF MOS TRANSISTORS IN THE SATURATION REGION AND HAVE FOUND IT TO BE "A SENSITIVE FUNCTION OF THE OXIDE THICKNESS AS WELL AS THE SUBSTRATE IMPURITY CONCENTRATION."[4] THE FOLLOWING IS A MODEL PRESENTED WHICH EVALUATES THE SATURATION DRAIN CONDUCTANCE OF AN N-CHANNEL MOS TRANSISTOR ON THE BASIS OF DEVICE PARAMETERS.

THE DRAIN VOLTAGE AT THE ONSET OF SATURATION MAY BE EXPRESSED AS[5]

$$V_{DSAT} = V_G - V_{FB} - 2\phi_F + \frac{K_S \epsilon_0 q C_B}{C_0^2} \cdot \left[1 - \sqrt{1 + \frac{2C_0^2 (V_G - V_{FB})}{K_S \epsilon_0 q C_B}} \right] \qquad \text{A-1}$$

WHERE C_B = IMPURITY CONCENTRATION OF THE SUBSTRATE

$C_0 = K_0 \epsilon_0 / x_0$ = CAPACITANCE OF THE OXIDE PER UNIT AREA

K_0, K_S = DIELECTRIC CONSTANTS OF THE OXIDE AND SEMICONDUCTOR, RESPECTIVELY

V_G = MOS TRANSISTOR GATE VOLTAGE

V_{FB} = FLAT-BAND VOLTAGE

q = MAGNITUDE OF ELECTRONIC CHARGE

x_o = THICKNESS OF THE OXIDE

ϵ_o = PERMITTIVITY OF FREE SPACE

ϕ_F = FERMI POTENTIAL IN THE SUBSTRATE

THE CORRESPONDING DRAIN CURRENT WHEN THE DRAIN VOLTAGE IS GREATER THAN V_{DSAT} IS GIVEN BY[6]

$$I_{DSAT}\Big|_{V_D = V_{DSAT}} = \frac{I_{DSAT}^*}{1 - \Delta L/L} \qquad \text{A-2}$$

WHERE I_{DSAT}^* IS THE DRAIN CURRENT WHEN V_D V_{DSAT}, L IS THE EFFECTIVE LENGTH OF THE INVERTED CHANNEL BEFORE SATURATION, ΔL IS THE LENGTH BY WHICH THE CHANNEL IS SHORTENED WHEN THE EXPOP HAS MOVED TOWARD THE SOURCE, AND WHERE IT IS ASSUMED THAT AN INCREASE IN DRAIN CURRENT AFTER THE ONSET OF SATURATION IS ATTRIBUTED ENTIRELY TO A REDUCTION OF CHANNEL LENGTH. IF THE EXPOP RECEDES ONLY SLIGHTLY AND $\Delta L \ll L$,

$$I_{DSAT} \simeq I_{DSAT}^* \qquad \text{A-3}$$

OVER A WIDE RANGE OF DRAIN VOLTAGES IN THE SATURATION REGION OF THE CURRENT-VOLTAGE CHARACTERISTICS.

THE LENGTH OF THE CHANNEL DEPLETION REGION BETWEEN THE EXPOP AND THE DRAIN JUNCTION IS GIVEN BY[7]

$$\Delta L = \frac{V_D - V_{DSAT}}{\mathcal{E}_T} \qquad \text{A-4}$$

WHERE V_D IS THE POTENTIAL AT THE DRAIN, V_{DSAT} IS THE POTENTIAL AT THE EXPOP, AND WHERE $\mathcal{E}_T$, THE AVERAGE TRANSVERSE ELECTRIC FIELD IN THE CHANNEL DEPLETION REGION, IS COMPOSED OF COMPONENTS ASSOCIATED WITH THE FOLLOWING:

1. THE ELECTRIC FIELD DUE TO THE FIXED CHARGE IN THE REVERSE BIASED DRAIN-TO-SUBSTRATE P-N JUNCTION;

2. THE FRINGING ELECTRIC FIELD DUE TO THE DRAIN-TO-GATE POTENTIAL DROP, $V_D - V_G'$; AND

3. THE FRINGING ELECTRIC FIELD DUE TO THE POTENTIAL DIFFERENCE $V_G' - V_{DSAT}$ BETWEEN THE GATE AND THE EXPOP AND MAY BE EXPRESSED AS[8]

$$\mathcal{E}_T = \frac{1}{K}(V_D - V_{DSAT})^{\frac{1}{2}} + \varsigma\frac{K_O}{K_S}\frac{(V_D - V_G')}{x_O} + \xi\frac{K_O}{K_S}\frac{(V_G' - V_{DSAT})}{x_O} \qquad \text{A-5}$$

WHERE $V_G' = V_G + Q_{SS}/C_O$ = THE EFFECTIVE GATE VOLTAGE

Q_{SS} = FIXED SURFACE-STATE CHARGE DENSITY PER UNIT AREA

ς, ξ = FIELD-FRINGING FACTORS EXPERIMENTALLY FOUND TO BE 0.2 AND 0.6, RESPECTIVELY[9]

AND WHERE[10]

$$K = \left(\frac{2K_S\epsilon_O}{\mathcal{G}C_B}\right)^{\frac{1}{2}} \qquad \text{A-6}$$

IS A CONSTANT INVERSELY PROPORTION TO THE SUBSTRATE IMPURITY CONCENTRATION.

AFTER SUBSTITUTING FOR $\mathcal{E}_T$ IN EQUATION A-4, THE LENGTH OF THE DEPLETION REGION IS GIVEN BY[11]

$$\Delta L = K(V_D - V_{DSAT})^{-\frac{1}{2}} + \frac{K_S x_O}{K_O}\frac{(V_D - V_{DSAT})}{\alpha(V_D - V_G') + \beta(V_G' - V_{DSAT})} \qquad \text{A-7}$$

WHICH EXPRESSES ΔL BY THE SUM OF TWO SEMI-AUTONOMOUS TERMS. THE FIRST IS AN INVERSE FUNCTION OF THE SEMICONDUCTOR IMPURITY CONCENTRATION (BASED ON THE EXPRESSION FOR K) AND THE SECOND IS DIRECTLY PROPORTIONAL TO THE OXIDE THICKNESS. ACCORDINGLY, THERE ARE TWO LIMITING CASES WHICH EMPHASIZE THE DEPENDENCIES OF THE SATURATION DRAIN CONDUCTANCE ON THE DEVICE PARAMETERS.

CASE 1. $x_o \gg K(V_D - V_{DSAT})^{\frac{1}{2}}$. WITH THE ASSUMPTION OF A HIGH SUBSTRATE IMPURITY CONCENTRATION, THICK OXIDE LAYER, OR BOTH, THE REDUCTION IN CHANNEL LENGTH BECOMES[12]

$$\Delta L \simeq K(V_D - V_{DSAT})^{\frac{1}{2}} \qquad \text{A-8}$$

AND THE SATURATION DRAIN CONDUCTANCE DUE TO A DIFFERENTIAL REDUCTION IN CHANNEL LENGTH FROM EQUATION 1-1 BECOMES[13]

$$g_{dSAT} \simeq \frac{K I_{DSAT}^{*}}{2L(1 - \Delta L/L)^2 \cdot (V_D - V_{DSAT})^{\frac{1}{2}}} \qquad \text{A-9}$$

WHICH IS DEPENDENT ONLY ON THE LEVEL OF BULK DOPING, C_B.

IT IS EVIDENT THAT THE SMALL-SIGNAL SATURATION DRAIN CONDUCTANCE INCREASES AS THE SQUARE-ROOT OF THE IMPURITY CONCENTRATION DECREASES. THIS AGREES WELL WITH RESULTS FOUND BY CRAWFORD[14] WHO HAS EXPRESSED THE LENGTH OF THE CHANNEL DEPLETION REGION AS A FUNCTION OF V_T, THE THRESHOLD VOLTAGE, AND THE DONOR IMPURITY CONCENTRATION[15]

$$\Delta L = \sqrt{\frac{2\epsilon_s [V_D - (V_G - V_T)]}{q N_D}} \qquad \text{A-10}$$

CASE 2. $x_o \ll K(V_D - V_{DSAT})^{\frac{1}{2}}$. WITH LOW BULK DOPING, THIN OXIDE, OR BOTH, ΔL IS GIVEN BY[16]

$$\Delta L \simeq \frac{K_s x_o}{K_o} \frac{(V_D - V_{DSAT})}{\alpha(V_D - V_G') + \beta(V_G' - V_{DSAT})} \qquad A\text{-}11$$

AND THE CORRESPONDING SMALL-SIGNAL SATURATION DRAIN CONDUCTANCE IS EXPRESSED AS[17]

$$g_{d_{SAT}} = \frac{K_s x_o}{K_o L} \frac{(\beta-\alpha)(V_G' - V_{DSAT})}{[\alpha(V_D - V_G') + \beta(V_G' - V_{DSAT})]^2} \cdot \frac{I_{DSAT}^*}{(1 - \Delta L/L)^2} \qquad A\text{-}12$$

WHICH IS A FUNCTION OF THE OXIDE THICKNESS ONLY. IT IS EVIDENT THAT VARIATIONS IN THE OXIDE THICKNESS PRODUCE DIRECT VARIATIONS IN DRAIN CONDUCTANCE. THE TERM x_o IS THEREFORE SLIGHTLY MORE DOMINANT AN INFLUENCING FACTOR THAN C_B.

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[4]Op. Cit., Bentchkowsky and Grove, p. 108.

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[6]Ibid., p. 109.

[7]Ibid., p. 109.

[8]Ibid., p. 110.

[9]Ibid., p. 109.

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[11]Ibid., p. 110.

[12]Ibid., p. 110.

[13]Ibid., p. 110.

[14]Robert H. Crawford, MOSFET in Circuit Design (New York, 1967). Ref. 1967-4.

[15]Ibid., p. 35.

[16]Op. Cit., Bentchkowsky and Grove, p. 110.

[17]Ibid., p. 110.

APPENDIX B

A DERIVATION OF THE EQUATION OF THE SPECTRAL INTENSITY OF THE SHORT-CIRCUIT DRAIN CURRENT FLUCTUATIONS IN METAL-OXIDE-SEMICONDUCTOR TRANSISTORS

THE ORIGIN OF EXCESS NOISE IN MOS TRANSISTORS CAN BE TRACED TO "CONDUCTION CHANNEL CHARGE DENSITY FLUCTUATIONS CAUSED BY THE MODULATION OF SURFACE POTENTIAL DUE TO RANDOM OCCUPANCY OF SURFACE STATES."[1] HSU[2] HAS UNDERTAKEN A DERIVATION OF THE 1/F NOISE SPECTRAL INTENSITY OF P-CHANNEL ENHANCEMENT MOSFET'S BASED ON MODULATION OF SURFACE-STATE DENSITY WITH THE FOLLOWING FIVE ASSUMPTIONS:[3]

1. ONLY A ONE-DIMENTIONAL PROBLEM IS CONSIDERED FOR CARRIER DISTRIBUTION AT THE FIELD-INDUCED DEPLETION REGION.

2. THE SURFACE STATES ARE UNIFORMLY DISTRIBUTED IN SPACE AND IN ENERGY AT THE CENTRAL PORTION OF THE SILICON FORBIDDEN GAP.

3. SINCE THE OXIDE THICKNESS IS ON THE ORDER OF 600 TO 2000Å, AND SINCE IT HAS BEEN SHOWN THAT THE GREAT MAJORITY OF SURFACE STATES RESIDE WITHIN NO MORE THAN 20Å FROM THE $Si-SiO_2$ INTERFACE,[4] ALL SURFACE STATES ARE LOCATED AT THE SURFACE OR INTERFACE OF THE OXIDE AND SILICON SUBSTRATE.

4. THE RELAXATION TIME OF FREE HOLES AND ELECTRONS INSIDE THE SURFACE DEPLETION REGION IS NEGLIGIBLY SMALL COMPARED TO THAT OF THE SURFACE STATES.

5. FOR A P-CHANNEL MOSFET, WHEN THE SURFACE IS INVERTED, THE FREE HOLE CONCENTRATION IS VERY LARGE WHILE THE FREE ELECTRON DENSITY IS NEGLIGIBLY SMALL IN THE CONDUCTION CHANNEL. THEREFORE, THE SURFACE STATES ACT AS TRAPPING CENTERS INSTEAD OF RECOMBINATION CENTERS.

USING THE GAIN-LOSS PROCESS OF BURGESS[5,6] AND OF VAN VLIET AND FASSETT,[7] THE RATE THAT SURFACE STATES OF ENERGY E, LOCATED AT A DISTANCE X INTO THE SILICON DIOXIDE LAYER, GAIN HOLES CAN BE EXPRESSED AS[8]

$$G = c\left[p_s \eta_T(E) + \eta_{SI}\eta_T(E)\right] A \Delta E \Delta x \qquad \text{B-1}$$

WHERE A = EFFECTIVE AREA OF THE GATE

$\eta_T(E)$ = NUMBER OF EMPTY SURFACE STATES AT ENERGY E AND LOCATED AT A DISTANCE X FROM THE $Si-SiO_2$ INTERFACE

η_{SI} = FREE ELECTRON CONCENTRATION AT THE SURFACE WHEN THE FERMI LEVEL IS AT THE SURFACE-STATE LEVEL

p_s = HOLE DENSITY IN THE INVERTED CHANNEL OF A P-CHANNEL ENHANCEMENT MOSFET

AND WHERE c IS THE HOLE CAPTURE PROBABILITY OF SURFACE STATES, A FUNCTION OF ENERGY AND DISTANCE INTO THE OXIDE AND STRONGLY DEPENDENT ON THE LOCATION OF THE TRAPPING CENTER, WHICH MAY BE EXPRESSED AS[9]

$$c = c_s e^{-\alpha x} \qquad \text{B-2}$$

HERE c_s IS THE CAPTURE PROBABILITY AT A DISTANCE $x = 0$ FROM THE $Si-SiO_2$ INTERFACE AND THE FACTOR α IS GIVEN BY[10]

$$\alpha = \frac{4\pi}{\hbar}\sqrt{2m^* E_B} \qquad \text{B-3}$$

WHERE E_B = ENERGY BARRIER TO BE TUNNELED BY HOLES

$\hbar$ = PLANCK'S CONSTANT

m^* = EFFECTIVE MASS OF A HOLE

If the capture probability of electrons is assumed to be the same as that for holes, then the rate that the surface states of energy E lose holes at a distance x into the oxide is given by [11]

$$R = c\left[\eta_s p_T(E) + p_{s1} p_T(E)\right] A\Delta E\Delta x \qquad \text{B-4}$$

where η_s = Electron density in the inverted channel of a p-channel enhancement MOSFET

p_{s1} = Free hole concentration at the surface when the Fermi level is at the surface-state level

$p_T(E)$ = Density of trapped holes at energy E and located at a distance x from the Si-SiO_2 interface

The time constant for the surface-state occupancy fluctuation, obtained by differentiating equations B-1 and B-4 with respect to the number of holes in the surface states ($p_T A\Delta E\Delta x$), is given by [12]

$$\tau = \frac{1}{c\left[p_{so} + \eta_{s1} + p_{s1} + \eta_{so}\right]} \qquad \text{B-5}$$

where p_{so} and η_{so} are the steady-state values of p_s and η_s, respectively.

When the surface is inverted, assumption (5) reduces the expression for τ to [13]

$$\tau = \frac{1}{c(p_{so} + \eta_{s1})} \qquad \text{B-6}$$

"THE VARIANCE OF THE FLUCTUATION OF THE TOTAL NUMBER OF OCCUPIED SURFACE STATES IN AN ENERGY ΔE AND AT A DISTANCE Δx IS GIVEN BY $G_0\tau$,"[14] WHERE G_0 IS THE STEADY-STATE RATE OF FORMATION OF TRAPPING CENTERS (THE RATE OF GAINING HOLES) WHICH IS ASSUMED TO BE EQUAL TO R_0, THE STEADY-STATE RATE OF LOSING HOLES. IN THE INVERSION REGION OF A P-CHANNEL ENHANCEMENT MOSFET VIRTUALLY ALL SURFACE STATES CAN BE THOUGHT OF AS TRAPPING CENTERS AND THE VARIANCE OF THE TRAPPED HOLE DENSITY FLUCTUATION IS[15]

$$\text{VAR}\,p_T = \frac{N_T p_{sc} n_{si}}{(p_{sc} + n_{si})^2} \qquad \text{B-7}$$

WHERE N_T IS THE DENSITY OF SURFACE STATES PER CM^3 PER EV.

THE SPECTRAL INTENSITY OF THE TRAPPED HOLE DENSITY FLUCTUATION MUST BE EVALUATED OVER A LENGTH ℓ FROM THE $Si-SiO_2$ INTERFACE AND OVER ALL POSSIBLE ENERGY LEVELS AND IS GIVEN BY[16]

$$S_{p_T}(\omega) = \int_{-\infty}^{+\infty}\int_{0}^{\ell} \frac{4\,\text{VAR}\,p_T \cdot A\tau}{1+(\omega\tau)^2}\,dx\,dE \qquad \text{B-8}$$

AFTER SUBSTITUTING FOR $\text{VAR}\,p_T$ AND τ, AND AFTER EVALUATING THE DOUBLE INTEGRAL, THE SPECTRAL INTENSITY OF THE TRAPPED HOLE DENSITY FLUCTUATION MAY BE EXPRESSED IN THE FORM[17]

$$S_{p_T}(\omega) = \frac{4kTAN_T(E)}{a\omega}\left[\tan^{-1}\omega\tau_s\, e^{a\ell} - \tan^{-1}\omega\tau_s\right] \qquad \text{B-9}$$

WHERE $N_T(E)$ IS THE COMBINED DENSITY OF FREE HOLES AND ELECTRONS IN CM^{-3}/EV AND WHERE τ_s IS THE TIME CONSTANT OF THE SURFACE STATES LOCATED RIGHT AT THE OXIDE-SEMICONDUCTOR INTERFACE.

THE FLOW OF MOBILE CHARGE IN THE CHANNEL IS DEPENDENT ON THE TRANSCONDUCTANCE, GM, THE OXIDE CAPACITANCE PER UNIT AREA, C_O, AND ON THE EFFECTIVE AREA OF THE GATE, A, AND IS GIVEN BY[18]

$$\left[\frac{q G_M}{A C_O}\right] = \left[\frac{(\text{COUL.})(\text{COUL.}^2/\text{JOULE}\cdot\text{SEC.})}{(\text{CM}^2)(\text{COUL.}^2/\text{JOULE}\cdot\text{CM}^2)}\right]$$

$$= \left[\frac{(\text{COUL.}^3/\text{JOULE}\cdot\text{SEC.})}{(\text{COUL.}^2/\text{JOULE})}\right] = \frac{\text{COUL.}}{\text{SEC.}} \qquad \text{B-10}$$

WHICH IS IN UNITS OF CURRENT.

CHARGE DENSITY FLUCTUATION CAUSING A VARIATION IN THE SURFACE POTENTIAL RESULTS IN DRAIN CURRENT FLUCTUATIONS IN THE DRAIN CIRCUIT. THESE MAY BE OBSERVED AS NOISE. THEREFORE, THE SPECTRAL INTENSITY OF THE SHORT-CIRCUIT DRAIN CURRENT FLUCTUATIONS MAY BE EXPRESSED AS[19]

$$S_{i(\omega)} = \left[\frac{q G_M}{A C_O}\right]^2 \cdot S_{\rho_T(\omega)} = \overline{i_{df}^2} \qquad \text{B-11}$$

WHERE $\overline{i_{df}^2}$ IS THE MEAN-SQUARED CURRENT FLUCTUATION.

THE NATURE OF THE FREQUENCY DEPENDENCE OF THE NOISE SPECTRAL INTENSITY IS DETERMINED BY EVALUATING THE EXPANSION OF THE ARCTANGENT TERMS IN EQUATION B-9.

CASE 1. VERY LOW FREQUENCY: $\omega\tau_s e^{\alpha\ell} < 1$. AFTER SUBSTITUTING FOR $\hbar$, m^*, $E_B = 4\text{eV}$, $\ell \simeq 20\text{Å}$, AND SOLVING FOR IN EQUATION B-3, $e^{\alpha\ell} \simeq 10^{17}$. THEN, IF $\omega\tau_s e^{\alpha\ell}$ IS ASSUMED TO BE LESS THAN UNITY, $(\omega\tau_s e^{\alpha\ell})^2 \ll 1$. THE APPROPRIATE EXPANSION FOR THE ARCTANGENT TERMS IN EQUATION B-9 WHEN $x^2 < 1$ (WHERE $x = \omega\tau_s e^{\alpha\ell}$), IS GIVEN BY[20]

$$\tan^{-1}(x) = x - \frac{x^3}{3} + \frac{x^5}{5} - \frac{x^7}{7} + \ldots - \ldots \qquad \text{B-12}$$

SUBSTITUTING FOR x IN EQUATION B-12 GIVES THE FOLLOWING PARTIAL SERIES EXPANSION FOR THE BRACKETED TERM IN EQUATION B-9:

$$\left[\omega\tau_s e^{\alpha\ell} - \frac{(\omega\tau_s e^{\alpha\ell})^3}{3} + \ldots\right] - \left[\omega\tau_s - \frac{(\omega\tau_s)^3}{3} + \ldots\right] \qquad \text{B-13}$$

AFTER NEGLECTING THE SMALL TERMS, THE SPECTRAL INTENSITY OF THE SHORT-CIRCUIT DRAIN CURRENT FLUCTUATIONS AT LOW FREQUENCIES IS GIVEN BY[21]

$$S_{i(\omega)} \doteq \left[\frac{g_{GM}}{AC_O}\right]^2 \cdot \frac{4kTAN_T(E)\tau_s}{\alpha}(e^{\alpha\ell} - 1) \qquad \text{B-14}$$

IN WHICH IT IS EVIDENT THAT VERY LOW FREQUENCY NOISE IS WITHOUT FREQUENCY DEPENDENCE AND IS PROBABLY WHITE. THIS IS IN EXCELLENT AGREEMENT WITH OTHER NOISE THEORIES.[22,23] FURTHERMORE, SINCE $\tau_s \simeq 10^{-9}$ SECOND, IT IS APPARENT THAT THE FLAT NOISE SPECTRUM BEGINS AT $f < 10^{-9}\text{Hz}$. SINCE THIS IS FAR LOWER THAN IT IS POSSIBLE TO MEASURE, THE LOWER LIMIT OF FREQUENCY-DEPENDENT NOISE WILL NO DOUBT REMAIN A PURELY THEORETICAL LIMIT.

CASE 2. INTERMEDIATE FREQUENCY: $\omega\tau_s < 1 < \omega\tau_s e^{a\ell}$.

THE EXPANSION FOR $\tan^{-1}(x)$ WHEN $x > 1$ (WHERE $x = \omega\tau_s e^{a\ell}$) IS GIVEN BY[24]

$$\tan^{-1}(x) = \frac{\pi}{2} - \frac{1}{x} + \frac{1}{3x^3} - \frac{1}{5x^5} + \cdots - \cdots \qquad \text{B-15}$$

WITH $e^{a\ell} = 10^{17}$, $\omega\tau_s$ REMAINS MUCH LESS THAN UNITY. THEREFORE, SUBSTITUTING $\omega\tau_s e^{a\ell}$ FOR X IN EQUATION B-15 AND $\omega\tau_s$ FOR X IN EQUATION B-12 GIVES THE FOLLOWING PARTIAL SERIES EXPANSION FOR THE ARCTANGENT TERMS IN EQUATION B-9:

$$\left[\frac{\pi}{2} - \frac{1}{\omega\tau_s e^{a\ell}} + \cdots\right] - \left[\omega\tau_s - \frac{(\omega\tau_s)^3}{3} + \cdots\right] \qquad \text{B-16}$$

AFTER NEGLECTING THE SMALL TERMS, THE SPECTRAL INTENSITY OF THE SHORT-CIRCUIT DRAIN CURRENT FLUCTUATIONS AT INTERMEDIATE FREQUENCIES IS GIVEN BY[25]

$$S_{i(\omega)} \doteq \left[\frac{qG_M}{AC_O}\right]^2 \cdot \frac{kT\text{AN}_T(E)}{\alpha f} \qquad \text{B-17}$$

WHICH IS INVERSELY PROPORTIONAL TO FREQUENCY. WITH $\tau_s \simeq 10^{-9}$ SECOND, THE FULL RANGE OF "1/F" NOISE IS WITHIN $10^{-9} < f < 10^{8}$. MEASUREMENTS MADE AT TEN CYCLES AND AT ONE KILOCYCLES WERE THEREFORE WELL WITHIN THE ACCEPTED RANGE OF FREQUENCIES. AS FOR EQUATION B-14, THE NOISE INTENSITY IS DIRECTLY PROPORTIONAL TO THE SURFACE-STATE DENSITY. THIS FACT HAS BEEN USED TO CORRELATE SATURATION DRAIN CONDUCTANCE WITH 1/F NOISE INTENSITY IN THIS RESEARCH.

CASE 3. HIGH FREQUENCY: $\omega\tau_s > 1$. USING THE EXPRESSION OF EQUATION B-15 FOR BOTH $\omega\tau_s e^{\alpha\ell}$ AND $\omega\tau_s$ GIVES THE FOLLOWING PARTIAL SERIES EXPANSION FOR THE ARCTANGENT TERMS IN EQUATION B-9:

$$\left[\frac{\pi}{2} - \frac{1}{\omega\tau_s e^{\alpha\ell}} + \cdots - \cdots\right] - \left[\frac{\pi}{2} - \frac{1}{\omega\tau_s} + \cdots - \cdots\right] \qquad \text{B-18}$$

FROM WHICH THE SPECTRAL INTENSITY OF THE SHORT-CIRCUIT DRAIN CURRENT FLUCTUATIONS AT HIGH FREQUENCIES MAY BE GIVEN BY[26]

$$S_{i(\omega)} \doteq \left[\frac{g_G M}{AC_O}\right]^2 \cdot \frac{4kTAN_T(E)}{\alpha\omega^2\tau_s}(1 - e^{-\alpha\ell}) \qquad \text{B-19}$$

HIGH FREQUENCY NOISE IS THEREFORE EXPECTED TO BE INVERSELY PROPORTIONAL TO THE SQUARE OF THE FREQUENCY AT WHICH IT IS MEASURED AND, AS WITH THE NOISE INTENSITY AT INTERMEDIATE AND LOW FREQUENCIES, IS DIRECTLY PROPORTIONAL TO THE SURFACE-STATE DENSITY.

REFERENCES

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[17]Ibid., p. 1453.

[18]Op. Cit., Hsu, "P-N Junctions," p. 848.

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[24] Op. Cit., Tables, p. 433.

[25] Op. Cit., Hsu, "MOS Transistors," p. 1453.

[26] Ibid., p. 1453.

APPENDIX C

THRESHOLD VOLTAGE DRIFT

IN P-CHANNEL ENHANCEMENT MOSFETS

SPECIFICATIONS

	DD07P	DD08K
LOW NOISE UNITS	56 57 77 79 80	103 109 110 112 121
HIGH NOISE UNITS	45 47 48 60 61	102 104 105 114 120
RATED V_{GS} GATE-TO-SOURCE	-30V. ZENER DIODE PROTECTED	±70V. NO GATE PROTECTION
APPLIED V_{GS} GATE-TO-SOURCE DRAIN, SOURCE, AND SUBSTRATE SHORTED	-25V.	-50V.
OVEN TEMPERATURE	130±5°C	130±5°C
TIME DURATION	500 HOURS	500 HOURS

CONNECTION DIAGRAM

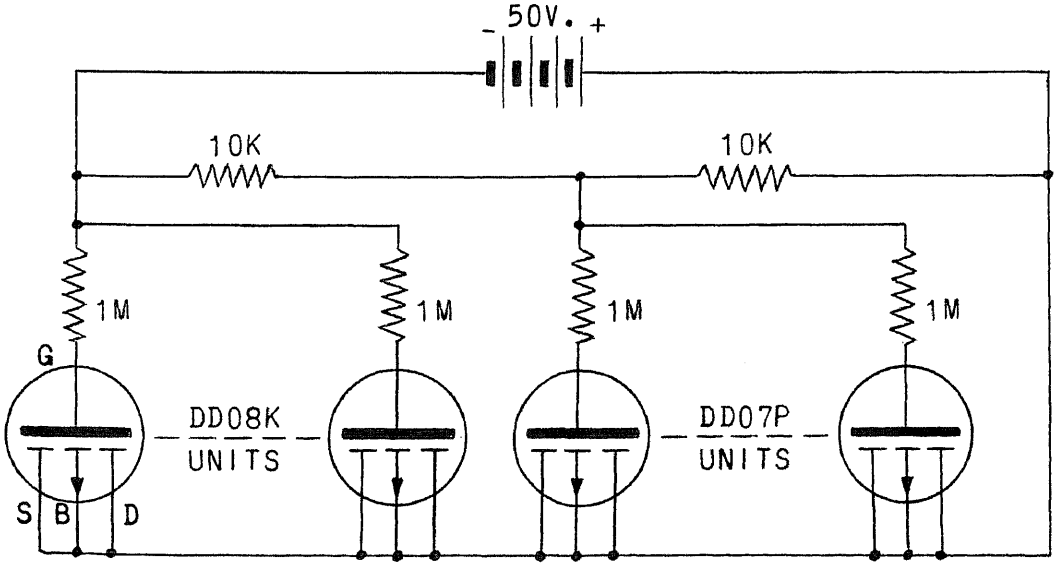

FIGURE C-1. CONNECTION DIAGRAM FOR BIASING P-CHANNEL MOS TRANSISTORS FOR NEGATIVE THRESHOLD VOLTAGE DRIFT.

Life-Test Data For DD07P

$-V_{T1}$ Threshold voltage as of 6/25/73

$-V_{T2}$ Threshold voltage as of 7/17/73

UNIT NO.	$-V_{T1}$ VOLTS	$-V_{T2}$ VOLTS	$\%\Delta V_T$
56	4.60	4.72	2.61
57	4.51	4.63	2.66
77	4.49	4.59	2.23
79	4.56	4.64	1.75
80	4.70	4.81	2.34
45	4.52	4.76	5.32
47	4.58	*	*
48	4.44	4.58	3.16
60	4.87	5.20	6.78
61	4.62	4.95	7.15

* Unit failed during bias at elevated temperature

Interpretation of Data

Mean $-V_{T1}$ = 4.59V. Standard deviation = 0.037V.

Mean $-V_{T2}$ = 4.63V. Standard deviation = 0.196V.

Absolute difference between means: 0.04V.

Standard error of the difference between means: 0.0887V.

Since the absolute difference between means is less than the standard error of the difference between means, it can be concluded that there was no significant change in threshold voltage for type DD07P MOSFET's after bias at 130±5°C for 500 hours.

Life-Test Data For DD08K

$-V_{T1}$ Threshold voltage as of 6/25/73

$-V_{T2}$ Threshold voltage as of 7/17/73

UNIT NO.	$-V_{T1}$ VOLTS	$-V_{T2}$ VOLTS	$\%\Delta V_T$
103	4.27	4.59	7.50
109	4.17	4.55	9.11
110	4.19	*	*
112	4.21	4.50	6.88
121	4.31	4.61	6.95
102	4.11	*	*
104	3.82	4.26	11.5
105	4.16	4.66	12.0
114	4.15	5.13	23.6
120	4.17	4.76	14.1

* Unit failed during bias at elevated temperature

Interpretation of Data

Mean $-V_{T1}$ = 4.16V. Standard deviation = 0.044V.

Mean $-V_{T2}$ = 4.62V. Standard deviation = 0.073V.

Absolute difference between means: 0.46V.

Standard error of the difference between means: 0.0945V.

Since three times the standard error of the difference between means is less than the absolute difference between means, the population after threshold voltage drift has less than 0.27% chance of being part of the original population. Therefore, it can be concluded that the type DD08K MOSFET's showed substantial negative threshold voltage drift after bias at 130±5°C for 500 hours.

APPENDIX D

EXCESS NOISE-DRAIN CURRENT MEASUREMENTS AT CONSTANT GATE VOLTAGE

SPECIFICATIONS

	DD07P	DD08K
LOW NOISE UNITS	56 57 77 79 80	103 109 110 112 121
HIGH NOISE UNITS	45 47 48 60 61	102 104 105 114 120
RATED V_{GS} GATE-TO-SOURCE	-30V. ZENER DIODE PROTECTED	±70V. NO GATE PROTECTION
APPLIED V_{GS} GATE-TO-SOURCE	-5.5V.	-5.5V.
RATED I_{DS} DRAIN-TO-SOURCE $V_{GS} = V_{DS} = -15V.$	-44.0MA	-44.0MA
MAX. APPLIED I_{DS} $V_{GS} = -5.5V.$ V_{DS} VARIABLE $V_{SSUB} = 0V.$	-8.0MA	-8.0MA
RATED DISSIPATION $T_A = 25°C$	225MW	225MW
AMBIENT TEMPERATURE	25±5°C	25±5°C
INSTANTANEOUS g_{dsAT} AT DRAIN BREAKDOWN	100 MHOS	100 MHOS

CONNECTION DIAGRAM

REFER TO FIGURE 3-1 ON PAGE 42 OF TEXT.

EXCESS NOISE-DRAIN CURRENT DATA FOR DD07P MOSFETS (6/25/73)

NOISE VOLTAGE IN μVOLTS AT INDICATED DRAIN CURRENTS AND SPECIFIED FREQUENCIES

	0.5mA			1.0mA			1.5mA		
UNIT NO.	10Hz	1KHz	$-V_{DS}$	10Hz	1KHz	$-V_{DS}$	10Hz	1KHz	$-V_{DS}$
45	44	5.7	15.5	69	8.2	24.0	100	10	30.0
47	42	5.4	13.0	63	8.2	23.5	79	11	30.5
48	35	5.5	6.5	66	8.5	14.0	76	9.8	21.0
60	72	7.2	19.5	110	11	26.0	120	12	29.0
61	47	6.0	13.5	76	8.2	20.5	92	9.2	25.0
56	28	6.6	39.0	47	10	58.0	60	11	68.5
57	31	6.3	36.5	49	9.5	60.0	66	12	70.5
77	31	6.0	22.5	51	9.8	44.5	77	12	54.0
79	28	6.3	34.0	44	8.7	57.0	52	12	69.5
80	31	6.6	44.0	47	9.5	64.5	50	11	72.0

	2.0mA			3.0mA			4.0mA		
45	130	14	35.0	140	17	41.5	110	16	49.0
47	110	13	36.0	130	16	43.0	80	15	56.0
48	110	13	26.5	130	17	33.0	110	17	40.0
60	130	14	33.5	140	18	36.0	130	17	42.5
61	120	13	29.0	125	14	33.0	120	16	43.0
56	70	11	70.0	60	10	75.5	50	9	80.0
57	60	12	71.0	62	11	78.0	45	10	83.5
77	62	11	65.0	55	10	74.5	43	9	78.0
79	73	13	76.5	60	10	80.0	47	8	83.0
80	60	12	77.0	54	10	81.0	39	8	82.0

	6.0mA			8.0mA		
45	100	15	53.0	88	14	60.5
47	70	13	58.0	50	12	63.0
48	100	16	46.0	80	14	54.5
60	100	16	46.5	79	15	51.5
61	95	15	52.0	81	14	57.0
56	17	4.2	83.5			
57	13	2.8	87.0			
77	13	3.4	80.5			
79	12	3.5	84.0			
80	11	2.6	84.0			

EXCESS NOISE-DRAIN CURRENT DATA FOR DD07P MOSFETS (7/17/73)

NOISE VOLTAGE IN μVOLTS AT INDICATED DRAIN CURRENTS AND SPECIFIED FREQUENCIES

	0.5mA			1.0mA			1.5mA		
UNIT NO.	10Hz	1KHz	$-V_{DS}$	10Hz	1KHz	$-V_{DS}$	10Hz	1KHz	$-V_{DS}$
45	90	45	22.5	145	90	32.0	180	110	36.0
47	*UNIT FAILED AFTER BIAS AT 130±5°C FOR 500 HOURS								
48	60	50	7.0	140	110	18.5	180	140	26.0
60	100	80	23.0	170	130	29.0	200	140	31.0
61	60	50	16.0	100	80	24.5	120	90	30.0
56	80	60	39.5	130	100	59.0	180	140	69.0
57	80	60	38.0	120	100	68.0	160	130	73.5
77	60	45	23.5	140	110	45.0	180	140	57.0
79	60	45	36.0	140	100	61.5	180	130	71.0
80	80	60	47.0	140	110	68.0	190	160	75.0

	2.0mA			3.0mA			4.0mA		
45	210	120	39.0	220	130	44.5	225	145	49.5
47	*	*	*	*	*	*	*	*	*
48	210	160	30.0	250	180	37.0	270	200	40.0
60	210	160	34.0	225	170	38.0	230	185	42.0
61	130	100	33.0	140	110	38.0	130	100	44.0
56	210	160	73.0	230	190	78.5	140	110	81.5
57	200	160	76.5	210	170	79.0	90	80	83.0
77	210	150	65.0	240	180	74.0	200	100	77.0
79	200	160	76.5	230	180	80.0	130	90	82.0
80	210	150	78.0	200	150	80.0	110	100	81.5

	6.0mA			8.0mA		
45	205	100	54.0	190	90	63.0
47	*	*	*	*	*	*
48	240	170	46.5	200	140	55.0
60	240	190	46.0	200	110	50.5
61	120	90	51.0	90	70	59.0
56	32	16	82.0			
57	24	15	84.0			
77	26	19	79.0			
79	22	18	83.0			
80	32	17	83.5			

EXCESS NOISE-DRAIN CURRENT DATA FOR DD08K MOSFETS (6/25/73)

NOISE VOLTAGE IN μVOLTS AT INDICATED DRAIN CURRENTS AND SPECIFIED FREQUENCIES

	0.5mA			1.0mA			1.5mA		
UNIT NO.	10Hz	1KHz	$-V_{DS}$	10Hz	1KHz	$-V_{DS}$	10Hz	1KHz	$-V_{DS}$
102	55	6.4	0.60	75	14	23.0	110	17	43.0
104	30	5.2	1.00	56	6.8	14.5	71	11	27.0
105	50	4.8	5.00	71	9.5	28.0	82	13	46.5
114	36	4.4	7.50	60	9.3	64.0	64	12	69.0
120	55	4.7	18.0	80	9.3	62.0	110	12	73.0
103	50	5.3	25.0	72	11	57.0	83	12	72.5
109	55	5.5	9.50	80	11	21.0	98	12	30.0
110	55	5.3	20.0	76	10	38.5	92	12	55.5
112	45	5.0	8.00	68	10	24.0	90	13	38.0
121	40	5.2	16.5	67	10	48.5	87	11	64.5

	2.0mA			3.0mA			4.0mA		
102	130	20	56.0	150	25	65.0	155	24	69.0
104	110	12	30.5	130	15	46.5	145	16	58.0
105	120	17	58.0	140	19	70.0	150	18	73.0
114	100	18	74.5	145	22	76.0	160	21	77.0
120	125	16	75.0	135	17	77.5	130	16	79.0
103	76	12	74.5	49	10	77.0	36	8.2	77.5
109	84	13	38.0	34	11	50.0	22	9.3	57.0
110	110	10	69.0	78	7.9	76.0	60	6.2	77.0
112	100	12	47.0	60	7.1	61.0	30	4.2	70.5
121	95	13	72.0	50	12	77.0	33	10	79.0

	6.0mA			8.0mA		
102	145	20	75.0	110	17	77.5
104	140	15	70.0	105	14	73.0
105	140	16	75.0	100	13	76.0
114	155	18	78.5	110	16	79.0
120	120	13	79.5	90	11	80.0
103	32	4.7	78.0	43	6.8	78.5
109	15	5.1	65.0	32	7.2	69.0
110	40	4.3	78.5	50	5.8	79.5
112	14	3.9	76.0	27	5.0	76.5
121	12	8.1	80.0	29	8.5	80.0

EXCESS NOISE-DRAIN CURRENT DATA FOR DD08K MOSFETS (7/17/73)

NOISE VOLTAGE IN μVOLTS AT INDICATED DRAIN CURRENTS AND SPECIFIED FREQUENCIES

	0.5MA			1.0MA			1.5MA		
UNIT NO.	10Hz	1KHz	$-V_{DS}$	10Hz	1KHz	$-V_{DS}$	10Hz	1KHz	$-V_{DS}$
102	*UNIT FAILED AFTER BIAS AT 130±5°C FOR 500 HOURS								
104	100	80	5.50	160	130	18.5	210	170	29.5
105	110	100	13.0	200	160	38.0	240	200	51.0
114	130	110	10.5	220	170	66.0	250	190	71.5
120	120	90	34.0	180	110	71.0	220	140	76.0
103	100	90	27.5	180	130	60.0	200	150	72.0
109	100	90	11.0	160	110	22.5	210	150	30.0
110	100	80	23.0	180	160	35.0	220	180	49.0
112	90	55	9.00	170	100	26.0	190	180	38.5
121	100	60	19.0	160	110	50.0	180	140	66.0

	2.0MA			3.0MA			4.0MA		
102	*	*	*	*	*	*	*	*	*
104	250	200	32.0	300	230	46.0	290	200	57.0
105	270	210	60.5	310	240	70.5	270	230	74.0
114	300	220	78.0	320	230	79.5	280	200	78.0
120	270	200	78.0	240	160	78.5	170	100	79.0
103	180	120	75.0	110	80	77.0	78	55	78.0
109	200	130	39.0	110	75	49.0	41	24	57.5
110	**UNIT DEFECTIVE AT HIGHER DRAIN CURRENTS								
112	210	160	46.5	170	100	61.5	90	60	70.0
121	120	90	73.0	100	70	78.0	76	45	79.5

	6.0MA			8.0MA		
102	*	*	*	*	*	*
104	250	190	71.0	170	140	75.0
105	200	180	76.0	120	80	77.0
114	210	110	79.0	90	50	79.5
120	140	90	79.5	89	65	80.5
103	48	18	80.0	34	12	80.5
109	30	20	69.0	17	16	72.0
110	**	**	**	**	**	**
112	21	19	75.0	18	12	76.0
121	32	22	80.0	22	12	80.5

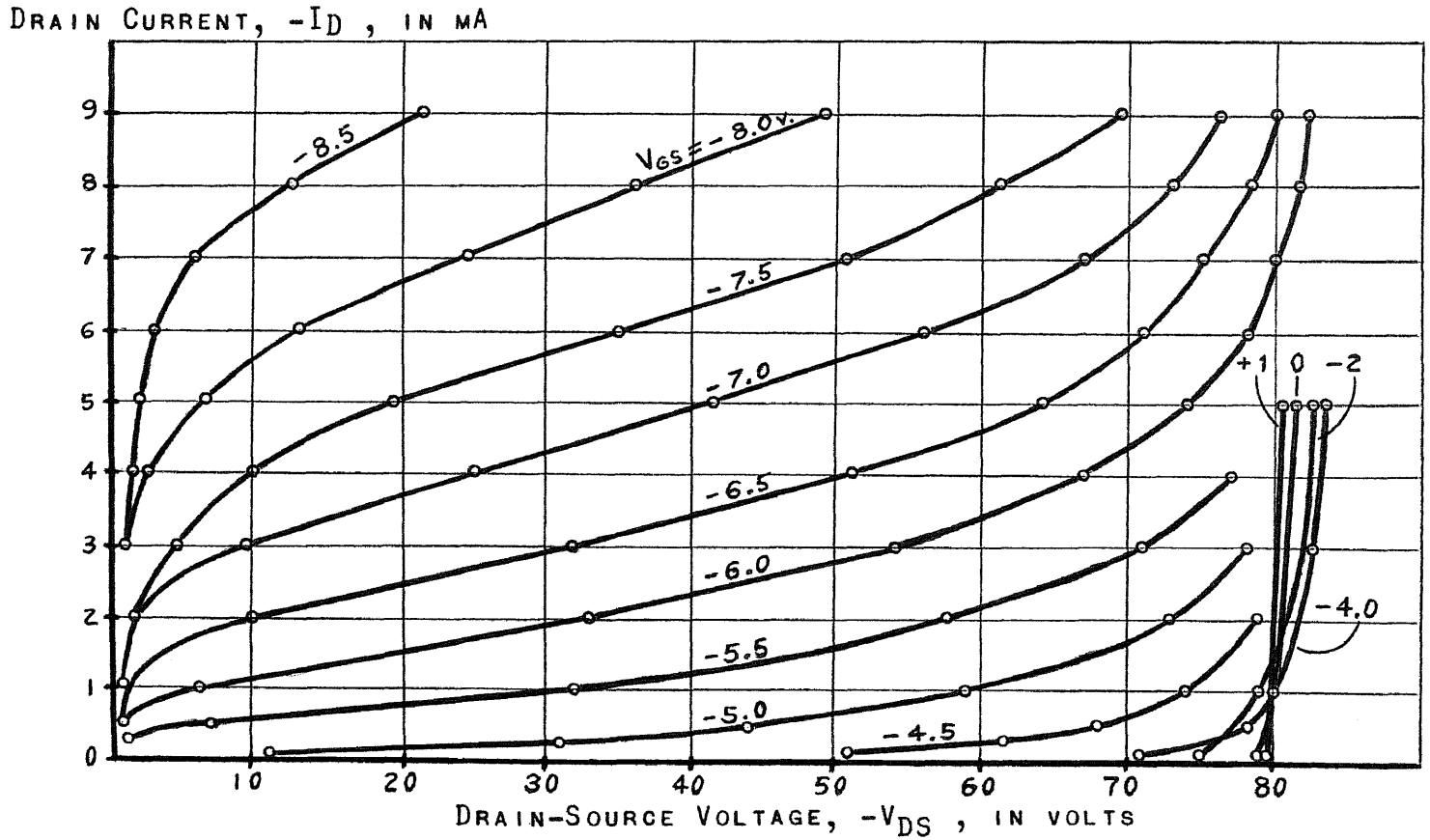

FIGURE D-1. CURRENT-VOLTAGE CHARACTERISTICS FOR A RELATIVELY LOW NOISE DD07P MOSFET DRAIN-DIODE BREAKDOWN IS EVIDENT WHEN THE DEVICE IS BIASED IN CUTOFF. UNIT NO. 44.

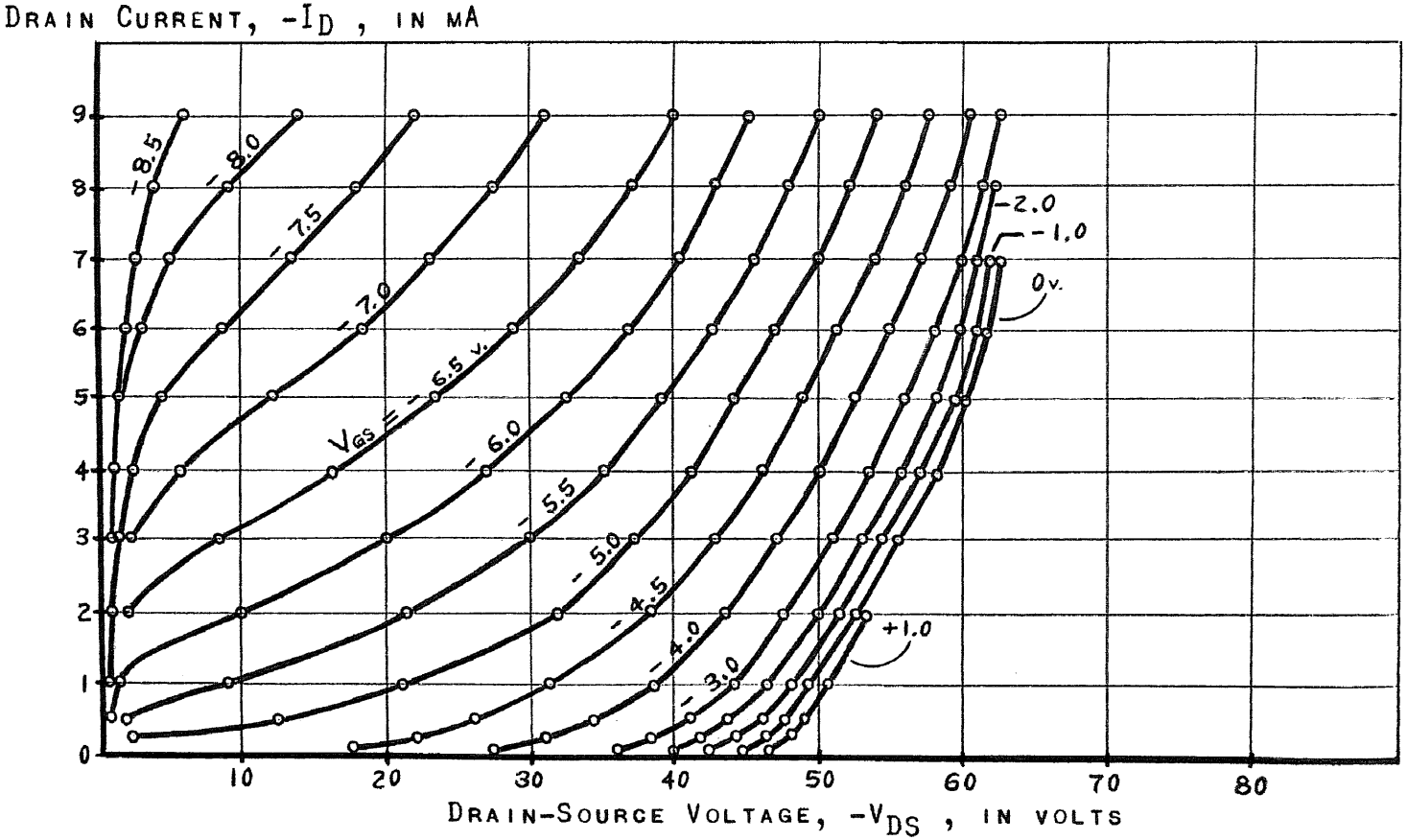

FIGURE D-2. CURRENT-VOLTAGE CHARACTERISTICS FOR A RELATIVELY HIGH NOISE DD07P MOSFET HIGH SATURATION DRAIN CONDUCTANCE AND EVIDENCE OF DRAIN PUNCH-THROUGH WERE TYPICAL OF SUCH HIGH NOISE TRANSISTORS. UNIT NO. 69.

APPENDIX E

DRAIN LEAKAGE CURRENT MEASUREMENTS

Definition of I_{DSS}

The short-circuit drain leakage current, I_{DSS}, of p-channel enhancement MOSFET's is defined at $V_{DS} = -10$ volts and $V_{GS} = V_{SSUB} = 0$ volts. It is a measure of the leakage around the entire drain-to-substrate p-n junction and is usually no more than a few nanoamperes (10^{-9} amperes) in most enhancement-mode devices.

Experimental Method

In order to assess the possible effects of drain leakage on the saturation I-V characteristics of p-channel enhancement MOSFET's and in order to correlate this leakage with changes in the surface-state density and other characteristics of the $Si-SiO_2$ interface, measurements of I_{DSS} were conducted on all units life-tested for threshold voltage drift, both before and after bias at 130±5°C for 500 hours.

Figure E-1 shows a simplified schematic of the General Radio Type 1230-A DC Amplifier and Electrometer which was used to measure I_{DSS} for the units tested. The instrument consisted of variable resistors R_A (adjustable from 10^4 to 10^{11} ohms in eight orders of magnitude) and R_B (preset for voltage measurements) and electrometer tube V_1 connected as

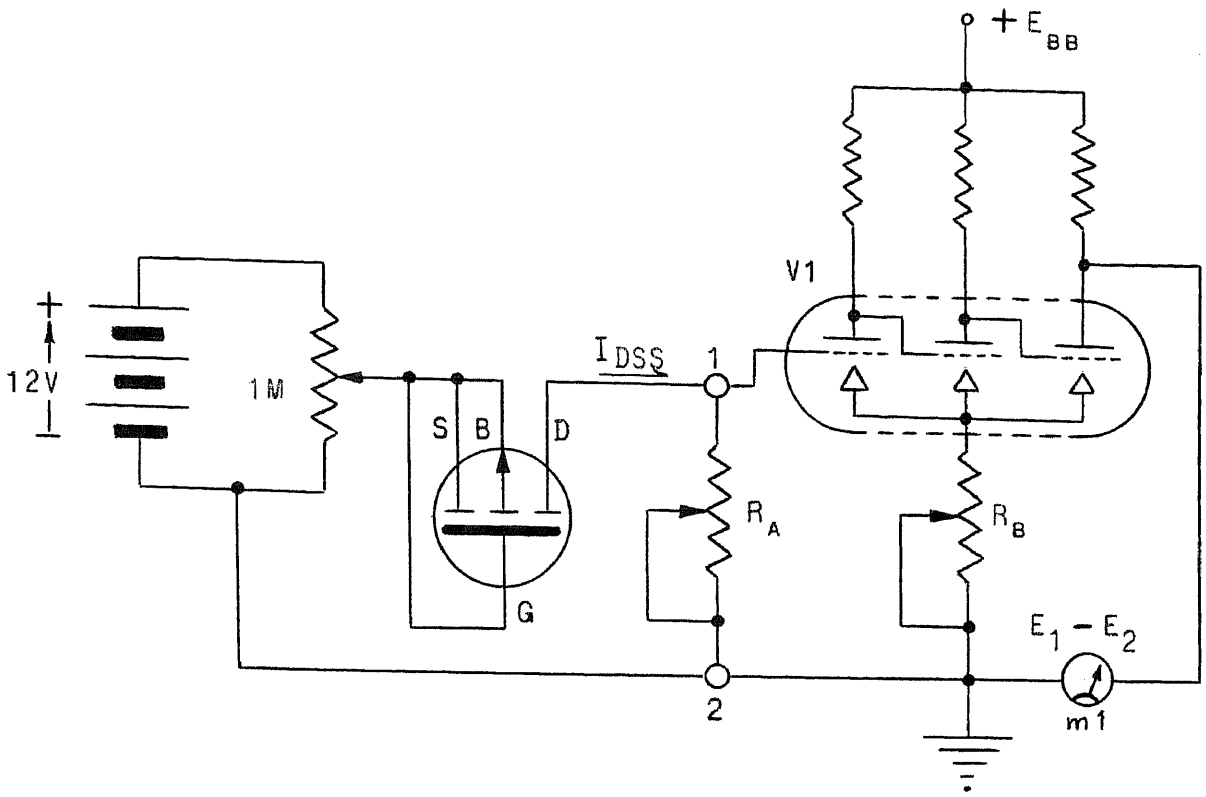

FIGURE E-1. SIMPLIFIED SCHEMATIC OF A GENERAL RADIO TYPE 1230-A DC AMPLIFIER AND ELECTROMETER AND EXTERNAL DC SUPPLY USED TO MEASURE I_{DSS} OF P-CHANNEL ENHANCEMENT MOSFET'S. TUBE V1 WAS CONNECTED AS A THREE-STAGE, DIRECT-COUPLED, VOLTAGE AMPLIFIER WHICH, DUE TO THE COMMON-CATHODE CONFIGURATION, PROVIDED AN INPUT RESISTANCE GREATER THAN 10^{14} OHMS AND WHICH DROVE METER M1. DUE TO THE EXTREMELY HIGH TRANSCONDUCTANCE OF THE ELECTROMETER AMPLIFIER, VOLTAGE VARIATIONS ACROSS R_A (ADJUSTABLE BETWEEN 10^4 AND $10^{11}\Omega$) PRODUCED ESSENTIALLY IDENTICAL VARIATIONS ACROSS R_B. THE LEAKAGE CURRENT PRODUCED A POTENTIAL DROP ACROSS TERMINALS 1 AND 2 AND WAS FOUND TO BE $(E_1-E_2)/R_A$.

A THREE-STAGE, DIRECT-COUPLED, CATHODE-FOLLOWER WHICH DROVE A 1MA METER AND WHICH PROVIDED AN INPUT RESISTANCE GREATER THAN 10^{14} OHMS (OPEN-GRID). TUBE V_1 WAS TREATED WITH GENERAL ELECTRIC DRI-FILM SC-87 AND ALL INSULATION WAS TEFLON FOR LOW LEAKAGE. A SPECIAL SHIELDED ENCLOSURE WAS USED TO COVER THE TEST JIG AND ALL MEASUREMENTS WERE CONDUCTED WITHIN A SHIELDED ROOM AT A TEMPERATURE OF 25±5°C WITH NOT MORE THAN 30% HUMIDITY.

TWO SIX-VOLT NICKEL-CADMIUM BATTERIES AND A POTENTIOMETER WERE USED TO PROVIDE THE PROPER DRAIN BIAS. THE MOSFET UNDER TEST WAS CONNECTED WITH GATE, SOURCE AND SUBSTRATE TO THE WIPER-ARM OF THE POTENTIOMETER AND WITH THE DRAIN TO THE TERMINAL 1 VOLTAGE INPUT OF THE METER.

WHEN MEASURING I_{DSS}, THE LEAKAGE CURRENT WHICH FLOWS DEVELOPES A VOLTAGE ACROSS INPUT RESISTANCE R_A. SINCE THE OVERALL TRANSCONDUCTANCE OF THE ELECTROMETER AMPLIFIER WAS SO GREAT, ANY VOLTAGE CHANGE ACROSS CATHODE RESISTANCE R_B WAS ESSENTIALLY THE SAME AS THAT ACROSS R_A AND WAS READ DIRECTLY ON THE METER. THE UNKNOWN LEAKAGE CURRENT WAS THEN FOUND FROM $(E_1 - E_2)/R_A$, WHERE R_A WAS ADJUSTED TO PROVIDE A LARGE DEFLECTION ON THE 100MV SCALE OF METER M_1.

DRAIN LEAKAGE CURRENT (I_{DSS}) MEASUREMENTS FOR TEN TYPE DD07P AND TEN TYPE DD08K MOSFET'S IS LISTED ON THE FOLLOWING PAGES.

Drain Leakage Data For DD07P MOSFET's

I_{DSS1} Drain leakage current as of 6/25/73

I_{DSS2} Drain leakage current as of 7/17/73

UNIT NO.	I_{DSS1} pA	I_{DSS2} pA	
56	1000	4000	
57	1000	4200	
77	1100	4300	Relatively low noise transistors
79	1000	4300	
80	900	4100	
45	1100	3900	
47	1600	4300	
48	1000	4000	Relatively high noise transistors
60	1200	4200	
61	1100	4100	

Drain Leakage Data For DD08K MOSFET's

I_{DSS1} Drain leakage current as of 6/25/73

I_{DSS2} Drain leakage current as of 7/17/73

UNIT NO.	I_{DSS1} pA	I_{DSS2} pA	
103	1200	4900	
109	1100	4800	
110	900	60 A*	Relatively low noise transistors
112	800	4600	
121	900	4700	
102	1100	.6 A*	
104	1600	4600	
105	1100	4500	Relatively high noise transisotrs
114	1600	4400	
120	1400	4900	

*Units 102 and 110 failed during bias at 130±5°C for 500 hours.

APPENDIX F

EQUIPMENT USED IN THIS RESEARCH

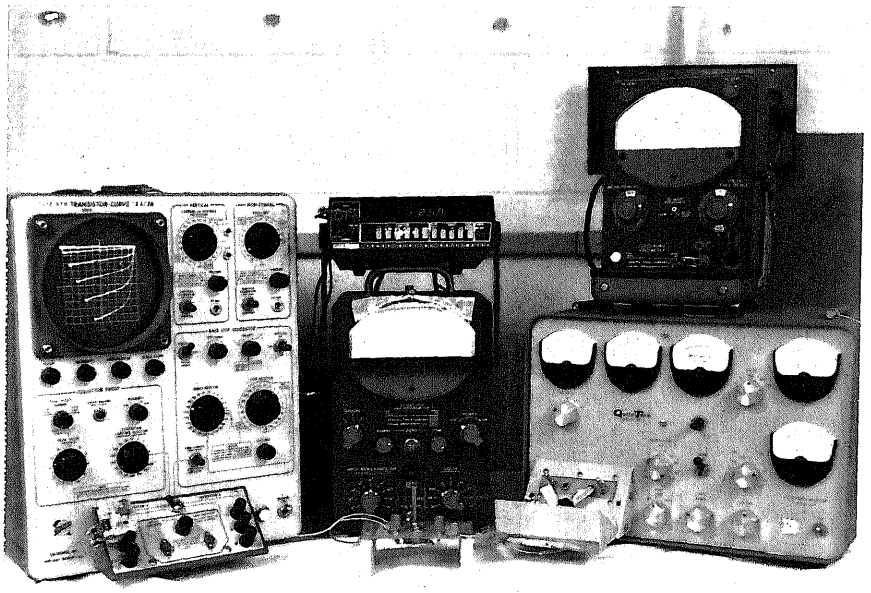

FIGURE F-1. PHOTOGRAPH SHOWING THE PRINCIPAL INSTRUMENTS USED IN THIS RESEARCH. AT CENTER ON TOP: DIGITAL MULTIMETER (FLUKE, MODEL 8000-A) AND ELECTRONIC VOLTMETER (GENERAL RADIO, TYPE 1808-A). LEFT TO RIGHT: TRANSISTOR CURVE TRACER (TETRONIX, TYPE 527 WITH ADAPTOR FOR P-CHANNEL MOS TRANSISTORS AND SHOWING TYPICAL CURRENT-VOLTAGE CHARACTERISTICS ON SCREEN); DC AMPLIFIER AND ELECTROMETER (GENERAL RADIO, TYPE 1230-A WITH SHIELDED ENCLOSURE AND TEST JIG NOT VISIBLE); AND DIODE NOISE ANALYZER (QUAN-TECH LABORATORIES, MODEL 327). FRONT, AT CENTER: VARIABLE BIAS POTENTIOMETER FOR GATE CIRCUIT.

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