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Correlation of 1/f noise with threshold drift in MOSFET's

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CORRELATION OF 1/f NOISE WITH THRESHOLD DRIFT IN MOSFET's

BY

JOHN PETER ROONEY

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CORRELATION OF 1/f NOISE WITH THRESHOLD DRIFT IN MOSFET's

BY

JOHN PETER ROONEY

FOR

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BY

FACULTY COMMITTEE

APPROVED: _____

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NEWARK, NEW JERSEY

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ABSTRACT

A brief review of the fundamentals of MOSFET's is given. A correlation between threshold drift and surface states is made, with a following correlation between surface states and 1/f noise. It therefore follows that MOSFET's with a high 1/f noise level will drift more than those with a low level of 1/f noise. Experiments were carried out to show this effect, but no clear cut conclusions can be drawn from the experimental work.

PREFACE

The first section of this paper deals with the construction and theory of operation of the MOSFET, the Metal-Oxide-Semiconductor Field-Effect Transistor.

After the first section, a review of the drift and failure mechanisms in MOSFET's is given. Emphasis is placed upon the drift in threshold voltage of the MOSFET. An explanation of the drift is given and a correlation between this drift and sodium ions is given.

Noise in MOSFET's is considered in the third section of this paper. A cause for 1/f noise is given in this section. Correlation between 1/f noise and drift mechanism is given in this section.

The fourth section is concerned with experimental procedures covered for this paper. Results are presented in this section for tests performed on the MEM-511, a P-channel MOSFET.

Finally, conclusions are drawn in section five.

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MOSFET FUNDAMENTALS

1.1 Construction

The technique of constructing a P-channel,enhancement mode MOSFET is described here for the arbitrary reason that the available sample devices are P-channel enhancement mode devices.

It is not the purpose of this section to go deeply and thoroughly into the construction of the MOSFET. Rather, it is the purpose of this section to emphasize those steps in the construction that are the source of the drift phenomenon.

Fabrication begins with the growth of a silicon ingot. The crystal is pulled from the molten silicon containing the substrate impurity (e.g. phosphorus) for an N-type substrate. Tests are made to determine the resistivity regions and the material is zone-cut to segregate the various resistivity regions.

Usually, the MOSFET substrate is made up of the four to five ohm-cm. region. Resistivity on this order permits inter-device isolation since the drain and source are heavily doped P-type material. The material is then cut into wafers approximately eight mils in thickness; this lower size limit is determined by handling problems.

The wafers are checked for crystal flaws in the silicon,as any substrate dislocation will result in improper oxide growth. The wafer is then lapped to achieve a high degree of flatness and polish. Other techniques used to obtain a nearly ideal surface are mostly proprietary and are not published.

An ideal surface is a surface obtained, in principle, by cutting a crystal in half while in a perfect vacuum. It is assumed that all the surface atoms are still at the exact positions they had before cleaving. Like all perfections, an ideal surface is impossible to achieve in practice.

If such an ideal surface is not achieved, then there will appear imperfections at the surface; such imperfections appear as localized electronic energy states. Because these states are localized at the surface, they are called surface states.

It will be shown in a later part of this paper that there is a correspondence between the number of surface states and the magnitude of 1/f noise and also that there is a dependence of the the drift mechanism and the surface states.

Continuing with the manufacturing process, a silicon dioxide layer is grown upon the chip. (See figure 1.1,a). It appears, as a matter of experience, that it is easier to grow silicon dioxide in the presence of water vapor than with dry oxygen alone. The chips are placed in an oven maintained at about $1200^{\circ}C$. Oxygen, bubbled through distilled water (to prevent sodium ion contamination) is passed over the surface of the chips. A measure of the purity of the water vapor introduced is its resistivity: about 22 Megohm-cm resistivity. The growth of thick oxide is allowed to continue to about 5000 to 8000 angstrom units* This oxide growth is called the masking oxide layer, since it acts as a mask, or shield, during the diffusion of the acceptor material into the drain and source areas.

The oxide is examined and measured optically to determine its uniformity of growth and thickness. Oxide thickness varies across the wafer in response to variations in the oven temperature. The protective oxide "passivates" the wafer.

* one angstrom unit $= 10^{-10}$ meters.

Figure 1.1,b, represents the beginning of the photolithographic process. The wafers are covered with a photoresist (KPR). The chips are then covered with the first of four masks. This step is represented schematically in fig.1.1,b, by the arrows,which represent exposure to ultraviolet light. Figures 1.1 and 1.2 are schematic, one dimensional portrayal of the process steps.

In photolothographic processes, proper precautions must be taken to prevent misalignment of the various masks. In order to prevent their expansion and contraction, the masks are cut and stored in a temperature controlled room. With the proper precautions, it is possible to achieve 0.0004 inch line widths and location accuracy of 0.0002 inch within a one square inch area.[1]

The chips are exposed to ultraviolet light through the mask. The mask consists of transparent and opaque areas in a predetermined pattern, which pass or stop, respectively, the ultraviolet light. The photoresist, a photosensitive emulsion, is then developed. Areas of the photoresist not exposed are removed by etching with a mixture of hydrofluoric acid and a buffer.

(1) Bower, .FH. & H.K. Dicken. "Photo Masks... The Tooling for ICs." Electronic Industries, Vol.25,No.6 (June,1966) p.41-48.

CONSTRUCTION PROCESS

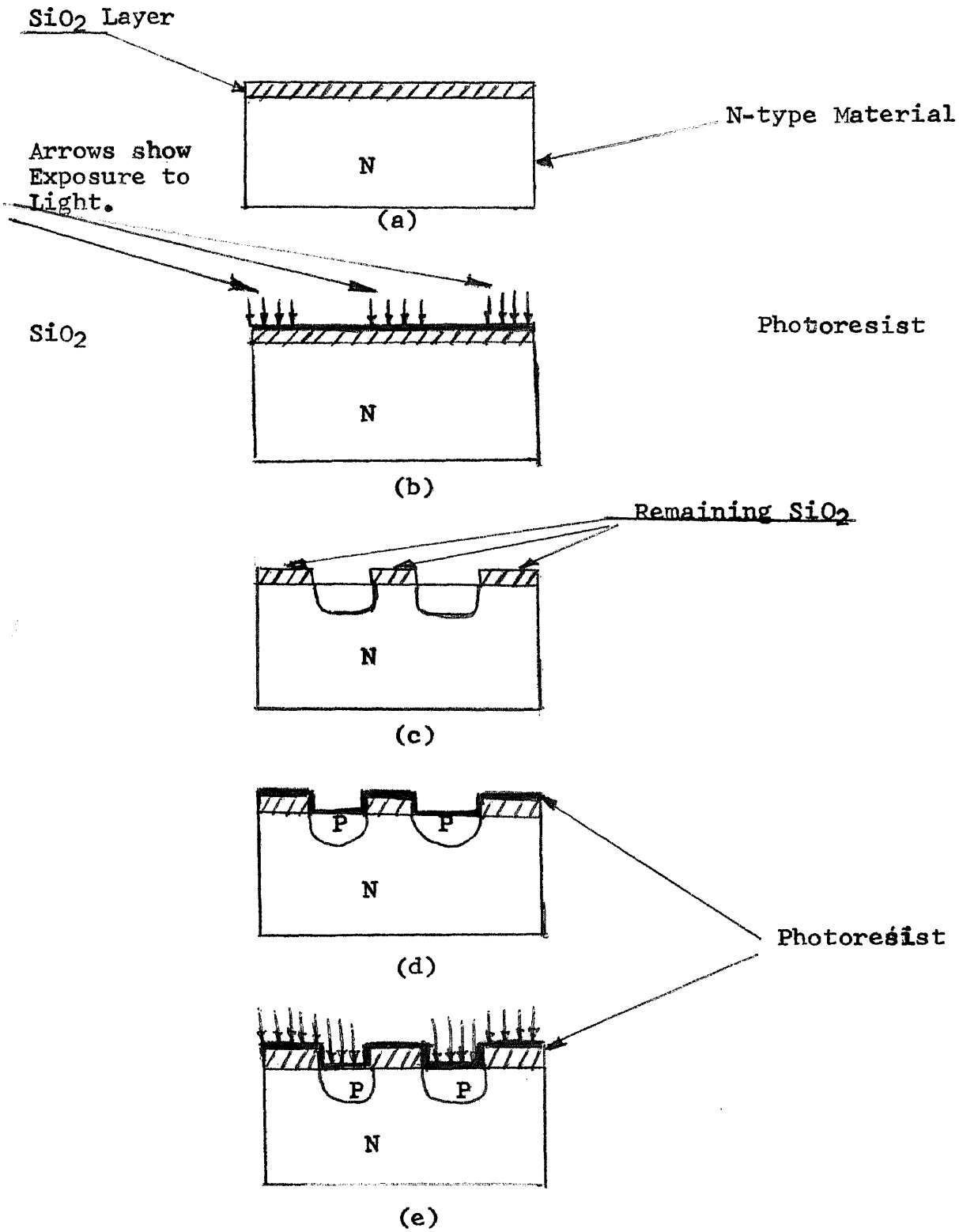


Figure 1.1

The photoresist areas that had been exposed are hardened and resist the etching, while the unexposed areas are easily etched. Etching continues down to the silicon substrate, forming windows through the oxide layer. These windows will allow the diffusion of P-type material into the wafer (fig. 1.1,c).

A typical technique for the diffusion of P-type material is to place the chip into a low temperature pre-deposition furnace. The dopant source is usually B_2O_3. Boron is deposited upon the exposed substrate surface, but is not diffused until the chip is placed in a driving furnace. This forms an abrupt junction. When the wafer is placed in the diffusion furnace, the boron is driven into the source and drain areas to a depth of several microns. The depth of diffusion is controlled by two factors: the temperature of the oven and the time spent at that temperature. This brings us up to fig. 1.1,d.

Step 1.1,d shows photoresist again applied to the chip. The chip is then exposed to ultraviolet light through the second mask. Again, the unexposed photoresist is etched away, leaving all areas protected excepting the oxide directly above the channel.

The oxide directly the channel is then etched away. This brings us to step 1.2,a. The remaining photoresist is scrubbed away. An insulating layer of silicon dioxide is grown upon the wafer. The care taken to grow this layer is of great importance.

This layer of oxide passivates the source and drain regions. The thickness of this layer above the channel is a factor in the determination of gate threshold voltage. This particular layer is the final silicon dioxide layer to be grown on the device and forms the dielectric material of the MOSFET. Therefore, it is in this step that safeguards must be taken to prevent ionic drift. The result is shown in fig. 1.2,b.

Again, photoresist is applied; the photoresist is exposed through a mask which allow access through windows to the oxide just above the drain and source. After the resist process is repeated, the area directly above the drain and source is accessible to the etching solution. (1.2,c).

The remaining photoresist is removed, allowing free access to the silicon dioxide layer. The contact metal, usually aluminum, is evaporated over the surface of the wafer.

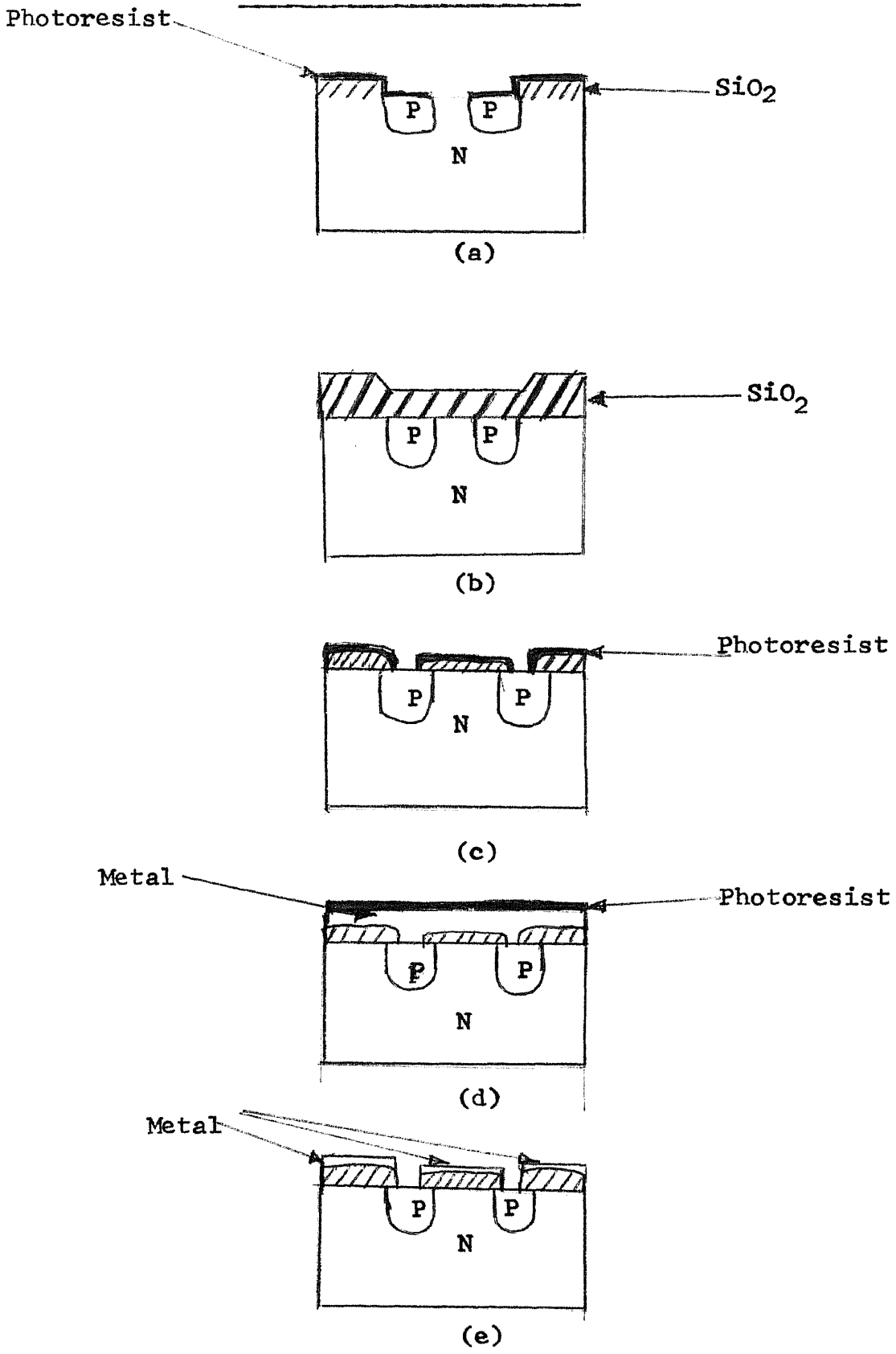

Photoresist
SiO_2
P
P
N
(a)
SiO_2
P
P
N
(b)
Photoresist
P
P
N
(c)
Metal
Photoresist
P
P
N
(d)
Metal
P
P
N
(e)

Figure 1.2

Two methods are possible for the aluminum deposition. One requires the wrapping of the aluminum around a tungsten filament, which is then heated until the aluminum vaporzies. Impurities from the heated filament, itself, are easily introduced here, and this particular method is a great contributor of sodium ions to the silicon dioxide layer.

The preferred method uses X-ray bombardment of the aluminum, located in a dish some twenty inches below the wafers. When the aluminum is heated enough, a protective shutter is removed and the metal deposition begins. The growth of the aluminum is stopped at some thousand angstrom units. The chip is again coated with photoresist in preparation for the next mask. (1.2,d).

The chip is again exposed through the mask to ultraviolet light, so that after the usual process of development, etching away the unexposed areas of the resist, removing the unwanted metal, and then scrubbing away the exposed resist, we arrive at a wafer with metal areas accessible for the bonding of wire contacts (fig.1.2e). Leads are attached to drain, aource and gate metalization areas by thermocompression bonding, a combination of force and high temperature.

Before the leads are attached, the wafer is scribed and broken up into the individual devices. The individual die is attached to the header, and one mil gold wires are then bonded to the proper bonding pads. Excessive heat generated in this step might result in the shifting of the MOSFET characteristics. An alternate approach to thermo-compression bonding used by some manufacturers is ultrasonic bonding.

The device is then placed in the package; encapsulation is done in a controlled atmosphere chamber. The package ambient gas is usually dry nitrogen. If there is any moisture in the package atmosphere, the operation of the device at elevated temperatures can be affected. The presence of water at high temperature can raise the gate to source threshold voltage since the water can act as a donor.

Eisenberg et al. report finding traces of hydrogen, oxygen, helium and hydrocarbons in the package atmosphere. Improper cleansing after the various steps inadvertently leaves organic solutions and solvents in the package atmosphere.(2)

(2) Eisenberg,P.H.,G.V.Brandewie and R.A.Meyer "Effects of Ambient Gases and Vapors at Low Temperatures on Solid State Devices." Seventh Annual N.Y. Conference on Electronic Reliability (May 20,1966)

1.2 Theory of Operation

MOSFET's (Metal-Oxide-Semiconductor Field-Effect-Transistors) depend upon only one carrier for their operation, which in the case of a P-channel MOSFET, is the positive carrier, holes.

The conventional transistor is known as a bipolar transistor since its operation depends upon minority carrier flow in the transistor base region. The bipolar transistor also differs in that its collector current flows at right angles to the physical surface of the device. In MOSFET's, the current flow is through narrow channels parallel to the surface.

The heart of the operation of the MOSFET is the inversion channel formed by a capacitor-like phenomenon. If the metal of the gate is taken as one plate is taken as one plate and the N-type substrate as the other plate of a parallel plate capacitor, then the silicon dioxide layer may be thought of as the dielectric. (See figure 1.3).

The polarities in the following discussion deal with P-channel MOSFET's; the following paragraphs hold for N-channel devices if the polarities are reversed.

Formation of inversion channel. If a negative voltage is applied to the gate, it becomes negatively charged, requiring that a positive line charge be formed opposite the gate at the gate/insulator interface. (See figure 1.3). In order that Gauss' law be satisfied, there must exist another line charge,of negative polarity, inside the insulator at the silicon dioxide /N-type substrate interface.

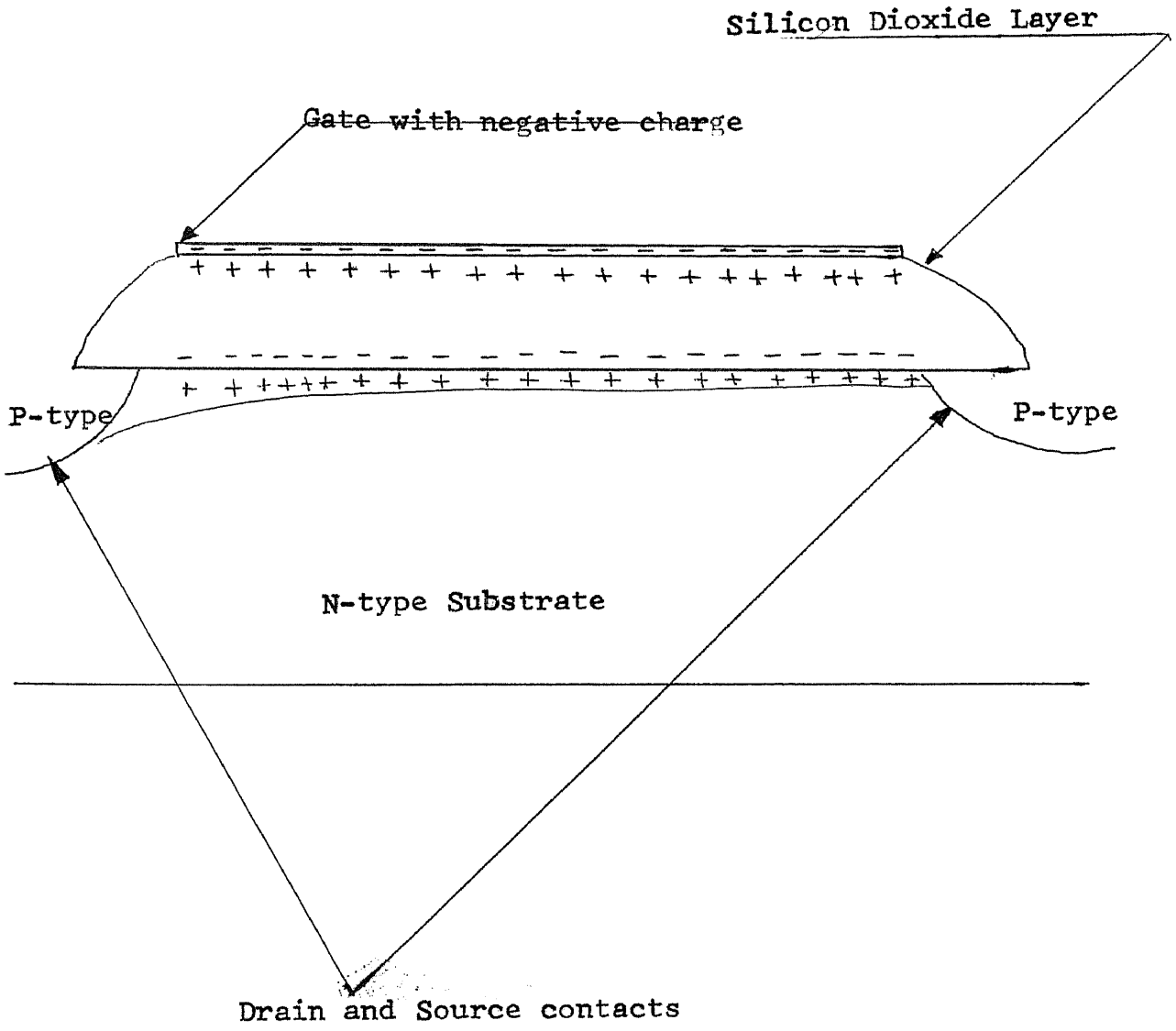
A counterbalancing charge must be drawn up through the substrate to this interface; this results in a channel of positive charge, holes, connecting the drain and source. The N-type substrate has been inverted to P-type material.

With the source and substrate leads grounded, and the drain tied to a negative voltage,e.g. -20 volts, current in the form of holes will start to flow at some value of gate voltage, V_T, the threshold voltage.

"The threshold, or turn-on, voltage of an MOS transistor can be defined as that value of gate voltage for which current just starts to flow between the drain and source." [3]

(3) Richman,Paul, Characteristics and Operation of MOS Field-Effect Devices (McGraw-Hill,New York, 1967)

FORMATION OF INVERSION CHANNEL



The conductance of the channel between the source and drain is a function of the gate voltage, and the drain to source voltage. If the source is grounded, then we speak of V_{DRAIN} only.

For a given gate voltage, as the drain voltage is increased, current increases up to a point where the channel "pinches off", or the device saturates.

In the region marked, 'A', in figure 1.4,a, the drain current flowing, for a fixed voltage from gate to source, changes as the drain voltage increases. This is known as the "triode region".

Saturation is reached when

$$V_{Drain} = V_{Gate} - V_{Treshold}$$

Saturation is shown in the region marked, 'B' in figure 1.4,a. In this region, the V_{GS} combined with the V_{DS} cannot change the current in the channel; the device has saturated.

The last region, region 'C', has been called the avalanche region. This is due to the avalanche breakdown of the back-biased drain/substrate diode. The drain is a pocket of P-type material diffused into an N-type substrate. This forms a diode that is back-biased in normal operation of the MOSFET.

CHARACTERISTIC CURVES

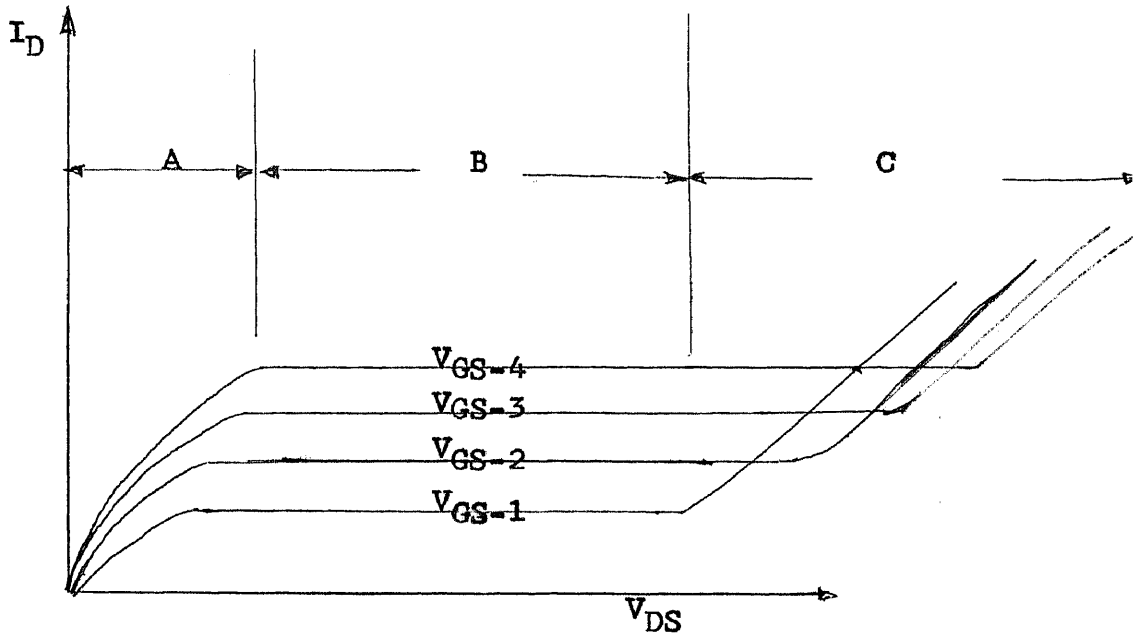
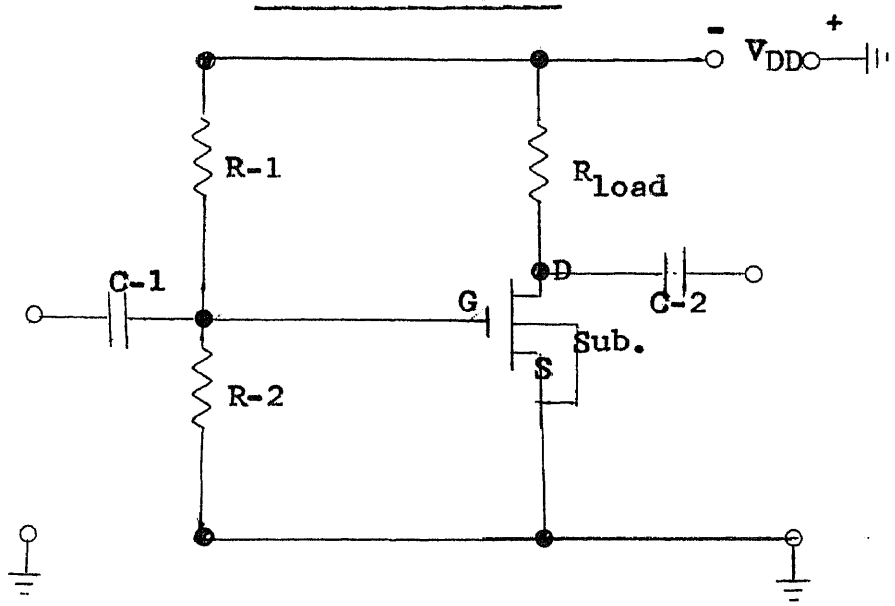


Fig. 1.4,a

TYPICAL CIRCUIT



When the voltage, V_{DS}, is increased while holding the gate voltage constant, the device passed from the variable resistance region, 'A', into the saturation region, 'B'. Now, as the drain voltage is further increased, the back-biased diode goes into normal avalanche breakdown, region 'C'. The drain current begins to increase from its saturation value, first gradually, then more rapidly, as the drain/substrate diode goes into avalanche breakdown.

In figure 1.4,b, V_{DD} is a negative voltage thus back-biasing the diode mentioned. Referring to figure 1.4,b, again, if a signal of alternating voltage is applied through the capacitor, C 1, to the gate terminal, there is a resulting modulation in the drain current. A relationship for the saturation region is given by:

$$I_D = \frac{\beta}{2} \left[V_G - V_T\right]^2$$

The factor, β, depends upon the length-to-width ratio of the channel, which, in turn, depends upon the physical layout of the device.

This results in the varying of the drain current in-phase with the alternating signal upon the gate. The varying drain current, i_{ds} , flowing in the output load, R_{load} , results in an amplified voltage that is out-of-phase with the input signal.

When the device is turned off , the leakage phenomenon involved in a MOSFET is exactly the same as that in a planar bipolar transistor. In MOSFET's, the leakage current, I_{DSS} is in the nanoampere range.

The operation of the MOSFET depends upon the capacitor formed by the silicon dioxide layer. This same layer is the cause of most of the troubles of the MOSFET.

DRIFT AND FAILURE MECHANISMS

2.1 Failure Mechanisms.

MOSFET's are afflicted with many of the failure mechanisms which afflict bipolar transistors, including: breaks in metalization, bonding failures, increase in leakage current and packaging leaks. These mechanisms are not peculiar to MOSFET's and will not be dealt with in this paper.

The failure mechanisms peculiar to MOSFET's are twofold: the breakdown of the thin silicon dioxide layer and the drift of threshold voltage with time and temperature. Threshold voltage drift is the main topic of this paper.

Insulator breakdown. The thin silicon dioxide layer is easily broken down under normal handling conditions. This layer, the heart of the device, is only about 1000 angstrom units thick. Since the dielectric breakdown of silicon dioxide occurs at approximately 10^7 volts/centimeter, only 100 volts will cause breakdown of the thin silicon dioxide layer.

If the low breakdown voltage is then compounded with the low value of gate capacitance, it can be seen that MOSFET's present a handling problem.

Taking a typical value of gate capacitance as 10 picofarads, and a breakdown voltage of 100 volts, it is seen that a charge of only 10^{-9} coulombs will be capable of destroying the insulating layer.

($Q = CV$; $Q = 10^{-11}$fx 100v = 10^{-9}coulombs).

This small quantity of charge is easily stored on the nylon smocks commonly worn in clean rooms and is easily generated by the movements of the personnel wearing them. Another source of destroyed devices was found to be the charge-generating styrofoam containers used to ship semiconductor devices. It was found that the motion of the styrofoam packing caused a build-up of static electricity in quantities large enough to destroy the insulating layer.

The solution to this problem was the inclusion of a zener diode on the chip with the MOSFET. The diode is connected from the gate electrode to the substrate, with such a polarity that normal operating potentials will not cause the zener diode to break down. However, if a voltage exceeding the zener breakdown voltage is applied, the diode will break down, thus putting an upper limit on the voltage applied to the gate.

Threshold drift. If an enhancement mode MOSFET is turned on for a period of time at an elevated temperature, a peculiar effect may be observed upon the removal of the turn-on gate voltage; the transistor does not turn off!

In order to turnon a P-channel MOSFET, a negative voltage must be applied to the gate. This sets up an electric field, directed from substrate to the gate as shown by the arrow in figure 2.1. This figure represents a cut-out section of the MOSFET's gate-insulator-substrate interfaces.

The electric field, directed from the substrate to the gate, causes any impurities in the insulator to line up in the direction of the field, if the impurities have a charge. The electric field so set-up causes any free positive ions in the insulator to travel away from the substrate and towards the gate. If the impurities are easily disassociated, the electric field imposes a force upon the charges so that the positive ions will migrate towards the gate.

If the electric field is present for a long period of time and if thermal energy is added to the reaction, the disassociated ions will have had a total force on them to force them to travel the thickness of the oxide.

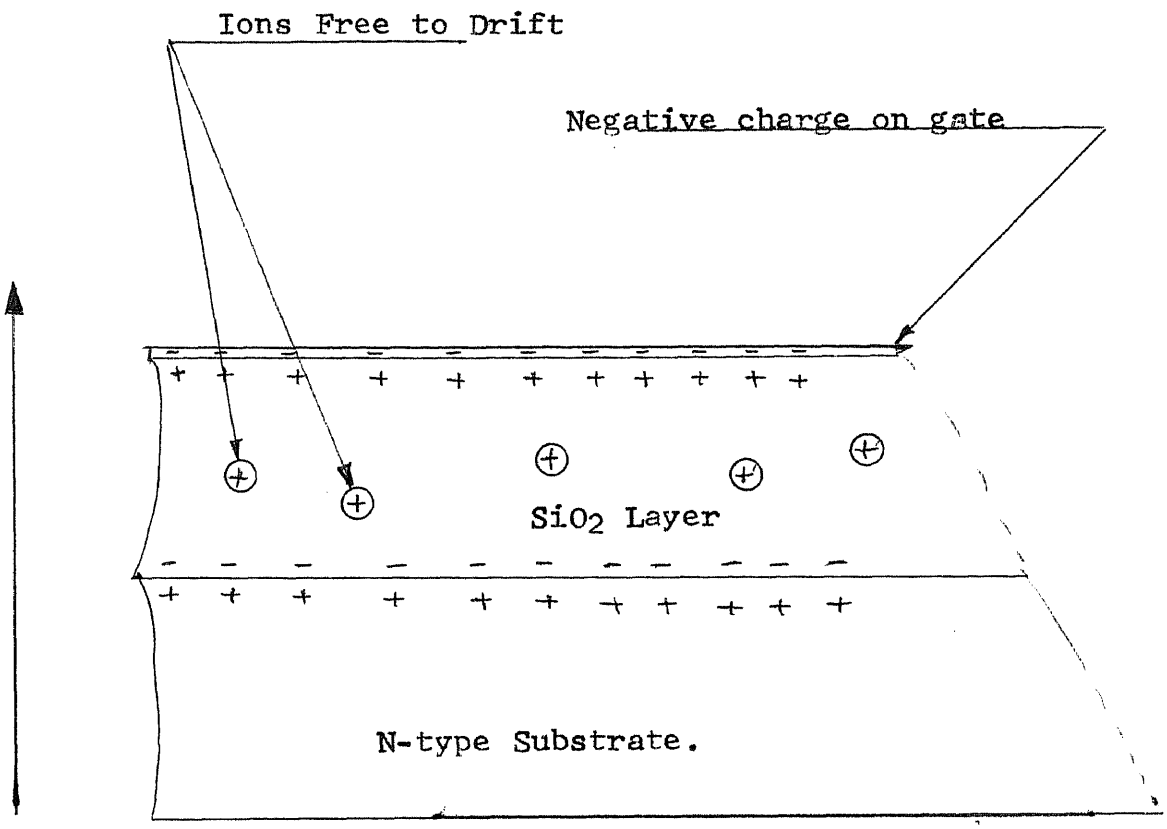

Ions Free to Drift
Negative charge on gate
SiO2 Layer
N-type Substrate.

Figure 2.1

This drift mechanism depends upon the ability of the ions to move freely in the oxide; different authors have shown that under the combination of high temperatures and electric fields, sodium ions migrate rapidly. (For example, under fields of ±50v/micron at 250°C, Snow et al. have shown sodium to drift.) [4]

In the P-channel devices used in this work, the positive ions would travel to the gate under the conditions described. With the removal of the gate signal, the ions have no force applied to them to cause them to assume their original positions. They remain at the gate.

There is then a positive line charge residing at the gate/oxide interface and this positive line charge is reflected at the oxide/channel interface as a negative charge. Following the steps out logically, it shows that a counterbalancing charge must be drawn up through the substrate to this interface, forming a channel between the source and the drain. Therefore, the magnitude of the negative voltage required to produce 10 microamperes of I_D (the threshold voltage), is reduced.

A microscopic drift mechanism has caused a macroscopic drift in MOSFET parameters.

(4) Snow,E.H.,A.S.Grove,B.E. Deal and C.T·Sah, Journal of Applied Physics, 36,p.1664 , 1965.

A measurement of the amount of drift is the magnitude of the voltage required to return the MOSFET characteristics to the same conditions that existed previous to the drift of the ions across the silicon dioxide layer. In a P-channel enhancement mode MOSFET, a more positive voltage is required to reduce the channel current to the same value that was present before the ionic drift.

This drift mechanism once produced a shift of five to six volts in the characteristics of the MOSFET. Today's technology has produced units with a drift voltage of less than 0.5 volts.

Explanation of drift mechanism. A more formal explanation for threshold drift may be found by looking at the expression for the threshold voltage. The threshold voltage is a function of the work function of the metal used for the gate, a function of the uncompensated charges in the structure, the characteristics of the oxide and the source to substrate voltage. For purposes of this paper, the source may be considered tied to the substrate.

The value of the threshold voltage is determined largely by the doping level of the substrate.

An expression for the threshold voltage is given:

$$V_T = \frac{-(Q_O + Q_{ss} + Q_b)}{\left(\frac{e_{ox}}{t_{ox}}\right)} + \phi_m - \Delta V_T$$

where:

Q_O is the charge contained in the oxide

Q_{ss} is the charge that resides at the Si/SiO_2 interface, the surface states.

Q_b is the charge in the substrate.

e_{ox} is the dielectric constant of the oxide.

t_{ox} is the thickness of the oxide.

ϕ_m is the work function of the aluminum-silicon dioxide interface.

V_T is a factor dependent upon the bias of the source to substrate, assumed zero in this paper.

Therefore, in order that a channel may be formed, the voltage on the gate must produce enough charge to neutralize the charge in the oxide, at the silicon/silicon dioxide interface and in the substrate between source and drain. This is done by calling up holes from the substrate to counterbalance the charge applied to the gate.[5]

(5) Hilbourne, R.A. and J.F. Miles "The Metal Oxide Semiconductor Transistor" Electronic Engineer (GB) Vol. 37, No. 445, March, 1965.

The quantity of oxide charge may shift the threshold voltage away from the value which normally would be predicted if only the doping level of the substrate were taken into consideration.

Defining the charge upon the gate as Q_G and using the symbols defined on the previous page, it may be said that:

$$Q_G = C_{ox}V_G$$

where Coxis the capacitance of the oxide and V_G is the voltage on the gate.

(N.B. All charges defined here and on the previous page are to be taken per cm^2.).

The charge residing on the gate and in the oxide must be counterbalanced by charge in the silicon and at the surface states. Therefore, it may be said:

$$Q_G + Q_{ox} = -(Q_b + Q_{ss}\ ).$$

and

$$C_{ox}V_G = -(\ Q_b + Q_{ss} + Q_{ox}\ ).$$

If, for the time being , we ignore the surface states, then the presence of the oxide charge has resulted in the shift of the threshold voltage by a factor of:

$$\Delta V_T = -\frac{Q_{ox}}{C_{ox}}$$

since the threshold voltage now not only has to counterbalance the bulk charge but also the oxide charge.

With the completion of the device, the parameters of oxide thickness, the work function and the dielectric constant are fixed. The only changes that can account for drift in threshold voltage are changes in the charge distribution. The charge distribution in the oxide changes when the ions drift under the influence of heat and electric field.

Therefore, it has been shown that the drift in threshold voltage, V_T , depends upon the charge in the oxide and at the surface states.

Identification of drifting ions. After manufacturers had shown that the drift in threshold voltage was caused by ionic drift in the oxide, a search was instituted to determine which ion was at fault. Two culprits of note were the sodium ion and the hydrogen ion. Today, it is generally accepted that the drift is due to sodium ions .

It has been found that contamination of the outer oxide surface with sodium ions can cause serious instabilities in MOSFET's.[6]

(6) Snow,E.H.,A.S. Grove et al. "Ion Transport Phenomena in Insulating Films." Journal of Applied Physics Vol. 36,No.5,1664 to 1673, May, 1965.

In another paper, it is shown that carefully prepared oxide films do not show instability effects. It is also shown in this particular paper that the number of surface charges per cm^2 (called N_f) at the silicon/silicon dioxide interface are lower in carefully grown oxide films.[7]

Other authors show that the instability of MOSFET's is due to the long-term ionic movement of sodium in the insulating layer.[8]

Thus, in oxide films where sodium is expressly excluded for the purposes of the experiment, effects of instability were not found.

It has also appeared that after the usual oxide preparation, there may be found a fairly large concentration of sodium ions in the top layer of the oxide film.[9]

(7) Grove, A.S, B.E.Deal et al. Solid State Electronics Vol. 8, pp. 145 to 163, 1965.

(8) Grove, A.S., E.H. Snow, et al. "Stable MOS Transistors" Electro-Technology, pp. 40-43,December, 1965.

(9) Yon,E. W.H. Ko, and A.B. Kuper, IEEE Trans. ED-13, pp.276-280, 1966.

Correlation of impurity ions with surface states.

On the previous page, it was reported that one author(7) had shown that the number of surface charges per cm^2(N_f) at the silicon/silicon dioxide interface is lower in oxide films carefully grown to exclude sodium. It would appear, then, that oxide films not carefully grown will have both sodium ion impurities and increased surface states.

It has also been suggested that the pile up of sodium in the oxide near the interface is responsible for the surface charge. (9).

Another author reports that the value of N_f, the number of surface charges per cm^2, depends most markedly upon the surface orientation of the silicon crystal (111 or 100 surface oriented) when sodium is present. The orientation called (111) has a lower value of N_f than the orientation called (100) with sodium being present in both cases. (10)

The value of N_f was found by means of C-V curves at a frequency of 500 kilohertz.

(10) E. Kooi, Philips Res. Repts. 20, pp.578-594, 1965.

Another author studying drift of MOSFET's threshold voltage concludes,

> " ...the application of an electric field for a long time across the SiO_2 layer produces in the two cases (field effect device and M.O.S. capacitance) variations of characteristics which can be interpreted in terms of variation of surface charges density." [11]

In general, if the manufacturing processes were such as to produce a great many interface surface states, there qualitatively exists the possibilty of impurities piling up at these interfaces during long term drift tests. As it has been shown that carefully grown oxide films have a lower number of surface states per cm^2, the reverse is true: that if less care is taken in the preparation of the device, sodium will enter the process and the number of surface states will increase.

(11) Grosvalet, J. "Mechanisms os Instability and Evolution in the M.O.S. System of Insulated Gate Field Effect Devices." Proc. IEEE Fifth Annual Conference on Basic Failure Mechanisms, Newark, New Jersey, June 15,1964

2.2 Drift Control.

There are three approaches to the control of the threshold voltage drift.

The first method is to eliminate the source of the trouble: the contaminating ions. However, under massproduction methods, it is almost impossible to eliminate sodium from any process in which human beings are involved.

A second approach would be to change the insulating material to some type of material that lowers the mobility of the ions. The mobility of the Na^+ ion seems to be lower in silicon nitride than in silicon dioxide. However, it also follows that a whole new technology for etching and growing the silicon nitride must be developed.[11]

A compromise approach would be to reduce the mobility of the sodium ion in the silicon dioxide layer. It has been reported that the sodium ion drift can be reduced drastically by putting a thin layer of phosphosilicate glass in the insulating layer. The mobility of the Na^+ ion is much lower in the glass layer than in the silicon dioxide layer.

(11) Woitsch, F. "Silicon Nitride Etching". Solid State Technology, pp.29 -31, January,1968.

The sodium ions travel through the silicon dioxide layer until they reach the glass layer, where their mobility is severely reduced. The ions cannot readily pass through the phosphosilicate glass layer; this eliminates most of the electric field drift instability.

"The addition of phosphorus forms a glass-like structure which is more dense than silicon dioxide. This may reduce the mobility of the ions, producing a more stable oxide." [12]

(12) Wallmark and Johnson, Field-Effect Transistors: Physics, Technology and Applications p.212 Prentice Hall, Englewood Cliffs, New Jersey, 1965

NOISE

3.1 Noise Theory

Noise is usually defined as any spurious unwanted signal, random in nature and being aperiodic. There are two ways to classify noise: by its cause and by its place in the frequency spectrum.

The types of noise of interest to this paper are: (1) thermal noise

(2) shot noise and

(3) 1/f noise.

Thermal noise. Thermal noise is due to the random motion of carriers caused by thermal agitation. A measure of the intensity of thermal noise is given by the Nyquist relation:

$$\bar{E}^2 = 4kTR(BW)$$

where: $\bar{E}^2$ = the rms noise voltage

k = Boltzmann's constant

T = the temperature in degrees, Kelvin

R = the resistance of the conductor in ohms,

(BW) = the bandwidth of the measuring system in hz.

Thermal noise is known as white noise as it has a uniform frequency distribution, and depends, as the equation shows, upon the temperature and on the resistance. A bipolar transistor generates thermal noise primarily because of its base resistance.

The value of noise voltage depends upon the bandwidth of the measuring device, for , since the frequency distribution is flat, a wider bandwidth contains more noise .

Shot noise. Shot noise also has a uniform frequency distribution. In bipolar transistors, shot noise is present due to the randomness of carrier diffusion from emitter to collector, and is associated with the generation and recombination of minority carriers. Shot noise in MOSFET's is due to the variation in channel mobile-carrier concentration.

1/f Noise. This type of noise has also been called modulation, flicker or semiconductor noise.

"Its origin is thought to lie in the semiconductor crystal imperfections and in surface effects. ... the mean square voltage is inversely proportional to the frequency, f."[13]

(13) Le Croissette,Dennis Transistors Prentice-Hall, Inc. Englewood Cliffs, New Jersey 1965.

A basic relationship for 1/f noise may be given by:

$$\bar{E}^2 = \frac{AI^2(BW)}{f}$$

where $\bar{E}^2$ = the rms value of the noise voltage;

A = some constant depending upon the physical case in question;

I^2 = the square of the current;

(BW) = the bandwidth of the measuring system;

f = the center frequency of the system.

It can therefore be seen that the rms magnitude of noise voltage varies inversely as the frequency and directly with the square of the current.

As can also be seen, the value of noise voltage measured depends upon the bandwidth of the measuring system. The measuring instruments used for this paper have a nominal bandwidth of one cycle around some center frequency.

Since the devices measured, (MEM- 511's), all have the same layout, the factor,'A', is held constant; The value of current squared, I^2, depends upon the signal applied to the device under measurement. This value will be held constant.

The frequency of measurement, f, is limited by the measuring system to 10 hertz and 1000 hertz. The frequency, 1000 hertz, is at the upper limit of what is normally called the 1/f region. The frequency, 10 hertz, is directly in the 1/f region. Thus, noise voltage measurements will be made at two different frequencies in the band of interest.

Since all factors are being held constant, differences in measured values for individual devices will have to be accounted for by some factor in the device itself that is different.

Noise measurements must be used to pinpoint some noise generating defect or some phenomenon that accompanies the defect and also has the property of increasing the noise power. If the defect and/or drift mechanism does not alter the noise spectrum of the device in question, then, noise measurments are of no use in predicting the drift and/or life of the device. In subsequent pages, a correlation will be made between drift and/or failure mechanisms and 1/f noise magnitude.

3.2 1/f Noise and Failure Mechanisms.

Noise measurements may be used to indicate which samples of a certain lot of devices will fail and/or drift, if there is a corresponding increase in noise due to the defect and/or failure mechanism. Various authors have reported correlation of noise measurements with the prediction of drift and/or failure of a device.

For example, certain resistor defects have the property of generating excessive 1/f noise, due to the high (relatively) current density formed along the defect in the resistor. These defects could be caused some contaminant, and imperfect construction of the resistor. These tiny faults channel current through them in excess of the surrounding areas, and thus become generators of 1/f noise of greater value than normal for the unit.

By examining resistors for 1/f noise, it is reported that it was possible to predict which of the resistors would change values during a life test.

> "The results of this test... show a perfect correlation in the drift vs the magnitude of noise."[14]

(14) Stansbury,Alan P. "Noise Analysis and Failure Mechanisms in Electronic Components." Proceedings IEEE Fifth Annual Conference on Basic Failure Mechanisms Newark, New Jersey, June, 1964.

Measurements of 1/f noise have also been used to predict failures in transistors. In one particular case, it was found that the noise level of a certain bipolar transistor increased greatly just before the end of the transistor's life.

Van der Ziel used noise measurements in conjunction with life tests to determine when a transistor would fail. He reported that just before the transistor failed, there was a marked increase in 1/f noise.

> "Low-frequency noise... is known to be very sensitive to changes in a transistor's surface conditions and the gas ambient atmosphere within the transistor package. Therefore, noise at 1000Hz. could be expected to give a better indication of the life expectancy of the device than any other parameter." [15]

Other authors have done work with noise and failure mechanisms. (For example, see 16).

(15) Van der Ziel and Hu Tong, "Low-frequency Noise Predicts Transistor Failure." Electronics, Vol. 39 No. 24, November 28,1966.

(16) Stansbury, Alan P. "Role of Noise in Failure Mechanisms in Transistors." Seventh Annual New York Conference on Electronic Reliability. May 20,1966

There are then many precedents for the use of 1/f noise measurements to differentiate between a device with the possibility of early failure and a device with a normal life expectancy.

3.3 Correlation of 1/f noise and Drift Mechanism.

Noise measurements must be used to pinpoint some noise generating defect in the device in question. In MOSFET's, the preceding sections have shown that the drift causing mechanism depends upon ions in the insulating layer. Further, it has been shown that surface states are related to these very ions. In this section, a correlation will be made between the presence of surface states and 1/f noise.

In a paper by Hsu,et al., it is shown that, "... the same surface states that gave rise to the increased noise in the p-n junction also lead to an increase in 1/f noise in MOS transistors." [17]

(17) Hsu, S.T., D.J.Fitzgerald and A.S Grove, "Surface-State Related 1/f Noise in p-n Junctions and MOS Transistors." Applied Physics Letters, Vol 12, No. 9, May 1,1968.

The term usually given to those silicon atoms of the crystal, located at the surface of the crystal, and having unfilled bonds, is "surface states." When these surface states occur at the joining of silicon and silicon dioxide, they are given the name, "interface states." It is estimated that there are about 10^{15} dangling bonds per square centimeter on the surface of semiconductor material.

An author who has correlated 1/f noise with surface states is O. Jäntsch. In one of his recent papers, he stated,

> " The 1/f noise at semiconductors is produced by a fluctuation of non-equilibrium minority carriers. By reason of the fact that it can be influenced by surface treatments, its origin can be traced to a fluctuation of surface recombination." [18]

He also states, in the same paper, that an ideal crystal with ideal contacts, and NO surface states cannot show a 1/f noise according to the model he presented.

(18) Jäntsch, O. "A Theory of 1/f Noise at Semiconductor Surfaces." Solid-State Electronics, Vol 11, pp 267-272 February, 1968.

Again recently, work has been done upon the correspondence of noise with surface states. In a paper by Abowitz et al.[19], the authors have correlated noise in MOS transistors with the uncontrolled variation of the surface state density in these transistors.

As explained previously, these surface states are related to the ions that drift through the oxide when under the influence of an electric field. There will be a greater drift of threshold voltage if there are more impurities present. At the same time, if there are a greater number of impurities present, then there will be a greater number of surface states. This increase in the number of surface states will be reflected in an increase in the 1/f noise of the device over a device without this increased number of surface states.

(19) Abowitz,G.,E.Arnold and E.A. Leventhal, IEEE Transactions on Electronic Devices, ED-14, 775, 1967

3.4 MOSFET Noise.

In this final section on noise, a synopsis of the noise characteristics of MOSFET's will be given.

Thermal noise. A MOSFET has thermal noise proportional to the factor, kT(BW) and is due to the resistance in the channel. This noise has a uniform frequency distribution.

Shot noise. As mentioned, this noise in bipolar transistors is dependent upon the generation and recombination of minority carriers. In MOSFET's, shot noise is due to the fluctuation of the concentration of channel mobile-carriers. As with thermal noise, shot noise has a uniform frequency distribution.

1/f noise. In MOSFET's, this type of noise has been shown to be related to variations in surface states and in the number of carriers occupying these surface states. In general, bipolar transistors have lower 1/f noise than MOSFET's. It is important to note that this noise varies almost exactly as the inverse of frequency. Therefore, low frequency measurements of noise voltage will give an indication of the number of surface states in the individual MOSFET.

EXPERIMENTAL PROCEDURES

4.1 Threshold Voltage Measurement.

The test circuit for measuring threshold voltage is shown in figure 4.1. Threshold voltage is defined as that voltage from gate to source, V_{GS}, that just causes 10 microamperes of drain current to flow.

In figure 4.1, the source is shown connected to the substrate and both of these terminals are grounded. Drain current was maesured with an accurate ammeter, (HP- 425A) and all voltages were measured with a digital voltmeter accurate to the fourth place, (HP-). The letters, HP, stand for Hewlett-Packard.

In order to show the slight effect the drain voltage has on the value of threshold voltage, measurements of threshold voltage were taken with drain voltages, V_{DS}, of -5,-10,-15 and -20 volts. Results are displayed in table 1, page 44.

Unit numbers which are missing are units that were inadvertently destroyed(e.g. by placing the unit in the socket backwards).

After this initial set of readings, all measurements of threshold voltage were taken with the drain voltage at -20 volts.

THRESHOLD VOLTAGE MEASURING CIRCUIT

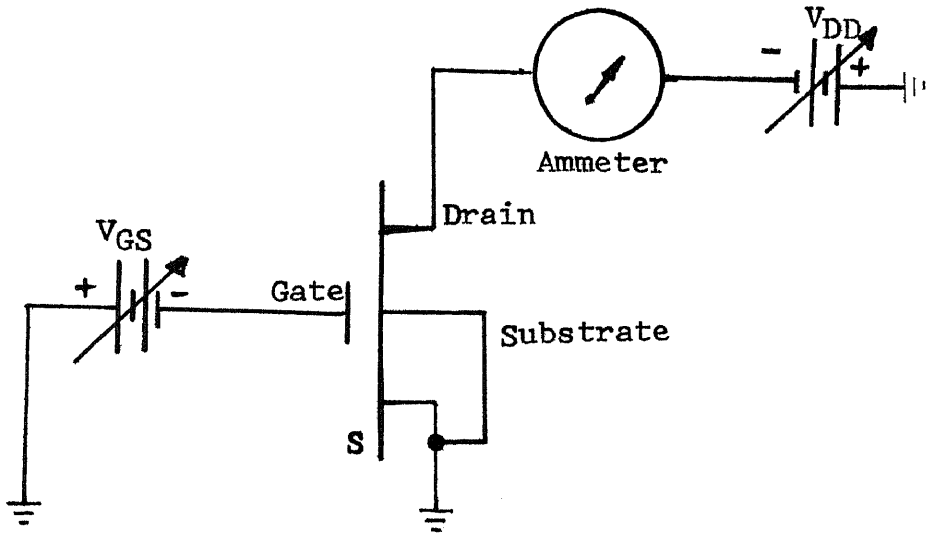


Figure 4.1

Table I: Threshold Voltage versus Drain Voltage.

UNIT	V_{DS} = -5.00v	V_{DS} = -10.00v	V_{DS}= -15.00v	V_{DS} = -20.00v
1	-3.8060	-3.7860	-3.7708	-3.7509
2	-3.5809	-3.5637	-3.5527	-3.5307
3	-4.4908	-4.524	-4.5208	-4.5099
4	-3.4687	-3.4601	-3.4437	-3.4458
7	-3.6847	-3.6635	-3.6556	-3.6325
8	-4.2668	-4.2328	-4.2218	-4.1840
9	-4.5831	-4.5789	-4.5528	-4.5589
10	-3.7560	-3.7389	-3.7260	-3.7090
11	-3.9153	-3.9074	-3.8863	-3.8886
12	-3.8850	-3.8744	-3.8529	-3.8629
13	-4.0269	-4.0006	-3.9976	-3.9876
14	-3.5837	-3.5755	-3.5536	-3.5556
15	-4.2135	-4.2088	-4.1974	-4.1976
16	-3.3447	-3.3226	-3.3147	-3.2916
17	-3.8345	-3.7888	-3.7246	-3.6276
18	-3.0766	-3.0718	-3.0716	-3.0638
19	-4.9388	-4.9255	-4.9088	-4.8818
20	-3.4949	-3.4868	-3.4648	-3.4678
21	-3.8048	-3.7977	-3.7735	-3.7776
22	-3.6729	-3.6584	-3.6279	-3.6224
24	-3.6776	-3.6475	-3.6476	-3.6205
25	-3.6998	-3.6786	-3.6758	-3.6506

Table I, cont.

Unit	V_{DS} = -5.00v	V_{DS}= -10.00v	V_{DS} = -15.00v	V_{DS}= -20.00v
26	-3.7547	-3.7286	-3.7347	-3.7206
27	-3.3967	-3.3928	-3.3667	-3.3766
28	-3.5343	-3.5237	-3.5148	-3.4929
29	-3.6377	-3.6157	-3.6077	-3.5757
30	-3.6461	-3.6453	-3.6301	-3.6253
31	-3.8707	-3.8547	-3.8169	-3.7809
32	-3.1595	-3.1555	-3.1305	-3.1435
33	-3.4505	-3.4475	-3.4264	-3.4356
35	-3.8137	-3.8306	-3.6347	-3.8187
37	-3.5988	-3.5918	-3.5988	-3.5848
38	-3.8960	-3.8755	-3.8734	-3.8364
39	-3.4805	-3.4784	-3.4563	-3.4484
40	-3.6503	-3.6457	-3.6196	-3.6257
41	-3.7856	-3.7674	-3.7705	-3.7507
44	-3.1277	-3.1007	-3.1118	-3.0787
45	-3.5566	-3.5446	-3.5257	-3.5285
46	-3.1429	-3.1328	-3.1339	-3.1229

As can be seen from the data presented in the table, on pages 44 and 45, the threshold voltage varies only in the hundredth place as the drain voltage, V_{DS}, goes from five to twenty volts in steps of five volts. Threfore, the threshold voltage is largely independent of drain voltage.

The devices used in this test were MEM - 511's, P-channel, enhancement mode MOSFET's, produced by General Instrument Corporation, Microelectronics Division. Each MEM - 511 is specified as having a minimum threshold voltage of -3.0 volts and a maximum threshold voltage of -6.0 volts. All of the units tested met this specification.

Statistics of Sample. A summary of the statistics for the values of threshold voltage measured at -20 volts VDS. The smallest value of threshold voltage of the thirty-eight devices was -3.0638 and the largest value of threshold voltage measured was -4.8818 volts.

The arithmetic mean for the sample was -3.72585 v. and the median was calculated as -3.6776 volts. The standard deviation was calculated as 0.38096 volts.

It is important to note here that the smallest value of threshold voltage measured was -3.0638 volts. Out of a total sample size of thirty eight units, thirty three units had a threshold voltage of less than 4.0 volts (this is 84 per-cent of the sample lot).

Drift test. A total of twenty units, randomly selected were put on drift test at an elevated temperature of 125° C. The test circuit is shown in figure 4.2. Under conditions of V_{DD} equal to -30 volts, a gate voltage of between -8 and -9 volts will be developed by the divider of R-1 and R-2. With a load resistor of 3300 ohms, a drain current of about 3.0 milliamperes will flow, resulting in a voltage of V_{DS} of -20 volts. Thus, the drift test was run with the same V_{DS} that the threshold voltage was measured at.

Measurements of the threshold voltage with the V_{DS} at -20 volts were used as the basic readings of threshold voltage. The units were put on high temperature drift tests and the units were again measured after 250 hours. This is a total of 5000 unit hours. The value of threshold voltage for the units measured are given in Table II for before and after drift test.

Table II: Threshold Voltage Drift

Unit	Before Test	After Test	Threshold Drift
13	-3.9876v	-4.2622v	+0.2746v
14	-3.556	-3.5103	-0.0457
15	-4.1976	-4.2133	+0.0157
17	-3.6276	-3.6092	-0.0184
16	-3.2916	-3.2933	+0.0017
18	-3.0638	-2.6350	-0.4288
20	-3.4678	-3.3293	-0.1385
21	-3.7776	-3.7561	-0.0215
22	-3.6224	-3.6113	-0.0111
24	-3.6205	-3.4112	-0.2091
27	-3.3766	-3.6092	+0.2326
29	-3.5757	-3.8931	+0.3174
31	-3.7809	-3.6912	-0.0897
32	-3.1435	-3.1686	+0.0251
33	-3.4356	-3.4052	-0.0304
35	-3.8187	-3.9048	+0.0861
38	-3.8364	-3.3630	-0.4734
39	-3.4484	-3.5387	+0.0903
44	-3.0787	-1.4653	-1.6134

Units were chosen randomly, but are arranged here numerically for clarity.

Distribution of Threshold Voltage

BEFORE TEST

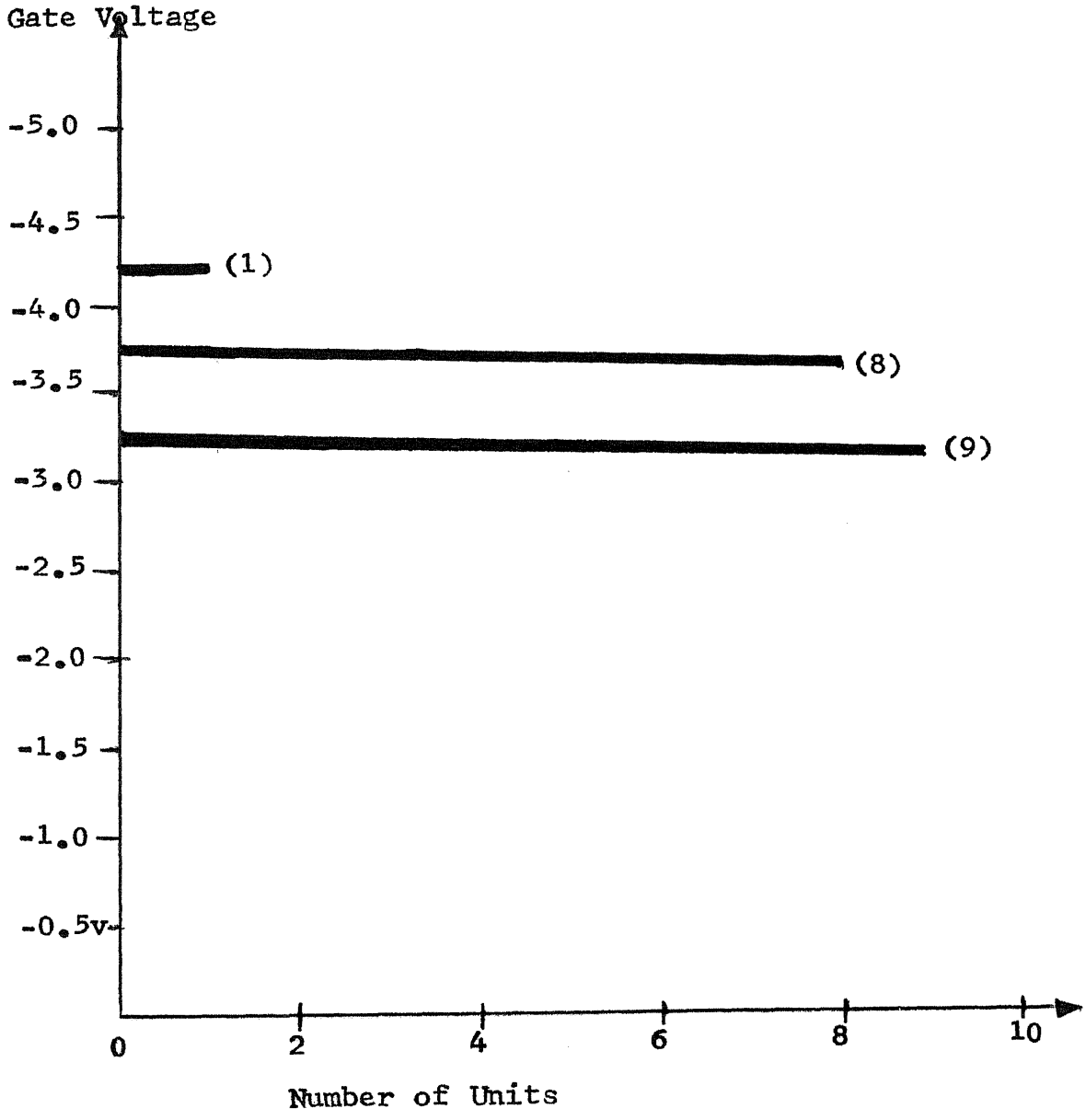


Figure 4.2

Distribution of Threshold Voltage

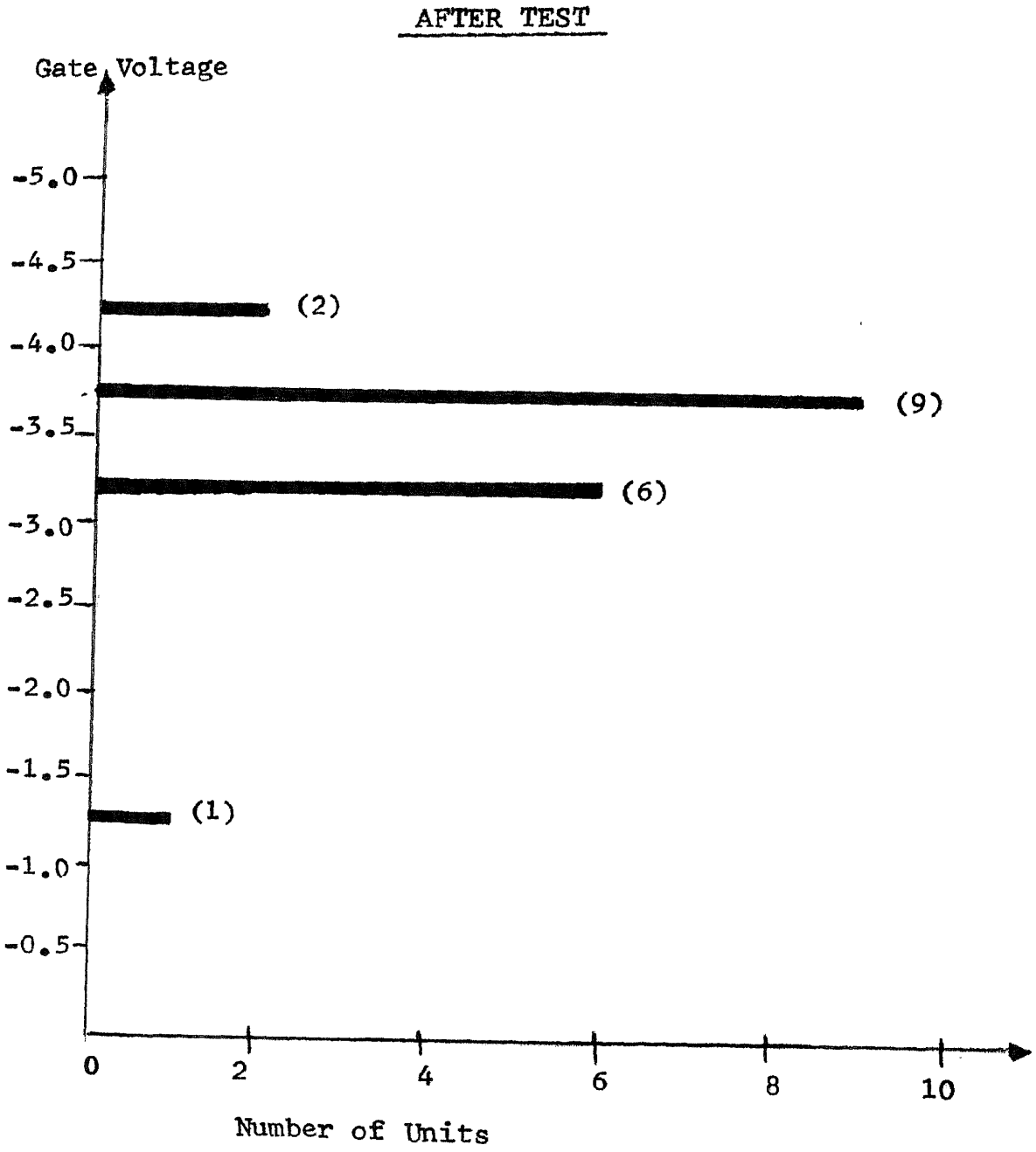


Figure 4.3

The tabulated results show that all of the units had a threshold drift of less than half a volt, in magnitude, excepting unit number 44. This unit not only drifted more than three times its partners, but it alos drifted out of specification (as did unit number 18). Recall that the specification for threshold voltage of an MEM-511 was between -3.0 and -6.0 volts.

The drift of threshold voltage for unit number 44 is in the direction of a more positive value. This drift fits in exactly with the theory set forth in section 2.1 of this paper. Thus, unit number 44 suffered threshold voltage drift due to ionic drift in the insulating layer.

4.2 Noise Voltage Measurements.

Noise measurements were made upon the units by use of the "Quan-Tech" transistor noise analyzer. The model 2173C in conjunction with model 2181 filter unit will give values of noise voltage, $\bar{E}^2$, the rms value of noise voltage, at five different frequencies.

Due to capacitive effects in the unit, the values of noise voltage at 10KHz and 100 KHz may not be truly due to the device under test. Therefore, the values of noise voltage at 10,100 and 1000 Hz were the only values recorded.

Conditions of test. The model 2173C allows the user to select the gate and drain voltages applied to the MOSFET under test (the source and substrate are tied together and grounded.). In order to prevent overload of the measuring meters in the noise analyzer,by experimentation,the drain voltage was set at -10 volts and the gate voltage was adjusted to give -1.0 milli-amperes of drain current, I_D.

Noise voltages were recorded at three frequencies: 10 Hz, 100 Hz and 1000 Hz. The results are recorded in Table III. Values given in Table III are in nanovolts, 10^{-9} volts.

Table III : Noise Voltage Measurements

Unit	Noise Volts @ 10 Hz	Noise Volts @ 100 Hz	Noise Volts @ 1000 Hz
0	1400 nv	450nv	140 nv
00	1300	510	160
13	2100	600	150
14	1600	600	150
15	2400	1000	245
17	2000	660	180
18	2200	660	180
20	2500	660	175
21	1500	510	160
22	1400	450	140
24	1700	640	160
27	1800	660	150
29	2200	680	180
32	1800	600	170
33	1400	500	155
35	1500	510	165
38	2000	660	180
39	1400	540	160
44	2600	700	180

Results of noise test. As can be seen from Table III, there is a wide range for noise voltage at any particular frequency.

However, the table does show that the noise voltage at 1000 Hz is fairly constant over the sample range and bears out the fact that the major component of noise in MOSFET's is of a 1/f nature.

The two units marked '0' and '00' were brand new units, purchased by the author in order to obtain some sort of a sample of units that had never been touched. As can be seen from the table, these two units had a noise frequency distribution similar to the units measured previously.

It should be brought out here that the unit that suffered the largest drift in threshold, #44, had the largest voltage at 10 Hz : 2600 nanovolts. However, it should also be brought out here that unit # 15, which had no appreciable threshold drift, also had a high 10 Hz noise voltage: 2400 nanovolts.

Units which had a fairly large drift in threshold voltage were 18, 29, and 38.

At 10 Hz. these three units had values of noise voltages as set forth below:

18	2200 nv
29	2200 nv
38	2000 nv

The average value of noise voltage at 10 Hz, was 1831 nanovolts. Each of the four units that suffered the greatest drift in this test had a value of 10 Hz noise that was almost 200 nanovolts above this average. However, unit # 15, which did not drift, had a noise voltage at 10 Hz of 2400 nanovolts.

The unit with the largest drift, # 44, also had the largest voltage at 10 Hz : 2600 nanovolts. This does represent some correlation of drift with low frequency noise, but, in view of the fact that a unit which did not drift also had a fairly high noise voltage at 10 Hz, a direct and binding correlation can not be made.

CONCLUSIONS

5.1 Summary of Drift Tests.

Twenty units of the forty units available to me were put on drift test at an elevated temperature of 125° C. Four of the twenty units tested had a drift in threshold voltage greater than 0.3 volts. Two of this four drifted out of specification for the MEM- 511. Unit number 44 had a drift of -1.6134 and unit number 18 had a drift of -0.4288 volts. This drift voltage is in the more positive direction.

This drift which units numbers 18 and 44 suffered is the typical drift described in section 2.1 of this paper; according to the theory set forth by many sources the drift of threshold voltage is due to ionic drift in the insulator.

Ten of the forty units available to me were not put on drift test at 125° C, but were put into a test circuit as shown in figure 4.1. These ten units were measured after the same length of time as the twenty units on elevated temperature test. The threshold voltage of these units were measured and found to have changed very little.

Correlation of noise and drift. In the attempt to correlate noise and drift magnitudes, a contradiction arose. The units which had a great magnitude of drift also had a great magnitude of noise voltage at 10 Hz. However, one of the units which did not drift also had a great magnitude of 10 Hz noise voltage. This does allow a one-to-one correlation to be made.

There is a correlation between the units that drifted and the magnitude of noise voltage, in that four units which drifted did have the largest voltages at 10 Hz. An absolute correlation can not be made because of the unit which was large in noise and did not drift.

Not enough units drifted to make a good statistical correlation with the noise measurements that were taken.

RECOMMENDATIONS

In theory, there has been made a correlation between the drift inducing mechanism and 1/f noise. An attempt to produce this condition experimentally did not meet with clear-cut success.

Therefore, it is recommended that more sample devices be run over drift and noise tests. Included in this sample should be P-channel and N-channel devices from different manufacturers so that no prejudice be introduced by a certain manufacturing process common only to one producer.

In general, this paper is a first step in the correlation of 1/f noise measurements and drift mechanisms in MOSFET's. It has been shown that the drift causing mechanism can be correlated with 1/f noise, but due to the limited resources available to the author, this correlation has not been definitely shown in experiments.

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