Spring 1993

Monolithic silicon opto-electro-mechanical light modulator

Ching-Horng Wu
New Jersey Institute of Technology

Copyright Warning & Restrictions

The copyright law of the United States (Title 17, United States Code) governs the making of photocopies or other reproductions of copyrighted material.

Under certain conditions specified in the law, libraries and archives are authorized to furnish a photocopy or other reproduction. One of these specified conditions is that the photocopy or reproduction is not to be "used for any purpose other than private study, scholarship, or research." If a, user makes a request for, or later uses, a photocopy or reproduction for purposes in excess of "fair use" that user may be liable for copyright infringement,

This institution reserves the right to refuse to accept a copying order if, in its judgment, fulfillment of the order would involve violation of copyright law.

Please Note: The author retains the copyright while the New Jersey Institute of Technology reserves the right to distribute this thesis or dissertation

Printing note: If you do not wish to print this page, then select "Pages from: first page # to: last page #" on the print dialog screen

ABSTRACT

Monolithic Silicon
Opto-Electro-Mechanical
Light Modulator

by
Ching-Horng Wu

A Fabry-Perot light beam modulator of the reflection-type has been designed with process and performance parameters optimized. This design takes advantage of the economies of surface micromaching using silicon substrates and selected thin films. High performance with a low drive voltage are achieved using electrostatic actuation of a thin polysilicon diaphragm. The diaphragm is a novel corrugated structure which has maximum compliance and maintains planarity during actuation. In addition, the corrugation-suspension used provides an improved linearity of amplitude modulation response as a function of the actuation voltage.

A preliminary version of this device has been fabricated through a contract foundry using some industry-standard film thicknesses. The preliminary version of the device confirms the physical mask design without optimal film processing. The optimized Fabry-Perot structure is designed for operation at a wavelength of 1.3 nm. Using a thin, corrugated diaphragm of 190 nm thickness a 48.90% modulation index is obtained with an actuation voltage of 5 volts based on detailed simulation results. The final optimized device will be fabricated at NJIT at a future date.

The proposed optimized device contains a titanium-tungsten metal film deposited into a cavity of half wavelength depth and insulated from the monolithic silicon substrate. An additional quarter wavelength film of silicon nitride is deposited over the metal to increase the modulation index. In the fabrication process a 325nm sacrificial film of spin-on glass is deposited to fill the cavity and form the spacer between the Fabry-Perot etalon

entrance and reflecting surfaces. The optical entrance surface is obtained next in the fabrication process by depositing an infrared-transmissive film of polysilicon. The selected polysilicon thickness is 190 nm or any odd integer multiple of a half wavelength.

This device can be used as an economical light modulator in near-infrared communications and control systems. This device suitable for relatively low bandwidth applications is expected to provide cost and reliability advantages over competing torsion mirror and macro-sized modulators.

MONOLITHIC SILICON OPTO-ELECTRO-MECHANICAL LIGHT MODULATOR

by
Ching-Horng Wu

A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering

Department of Electrical and Computer Engineering

May, 1993

APPROVAL PAGE

Monolithic Silicon Opto-Electro-Mechanical Light Modulator

Ching-Horng Wu

Dr. William N. Carr, Thesis Adviser
Professor and Holder of Sponsored Chair in Microelectronics,
NJIT

Dr. Edip Niver, Committee Member
Associate Professor of Electrical Engineering,
NJIT

Dr. Robert B. Marcus, Committee Member
Research Professor of Applied Physics,
NJIT

Dr. Farmer, Kenneth R., Committee Member
Assistant Professor of Physics,
NJIT

BIOGRAPHICAL SKETCH

Author: Ching-Horng Wu

Degree: Master of Science in Electrical Engineering

Date: May 1993

Undergraduate and Graduate Education:

- Master of Science in Electrical Engineering,
  New Jersey Institute of Technology, Newark, NJ, 1993

- Bachelor of Science in Electrical Engineering,
  Feng-Chia University, Taichung, Taiwan, R. O. C., 1991

Major: Electrical Engineering

To my parents

ACKNOWLEDGMENT

The author would like to express his sincere gratitude to his supervisor, Dr. William N. Carr, for his guidance, friendship, and moral support throughout this work. Especially thanks Dr. Carr sent him to Mentor Graphics Co., San Jose, CA. taking training courses which is great helpful for this work.

Special thanks to Professor Niver, Professor Marcus, and Professor Farmer for serving as members of the committee.

The author appreciates the kindly help, suggestions and discussion from Michael Grieco, Michael Berry, Dr. Xiaoyi Gu, Chang-Joo Kim, Chao Ye, and Chao Sun.

The author also appreciates the help from MCNC labs.

And finally, the author would like to thank his parents and Pingyu Wang for their love and encouragement. He also wants to express his thanks to his grandparents for their encouragement and they both died in February, 1993.

TABLE OF CONTENTS

Chapter **Page**

LIST OF TABLES

Tables **Page**

LIST OF FIGURES

Figure **Page**

Figure **Page**

Figure **Page**

Figure **Page**

CHAPTER ONE
INTRODUCTION

1.1 Thesis Description

Optical sensing technology has developed enormously during the last decade. Particular use has been made of optical fibers not only for conveying the beams but also as the sensing elements themselves. Advances to 1982 were reviewed by Giallorenzi et al (1982) with reference to over one hundred and thirty papers. Devices for sensing various physical perturbations, including magnetic, acoustic, thermal, acceleration, rotation etc., have now been developed and are usually categorized as either amplitude or phase (interferometric) sensors. In the former class the physical perturbation acts directly to modulate the intensity of the light; such sensors are simple and reliable with a performance matching that of existing technologies. In many cases however interferometic phase sensors offer theoretically orders of magnitude improvement in sensitivity. In the most widely used sensors they are made in centimeter scale.

With the increasing requirement for high density silicon memory cells has come the need for sophisticated I/O interfaces with a high data rate, low crosstalk and high reliability. Contactless connections such as optical interconnects are a promising solution, provided that reliable transmitters and receivers can be fabricated. Reliable and cheap transmitters fabricated in silicon, and compatible with standard silicon processing remain a major problem in releasing these devices.

Structures such as GaAlAs diodes grown in silicon substrates have been fabricated, but this increases production costs. A further solution is to use hybrid structures but this increases the size of the device. The ideal solution is to fabricate a transmitter which can be fabricated in silicon and is compatible with standard processing.

Light modulators have been produced in silicon by, for example, a silicon torsional mirror [1], or a deformable mirror device [2]. However, these techniques have the

disadvantages of a slow response time. Fabry-Perot interferometers have been fabricated using a combination of bulk micromachining and wafer-to-wafer bonding [3]. This process resulted in a high performance device with batch fabrication capabilities. However, bulk micromaching does not lend itself to high density arrays. Surface micromachining, on the other hand , by definition leads to small size and thus easy manufacture of arrays and furthermore, these structures do not suffer from slow response time. With careful consideration of the processing yields a process which is compatible with standard silicon processing.

In this thesis, the design and processing consideration for developing a micromechanical light modulator is described.

Chapter 1 reviews the development of Fabry-Perot etalon and micromechanics, the brief history of Fabry-Perot etalon and bulk micromechanical techniques and surface microengineering, Chapter 1 also introduces the background which inspired this work. Those readers interested in the Fabry-Perot etalon theory and the design work of this novel light modulator structure may concentrate on Chapter 2. The detailed theoretically analysis is covered in Chapter 3. The detail processing and mask design are discussed in Chapter 4. Chapter 5 describes spin on glass, as a sacrificial layer and planarization material and corrugated support structure developed for cavity structure process. Chapter 6 describes application for this devices. Finally in Chapter 7, conclusions are made.

1.2 Fabry-Perot Etalon

In 1831 George Biddell Airy, Professor of Astronomy in the University of Cambridge brought out a second edition of his 'Mathematical Tracts'. For that edition he had added a chapter on 'The Planetary Theory' and one on 'The Undulatory Theory of Optics'. A direct copy of Airy's figure 17 is shown as figure 1.1. In an elegant derivation Airy calculated the retardation V of successive components of vibration as being $2D\cos\beta$ and showed that the brightness of the reflected light was

$$\Phi_R = 4a^2e^2 \sin^2 \frac{\pi V}{\lambda}(1-2e^2 \cos^2 \frac{\pi V}{\lambda}+e^4)^{-1}$$

and of the transmitted light was

$$\Phi_T = a^2(1-e^2)^2[(1-e^2)^2 +4e^2 \sin^2 \frac{\pi V}{\lambda}]^{-1}\text{-})^{-1}$$

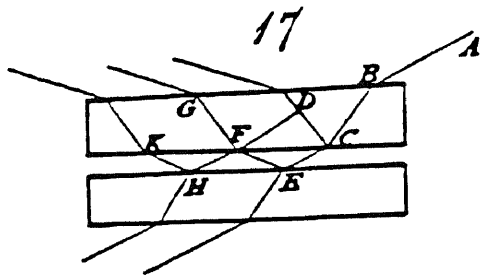


Figure 1.1 From Airy (1831, figure 17). The incident ray is shown entering along AB and experiencing successive reflections and refractions at *C, E, F, H* and *K*. The construction line *FD* is drawn perpendicular to the ray path *CD*.

In the forty years following Airy many significant advances were made in optics with contributions from most of the notable physicists of the 19th century. (For a brief review see for example the historical introduction to Principles of Optics by Born and Wolf (1975)). In December 1897 Fabry and Perot published in *Annales de Chimie et de*

Physique their paper *'On the fringes of thin silvered plates and their application to the measurement of small thicknesses of air'.* They noted prophetically that these '....*have led to the study of optical phenomena interesting in themselves, and to the invention of a method of measurement of small thicknesses which will doubtless be useful in other cases.'* Fabry and Perot firstly pointed to the sharpness and contrast ratio of fringes arising in a thin film of air between glass plates. In an ingenious device they described a mobile plate constrained between the two plates, movements as small as $\lambda/200$ of the tethered plate could be observed. In addition the tethered plate could itself be readjusted to a set position without the necessity of following its displacement and counting fringes.

Some idea of the increased use of Fabry-Perot interferometers is given by the list of leading centuries involved with measurement of standard wavelengths. Those topics have remained of interest to the present and , for the most part, the basic remained essentially unchanged from Fabry and Perot's day until the invention of the laser. The detail theory for the Fabry-Perot etalon will be introduced in chapter 2.1.

1.3 Silicon Micromechanics

An important and rapidly expanding area of silicon integrated circuit technology is silicon micromechanics [4]-[7]. This technology utilizes and develops silicon integrated circuit processing techniques to fabricate micromechanical structures together with electronic devices on silicon wafers. These micromechanical structures and devices when interfaced with integrated circuits and signal processing open up new opportunities for integrated sensors and robotics.

Two groups of unique processing techniques have been developed primarily for the fabrication of micromechanical sensor devices, bulk technology and surface technology. Bulk technology uses anisotropic wet chemical etching and special bonding techniques [8]-[11]. Surface technology, in contrast, uses silicon thin film technology of

polysilicon, oxide, PSG, silicon nitride, metal, and special purpose film such as stress free polysilicon [12], polymer, piezoelectric films, tin-oxide films and special metal films [13].

1.4 Bulk Micromechanics Technology

The first micromechanical device was a silicon diffused element piezoresistive diaphragm made in 1962 with bulk technology [14]. The main feature of this technology is the anisotropical etching of the silicon substrate with doping dependent chemical etchants, and some special bonding techniques. This technology has been extensively investigated and it has been successfully used to micromachine complex structure. A representative example is a integrated gas chromatography system developed by Standford in 1975 [15]. This work integrated the GC system including a 1.5-m-long capillary column, a gas control valve, and a detector element on a 2-inch wafer with isotropic etching, anisotropic etching and anodical bonding of glass plate to silicon techniques.

Figure 1.2 shows a cross section of a typical device formed using selective etching technology. The device could be a pressure sensor, an accelerometer, or light modulator. The wafer is to be selectively thinned from 300-500μm to from a diaphragm having a thickness control in the order of 1μm. Anisotropic etching will produce the desired lateral control. Anisotropic etchants attack the <100> and <110> directions at considerable etch rate, but attack the <111> direction at a rate typically 50 times slower. Thus, as illustrated in Figure 1.3(a), in <100> material, a cavity is formed with respect to the surface at an angle of 54.7°. In <110> material, vertical sidewall are produced [8][18].

There are three generally accepted anisotropic etching solutions for silicon: potassium hydroxide (KOH) [17], hydrazine [18], ethylene diamine-pyrocatechol-water (EDP) [19][20], and cesivm hydroxide (CsOH). While hydrazine has the distinction of not etching aluminum, it has few other advantages, tends to produce a rough surface, and can

be very dangerous to handle. It is thus not widely used. KOH is rsed in near saturated solutions (1:1 in water by weight) at 85°*C*. It produces a uniform etch and bright surface. This etch is preferred for shallow cavities where uniformity is important. It attacks silicon dioxide at a rate of about 60 A/min. EDP is better suited for deep etching since its oxide etch is negligible (5A/min). Also EDP produces a somewhat smoother surface compared with KOH.

In terms of vertical thickness control, the boron etch-stop technique has been developed to allow the etching process stops at desired vertical thickness [21]. This process relies on the fact that EDP essentially stops etching when the boron impurity concentration exceeds about 5×10^{19} cm^{-3} in the silicon lattice.

Bonding of one substrate to another substrate is also an important technology usedd in the fabrication of this device. The most generally used techniques are eutectic bonding [22], electrostatic silicon-to-glass bonding [23], silicon to silicon fusion bonding [24] and cemented bonding.

The main problem with bulk micromachining technology is the reduced compatibility with conventional IC processing for some process steps. One of the problems occurs in masking where photoresist will etch away quickly with anisotropic etchants. Special masking layers such as silicon nitride for KOH, aluminum or Silicon dioxide for EDP have to be deposited and patterned before the etching. The other problem is the slow etch rate of anisotropic wet etching. The temperature of the tech tank must be increased to obtain resonable etch rates. For example the etch rate of silicon [100] surface in KOH at 85°*C* is 1μm/min [27]. The boron etch stop requiring a high doping level is also a major problem in some processes. The high concentration doping makes the formation of integral circuits more difficult in some instances. If the devices are formed in epitaxial material grown on the top of the etch stop layer (a boron buried layer), there are problems

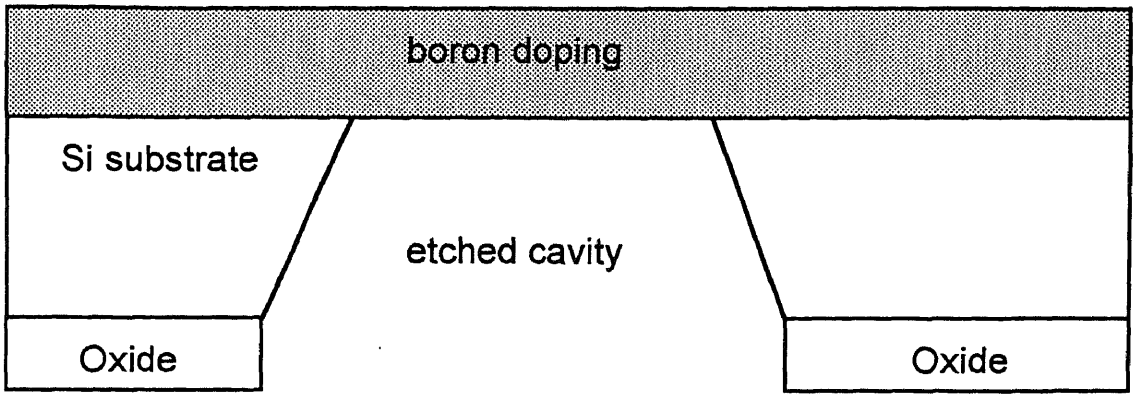


Figure 1.2 Cross section of a typical sensor device formed using anisotropic and selective etching techniques

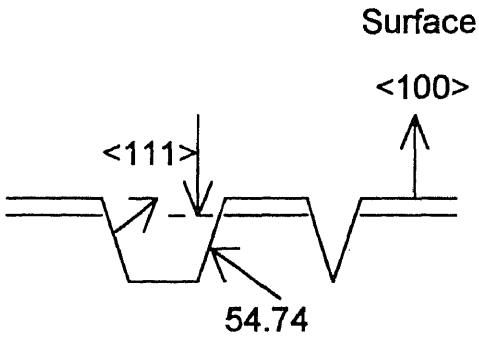


Figure 1.3a Anisotropic etching on <100> surface

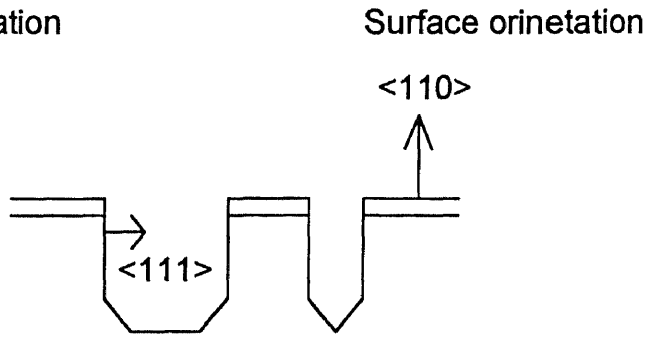


Figure 1.3b Anisotropic etching on <110> surface

with epitaxial film quality and out-diffusion of boron from the buried layer.

1.5 Surface Micromechanics Technology

Recently, surface technology represented by using polycrystalline as a mechanical material is drawing more attention because this technology avoids some challenging processing difficulties of bulk technology. It provides better compatibility with standard silicon device processes, and offers new degrees of freedom for the design of integrated sensors, actuators and circuits [5][28]. Using this technology, various types of structures such as

rotating and sliding structures, gears, springs [29][30] and various applications such as micrometer [31][32] have been made.

Figure 1.4 illustrates the processing sequence for fabricating a polysilicon cantilever and a double supported beam (microbridge). As shown in the figure, an oxide layer is initially grown or deposited on the silicon wafer. The first masking step opens windows in the oxide at the location the beam support areas, as shown in figure 1-3.2(a). Polysilicon is then deposited by chemical vapor deposition (CVD), and patterned by reactive ion etching in the second masking step. A lip of poly-Si is left around the perimeter of the oxide window to allow for misalignment error. If the poly-Si edge fails to overlap the oxide, then conventional RIE will erode the substrate after etch through the polysilicon layer. Immersing the wafer in buffered HF to remove all oxide and undercut the poly-Si layer. In figure 1.4(c) a free standing cantilever beam is created as illustrated. A double supported micromechanical beam (microbridge) is made by including a second oxide window, as illustrated in figure 1.4 (d) to (f).

Surface technology often uses polysilicon as a mechanical material. Silicon dioxide or phosphosilicate glass (PSG) as a sacrificial layer, and silicon nitride as an etch stop. The feature size of the micromechanical device is 1 to 2 orders of magnitude smaller than bulk technology. This technology is highly compatible with conventional processing technology. Several applications of integrating polysilicon micromechanical devices with on chip MOS circuit have reported [33][34].

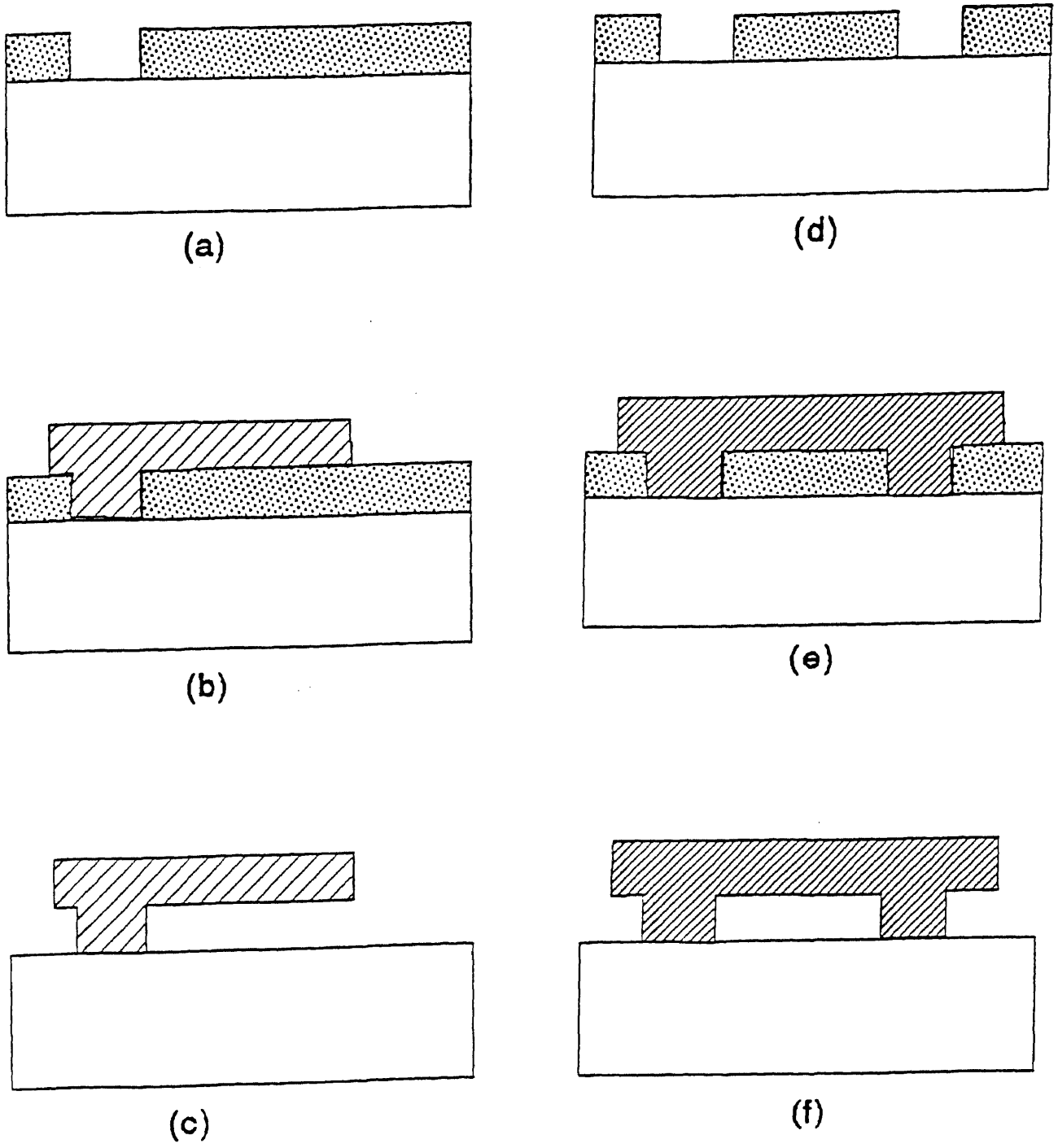


Figure 1.4 The processing sequence of polysilicon cantilever and double supported beam (microbridge)

One major problem of surface technology is that as-deposited LPCVD polysilicon film tends to buckle down due to strain after sacrificial layer of oxide is removed. Special techniques are being developed to produce a smooth surfaced, stress relieved polysilicon beam. Details will be discussed in Chapter 5 as it relates to this thesis.

1.6 Cavity Micromechanical Sensor Structure

One of the major applications of micromechanical technology is the solid state sensor [33][35]. By using micromechanical technology, numerous types of sensors such as accelerometer [36][38], pressure sensor, have been made.

Most microengineered accelerometer and pressure sensors reported up to now have been made with bulk micromechanical technology. Surface microengineering alone has not been used for many sensor applications yet. Surface microengineering is an even newer field compared with bulk technology. Currently, most surface microengineering techniques are more likely planar VLSI structures. As shown in figure 1.4., the planar structure allows only thin sacrificial layers.

Up to now, all reported methods to produce cavities were using bulk micromechanical techniques. The typical methods are:

1. Using anisotropic etching of silicon bulk to form cantilever beam, etching cavity from glass plate and using special bonding techniques to bond them together [41].

2. Producing SiO_2/Si epi/Heavy doped P+ buried layer sandwich. The silicon cavity is anisotropic etched from under the oxide to the heavily doped P+ buried layer to release the SiO_2 beam [42].

Those methods present processing complexity and compatible problems with conventional IC processing.

This cavity based bottom metal layer, sacrificial layer, polysilicon sensing element layer structure is a very powerful structure. It can be used to build three different types of

sensor, capacitive type, mechanical resonance type or piezoresist type, if different external circuits are connected.

Discussion will be limited to the light modulator application in this thesis although other sensor types could be involved.

CHAPTER 2
Fabry-Perot Etalon

2.1 Principles of Operation

The Fabry-Perot etalon, or interferometer, named after its inventors, is a basis of this thesis. It consists of a plane-parallel plate of thickness *l* and index *n* that is immersed in a medium of index n'. Let a plane wave be incident on the etalon at an angle θ' to the normal, as shown in Figure 2.1-1. We can treat the problem of the transmission (and reflection) of the plane wave through the etalon by considering the infinite number of partial waves produced by reflections at the two end surfaces. The phase delay between two partial waves is attributable to one additional round trip. It is given, according to Figure 4.2, by

$$\delta = \frac{4\pi nl\cos\theta}{\lambda} \qquad [2.1\text{-}1]$$

where λ is the vacuum wavelength of the incident wave and θ is the internal angle of incidence. If the complex amplitude of the incident wave is taken as A_i, then the partial reflections, B_1, B_2, and so forth, are given by

$$B_1 = rA_i, \qquad B_2 = tt'r'A_i e^{i\delta}, \qquad B_3 = tt'r'^3 A_i e^{2i\delta}, \ \ldots\ldots\ldots$$

where r is the reflection coefficient (ratio or reflected to incident amplitude), ℘ is the transmission coefficient for waves incident from n' toward n, and r' and t' are the corresponding quantities for waves traveling from n toward n'. The complex amplitude of the total reflected wave is $A_r = B_1 + B_2 + B_3 \ldots\ldots$, or

$$A_r = \{r + tt'r'e^{i\delta}(1 + r'^2 e^{i\delta} + r'^4 e^{2i\delta} + \ldots.)\}A_i \qquad [2.1\text{-}2]$$

For the transmitted wave,

$$A_1 = tt' A_i, \qquad A_2 = tt' r'^2 e^{i\delta} A_i, \qquad A_3 = tt' r'^4 e^{2i\delta} A_i, \ \ldots\ldots\ldots$$

where a phase factor exp(iδ), which corresponds to a single traversal of the plate and is common to all the terms, has been left out. Adding up the A terms, we obtain

$$A_t = A_i tt'(1 + r'^2 e^{i\delta} + r'^4 e^{2i\delta} + \ldots.) \qquad [2.1\text{-}3]$$

for the complex amplitude of the total transmitted wave. We notice that the terms within the parentheses in [2.1-2] and [2.1-3] form an infinite geometric progression; adding them, we got

$$A_r = \frac{(1 - e^{i\delta})\sqrt{R}}{1 - Re^{i\delta}} A_i \qquad [2.1\text{-}4]$$

and

$$A_t = \frac{T}{1 - Re^{i\delta}} A_i \qquad [2.1\text{-}5]$$

where we used the fact that r'= -r, the conservation of energy relation that applies to lossless mirrors

$$r^2 + tt' = 1$$

as well as the definitions

$$R = r^2 = r'^2 \qquad T = tt'$$

R and T are, respectively, the fraction of the intensity reflected and transmitted at each interface and will be referred to in the following discussion as the mirrors' reflectance and transmittance.

If the incident photo intensity (watts per square meter) is taken as $A_i A_i$ ", we obtain from (2.1-4) the following expression for the fraction of the incident intensity that is reflected:

$$\frac{I_r}{I_i} = \frac{A_r A_r''}{A_i A_i''} = \frac{4R\sin^2(\delta/2)}{(1-R)^2 + 4R\sin^2(\delta/2)} \qquad [2.1\text{-}6]$$

moreover, from [2.1-5],

$$\frac{I_t}{I_i} = \frac{A_t A_t''}{A_i A_i''} = \frac{(1-R)^2}{(1-R)^2 + 4R\sin^2(\delta/2)} \qquad [2.1\text{-}7]$$

for the transmitted fraction. Our basic model contains no less mechanisms, so conservation of energy requires that $I_t + I_r$ be equal to I_i , as is indeed the case.

Let us consider the transmission characteristics of a Fabry-Perot etalon. According to [2.1-7] the transmission is unity whenever

$$\delta = \frac{4\pi nl\cos\theta}{\lambda} = 2m\pi, \qquad \text{m=any integer} \qquad [2.1\text{-}8]$$

Using [2.1-1], the condition [2.1-8] for maximum transmission can be written as

$$\nu_m = m\frac{c}{2nl\cos\theta}, \qquad \text{m=any integer} \qquad [2.1\text{-}9]$$

where $c = \nu\lambda$ is the velocity of light in vacuum and υ is the optical frequency. For a fixed l and θ, [2.1-9] defines the unity transmission (resonance) frequencies of the etalon. These are separated by the so-called *free spectral range*

$$\Delta\nu = \nu_{m+1} - \nu_m = \frac{c}{2nl\cos\theta} \qquad [2.1\text{-}10]$$

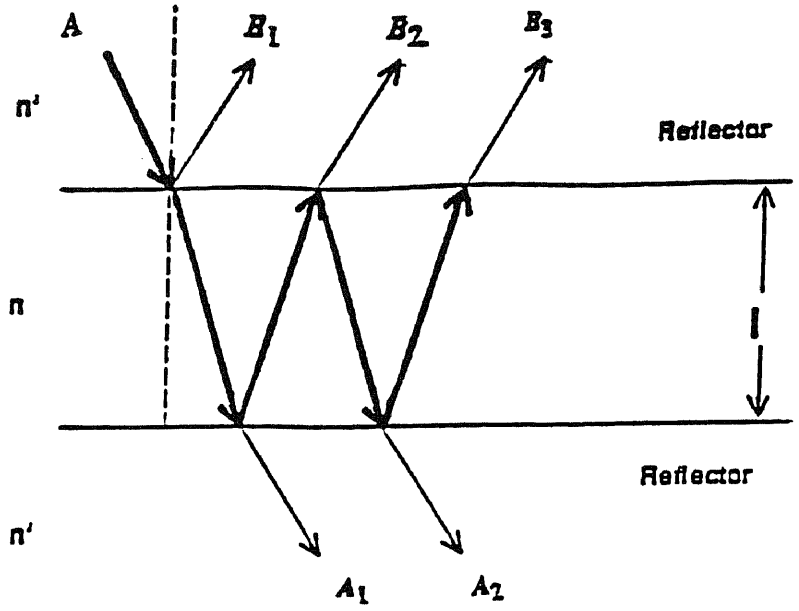


Figure 2.1 Multiple reflections model for analyzing the Fabry-Perot etalon

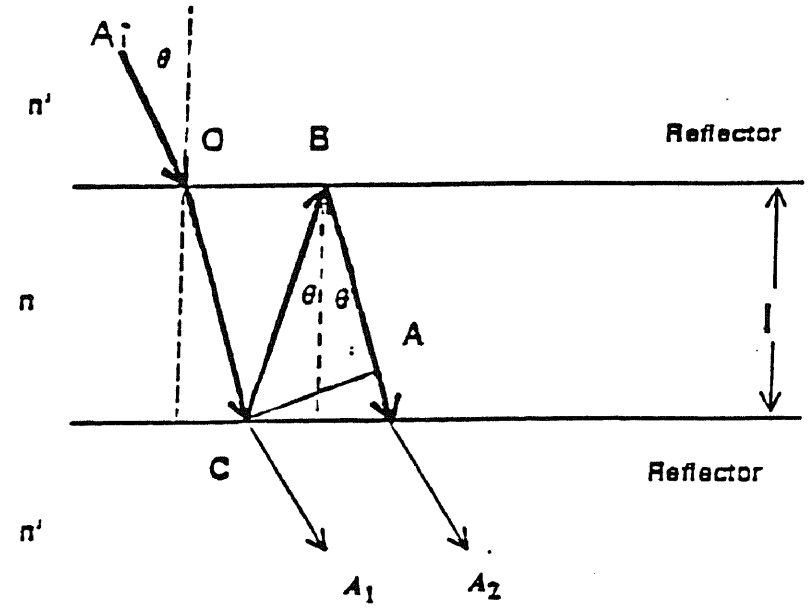


Figure 2.2 Two successive reflections, A_1 and A_2.

Theoretical transmission plots of a Fabry-Perot etalon are shown in Figure 2.3. The maximum transmission is unity, as stated previously. The minimum transmission, on the other hand, approaches zero as the net reflectance R approaches unity.

If we allow for the existence of losses in the etalon medium, we find that the peak transmission is less than unity. Taking the fractional intensity loss per pass as (1-A), we find that the maximum transmission T drops from unity to

$$T = \frac{I_t}{I_i} = \frac{(1-R)^2 A}{(1-RA)^2}$$

Calculated transmission plots of Fabry-Perot etalons are shown in Figure 2.4. This device geometry is given in figure 2.2. The incident optical source is normal to the interferometer surface. The bulk absorption of the device is neglected. The refraction index of the front and back surface is silicon dioxide (n=1.5).

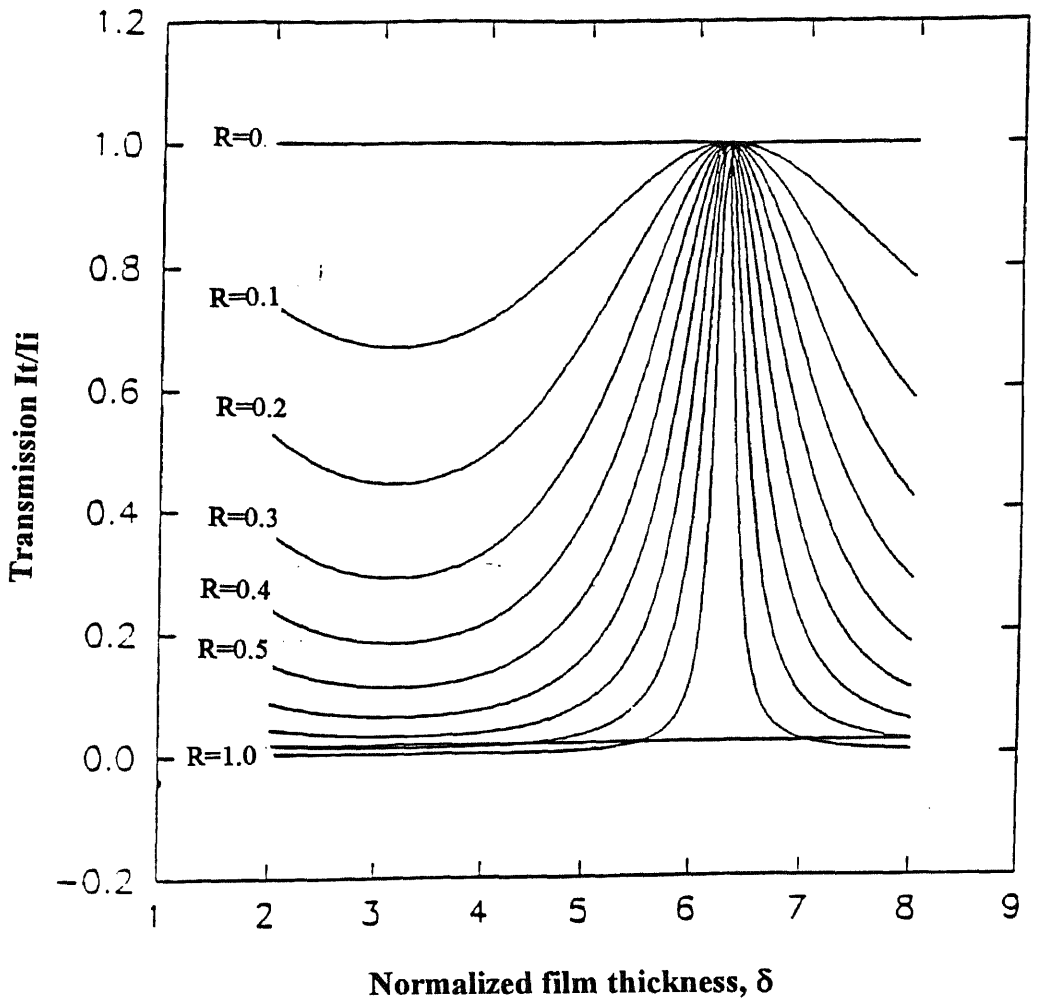


Figure 2.3a Transmission characteristics of a single film Plotted with equations 2.1-7a and δ is defined by 2.1-8

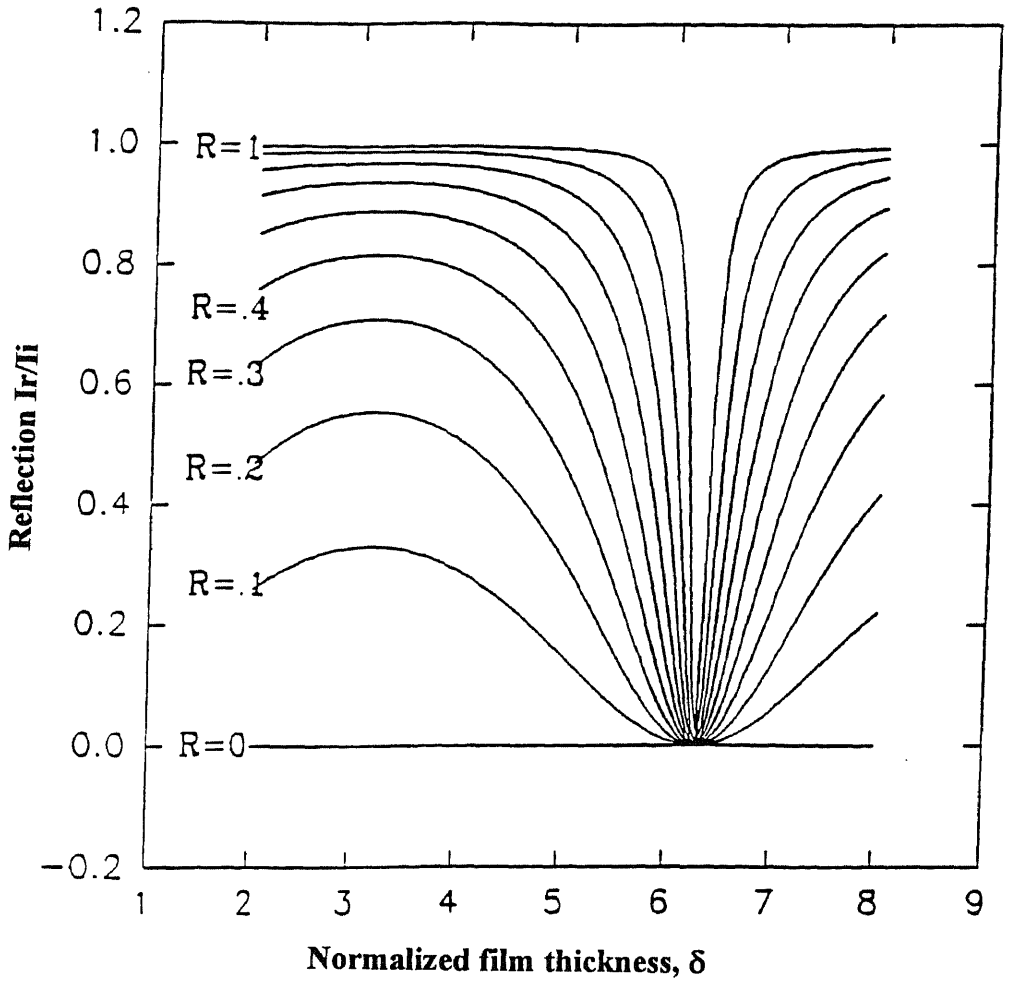


Figure 2.3a Reflection characteristics of a single film Plotted with equations 2.1-6a and δ is defined by 2.1-8

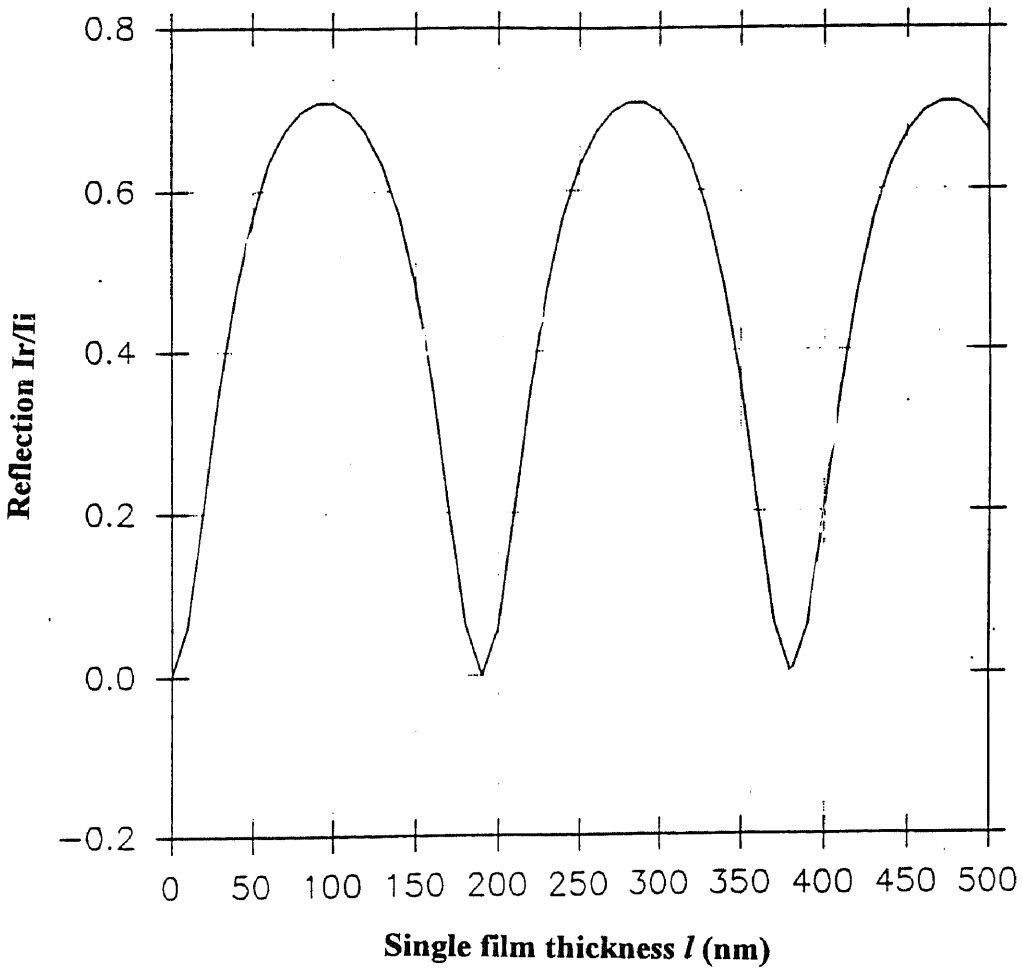


Figure 2.4a Calculated reflection characteristics of a Fabry-Perot single film etalon at 1300nm as a function of the etalon optical length with n'=1 and n=3.42 (figure 2.1). The peaks shown correspond to a change in the optical length $\Delta(nl)=\lambda/2$. ($\lambda=\lambda air/3.42$)

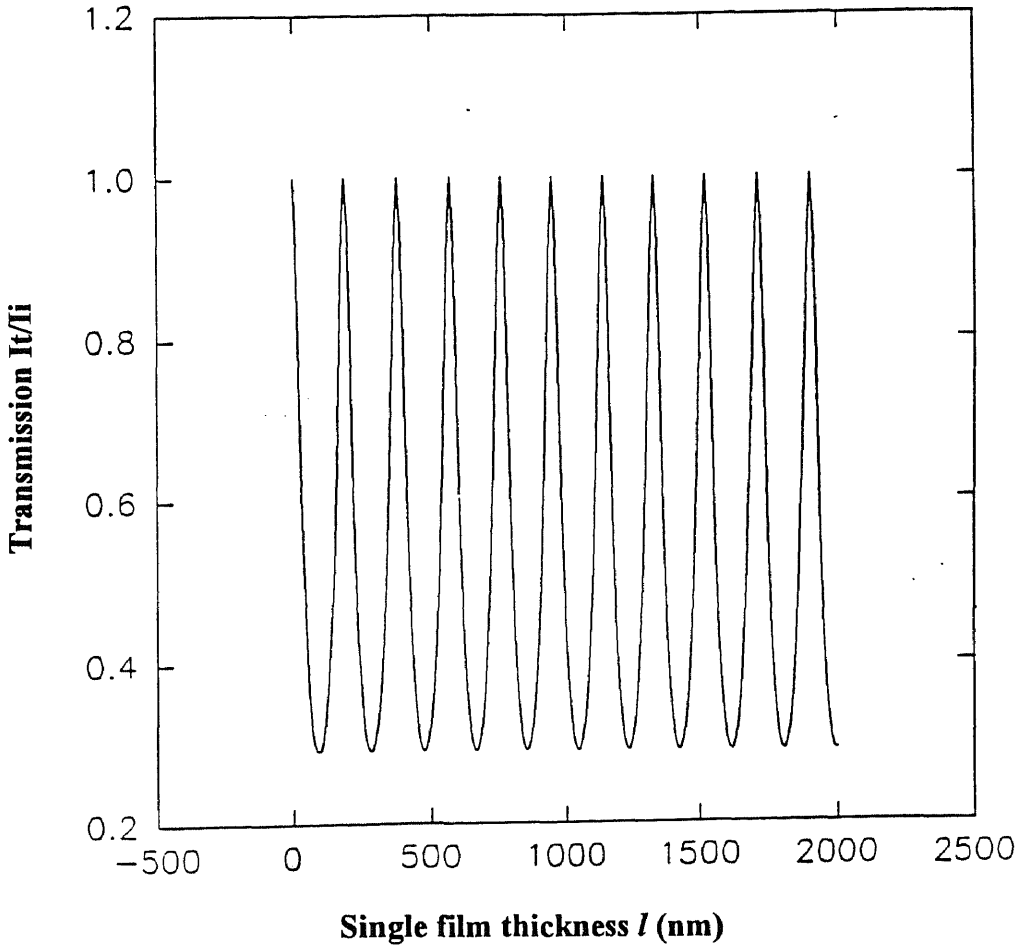


Figure 2.4b Calculated transmission characteristics of a Fabry-Perot single film etalon at 1300nm as a function of the etalon optical length with n'=1 and n=3.42 (figure 2.1). The optical length l vary from 0 to 2000nm.

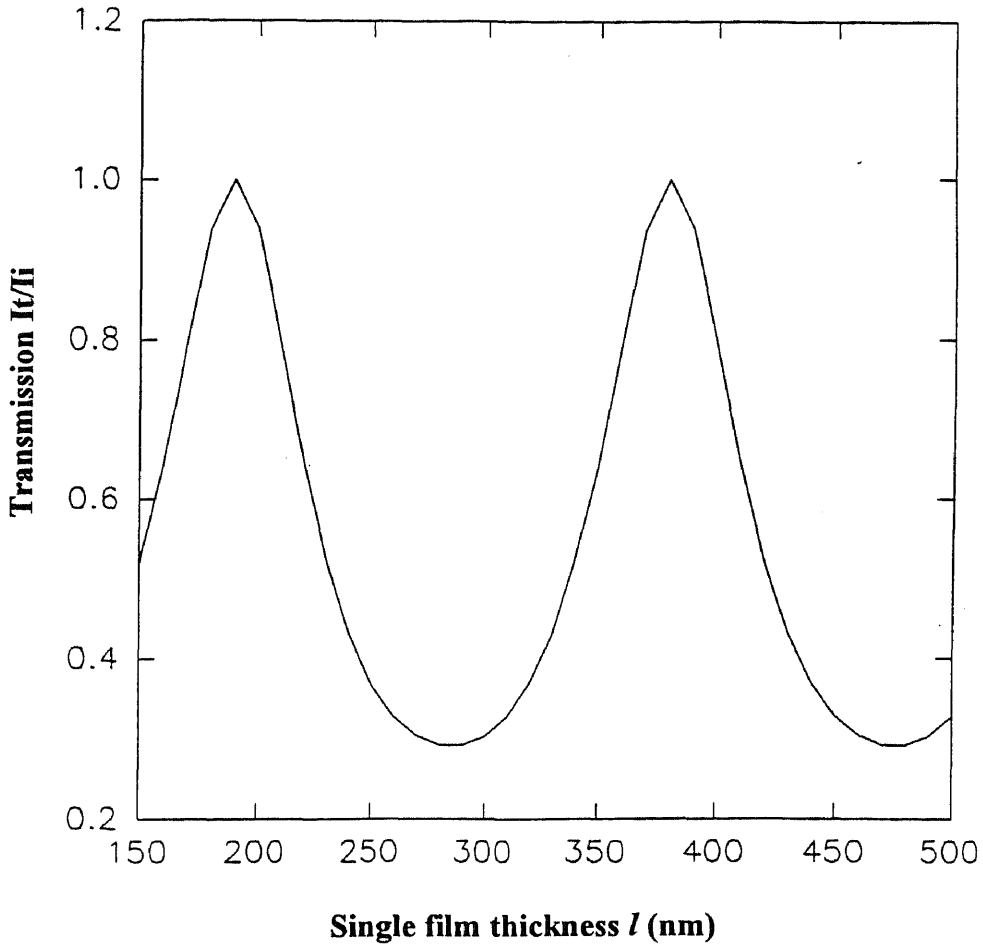


Figure 2.4c Calculated transmission characteristics of a Fabry-Perot single film etalon at 1300nm as a function of the etalon optical length with n'=1 and n=3.42 (figure 2.1). The optical length l vary from 150 to 500nm.

2.2 Previous Work

In the last years of the 19th century two young French physicists at the University of Marseilles, Alfred Perot and Charles Fabry, described a novel form of interference device. This made use of interference phenomena due to waves successively reflected between two thinly silvered plane glass plates set accurately parallel. Comparable instruments of the time were the diffraction grating which had been brought to its highest pitch in the work of Rowland, and the two beam interferometer of Michelson. All these instruments, including the grating, relied on interference. However for the Fabry-Perot etalon's advantages, real and potential. is with great clarity and vigor. Within ten years all the major applications and techniques had been introduced, largely from Marseilles, and remained standard practice for over fifty years. For the reason of precisely adjust optical length, all these instruments were made very large and heavy. Some of these instruments are shown below.

By the early 1920s the Fabry-Perot interferometer had become well established in the lab. For these years the application, apart from astrophysical measurements, would be found in isotope shifts, line broadening and shift due to source conditions, and the structure of complex lines. The basic manner of use remained essentially unchanged from Fabry and Perot's day until the invention of the laser. Apart from photoelectric recording, however, it is difficult to point to anything that had not been at least envisaged by Fabry and Perot in their early work. This perhaps may stand as the highest possible tribute to their endeavors.

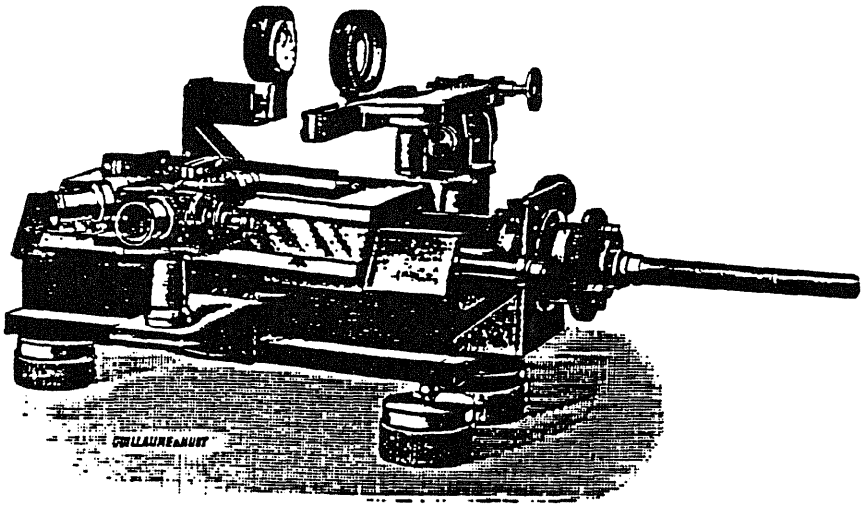


Figure 2.5 The highly engineered interferometer built by M Jobin for Fabry and Perot are described and illustrated in 1901. This is the same basic layout as the prototype instrument described in detail in 1899.

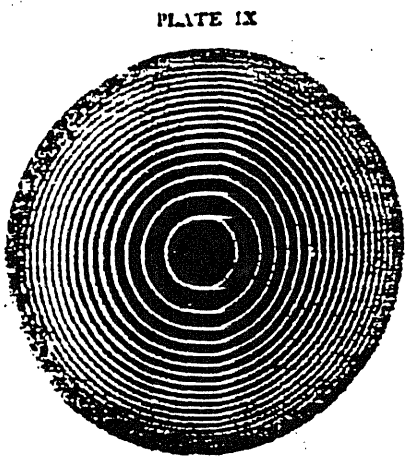


Figure 2.6 A photograph of interference rings of the green mercury line, shown by Fabry and Perot in 1901 in the *Astrophysical Journal.* The full structure of four satellite rings was lost in reproduction. This appears to be the first published record of Fabry and Perot fringes.

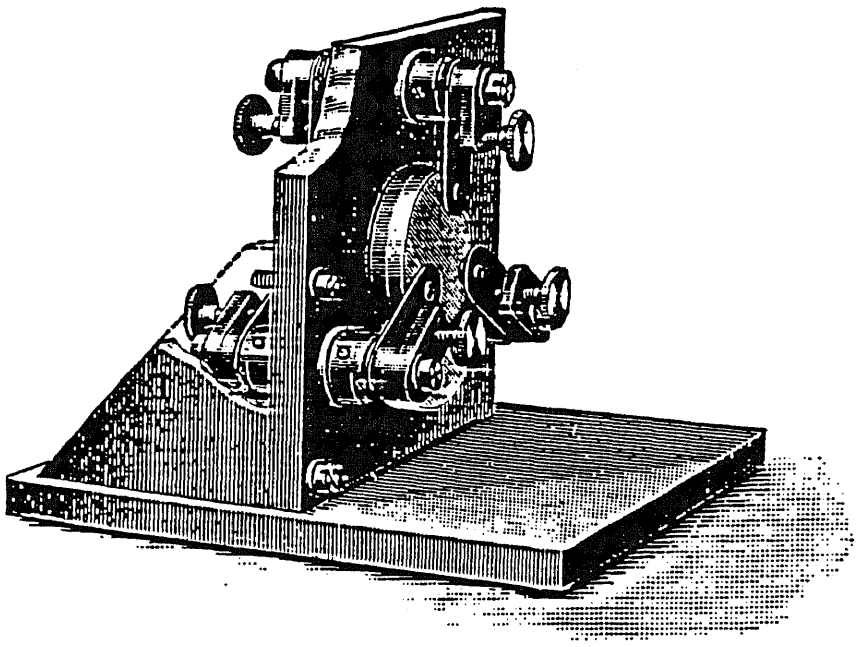


Figure 2.7 A fixed etalon or standard of thickness developed by Fabry and Perot for measurement on arc and solar lines.

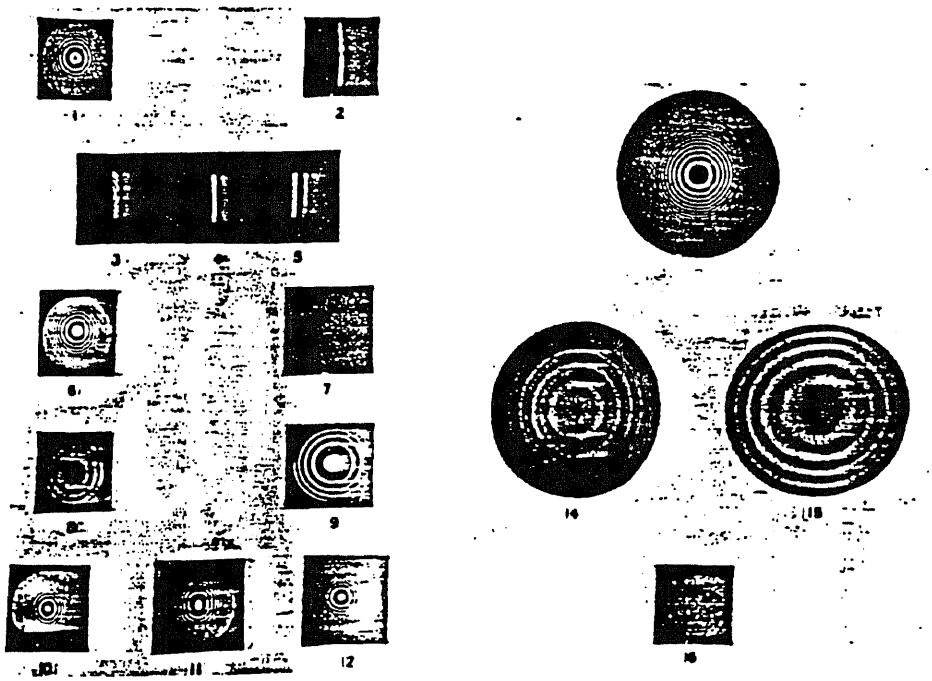


Figure 2.8 Interference fringes photographed by Barnes (1904) under various conditions of plate separation, optical arrangement and focusing of the fringe forming lens.

2.3 This Thesis Device

This thesis present the design and processing considerations of fabricating an optoelectronic reflection type modulator device basically apply Fabry-Perot etalon. The challenge is to make the etalon to micromachine scale and use electric to control the optical length of the interferometer.

In previous design, people use very heavy and large mechanical instrument to achieve the idea of control optical length. In these days the fast development of VLSI technology made it possible to shrink the scale of the etalon to micro. It is possible to control micro-sized gap between the two thin diaphragms by electrostatic force.

Figure 2.9 shows the basic idea of this thesis device. The detail will be illustrated in chapter 3 and chapter 4.

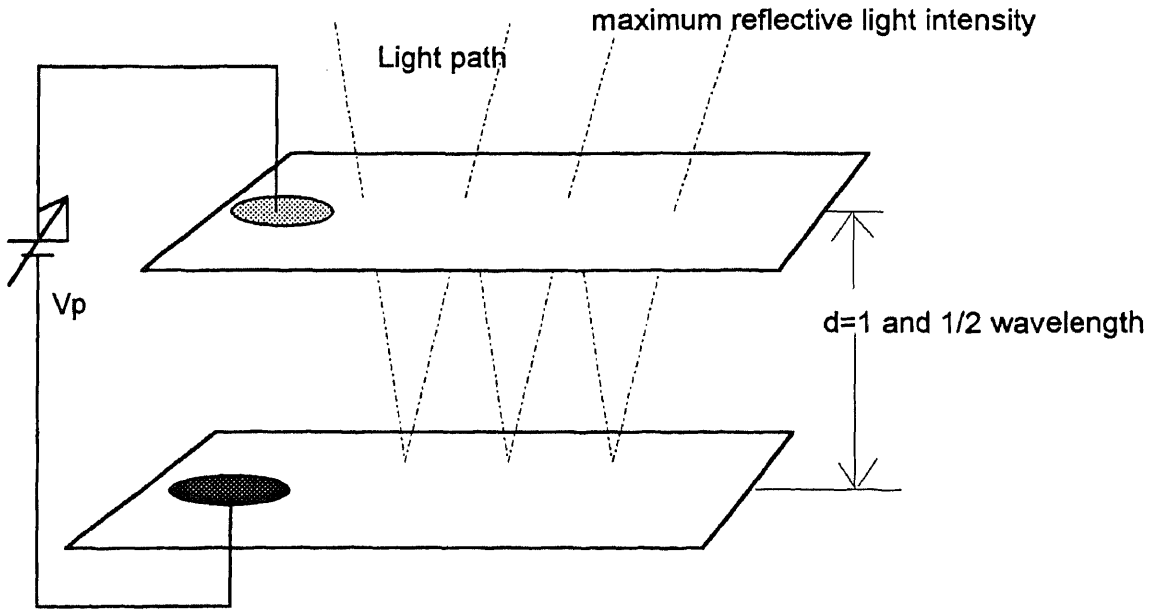


Figure 2.9 The original idea of this thesis device

CHAPTER THREE
PERFORMANCE DESIGN OF THE LIGHT MODULATOR

3.1 Introduction

The Fabry-Perot interferometer (FPI) is an optical element consisting of two partially-reflecting low-loss parallel mirrors separated by a gap. The optical reflection or transmission characteristic of such an element consists of a series of sharp resonant peaks. When the gap equals multiples of half wavelengths of primary and secondary reflection the transmission T is a maximum, and the reflectance is a minimum. These peaks are caused by wave interference between the two parallel plates. This device can operate in the a wide range of wavelengths.

Figure 3.1 shows a first-generation microscaled FPI [45][46], consisting of a similar fixed central thick silicon diaphragm, and a moveable diaphragm. The moveable diaphragm serves as the moveable mirror. Although this device demonstrated the feasibility of applying micromachining technology for Fabry-Perot etalon, the suspension characteristics of the flat diaphragm resulted in an overall die size of about 12 mm×14 mm, much too large for fiber optic modulation. The proposed structure of this thesis uses an etch-stopped corrugated diaphragm support in place of a flat diaphragm, to obtain increased linear travel and isolation from stresses and resistance to off-axis bending. Corrugated structures can be particularly useful in providing a large vertical travel with a relatively small suspension area. These corrugations are formed by etching concentric grooves in the front surface of a wafer and diffusing an etch-stop layer into the resulting non-planar surface. After etching from the back surface, the diaphragm that is formed follows the etched contour of the front surface. By using anisotropic etch for the groove formation, the corrugations can follow any desired pattern, including circular, spiral and serpentine. In this case, the grooves have straight sides with rounded corners, surrounding

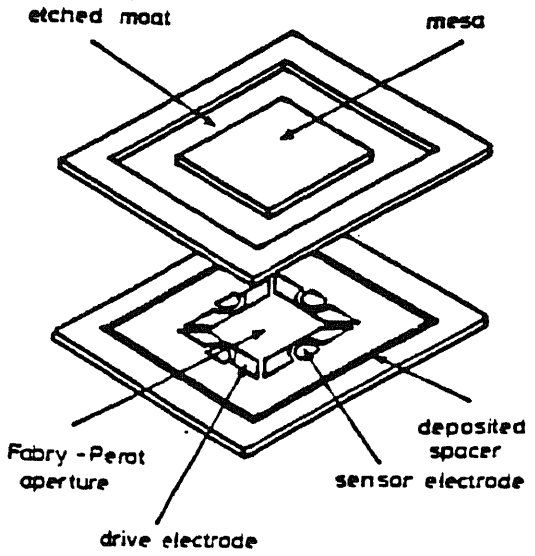


Figure 3.1 The first generation of FPI. [45][46]

a square center boss. The overall die size is 5 mm square, with a central optical cavity 1.4 mm square.

The second generation FPI [47], shown in Figure 3.2, consists of two silicon wafers, bonded together at the wafer level, and sawed into individual devices. Both wafers have highly reflective multilayer dielectric mirrors and arrays of metallic electrodes deposited on the interior devices. One wafer consists of silicon mesas surrounded by corrugated diaphragm suspensions. The other wafer has a matching set of electrodes which are uses to vary the gap in the devices electrostatically.

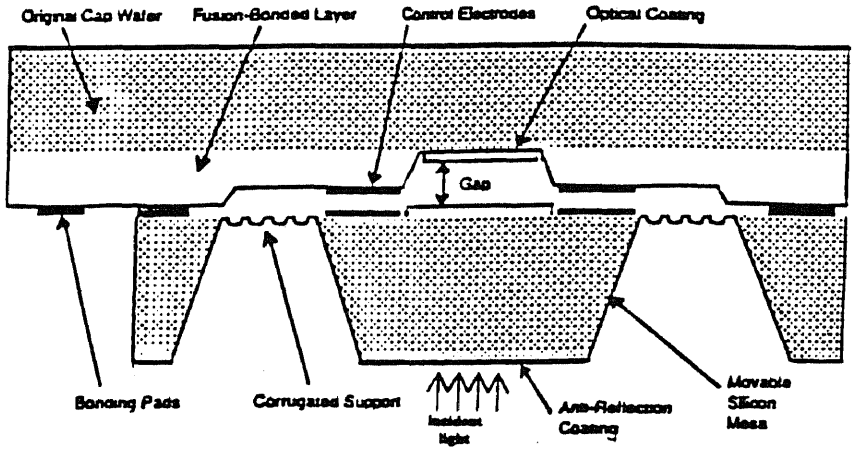


Figure 3.2 Cross-sectional schematic view of second-generation reflection type FPI. Vertical scale exaggerated for clarity. [47]

3.2 Device Geometry

The third-generation Fabry-Perot Etalon (FPI) of this thesis, shown in Figure 3.3 is fabricated entirely on a single wafer using surface micromachining technology. It has highly reflective multilayer dielectric mirrors and arrays of metallic electrodes deposited on the interior surfaces. The top side of the cavity consists of polysilicon thin film surrounded by corrugated diaphragm suspensions. The substrate side has a matching electrode which is used in conjunction with the top electrode to vary the gap electrostatically.

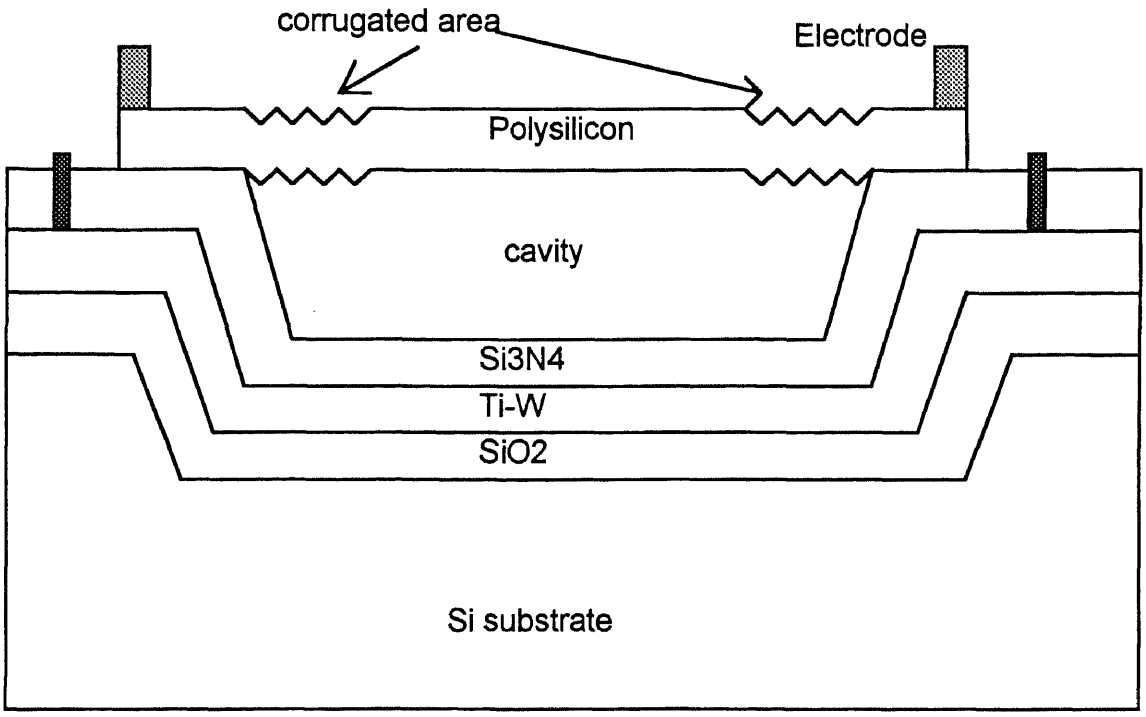


Figure 3.3 Cross-sectional schematic view of third-generation reflection type FPI. Vertical scale expanded for clarity.

This new device uses a novel technique for forming the optical gap cavity. The silicon surfaces on which the optical coatings are deposited must have high polish characteristic. This precludes the use of an etched silicon surface as the front surface of the backside mirror. The isolated layer and metallization are then deposited and patterned.

Next spin-on glass (SOG) is used as a sacrificial layer. The cap film which is a polysilicon layer is then deposited. Next, the SOG layer is sacrificially etched away to provide the desired gap of about 0.65μm. The final step is coated with optical coatings, which increasing the transparency of light intensity. The detail process is presented in chapter 4.

The quality of the optical coating is critical to the operation of the device. The coatings must have high reflectivity to provide narrow optical bandwidth, but with very low loss to provide high peak transmittance. The reflective coatings used are multilayer dielectric mirrors made up of multiple pairs of quarter wavelength layers with high and low refractive indices. A common technique is to use a relatively low-index material, such as silicon dioxide, and a higher index metallic oxide.

3.3 Electrostatic Force Model

The optical gap l is controlled by varying voltages between the two control electrodes (diaphragm cap and the substrate). The electrostatic force tends to draw the cap film towards the opposite surface reducing the cavity spacing. This motion is balanced by the elastic restoring force of the diaphragm structure. There is a pair of drive electrodes on the device. These electrodes are designed to allow not only the spacing of the cavity to be controlled, but also the parallelism of the two mirrors, maximizing the finesse of the system. Additionally, the spacing of the electrodes can be monitored capacitively. The gap between the films must be maintained to high precision. Active control of the gap is sometimes necessary to correct for the small changes in gap due by acceleration or temperature changes.

The microstructure of this device with no applied voltage has the capacitance $C_o = \varepsilon Lb / d$ in the parallel-plate approximation neglecting fringe fields. When a potential $V = E_z d$ is applied, a uniform pressure $P = \frac{\varepsilon V^2}{2d^2} = \frac{\varepsilon E_Z^2}{2}$ is created which pulls the electrodes together. The film warp caused by this pressure will be discussed in section 3.5.

3.4 Optical Transmission

The transmission of a FPI is described by the Airy function

$$T = [1 - \frac{A}{(1-R)}]^2 \{1 + [\frac{4R\sin^2(kd\cos\theta)}{(1-R)^2}]\}^{-1} \qquad [3.4\text{-}1]$$

where A= mirror absorptance, R= mirror reflectance, d= cavity gap, θ= angle of incidence of the beam, and k= 2π/λ.

The wavelength response described by the Airy function consists of a series of resonant peaks. It can be seen from equ. 3.4-1 that with kd=nπ, and with n, the order of the interference, equal to a positive integer, the transmission for normal incidence eq. 3.4-1 becomes :

$$T_{max} = [1 - \frac{A}{(1-R)}]^2 \qquad [3.4\text{-}2]$$

and the transmission intensity minimum between these peaks is given by

$$T_{min} = T_{max}[\frac{(1-R)}{(1+R)}]^2 \qquad [3.4\text{-}3]$$

The transmission peaks are separated in wavelength by $\Delta\lambda = \lambda^2/(2d)$, and this spacing is referred to as the free spectral range (FSR). Each peak has a full width at half maximum (FWHM) bandwidth given by

$$FWHM = \lambda(1-R)/n\pi\sqrt{R} \qquad [3.4\text{-}4]$$

The instrument finesse F is the ratio of the free spectral range to the FWHM linewidth. F_R is the reflection finesse given by

$$F_R = \pi\sqrt{R}\, F_R = \pi\sqrt{R}/(1-R) \qquad [3.4\text{-}6]$$

An important feature of a FPI is that the free spectral range and the FWHM bandwidth can be independently controlled. For a given wavelength, the cavity gap sets

the free spectral range and the mirror reflectivity controls the bandwidth. Thus the properties of the filter can be tailored to a particular application.

3.5 Mechanics of Corrugated Diaphragm

Most reported micromachined silicon diaphragms have been flat and either square or rectangular. These configuration have served well for piezoresistive pressure sensors for pressure ranges above 100 mmHg. For very low pressure ranges, however, the non-linearity caused by membrane stresses in a square diaphragm becomes appreciable, and other, more elaborate schemes are needed. These have primarily taken the form of bossed regions on the back side of the diaphragm to concentrate stress at the periphery for piezoresistive devices or to produce piston-like travel from the central region of the diaphragm [48]-[50]. These bossed structure offer better linearity than a non-bossed structure, but the linear deflection possible from such structure is still vary small. It has been recognized for decades in the field of conventionally formed metal diaphragms that by introducing corrugations into the diaphragm structure, the linearity of a diaphragm can be increased considerably [51]. To date only a limited amount of work has been undertaken to transfer conventional corrugated diaphragm technology to micromachined silicon structures [52]. In the present work a useful technique for forming these structures is proposed modeled to increase the linearity of this device. But, however, the corrugated structure will reduce the resonant frequency.

With the introduction of corrugations into the diaphragm structure, the device performance can be improved dramatically. For shallow, sinusoidal corrugations the deflection is approximately given by [53]:

$$\frac{PR^4}{E'h^4} = a_p \frac{y}{h} + b_p \frac{y^3}{h^3} \qquad [3.5\text{-}1]$$

where P is the applied pressure, R is the diaphram radius, h is the diaphragm thickness, E is Young's modulus, ν is poisson's ratio and y is the center deflection of the diaphragm.

$$a_p = \frac{2(q+3)(q+1)}{3(1-\frac{\nu^2}{q^2})}$$

$$b_p = \frac{165(q+1)^3(q+3)}{q^2(q+4)(q+11)(2q+1)(3q+5)} \qquad [3.5\text{-}2]$$

and

$$E' = \frac{E}{1-\nu^2} \qquad [3.5\text{-}3]$$

and for shallow, sinusoidal profiles:

$$q^2 = 1 + 1.5\frac{H^2}{h^2} \qquad [3.5\text{-}4]$$

with q is the corrugation quality factor and H is the corrugation depth. Thus q varies from 1, for a flat diaphragm, to a value that approaches 1.22 times the ratio of corrugation depth to diaphragm thickness. For conventional metal corrugated diaphragms, the value of q is typically chosen to be between 10 and 30. It is clear that the coefficient a_p increases rapidly with increases in q, while the coefficient b_p decreases rapidly with increases in q. Thus the linearity of the diaphragm can be increased dramatically by providing corrugations that are as little as three times the diaphragm thickness. In this case, q=3.8, and the linear term, a_p, is increase by about a factor of four while the cubic coefficient, b_p , is reduced by a factor of over 10.

In many useful structures it is desirable to introduce a center boss into the structure. This makes the structure stiffer for a given diaphragm thickness and corrugation depth. Small deflections of a bossed, corrugated diaphragm can be expressed as:

$$\frac{PR^4}{E'h^4} = a_p n_p \frac{y}{h} \qquad [3.5\text{-}5]$$

where

$$\frac{1}{n_p} = (1-r^4)(1-\frac{8qr^4(1-r^{q-1})(1-r^{q-3})}{(q-1)(q-3)(1-r^{2q})}) \qquad [3.5\text{-}6]$$

and r is the ratio of boss radius to diaphragm radius. This correction is less than 20% for boss ratios less than 0.4 with values of q grater than 4. It is vary significant, however, for nearly flat diaphragms with boss ratios greater than 0.3. The influence of a boss on the cubic term is somewhat more complicated; a factor similar in magnitude to n_p can be used to modify the b_p term.

There is an additional factor that needs to be considered depending on the method of fabrication of the diaphragms. The traditional approach has been to use a heavily doped boron layer as the etch stop used to form the diaphragm. It has been shown that these etch stops introduce considerable residual tension in the resulting diaphragms. For large values of initial tension the deflection of a flat diaphragm can be represented by:

$$\frac{PR^4}{E'h^4} = \frac{4\sigma R^2}{Eh^2}(\frac{y}{h}) \qquad [3.5\text{-}7]$$

where σ is the initial stress. This resistance to bending due to initial stress can be added to the terms given above using the principle of superposition to given, for a flat diaphragm:

$$\frac{PR^4}{Eh^4} = (\frac{16}{3(1-v^2)} + \frac{4\sigma R^2}{Eh^2})\frac{y}{h} + \frac{2.83}{(1-v^2)}\frac{y^3}{h^3} \qquad [3.5\text{-}8]$$

This initial tension in very heavily doped etch stops can be very great. Chau and Wise report a 3 mm square diaphragm, 1.7 μm thick, that is 600 times stiffer than a stress-free diaphragm. The use of an electrochemically etch-stopped diaphragm can produce a structure that has considerably less residual stress.

With this equation we get the followiing charts.

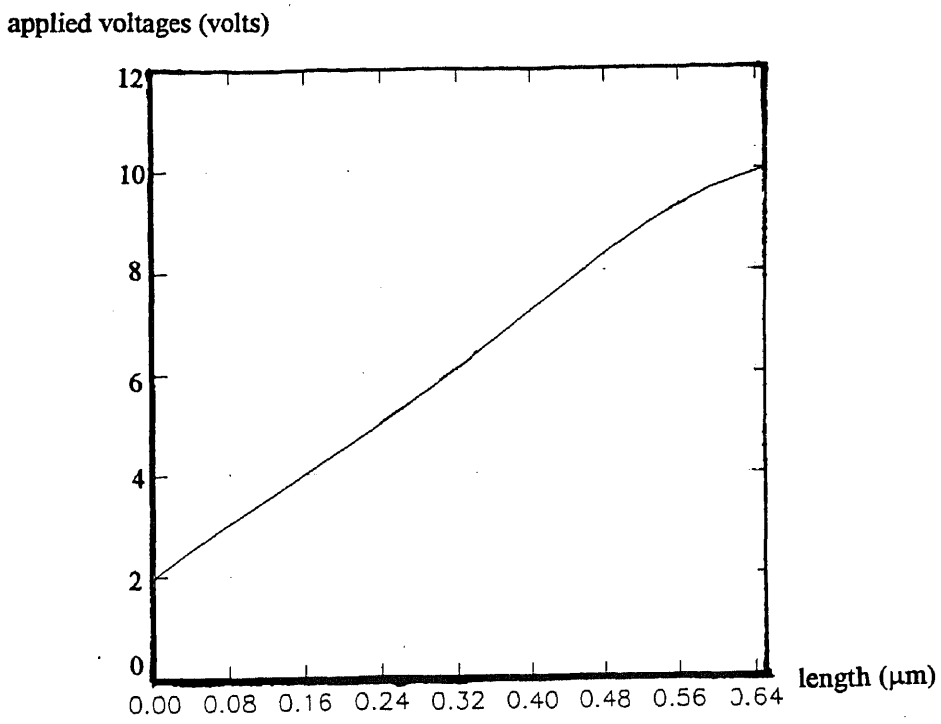


Figure3.4 Applied voltages vs. modulated lengths (with corrugation)

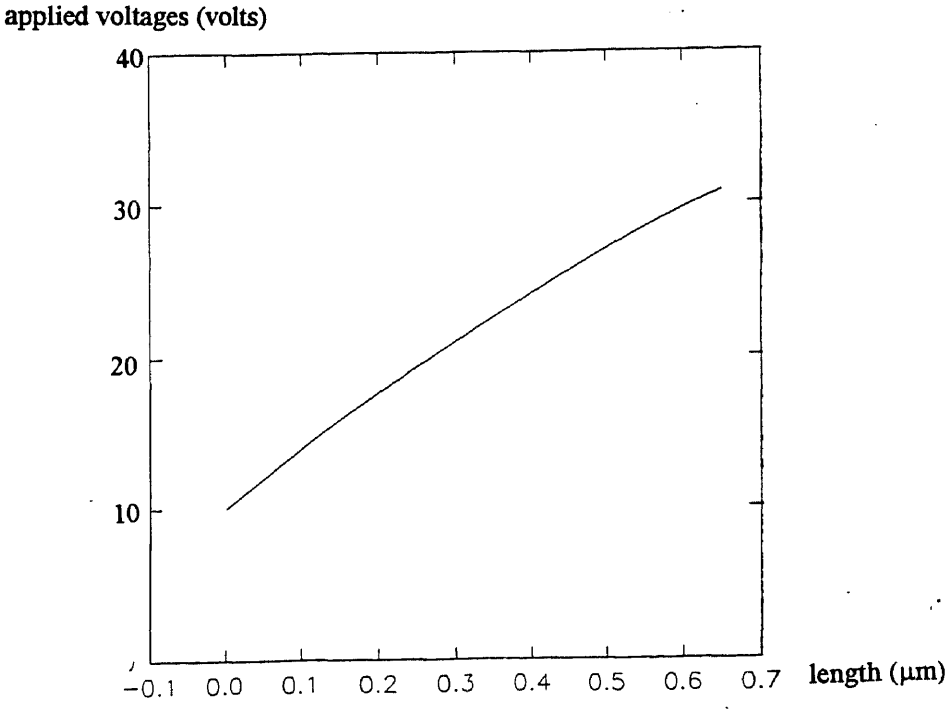


Figure3.5 Applied voltages vs. modulated lengths (without corrugation)

3.6 Results and Discussion

This device bases on the FPI but it is more complex than simple FPI. It is composed by five different layers. The overall effect is illustrated here.

Figure 3.6 shows the main working area of this device. The light incident from air through polysilicon layer, air (cavity), and silicon nitride then reflected by tungsten film and bake through the same path again. Each layers' interface will transmit reflect light intensity.

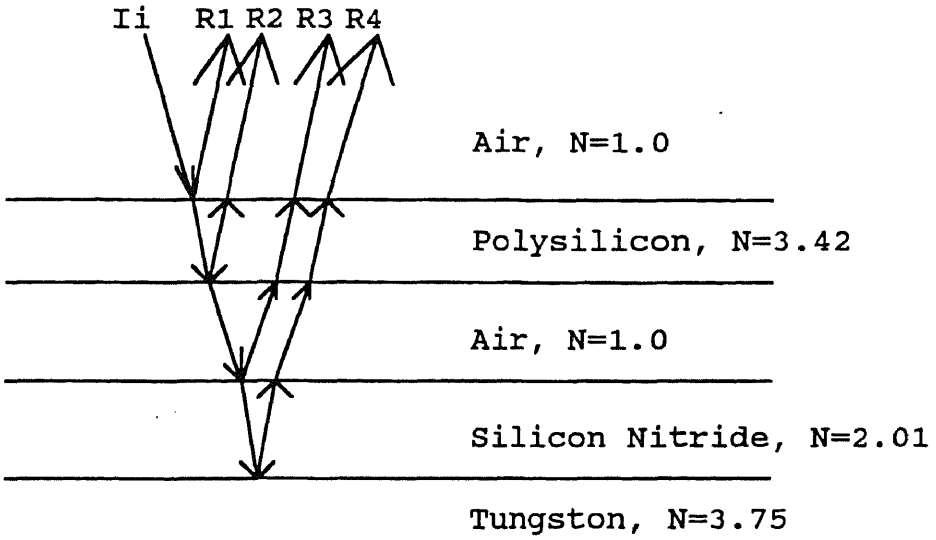


Figure 3.6 The overall light path of this device

We now consider the top sandwiches construction which is show in figure 3.7. This structure is a air-polysilicon-air structure.

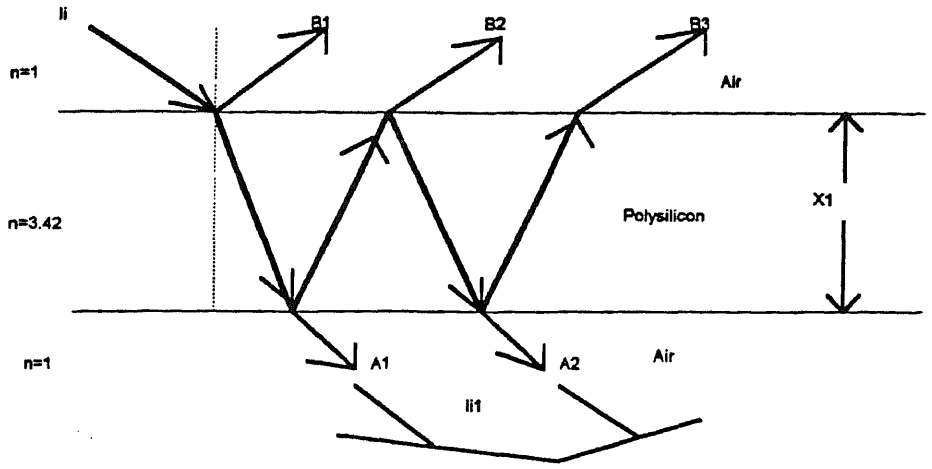


Figure 3.7 The top sandwich construction of this device

The transmission intensity of this constructure we have already discuss in chapter 2. Figure 3.8 shows the transmission characteristic. Here we pick

$$X_1 = \frac{1300\text{nm}}{3.42 \times 2} = 190.058\text{nm}$$

In this condition we can get a 98% transmission intensity, that is $I_{i1}=I_{\Sigma A}=98\%Ii$.

Even the processing error change the polysilicon thickness ±50nm. We still get 90% transmission intensition.

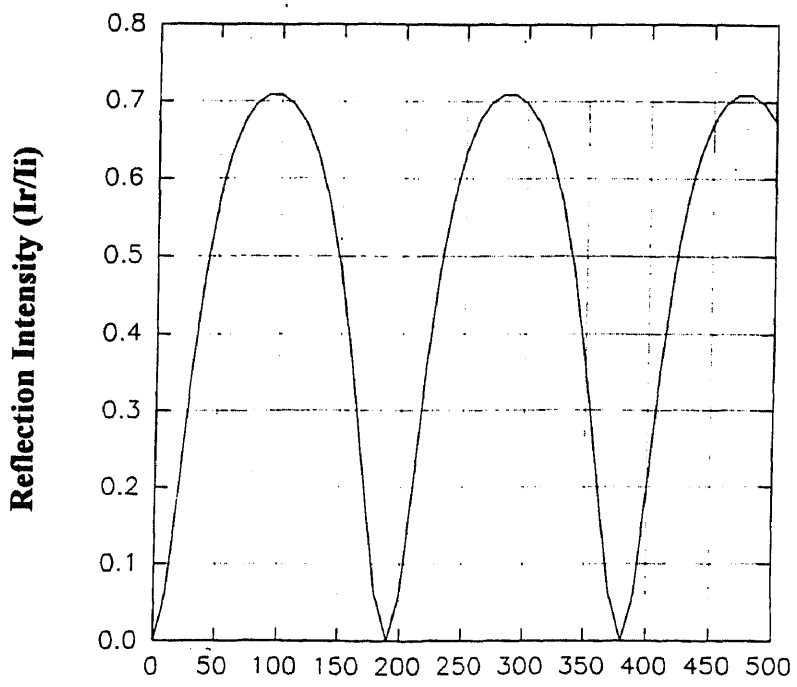


Figure 3.8 Reflection Intensity vs. Polysilicon Film Thickness (nm)

The second sandwich of this device is shown in figure 3.9. Now the complex amplitude of this incident wave is A_{I2}, then the partial reflections, R1, R2, and so forth, are given by

$$R_1 = r_1 A_{II}, \quad R_2 = t_1 t_1' r_2 A_{II} e^{i\delta}, \quad R_2 = t_1 t_1' r_2^2 r_1' A_{II} e^{2i\delta}, \ldots\ldots$$

where r_1 is the reflection coefficient of polysilicon interface, r_2 is the reflection coefficient of air and silicon nitride interface, t_1 is the transmission coefficient for waves incident from polysilicon toward air, and t_1' and r_1' are the corresponding quantities for waves traveling from air toward polysilicon. The complex amplitude of the total reflected wave is

$$A_r = R1 + R2 + \ldots\ldots = \{r + t_1 t_1' r_2 e^{i\delta}(1 + r_1 r_2 e^{i\delta} + r_1^2 r_2^2 e^{2i\delta} + \ldots\ldots)\} A_{II} \qquad [3.6\text{-}1]$$

For the transmitted wave,

$$D_1 = t_1 t_2 A_{II}, \; D_2 = t_1 t_2 r_1 r_2 e^{i\delta} A_{II}, \; D_3 = t_1 t_2 r_1'^2 r_2^2 e^{2i\delta} A_{II}, \; \ldots\ldots\ldots$$

where a phase factor exp(iδ), which corresponds to a single traversal of the plate and is common to all the terms, has been left out. Adding up the D terms, we obtain

$$A_t = A_{II} t_1 t_2 (1 + r_1' r_2 e^{i\delta} + r_1'^2 r_2^2 e^{2i\delta} + \ldots\ldots) \qquad [3.6\text{-}2]$$

for the complex amplitude of the total transmitted wave. We notice that the terms within the parentheses in [3.6-1] and [3.6-2] form an infinite geometric progression; adding them, we got

$$A_r = \frac{(1 - e^{i\delta}) r_2}{1 - r_1 r_2 e^{i\delta}} A_{II} \qquad [3.6\text{-}3]$$

and

$$A_t = \frac{t_1 t_2}{1 - r_1' r_2 e^{i\delta}} A_{II} \qquad [3.6\text{-}4]$$

where we used the fact that r'= -r.

If the incident photo intensity (watts per square meter) is taken as Ir, we obtain from (3.6-3) the following expression for the fraction of the incident intensity that is reflected:

$$\frac{I_r}{I_i} = \frac{A_r A_r^{"}}{A_{II} A_{II}^{"}} = \frac{4r_1 r_2 \sin^2(\delta/2)}{(t_1 t_2)^2 + 4r_1 r_2 \sin^2(\delta/2)} \qquad [3.6\text{-}5]$$

moreover, from [3.6-4],

$$\frac{I_t}{I_i} = \frac{A_t A_t^{"}}{A_{II} A_{II}^{"}} = \frac{(t_1 t_2)^2}{(t_1 t_2)^2 + 4r_1 r_2 \sin^2(\delta/2)} \qquad [3.6\text{-}6]$$

for the transmitted fraction. Our basic model contains no less mechanisms, so conservation of energy requires that $I_t + I_r$ be equal to I_{i2}, as is indeed the case.

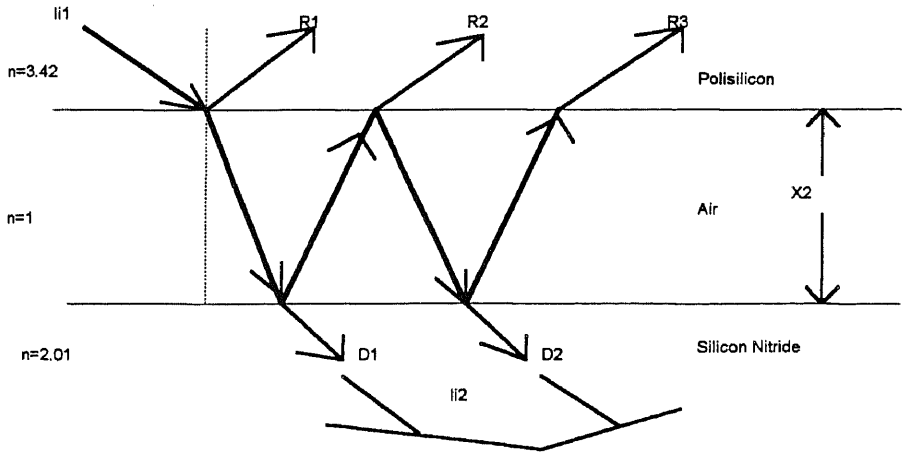


Figure 3.9 The second part construction of this device

Figure 3.10 shows the reflection characteristic. With this structure, we can get a 0.53 reflection index.

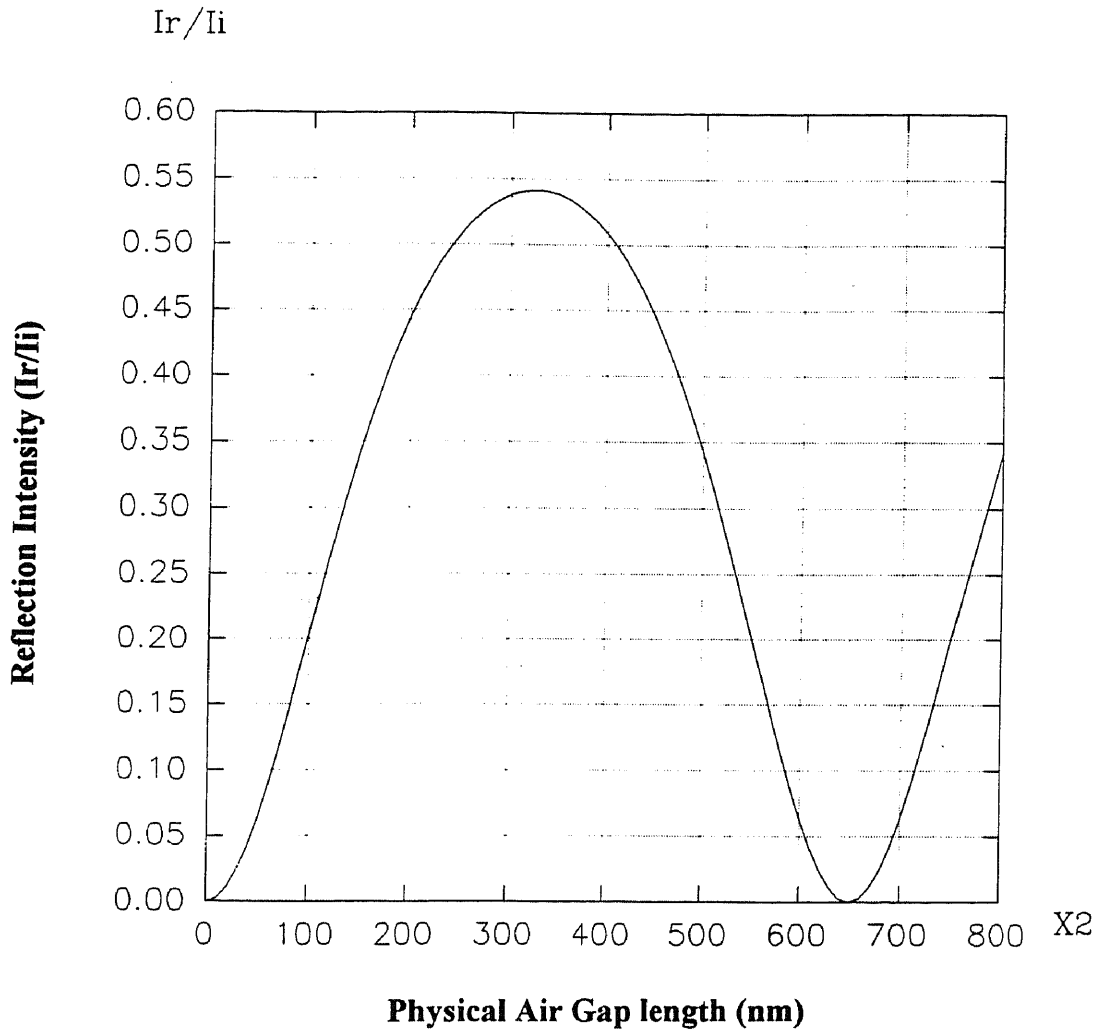


Figure 3.10 Reflection Intensity vs. Physical Air Gap Length

Now we discuss the bottom sandwich which is air-silicon nitride-tungsten construction. With a similar method we get figure 3.12 which shows the reflection characteristic of this construction. We choose X3=$\frac{1300\text{nm}}{2.01\times 2}=323.38\text{nm}$ to get a zero reflection.

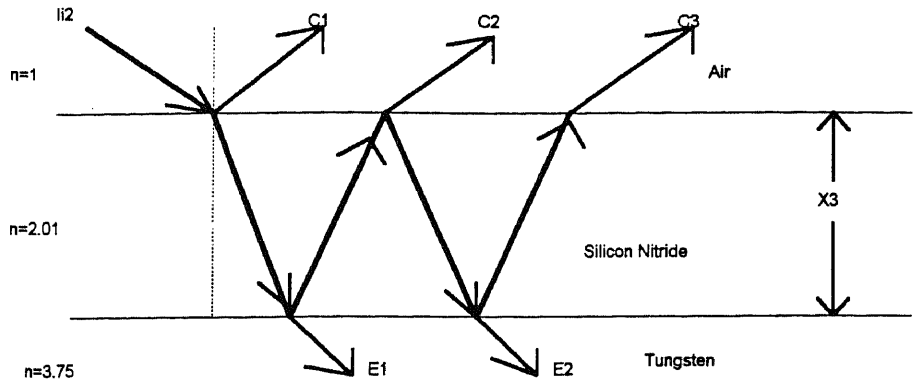


Figure 3.11 The bottom sandwich construction of this device

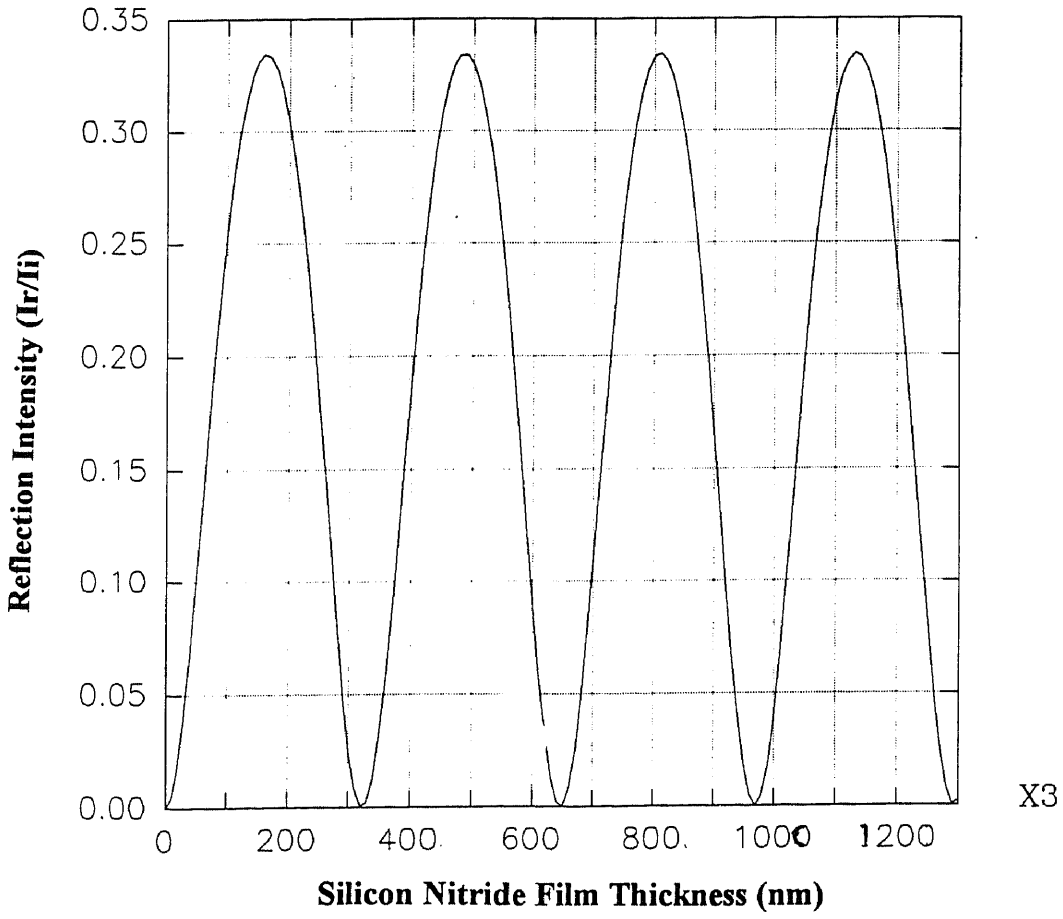


Figure 3.12 Reflection Intensity vs. Silicon Nitride Thickness

Figure 3.13 shows the overall effect of this device. From the above calculations, I_{i1}=98% I_i. We can modulate Ii so that I_{Ri2} varies from 0 to 53% of I_{i1}. The reflection intensity of the bottom sandwich is properly choose so that no reflection. The overall modulation index of this device is, if we define that

$$N_{fbi} = R_{max}\% - R_{min}\%$$

then

$$N_{fbi} = (98\% \times 53\% \times 98\%)I_i - (2\%I_i) = 48.90\%$$

and the reflection intensity is about 50% of Ii.

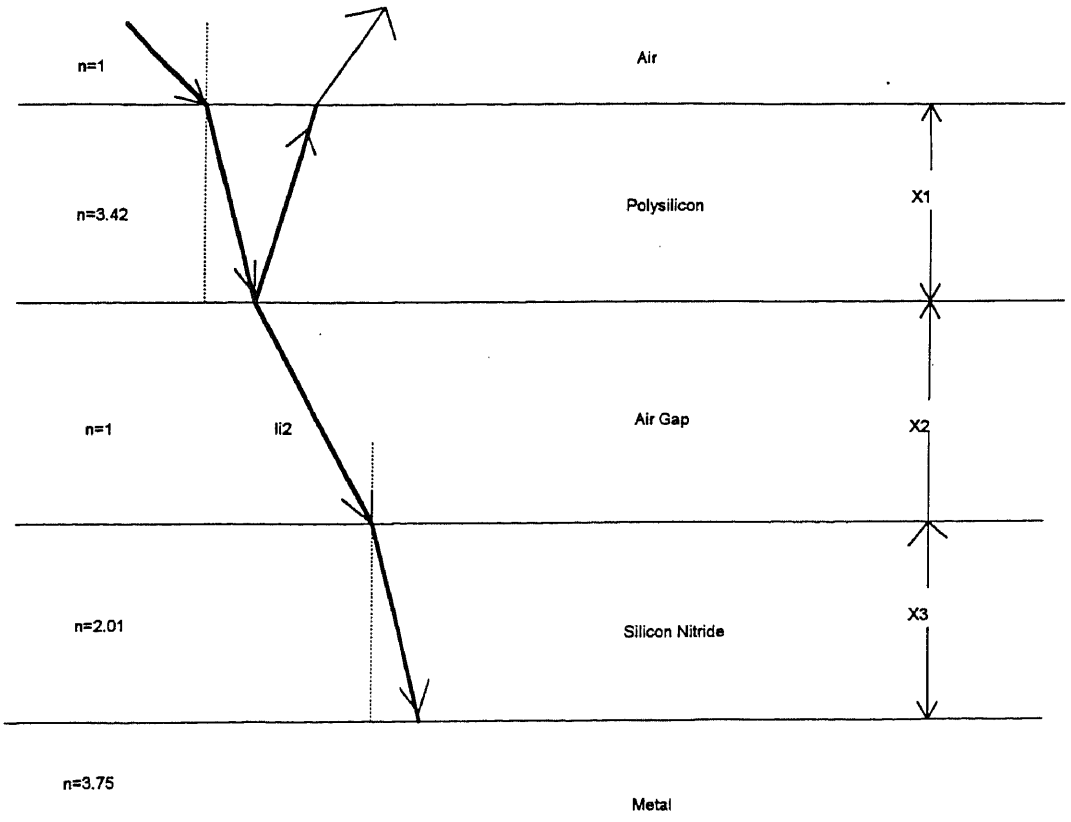


Figure 3.13 The overall effect of this device

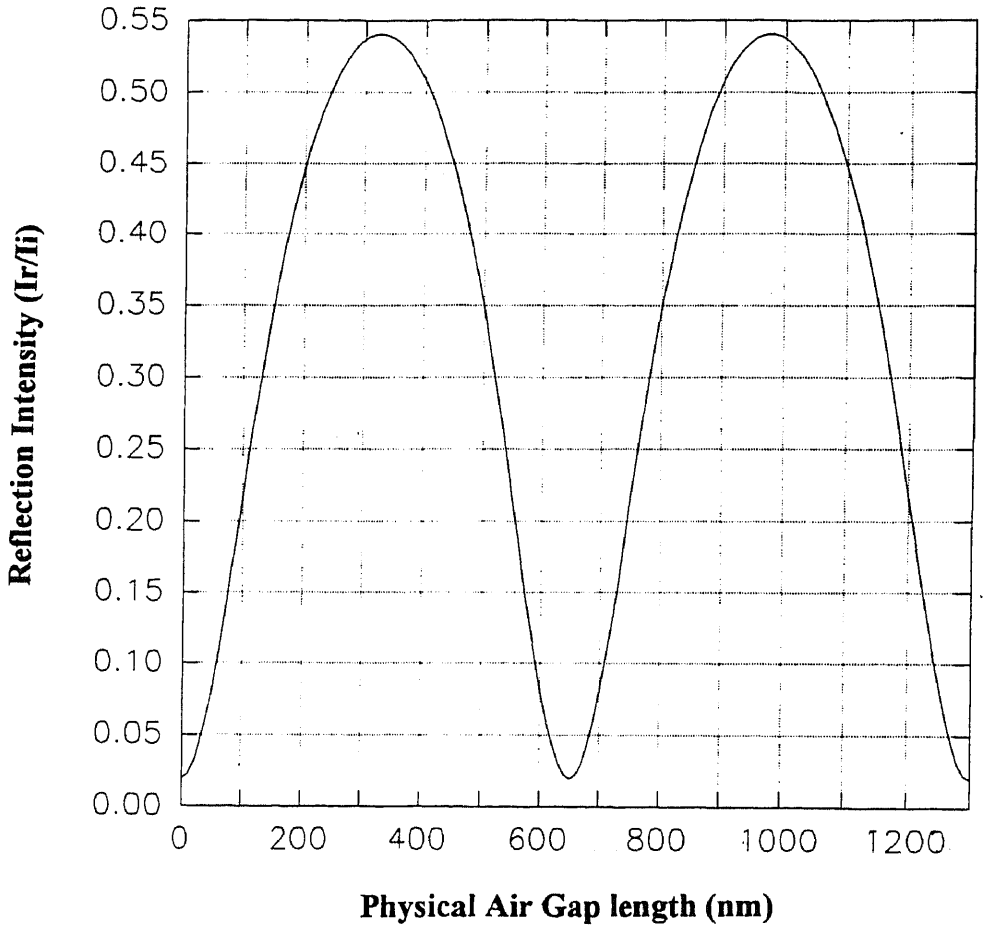


Figure 3.14 Total Reflection Intensity of this Device vs. Physical Length of Air Gap

CHAPTER 4
MASK DESIGN AND PROCESS PROCEDURE

4-1. Device Structure

A top view of the device design in this thesis is shown in figure 4.1. In this figure the cavity underlies the diaphragm and corrugated structure. A cross section is shown in fig. 4.2. This device is fabricated within a single silicon wafer. The process uses six masks.

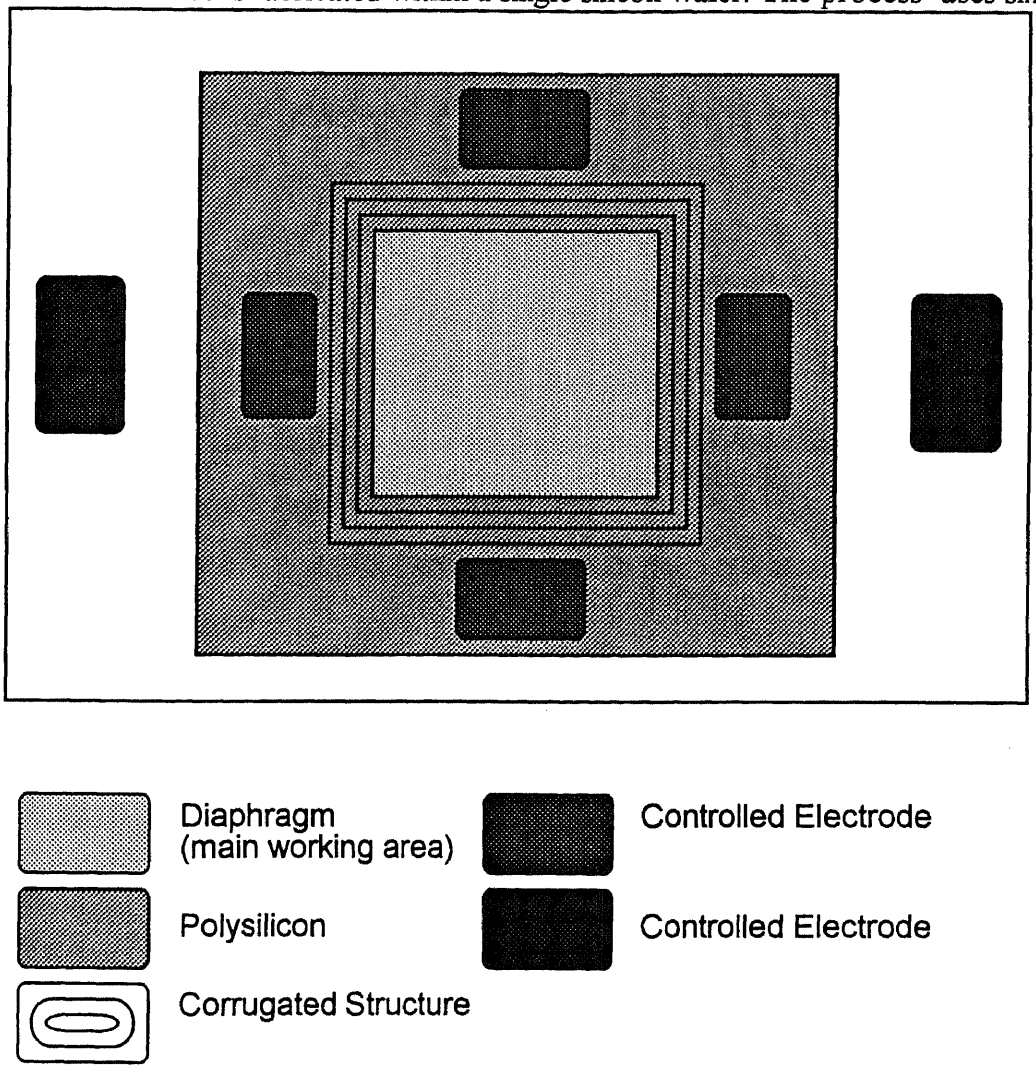


Figure 4.1 A top view of the full diaphragm region showing the corrugated structure

The third-generation Fably-Perot etalon (FPI) of this thesis, shown in Figure 4.1, contains a single cavity structure. It has highly reflective multilayer dielectric mirrors and metallic electrodes that are surface machined. The top side of the cavity consists of a polysilicon thin film surrounded by corrugated diaphragm suspensions. The bottom or lower side has a fixed position metal film which is used for electrostatic actuation.

This new device uses a novel technique for forming the initial optical gap which is the depth of the cavity. The silicon surfaces on which the optical coatings are deposited must be equivalent in surface finish to unprocessed silicon wafers. This precludes the use of an etched silicon surface as the mirror surface, the isolated layer and metallization are then deposited and patterned. Spin-on glass is used as a sacrificial layer to create the cavity. The polysilicon cap film is then deposited. After that the sacrificial layer is etched down to the desired gap width of approx. 1μm. In the final processing step, the diaphragm is coated with optical coatings, thereby increasing the transparency for a incident light. The detail process will be discussed in chapter 4.3. Figure 4.3 shows the process flow of this device fabrication.

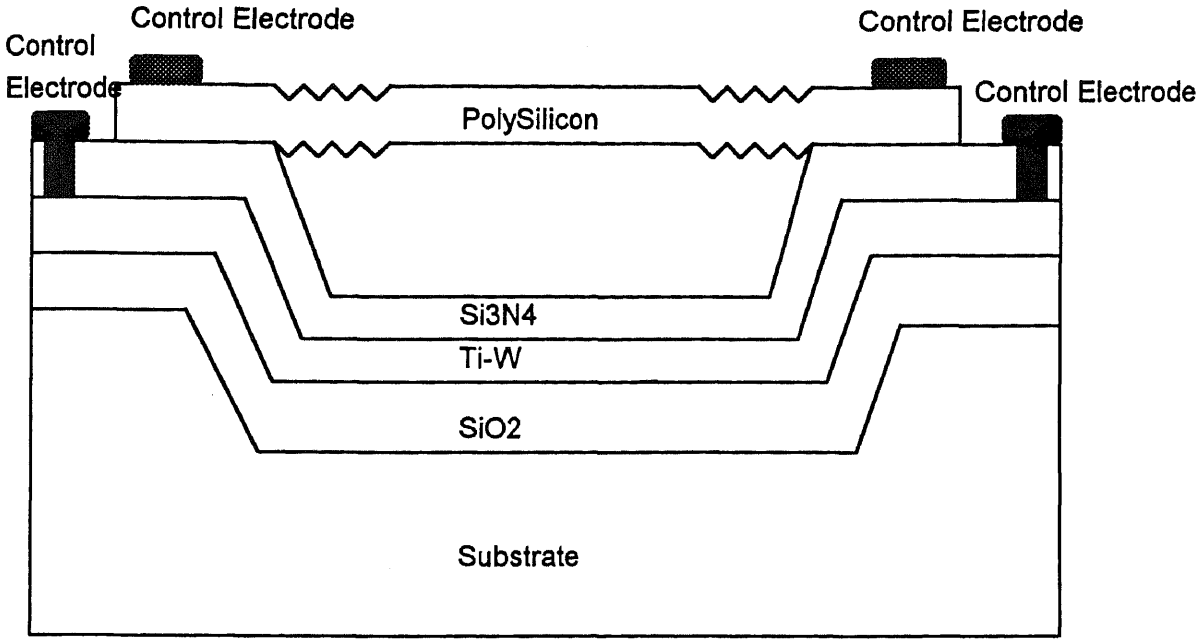
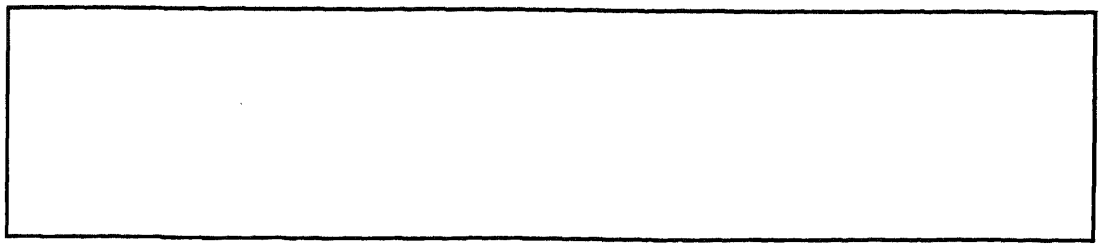
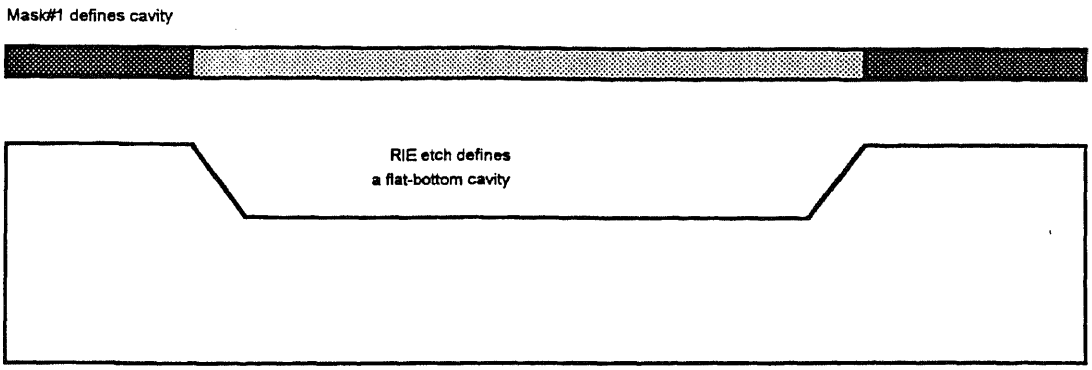


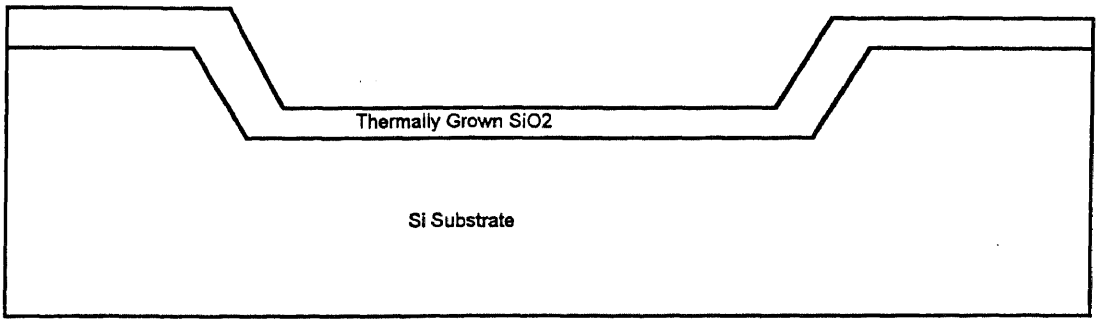
Figure 4.2 Cross-sectional schematic view of third-generation FPI. Vertical scale exaggerated for clarity.



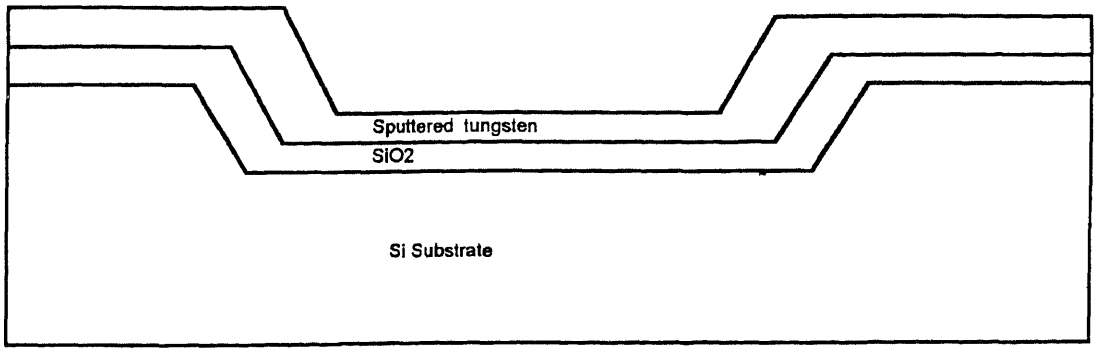
1.Starting material (silicon wafer with [100] direction)



2. RIE etch define a flat-bottom cavity

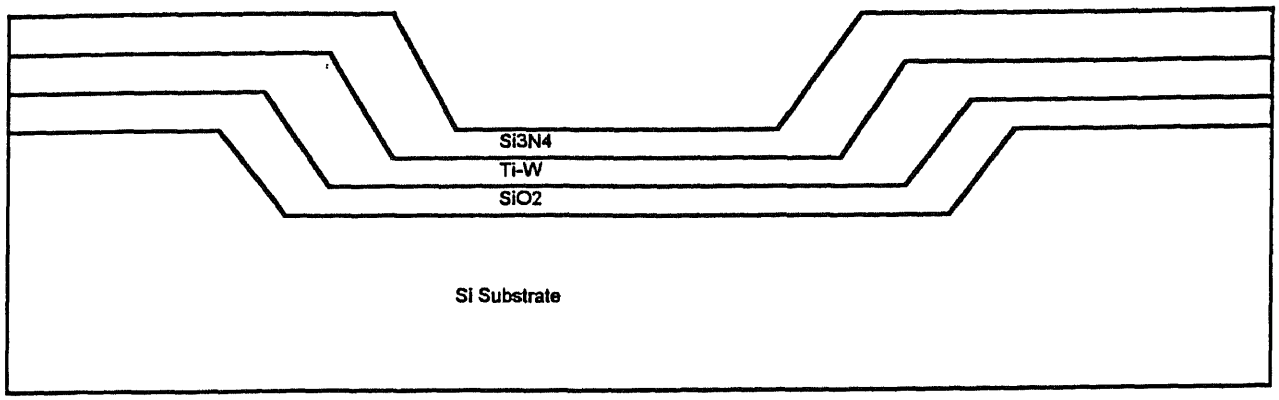


3. Deposit SiO_2 as an isolated layer between substrate and metal layer

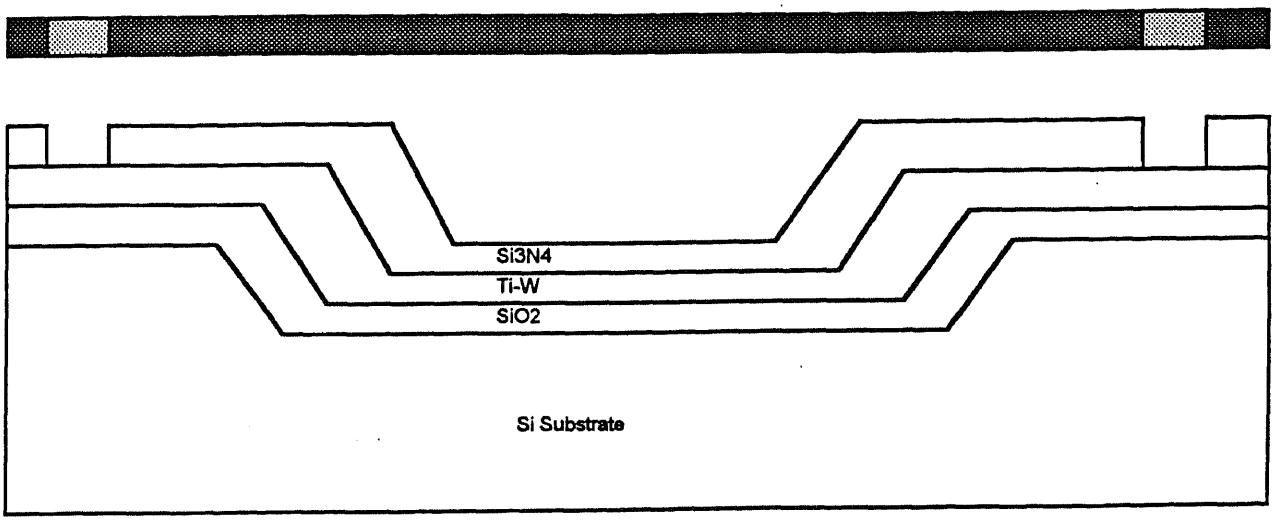


4. Sputter tungsten as a mirror surface

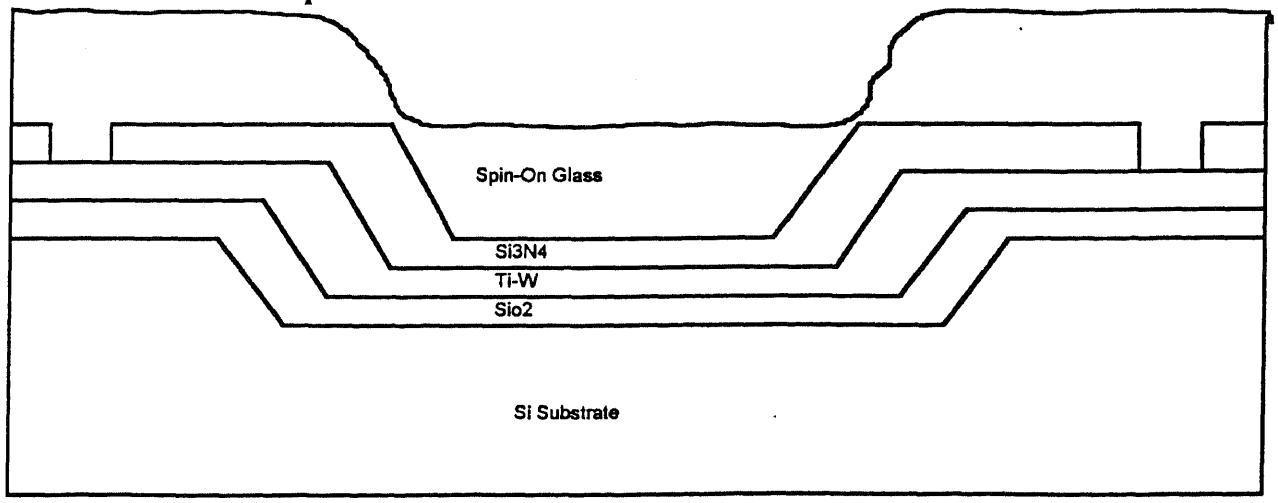
Figure 4.3a The process flow of this device fabrication



5. LPCVD Si_3N_4

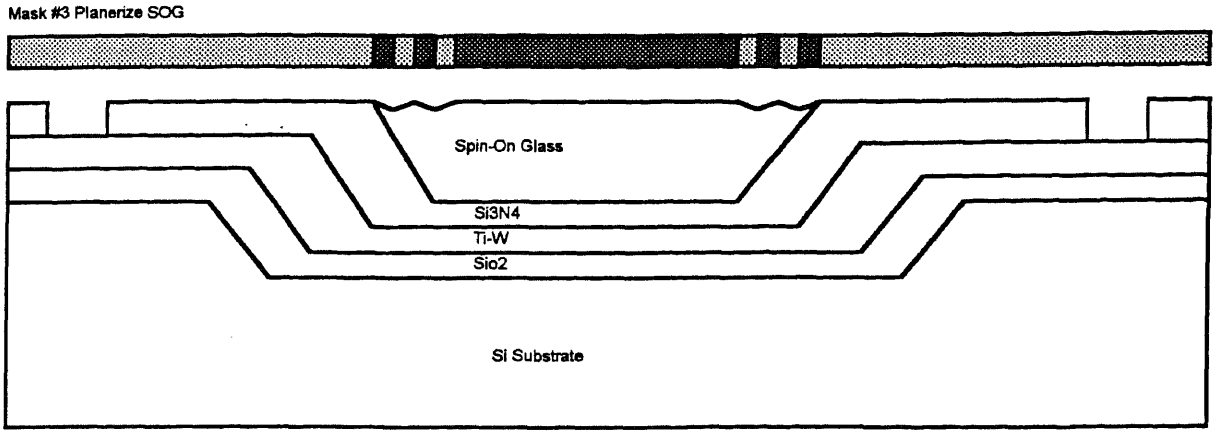


6. Open windows for contact to the buried electrode

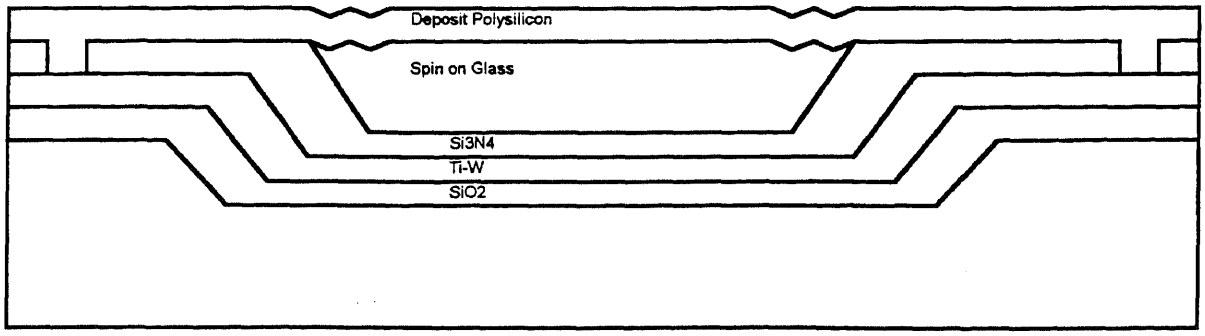


7. Spin-on glass as a sacrificial layer

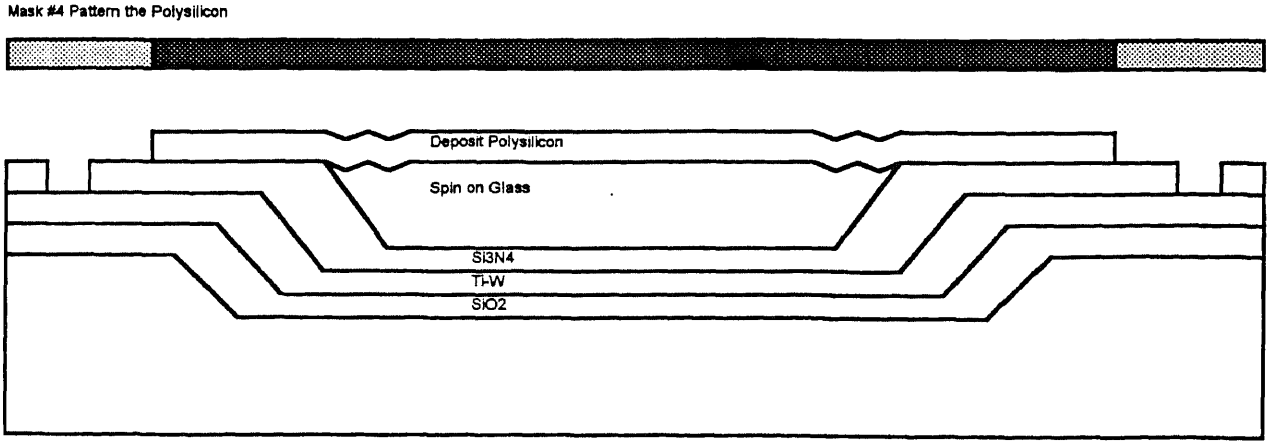
Figure 4.3b The process flow of this device fabrication



8. Planerize spin-on glass

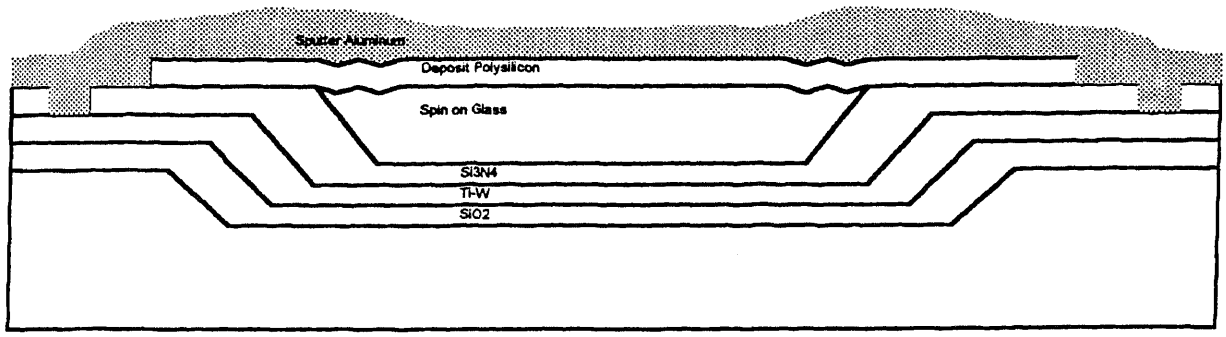


9. Deposited polysilicon



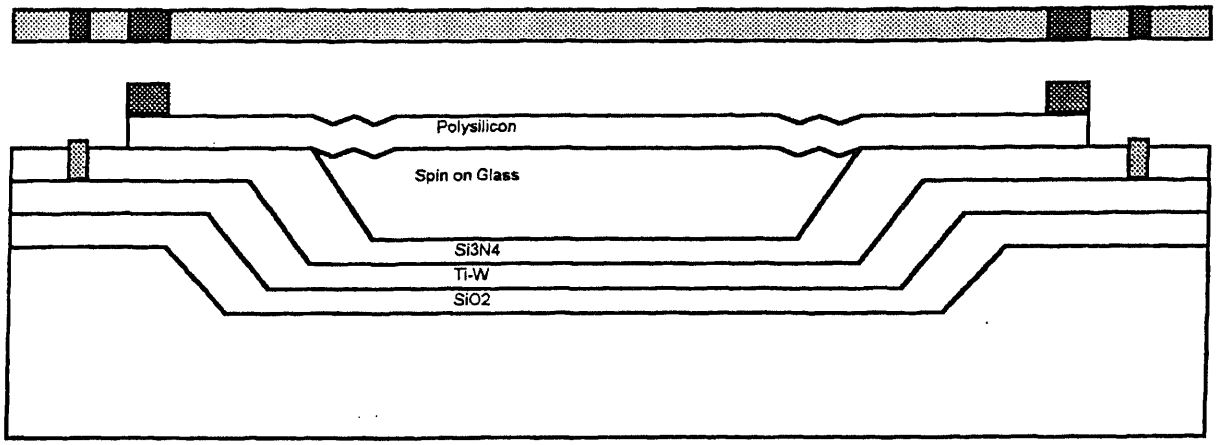
10. Pattern the polysilicon layer

Figure 4.3c The process flow of this device fabrication (cont)

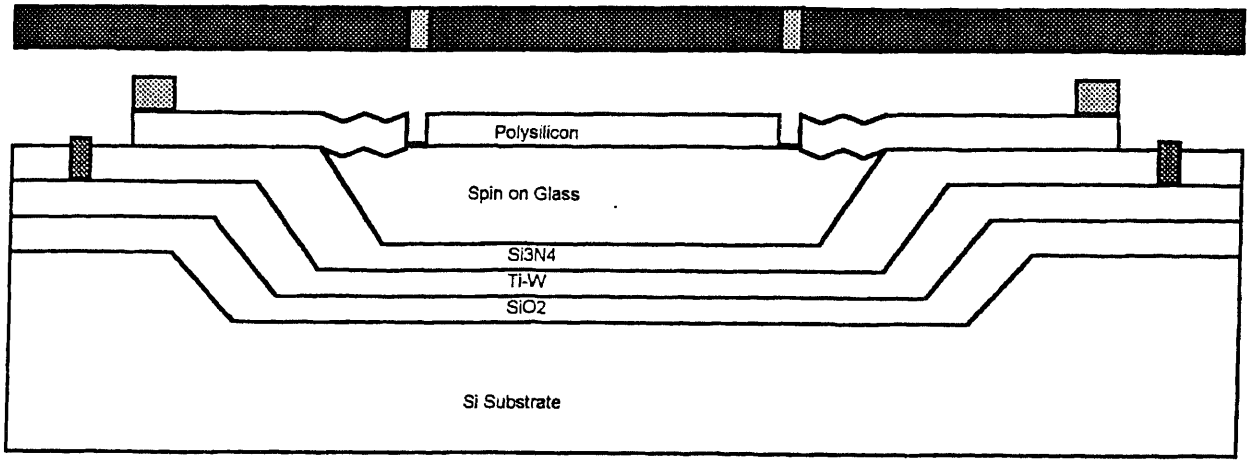


11. Sputter Aluminum as bonding pad

Mask #5 Aluminum Removal

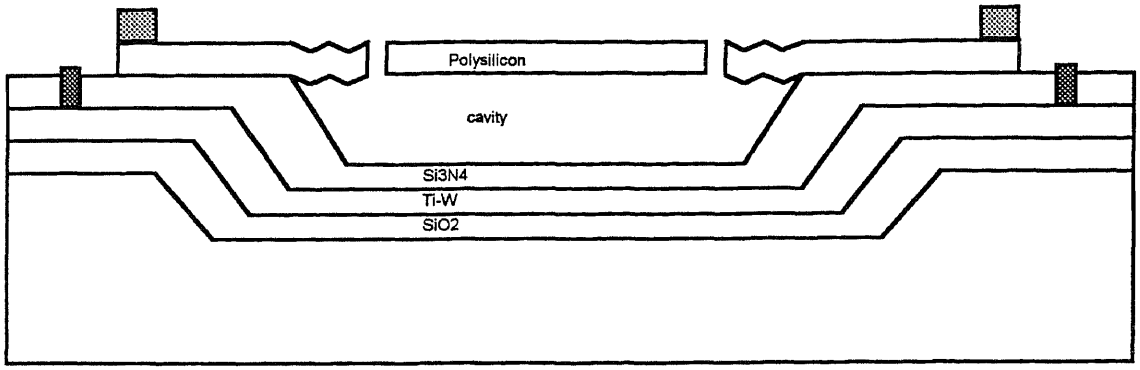


12. Aluminum Removal



13. Etch small holes for the etchants coming into the cavity

Figure 4.3d The process flow of this device fabrication



14. Etch out the cavity

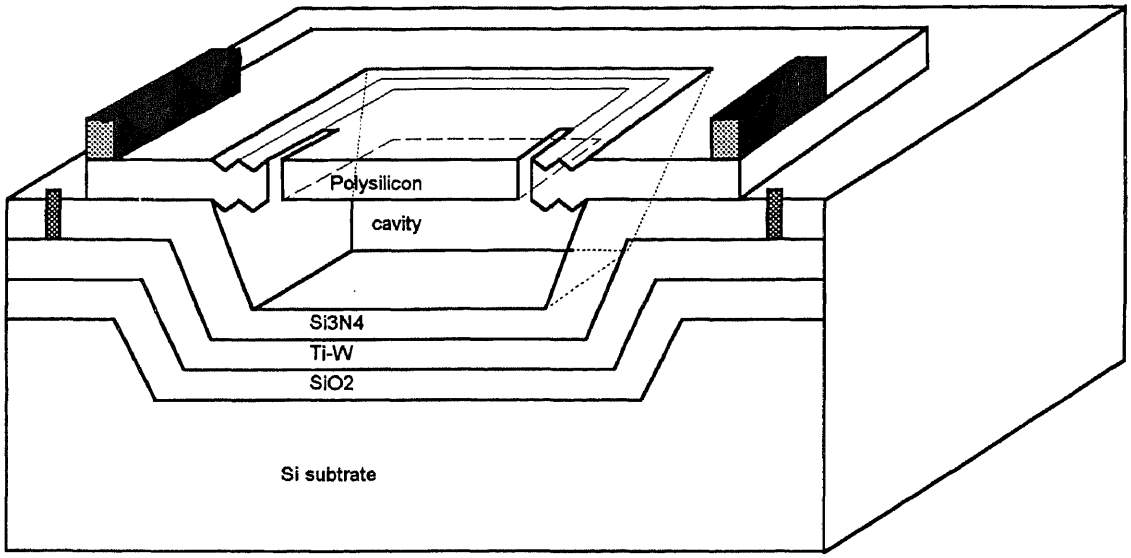


Figure 4.3e process flow of this device fabrication

4-2. Mask Design

Physical layouts of the 6 mask levels are in Appendix A. Figure 4.4(a) to (f) shows the typical device mask layout.

In this third generation FPI, six masks are needed for fabrication. These mask levels are :

Mask #1: Define the cavity

We apply this mask (figure 4.4(a)) in the very first step. The area of the cavity is the mean working area. For experimental testing, three different sizes were designed to get the best effect, they are 100×100 μm, 200×200 μm, and 500×500 μm. Fields are specified for positive photoresist.

Mask #2 Contact to the buried electrode

Two electrodes on each side of the cavity provide the electrostatic actuation. The top electrode is the cap film that is doped polysilicon film. The other side is a tungsten reflective metal film. The isolator film between these two electrodes is silicon nitride. Mask #2 is shown in figure 4.4(b) which is a light field mask.

Mask #3 Planerize Spin-On Glass

The cavity of this device is fabricated through a sacrificial layer process. The material which is used for the sacrificial layer is SOG. The SOG is applied by a spin-on process. The SOG will cover the entire wafer. This mask is used to remove the SOG from areas outside of the cavity. Additionally, this mask contains structures to define the corrugation of the diaphragm. Mask #3 is shown in figure 4.4(c) which is a light field mask.

Mask #4 Pattern the Polysilicon

This mask exposes the bonding pad which contacts the lower electrode. This opens the polysilicon to expose the under lying metal. Figure 4.4(d) shows mask #4 which is a dark field mask.

Mask #5 Aluminum Removal

The device should be connect to the outside world. We use aluminum as the "wire" in the device, then use it to wire bonding. This mask is for the aluminum removal. The left area is the electrodes. They connect the electrode to the outside world.(Figure 4.4(e))

Mask #6 Etch small hole in polysilicon

The sacrificial layer is released as a final process stop. This mask opens an etch window through the polysilicon. These holes should not be too large to effect the light reflection and transmission (or, effect the result as little as possible). Several different hole diameters and positions designs are used to get the best result. These holes also cannot be too small, otherwise the time for the cavity release will be too long. (Figure 4.4(f))

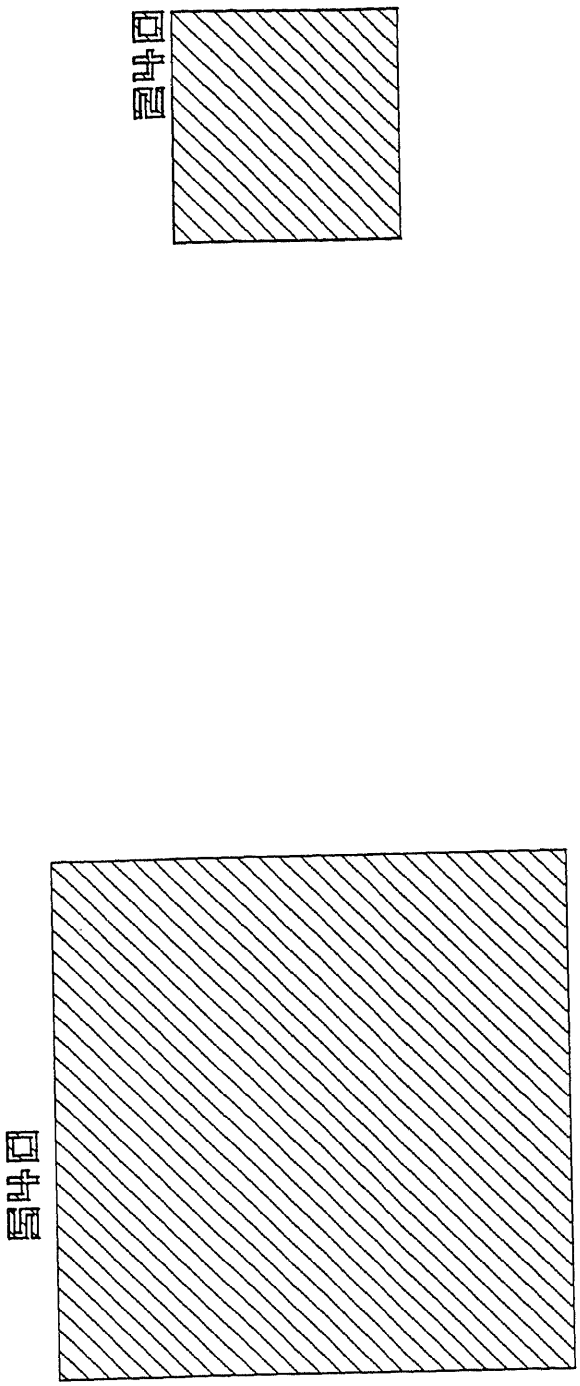


Figure 4.4(a) Mask #1 Define the cavity

Figure 4.4(b) Mask #2 Contact to the buried electrode

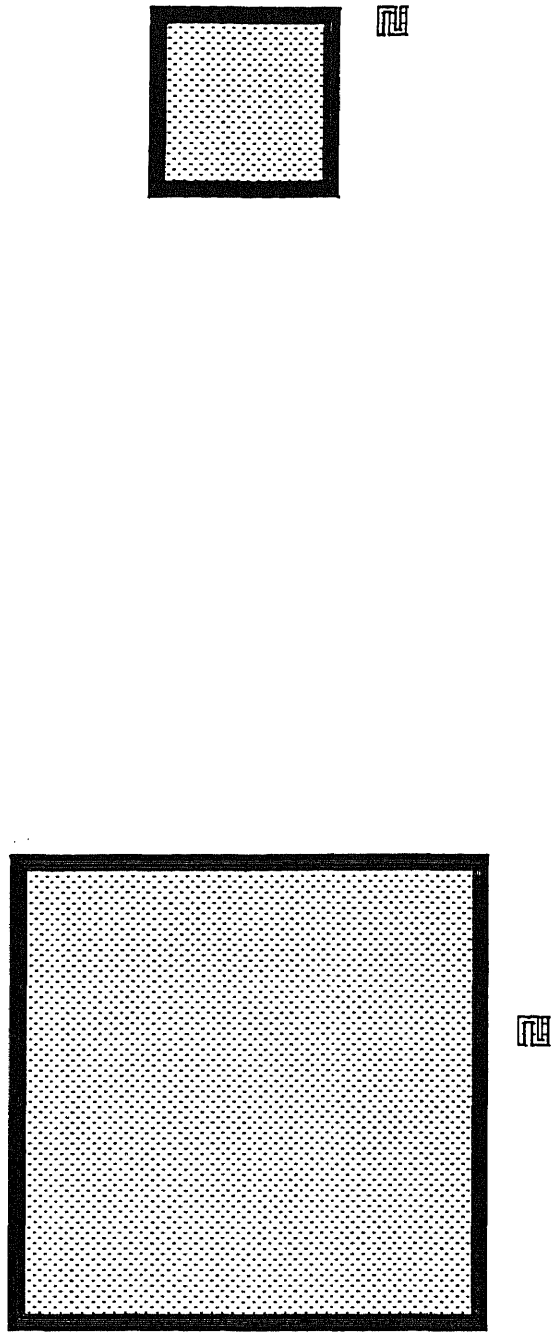


Figure 4.4(c) Mask #3 Planerize Spin-on glass

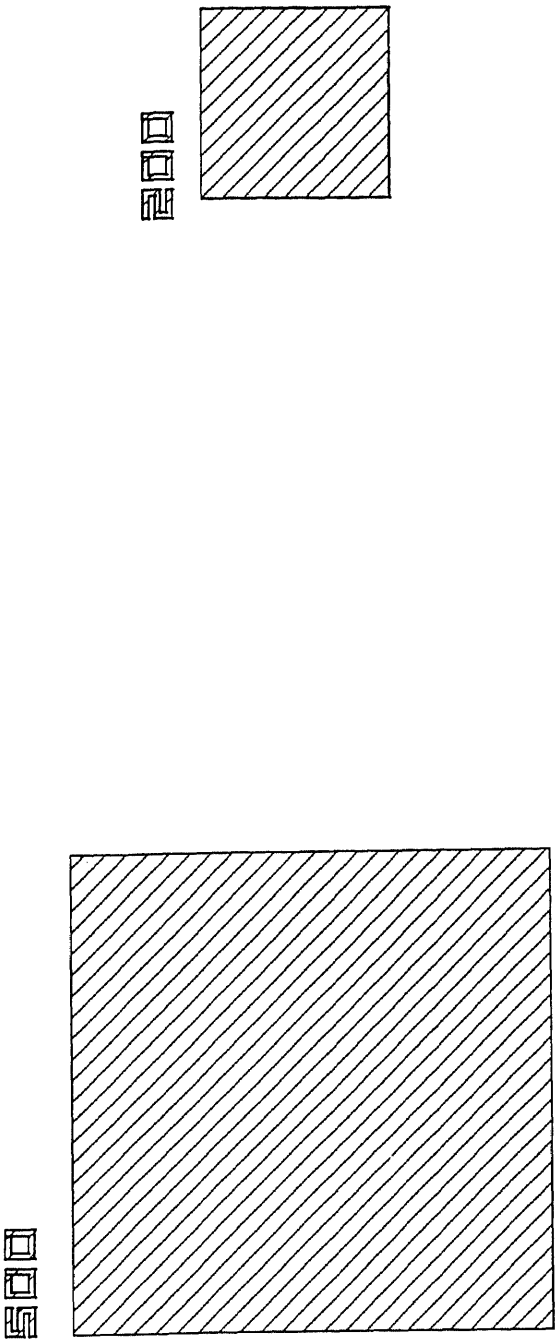


Figure 4.4(d) Mask #4 Pattern the polysilicon

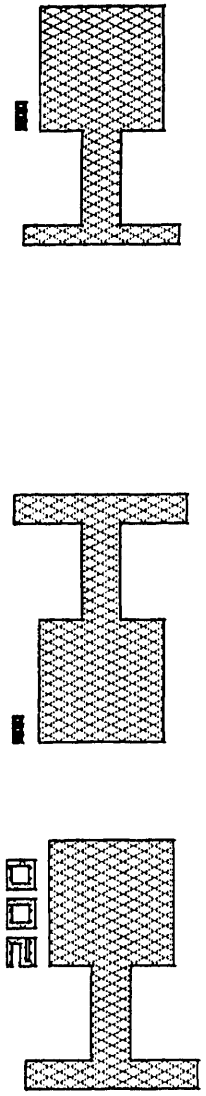


Figure 4.4(e) Mask #5 Aluminum removal

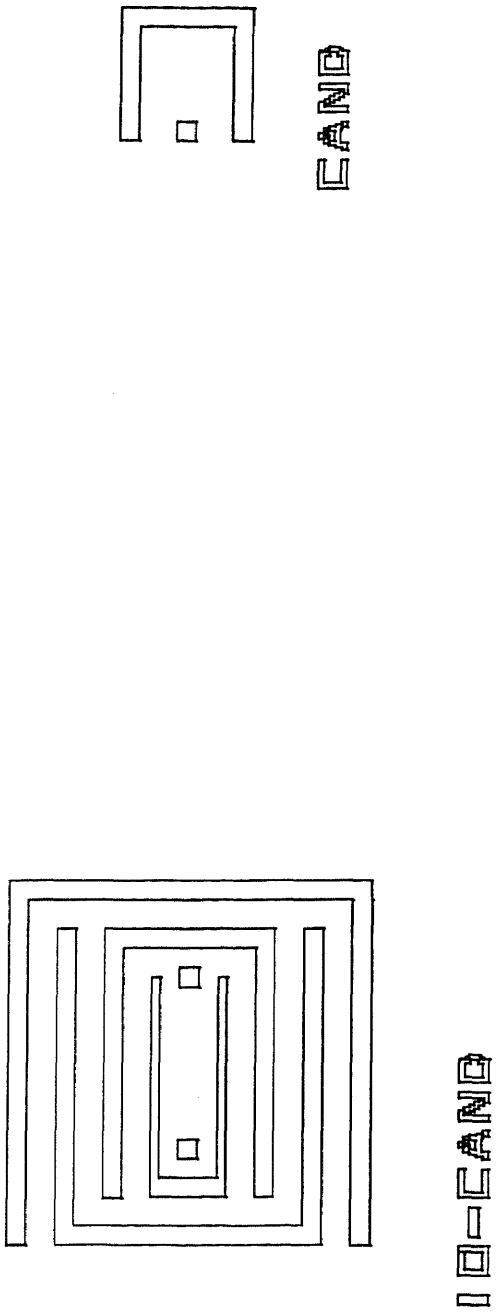


Figure 4.4(f) Mask #6 Etch small hole in polysilicon

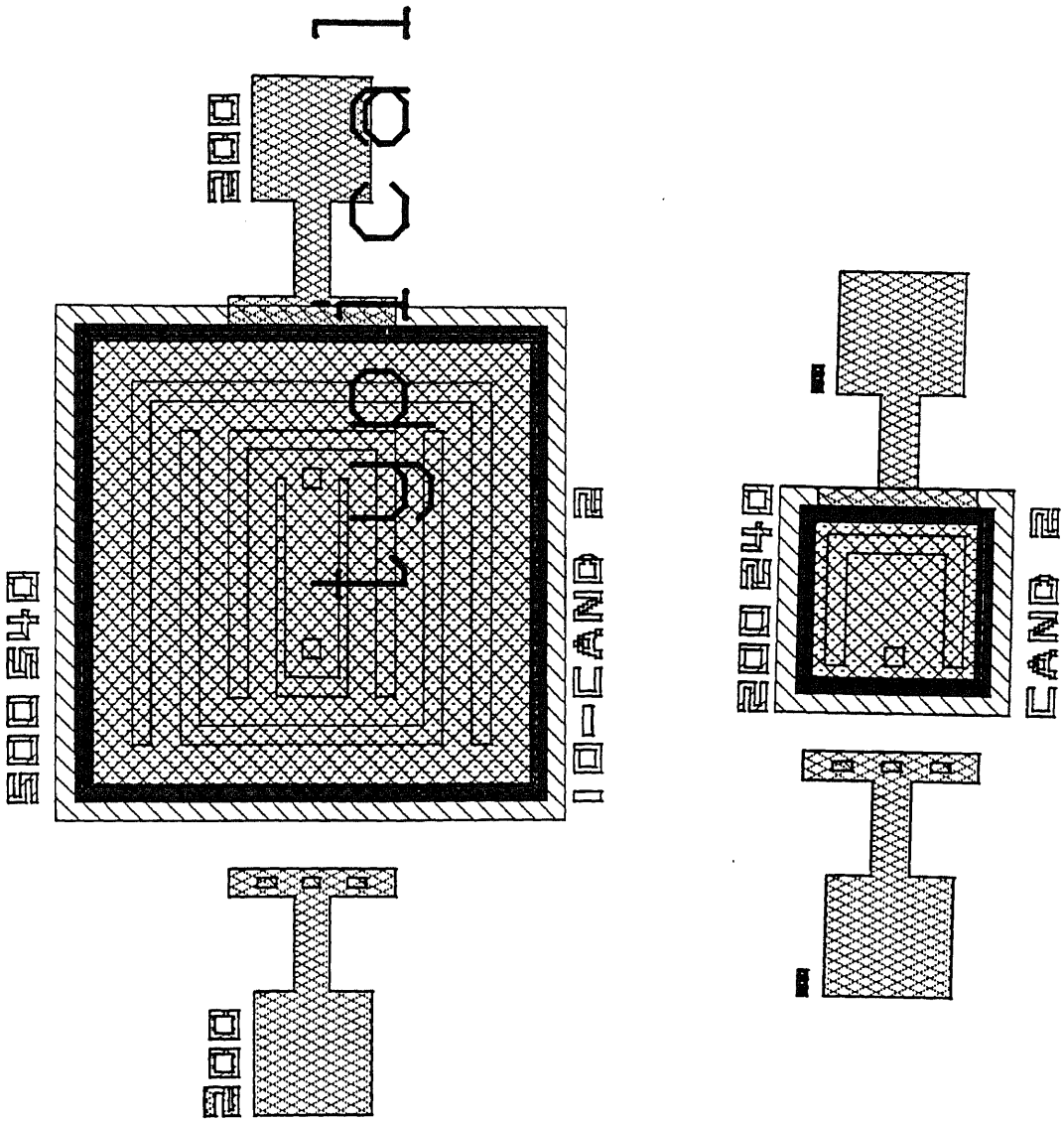


Figure 4.3 The six mask levels combined

4-3. Process Description

4.3-1 Starting material

Silicon wafers oriented in the [100] crystallographic plane are used in this thesis. Prior to use silicon wafers are cleaned chemically to remove surface contamination. Commonly used are aqueous mixtures of NH_4OH-H_2O_2, HCI-H_2O_2, and H_2SO_4-H_2O_2. Here we use H_2SO_4-H_2O_2. All of the solutions are efficient in removing metallic impurities. The ammonium hydroxide and sulfuric acid based mixtures will also remove organic contaminants, but the latter is better in this regard. These cleaning solusions leave the surface of the wafers in a hydrophilic state due to the oxidizing nature of the peroxide. In a hydrophilic state, water will wet the wafer surface (i.e., will be retained by surface tension). Since the chemically grown oxide can contain impurities from the chemicals, it is usually removed by a short immersion in dilute hydrofluoric acid. A typical cleaning sequence would be a sulfuric acid-hydrogen peroxide clean followed by the hydrofluoric acid dip, with deionized water rinses following each acid step.

4.3-2 Lithography step: Mask #1 Defines Cavity

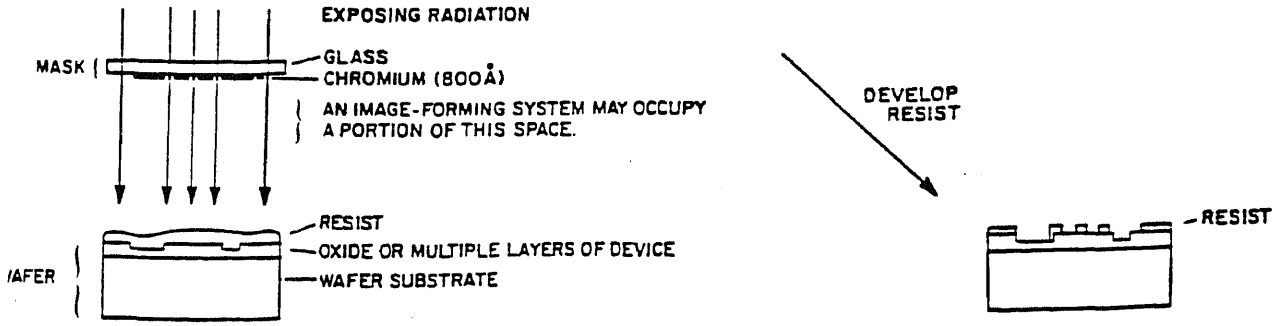


Figure 4.5 Device lithography generalization

Figure 4.5 illustrates schematically the lithographic process used to process wafers. The incident radiation is transmitted through the "clear" parts of the lithography mask. The circuit pattern of opaque chromium blocks some of the radiation. This type of chromium/glass mask is used with ultraviolet (UV) light.

Here we use optical lithography comprise the formation of images with visible or ultraviolet radiation in a photoresist using contact printing. For integrated circuit production the linewidth limit of optical lithography lies near 0.4 μm, although 0.2 μm features may eventually be printed under carefully controlled conditions.

Positive resists are used for processing this device. Positive resists have two components: a resin and a photoactive compound dissolved in a solvent. The photoactive compound is a dissolution inhibitor. When it is destroyed by exposure to light, the resin becomes more soluble in an aqueous developer solution, so higher resolution is possible with positive resists. The development process of projection printed images in positive resists has been modeled theoretically. It is an isotropic etching process. The sensitivity of most standard resists peaks in the 300 to 400 nm spectral range.

We open this window on the silicon substrate for the main working area. This cavity forms the optical path, the cap. The window's size is really depend on the application need. Three different window sizes: $100\times100\mu m^2$, $200\times200\mu m^2$, and $500\times500\ \mu m^2$ are used for the present design.

4.3-3 Silicon substrate etch (RIE)

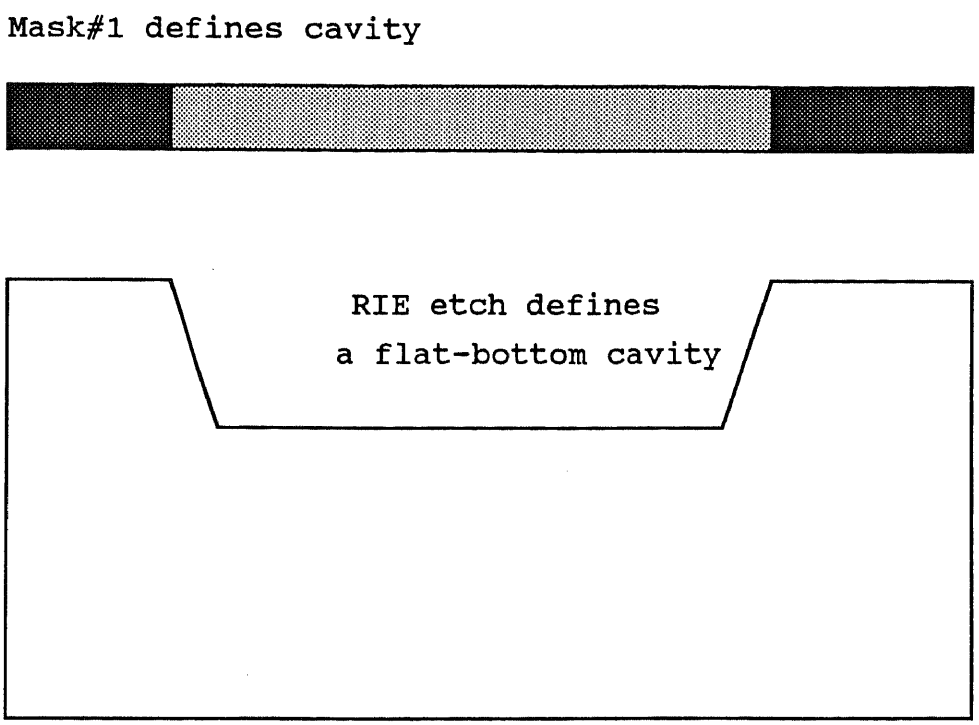


Figure 4.6 RIE etch define a flat-bottom cavity

We use reactive ion etching (RIE) to define a flat-bottom cavity. RIE has three characteristics: physical (ion) and chemical, directional, and more selective than sputtering. The pressure of this etching is in the range of 100 millitorr. The term reactive ion etching is commonly used to denote processes in which plasma etching is accompanied by ionic bombardment, is actually somewhat of a misnomer. Since the etching by the reactive radicals is principally enhanced by the ionic bombardment, sometimes these processes would be described as ion-assisted etching processes.

Since this bottom act like a mirror after sputtering metal. The bottom of the cavity must be very flat. RIE provide the most uniform etching across the entire wafer to match the requirement.

4.3-4 Thermally Grown Oxidation

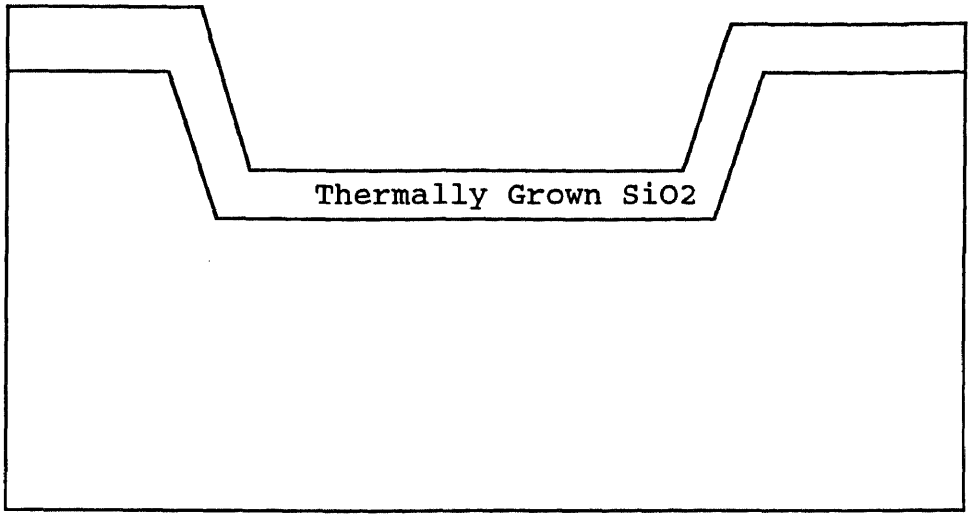


Figure 4.7 deposit SiO_2 as an isolated layer between substrate and metal layer

Silicon Oxide has several uses here: to serve as a mask against implant or diffusion of dopant into silicon, to provide surface passivation, and to provide electrical isolation of next level metallization. Several techniques for forming the oxide layers have been developed, such as thermal oxidation (including rapid thermal techniques), wet anodization, vapor-phase technique [chemical vapor deposition (CVD)], and plasma anodization or oxidation. Since the interface between the oxide and the silicon requires a low-charge density level, thermal oxidation has been the preferred technique.

Because a silicon surface has a high affinity for oxygen, an oxide layer rapidly forms when silicon is exposed to an oxidizing ambient. The chemical reactions describing the thermal oxidation of silicon in oxygen or water vapor are given in equation 4.3-4(1) and 4.3-4(2), respectively.

$$Si\ (solid) + O_2 \rightarrow SiO_2(solid) \qquad 4.3\text{-}4(1)$$

$$Si\ (solid) + 2H_2O \rightarrow SiO_2(solid) + 2H_2 \qquad 4.3\text{-}4(2)$$

The basic process involves shared valence electrons between silicon and oxygen; the silicon-oxygen bond structure is covalent. During the course of the oxidation process, the Si-SiO_2 interface moves into the silicon. Its volume expands, however, so that the external SiO_2 surface is not coplanar with the original silicon surface. Based on the densities and molecular weights of Si and SiO_2, we can show that for growth of an oxide of thickness d, a layer of silicon with a thickness of 0.44d is consumed (figure 4.8)

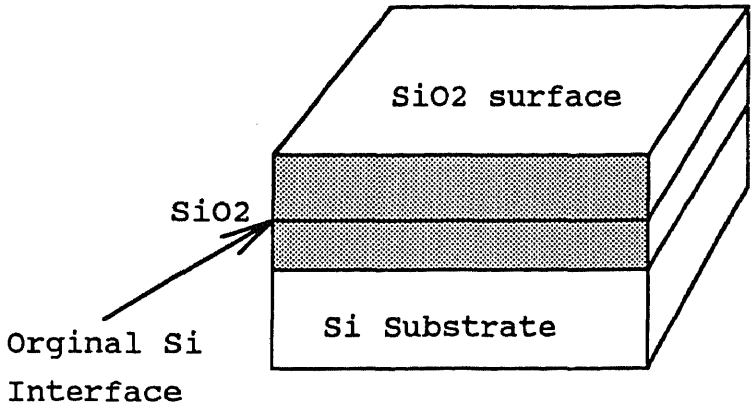


Figure 4.8 Growth of SiO_2

Thermally grown SiO_2 is in thickness ranging from 60 Å to 10000 Å. For here we want 300 Å thickness for isolating the metal and substrate.

4.3-5 Sputtered tungsten film

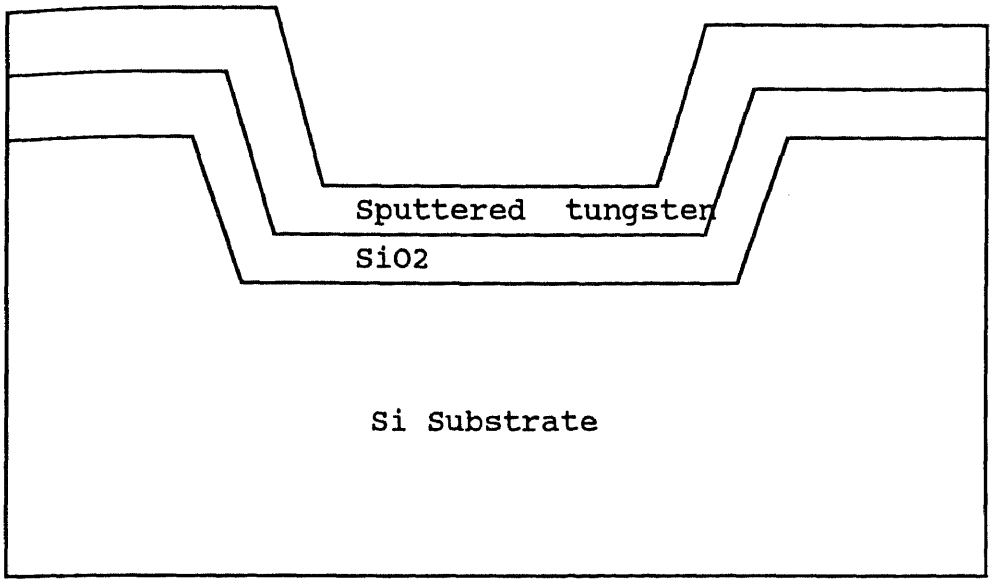


Figure 4.9 Sputter tungsten as a mirror surface

4.3-5(a) Sputtering

Sputtering is a term used to describe the mechanism in which atoms are dislodged from the surface of a material by collision with plasma-produced particles. It has become the most widely utilized deposition technique for a variety of metallic films in VLSI fabrication, including aluminum, aluminum alloys, platinum, gold, titanium:tungsten and tungsten. It is also used in some applications to deposit molybdenum, Si, SiO_2(silica glass), and refractory metal silicides.

We choose sputtering to deposit metal layer because of the following reasons:

a) Sputtering can be accomplished from large-area targets, which simplifies the problem of depositing films with uniform thickness over large wafers.

b) Film Thickness control is relatively easily achieved by selecting a constant set of operating conditions and then adjusting the deposition time to react.

c) Many important film properties, such as step coverage and grain structure, can be controlled by varying the negative bias and heat applied to the substrates.

4.3-5(b) Tungsten film

I. Fabrication concern

For fabrication concern, refractory films are required in contact and interconnection, where low-resistivity and thermally stable layers are particularly required. This growing requirement is a logical constant decrease of device dimensions in order to achieve higher densities and performances. For "self-aligned" technology, the use of refractory metals able to withstand the strong postime/plantation annealing (800-900 °C) without any degradation of the film integrity is a requirement of prime necessity.

The refractory metals are legitimate candidates for the above-mentioned very large scale integration (VLSI) requirements. The advantages of tungsten, in particular, are compared in Table 4.3-5 I with those of AL and summarized below:

(i) The electrical resistivity is fairly low (W bulk resistivity: 5.6 μΩ cm)

(ii) The heat resistance is intrinsically high.

(iii) The films are readily etchable.

(iv) The patternability is fine.

Table 4.1 Compared advantages of two metals (AL and W) according to VLSI requirements.

Film characteristics	Aluminum	Tungsten
Resistivity (μΩ cm)	2.7 (bulk)	5.6 (bulk)
Lithography resolution (μm)	1	0.2
Critical linewidth (μm)	3	0.5
Maximum temperature of postannealings (°C)	500	800
Adhesion	very good	irregular
Low temperature Oxidation	Al_2O_3 problem with etching	Low thermal stability in oxygen ambients

II. Reflectivity

Figure 4.10 shows the variations of the optical reflectivity (light wavelength: 546 nm) for two W film Thickness (80 and 250 nm) in the 100-1000 W rf power range (during deposition). In each case, a strong decrease of the reflectivity is observed ~100-200 W and is particularly pronounced for the lower thicknesses. Beyond 200 W, the reflectivity tends to stabilize at a 54% upper limit, which corresponds to the following mean value of the complex refractive index: $\tilde{N} = 3.15$ For comparison, the complex refractive index of a quasi-ideal W surface (atomically clean and well-ordered surface) is $\tilde{N} = 3.75$ at 546 nm and the corresponding reflectivity is also 54%.

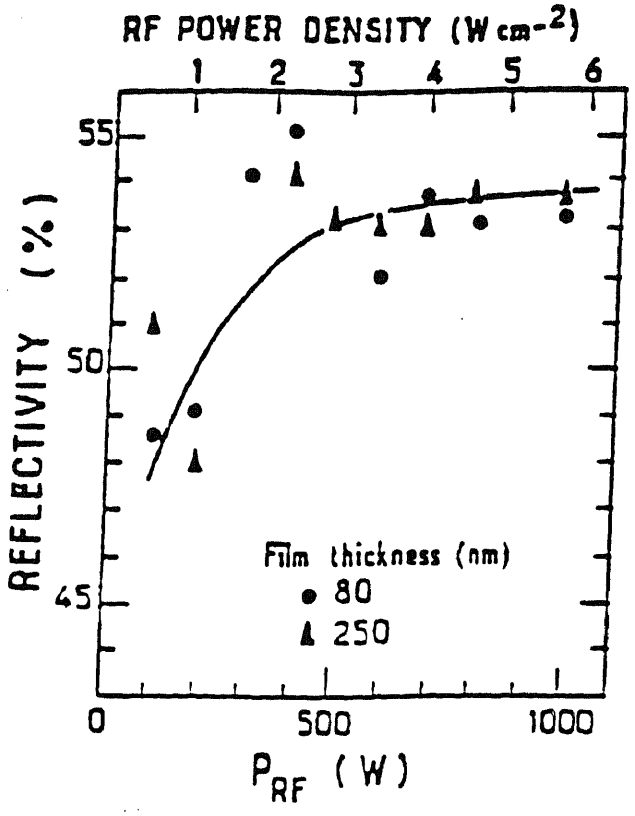


Figure 4.10 Optical reflectivity vs rf power for two film thickness (150 and 250 nm). for tungsten [56]

4.3-6 Use low-pressure chemical vapor deposition to grow silicon nitride

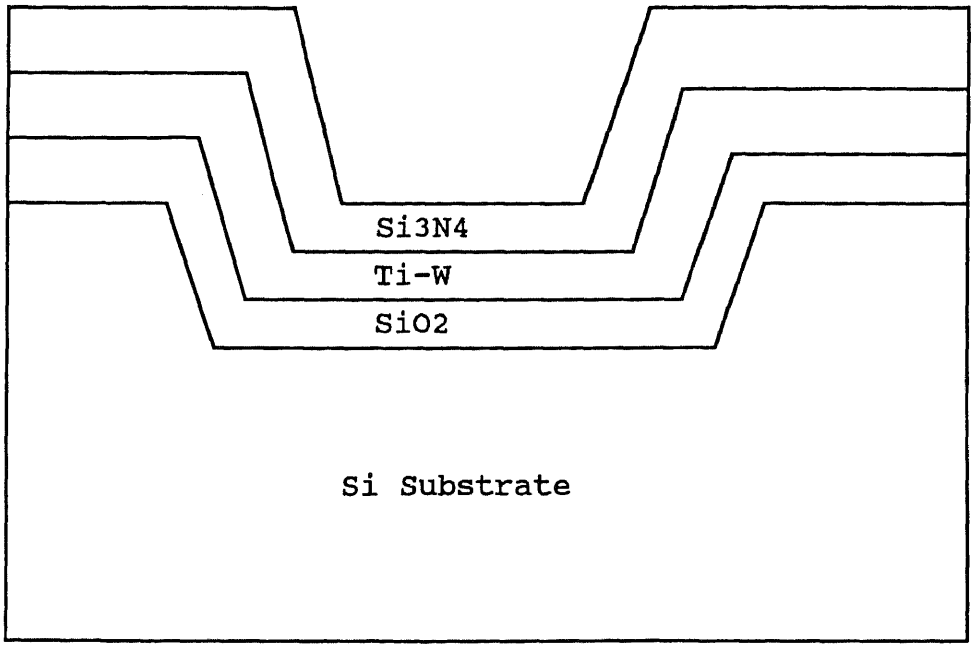


Figure 4.11 LPCVD Si_3N_4

Stoichiometric silicon nitride (Si_3N_4) is used for passivating the tungsten layer because it serves as an extremely good barrier to the diffusion of water and sodium. These impurities cause devise metallization to corrode or devices to become unstable. Silicon nitride is patterned and the exposed silicon substrate is oxidized. The silicon nitride oxidizes slowly and prevents the underlying silicon from oxidizing. This process of selective oxidation produces nearly planar device structures.

Silicon nitride is chemically deposited by reacting silane and ammonia at atmospheric pressure at temperatures between 700 and 900°C (That's why tungsten was selected as the metal layer) or by reacting dichlorosilane and ammonia at reduced pressure at temperatures between 700 and 800°C. The chemical reactions are

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

$$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$$

The reduced-pressure technique has the advantage of good uniformity and high wafer throughput.

Silicon nitride, chemically deposited at temperatures between 700 and 900°C, is an amorphous dielectric containing up to 8 atmospheric % hydrogen. The hydrogen is bonded to the nitrogen and the silicon. The amount of hydrogen depends on the deposition temperature and the ratio of reactants. More hydrogen is incorporated into the deposited film at low deposition temperatures or at high ammonia to dichlorosilane ratios. Silicon nitride deposited at low ammonia to dichlorosilane ratios contains excess silicon that decreases the electrical resistivity which is the effect we don't want.

Silicon nitride films have a refractive index of 2.01 and an etch rate in buffered hydrofluoric acid of less than 1 nm/min. Both properties are used to check the quality of deposited nitrides. Oxygen impurities in the film cause a higher etch rate. High refractive indices suggest a silicon-rich film; low indices are caused by oxygen impurities. Figure 4.3-6 shows how the refractive index changes with composition. Silicon nitride films that contain oxygen are silicon oxynitride. The composition of silicon oxynitride can vary from silicon dioxide with a refractive index of 1.46 to silicon nitride with an index of 2.01. Films that are free of oxygen but have silicon to nitrogen ratios greater than 0.75 are silicon-rich silicon nitride and have a refractive index that increases as the amount of excess silicon.

Silicon nitride has a high tensile stress, about 1×10^{10} dyne/cm^2. Films thicker than 200 nm sometimes creak because of high stress. The resistivity of silicon nitride at room temperature is about 10^{16} ohm-cm. The electrical resistivity depends on the deposit temperature, film stoichiometry, amount of hydrogen in the film, and the presence of oxygen impurities.

Table 4.2 summarizes the properties of LPCVD silicon nitride.

Table 4.2 Properties of LPCVD silicon nitride

Temperature (°C)	700-800
Composition	$Si_3N_4(H)$
Si/N ratio	0.75
Atom % H	4-8
Refractive Index	2.01
Density(g/cm^3)	2.9-3.1
Dielectric constant	6-7
Resistivity (ohm-cm)	10^{16}
Dielectric strength (10^6V/cm)	10
Energy gap (eV)	5
Stress (10^9 dyne/cm^2)	10 T

The thickness of this layer we choose is 485nm. Figure 4.12 shows the reflection intensity vs length.

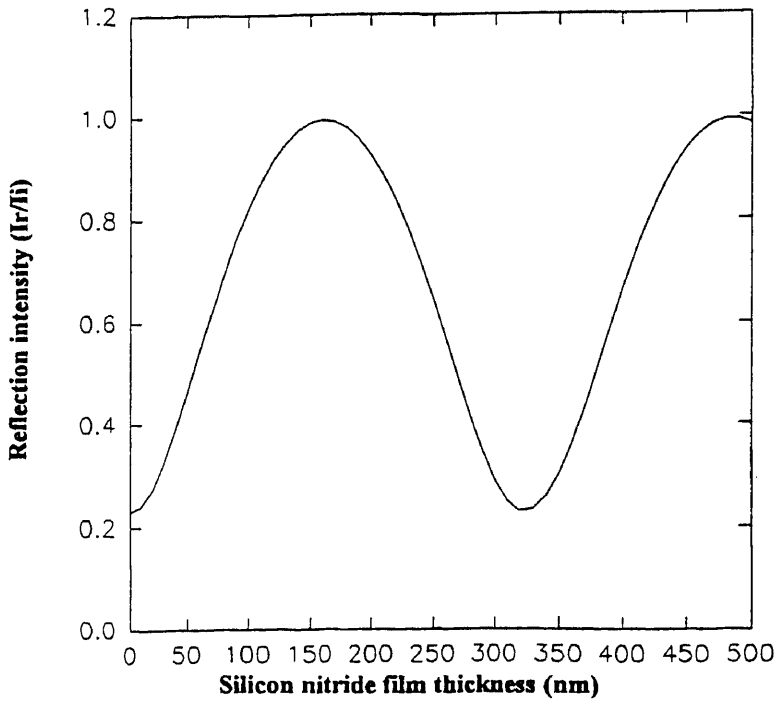


Figure 4.12 The reflection light intensity vs. silicon nitride thickness EQU [2.1-6]

4.3-7 Lithography Step: Open windows on silicon nitride

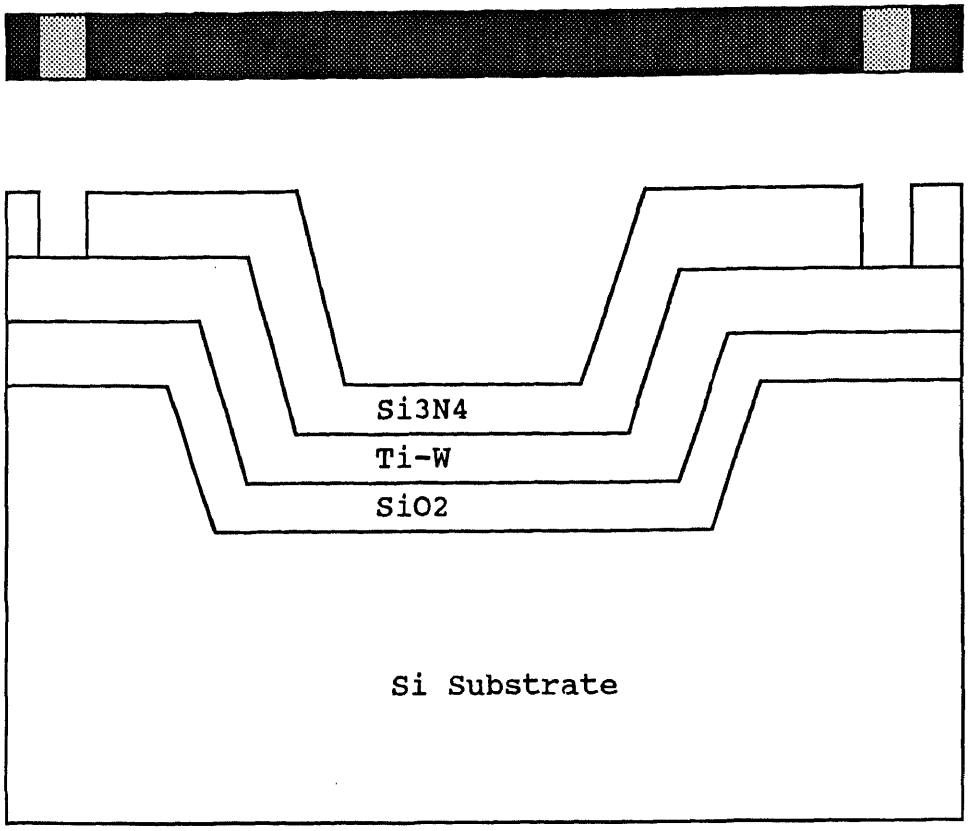


Figure 4.13 Open windows for contact to the buried electrode

Since the silicon nitride film is used to isolate the W electrode, we need an electrical path to the buried layer contacting the outside bonding pad. That's why we open these windows. This window is designed 15×15 μm. The detail please reference to chapter 4.3-2. We use the following steps to open the windows.

Silicon nitride can be etched by reflux boiling 85% phosphoric acid at 180°C. However photoresist is lifted during such etching and does not make a good etch mask for this application. Most wet silicon nitride etching thus utilizes a thin SiO_2 layer (either thermally grown or deposited), to mask the nitride. The SiO_2 layer is first etched using a resist mask, then the resist is stripped, and the patterned oxide serves as the etch mask for the nitride in the phosphoric acid etch. The Si_3N_4 etch rate is about 100 A/min., but only

0-25 A/min. for CVD SiO_2. Films of plasma-enhanced CVD Si_3N_4 have much higher etch rates than conventional high temperature CVD Si_3N_4. The rates depend strongly on the film composition, which may be expressed as $Si_xN_yH_z$.

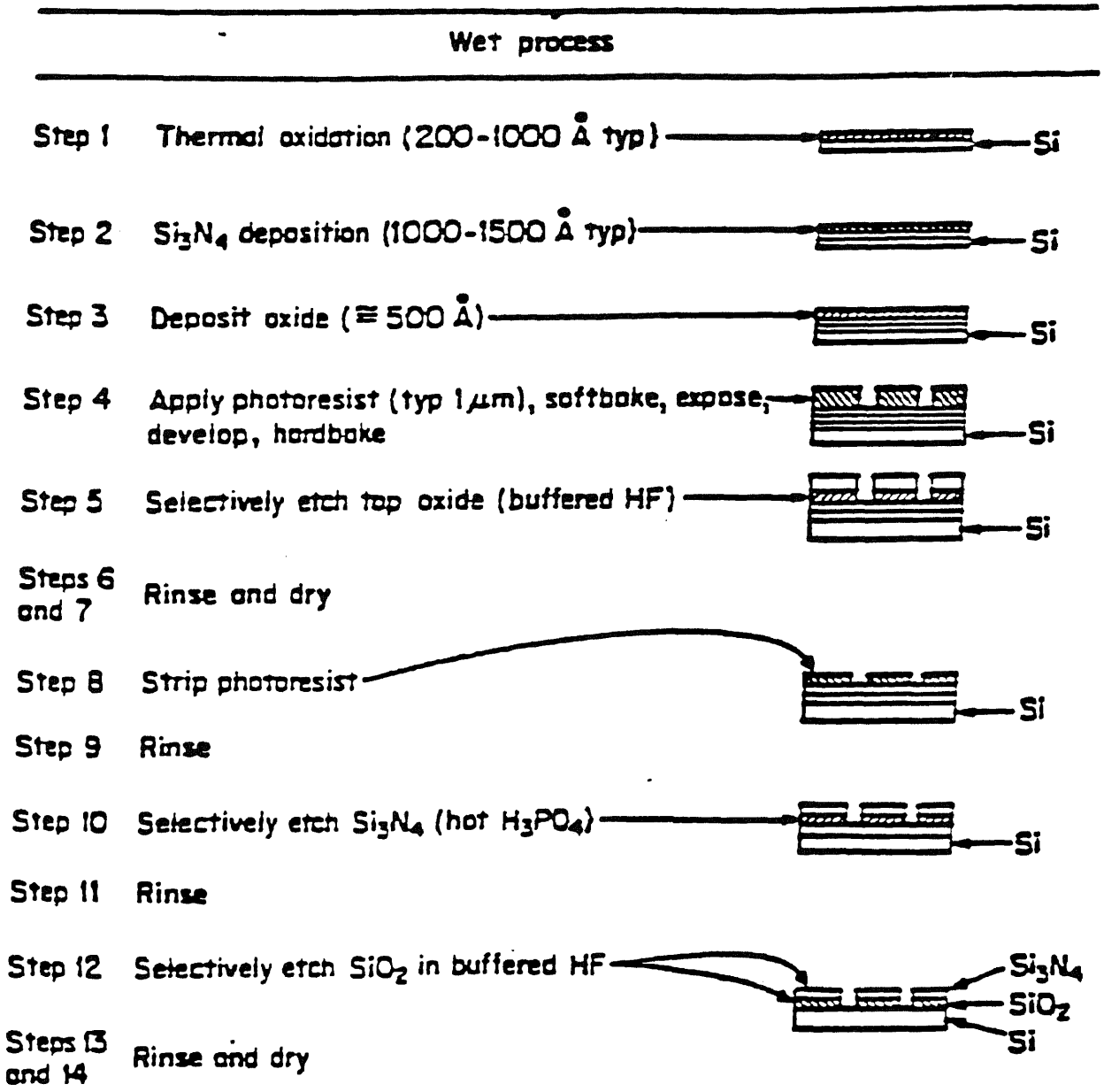


Figure 4.14 The wet process for Si_3N_4 [54]

4.3-8 Spin-on glass as a sacrificial layer

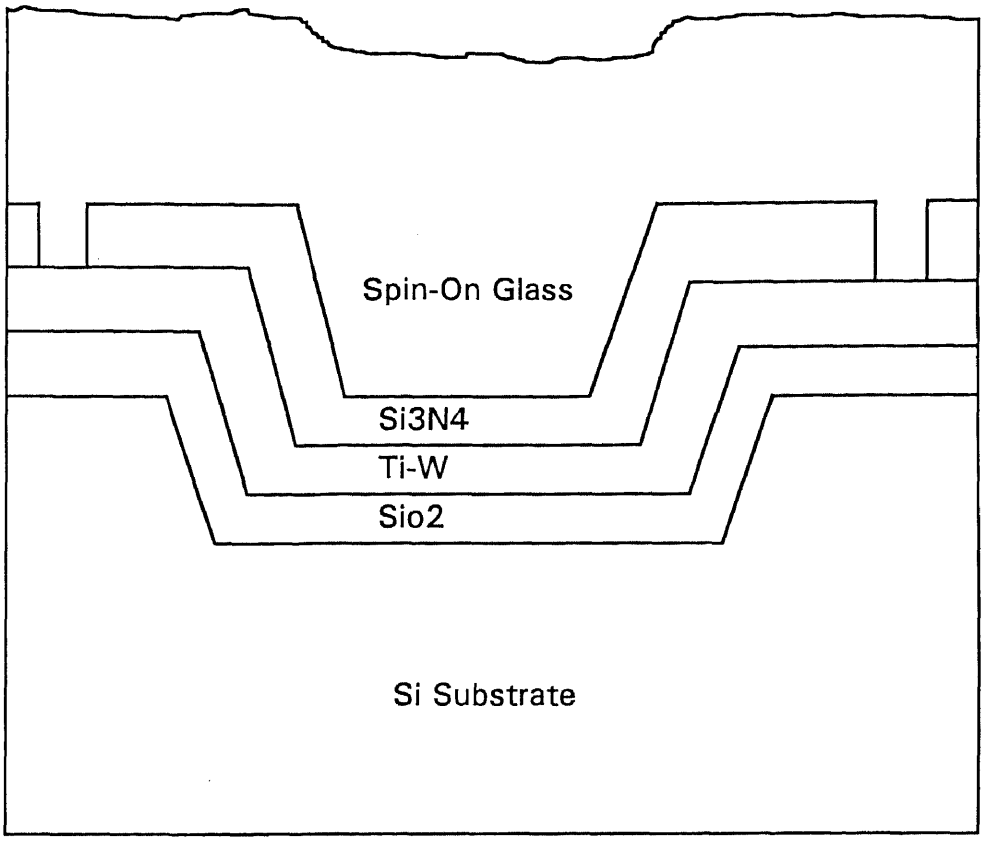


Figure 4.15 Spin-on glass as a sacrificial layer

The spin-on glass is liquid solutions which, upon drying, form doped SiO_2 layers. Most of the formulations are held proprietary by their manufacturers. The spin-on dopants are applied to the wafers in a similar fashion as photoresist. The thickness of the deposit depends on the solution viscosity and the spin speed. The dopant concentration in the film can be varied by dilution with organic solvents. It is often necessary to bake the wafers at 200°C for 15 minutes to dansify the film, and to prevent absorption of water vapor prior to driving the dopant into the silicon. The diffusion is performed over a range of temperatures and times depending on the desired sheet resistance, and junction depth. The detail will be discuss in chapter 5.

4.3-9 Planerize spin-on glass

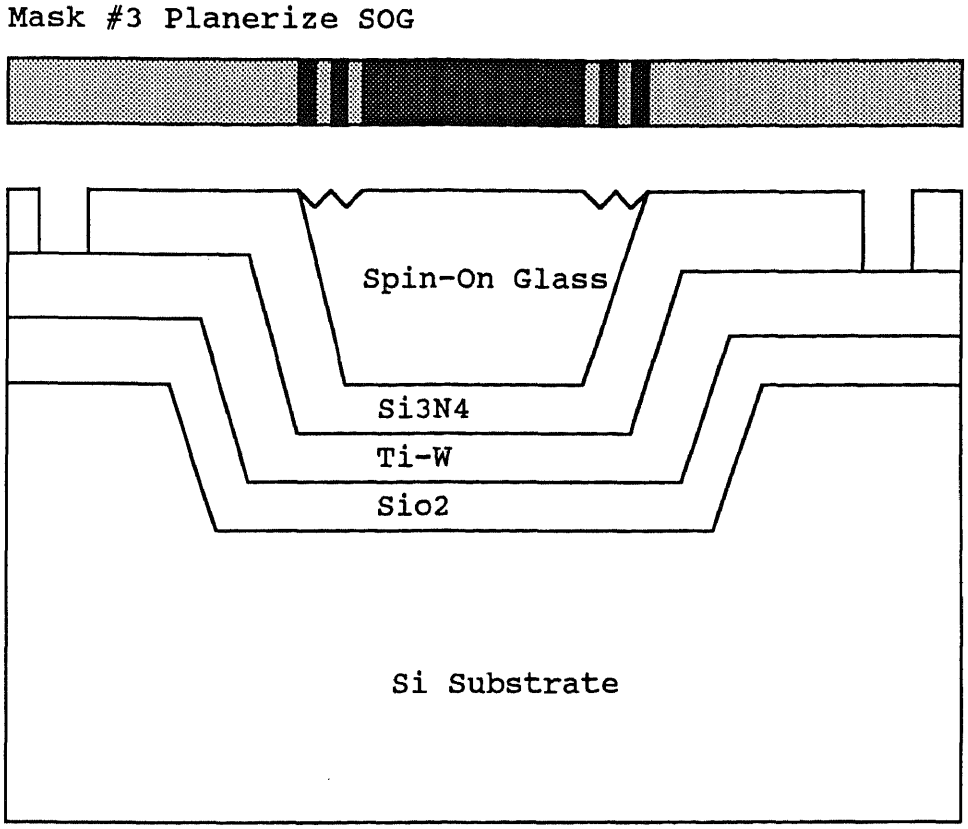


Figure 4.16 Planerize spin-on glass

The conformal deposition of a dielectric such as phosphorus-doped silicon dioxide over a pattern conducting layer results in a stepped profile similar to that in figure 4.3-8. In order to ensure uniform coverage of the next conducting layer, the dielectric surface must be smoothed. This can be accomplished by flowing the dielectric at high temperatures (>800°C). When the highest allowable substrate temperature is less than the dielectric flow temperature, two etching techniques can be used to smooth the surface. The first, called planarization, is accomplished by spinning a resist or any other polymeric layer onto the irregular dielectric film, which is deposited thicker than necessary for the final structure. This results in a smoothing of the new top surface. This new surface is then transferred into the dielectric by etching in a reactive plasma that etches the resist and the

dielectric at the same rate. Smoothing of a dielectric surface can also be accomplished by depositing more dielectric than necessary and then simply etching in an RIE mode.

The mask used in planarization also has some frame-like structure. It is used for generating the corrugated structure. The detail will be introduced in chapter 5. We may need two masks (one for plannerize, one for frame-like structure) to finish this process.

4.3-10 Deposit Polysilicon

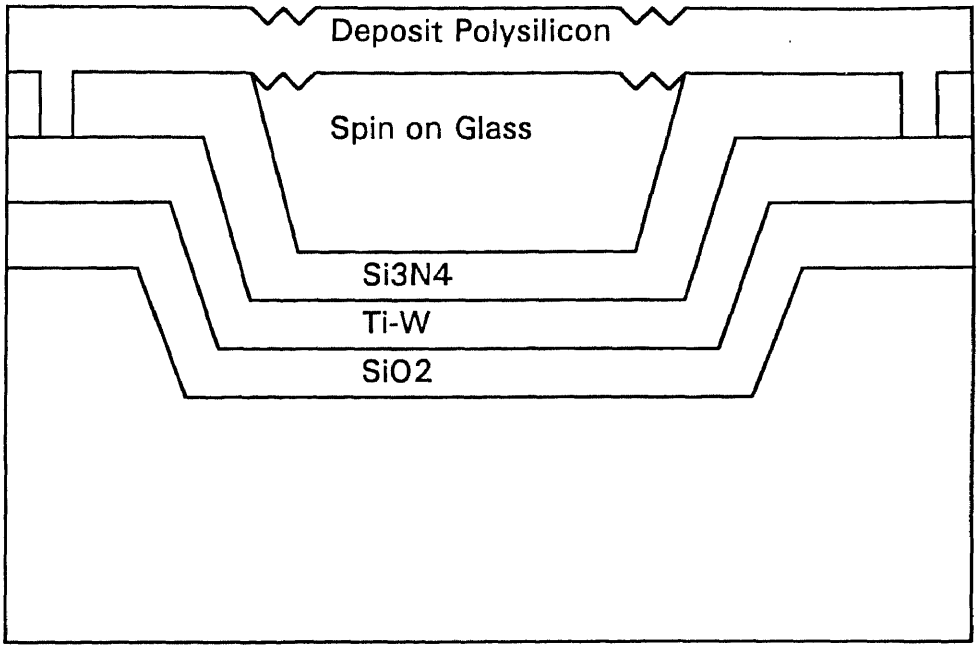


Figure 4.17 Deposit Polysilicon

Polycrystalline silicon, usually referred to as polysilicon, is prepared by pyrolyzing silane at 575 to 650°C. Polysilicon is used as the cap film in this device. The doping elements arsenic, phosphorus, or boron reduce the resistivity of the polysilicon and are added later by diffusionor ion implantation.

We use LPCVD to deposit the polysilicon film. The chemical reaction is

$$SiH_4 \rightarrow Si + 2H_2$$

A low-pressure process is used for depositing polysilicon. We use 20 to 30% silane diluted in nitrogen at a pressure of 25 to 130 Pa (0.2 to 1.0 Torr). This process deposits

that results in low resistivities. The dopant concentration in diffused polysilicon often exceeds the solid solubility limit, with the excess dopant segregated at the grain boundaries. Hall mobilities for heavily diffused polysilicon are usually 30 to 40 $cm^2/V\text{-}s$.

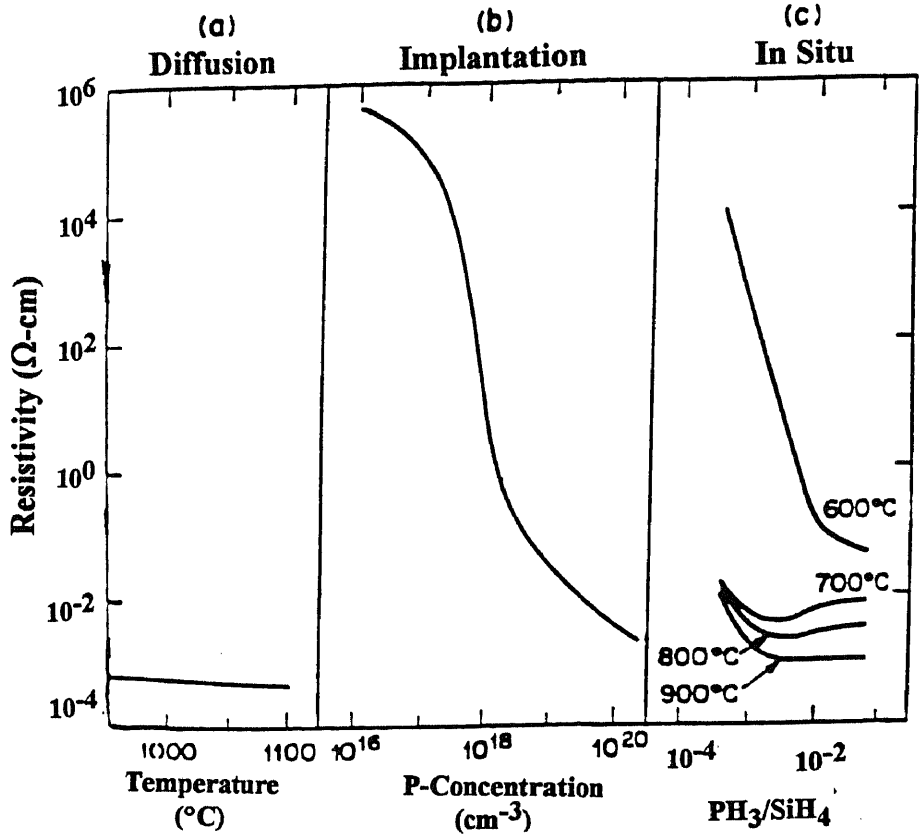


Figure 4.19 Resistivity of P-doped polysilicon. (a) Diffusion: 1 h at the indicated temperature.(b) Implantation: 1 h anneal at 1100°C. (c) In situ: as deposited at 600°C and after a 30-min anneal at the indicated temperature.

The resistivity of implanted polysilicon depends primarily on implant dose, annealing temperature, and annealing time. The high resistivity in lightly implanted polysilicon (figure 4.3-19) is caused by carrier traps at the grain boundaries. Once these traps are saturated with dopants, the resistivity decreases rapidly and approaches the resistivity for implanted single-crystal silicon. The mobility for heavily implanted polysilicon is about 30 to 40 $cm^2/V\text{-}s$, similar to the values for diffused polysilicon.

Implanted polysilicon has about ten times higher resistivity than diffused polysilicon because of the differences indopant concentrations: about 10^{20} cm^{-3} for a heavy diffusion.

The thickness of this polysilicon layer is very important. It is designed to allow the maximum intensity of light to pass through this layer. Figure 4.20 shows the transmission light intensity vs. thickness of polysilicon.

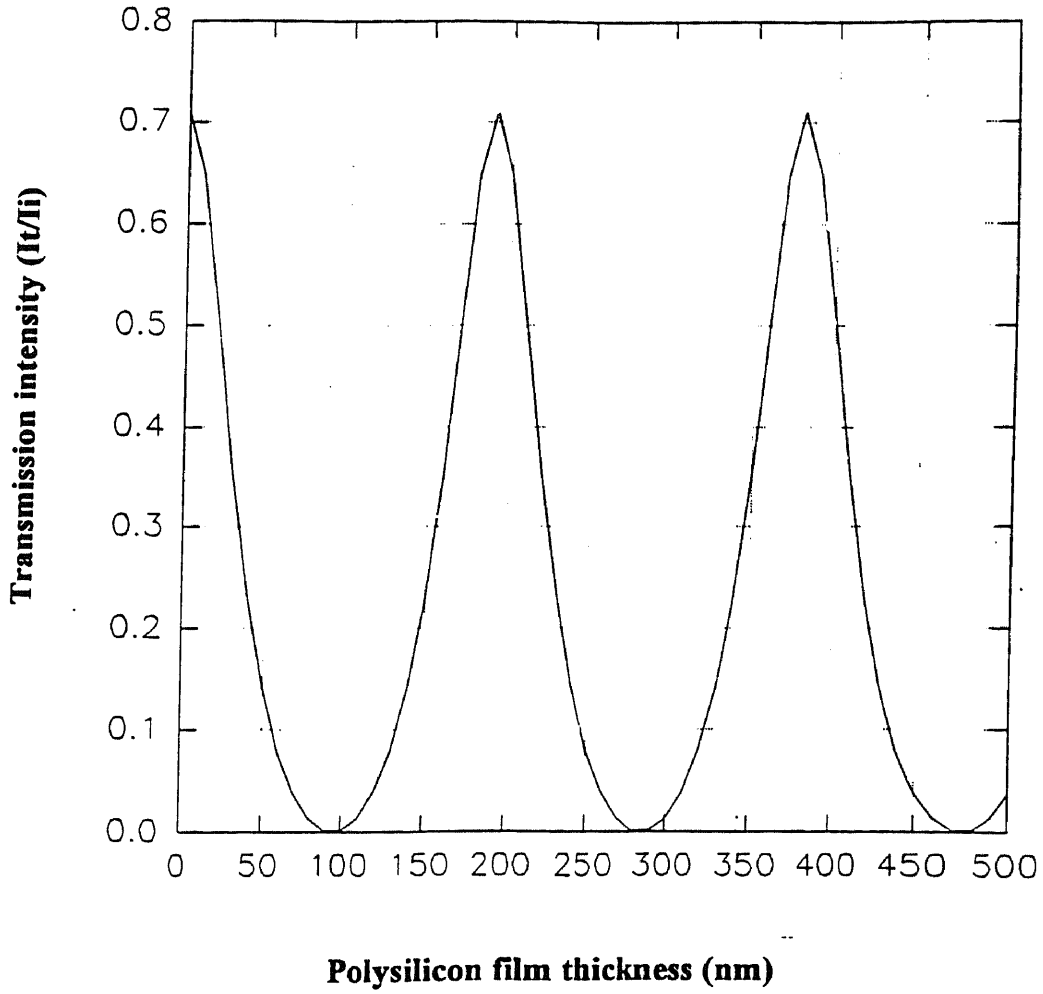


Figure 4.20 Light transmission intensity VS. polysilicon layer thickness

4.3-11 Pattern the polysilicon layer

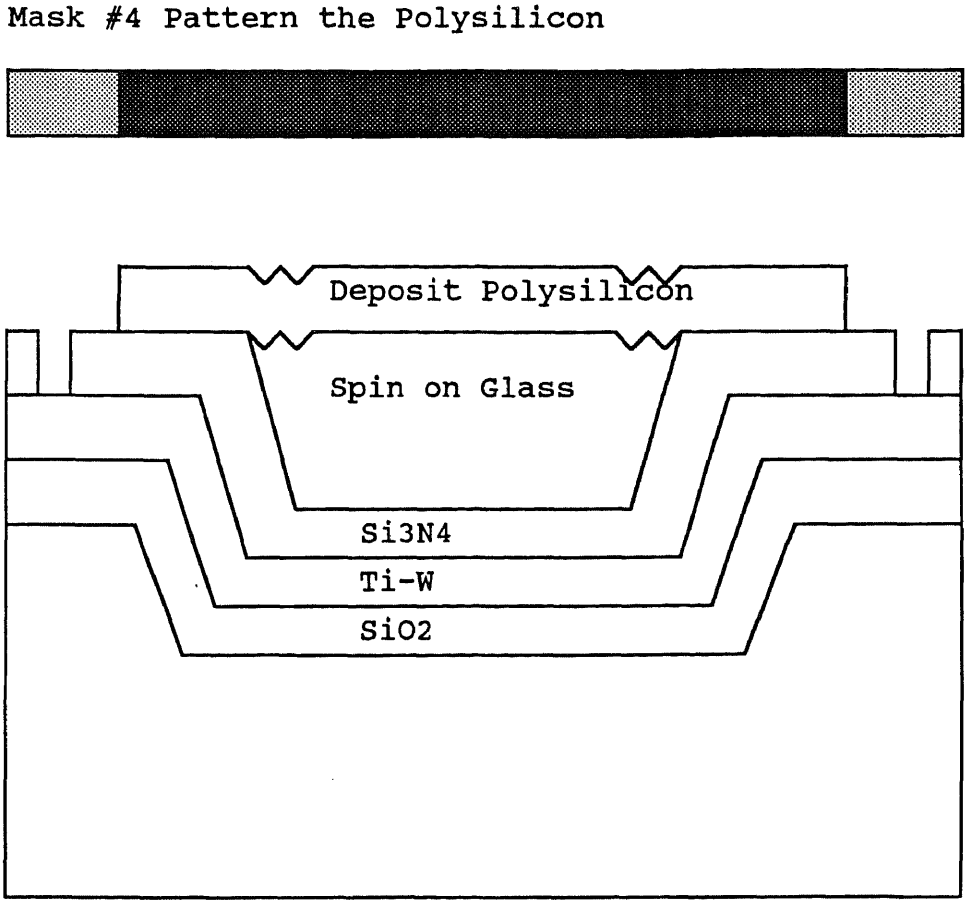


Figure 4.21 Pattern the polysilicon layer

We use wet etch to etch out the area not in the pattern. Polysilicon is typically wet etched in mixtures of nitric acid (HNO_3) and hydrofluoric acid (HF). The reaction is initiated by the HNO_3 which forms a layer of silicon dioxide on the silicon, and the HF dissolves the oxide away. The overall reaction is :

$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2 + H_2O$$

Water can be used to dilute the etchant, but acetic acid (CH_3COOH) is preferred as a buffering agent, since it causes less dissociation of HNO_3, and thus yields a higher concentration of the undissiciated species.

The mixture compositions can be varied to yield different etch rates. At high HF and low HNO_3 concentrations (the region near the upper corner of the triangle), the etch rate is controlled by the HNO_3 concentration, because in such mixtures there is an excess of HF to dissolve the SiO_2 created during the reaction. On the other hand at low HF and high HNO_3 concentrations, the etch rate is limited by the ability of the HF to remove the SiO_2 as it is created. In such etchants the etching is isotropic, and they are used as polishing agents.

After etch the polysilicon, the device will look like figure 4.21. The left polysilicon forms the cap film. This film will be attracted to move toward the bottom by electrostatic force. The optical length will be controlled by the different voltage we put between cap and bottom.

4.3-12 Sputtered Aluminum

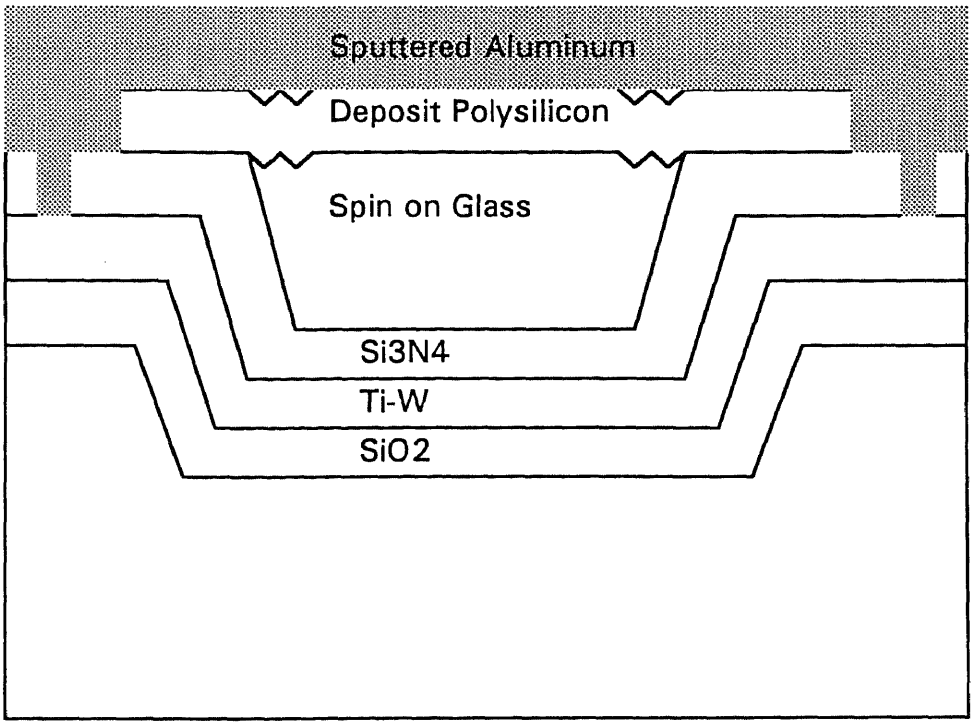


Figure 4.22 Sputtered Aluminum as bonding pads

Table 4.3 Properties of Aluminum and Aluminum alloy thin films

Name	Symbol	Melting Point (°C)	Al/Si Eutectic (°C)	Density (g/cm^3)	Resistivity ($\mu\Omega$-cm)
Aluminum	Al	660	577	2.70	2.7
Aluminum/ 4% Copper	Al 4%Cu	650	~577	2.95	3.0
Aluminum/ 2% Silicon	Al 2%Si	640	~577	2.69	2.9
Aluminum/ 4% Copper 2% Silicon	Al 4%Cu2%Si		~577	2.93	3.2

The sputtering technique has been described in section 4.3-5(a).

Aluminum is primarily utilized in these applications in thin-film form, and it functions as a material which interconnects the device structures formed in the silicon substrate. Aluminum is emerged as the most important material for device metallization because of its low resistivity (ρ_{Al} = 2.7 $\mu\Omega$-cm) and ease of processing. Aluminum thin-films are deposited as polycrystalline materials, usually in the 0.5μm-1.5μm thickness range.

4.3-13 Aluminum Removal

Mask #5 Aluminum Removal

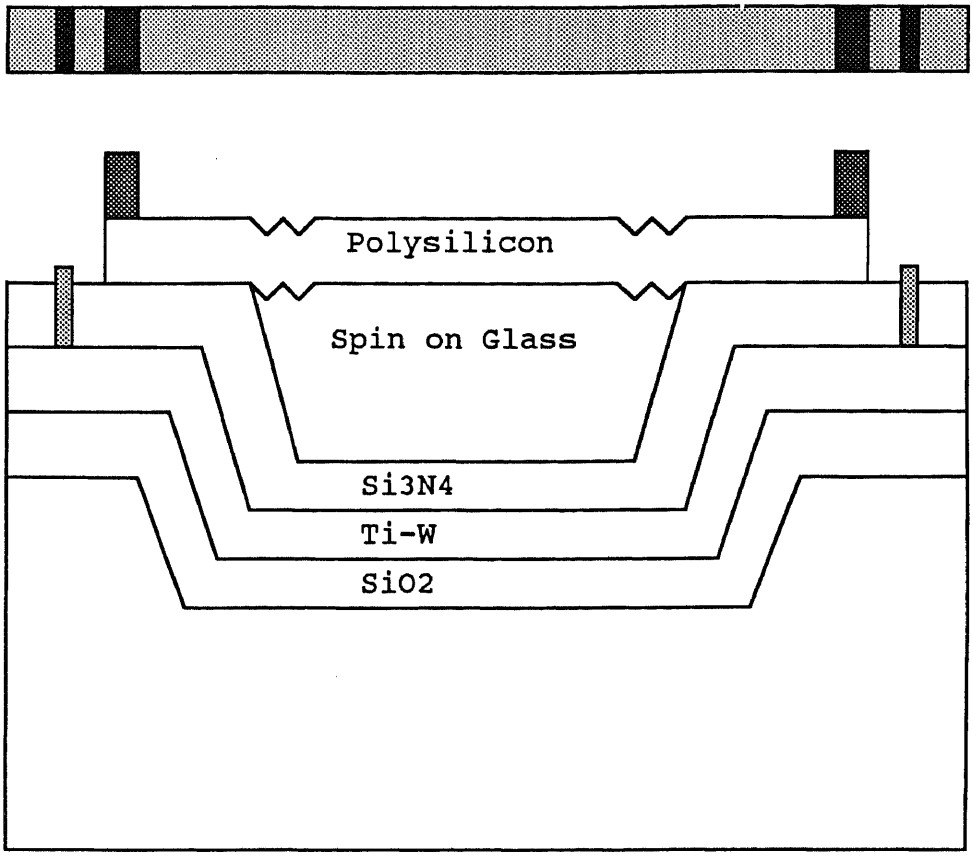


Figure 4.23 Aluminum Removal

We used wet etching to etch out the aluminum. Wet etching of aluminum is generally done in heated solutions (35-45°C) of phosphoric acid , nitric acid, acetic acid, and water. A typical etch composition may be 80% phosphoric acid, 5% acetic and 10% water. The etch rate is in the range of 1000-3000 Å/min and depends on several factors including etchant composition and temperature, type of resist used, agitation of wafers during etch, and impurities or alloys in the predominantly aluminum film.

The chemical mechanism of wet etching aluminum proceeds as follows: The nitric acid forms aluminum oxide, and the phosphoric acid and water dissolve this material. Conversion to Al_2O_3 takes place simultaneously with the dissolution process.

One of the difficulties encountered in wet etching of aluminum is H_2 gas bubble creation. These bubbles tend to adhere firmly, locally inhibiting etching. Mechanical agitation during etching, and the addition of agents which lower the interfacial tension, are used to minimize this problem. Periodic removal of the wafers from the etching solution also breaks the bubbles.

The H_2 bubble formation and other problems (e.g. local contamination of the developed metal, local oxidation, and delayed etching in certain locations [particularly in narrow spaces due to incomplete removal of resist residue]) delay the start of etching or prolong the time to clearly etch all the areas on the wafer. Thus, once the minimum etching time for a given pattern is established, 10-50% overetch time is usually added to assure the complete isolation of features.

4.3-14 Etch small holes for the etchants coming into the cavity

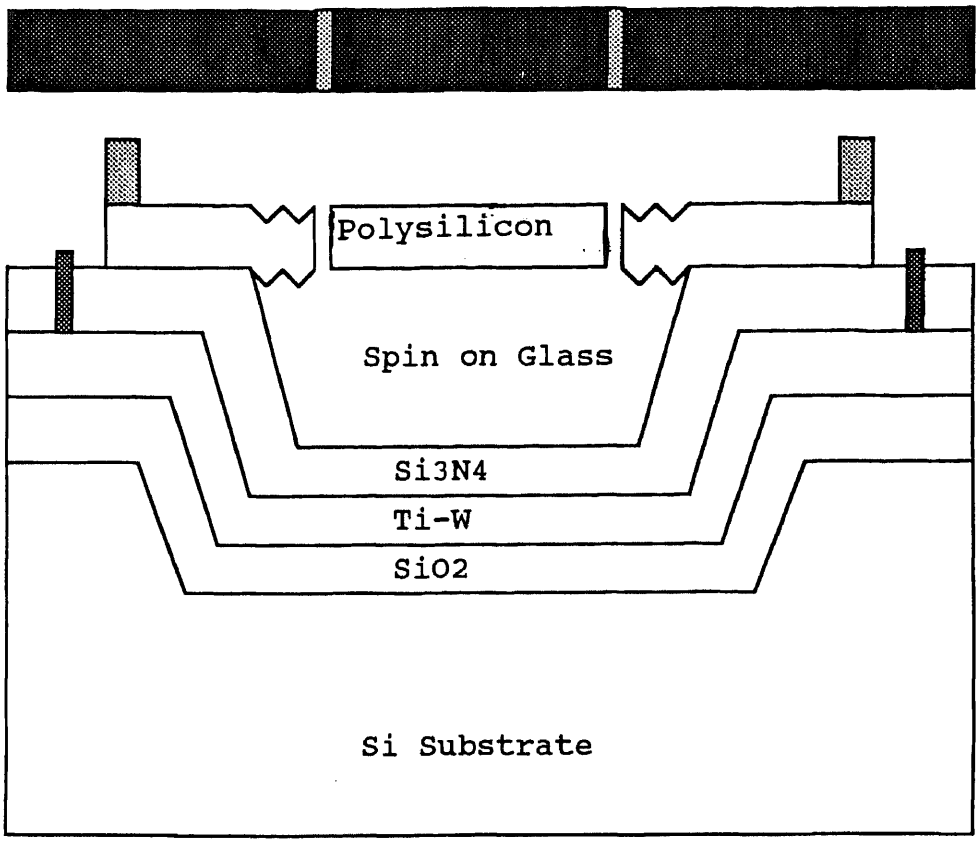


Figure 4.24 Etch small holes for the etchants coming into the cavity

This device has so far almost done. The only things left are to etch out the cavity. The cavity is formed by spin-on glass which is a sacrificial layer. To etch out this SOG, we must open some windows on the top layer. These windows should not be too large to change the intensity of the light, but can't too small to let the etching time too slow. Several different designs of the locations and sizes are shown in figure 4.2. The solution for etch these small holes on the polysilicon film is described in section 4.3-11.

4.3-15 Etch out the cavity

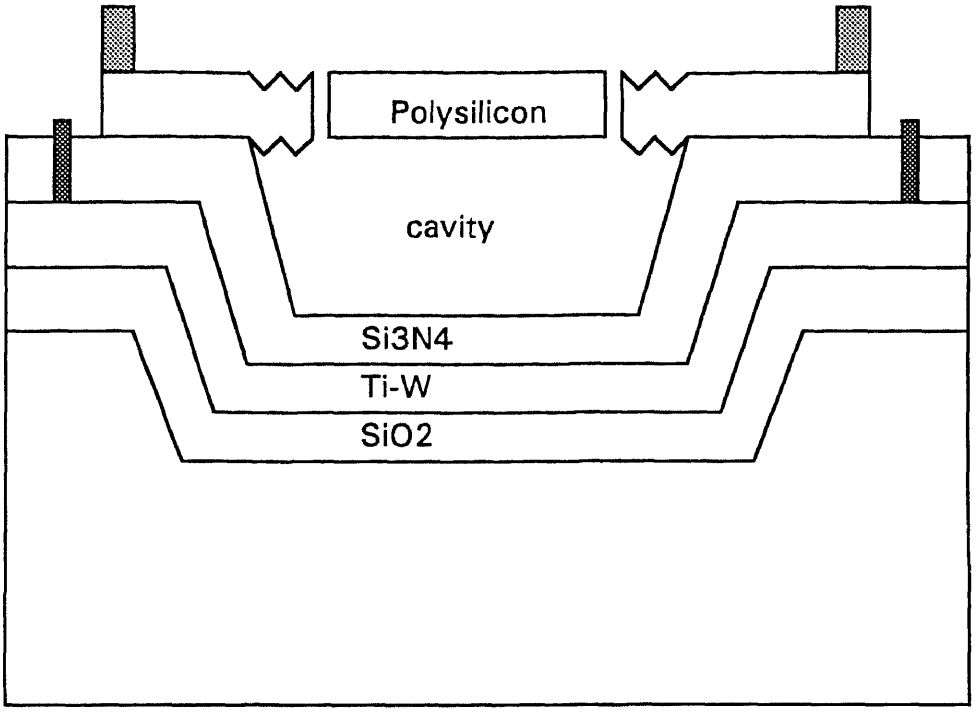


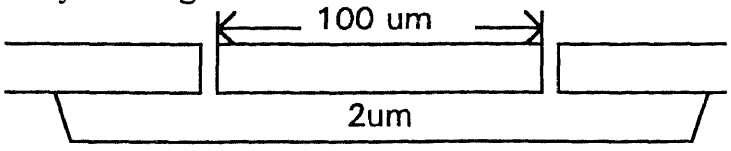
Figure 4.25 Etch out the cavity

After open the windows on the top film, we can use 49% HF to etch out the SOG. The etching rate is depend on the SOG. In this thesis's case, the etching rate is 15μm/min. It is much faster than the etching rate of aluminum. So we don't have to protect those aluminum circuits. To calculate the time we put the wafer in the solutions (49% HF) not only concern the thickness of SOG, but also the distance of the holes. Figure 4.3-15(b) shows how the distances of holes effect the etching time.

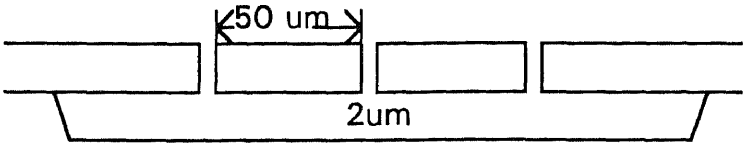
The high temperature SOG may not etch very fast in HF compared to ITO or doped SiO_2. It need some more experimences to varify the data we got from the paper.

In figure 4.26 example 1, the distance between holes is 100μm, with the etching rate 15μm/min. we need 100/15=6.67 mins to etch out all the SOG. In example 2, we need 50/15=3.33 mins to etch out the whole thing. The smaller distance will save etching

time but too many holes makes not only the cap film easy to broken but also decreasing the reflection intensity of the light.



Example 1 Hole distance Hd = 100um



Example 2 Hole distance Hd = 50um

Figure 4.26 Two examples show that same thickness SOG with different etch holes

CHAPTER FIVE
TECHNIQUES FOR FABRICATION

5.1 Fabrication of Cavity using a sacrificial layer

Cavity structure is a very important basis of this device. It is also a very important structure in micro-sensor field like pressure sensor, accelerometer, and light modulator. Up to now, all reported methods to produce cavities were using bulk micromechanical techniques. The typical methods are:

1. Using anisotropic etching of silicon bulk to form cap film (cantilever beam.....), etching cavity from glass plate and using special bonding techniques to bond them together.
2. Producing SiO_2/Si epi/Heavy doped P_+ buried layer sandwich. The silicon cavity is anisotropic etched from under the oxide to the heavily doped P+ buried layer to release the SiO_2.

Most cavity structure reported up to now were made with bulk micromechanical technique. They made the cavity structure with two wafers, making cavities on both first and then bonding them together. This technique has the advantages of easy making and multilayer capacitance. Somehow most of those sensors with cavity structure are not too many layers to be made in single wafer. The only advantage of wafer bonding is easy making, besides this method present processing complexity and compatible problem with IC processing.

Compare to the wafer bonding, sacrificial layer technology can make the cavity-structure sensors in single wafer. The advantages of sacrificial layer technology shrink the sensor size and more precisely structure could be made because we don't have to involve the process of wafer bonding. The processes involved in making the sacrificial layer-cavity are: etching a cavity on the substrate, thermal oxidize the button, sputter a metal film as

the bottom electrode, spin-on glass as a sacrificial layer, deposit a nitride layer, deposit a polysilicon layer with small holes, and etch out the SOG. The detail processes has been introduced in chapter 4.

The most often used sacrificial layer in surface microengineering is PSG. The PSG layer may be produced either with in stiu deposited LPCVD PSG or with LPCVD oxide doped with phosphorous. However, PSG layer, after filling the cavity and patterned, will tend to produce a leaning angle at the surface. Polysilicon deposited on such a surface will tend to buckling or produce unflatness on the surface. Besides, in stiu LPCVD PSG is usually not available, PSG would have to depend on the post phosphorous doping process. However, post P doping process exhibits difficulties as oxide thickness in the range of 1 μm. High temperature doping will create cracks on thick LPCVD oxide.

5.2 SOG processing

Spin-on glass (SOG) technique has been developed for intermetal planarization process for many years. Its minimal thermal budget and equipment requirement is very attractive for applications requiring or compatible with low temperature processing. The present work is motivated toward the newly developed surface micromechanical device technology.

The nonplanar surface of LPCVD polysilicon film due to LPCVD PSG layer can well be avoided by using multicoating process of SOG. Besides, phosphorous doped SOG etches very fast in HF due to its low density, which is advantages of sacrificial layer. As another tip, SOG process does not require special equipment, a spinner, a couple of hot plates, baking furnaces or regular oxidation furnaces will do all the work. SOG has a good potential as a surface planarization material and sacrificial film for micromechanical device applications.

In this device, a phosphorous doped spin-on glass multicoating process proposed to form a 0.65 μm $(\frac{1}{2}\lambda = 1300\text{nm} \times 0.5 = 650\text{nm})$ thick sacrificial layer for

micromechanical device of polysilicon film were carried out to evaluate SOG process conditions. SOG was evaluated as a planarization material and sacrificial film for micromechanical device applications by building a device with polysilicon-SOG-nitride protected oxide cavity sandwich.

Multicoating process is required for this device because:

1. One typical coating produces 1000A to 4000A dielectric layer, the sacrificial layer thickness is 0.95 μm. To obtain enough thickness for a sacrificial layer, multicoating is unavoidable.
2. Better planarization can be achieved through multicoating.

However, multicoating may bring problems like thermal stress between coated layers, and the dielectric layer may crack when thickness reaches around 1 μm. By curing the coated layer carefully, and choose the proper SOG product, those problems can be solved.

SOG liquids consist of Si-O network polymers dissolved in common organic solvents like alcohol and ketone. Inorganic silicate SOG is typically fragile and creaks when thickness exceeds 0.5-0.7 μm. Organic siloxane SOG has a better creak resistance and planarity.

The SOG used in this work is an organic siloxane SOG which has organic group of methyl incorporated within the silicon-oxygen structure. Typically SOG like Allied Signal Accuglass 311P exhibits a high creak resistance, low film shrinkage, very small Silano/H_2O content.

As reported elsewhere, differential thermal analysis suggested curing conditions. From the analysis result shown in Figure 5.1, it was found that the solvent was

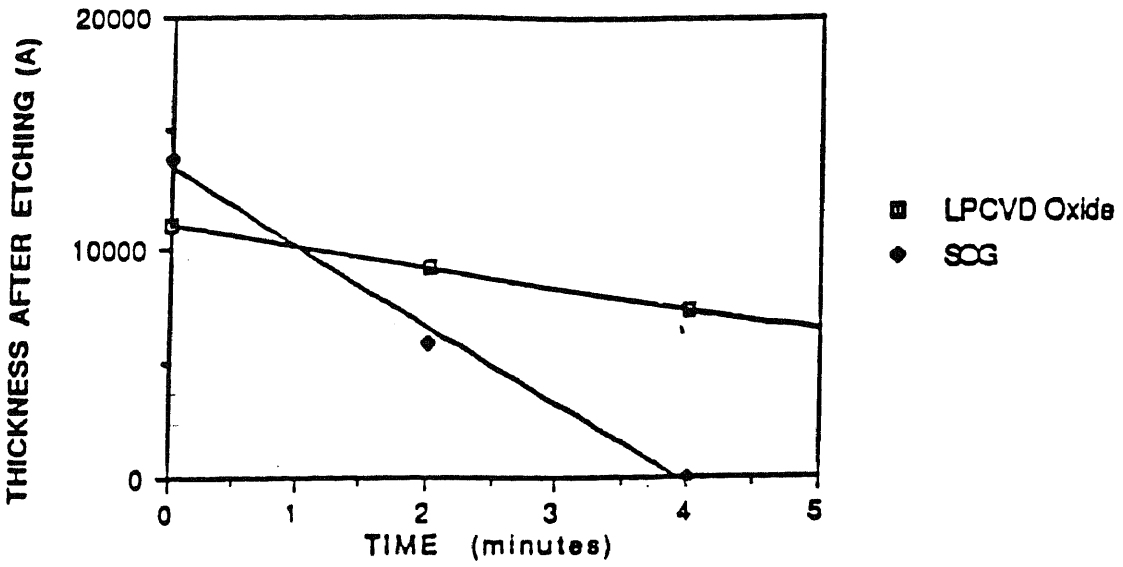


Figure 5.1 Differential Thermal Analysis of SOG [56]

evaporated at about 100°C. The SOG material formed a network of Si-O bond at the range between 250°C and 300°C and the SOG layer was condensed at 400°C.

The high etch rate of SOG in HF is a very desirable property as a sacrificial layer for surface micromechanical device applications. Figure 5.2 shows that the etch rate compared with LPCVD Oxide. High etch rate makes the SOG very suit for sacrificial layer. It can be etched out before the other material be etched.

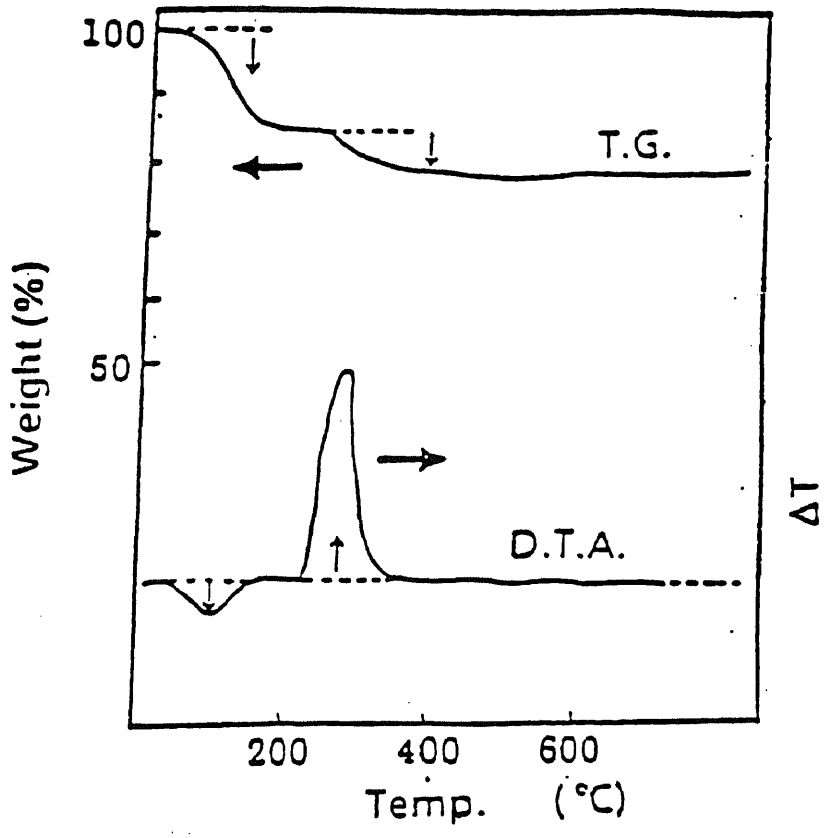


Figure 5.2 Etch rate comparison between LPCVD oxide and doped SOG (in BHF) [56]

5.3 The Corrugated Silicon Diaphragms Structure

The method used to fabricated these corrugated diaphragms has been to etch a series of grooves on the top surface of the SOG. These grooves can be isotropically or anisotropically etched, depending on the desired final diaphragm contour. If an isotropic etch is used, the grooves can follow almost any desired pattern, including circular, spiral, serpentine or radial.

An polysilicon is then deposited into the convoluted surface so that the polysilicon layer follows the etched contours. The SOG is then etched out through the windows we open on the polysilicon layer, left the desired corrugated cross-section, a free-standing diaphragm.

The precise shape of the corrugation profile is not particularly important in determining the characteristics of the diaphragm. The design described here shows that this structure causes stress concentration in the corners of the diaphragm, which considerably reduces its maximum deflection.

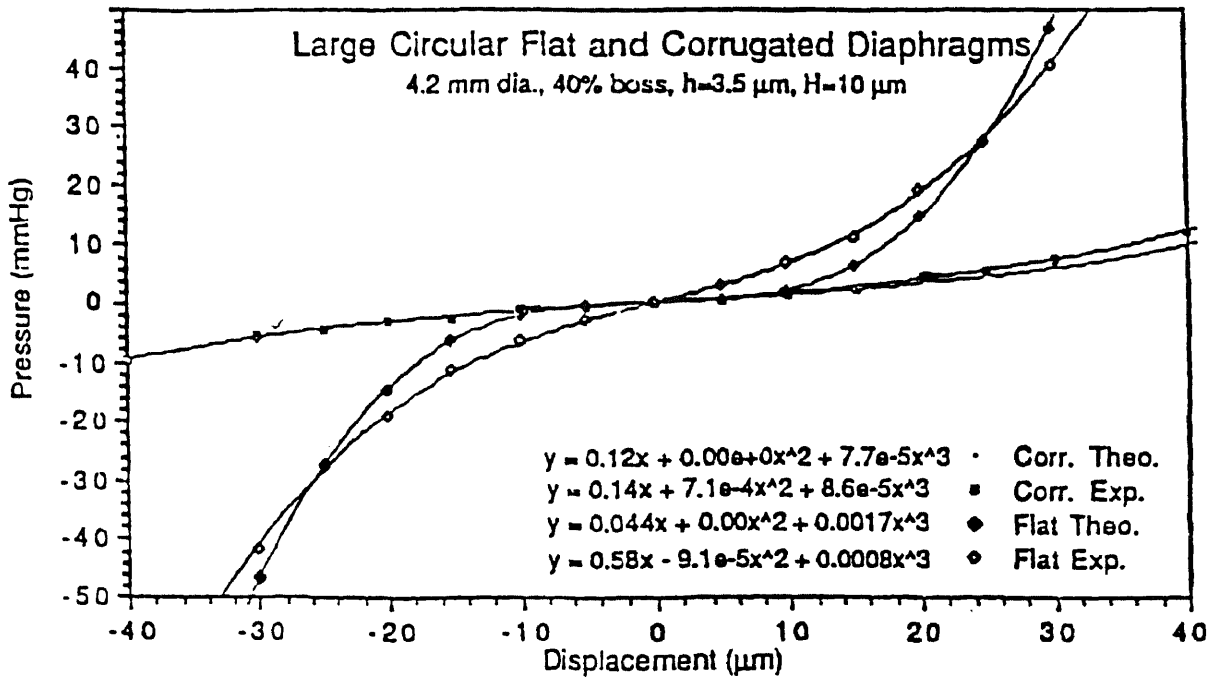


Figure 5.3 Deflection characteristics of flat and corrugated diaphragms [57]

CHAPTER SIX
APPLICATION

This device has great potential of application. It can be used in configurations within conventional cavities, solid etalons, and fiber-optic resonators. General application areas include atomic spectroscopy area, astronomy and astrophysics area, metrology, optical bistability, velocimetry, infrared, sensors, plasma physics and miscellaneous devices. Here we describe a typical usage as a wavelength-selective filters for single-mode fiber wavelength division multiplexing (WDM) systems.

In recent years optical fiber technology for telecommunication has progressed rapidly. The attenuation of silica fiber has been reduced to as low as 0.2 dB/km by the exploitation of the low-loss window at 1.55μm wavelength. Similarly, new source and detector technologies have enabled systems to be demonstrated with data rates exceeding 1 G Bit/s, spanning a hundred kilometers and more. This FPI device has application within these systems.

It has long been recognized that the ultimate theoretical transmission capacity of optical fiber, and particularly single-mode fiber, is extremely high. Consequently, attention has been directed toward the maximal utilization of the bandwidth by the use of: (a)single-mode fiber, (b)line-narrowed laser source, (c)heterodyne detection systems, (d)wavelength division multiplexing, (WDM), and more recently (e)optical frequency division multiplexing (OFDM). WDM may be distinguished from OFDM in that each channel is allocated to a physically separate optical source. OFDM is based on the use of a single narrow line source, from which are derived optical subcarriers, onto which each information channel is separately modulated.

As is commonly found, conceptual developments relating to WDM system configurations and devices are far in advance of actual hardware. Consequently, in spite of a plethora of research papers describing prototypes, comparatively few components are

commercially available. The reasons are partially attributable to the complex optomechanical requirements of the multiplexer components. The function of a wavelength division multi/demultiplexer is to perform a spatial/spectral transformation. In the case of a multiplexer, the radiation from n spatially separate sources emitting at different wavelengths is coupled into a single fiber. Commonly this transformation is performed in parallel, providing a communication link supporting n separate channels. Should the transformation be performed serially, the device would be termed a wavelength switch. Hence it may be seen that optical multiplexing and this form of switching are closely allied. The demultiplexer performs the complementary function, separating spatially according to wavelength the n channels. This selection may be in parallel (n channels directed toward n detectors simultaneously), or serially (one of n channels directed to a single detector). In general, parallel elements are multiple fiber devices; serial elements are tunable and therefore require a control system.

Although the Fabry-Perot Interferometer was first reported in the last century, the device was not widely used. The device of this thesis could be used in here. The spacing between successive peaks being termed the free spectral range (FSR). To effect demultiplexing, one of the transmission peaks is tuned to the wavelength of the required channel. Provided that the system spectral span is less than the nominal FSR of this device, unambiguous channel selection is possible. The passband width and FSR may be chosen by a suitable cavity spacing. Since WDM systems have channel spacing of the order of nanometers, the small mirrors spaced characteristic of this device is very suit for this application. OFDM system channel spacing are measured in megahertz, the consequence being that FPI demultiplexers would have cavities ranging from a few centimeters to many meters long. The selectivity of the FPI is determined by the finesse, a parameter which is nominally determined by the reflectance of the mirrors, and degraded by cavity losses produced by mirror misalignment and defects. The device is tuned by changing the optical path length in the cavity by means of electrostatic actuation.

This device (fig. 6.1) consists of two single-mode fibers mounted in this device. This device lends itself to the use of intracavity electrooptic materials. While many FPI devices are relatively exotic and require large voltages to induce a sufficient phase change, this device just need low voltage and very small space. This tunable FPI could work as a optical filter to filter the frequency range we intend and then reflect to the output fiber.

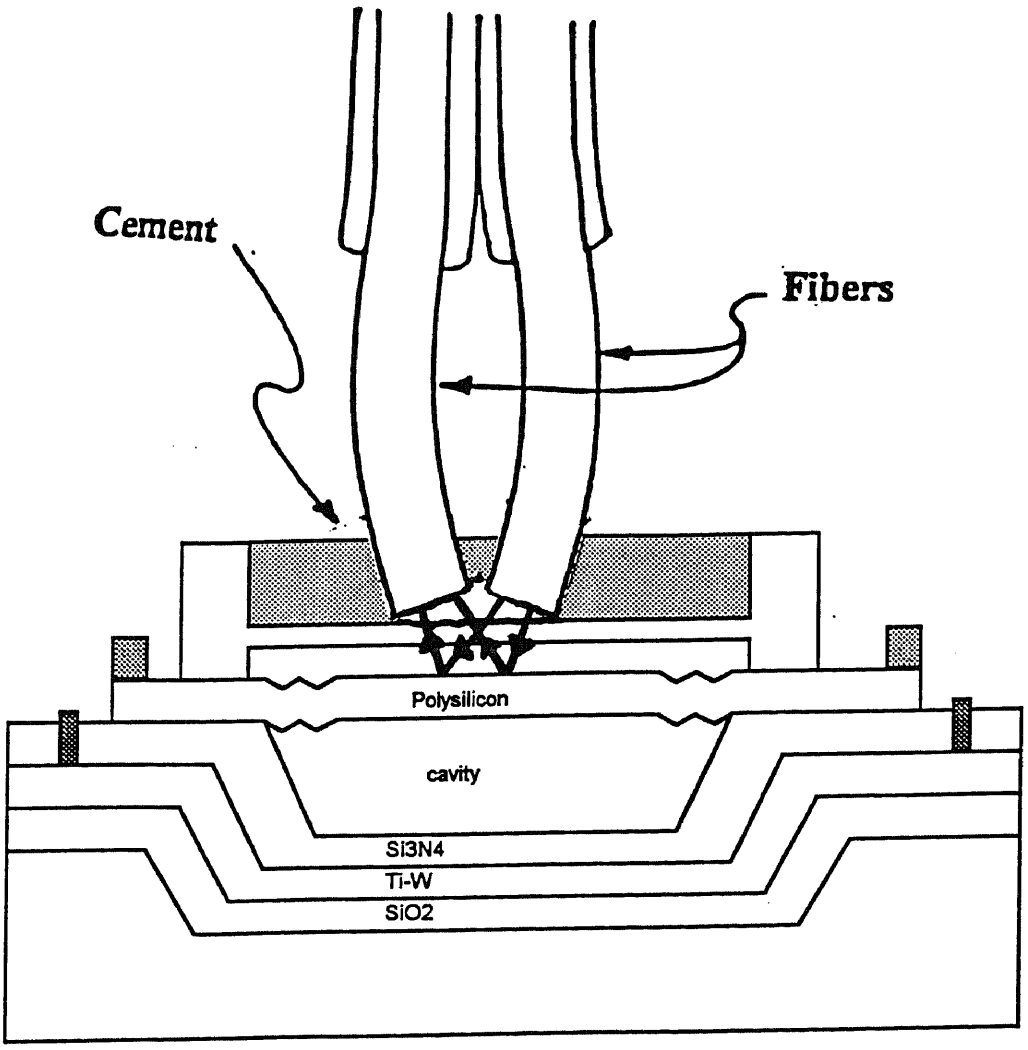


Figure 6.1 An application of this device: A incident light, from the upper fiber as drawn, is selectively reflected to the lower fiber and transmitted to a spectrum analyzer.

CHAPTER SEVEN
CONCLUSIONS

The use of silicon micromachining has resulted in a high-performance Fabry-Perot interferometer. This fabrication technique allows the inclusion of electrodes to tune and adjust the parallelism, along with the ability to specify the initial gap of the device closely. The ability to batch fabricate these devices should result in a substantially less expensive device than is currently available. The use of an sacrificial layer and a corrugated support in these third-generation devices has resulted in a device with increased performance and reduced die size. These devices have significant benefits of being considerably smaller than other types of FPI and operate at low drive voltages. They should prove to be of use as wavelength-selection components in optical fiber communication systems. The economies in processing for this device make it an excellent candidate for application as an optomechanical device.

Using this process, free-standing structures remained flat and all the optical and mechanical requirements have been met. By careful design a process compatible with standard processing has been proposed. Initial calculations indicate that the cap film can be moved by 0.32μm with a voltage of 5V. The high sensitivity of the filter characteristic of this device to voltage opens many further application opportunities.

Compared with the previous published similar device, this present device has the advantages of easy making and low voltage required.

Table 7-1 Compared three different design FPI

	Proposed Design	Ref[45]	Ref[58]
Operation Voltage	5v	70v	175v
Wave Length	1.3μm	1.3μm	1.5μm
Technique	Monolithic	Wafer Bonding	Wafer Bonding

APPENDIX A

PHYSICAL LAYOUT FOR MCNC FOUNDRY

MCNC Center for Microelectronic Systems Technologies

Process and Design Specification for the MEMS Multiproject Run
2 Layer polysilicon surface micromachine technology

The attached document is the final design rules and process specification for the first multiproject run of the 2 layer polysilicon micromachine process at MCNC. The project is being sponsored by DARPA, and is open to all US companies, universities and organizations.

The cost structure for the project is as follows:
Each 1 cm x 1 cm mask position costs

$500 if a cif, GDSII or stream-file tape is provided to MCNC by November 30, 1992
$1000 if layout support from MCNC is requested (or tape conversion labor in excess of two hours is required)

The lot will be fabricated starting January 15, 1993, with anticipated delivery of up to 20 die/ mask position around February 20, 1993.

The die will be returned to the customers unreleased. If you are not able to (or do not wish to) perform the release step in your own facility, arrangements can be made for the release to be performed at MCNC.

For additional information, clarification or questions contact:
Karen Markus
Program Manager: MEMS Technology Applications
(919) 248-1437
(919) 248-1455 fax
markus@mcnc.org (email)

Process Sequence

The process sequence for the multiproject MEMS run is an enhanced 2-poly, 2-sacrificial oxide process. A silicon nitride layer, for device -to- substrate isolation, and a metalization layer, for improved electrical performance, are also included. Dimpling of the polysilicon 1 layer is provided to reduce the surface area for stictioning friction. The thick oxide etch layer (COL) allows anchoring of polysilicon 2 to the substrate or nitride.

The basic process is outlined below. Thicknesses are targets, and the design rules for each lithographic layer are provided in section 2.

Starting wafers: 100 mm N-type Si, (100) orientation, ~1 Ω-cm resistivity

Deposit 2500Å low stress Si_xN_y
Coat with positive photoresist, and expose level 10 (CSN)
RIE etch nitride and piranha strip PR
Deposit 2.0 µm oxide - first oxide (High etch rate material)

Coat with positive PR and expose level 20 (COF) (20 aligns to 10)
RIE first oxide and piranha strip PR

Coat and expose level 40 - dimples (COS) (40 aligns to 20)
Wet etch dimples - target depth 3500Å
Piranha strip PR
Deposit 2.0 µm polysilicon - first polysilicon
Deposit 500Å hard mask and phosphorous dope the oxide

Coat and expose level 50 - first poly (CPF) (50 aligns to 20)
RIE etch hard mask LTO
RIE etch polysilicon
Solvent strip PR
Deposit 5000Å oxide - second oxide

Coat and expose level 60 - thin oxide (2) etch (COT) (60 aligns to 50)
RIE etch thin oxide (openings for poly 2 - poly 1 connection)
Piranha strip PR

Coat and expose level 90 - thick oxide (2) etch (COL) (90 aligns to 50)
RIE etch thick oxide (openings for Poly 2 - substrate or nitride connection)
Piranha strip PR
Deposit 1.5 µm polysilicon - second poly
Deposit 500 Å hard mask and phosphorous dope the oxide
Anneal at 1050 °C - 1 hour

Coat and expose level 70 - second poly (CPT) (70 aligns to 60)
RIE etch hard mask LTO
RIE etch second polysilicon
Solvent strip PR

Coat with positive photoresist and expose level 80 - metal (CCM) (80 aligns to 70)
Imtek bake and flood expose for reverse image pattern
Deposit () Al metal
Acetone liftoff metal level
Anneal 400 °C - 30 minutes

Protective coat wafer frontsides
Remove polysilicon (and nitride?) layers from wafer backsides
Dice wafers and sort die
Solvent clean die to remove frontside protection layer
Die packs delivered with die ready for release processing in 49% HF.
Sacrificial oxide layer etchrate in 49% HF ~ 4 µm/minute

Design Rules

The design rules were developed to provide a guide for layout of 2 layer polysilicon structures for fabrication on the multiproject run. The minimum rules are given so as to ensure that all layout will remain compatible with MCNC's process tolerances. The 11 mandatory rules are highlighted with an asterix (*). All other rules are cautionary rules, which may be violated for certain desired applications.
Table 1 lists MCNC's layer name associated with a feature levels, the GDS layer number, and the minimum feature (line) and space allowable for that level. Figure 1 provides a composite cross sectional drawing of the 2 layer polysilicon process.
Table 2 lists the minimum allowed dimension for overlaps and interlevel spaces, and is followed by more detailed explanations of each rule. Figures 2 - 5 illustrate the rules in table 2.
Terminology is consistent with the process outline above. If there are additional rules you would like defined, or if you wish clarification on existing rules, please contact MCNC.

Level	MCNC layer name	GDS layer number	Minimum line	Minimum space
*Nitride	CSN	42	2.0	2.0
*First oxide	COF	43	2.0	3.0
*Dimple	COS	50	2.0	3.0
*First poly	CPS	45	2.0	2.0
*Thin oxide	COT	47	2.0	2.0
*Thick oxide	COL	52	2.0	3.0
*Second poly	CPT	49	2.0	2.0
*Metal	CCM	51	2.0	2.0

Figure 1: Cross sectional view of 2 polysilicon process

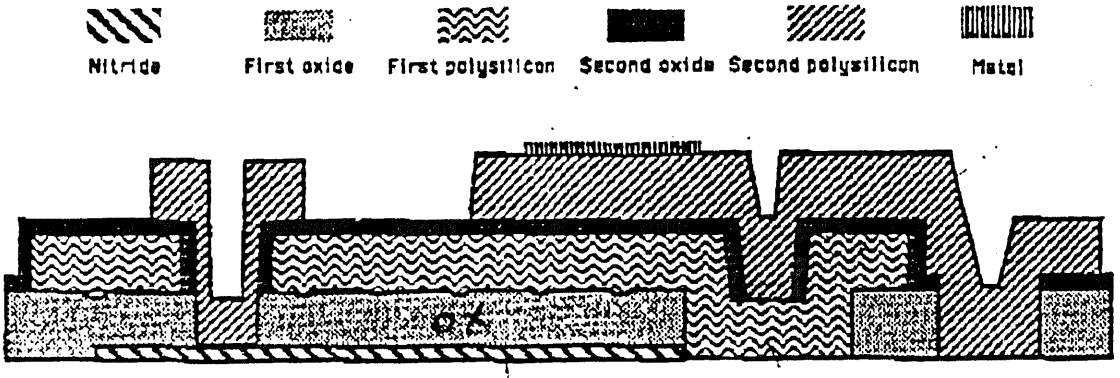


Table 2: Design rules for overlap and interlevel spacings

Rule	Reference to figures (figure # - rule letter)	Minimum value (μm)
Nitride border of oxide 1	2-A	4.0
Nitride overlap of poly 1	2-E	4.0
Nitride overlap of thin oxide 2 cut	3-H	5.0
Nitride overlap of thick oxide 2 cut	4-I	5.0
Nitride overlap of poly 2	5-O	4.0
Thick oxide 2 cut border of nitride	5-T	4.0
Dimple to oxide 1 space	2-B	3.0
Poly 1 overlap outside oxide 1	2-C	4.0
*Poly 1 overlap inside oxide 1	2-D	5.0
Poly 1 overlap of thin oxide 2 cut	3-F	4.0
Poly 1 space to thin oxide 2 cut	3-G	3.0
Poly 1 space to thick oxide 2 cut	4-J	3.0
Poly 2 overlap outside thick oxide 2 cut	4-K	5.0
*Poly 2 overlap inside thick oxide 2 cut	4-L	5.0
Poly 2 overlap outside thin oxide 2 cut	4-M	4.0
Poly 2 overlap inside thin oxide 2 cut	4-N	5.0
Poly 2 overlap outside oxide 1 cut	5-P	5.0
Poly 2 overlap inside oxide 1 cut	5-Q	5.0
Poly 2 border of metal	5-S	3.0
Poly 2 space to poly 1	5-U	3.0
*Lateral etch holes in poly1 and poly 2	6-V	≤30 (max value)

Explanation of rules A - V:

Nitride border of oxide 1 - 2-A
The amount of nitride border to ensure that the entire oxide 1 opening is on nitride.

Nitride overlap of poly 1 - 2-E
The amount of nitride overlap to ensure that all the poly 1 is on nitride.

Nitride overlap of thin oxide 2 cut - 3-H
The amount of nitride overlap to ensure that the entire thin oxide 2 opening is on nitride.

Nitride overlap of thick oxide 2 cut - 4-I
The amount of nitride overlap to ensure that the entire thick oxide 2 opening is on nitride.

Nitride overlap of poly 2 - 5-O
The amount of nitride overlap to ensure that all the poly 2 is on nitride.

Thick oxide 2 cut border of nitride - 5-T
The amount of overlap of the thick oxide 2 opening of the nitride to ensure that the silicon substrate is exposed as well.

Dimple to oxide 1 space - 2-B
The space required between an oxide 1 opening and a dimple to ensure that the dimensions of the oxide 1 opening are not altered.

Poly 1 overlap outside oxide 1 - 2-C
The amount of poly1 overlap outside an oxide 1 opening to ensure that the entire oxide 1 opening is covered with poly 1.

Poly 1 overlap inside oxide 1 - 2-D
The amount of poly 1 overlap inside an oxide 1 opening to ensure no poly 1 stringers.

Poly 1 overlap of thin oxide 2 cut - 3-F
The amount of poly 1 overlap to ensure that the entire thin oxide 2 opening is on poly 1.

Poly 1 space to thin oxide 2 cut - 3-G
The space required between a thin oxide 2 opening and a poly 1 feature to ensure that the poly1 remains covered with oxide.

Poly 1 space to thick oxide 2 cut - 4-J
The space required between a thick oxide 2 opening and a poly 1 feature to ensure that the poly1 remains covered with oxide.

Poly 2 overlap outside thick oxide 2 cut - 4-K
The amount of poly 2 overlap outside a thick oxide 2 opening to ensure that the entire thick oxide 2 opening is covered with poly 2.

Poly 2 overlap inside thick oxide 2 cut - 4-L
The amount of poly 2 overlap inside a thick oxide 2 opening to ensure no poly 2 stringers.

Poly 2 overlap outside thin oxide 2 cut - 4-M
The amount of poly 2 overlap outside a thin oxide 2 opening to ensure that the entire thin oxide 2 opening is covered with poly 2.

Poly 2 overlap inside thin oxide 2 cut - 4-N
The amount of poly 2 overlap inside a thin oxide 2 opening to ensure no poly 2 stringers.

Poly 2 overlap outside oxide 1 cut - 5-P

The amount of poly 2 overlap outside an oxide 1 opening to ensure that the entire oxide 1 opening is covered with poly 2.

Poly 2 overlap inside oxide 1 cut - 5-Q

The amount of poly 2 overlap inside an oxide 1 opening to ensure no poly 2 stringers.

Poly 2 border of metal - 5-S

The amount of poly 2 border to ensure that the entire metal area is on poly 2.

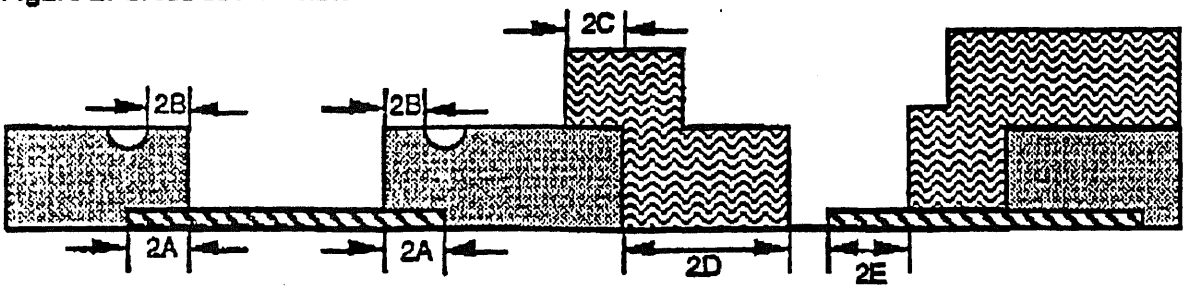
Poly 2 space to poly 1 - 5-U

The space required to between poly 2 and poly 1 to ensure that the features are separate.

Lateral etch hole in poly 1 and poly 2 - 6-V

Maximum spacing between holes opened in poly1 and poly 2 to allow dissolution of the SiO_2 layers

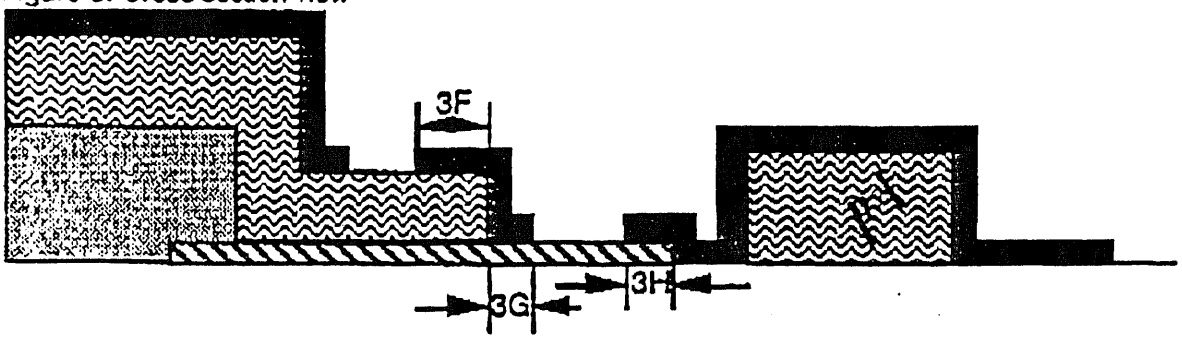
Figure 2: Cross section view



2-A: Nitride overlap of oxide 1 - 4.0 µm
2-B: Dimple to oxide 1 space - 3.0 µm
2-C: Poly 1 overlap outside oxide 1 cut- 4.0 µm
2-D: Poly 1 overlap inside oxide 1 cut - 5.0 µm
2-E: Nitride overlap of poly 1 - 4.0 µm

Not to scale

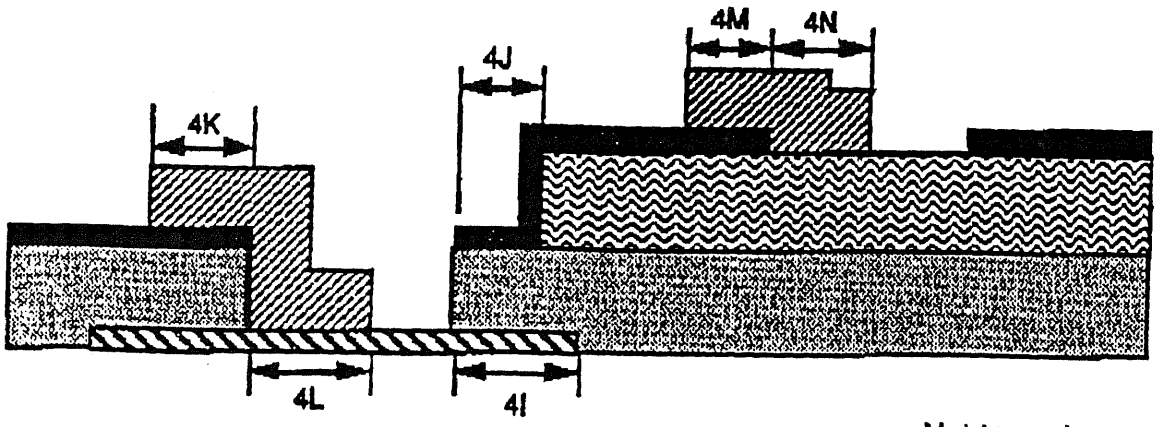
Figure 3: Cross section view



Not to scale

3-F: Poly 1 overlap of thin oxide 2 - 4.0 µm
3-G: Poly 1 space to thin oxide 2 - 3.0 µm
3-H: Nitride overlap of thin oxide 2 - 5.0 µm

Figure 4: Cross section view

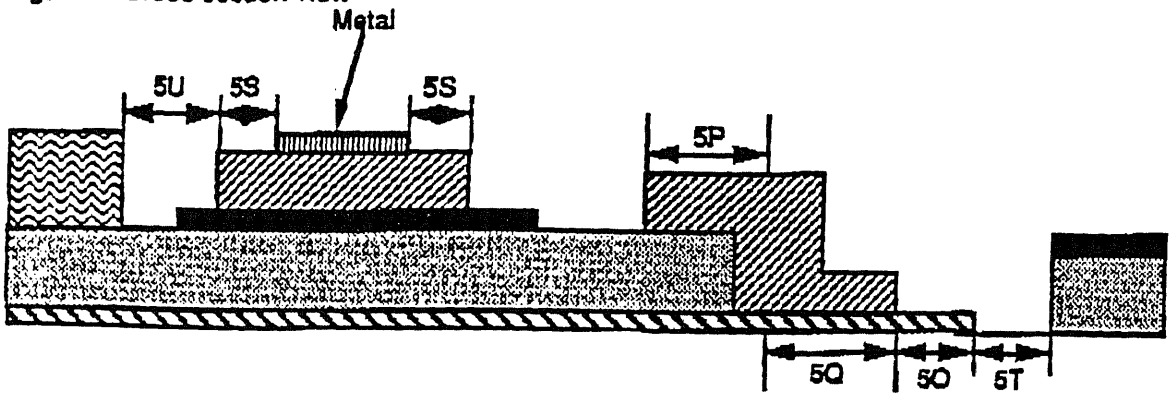


Not to scale

4-I: Nitride overlap of thick* oxide 2 cut - 5.0 µm
4-J Poly 1 space to thick oxide 2 cut- 3.0 µm
4-K: Poly 2 overlap outside thick oxide 2 cut - 5.0µm
4-L: Poly 2 overlap inside thick oxide 2 cut - 5.0 µm
4-M: Poly 2 overlap outside thin oxide 2 cut - 4.0 µm
4-N: poly 2 overlap inside thin oxide 2 cut - 5.0 µm

* thick oxide" is cut to substrate or nitride through both oxide 1 + oxide 2

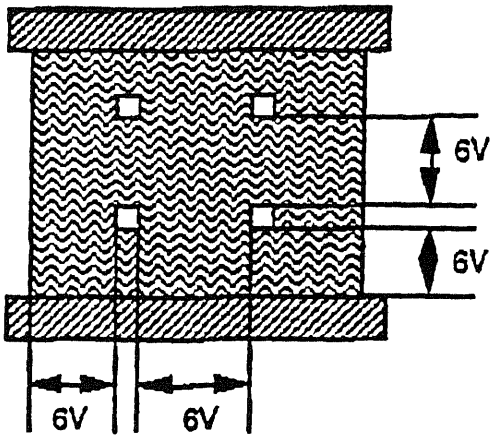
Figure 5: Cross section view



5-O: Nitride overlap of poly 2 - 4.0 µm
5-P: Poly 2 overlap outside oxide 1 cut - 5.0 µm
5-Q: Poly 2 overlap inside oxide 1 cut - 5.0 µm
5-S: Poly 2 border of metal - 3.0 µm
5-T: Thick oxide 2 cut border of nitride - 4.0 µm
5-U: Poly 2 space to poly 1 - 3.0 µm

Not to scale

Figure 6: Top view of (for example) poly 1 plate flanged by poly 2



Not to scale

6-V: Lateral etch holes in poly 1 and poly 2 - ≤40 µm

This rule ensures that the HF release etch has sufficient time to remove oxide from under all polysilicon layers. (rule applies equally to poly 1 AND poly 2)

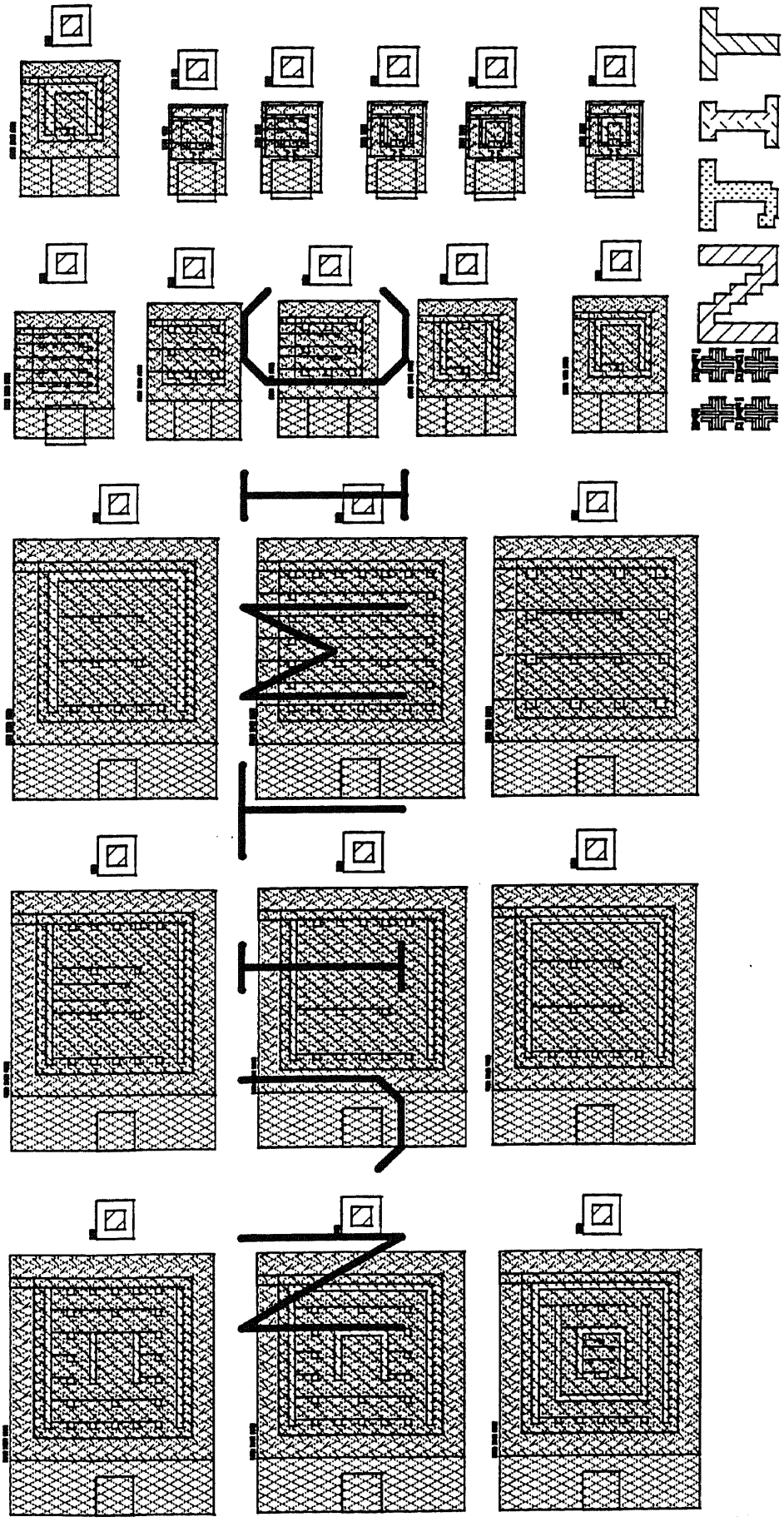


Figure A.1 Physical layout of device mask

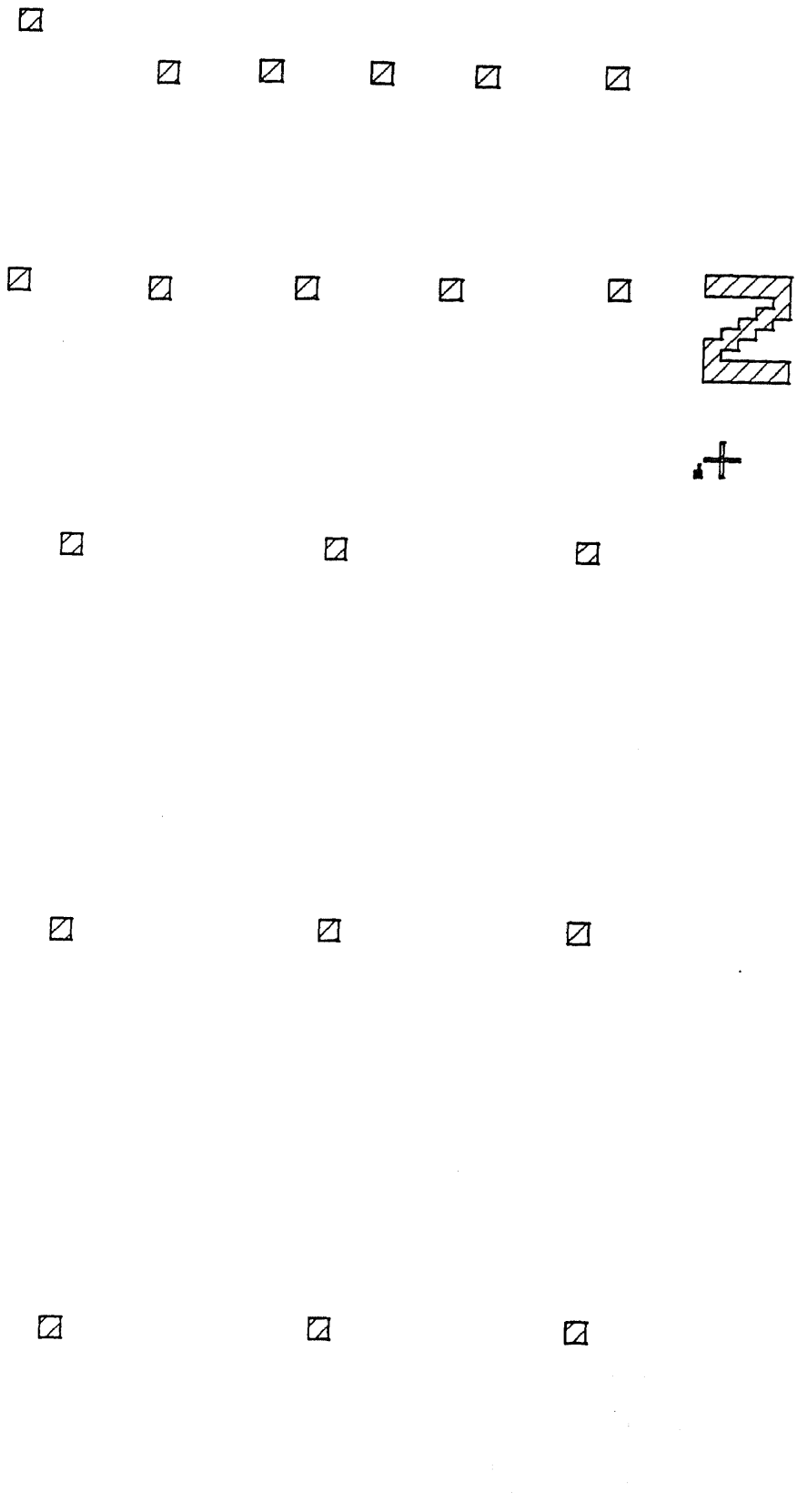


Figure A.1a Mask#1 for deposit low stress silicon nitride

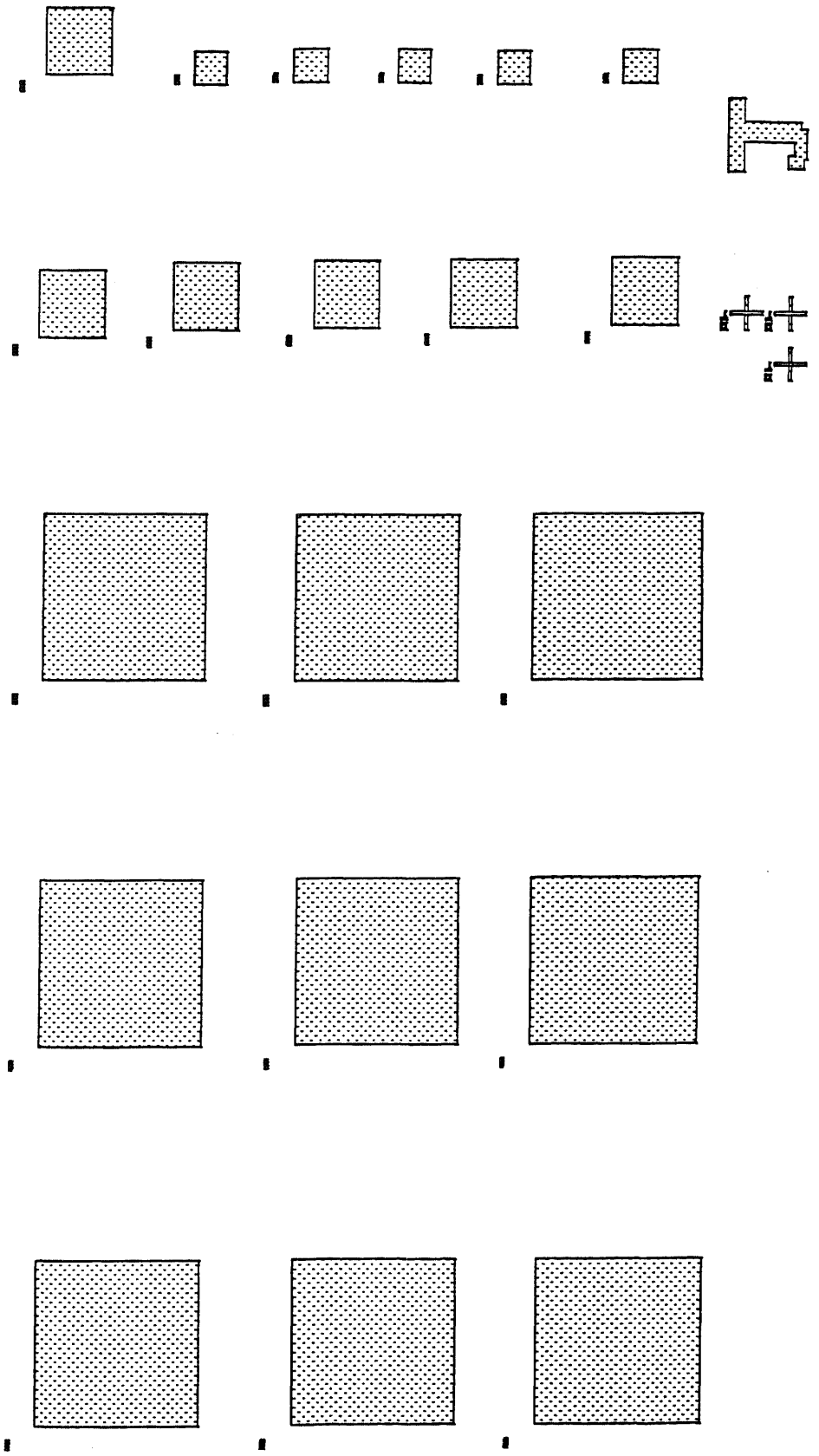


Figure A.1b Mask#2 for first oxide layer

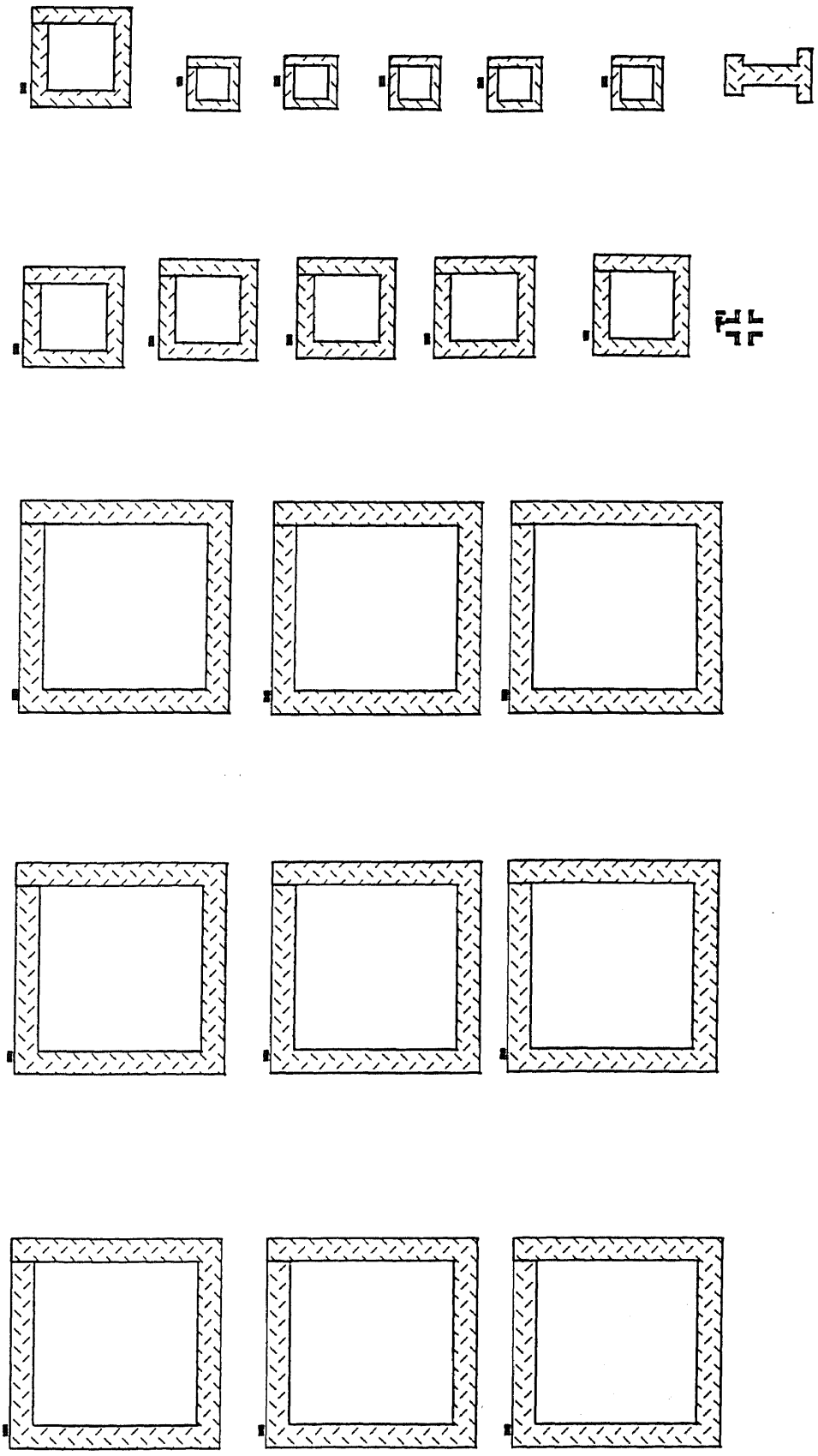


Figure A.1c Mask#3 for first polysilicon

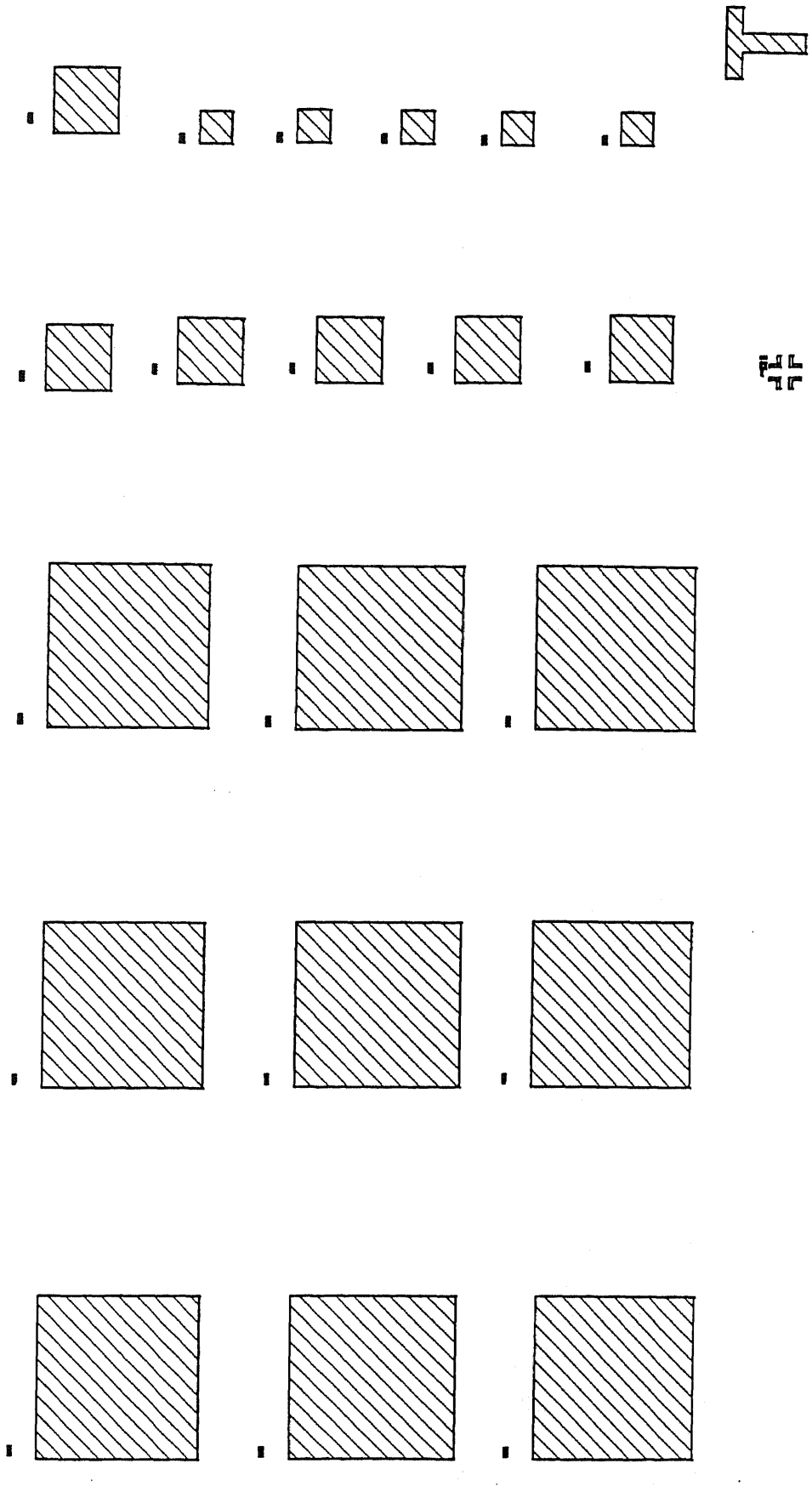


Figure A.1d Mask#4 for second oxide layer

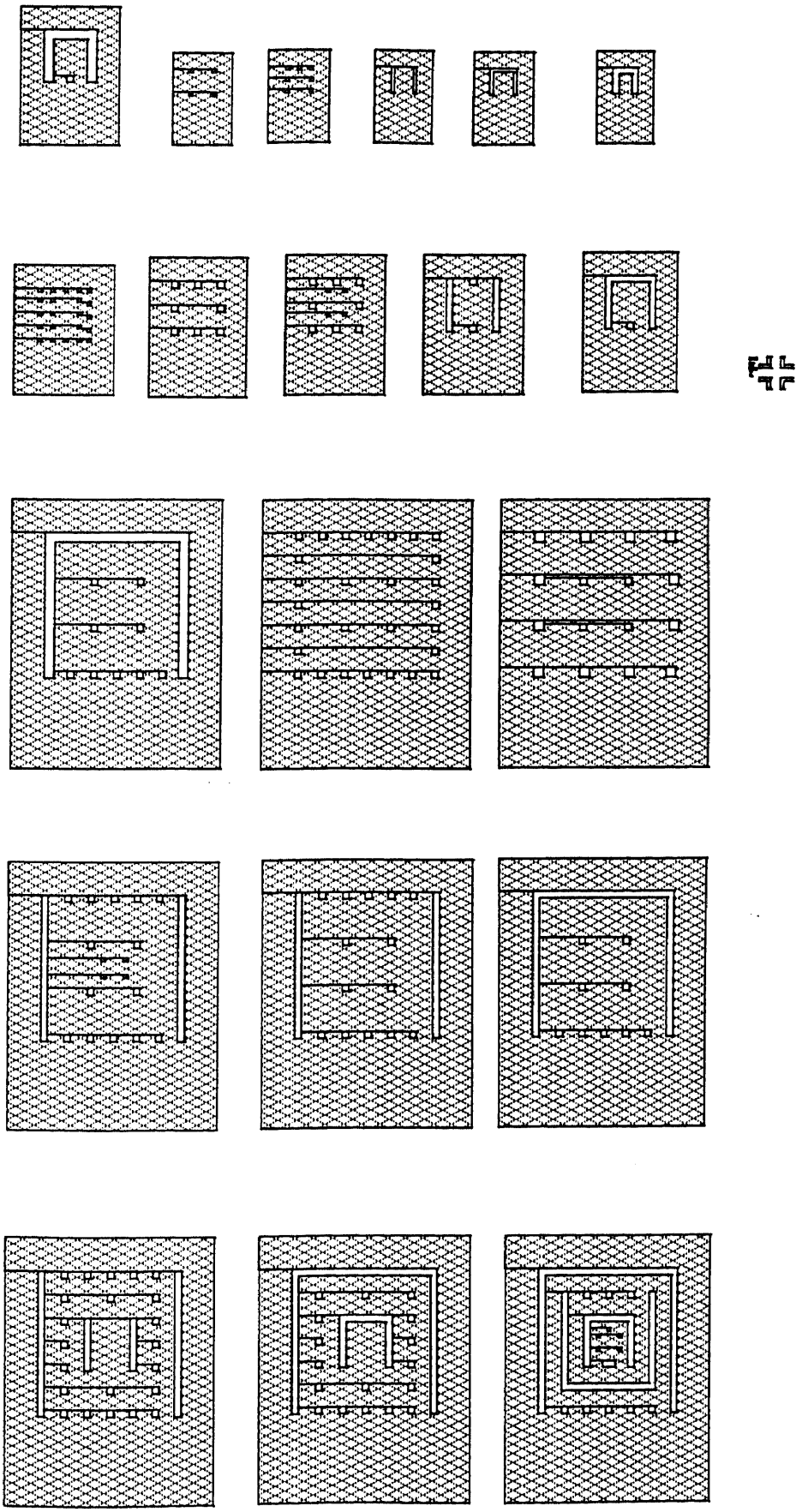


Figure A.1e Mask#5 for second polysilicon

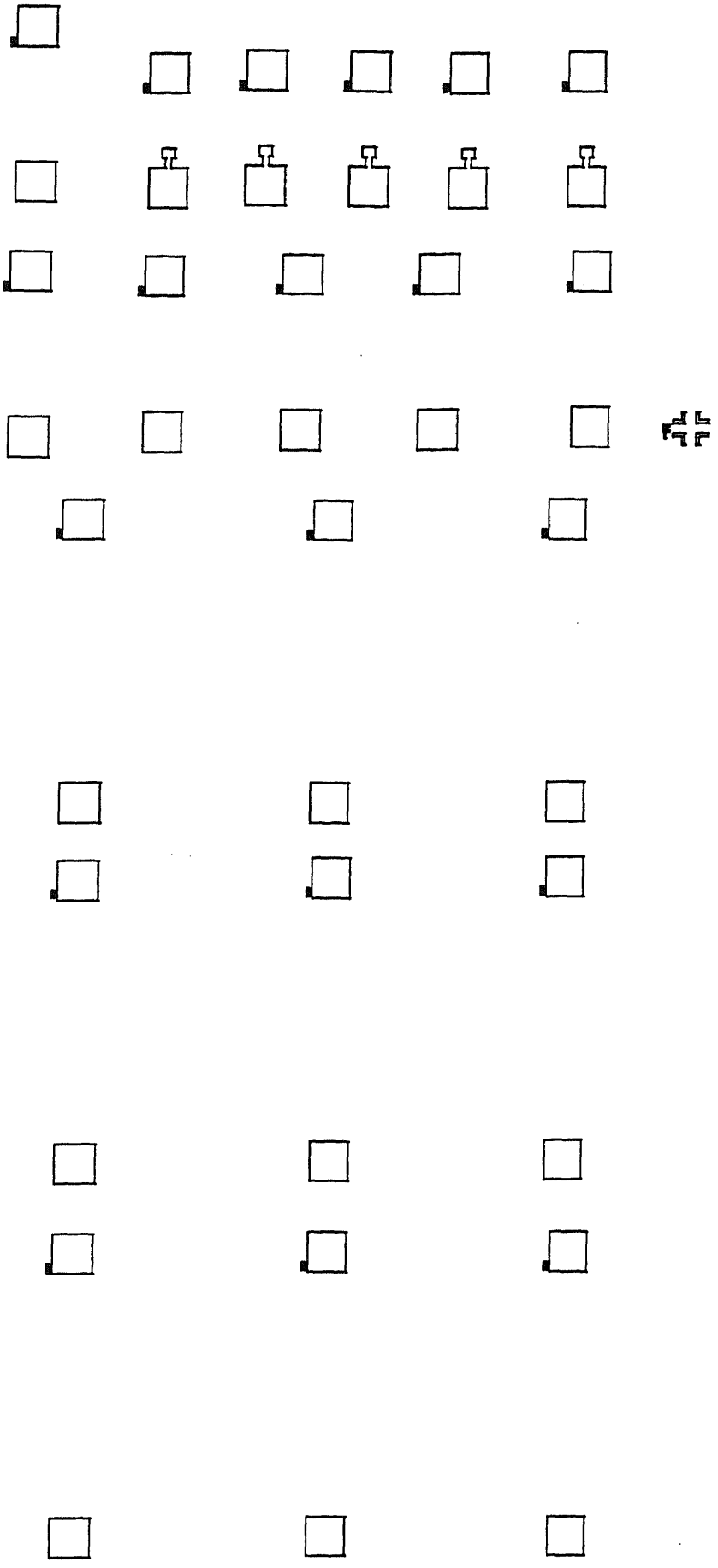


Figure A.1f Mask#6 for deposit Al metal

APPENDIX B

PHYSICAL LAYOUT FOR NJITMRC

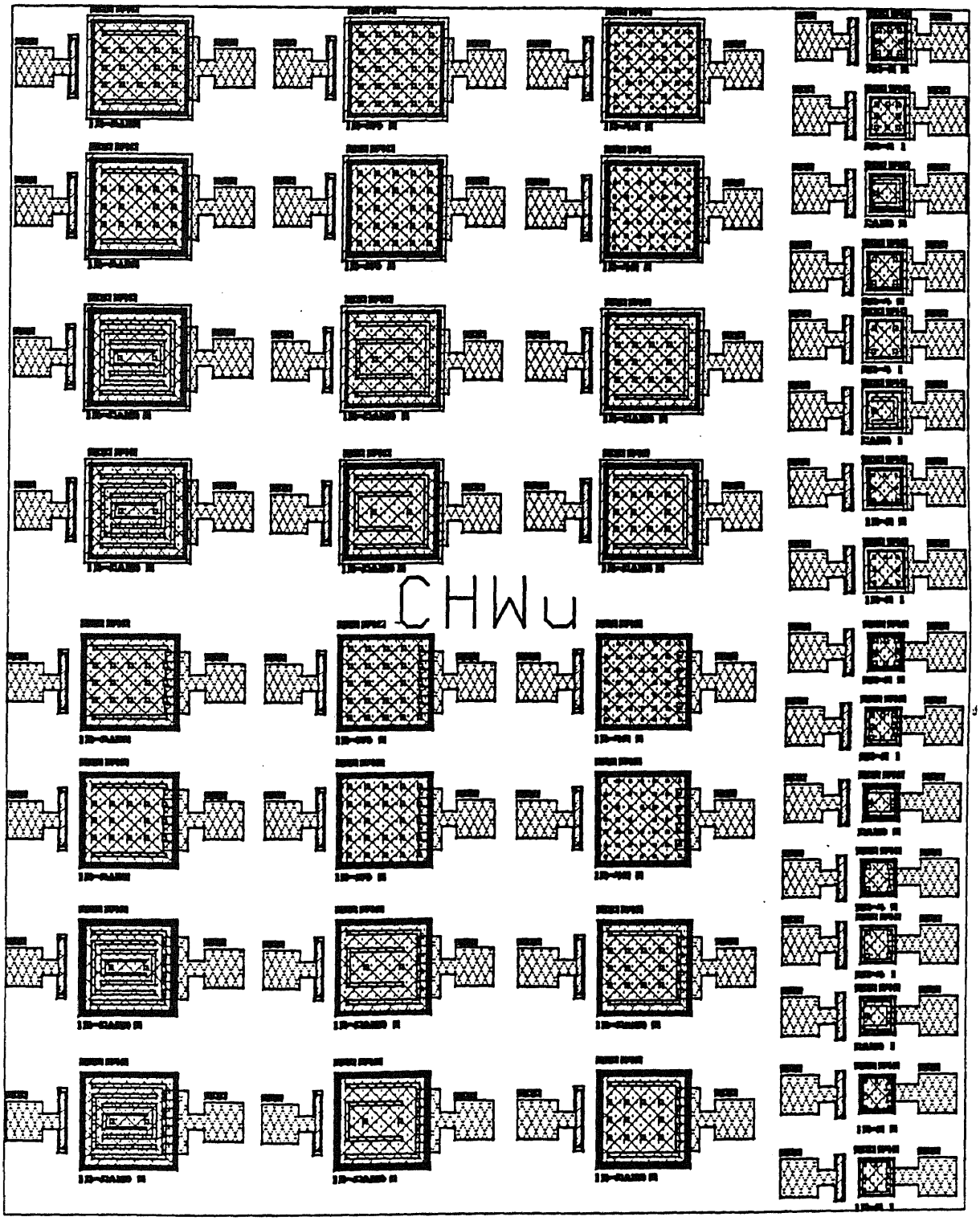


Figure B.1 Physical layout of device mask

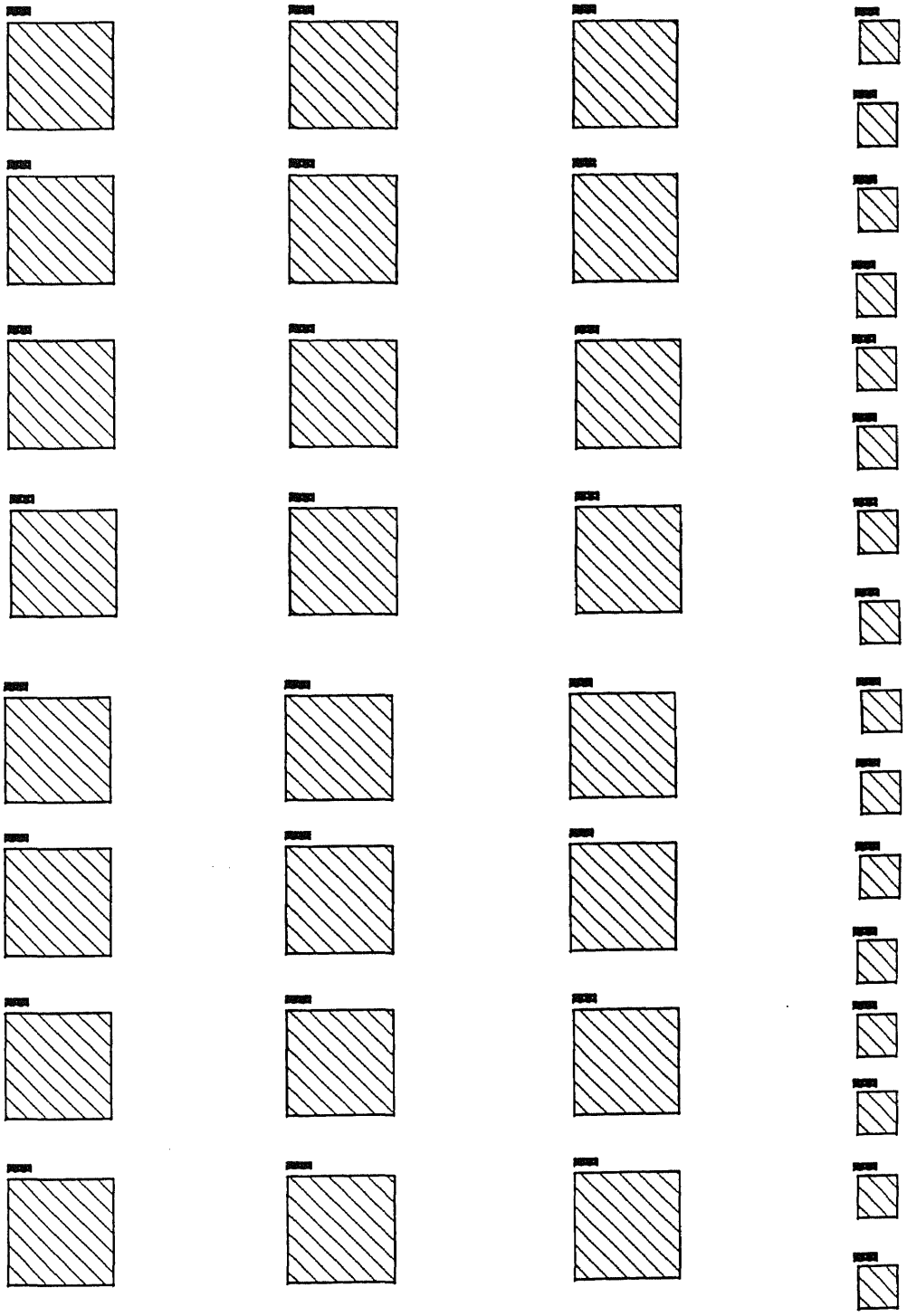


Figure B.1a Mask#1 for etch out the cavity

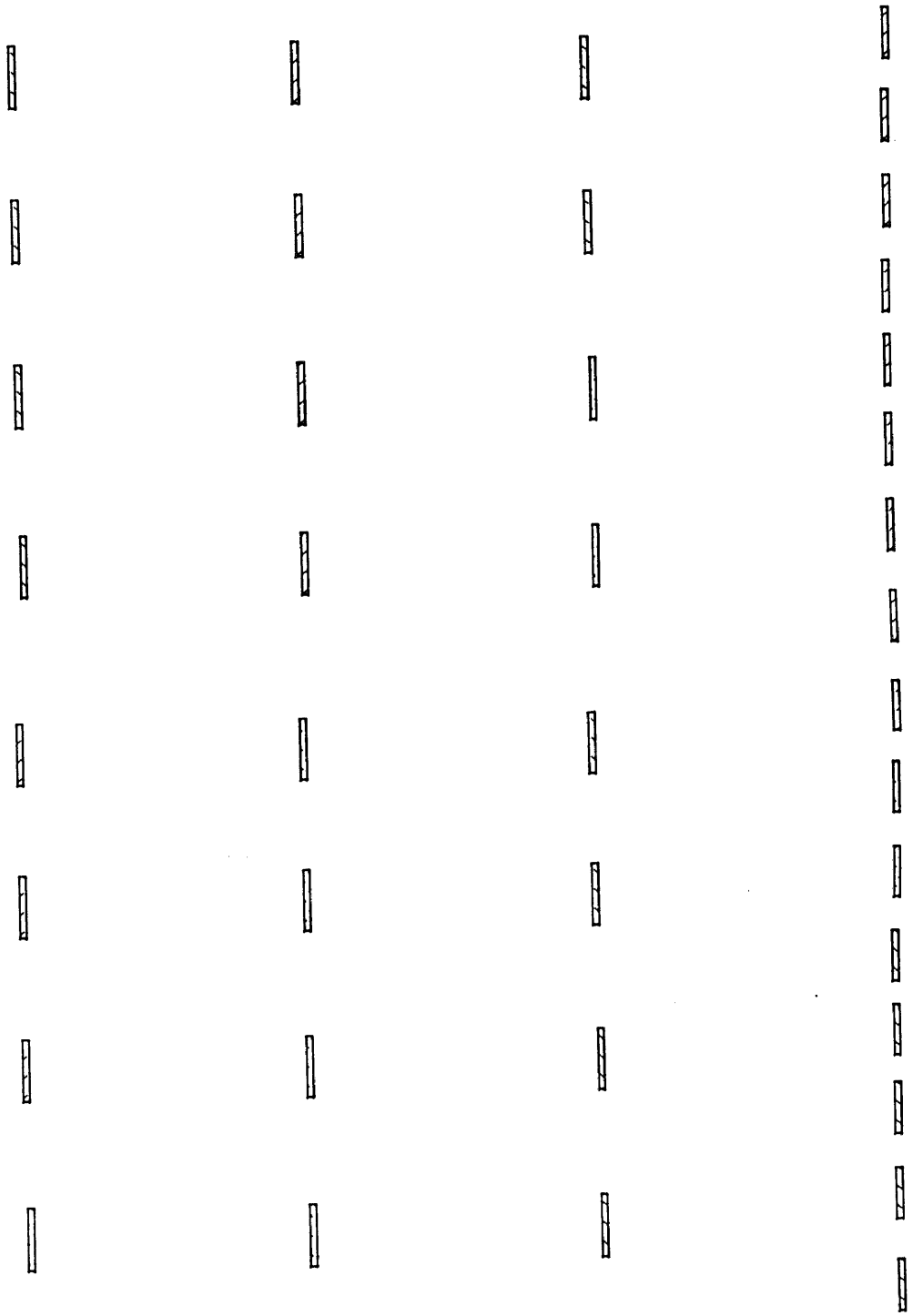


Figure B.1b Mask#2 for contact to the lower electrode

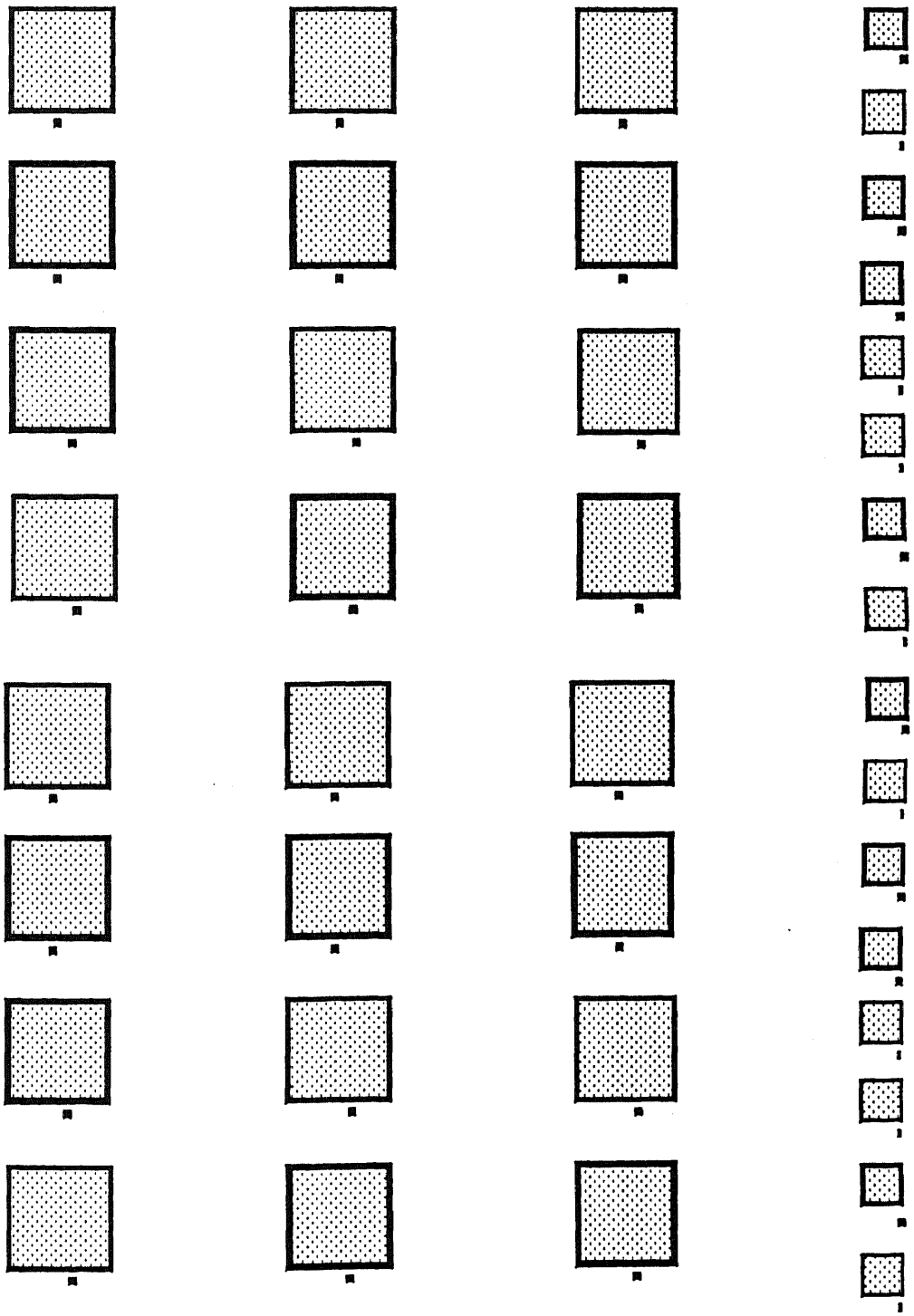


Figure B.1c Mask#3 for planerize the SOG and corrugated construction

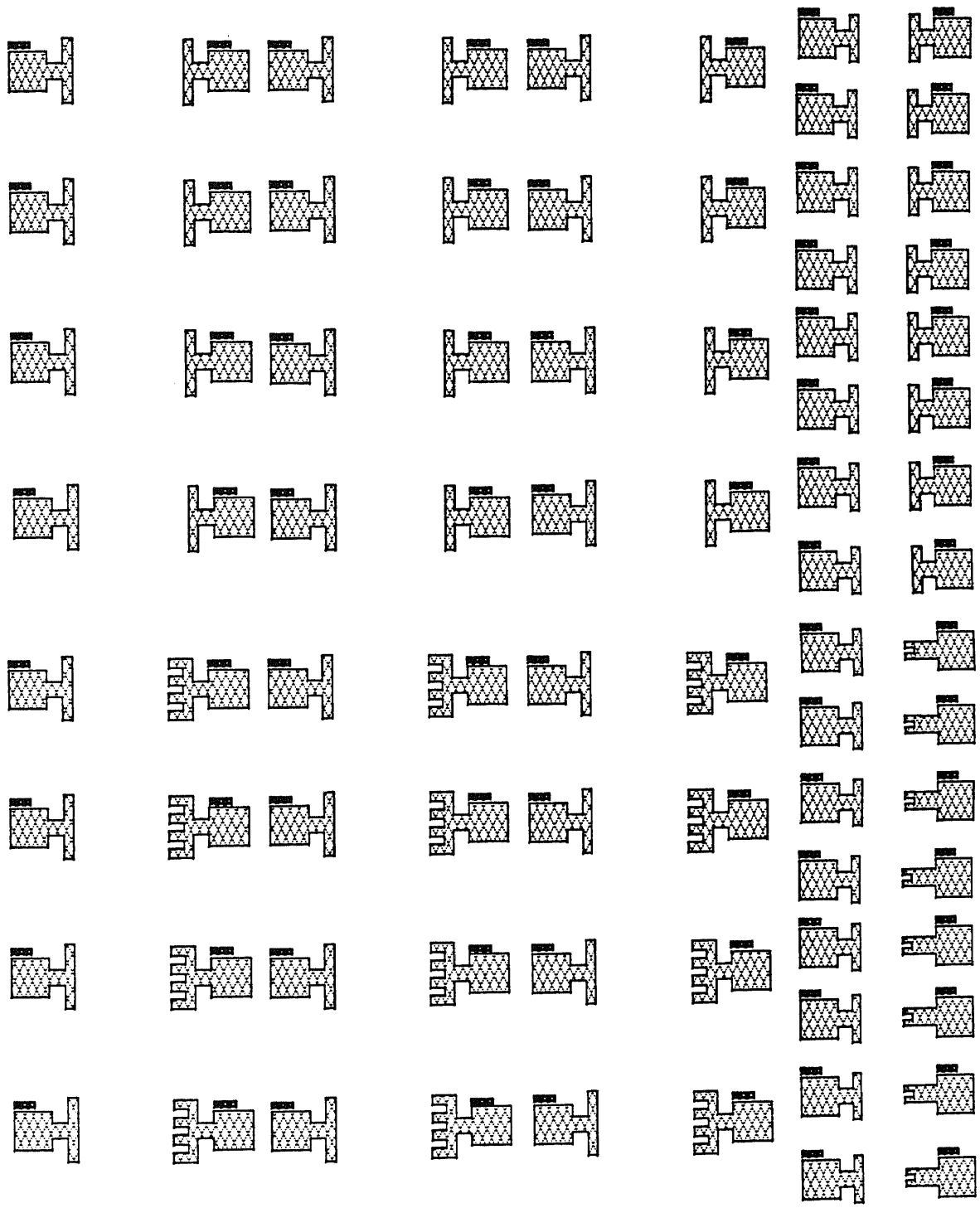


Figure B.1d Mask#4 for aluminum removal

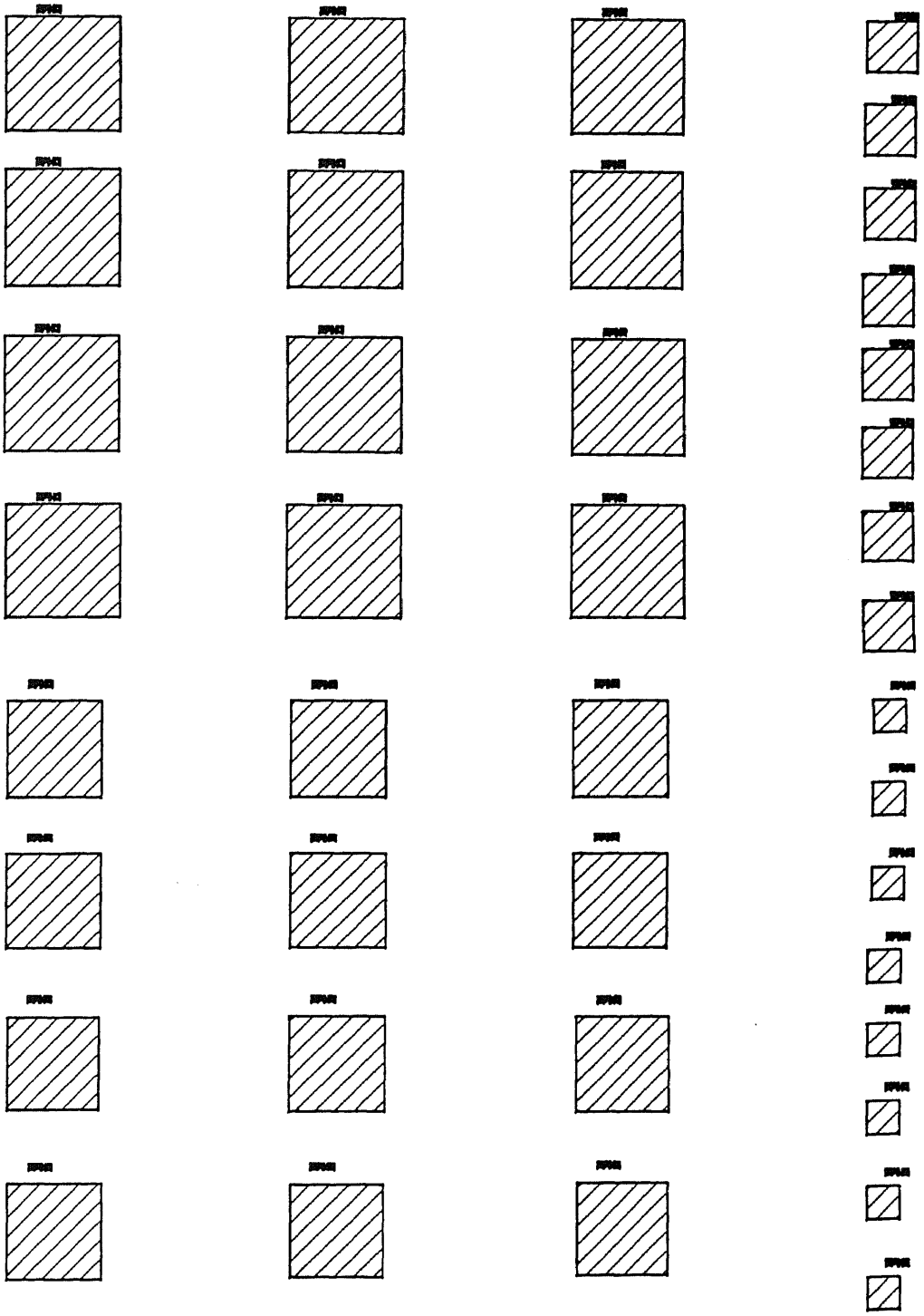


Figure B.1e Mask#5 for deposit polysilicon

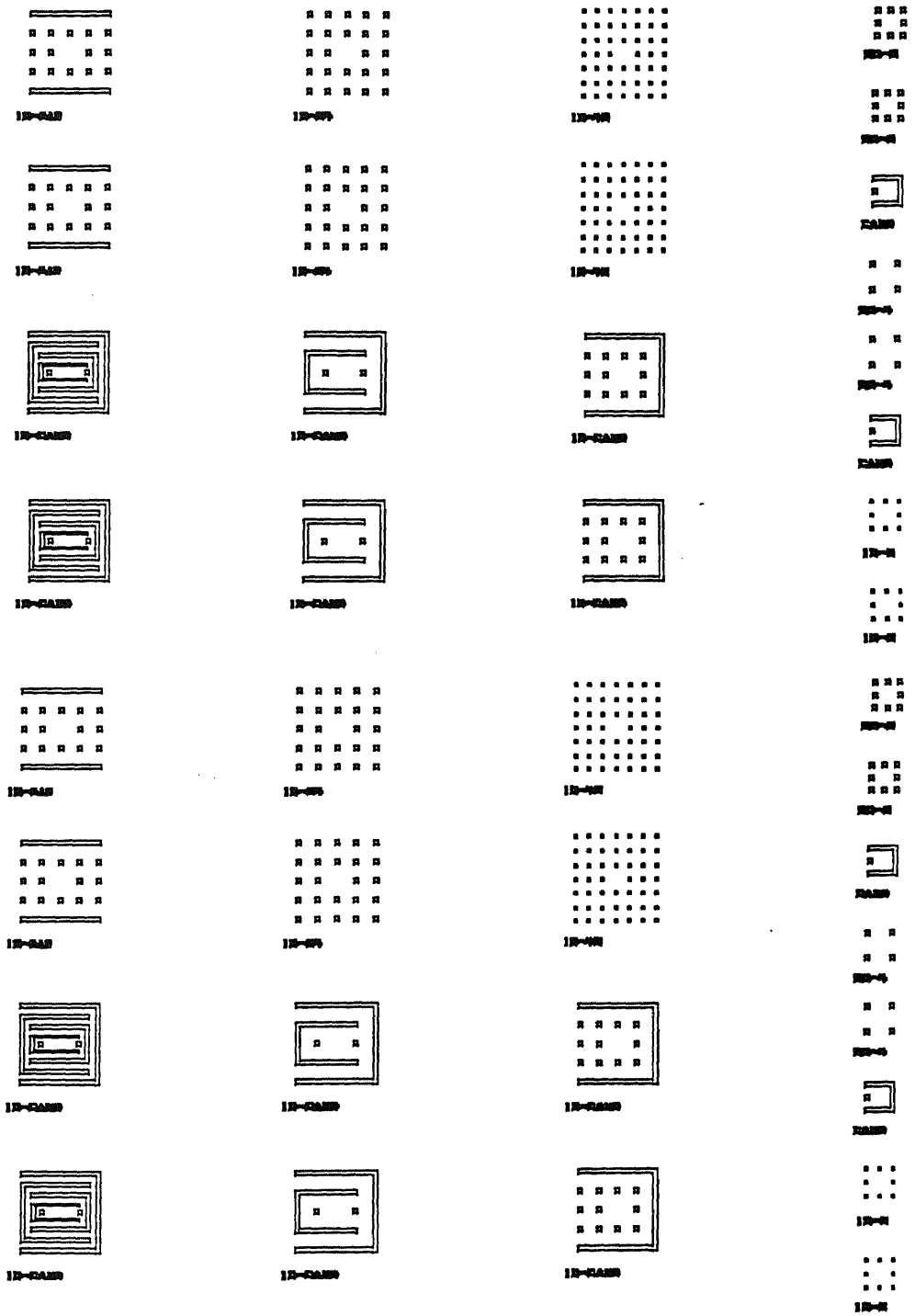
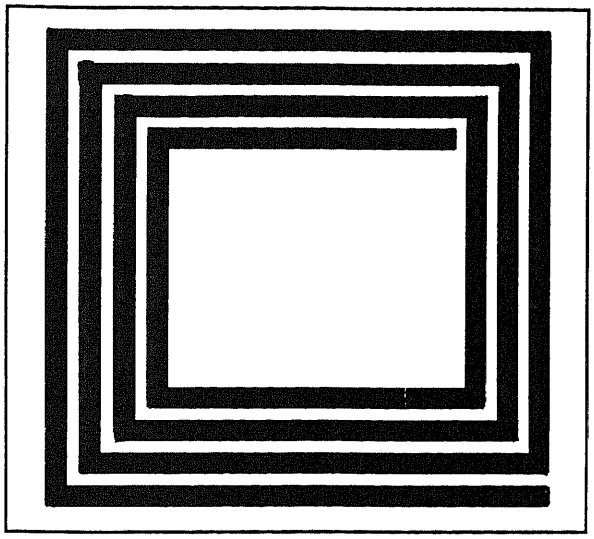


Figure B.1f Mask#6 small holes for etchant go into the cavity

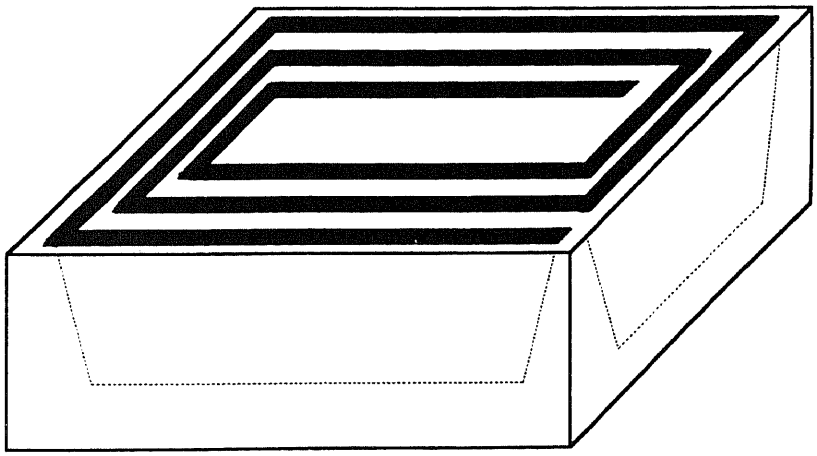
APPENDIX C

SEVERAL DESIGN FOR OPTIMAL POLYSILICON FILM ACTUATION

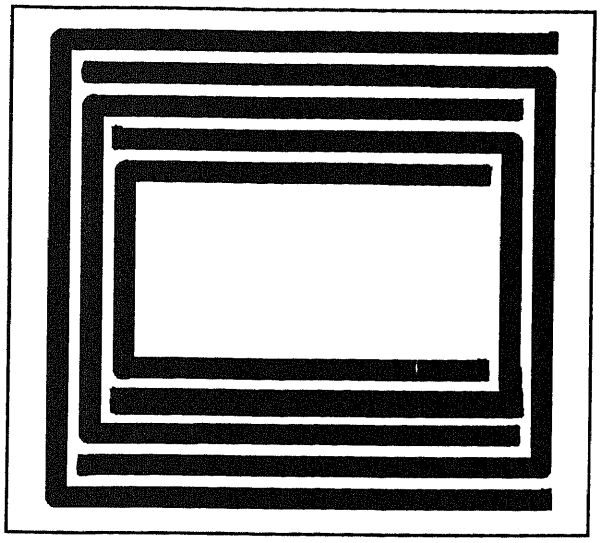
In the following pages, we present several different design to get better effect. These designs will reduce the driven voltages.



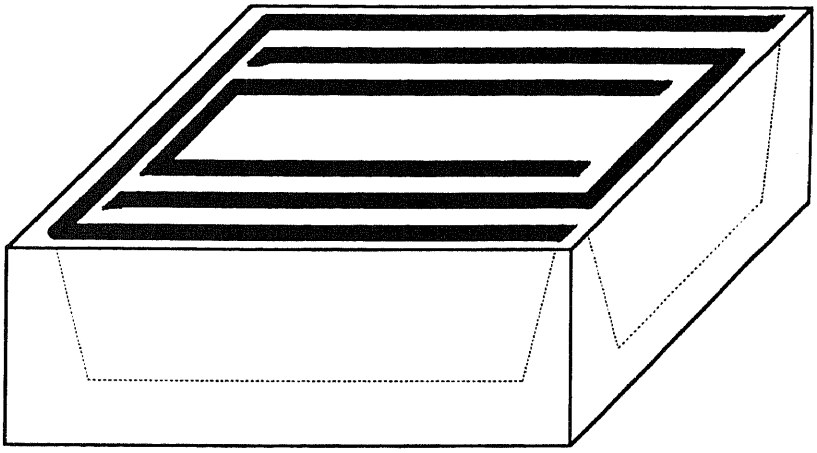
TOP VIEW



SIDE VIEW



TOP VIEW



SIDE VIEW

REFERENCES

[1] K.E. Petersen, "Silicon torsional scanning mirror", IBM J. Res. Development, vol 24, pp 631-637,1980.

[2] D.R. Collins, J.B. Sampsell, L.J. Hornbeck, J.M. Florence, P.A. Penz and M.T. Gately, "Deformable mirror device spatial light modulators and their applicability to optical neural networks", Appl. Opt., vol. 22, pp 4900-4907, Nov 1989.

[3] J.H. Jerman and S.R. Mallinson, "A miniature Fabry-Perot interferometer using silicon micromachining techniques", Proc. Solid state sensors and actuators, Hilton Head, pp 16-18, 1988.

[4] K. Gabriel, J. Javis, and W. Trimmer, *Small Machines, Large Opportunities: A Report on the Emerging Field of Microdynamics*, 1987.

[5] Richard S. Muller, "From ICs to microstructures: material and technologies", Technical Digest, IEEE International Electron Device Meeting,1987

[6] Kurt Pertsen, "The silicon micromechanics foundry", Technical Digest, IEEE International Electron Device Meeting,1987.

[7] Kurt Pertsen, "Silicon as a mechanical material", Proc. of IEEE, Vol. 70, No. 5, pp 420-457 1982.

[8] K. D. Wise, *Silicon micromaching and its application to high-performance integrated sensors*, Micromachining and Micropackaging of Transducers, Edited by C.D. Fung, P.W. Cheng, W. H. Ko, and D. G. Fleming, Elsevier Science Publishers, Amsterdam, 1985, pp 3-18.

[9] W.H. Ko, J.T. Suminto and G.T. Yeh, *Bonding Techniques for Microsensors*, Micromachining and Micropackging of Transducers, Edited by C.D. Fung, P.W. Cheng, W. H. Ko, and D. G. Fleming, Elsevier Science Publishers, Amsterdam, 1985, pp 41-61.

[10] Ernest Bassous, "Fabrication of Novel Three-Dimensional Microstructures by the Anisotropic Etching of [100] and [110] Silicon", IEEE Trans. of Electron Device, Vol. ED-25, No. 10, Oct. 1978, pp 1178-1193.

[11] H. Seidel, " The Mechanism of Anisotropic Silicon Etching and its Relevance on Solid-state Sensors and Actuators, Tokyo, Japan, June 2-5, 1987, pp 120-125

[13] L.Y. Chen, and et al, "Selective Chemical Vapor Deposition of Tungsten for Microdynamic Structures", Technical Digest, 2nd IEEE Workshop on Micro Electromechanical Systems, Salt Lake City, Utah, Feb, 20-22, pp 82-87,1989.

[14] O.N. Tufte, P.W. Chapman, and D. Long, "Silicon Diffused-Element Piezoresistive Diaphragms", J. Appl. Physics, 33, pp 3322-3329 1962

[15] S.C. Terry, J.H. Jerman and J.B. Angell, "A Gas choromatograph air analyzer fabricated on a silicon wafer", IEEE Trans. Electron Devices, vol. ED-26, pp 1880, 1979.

[16] K.E. Bean and W.R. Runyan, "Dielectric Isolation: Compressive, Current and Future", J. Electrochem. Soc., 124, pp 56,1977.

[17] D.B. Lee, "Anisotropic Etching of Silicon", J. Appl. Physics, 40, 1969, pp. 4569.

[18] M.J. Declercq, L. Gerzberg, and J.D. Meindl, "Optimization of the Hydrazine-Water Solution for Anisotropic Etching of Silicon in Integrated Technology", J. Electrochem. Soc., 122, pp 545,1975.

[19] R.M. Finne and D.L. Klein, " A Water-Amine-Complexing Agent System for Etching Silicon", J. Electrochem. Soc., 114, pp 965-970, 1967.

[20] A. Reisman, M. Berkenblit, S. A. Chan, F. B. Kaufman, and D.C. Green, "The Controlled Etching of Silicon in Catalyzed Ethylene diamine-Pyrocatechol-Water Solutions", J. Electrochem. Soc. 126, August, pp 1406-1414, 1979.

[21] A. Bohg, "Ethylene diamine-Pyrocatechol-Water Mixture shows Etching Anomaly in Boron-Doped Silicon", J. Electrochem. Soc. 118, Feb., pp 401-402, 1971.

[22] W.H. Ko, J. Hynecek, S. F. Boettcher, "Development of a miniature pressure transducer for biomedical applications", IEEE Trans. Electron Devices, vol. ED 26, No. 12, pp. 1896-1905, 1979.

[23] W.H. Ko, M. H. Bao, Y.D. Hong, "A High Sensitivity Integrated Circuit Capacitive Pressure Transducer", IEEE Trans. Electron Devices, vol. ED 29, pp. 48-56,1982.

[24] A.D. Brooks, and R.P. Donovan, "Low Temperature Electrostatic Si-to-Si Seals Using Sputtered Borosilicon Glass", J. electrochem. Soc. 1119, pp 545-546, 1972.

[25] E. Bassous, "Fabrication of Novel Three Dimensional Microstructure by Anisotropic Etching of [100] and [110] Silicon", IEEE Trans. Electron Devices, vol. ED 25, pp 1178-1185, 1978.

[26] T.L. Poteat, "Submicron Accuracies in Anisotropic Etched Silicon Piece Parts - A CASe Study", Micromachining and Micropackaging of Transducers, Edited by C.D. Fung, P.W. Cheung, W. H. Ko, and D.G. Fleming, Elsevier Science Publishers, Amsterdam, pp151-158, 1985.

[27] Kenneth E. Bean, "Anisotropic Etching of Silicon", IEEE Trans. Electron Devices, vol. ED 25, No. 10, pp 1193,1978.

[28] R.T. Howe, "Polycrystalline Silicon Microstructure", Micromaching and Micropackaging of Transducers, Edited by C.D. Fung, P.W. Cheung, W. H. Ko, and D.G. Fleming, Elsevier Science Publishers, Amsterdam, pp169-187, 1985.

[29] Long-Sheng Fan, Yu-Chong Tai, and Richard S. Muller, "Integrated Movable Micromechanical Structures for Sensors and Actuators", IEEE Trans. Electron Devices, vol. ED 35, No. 6, pp 724-730, 1988.

[30] Mehran Mehregany, Kaigham J. Gabriel, and William S.N. Trimmer, "Integrated Fabrication of P{olysilicon Mechanism", IEEE Trans. Electron Devices, vol. ED 35, No. 6, pp 719-723, 1988.

[31] Long-Sheng Fan, Yu-Chong Tai, and Richard S. Muller, "IC Processed Micromotors: Design, Technology, and Testing", Technical Digest, 2nd IEEE Workshop on Micro Electromechanical Systems, Salt Lake City, Utah, Feb. 20-22, pp 1-4,1989.

[32] Long-Sheng Fan, Yu-Chong Tai, and Richard S. Muller, "IC Processed Electrostatic Micromotors", Technical Digest, IEEE International Electron Devices Meeting, San Francisco, CA, Dec. 11-14, pp 666-669,1988.

[33] Richard S. Muller, "Strategies for Sensor Research", Technical Digest, International Conference on Sensors and Actuators, Tokyo, Japan, pp 853-856,1987.

[34] Wen H. Ko, "Frontiers in Solid State Biomedical Transducers", Technical Digest, IEEE International Electron Devices Meeting, pp 112-114, 1985.

[35] S. Middelhoek and A.C. Hoogerwerf, "Smart Sensors, When and Where?", Sensors and Actuators, 8, pp 39-48, 1985.

[36] P.L. Chen, R.S. Muller, and et al, "Integrated Silicon Microbeam PI-FET Accelerometer", IEEE Trans. on Electron Devices, ED 29, pp 27-33, 1982.

[37] K.E. Petersen, A. Shartel, and N. F. Raley, "Micromechanical Accelerometer Integrated with MOS Detection Circuitry", IEEE Trans. on Electron Devices, ED 29, pp 23-27,1982.

[38] S.C. Chang, M.W. Putty, D.B. Hicks and C.H. Li, and R. Howe, "Resonant-bridge Two-axis Microaccelerometer", Abstract, Transducers, The 5th International Conference on Solid-State Sensors and Actuators & Eurosensors III, Montreux, Switzerland, June 25-30, pp 142-143, 1989.

[39] T.S. J. Lammerink, W. Wlodarski, "Integrated Thermally Excited Resonant Diaphragm Pressure Sensor", Technical Digest, 3rd International Conference on Solid State Sersors and Actuators, Philadelphia, Pennsylvania, June 11-14, pp 97-100, 1985.

[40] M.W. Putty, S.C. Chang, R.T. Howe, A.L. Robinson, and K.D. Wise, "One port Active Polysilicon Resonant Microstructure", Technical Digest, IEEE Micro Electromechanical System Workshop, Salt Lake City, Utah, Feb. 20-22, pp 60-65,1989.

[41] L.M. Roylance and J.B. Roylance and J.B. Angell, "A batch fabricated silicon accelerometer", IEEE Trans. Electron Devices, vol. ED 26, pp 1911,1979.

[42] Kurt Petersen, "Micromechanical light modulator array fabricated on Silicon", Appl. Phys. Lett., vol. 31, pp 521, 1977.

[43] Amnon Yariv, "Optical Electronics" Fourth Edition, Hotl, Rinehart and Winston, Inc., 1991.

[44] J.M. Vaughan M.A., DPhil, "The Fabry-Perot Interferometer - history, theory, practice and applications", Adam Hilger imprint by IOP publishing Ltd., 1989.

[45] S.R. Mallinson and J.H. Jerman. "Miniature micromachined Fabry-Perot interferometers in silicon", Electron. Lett. 23, pp 1041-1043. 1987.

[46] S.R. Mallinson and J.H. Jerman. "A miniature Fabry-Perot interferometer fabricated using silicon micromachining techniques", Tech. Digest. Hilton Head Workshop, Hilton Head Island, SC, U.S.A., pp 16,1988.

[47] J.H. Jerman, D.J. Clift and S.R. Mallinson, "A miniature Fabry-Perot interferometer with a corrugated silicon diaphragm support", Sensors and Actuators A, 29 pp 151-158,1991.

[48] M. Shimazoe, Y. Matsuoka, T. Oyama, Y. Yamamoto and A. Yusakawa, "A silicon diaphragm pressure sensor for very low pressure", Proc. 3rd Sensor Symp., Japan, p309, 1983.

[49] J. T. Suminto, Gong-Jong Yeh, T. M. Spear and Wen Ko," Silicon diaphragm capacitive sensor for pressure, flow, acceleration and attitude measurements", Proc.

4th Int. Conf. Solid-State Sensors and Actuators (Transducers '87), Japan, Tokyo, pp 336,1987.

[50] J.H. Jerman and S.R. Mallinson, " A miniature Fabry-Perot interferometer fabricated using silicon micromachining techniques", Proc. IEEE Solid-State Sensors and Actuators Workshop, Hilton Head Island, SC, U.S.A., June 6-9, pp16, 1988.

[51] W. A. Wildhack and V. H. Goerke, "Corrugated metal diaphragms for aircraft pressure-measuring instruments", National Advisory Committee for Aeronautics, Tech. Note 738,1939.

[52] J. R. Mallon and A. D. Kurtz, " Transducer apparatus employing convoluted semiconductor diaphragms", U. S. Patent 4 467 656 (1984).

[53] J. A. Haringx, "Design of corrugated diaphragms", ASME Trans., 79 ,1957.

[54] S. M. Sze, *VLSI Technology*, second edition, 1988.

[55] Stanley Wolf, *Silicon Processing for the VLSI Era volume 1: Process Technology*, Lattice Press,1986.

[56] J.H. Jerman, "The Fabrication and use of Micromachined Corrugated Silicon Diaphragms",Sensors and Actuactors, A21-A23, pp 988-992, 1990.

[57] Massood Tabib-Azar and Jeffrey S. Leane, "Direct Optical Control for a Silicon Microactuator", Sensors and Actuactors, A21-A23, pp 229-235, 1990.

[58] N.F. Raley, D.R. Ciarlo, J.C. Koo, B. Beiriger, J.Trujillo, C. Yu, G. loomis and R. Chow, "A Fabry-Perot Microinterferometer for Visible Wavelengths", IEEE 1992