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Radiation damage studies in gate oxides

Sandeep G. Bharathi
New Jersey Institute of Technology

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ABSTRACT

RADIATION DAMAGE STUDIES IN GATE OXIDES

Detailed investigation of the effects of Gamma-ray irradiation on the electrical properties such as current-voltage and capacitance-voltage characteristics in thermally grown SiO_2 films in the thickness range of 15 to 120 nm on silicon substrates is presented in this thesis. The structures used in this study are Al/Poly/SiO_2/Si/Al and Al/SiO_2/Si/Al MOS capacitors. Based on the electrical characterization studies, we observe that irradiation causes generation of positive charges in the oxide leading to a shift of the high frequency Capacitance-Voltage (C-V) curves. An increase in surface state density at the SiO_2-Si interface with increase in radiation dose is also observed. Static current-voltage (I-V) characteristics lead to a further insight in the formation of radiation induced oxide traps. Fowler-Nordheim tunneling in irradiated MOS structures is investigated.

RADIATION DAMAGE STUDIES IN GATE OXIDES

by
Sandeep G. Bharathi

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APPROVAL PAGE

RADIATION DAMAGE STUDIES IN GATE OXIDES

Sandeep G. Bharathi

Dr. N. M. Ravindra, Thesis Advisor — Date
Associate Professor of Physics,
New Jersey Institute of Technology

Dr. Walter F. Kosonocky, Committee Member — Date
Distinguished Professor
Foundation Chair of Optoelectronics and Solid State Circuits
New Jersey Institute of Technology

Dr. Marek Sosnowski, Committee Member — Date
Associate Professor of Electrical Engineering,
New Jersey Institute of Technology

BIOGRAPHICAL SKETCH

Author: Sandeep G. Bharathi

Degree: Master of Science in Electrical Engineering

Date: May 1995

Undergraduate and Graduate Education

- Master of Science in Electrical Engineering,
  New Jersey Institute of Technology
  Newark, New Jersey, 1995

- Bachelor of Science in Electronics Engineering,
  Bangalore University
  Bangalore, India, 1992

Major: Electrical Engineering

This thesis is dedicated to
my Parents

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CHAPTER 1

INTRODUCTION

1.1 Background

Scientific research on radiation effects in semiconductors has been conducted for a number of years. The term radiation here is not restricted to photons, but is quite general and includes incident electrons, protons, neutrons and almost any particle that may interact with the material of interest. Our interest is not so much in radiation detection, but changes in material properties due to radiation. In the case of strong radiation, these changes are sometimes deleterious, significantly affecting the electrical conductivity and other electrical characteristics.

The main interest in radiation effects in semiconductors stems from the use of semiconductor devices in industrial, space and military applications in a radiation environment. The effects of radiation are also of considerable importance in device fabrication processes such as electron beam deposition, sputtering, ion etching and ion implantation that expose the device to radiation.

The principle cause of radiation damage varies with the utilization of the device in a particular environment. In general, the irradiating particles involved are classified into three main categories: photons (X-rays and γ-rays), neutrons and charged particles (electrons, protons, α-particles, heavy ions..). In our study, we confine ourselves to the effect of γ-rays on Al/SiO_2/p-Si/Al and Al/Poly/SiO_2/p-Si/Al structures for oxide thicknesses in the range of 125Å - 4500Å..

We shall briefly digress into the history of research performed on radiation induced damage in semiconductor devices and we will present our work in the rest of this thesis. The radiation damage in bulk silicon [1] and in SiO_2 [2] has been studied in order to improve the radiation hardness of microelectronic components. The effects of radiation

include electrical parameter drift such as threshold voltage shift, mobility degradation, increased leakage current and latch up. In both bipolar and MOS transistors, radiation damage in either silicon or the SiO_2 will affect the device characteristics. Szedon and Sandor [3] were among the first to recognize that the change in MOSFET characteristics was caused by the formation of positive charge in the oxide. This led to an intensive study of radiation effects in SiO_2. In most cases, radiation damage in SiO_2 was the most dominant effect. In this thesis, we confine our study to the radiation induced damage at the SiO_2-Si interfaces and the oxide in the Metal Oxide Semiconductor (MOS) system.

The MOS capacitor is widely used in the study of radiation effects in SiO_2. The MOS capacitor is most powerful for investigating the electrical properties of the MOS system. The superiority of MOS capacitor rests on its simple structure, simple fabrication and simplicity of analysis. The simplicity of analysis results because thermal equilibrium conditions are easy to obtain and a one dimensional treatment is accurate. Using the MOS capacitor, nearly all properties of interest in the SiO_2 at the SiO_2-Si interface and in Si can be measured. The effects of ionizing radiation on metal/oxide/Si structures have been intensively investigated [4-10] and it has been established that irradiation results in trapping of holes (generated by the radiation) in the SiO_2 and creation of interface states at the SiO_2-Si boundary.

Radiation induced effects have been reported on both p- and n- type substrates with varying oxide thicknesses, orientations, doping concentrations etc. It is difficult to generalize the results of various past experiments. Table 1.1 is an attempt to present a comprehensive summary of the research performed in the past three decades.

The frequency dependent Capacitance-Voltage (C-V) techniques are commonly used to characterize and study the irradiated and control samples. When ionizing radiation passes through a gate insulator, it creates free electrons and holes in the valence and conduction bands of the insulator. The highly mobile electrons are swept out of the

Table 1.1 Overview of some of the radiation damage studies performed in the past thirty years.

Device Structure	Method of Radiation	Technique	T_{ox} (thickness of the oxide)	Radiation Damage Studied
Al/SiO_2/n-Si n - 50Ωcm n - 5 Ωcm	Electron Energies of 10 to 16 KeV. Total electronic charge received by samples was 2-5 x 10^{-6} coul/cm^2.	HF CV measurement. Comparison with theoretical curve.	50Ωcm wafers had 1500 Å.	Electron bombardment under study conditions introduced added +ve charge which were detected by CV measurements.[3]
MOS capacitor	10^4 - 10^9 rads with gate bias of +2 volts applied during irradiation.	HF CV measurement. Comparison with control sample.	2000 Å	Shift of CV characteristics along voltage axis for various dose rates. ΔV saturates above 10^8 rads.[11]
MOFSET	Co-60 γ ray doses. (0-4) x 10^6 rads for +ve gate bias (0-0.6) x 10^6 rads for -ve gate bias.	HF CV measurement. Comparison with control sample.	1600 Å	Shift of CV characteristics corroborates with [11] for positive gate bias and ΔV saturates for high doses. The same characteristic is exhibited for -ve gate bias too. Saturation voltage shift due to +ve oxide charge build up is much greater for positive bias than for negative gate bias applied during radiation. [12]
MOS capacitor p-type	6 x 10^4 rads 2 x 10^6 rads with +2.5 volts on gate.	HF CV measurement.		Shift of CV characteristics along the voltage axis in MOS capacitor as a result of irradiation at two different dose levels under the same positive gate bias.[13]
MOS capacitor p-type	Radiation with photon energies from well below to well above the bandgap energy. +ve gate bias of 20 volts applied			

Table 1.1 (Continued)

Device Structure	Method of Radiation	Technique	T_{ox} (thickness of the oxide)	Radiation Damage Studied
	during radiation at 6.7×10^{14} photons/cm^2 i.e. 2.4×10^8 rads at 10.2 eV.	HF CV and LF CV.		CV(curves) HF are shifted to more negative bias corresponding to creation of positive oxide charge. The effect of positive oxide charging in SiO_2 was investigated for high and low photon energies for positive and negative gate bias during irradiation. [14]
p-type MOS $N_a = 1 \times 10^{14}$, 9×10^{14} and 5×10^{15} / cm^3 n-type MOS $N_d = 4 \times 10^{14}$, 3×10^{15} /cm^3 <100> orientation.	25 KeV electron beam. Irradiation dose was 1×10^{-5}, $1.6 \times ^{-5}$ and 6.6×10^{-5} C/sq. cm.	HF CV and quasi-static CV.	500 Å	Interface state generation in MOS capacitors for both p-type, n- type silicon substrates having different doping concentrations were studied. [15]
MOS capacitors.	5 KeV electron beam with +4V gate bias.	HF CV and LF CV both at low temperature and room temperature.	2000 Å About 100 variations in fabrication parameters were made.	Interface state generation and oxide charges generation by ionizing radiation were investigated. An attempt to construct atomic models of oxide charges and interface states was made. Randomly located trivalent silicon atoms are shown to account for thermally generated interface states at SiO_2-Si interface. [16]
MOS capacitors, n-channel and p-channel MOSFETs.	Co-60 gamma ray irradiation of 1×10^6 rads. +ve bias was applied for MOSFETs during irradiation.	Temperature bias stress CV curves. HF CV and IV analysis.	900 Å, 5600 Å and a number of process variables.	Reported radiation induced increase of mobile Na^+ ions in MOS capacitors and a bias temperature stress induced relaxation or "annealing" of radiation displaced ion current peak accompanied by small increase in mobile Na in MOS capacitors.[17]

Table 1.1 (Continued)

Device structure	Method of Radiation	Technique	T_{ox} (thickness of the oxide)	Radiation Damage Studied
W - SiO_2 - p-Si W - SiO_2 - n-Si	1MeV electron beam of dose rate 140 rad/sec with +10V bias.	HF CV plots	500 Å, 670 Å.	Feasibility of using new materials like tungsten instead of poly as gate bias and interconnection material for VLSI radiation hardened applications were studied. [18]
MOS capacitors <100> orientation n-type Si, SOS n-channel phosphorous doped poly gate transistors.	Co-60 source. 1 x 10^6 rads with +10 volts bias.	HF CV plots quasi-static CV.	500 Å 650 Å Dry high press-ure oxides.	Examination of radiation behavior of high pressure oxides was found to be similar to that of dry and wet atmospheric pressure oxides. Calculation of interface state densities for various samples were done. [19]
MOS capacitor, <111> orientation n-type Si.	γ rays 10M rads.	ESR	1400 Å	Effects of bias on radiation induced paramagnetic defects at Si/SiO_2 interface were studied with ESR measurements. A large change in density of radiation induced Pb centers with bias was observed. Pb defects were found to account for a large portion of radiation induced defects at the interface.[20]
MOS capacitor n type 100 wafers.	0 - 20 eV electron irradiation.	XPS	850 Å	Holes and electrons were found to induce formation of trivalent Si centers. Description of bond strain gradient [BSG] model to explain interface state build up. [21]

Table 1.1 (Continued)

Device Structure	Method of Radiation	Technique	T_{ox} (thickness of the oxide)	Radiation Damage Studied
MOS capacitor. <111> orientation n-type 2×10^{16} /cm^3 donor concentration.	X-ray 1.1×10^4 rads - 10^6 rads.	HF CV and GV characteristics.	5000 Å	Investigation of flat band voltage shift and generation of surface states for X-ray irradiated samples were done. [22].
MOS capacitor.	Soft X-rays with 1 MV/cm, +ve gate bias, total dose 10K rad at low temperature.	Low temperature HF CV curves.		A general relationship between location of trapped holes and subsequent generation of interface states were reported. [23]
MOS capacitors.	X-rays.	TSC and CV technique.	3500 Å	Trapped hole annealing was quantitatively estimated by TSC and CV techniques. Models of oxide trap charge buildup and annealing are discussed. [24]
n-type Si <100> orientation MOS capacitor.	γ rays , X-rays 10^3 to 10^6 rads.	HF and quasi-static CV.	1000 Å - 2000 Å thick.	Change in density of surface states as a result of annealing, irradiation and annealing as a function of temperatures between 300 and 900 K has been studied. [25].

oxide by even a small field. However, the holes are trapped usually near the most negative electrode and form a semi-permanent positive space charge. When subjected to ionizing radiation, the accumulation of trapped positive charge is noted as a shift in flat band voltage to more negative values. The amount of this shift will depend on the gate bias during irradiation. For positive gate bias, the holes are trapped closer to silicon resulting in a large flatband shift. For negative bias, they are trapped closer to the metal where they cause a lesser flat band shift.

Figure 1.1 shows the shift along the voltage axis in MOS capacitor C-V characteristics as a result of irradiation at two different dose levels under the same positive gate bias. In p-type silicon used for n-channel transistors, inversion occurs when the Fermi level is close to the conduction band so that the interface states are charged neutral or negative at threshold conditions. With the same argument, n-type silicon used for p-channel transistors have interface states which are charged neutral or positive. In most cases, the positive charge build up dominates at low radiation levels [26]. Figure 1.2 shows shift of the C-V characteristics of an MOS capacitor along the voltage axis and the corresponding oxide trap charge (Q_{ot}) as a function of dose with dose rate as parameter. We observe that ΔV saturates above a dose of 10^8 rads. Surface state formation is sensitive to radiation doses [26]. Many n-channel devices show a negative shift in threshold voltage for doses less than 10^5 rads and then begin to shift to more positive values for increased dose levels [22]. But p-channel devices usually show a continuous shift to more negative values with increasing radiation dose. Figure 1.3 shows shifts of C-V curves measured between the gate and the substrate of a MOSFET along the voltage axis for positive and negative aging gate bias.

The other notable contributions to this study is Repace's [17] report on mobile Na ions in irradiated MOS capacitors and effect of bias on radiation induced paramagnetic defects at the Si/SiO_2 interface [20]. Models where trapped holes are converted directly to interface traps have been proposed by many authors [21,23,27]. Co-60 irradiation studies

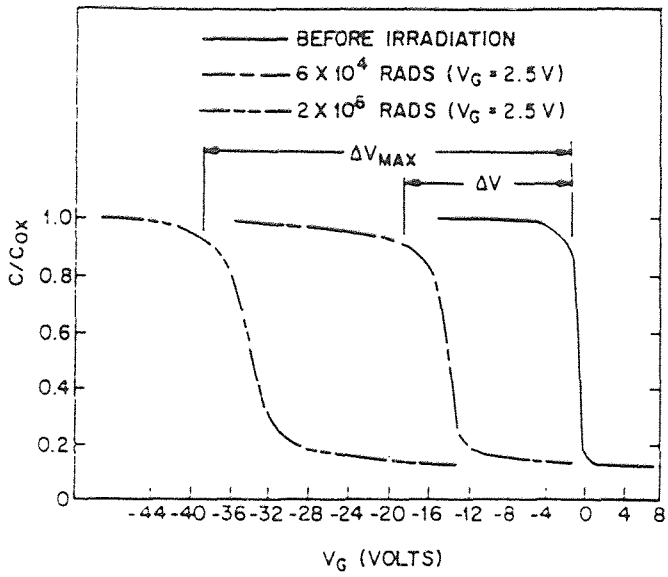


Figure 1.1 Shift of MOS capacitor C-V curves for two different doses of radiation under the same positive gate bias.[13]

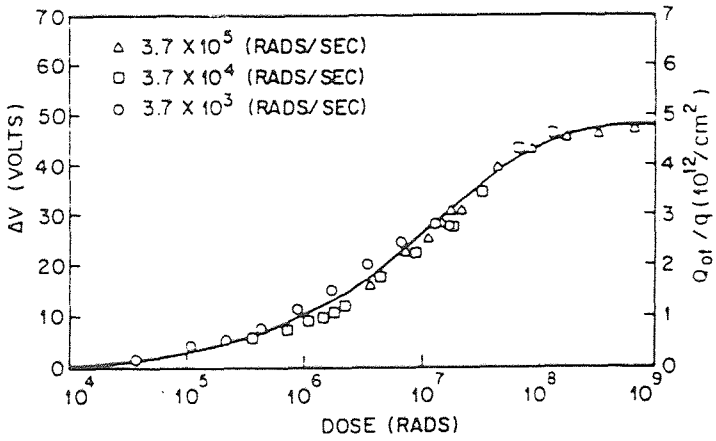


Figure 1.2 Shift of C-V characteristics of a MOS capacitor and the corresponding oxide trapped charge for different doses of radiation.[11]

on Aluminum/Tantalum oxide/silicon oxide/silicon capacitors have also been studied [28]. The effect of heat treatment on interface parameters in SiO_2-Si structures after irradiation opens a whole new field for investigation. With this as the background, we shall discuss at length the findings of our research.

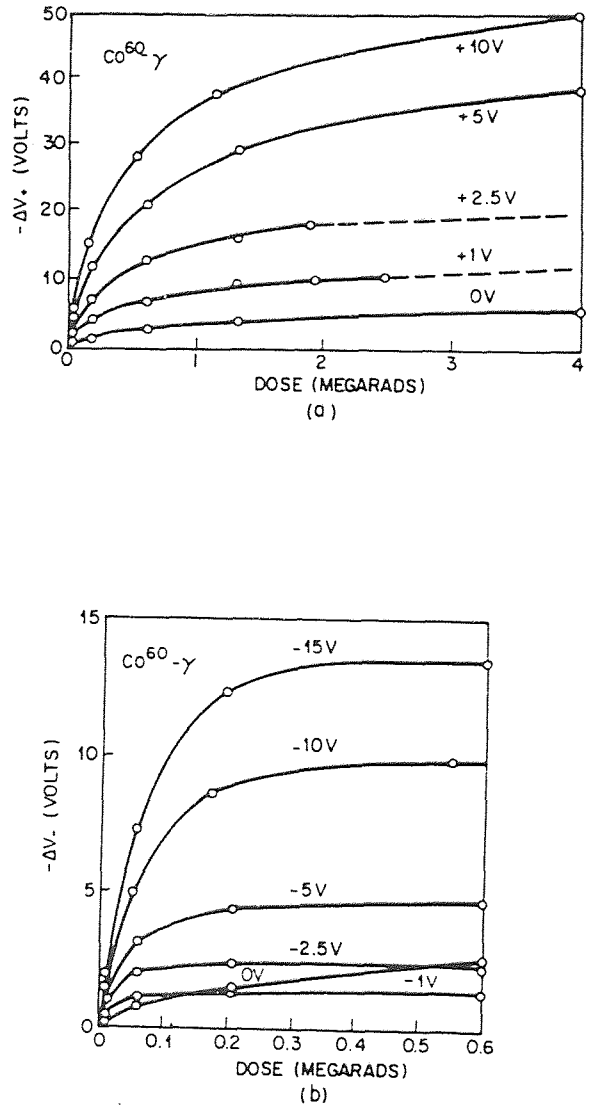


Figure 1.3 Shift of C-V curves for a MOSFET along the voltage axis as a function of gamma-ray dose (Co-60) (a) positive aging gate bias; (b) negative aging gate bias.[12]

1.2 Outline of Remaining Chapters

Chapter Two covers oxidation kinetics and various aspects of oxide growth. Chapter Three deals with the ideal MOS capacitor in terms of its energy band diagrams and also describes the MOS capacitor model under non-ideal conditions. Chapter Four discusses in depth the electrical characterization techniques. Chapter Five describes the experimental procedures used in the fabrication of MOS capacitors and the characterization set up is also outlined. Chapter Six is devoted to the results of the various experiments performed on irradiated MOS capacitors and the effects of radiation on these structures are discussed in detail. Chapter Seven concludes our study of the radiation damage in MOS structures.

CHAPTER 2

OXIDATION KINETICS

2.1 Introduction

Oxidation of Silicon is a very important step during the process of fabricating VLSI circuits. A high quality oxide is an absolute necessity in order to ensure the reliability of the devices. Silicon dioxide has several uses: to serve as a mask against implant or diffusion of dopant into silicon, to provide surface passivation, to provide electrical isolation of multi-level metallization schemes, for device isolation and to serve as a dielectric insulator in MOS structures. Several methods of oxidation are currently in use such as vapor phase reaction, plasma anodization, wet anodization and thermal oxidation in both dry and wet environments. In this chapter, we shall discuss the classical theory of oxidation proposed by Deal and Grove [29] and its limitations, the role of non-bridging oxygen at SiO_2-Si interface and the effects of orientation, temperature and other factors on oxide growth. We will consider the relative differences of dry and wet oxides , thin and thick oxides.

2.2 Classical Theory of Oxidation of Silicon

The macroscopic oxidation of single crystal was first suggested by Deal and Grove. The model is schematically illustrated in Figure 2.1. They proposed that oxidation proceeds by the diffusion of an oxidant (molecular H_2O or O_2) through the existing oxide to the SiO_2/Si interface. The reactions describing the thermal oxidation of Silicon are given as:

Si (solid) + O_2 (vapor) ====> SiO_2 (solid)

Si (solid) + $2H_2O$ (vapor) ====> SiO_2 (solid) + $2H_2$

This model proposed by Deal and Grove is valid for oxide thicknesses above 200 Å, oxidation in dry oxygen, oxidant partial pressure of 1 atm or less and temperatures

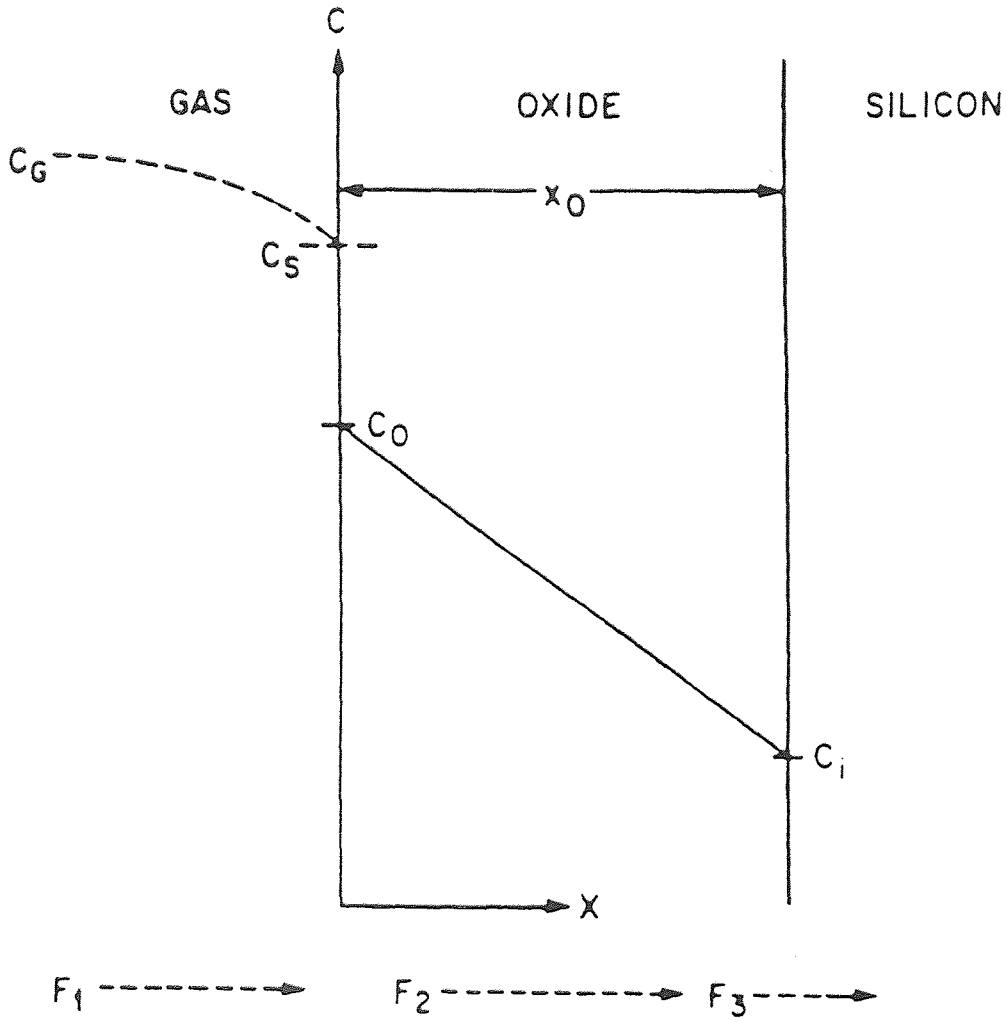


Figure 2.1 Cross section of silicon with a growing SiO_2 layer illustrating the model for thermal oxidation of silicon. The three fluxes, F_1 into the silica, F_2 through the silica, and F_3 at the SiO_2-Si interface, are shown. [29]

between 700 and 1300° C. The overall oxidation process based on Figure 2.1 depends on fluxes. After considering the initial oxide layer, various fluxes, gas laws [30] etc., the following relation has been shown to be applicable:

$$x^2 + Ax = B\,(t + \tau) \qquad (2.1)$$

where,

t is the time duration for which the oxidation has taken place,

τ is the time co-ordinate shift to account for the initial oxide layer,

x is the oxide thickness,

B is the parabolic rate constant and

B/A is the linear rate constant.

Experimentally measured results agree with the predictions of this model over a wide range of oxidation conditions. For wet oxidation, the initial oxide thickness is very small. However for dry oxidation, the extrapolated value of initial oxide thickness is about 200 Å. Therefore Deal and Grove found that there was an initial accelerated growth during oxidation in dry oxygen. A number of different forms and mechanisms have been suggested for the initial thin oxide growth kinetics. The proposals in the literature have included schemes based on enhanced oxidant diffusion, reduced oxidant diffusivity in the oxide, fixed charge effect on the interface reaction rate and micropore diffusion.

2.3 Chemical Structure of SiO_2

SiO_2 basically has two states: (a) amorphous state termed as glass of fused silica which is extensively used in furnace hardware and (b) crystalline state termed as quartz. The amorphous state of SiO_2 is thermodynamically unstable below 1710° C. Fused silica does not have a long range structure because of its amorphous state but a short range order does exist. The short range order is centered around the structural formula for the material which is SiO_4^{4-}. The structure can be described as follows:

The valency of Silicon is four and this Si atom is located at the center of a regular tetrahedron as shown in Figure 2.2a and the oxygen ions are at each of the corners of the tetrahedron. The tetrahedral distance between Si and oxygen ions is 1.60 Å, and the inter-ionic oxygen-oxygen distance is 2.27 Å.

The tetrahedral structures are then joined to each other by an oxygen ion called a bridging oxygen, which is shared between the two touching tetrahedra. This gives rise to a crystalline structure as shown in Figure 2.2b. But for the amorphous state of SiO_2 shown in Figure 2.2c, some of the vertices of the tetrahedra are not shared and this results in the structure having non bridging oxygen ions.

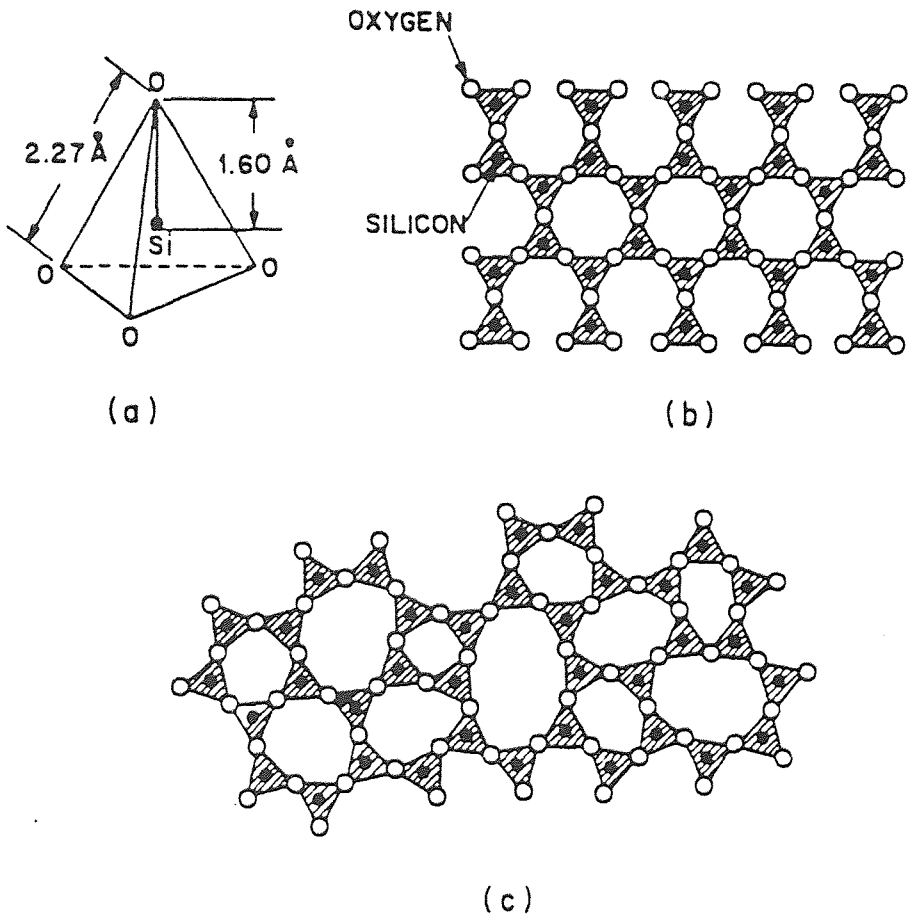


Figure 2.2 (a) Basic structural unit of SiO_2; (b) Two dimensional representation of a quartz crystal lattice; (c) Two dimensional representation of the amorphous structure of SiO_2.[31]

The cohesiveness of the glass depends on the ratio of bridging to non bridging oxygen ions. Greater the ratio, the better will be the cohesiveness of the glass. The atomic movement in silica is more likely to occur by the movement of oxygen atoms rather than the silicon atom. The reason for this is the bonding mechanism of the atoms, Si has four bonds to oxygen, as a result four bonds have to be ruptured for the silicon atom to be free whereas the rupture of only two Si-O bonds are required to free a bridging oxygen atom. If the rupture occurs, an oxygen ion vacancy is formed. This vacancy has a net positive charge in the network. Both bridging and non bridging oxygen vacancies may be formed, but the non bridging vacancy is more likely to occur based on binding energy considerations.

SiO_2 films grown by the oxidation of silicon, have an amorphous structure with a random network of polyhedra. The density of thermally grown fused silica (2.25 g/cc) is less than that of the crystalline quartz (2.65 g/cc). The lower density implies a more open structure. This open structure is conducive to the interstitial diffusion of impurities through the network. Impurities in silica alter its properties appreciably. There are two kinds of impurities, substitutional and interstitial. The substitutional impurities (e.g. B^{3+} & P^{5+}) replace Si in the structure and they are also known as network formers. The missing or extra electrons in the tetrahedra, when these materials are added, are accomodated by the elimination or formation of bridging oxygen ions respectively. The elimination of bridging oxygen tend to weaken the network.

Interstitial impurities like the oxides of Na, K, Pb and Ba enter the structure resulting in the metal ions giving up its oxygen to the network, thereby producing two non bridging oxygen ions, which replace the original binding oxygen. The additional non bridging oxygen also tends to weaken the structure facilitating the increased diffusion of other species within the glass. Impurity oxides of this type are termed network modifiers since they do not form glasses themselves.

Water vapor is an important impurity in fused silica, and can enter from the atmosphere or be grown-in during wet oxidation. The water vapor combines with a bridging oxygen to form a pair of stable non bridging hydroxyl groups (OH^-). This reaction can be represented by:

H_2O + Si--O--Si = Si--OH + OH-Si.

The increase in non bridging oxygen again tends to weaken the Si network, thereby increasing the diffusivities of many materials in the network. The presence of OH can be detected by IR spectroscopy, since the Si-OH stretching frequency is different than that of Si-O. Figure 2.3 shows the structure of fused silica glass.

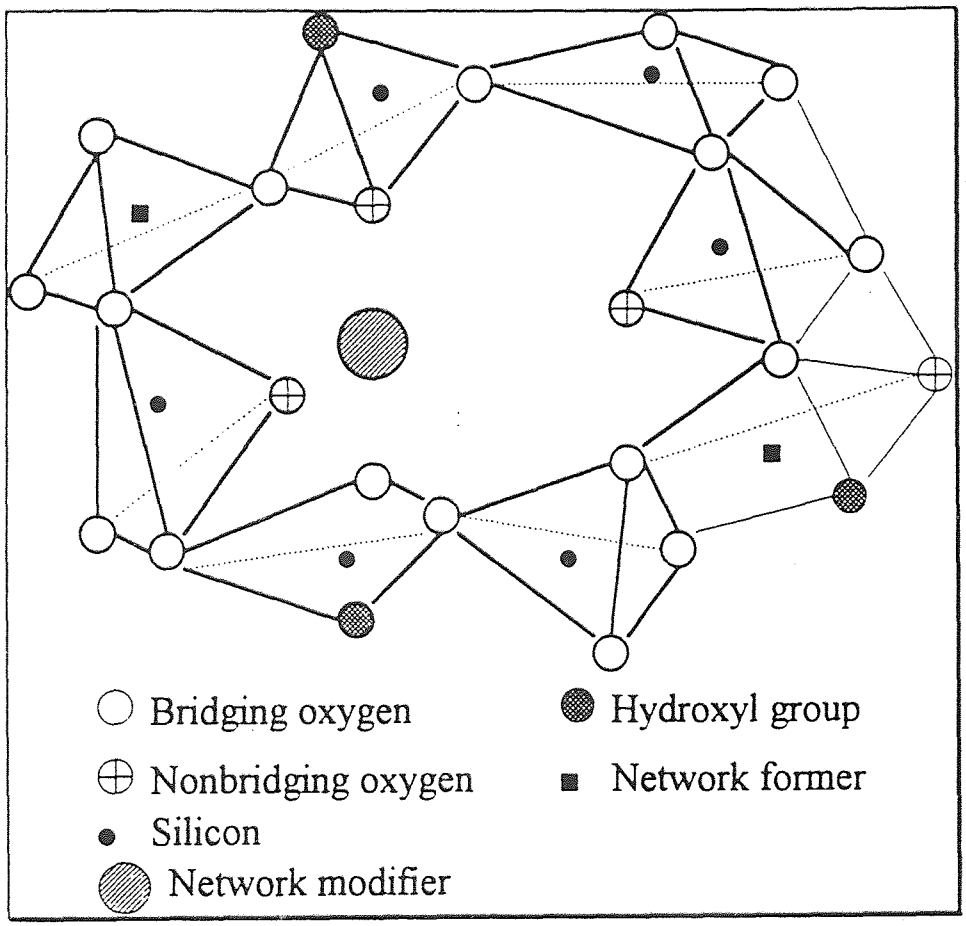


Figure 2.3 The structure of fused silica glass.

2.4 Other Aspects of Thermal Oxidation and CVD Deposition

Oxides grown in pure dry oxygen have the very best electrical properties, but considerably more time is required for growing the same thickness of the oxide at a given temperature in dry oxygen than in water vapor. For relatively thin oxides, such as the gate oxide in a MOSFET, typically lesser than 100 nm thick, dry O_2 oxidation is commonly used. Such a film can be grown very quickly. In many other applications, such as for bipolar transistors and for thick field or isolation oxide (greater than 500 nm) in MOS integrated circuits, oxidation in water vapor or steam is used and provides adequate passivation.

Thin oxides (2.5 nm - 10 nm) are very important in a class of memory devices that use potential wells at the interface between SiO_2 and another insulator to store charge. The potential wells at the insulator-insulator interface are filled and emptied with electrons by tunneling between the wells and the silicon through the thin SiO_2 layer. Another possible application of thin oxides is in semiconductor photovoltaic solar cells, where a thin oxide layer (in the order of 3 nm) between a metal electrode and the semiconductor has been found to increase the output voltage and efficiency of the cell.

The oxidation mechanism is found to depend on the crystallographic orientation of the silicon surface. In particular, the linear oxidation rate is observed to depend on the crystallographic orientation of the silicon surface. The parabolic rate constant (Equation 2.1) is independent of silicon surface orientation, as the parabolic oxidation rate is diffusion limited.

Oxides can also be formed not by oxidation of Si but by CVD deposition at different temperatures. The oxide properties change depending on the temperature at which they were grown. Intermediate temperature (500 - 800° C) oxides may be deposited using pyrolysis of tetraethylorthosilicate, $(C_2H_2O)_4Si$, in a hot wall tube furnace reactor [32,33]. Advantages of the intermediate temperature method are a short time cycle, and large numbers of silicon wafers can be handled on a furnace paddle or rack. Intermediate temperature CVD oxides have been used most often as a masking layer for the etching of

silicon nitride films and for diffusion masking of germanium substrates. High temperature deposition of SiO_2 is usually done at temperatures of 850-1100° C using silane diluted to 1% in nitrogen, CO_2, and hydrogen carrier gas. The high temperature deposition method is most useful for the top masking oxide for etching holes in silicon nitride films. There are a number of advantages to depositing SiO_2 by the pyrolysis of tetraethylorthosilicate at low pressures: less particulates that can deposit on the wafers are generated, up to 200 wafers can be processed at a time, better thickness uniformity across each wafer is obtained, a more specular surface results, less material is used, and this method is less hazardous and lower in cost.

There are still a number of factors that affect the oxidation like nature of the diffusing species, state of water in silica and influence of impurities on oxidation rates. All these factors are discussed by Sze [30] and Ghandhi [34].

CHAPTER 3

FUNDAMENTALS OF MOS STRUCTURE

3.1 Introduction

The MOS capacitor is the simplest, most reliable device structure for investigation of radiation damage in the oxide and its interface with the semiconductor. Hence it is mandatory to have a thorough knowledge of the physical characteristics of MOS structure under equilibrium and non-equilibrium conditions. In this chapter, we are concerned primarily with the MOS structure shown in Figure 3.1.

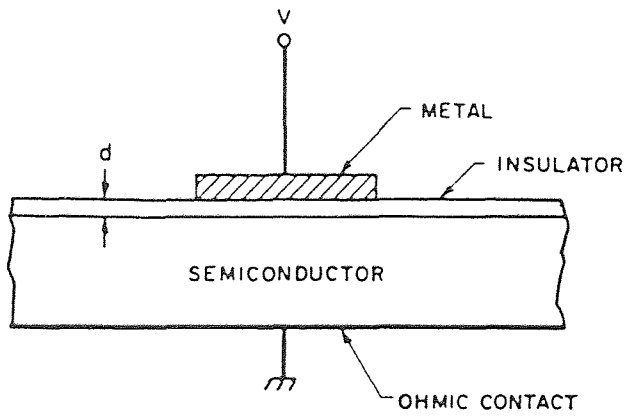


Figure 3.1 Metal-oxide-semiconductor (MOS) structure.[35]

We first consider the ideal characteristics of MOS structure and then extend our discussion to include the effects of metal semiconductor work function differences, interface traps, oxide charges etc.

3.2 Ideal MOS Structure

We will consider the energy band diagrams of ideal MOS capacitors for zero applied voltage. Figure 3.2 shows the band diagrams for both n-type and p-type semiconductors. Figure 3.3 shows the energy band diagram quantitatively representing the energy levels.

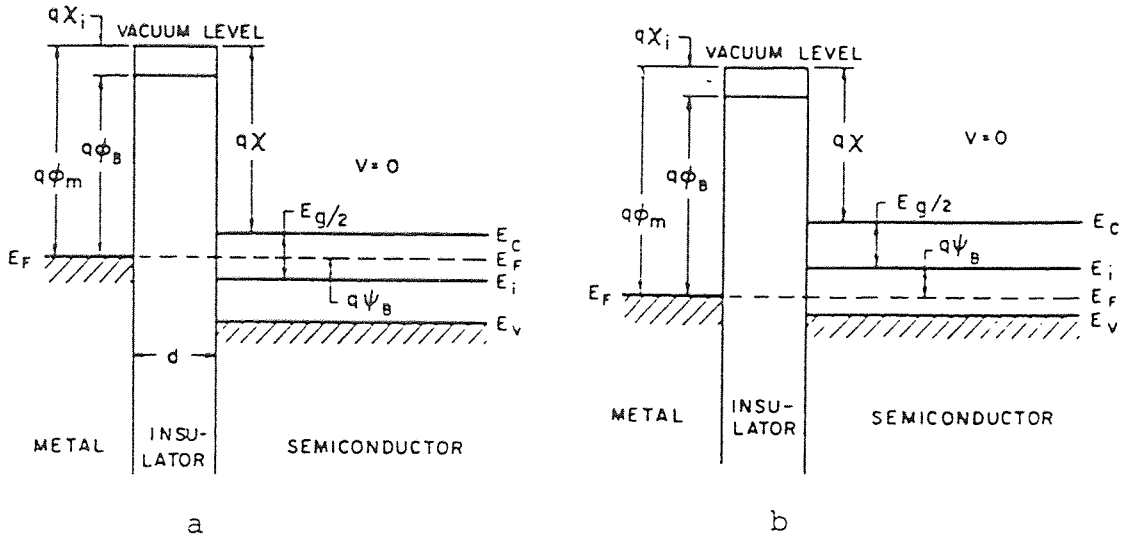


Figure 3.2 Energy-band diagrams of ideal MOS capacitors at V = 0. (a) n-type semiconductor. (b) p-type semiconductor.[35]

The position of the Fermi level in the gate and in the silicon gives us a very clear picture of the physical device aspect. The forbidden gap in SiO_2 is very large whereas that of silicon is much smaller. At zero applied bias, energy difference between the metal work function and the semiconductor work function is zero or the work function difference [35] ϕ_{ms} is zero. For completeness, we have:

for n-type

$$\phi ms = \phi m - \left(\chi + \frac{Eg}{2q} - \psi B \right) = 0 \qquad (3.1)$$

for p-type

$$\phi ms = \phi m - \left(\chi + \frac{Eg}{2q} + \psi B \right) = 0 \qquad (3.2)$$

where ϕ_m is the metal work function, χ is the semiconductor electron affinity, χ_i is the insulator electron affinity, E_g is the bandgap, ϕ_B is the potential barrier between the metal and the insulator and Ψ_B is the potential difference between Fermi level E_F and intrinsic Fermi level E_i. This condition where the energy band is flat when there is no applied voltage is termed as flat band condition (Figure 3.2). The only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those with equal but opposite sign on the metal surface adjacent to the insulator. There is no carrier transport through the insulator under dc biasing conditions or the carrier transport through the insulator is infinite.

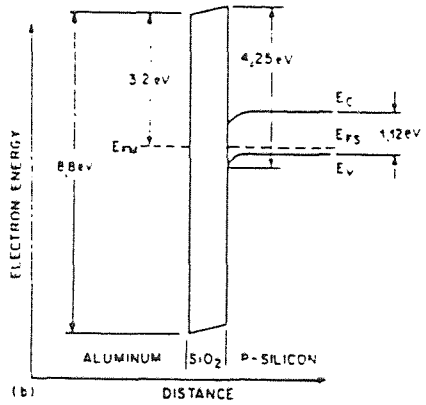


Figure 3.3 Energy-band diagram of the MOS capacitor showing the energy barrier between metal and SiO_2 and between silicon and SiO_2.[2]

When an ideal MOS capacitor is biased with positive or negative voltages, we may examine three cases at the semiconductor surface namely, accumulation, depletion and inversion. These cases are shown in Figure 3.4 for both p-type as well as n-type

substrates. The relevance of accumulation, depletion and inversion is also explained with respect to capacitance voltage curves (C-V) in the next chapter. If we apply a negative voltage between the metal and semiconductor, we are effectively depositing a negative charge on the metal. In response, an equal net positive charge accumulates at the surface of the semiconductor. In case of p-type substrate, this occurs by hole accumulation at semiconductor-oxide interface. A positive voltage from metal to semiconductor deposits positive charge on the metal and calls for a corresponding net negative charge at the surface of the semiconductor. Such a negative charge in p-type material arises from depletion of holes from the region near the surface, leaving behind uncompensated ionized acceptors.

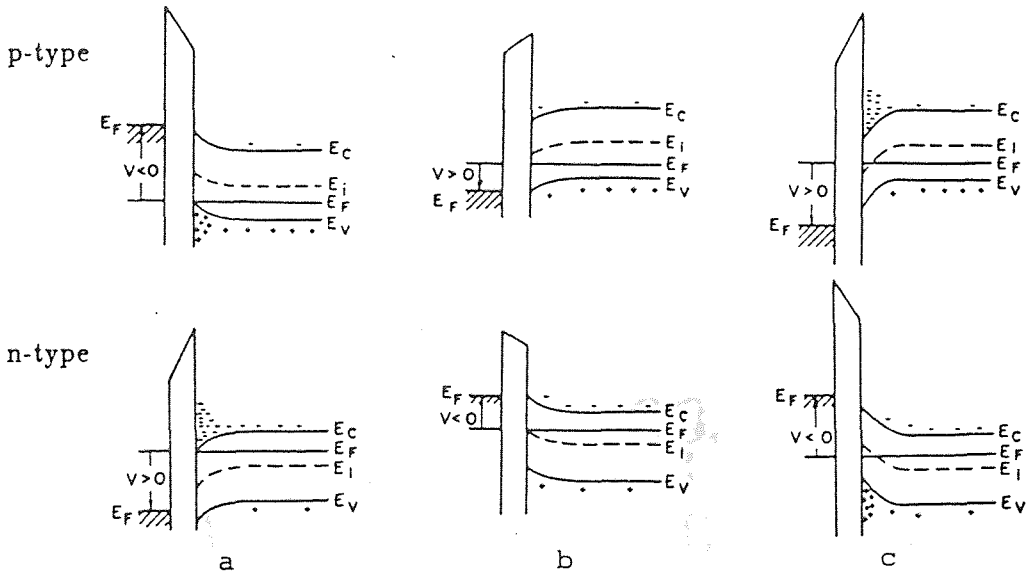


Figure 3.4 Energy-band diagrams for ideal MOS capacitor when $V \neq 0$, for the following cases: (a) accumulation; (b) depletion; (c) inversion [35]

If we continue to increase the positive voltage, the bands at the semiconductor surface bend down more strongly. Since E_i is below E_F and $E_F >> E_i$ implies a large concentration of electrons in the conduction band, this is the inversion phenomena. The

above discussion applies to n-type substrate devices simply by reversal of polarities of voltages.

3.3 Effects of Real Surfaces

The departure of the physical characteristics of MOS capacitor from the ideal model is due to work function differences and interface charges. As a result, the MOS capacitor happens to be the only semiconductor device that is in equilibrium (considering flat band conditions), when a voltage is applied to it.

The work function of a semiconductor, $q\phi_S$, varies with the doping concentration. Hence work function difference, $q\phi_{ms} = q\phi_m - q\phi_S$, also varies depending on the doping concentration. Generally, $q\phi_{ms}$ is not zero as opposed to the ideal case. Considering a p-type semiconductor MOS system, the bands bend down due to the work function difference as shown in Figure 3.5

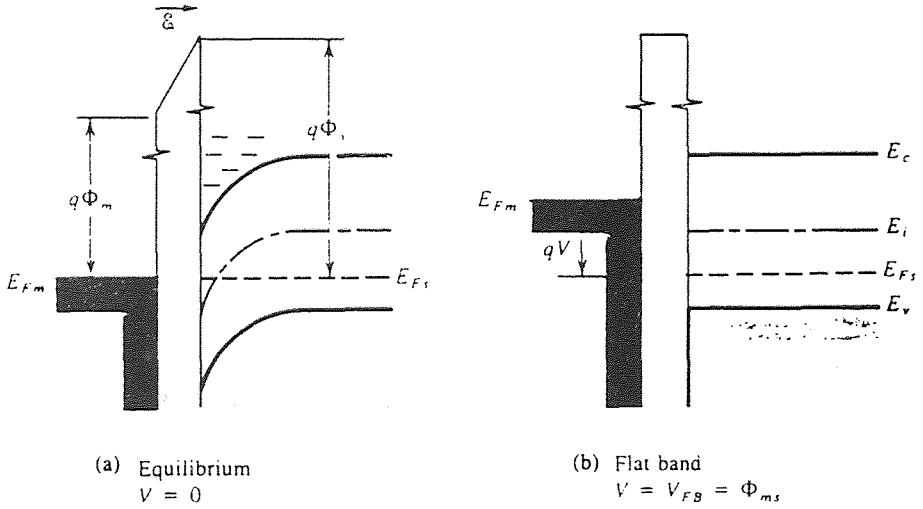


Figure 3.5 Energy-band diagrams for negative work function difference . (a) Band bending at equilibrium. (b) Flat band condition for negative applied voltage.[36]

Thus the metal is positively charged and the semiconductor surface is negatively charged at thermal equilibrium. To obtain the flat band condition pictured in Figure 3.5b,

we must apply a negative voltage to the metal $V_{FB} = \phi_{ms}$, which is called the flat band voltage. In addition to the work function difference, the equilibrium MOS capacitor is affected by charges in the oxide and at the SiO_2-Si interface [37]. Figure 3.6 shows charges and their locations for thermally oxidized silicon. There are four general types of charges associated with SiO_2-Si system. The charges are described as [37]:

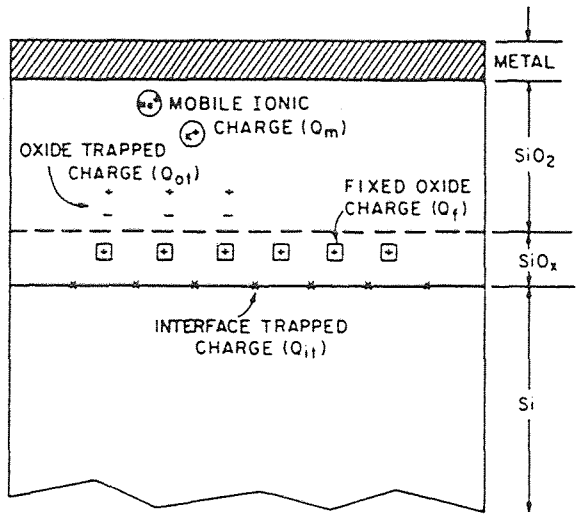


Figure 3.6 Charges and their locations for thermally oxidized silicon.[35]

(1) Fixed oxide charge (Q_f, N_f): These are located in the oxide layer less than 25 Å from the SiO_2-Si interface. The dependency on oxidation ambient temperature, silicon orientation and other related parameters has been clearly explained by Deal [37].

(2) Mobile oxide charge (Q_m, N_m): These are due to ionic impurities such as Na^+, Li^+, K^+ that are mobile within the oxide under bias temperature aging condition.

(3) Oxide trapped charge (Q_{ot}, N_{ot}): These may be positive or negative due to holes or electrons trapped in the bulk of the oxide. Trapping may result from any form of ionizing radiation or hot electron injection.

(4) Interface trapped charge (Q_{it}, N_{it}, D_{it}): These are charges located at the Si-SiO_2 interface with energy states in the silicon forbidden gap. They can possibly be

produced by structural defects, impurities or other defects caused by radiation. Unlike the other three, these can exchange charges with the underlying silicon. These are also referenced as surface states, fast states or interface states in the literature.

Any form of ionizing radiation will affect device structure and characteristics mainly in modifying the charge distributions. In chapter 4, we discuss several characterization techniques to account for radiation induced damage in semiconductor devices.

CHAPTER 4

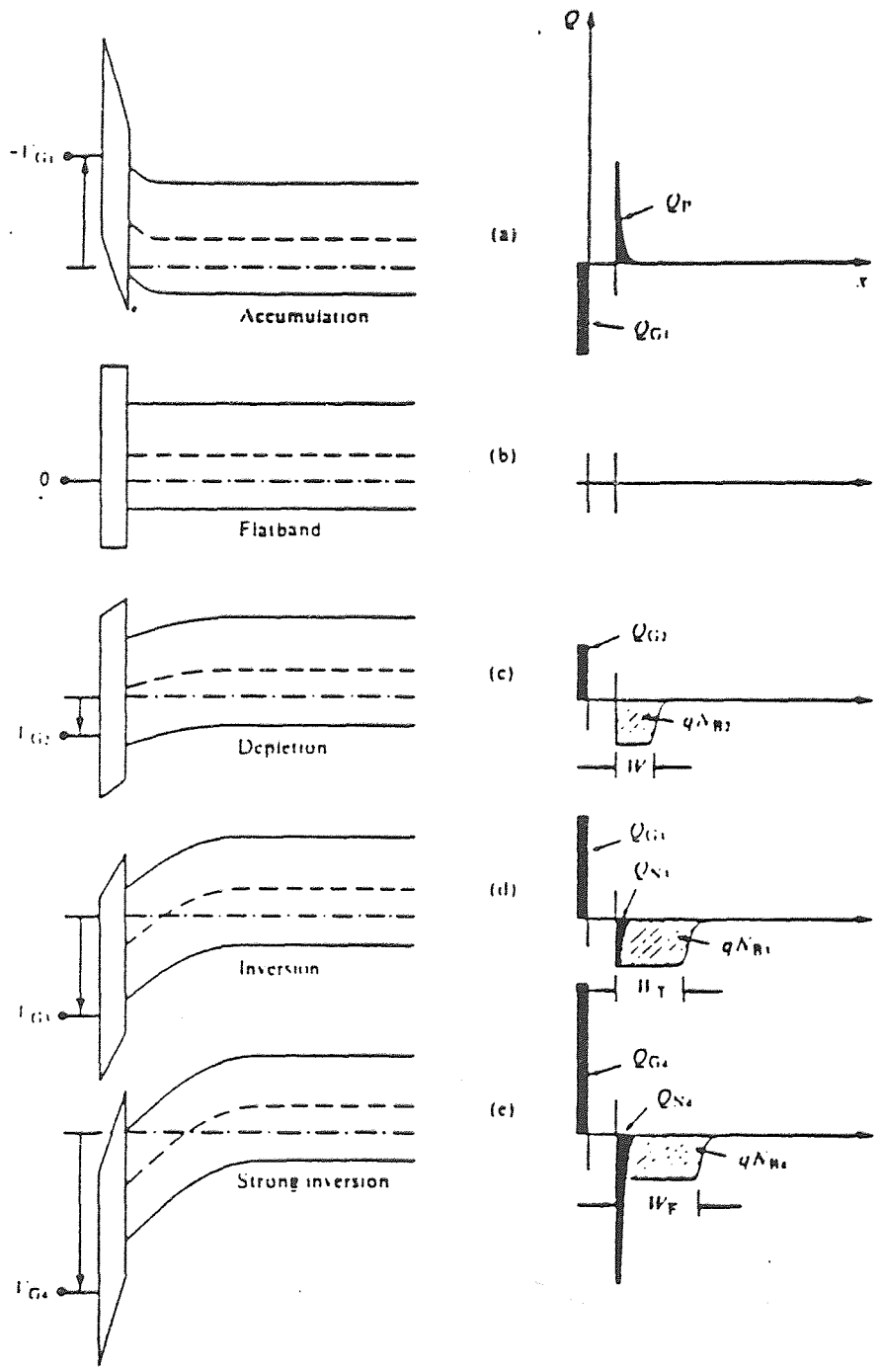
ELECTRICAL CHARACTERIZATION TECHNIQUES

4.1 Introduction

Radiation hard microelectronics is a vital part of research in the modern day high speed VLSI applications. Therefore the study of radiation induced defects is accomplished by a variety of device characterization techniques. We give importance to electrical characterization methods as they are the most relevant techniques capable of yielding information on device properties. Optical methods are also popular because of their non contacting nature and their high sensitivity is an important advantage. Chemical and physical characterization methods, with their high spatial resolution and ability to identify elements and compounds make them highly indispensable too. A popular technique for characterization of electrical properties of MOS structure is the C-V technique [38].

4.2 C-V Measurements

Various charges in the MOS system can be measured by the most popular approach of Capacitance-Voltage measurements. Before discussing the measurement methods, we will analyze the effect of gate voltage on MOS capacitances [39]. The energy band and charge distribution diagrams for a MOS capacitor on a p-type substrate for various bias voltages are shown in Figure 4.1. When the gate bias is swept from negative to positive values for a p-type MOS capacitor, the capacitance varies as shown in Figure 4.2 [39]. Figure 4.3 shows the high frequency (HF) curve and the deep depletion regime. We discussed previously accumulation, depletion and inversion with respect to energy bands. The corresponding cases in the C-V plot is shown in Figure 4.3. The C-V curve (a) to (e) in Figure 4.3 is experimentally obtained by sweeping the gate voltage. All the above



igure 4.1 Energy-band and charge-distribution diagrams for an MOS capacitor on a p-
›strate in (a) accumulation; (b) flatband; (c) depletion; (d) weak inversion and (e) strong inversion. [39]

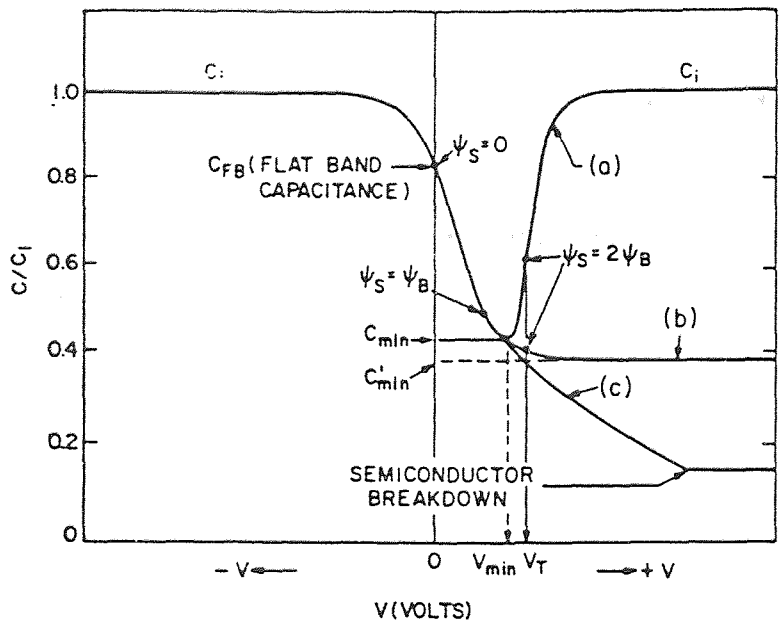


Figure 4.2 MOS capacitance-voltage curves: (a) Low frequency; (b) High frequency; (c) Deep depletion. [35]

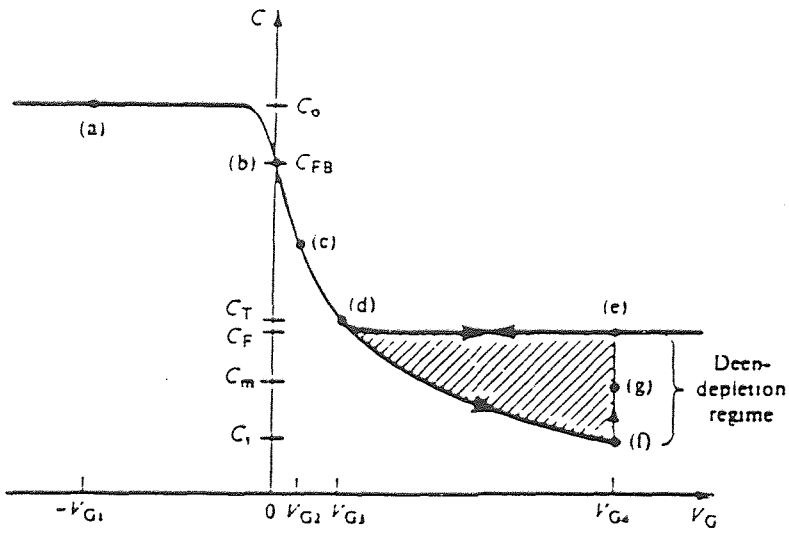


Figure 4.3 Capacitance-gate voltage curves for MOS capacitor. [39]

the above characteristics are related to p-type silicon substrate and we will limit ourselves to p-type substrate in the rest of the discussion.

Let us consider a MOS capacitor with the dc gate voltage swept from negative to positive voltages. Superimposed on the dc voltage is a small amplitude ac voltage of typically 10-15 mV amplitude which is necessary to measure the capacitance. The dc voltage determines the bias condition. The three capacitance voltage curves (Figure 4.2) are identical in accumulation and depletion. The energy band diagram of a MOS capacitor on p-type substrate is shown in Figure 4.4 [40].

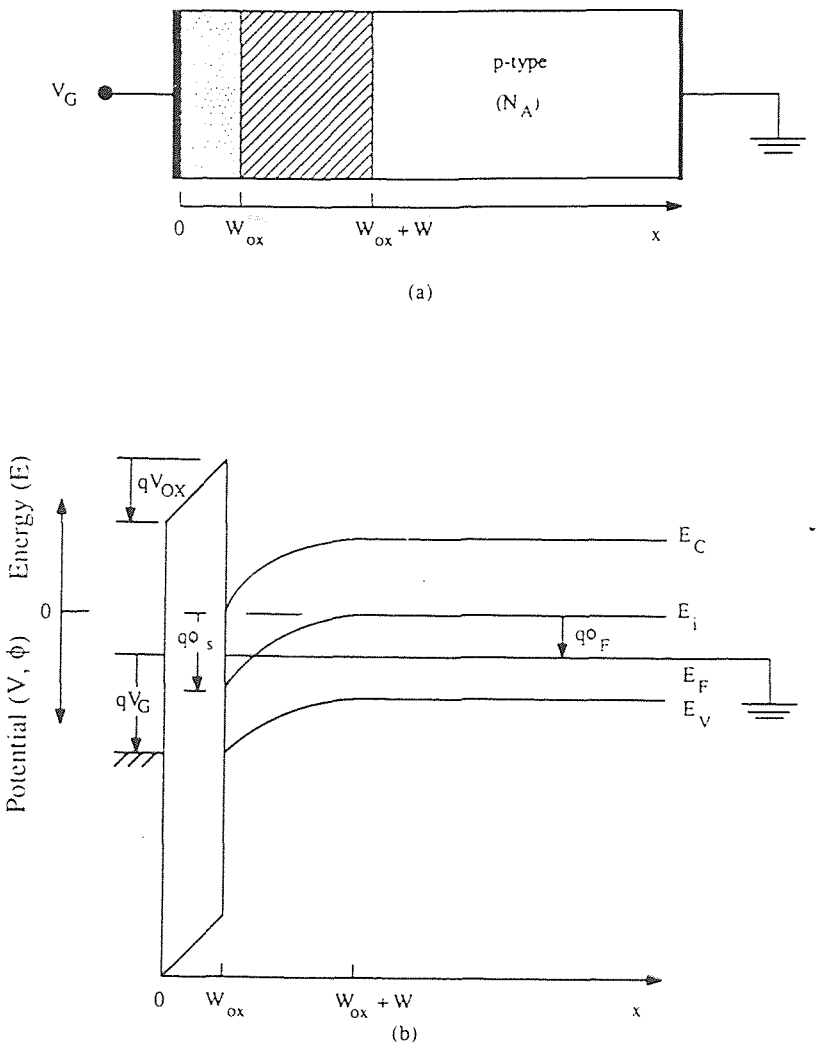


Figure 4.4 Cross section and energy band diagram of an MOS capacitor. [40]

The capacitance measured [40] between the gate and the substrate is given as:

$$C = \frac{C_{ox}(C_P + C_B + C_N + C_{it})}{C_{ox} + C_P + C_B + C_N + C_{it}} \tag{4.1}$$

where,

C_{ox} is the capacitance due to the oxide charge,

C_P is the capacitance due to the hole accumulation charge,

C_B is the capacitance due to the space charge region bulk charge,

C_N is the capacitance due to the electron inversion charge and

C_{it} is the capacitance due to the interface trapped charge.

Now we shall discuss the regions of accumulation, depletion and inversion with reference to the C-V plot:

(a) Accumulation: For sufficiently large negative voltages, majority carriers are attracted to the surface of the silicon leading to a p-type surface accumulation layer [41]. Since accumulation charge is very high, the four capacitances shown in Figure 4.5a are neglected and the equivalent capacitance reduces to Figure 4.5b [40]. The high concentration of holes near the Si surface can be thought of as forming the second electrode of a parallel plate capacitor with the gate electrode. Since the accumulation layer is in direct Ohmic contact with the p-type substrate, the capacitance of the structure under accumulation is approximately equal to:

$$C = \frac{A\varepsilon_{ox}}{t_{ox}} \tag{4.2}$$

where,

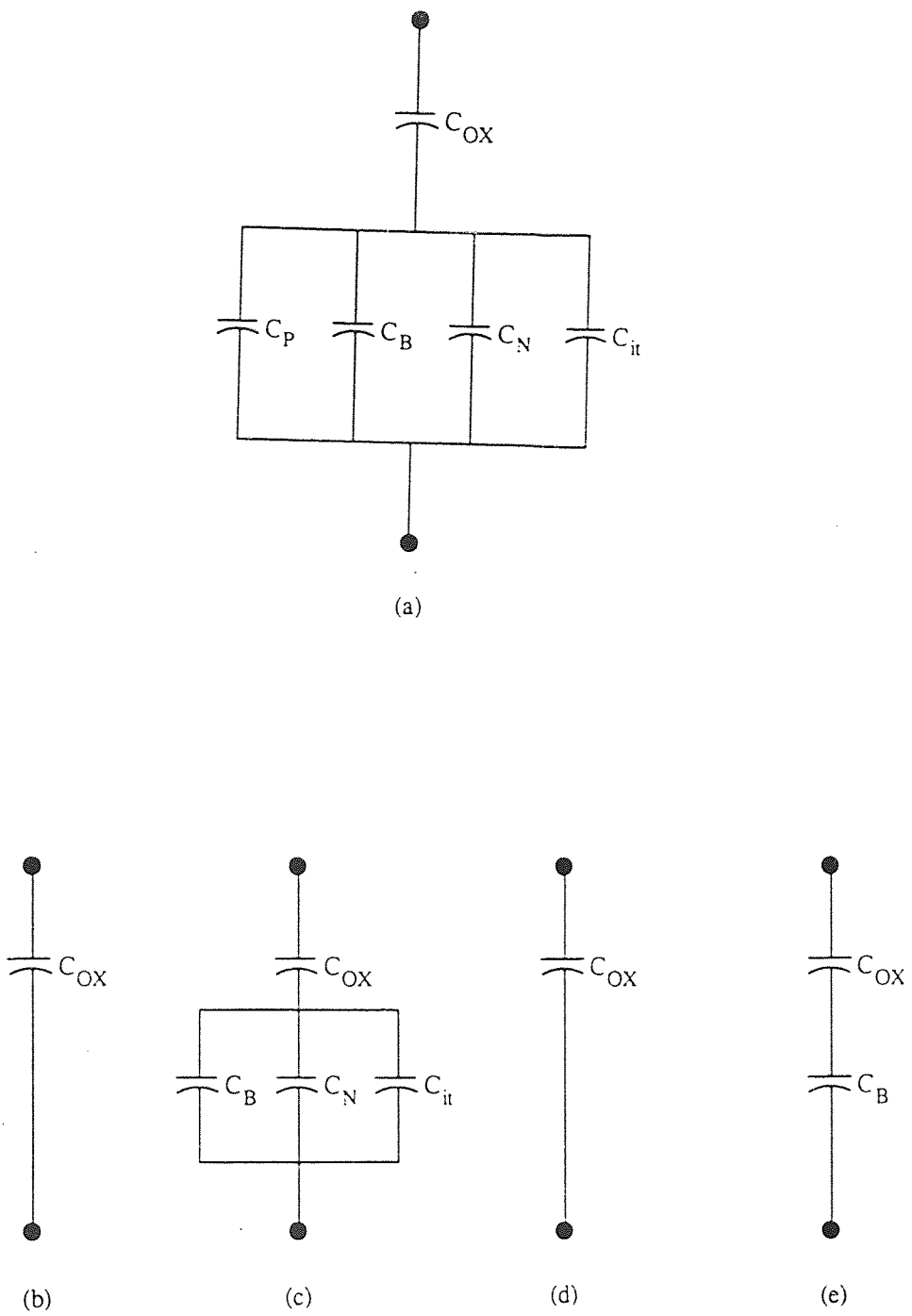


Figure 4.5 Capacitances of an MOS capacitor for various bias conditions as discussed in section 4.2. [40]

A is the area of the gate,

ε_{ox} is the permittivity of the oxide and

t_{ox} is the oxide thickness.

On the C-V plot (Figure 4.3), under negative voltage, the capacitance is the maximum recorded and hence is just the insulator capacitance.

(b) Depletion: When the gate voltage is increased, the surface hole concentration reduces and becomes zero and at this point only a surface depletion region consisting of immobile ionized acceptors will be present (Figure 4.1). In this case, the space charge dominates and the space charge region charge Q_B is:

$$Q_B = -qN_AW \tag{4.3}$$

where,

q is the electron charge,

N_A is the acceptor concentration and

W is the width of the surface depletion region.

As gate voltages become more positive, both Q_B and W increase. As the width of the surface depletion region increases, the capacitance from gate to substrate associated with the MOS capacitor structure will decrease which is shown in the equivalent circuit of Figure 4.5c [40]. The total capacitance is the combination of C_{ox} in series with C_B, which in turn is in parallel with C_{it}. C_N can be neglected in depletion region.

(c) Inversion: With the gate voltages becoming more positive, the surface depletion region will continue to widen until the onset of inversion in which case electrons are attracted up to the silicon surface to form n-type inversion layer. Under weak

inversion depicted in Figure 4.1, we apply the equivalent circuit of Figure 4.5c and in this case C_N is not neglected.

The width of the surface depletion region for a MOS structure in equilibrium will remain essentially constant after the formation of the inversion layer even if the gate voltage is made more positive. For strong inversion, C_N dominates because Q_N is very high. Now Q_N may or may not be able to follow the high frequency small signal ac gate voltage, superimposed on the dc bias and as such the capacitance of the MOS capacitor under inversion conditions is really a function of the frequency of the applied gate ac voltage.

If Q_N is able to follow the applied ac voltage, the equivalent circuit of Figure 4.5d is a good low frequency approximation and therefore the capacitance is nothing but the oxide capacitance. This is the LF CV curve (Figure 4.2). If Q_N is unable to follow the ac voltage, the equivalent circuit of Figure 4.5e is the high frequency approximation and therefore capacitance is the series combination of C_{ox} and C_B, giving the HF CV curve (Figure 4.2).

(d) Deep depletion: When the dc bias gate voltage is changed rapidly with insufficient time for the generation of inversion charge, then the device is driven into the deep depletion and this is point (f) in Figure 4.3 in the deep depletion curve. Under these conditions, the capacitance is less than the inversion capacitance for obvious reasons.

The three C-V curves (Figure 4.2) are identical in accumulation and depletion but deviate for positive gate voltages because the inversion charge is unable to follow the applied ac voltage for the HF case and does not exist in the deep depletion region. We now discuss charges in the oxide system and their measurement methods.

4.3 Oxide Charges and their Measurement Methods

4.3.1 Interface Trapped Charge (Q_{it})

The interface trap charge may arise from irradiation or other similar bond breaking processes [42]. The characteristics of interface trapped charge are briefly outlined in the following paragraphs.

The interface trapped charge may be either positive or negative. Structural, oxidation induced defects such as trivalent silicon centers [43] and metal impurities are other causes for the presence of traps. The density increases drastically with small amounts of hot electron trapping [44]. The introduction of Q_{it} into an ideal oxide charge free system will usually result in C-V curves which are distorted and stretched out along the voltage axis relative to the ideal case.

This is due to the variation in the total number of empty or filled traps as the Fermi level is swept across the band gap by changing the applied voltage. They exhibit trap time constant dispersion for laterally non uniform distribution of charges [45]. They can be reduced significantly by annealing at 400°C to 500°C in hydrogen containing ambients [46] or in nitrogen ambients if aluminum is used for the metal [47]. Characterization methods for interface trapped charge can be found in Nicollian and Brews [2], Goetzberger et al., [48] and De Clerck [49].

4.3.2 Quasi Static Method:

This technique [50,51] measures the density of interface trapped charge that contributes to low frequency (LF) capacitance but not to high frequency (HF) capacitance. The effect of interface traps on both HF and LF C-V curves is discussed by Schroder [40]. This method uses standard laboratory equipment and a suitable HF C-V set is also required. The procedure consists of recording the displacement current versus bias (low frequency curve) at a low sweep rate typically lesser than or equal to 100 mV/sec. The high

frequency curve is also plotted, superimposing the capacitance in strong accumulation (C_{ox}) on the corresponding quasi static plot. The resulting curves should resemble those in Figure 4.6. For long life time material, the quasi static curve capacitance may not recover to the C_{ox} value in inversion [52].

The calculation of interface trap density is done at a particular value of surface potential by the following equation: [53]

$$D_{it}(\phi_s) = \frac{C_{ox}}{q}\left(\frac{C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{HF}}{C_{ox} - C_{HF}}\right) \text{cm}^{-2}\text{eV}^{-1} \qquad (4.4)$$

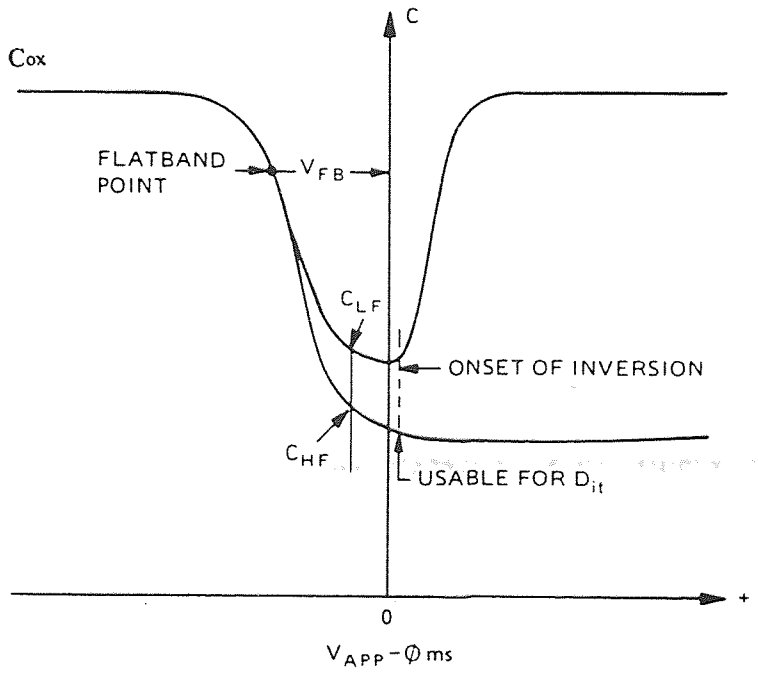


Figure 4.6 Quasi-static and High-frequency C-V curves used to determine the surface state density in the depletion region.

where,

$D_{it}(\phi_s)$ is the interface trap density at a particular value of surface potential,

C_{ox}, C_{LF}, C_{HF} are capacitances as shown in Figure 4.6 measured in farads/cm^2 and

q is the electronic charge.

It is not always necessary to measure D_{it} as a function of surface potential. We can use the graphical techniques proposed by several researchers [54, 55]. A brief overview of these techniques are given by Schroder [40].

4.3.3 Conductance Method

The frequency dependent conductance technique described in detail by Nicollian and Goetzberger [45] is generally considered to be the most sensitive method to determine D_{it}. The resolution of this method is around 10^9 cm^{-2}eV^{-1} as compared to the quasi-static method which has a resolution of 10^{10} cm^{-2}eV^{-1} . The measurements are very elaborate. Hill and Coleman [56] described a less elaborate approximation technique that combines q-V_G and C-V_G data at one frequency to calculate a minimum value of D_{it} between the midgap and flatband.

4.3.4 Other Methods to Measure D_{it}

Other high frequency methods like the Terman method [57] rely on a HF C-V curve measurement at a high enough frequency that interface traps are assumed not to respond. The Gray Brown method utilizes H-F capacitance as a function of temperature [58, 59]. The charge pumping method [60] uses a MOSFET as the test structure. A sensitive method is deep level transient spectroscopy [61-64]. Crystallographic structural information on interface traps can be obtained from electron spin resonance measurements [65] but it requires densities of $D_{it} \geq 10^{11}$ cm^{-2}eV^{-1} .

4.3.5 Oxide Trapped Charge (Q_{ot})

Radiation can induce electron traps that are neutral until filled by electrons or holes injected into the oxide. As discussed earlier, the charge located in the oxide may be positive or negative. The magnitude of Q_{ot} is a function of radiation dose and energy and the field across the oxide during irradiation [42]. Saturation of induced charge occurs with increasing dose [66] and it is also one of the findings of our research. Trapped positive charge can be annealed at low temperature in inert ambients [42]. RF plasmas can either generate or anneal out electron traps [67]. Low temperature anneals do not remove trap sites in oxides, but cause compensation of trapped charge. These trap sites can be refilled with holes or electrons [66]. Higher temperatures are required to remove trap sites. Radiation generates Q_{ot} as it also causes increase in interface trapped charge and its associated C-V curve distortion [43].

4.3.6 C-V Method

This method involves the measurement of the flatband voltage, which is used to calculate the concentration of oxide trapped charge and is given by:

$$\Delta N_{FB} = N_{ot} + (\Delta N_{it})_{FB} = \left(\frac{C_{ox} \Delta V_{FB}}{q} \right) \tag{4.5}$$

where,

ΔN_{FB} is the total change in flatband charge (cm^{-2}),

$(\Delta N_{it})_{FB}$ is the change in interface trapped charge density at $\phi_S=0$ (cm^{-2}),

C_{ox} is the oxide capacitance per unit area and

q is the electronic charge.

The term ΔN_{FB} is the difference in flat band charge before and after irradiation. The flatband voltage shift is generally interpreted by assuming the charge to be located at the SiO_2-Si interface and is given by [40]:

$$Q_{ot} = -\Delta V_{FB} C_{ox} \tag{4.6}$$

4.3.7 Photo I-V Method

This is a non destructive technique which yields information on neutral trap density. It is based on optically induced hot electron injection from the gate or from the semiconductor into the oxide. DiMaria et al., [68] have extensively discussed this method. A circuit implementation of this method has been explained by Li et al., [69]. Etch-off method is another important method for characterization of oxide traps.

4.3.8 Mobile Charge and Fixed Charge

Characteristics of mobile ionic charge [42, 70-73] depends upon processing conditions. When located near the SiO_2-Si interface, they cause parallel shift of CV curves along the voltage axis. Device instabilities from mobile ions are minimized by avoiding contamination during processing. One of the methods of characterizing mobile ions is the bias-temperature drift method [71]. Fixed oxide charge [42, 74] can be characterized using information obtained by work function and flat band voltages. Schroder [40] has given a complete explanation for this evaluation technique.

4.4 I-V Measurements

The current-voltage (I-V) measurements have been the index of a device characteristic for a long time. The behavior of two terminal devices like a diode or a three terminal devices like BJT, JFET, SCR has always been explained through non destructive I-V measurements. I-V technique has been used to measure the barrier height of a metal-

semiconductor contact. The breakdown mechanism of thin insulators can be studied by this technique. Usually both static and dynamic current-voltage measurements are used to study the damage effects and dielectric breakdown of thin SiO_2 films grown on etched Si surfaces. The effect of plasma on Si and breakdown of the oxide has been measured by I-V technique [75, 76]. Study of breakdown in dielectrics is essential to improve the reliability of VLSI and ULSI devices. Klein [77] has explained electronic dielectric breakdown based on band to band impact ionization. Radiation introduces charges in the oxide which might alter the breakdown statistics of insulators. To measure the true behavior of an oxide subjected to breakdown, a large number of devices will have to be tested which also depends on the quality of the device structure.

4.4.1 Conduction Process and Breakdown Statistics of Thin Insulators

In an ideal MIS diode, the conductance of the insulating film is assumed to be zero but in the real case there is significant conduction under high fields or temperatures. The basic conduction processes in insulators are summarized in Table 4.1 [35]. Under conditions of

Table 4.1 Basic conduction process in insulators. [35]

Process	Expression[a]	Voltage and Temperature Dependence[b]
Schottky emission	$J = A^{*}T^{2}\exp\left[\frac{-q(\phi_B - \sqrt{q\mathcal{E}/4\pi\epsilon_i})}{kT}\right]$	$\sim T^{2}\exp(+a\sqrt{V}/T - q\phi_B/kT)$
Frenkel–Poole emission	$J \sim \mathcal{E}\exp\left[\frac{-q(\phi_B - \sqrt{q\mathcal{E}/\pi\epsilon_i})}{kT}\right]$	$\sim V\exp(+2a\sqrt{V}/T - q\phi_B/kT)$
Tunnel or field emission	$J \sim \mathcal{E}^{2}\exp\left[-\frac{4\sqrt{2m^{*}}(q\phi_B)^{3/2}}{3q\hbar\mathcal{E}}\right]$	$\sim V^{2}\exp(-b/V)$
Space-charge-limited	$J = \frac{8\epsilon_i\mu V^{2}}{9d^{3}}$	$\sim V^{2}$
Ohmic	$J \sim \mathcal{E}\exp(-\Delta E_{ac}/kT)$	$\sim V\exp(-c/T)$
Ionic conduction	$J \sim \frac{\mathcal{E}}{T}\exp(-\Delta E_{ai}/kT)$	$\sim \frac{V}{T}\exp(-d'/T)$

bias, the electric field [35] in an insulator is given by:

$$E_i = E_s\left(\frac{\varepsilon_s}{\varepsilon_i}\right) \tag{4.7}$$

where,

E_i and E_s are electric fields in the insulator and the semiconductor, respectively and

ε_i and ε_s are the corresponding permittivities.

From the experimental statistical data [78,79], several causes of breakdown have been discovered and it has been determined that the breakdown is a local phenomenon. The electric measurements and SEM images [78] provide direct evidence of the existence of breakdown spots. Probabilistic models and distributions have given further insight into the breakdown fields and breakdown time [80]. Low field defect related breakdown and high field intrinsic breakdown [78] are the two different types of breakdowns that have been detected. Dielectric breakdown has been researched for many years and there are different methods [79,81] that have been used to evaluate dielectric breakdown. The important methods are summarized by Vankayalapati [76].

4.4.2 Fowler Nordheim Tunneling (FNT) in Thin SiO_2 Films

The dielectric strength of SiO_2 films, on silicon is an important factor for reliable VLSI and ULSI devices. It is well established that FNT contributes to current conduction in thin SiO_2 films. The FNT equation [82] is given by:

$$J = CF^2 e^{-\frac{\beta}{F}} \tag{4.8}$$

$$C = \frac{q^3 m_o}{16\pi^2 \hbar m_{ox} \phi_b} \quad ; \quad \beta = \frac{4(2m_{ox})^{\frac{1}{2}}}{3q\hbar}\phi_b^{\frac{3}{2}} \tag{4.9}$$

where,

F is the uniform electric field,

q is the electronic charge,

m_o, m_{ox} are the free electron mass and the effective electron mass in the oxide respectively,

$\hbar$ is the Planck's constant and

ϕ_b is the barrier height.

The role of roughness at the SiO_2-Si interface in determining the FNT current and breakdown mechanisms in MOS structures are presented by Ravindra and Zhao [83].

CHAPTER 5

EXPERIMENTAL PROCEDURE

5.1 Fabrication of the MOS Capacitor

The MOS capacitors used in our study were fabricated on p-type substrates. Figure 5.1a shows the process steps of a MOS capacitor array with an Al/Polysilicon gate whereas Figure 5.1b shows the process steps of a MOS capacitor array with an Al gate only. Now, we shall discuss the processing steps.

The MOS structures were fabricated on boron doped p-type [100] silicon wafers of 1.5 Ω-cm resistivity. The cleaning procedure was done in a 5:1 H_2SO_4:H_2O_2 solution at 110°C for 10 minutes. This was followed by a thorough rinsing with hot and cold deionized water for 10 and 5 minutes respectively. They were spin dried and again pre-cleaned by a dilute HF dip for about one minute. Then these wafers were subjected to a thorough rinsing and spin dried. Gate oxides (dry) were thermally grown on one set of wafers at 950°C and the thickness of the oxides were in the range of 12.5-40 nm. Another set of wafers with oxides (dry) grown at temperature of 1050°C were of thickness 100 and 450 nm. On one set of wafers, a 325 nm thick polycrystalline silicon (polysilicon) was deposited in an LPCVD system at 600°C using SiH_4 at a pressure of 400 m Torr for 2.5 hours. Subsequently, phosphorus diffusion was done at 950°C for one hour. A 500 nm thick Al film was deposited by sputtering on the polysilicon. The Al was patterned using a wet etch process and after the wet etch process, the reactive ion etching of poly was done. All the wafers received a back side aluminum deposition. The fabrication of the MOS capacitors with only Al as the metal followed the same steps except for the poly deposition and etching steps. Thickness of the oxide was measured at several points of the wafer by using an ellipsometer and Nanospec/AFT Model 200. The thickness was also

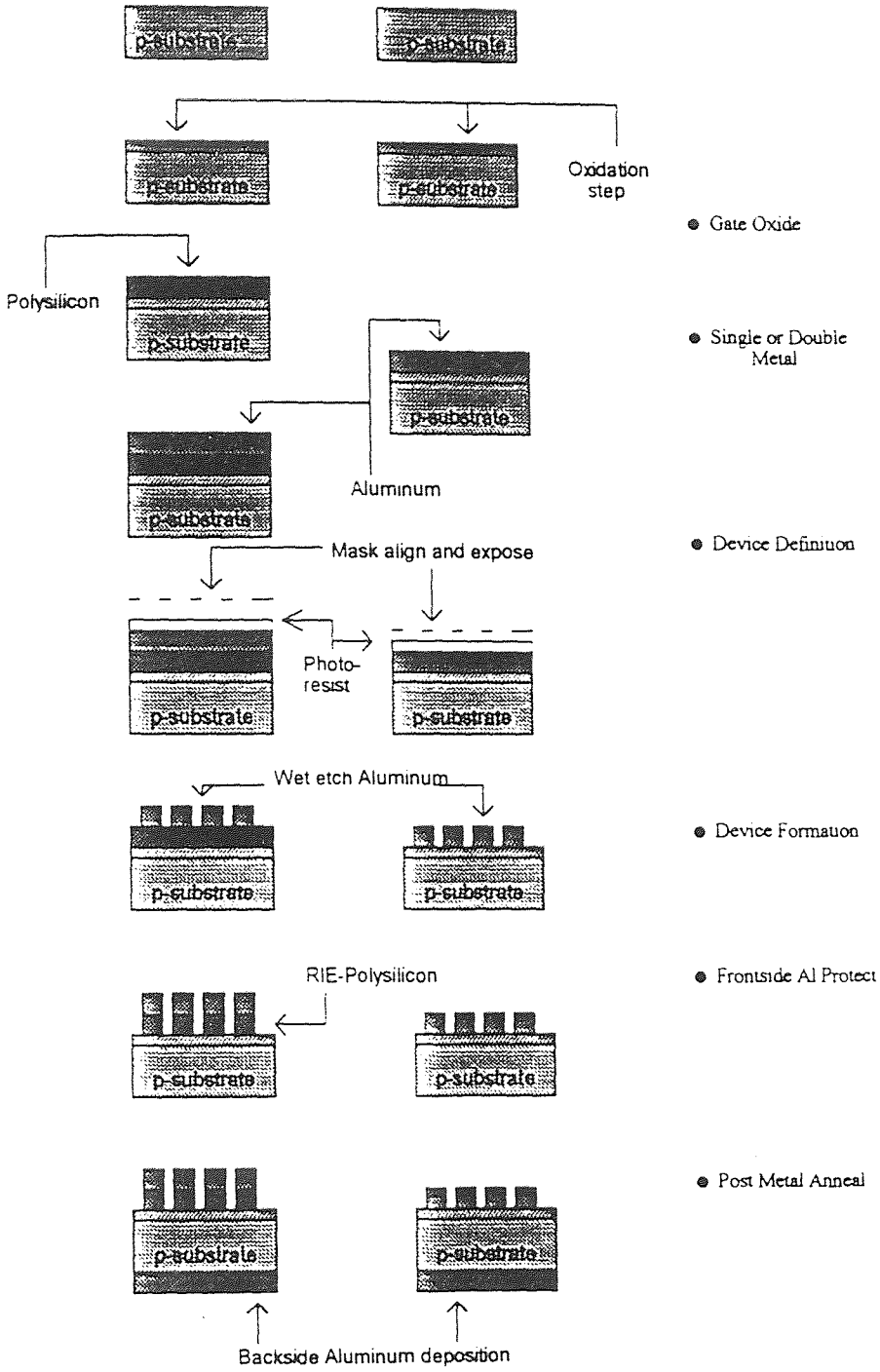


Figure 5.1 Process steps for a MOS capacitor array (a) with Al/poly gate (b) with Al gate only.

verified by determining the capacitance of the MOS capacitor in the strong accumulation region.

5.2 Oxide Thickness Measurement

The wafers, after the completion of oxidation process, were taken out from the furnace and were placed on Nanospec/AFT Model 200 which is an automatic film thickness measurement system. Wafers with different oxidation time were measured for their thickness. The thickness was measured at nine fixed points on each wafer so that the uniformity of measurement and accuracy could be maintained. Details of Nanospec/AFT Model 200 are given in Appendix E.

5.3 Method of Radiation

The MOS capacitors which were fabricated , as explained in the previous section, were subjected to gamma-radiation. A Co-60 source, at Brookhaven National Labs, was used for this purpose. This irradiation setup has been nominally rated at 1.85 MRad/hour but since then, the strength has decayed to a current rate of irradiation which is 1.5 MRad/hour. The duration of radiation was 15, 30, 45, 60, 75 and 90 minutes respectively. Assuming a current irradiation rate of the source as 1.5 MRad/hour, a package irradiated for 60 minutes will have received a radiation dose of 1.5 MRad. In this thesis, we analyze the effects of Gamma-ray irradiation on Al/Poly/SiO_2/p-Si/Al (Type I) and Al/SiO_2/p-Si/Al (Type II) device structures. The devices were irradiated for varying duration under no external bias. The MOS capacitors that were characterized by CV and IV methods had an area of 1.9634×10^{-3} cm^2.

5.4 Electrical Measurement Techniques

The following electrical measurements have been employed to investigate the effects of radiation: (a) high frequency (HF) 1 MHz and quasi-static capacitance-voltage (CV) measurements, (b) static current-voltage (IV) measurements. HF CV and quasi-static CV measurements were performed at room temperature (295 K) using an Allessi AER-01 probe station, Keithley 595 quasi-static meter and Keithley CMS version (2.0) software. The delay time involved in the measurements was 0.2 seconds and the step size was 10 mV. Most of the measurements were done with a sweep from +5 volts to -5 volts. The static I-V measurements were performed using a Keithley 236/237 source measure unit. The technique consists of a ramp voltage applied to a capacitor until the set current limit is reached. The contact to the counter electrodes is made by means of a probe placed directly on top of the capacitor.

From the HF and quasi-static CV measurements, we calculated the interface state density for the control samples as well as the irradiated wafers using the graphical technique proposed by Berglund [54]. The interface state density was calculated both at flatband and midgap conditions. The numerical values, thus obtained, were compared with those computed by the Keithley software and they were found to agree very well. In the next chapter, we will analyze and discuss the results from our characterization experiments.

CHAPTER 6

RESULTS AND DISCUSSION

6.1 Introduction

In this chapter, the experimental results of high frequency (HF) and quasi-static (QS) capacitance-voltage (CV) measurements, static current-voltage (IV) measurements have been summarized and discussed. This chapter has been divided into three sections. The first section deals with the oxidation kinetics obtained during the process described in chapter 5. The second section deals with the HF and QS CV analysis of control as well as irradiated samples. The third section discusses the IV measurements and their analysis.

6.2 Kinetics of Oxidation

The oxidation was performed on our wafers at two different temperatures of 950°C and 1050°C. The plot of dry oxide thickness versus time for our wafers is shown in Figure F.1 (Appendix F). This plot is compared with Figure F.2 (Appendix F) available in the literature [84]. When we compare the two plots, we observe that the oxidation kinetics for the temperature of 1050°C is almost similar in both cases. The wafers that we used in our study were also p-type and the orientation was <100>. The thickest oxide that we have grown is 450 nm and the oxidation time was 18 hours. Figure F.2 has a plot for <100> orientation p-type wafers and the plot shows an oxidation time of approximately 18 hours for a similar thickness in oxide. Hence, our oxide growth has been consistent with previous (oxide thickness versus time) results at a temperature of 1050°C.

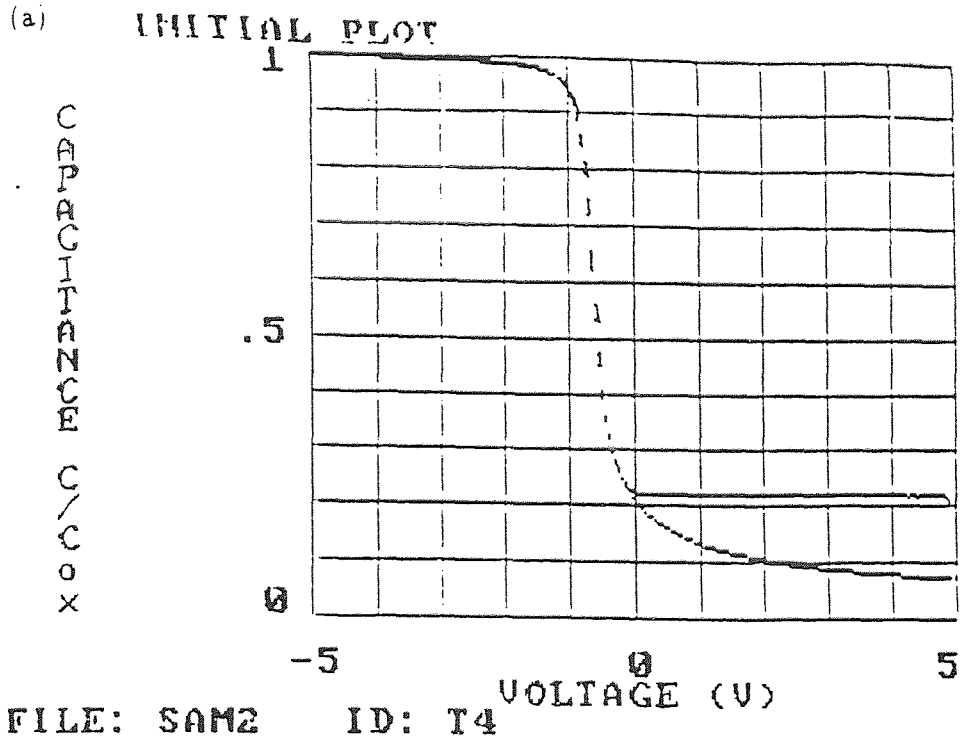
The temperature of 950°C is conducive to grow oxides in the thin oxide regime. The plot of dry oxide thickness versus time for this temperature is also shown in Figure F.1. From the plots, we get a clear indication of the effect of temperature on the thickness of oxide and also the variation in duration to grow a certain thickness. The growth is also

dependent on the orientation of the wafer. We observe from Figure F.2 that <111> wafers will have a thicker oxide growth for the same duration under same temperature, when compared to the <100> wafers. Thin oxides are grown at a lower temperature than the thick oxides.

6.3 Capacitance-Voltage Analysis

The CV measurements have been used to detect the change in the characteristics of a MOS capacitor subjected to radiation. As we know, past studies have indicated a change in flatband voltage and an increase in surface state density, among other important changes. Figure 6.1 shows the HF CV curves for p- and n-type samples. This difference in the shape of the characteristic curve follows from the physical aspect of the devices. The accumulation, depletion and inversion regions differ with respect to the voltages applied and as such, the HF curves for n- and p-type are transverse images of each other. Tables 6.1 and 6.2 summarize the HF and quasi-static CV measurements for the type I device structure (Al/Poly/SiO_2/p-Si/Al) and type II device structure (Al/SiO_2/p-Si/Al) respectively. As can be seen from Table 6.1, the capacitors which were characterized have been classified into four groups based on oxide thickness. Table 6.2 provides data for samples with two ranges of oxide thicknesses, one set of capacitors has less than 20 nm as the thickness and the other set has 20 nm oxide thickness.

First, we will discuss the results of each table and then we shall compare the two tables. For the type I device structure, we observe that there is an increase in flatband voltage (V_{fb}) with increase in radiation duration for all oxide thicknesses. The important factor is that the intrinsic flatband voltage for the control sample for different thicknesses is different. This change is appreciable in oxides >100 nm and the reason for this is due to



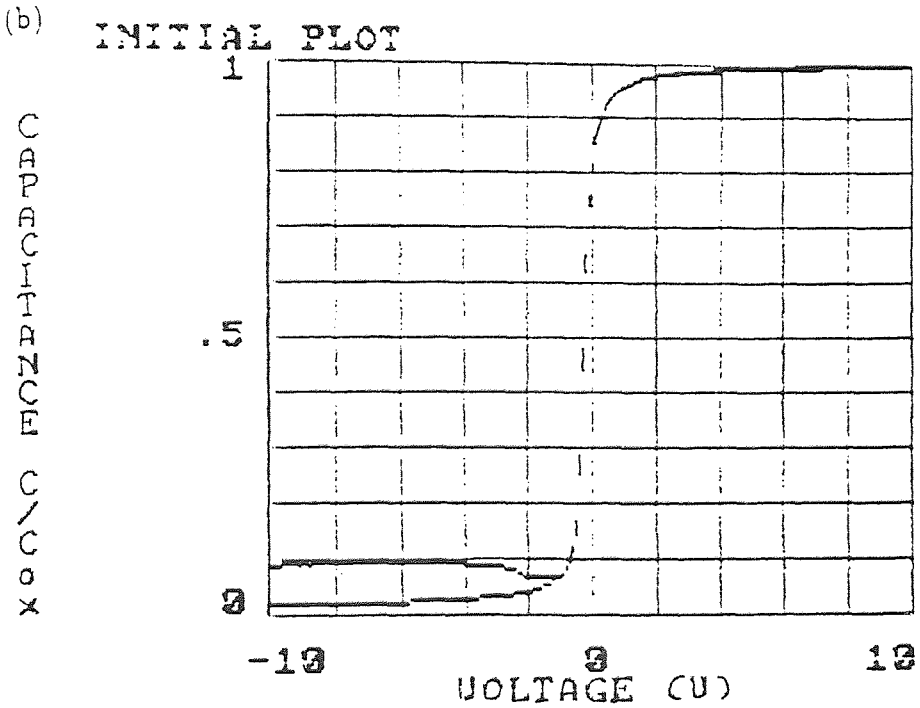


Figure 6.1 A representative experimental 1 MHz C-V curve of a MOS capacitor (a) p-type Si substrate; (b) n-type Si substrate.

Table 6.1 Summary of the HF and quasi-static CV characterization on type I device structures.

Thickness of the oxide (t_{ox}) Å	D_{it} (midgap) $cm^{-2}eV^{-1}$	D_{it} (Flatband) $cm^{-2}eV^{-1}$	Radiation duration (1.5 Mrad/hour source)	Maximum Capacitance (high frequency) pF	Maximum Capacitance (low frequency) pF	Minimum Capacitance (high frequency) pF	Minimum Capacitance (low frequency) pF	Flatband voltage (V_{fb}) volts
192	8×10^{9}	3.125×10^{10}	Control	347	347	42	48	-0.89
173	5.2×10^{10}	1.73×10^{12}	15 minutes	390	390	42	125	-1.02
170	7×10^{11}	2.77×10^{12}	30 minutes	396	396	44.5	160	-1.12
163	3×10^{12}	6.2×10^{13}	60 minutes	413	413	48.2	200	-1.21
221	7×10^{9}	1.58×10^{10}	Control	301	306	38	46	-0.89
230	2×10^{12}	8.1×10^{12}	30 minutes	293	293	40.5	160	-1.29
222	4×10^{12}	1.2×10^{13}	60 minutes	304	304	43.5	170	-1.32
438	1×10^{10}	1.36×10^{11}	Control	152.3	152.3	38	45	-0.93
429	3×10^{12}	5.7×10^{13}	30 minutes	150	150	30	125	-2.05
453	6×10^{12}	1×10^{14}	60 minutes	150	150	33	130	-2.1
1118	1×10^{10}	2.2×10^{11}	Control	59.7	59.7	26.4	30.4	-1.0
1123	5.1×10^{12}	4×10^{13}	30 minutes	60.2	60.2	25.9	58.1	-5.34

Table 6.2 Summary of the HF and quasi-static C-V on type II device structures.

Thickness of the oxide (t_{ox}) Å	D_{it} (midgap) $cm^{-2}eV^{-1}$	D_{it} (Flatband) $cm^{-2}eV^{-1}$	Radiation duration (1.5 Mrad/hour source)	Maximum Capacitance (high frequency) pF	Maximum Capacitance (low frequency) pF	Minimum Capacitance (high frequency) pF	Minimum Capacitance (low frequency) pF	Flatband voltage (V_{fb}) volts
151	5×10^{10}	4.13×10^{11}	Control	441	441	40	66	-0.77
193	8×10^{11}	1.58×10^{12}	30 minutes	349	349	43.5	148	-0.91
136	1×10^{12}	3.5×10^{13}	60 minutes	497	497	40	210	-0.94
200	5×10^{10}	3.9×10^{11}	Control	332	332	42.8	60	-0.77
200	7×10^{12}	1.4×10^{13}	60 minutes	340	340	41	190	-1.1

the variation in oxidation temperature. From chapter 5 , we notice that the thicker oxides (100 nm - 450 nm) were grown at 1050°C and the thinner oxides (12.5 nm - 40 nm) were grown at 950°C. We observe that the flatband voltage (control samples) for very thin oxides (16 nm - 23 nm) is the same, but it increases with the oxide thickness in the range of 100 - 500 nm. Derbenwick and Gregory [85] have found that the flatband voltage shift varies as the cube of the oxide thickness for dry oxides for high energy radiation. The radiation induced flatband voltage shift in oxides grown in dry oxygen varies linearly with oxide thickness [86]. Because radiation induced positive oxide charge is located at the SiO_2/Si interface, the charge centroid is equal to the oxide thickness. If the radiation induced oxide charge density is independent of oxide thickness, the flatband voltage shift will vary linearly with the oxide thickness [2]. For the type I device structures, for oxide thicknesses less than 20 nm, the variation of V_{fb} with radiation dose (RD) is as follows: an increase in V_{fb} with RD for the first thirty minutes (0.75 Mrad) is followed by a saturation of V_{fb} with RD for doses greater than 1.5 Mrad. Flatband voltage shift (ΔV_{fb}) for oxide thicknesses in the range of 110 nm is higher than ΔV_{fb} for thinner oxides for the same RD.

Type II device structures show the same kind of behavior as type I with respect to changes in flatband voltage for thin oxides. But V_{fb} in the control sample of type I device is more than that for type II because of the differences in work function for the two gate materials. ΔV_{fb} for type I device for an irradiation of 60 minutes is more than that for type II device for oxide thicknesses in the range of 15 nm to 23 nm. Therefore, we note that ΔV_{fb} is thickness dependent as evidenced from CV measurements and reported by previous workers. [85,86]. ΔV_{fb} is more in thick oxides (100 nm) than in thin oxides (15 nm) for the same irradiation duration. The same kind of behavior is reported by Naruke et al., [87] but their devices were biased positively or negatively during irradiation. In our case, the MOS capacitors were not biased during irradiation. It is also observed that the saturation in V_{fb} is more prominent in thick oxide (45 nm) than thin oxide (20 nm) for an irradiation time of 60 minutes for the type I device structure.

For small doses of radiation in the range of 10^4 rads, it is reported [22] that an increase in V_{fb} due to low irradiation dose is evident but with increasing irradiation dose, the increase of flatband voltage shift stops and reverses direction. However, we have not observed this kind of behavior because our irradiation dose was much higher in the region of 10^5 rads. The dose dependence of V_{fb} can be explained as follows: Under very heavy doses, the increase of trapped holes become dominant compared with the increase of interface states, resulting in the V_{fb} shifts in the negative direction. The dependence of V_{fb} on oxide thickness varies with the oxide quality. A distribution of hole traps into the oxide from SiO_2-Si interface , the possible dependence of hole trap density on oxide thickness, and interface traps generated at high doses could alter the square law dependence [86]. The square law dependence was predicted assuming uniform generation of interface states due to the radiation. Under conditions of uniform generation in the oxide and trapping of a constant fraction of the generated holes, the oxide trapped charge will vary linearly with the thickness and therefore the radiation induced flatband voltage shift varies as the square of the oxide thickness. It is not known why the oxide thickness dependence of the flatband voltage shift is so varied.

Figures 6.2 - 6.4 illustrate HF and quasi-static curves on control as well as irradiated MOS capacitors for the thinnest oxide group (17 nm - 20 nm) belonging to the type I device structure. From these figures, we can clearly see the change in shape of the quasi-static curve with increase in radiation dose. Figures in appendix A show similar plots for different oxide thicknesses for type I as well as type II device structures. From these plots, we have summarized the salient features of radiation damage on MOS capacitors in Tables 6.1 and 6.2 and these plots provide us with a better understanding of the role of radiation dose on device capacitance. Figures 6.5 - 6.7 illustrate the effect of irradiation on interface trap density (D_{it}) for the type I device structures for the thinnest oxide group (17 nm - 20 nm). We can clearly see the increase in interface state density at midband for the irradiated MOS capacitors. When compared with reference to the control sample, the

MOS capacitor irradiated for thirty minutes has almost two orders of magnitude higher interface state density at midband and the capacitor irradiated for sixty minutes has three orders of magnitude higher interface state density at midband. Similar plots for type I and type II devices are included in appendix B for different oxide thicknesses to help us have a clear understanding of the variation of interface state density as a function of oxide thickness (Control samples). We find from Tables 6.1 and 6.2, that the minimum capacitance as obtained from the quasi-static measurement increases with increase in radiation duration. Magnitude of surface state density has been calculated by the Berglund's technique [54] (Equation 4.4). From the Figures 6.5 - 6.7 , we observe that the interface state density for the irradiated samples increase when compared to the control

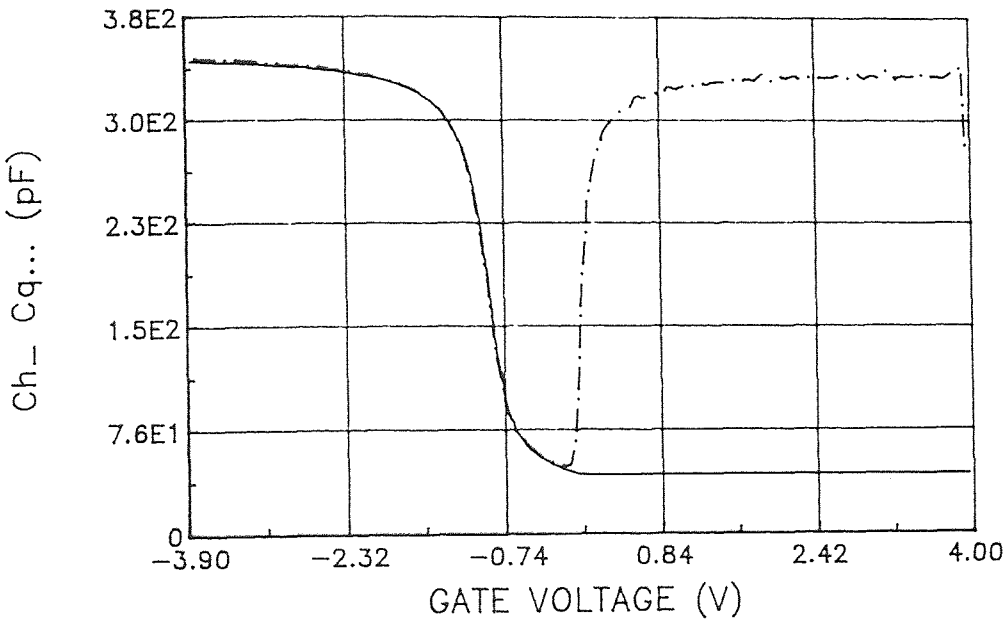


Figure 6.2 HF CV and quasi-static CV curves for type I device structure with t_{OX} = 19.2 nm (Control sample).

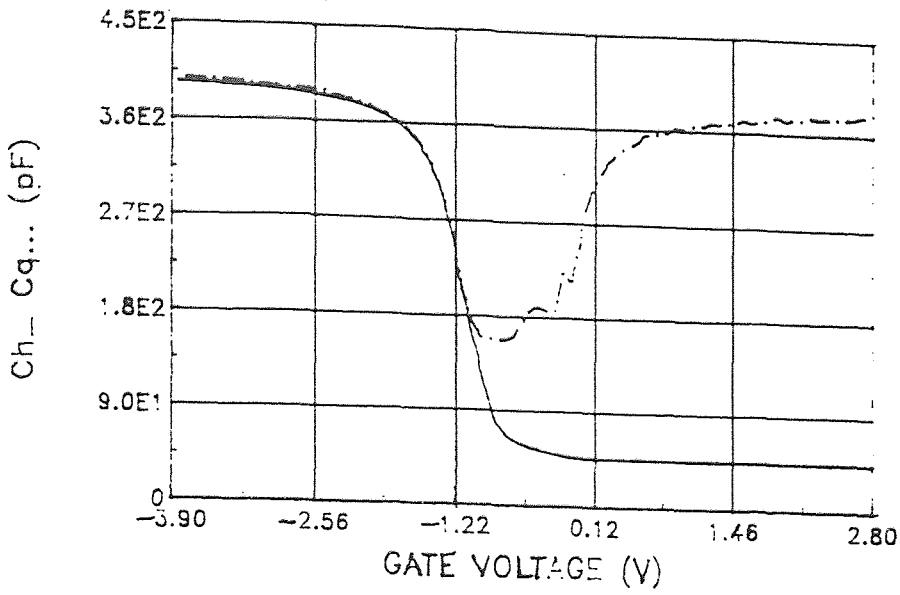


Figure 6.3 HF CV and quasi-static CV curves for type I device structure with t_{ox} = 17 nm (sample irradiated for 30 minutes).

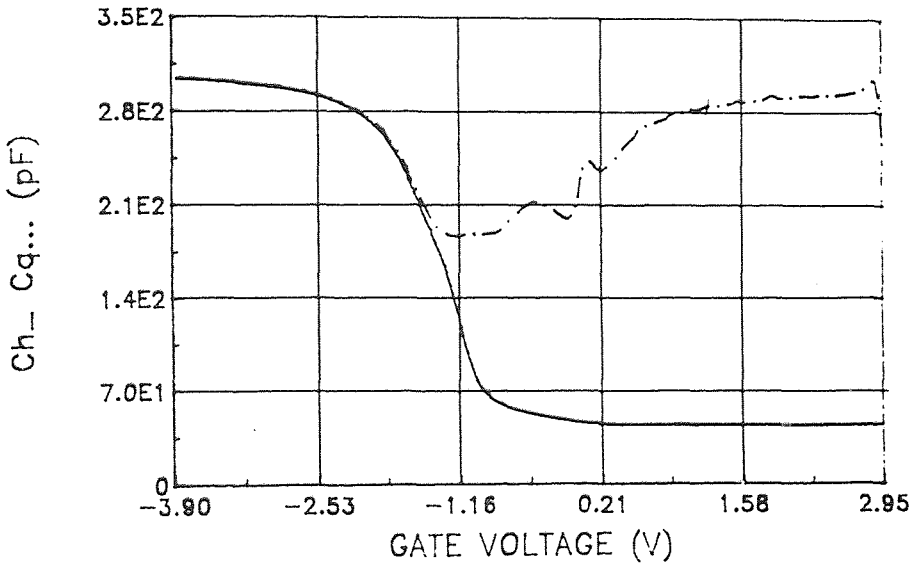


Figure 6.4 HF CV and quasi-static CV curves for type I device structure with t_{ox} = 20 nm (sample irradiated for 60 minutes).

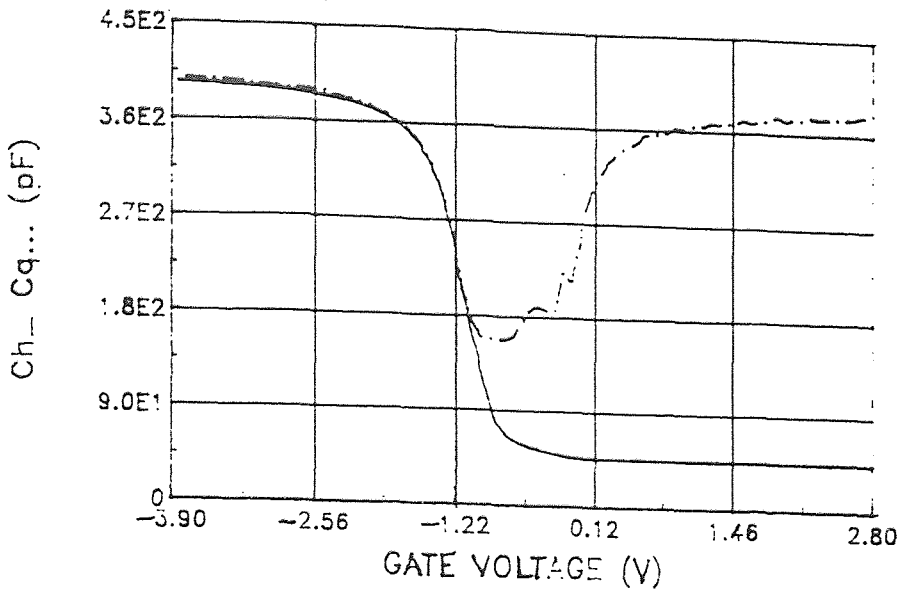


Figure 6.3 HF CV and quasi-static CV curves for type I device structure with t_{ox} = 17 nm (sample irradiated for 30 minutes).

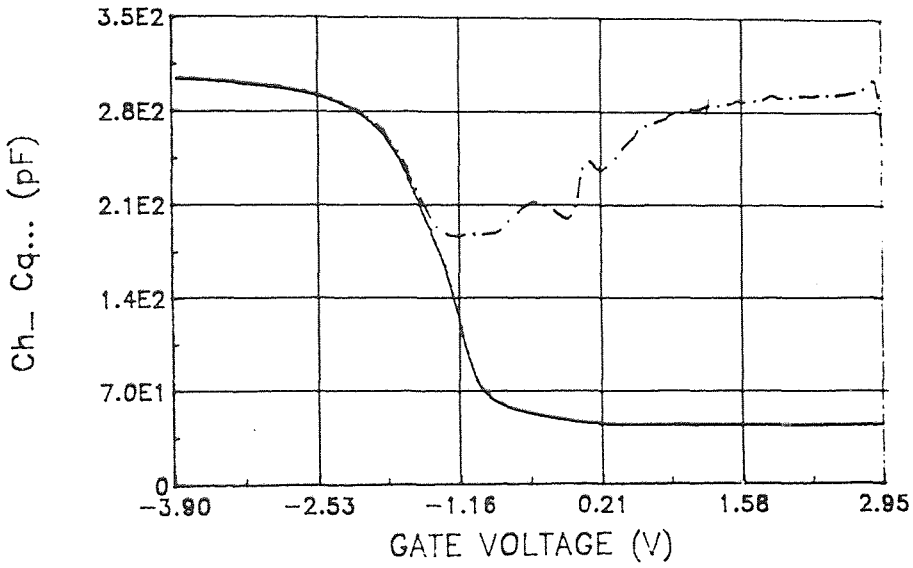


Figure 6.4 HF CV and quasi-static CV curves for type I device structure with t_{ox} = 20 nm (sample irradiated for 60 minutes).

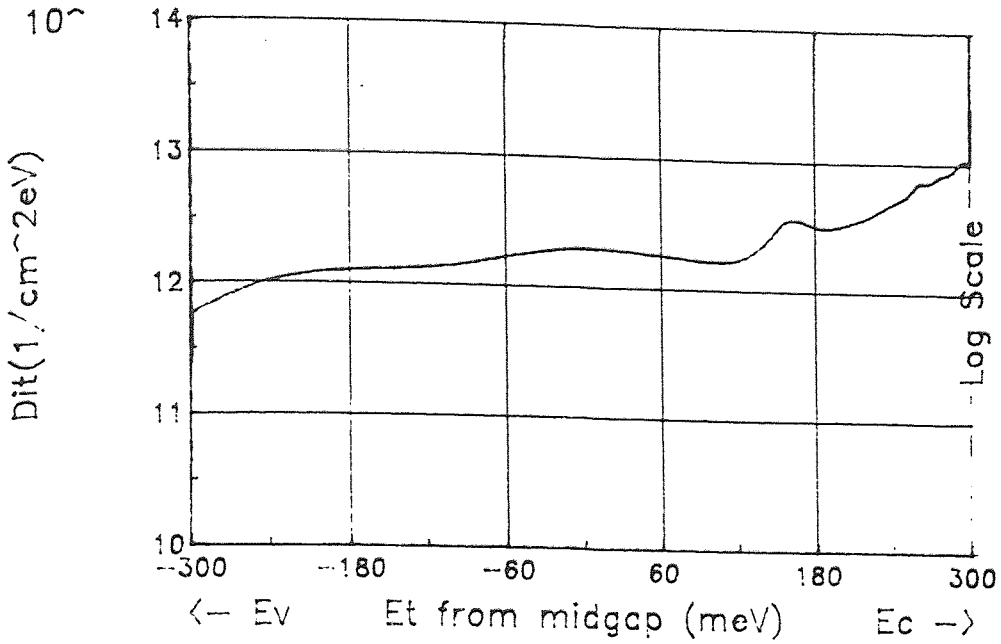


Figure 6.7 D_{it} plot for type I device structure with t_{ox} = 20 nm (sample irradiated for 60 minutes)

samples for varying oxide thicknesses. From Tables 6.1 and 6.2, we observe that D_{it} at flatband is always greater than the interface state density at midgap for both device types and for control as well as irradiated wafers. We see that the radiation dose of 1.5 x 10^6 rads is insufficient to saturate the generation of interface state density. Radiation damage studies by Gupta et al., [19] performed on MOS devices fabricated on n-type Si yield results similar to those being reported here for p-type substrates. Another remarkable observation between the two device structures is the difference in the interface trap density in the control and irradiated capacitors. There is an order of magnitude difference between type I and type II device structures in the trap density for control samples for thin oxides (15 nm - 19 nm). But the trap density has almost the same quantitative saturation levels for high doses in both the device structures. Zvanut et al., [88] have discussed the defect density and net oxide charge produced in wet and dry thermal oxides subjected to a

treatment in H_2 and irradiation with no applied bias. Their quasi-static analysis for irradiated MOS structures comprising of wet oxide, show a uniform distribution of interface states for the film without H_2 treatment and a distribution with two peaks in the Si bandgap for the H_2 treated film. We have observed such dual peaks in our quasi-static analysis (Figures A.4, A.5) for much thinner oxides (~ 45 nm) irradiated for a duration of thirty minutes and our samples were not H_2 treated. From our results, it appears that irradiation of dry oxides also generates states at discrete energies.

The mechanism of radiation induced interface state creation are primarily due to three processes [89]: (a) electron-hole recombination near the interface, (b) A multi step process wherein holes in the SiO_2 bulk interact with hydrogen to form H^+ ions which then transport to the interface [6, 90] and (c) the neutral hydrogen diffusion model proposed by Griscom [91]. There still remains a controversy on which process dominates. Of the several mechanisms that have been proposed for the generation of interface states, it is more likely that interface trap creation is when electron-hole pairs are produced in the oxide by radiation. The clustering of the low mobility radiation induced holes near the interface is due to the field present in the oxide. The main consideration is that the radiation induced charge density increases with increasing oxide thickness for high energy radiation and later saturates.

6.4 Current-Voltage Analysis

The static IV analysis was performed to observe the changes in currents in irradiated capacitors, when compared to the control samples. Our analysis was confined only to observe the magnitude of current and we have performed only non destructive breakdown studies of the dielectric. The results of the static IV analysis are summarized in Table 6.3 for type I devices. Figures 6.8 - 6.14 show the static IV plots for control as well as irradiated MOS capacitors for type I device structures for two oxide thicknesses (17 nm & 23 nm). Similar IV plots for type I and type II device structures for different oxide

Table 6.3 Summary of the static I-V characterization on type I device structures.

Radiation duration (1.5 Mrad/hour source)	Thickness of the oxide (t_{ox}) Å	Current at maximum voltage sweep (amperes)	Voltage at maximum voltage sweep (volts)
Control	170	-6.5×10^{-10}	-14
15 minutes	170	-5.3×10^{-9}	-13
45 minutes	170	-6.8×10^{-9}	-14
Control	230	-5.75×10^{-10}	-19
15 minutes	230	-5.5×10^{-9}	-19
45 minutes	230	-6.5×10^{-8}	-19
Control	430	-6.5×10^{-10}	-33
15 minutes	430	-2.3×10^{-9}	-33
45 minutes	430	-2.4×10^{-9}	-30
90 minutes	430	-8.4×10^{-9}	-28

thicknesses are included in appendix C. We observe that the radiation induced charges are responsible for the increase in current through the device for the same voltage applied across the device. In Figures 6.8 - 6.14, we observe that the magnitude of current in a control sample, for a given oxide thickness, is recorded for an irradiated wafer at a much lesser value of applied voltage. Results reported by previous workers [17] using IV technique have found current peaks in the IV characteristics due to mobile Na ions. This study [17] also reported that there is an increase in mobile sodium after radiation. The reason is that: a great deal of sodium is present in MOS oxides than is electrically active, indicating that some sodium is bound up in deep traps in an electrically neutral state. Under the influence of ionizing radiation, Si-O-Na or Si-Al-Na bonds are broken and some of this sodium is promoted to shallow traps. Under the influence of post-radiation electric

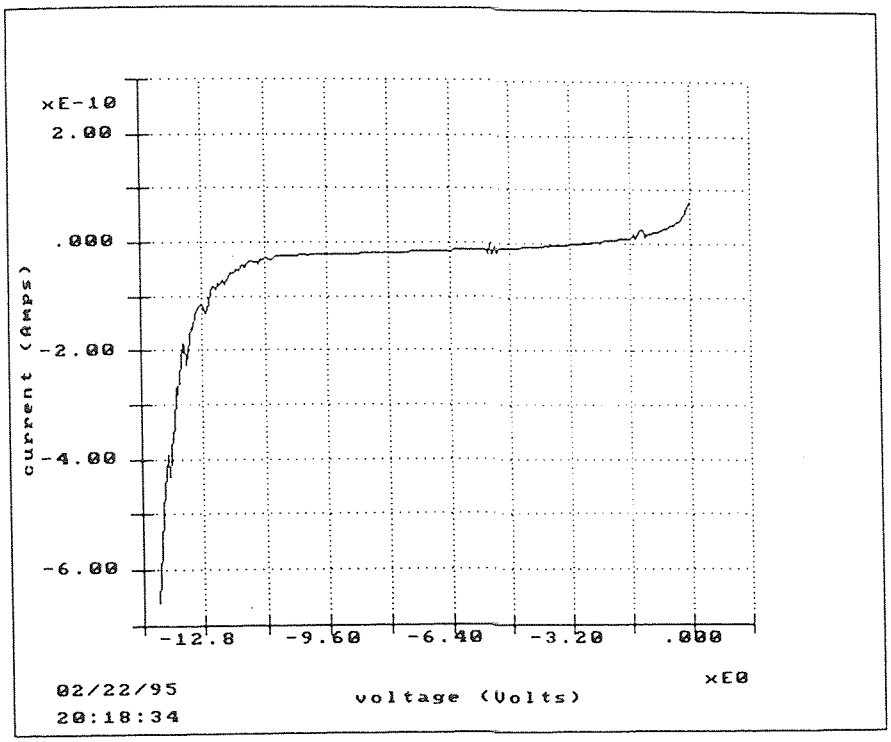


Figure 6.8 Static IV plot for type I device structure with t_{ox} = 17 nm (Control sample)

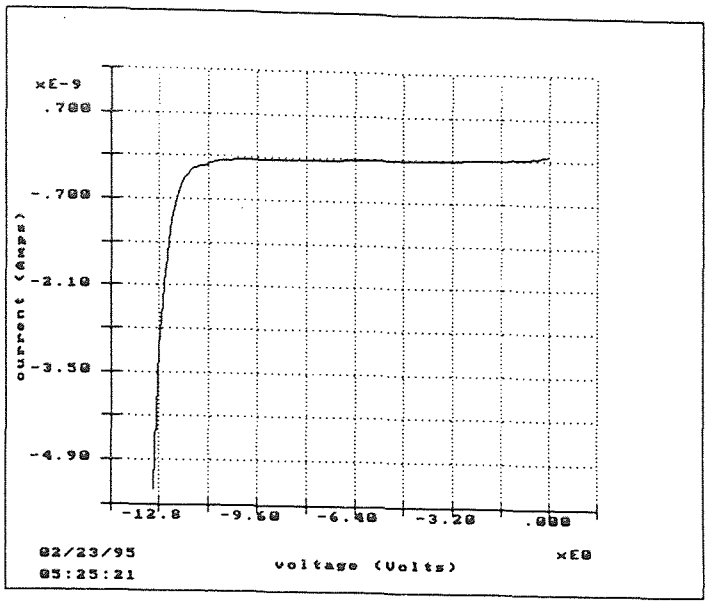


Figure 6.9 Static IV plot for type I device structure with t_{ox} = 17 nm (sample irradiated for 15 minutes).

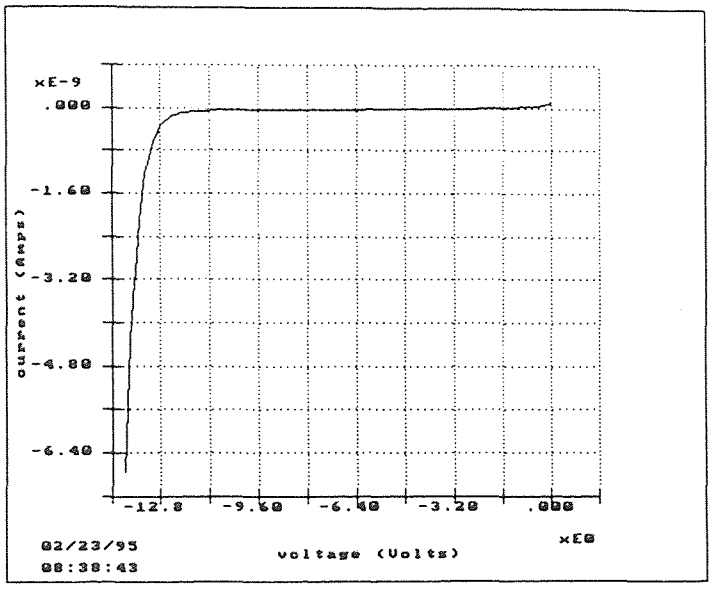


Figure 6.10 Static IV plot for type I device structure with t_{ox} = 17 nm (sample irradiated for 45 minutes).

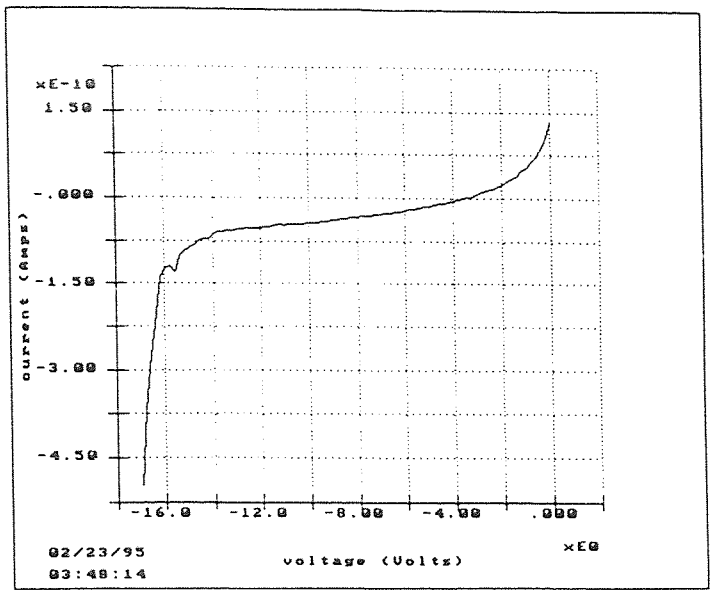


Figure 6.11 Static IV plot for type I device structure with t_{OX} = 23 nm (Control sample).

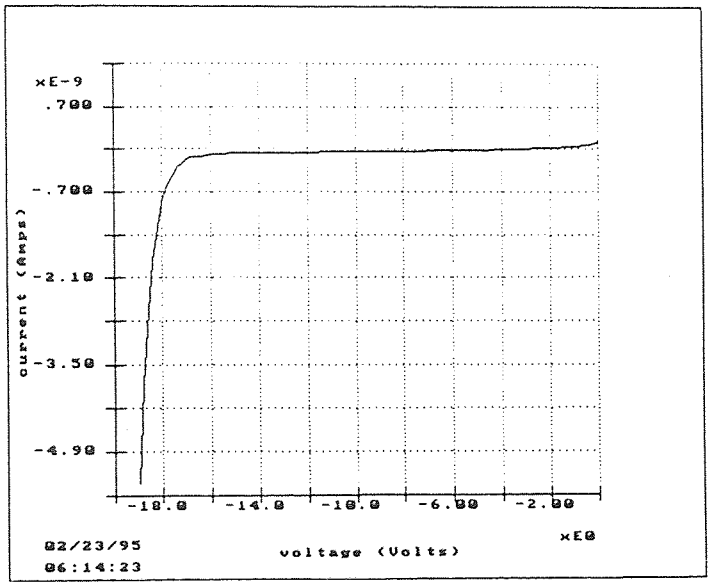


Figure 6.12 Static IV plot for type I device structure with t_{OX} = 23 nm (sample irradiated for 15 minutes).

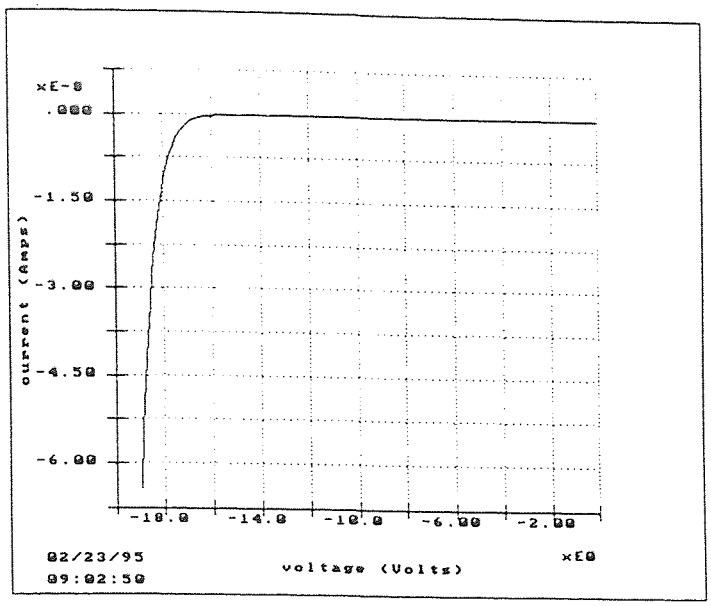


Figure 6.13 Static IV plot for type I device structure with t_{OX} = 23 nm (sample irradiated for 45 minutes).

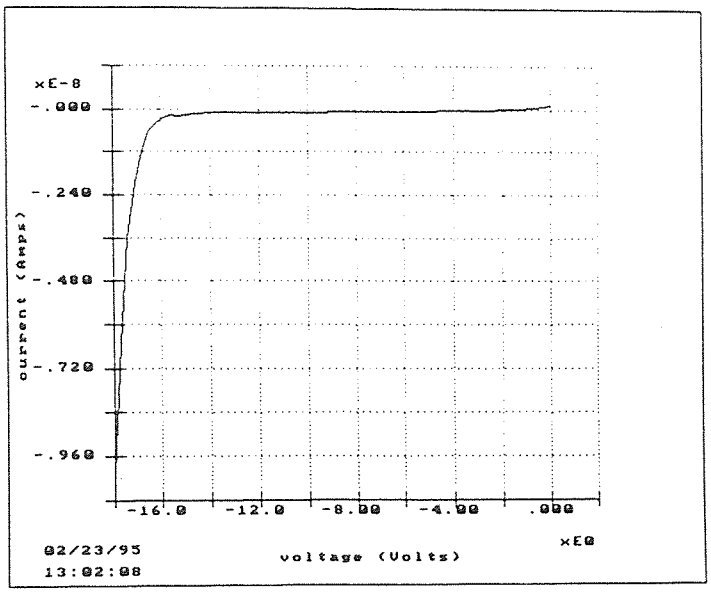


Figure 6.14 Static IV plot for type I device structure with t_{OX} = 23 nm (sample irradiated for 90 minutes).

fields associated with the IV measurement, this sodium would become mobile.

We observe that the devices irradiated for a longer time showed increase in currents by almost an order of magnitude for the same applied voltage across the control sample. Table 6.3 and Figures 6.8 - 6.14 show results for different oxide thicknesses and the breakdown is hastened by the increased dose received by some of the samples. Figure 6.15 shows the Fowler-Nordheim tunneling plot for control and sample irradiated for 45 minutes. There is a marked increase in current density for the irradiated MOS capacitor and is due to the FNT component as well as the radiation induced current. It is believed that the radiation induced current is thickness dependent [92]. The radiation induced conductivity of MOS structures in the field region at the SiO_2-Si contact is dependent on the bulk properties of silicon dioxide.

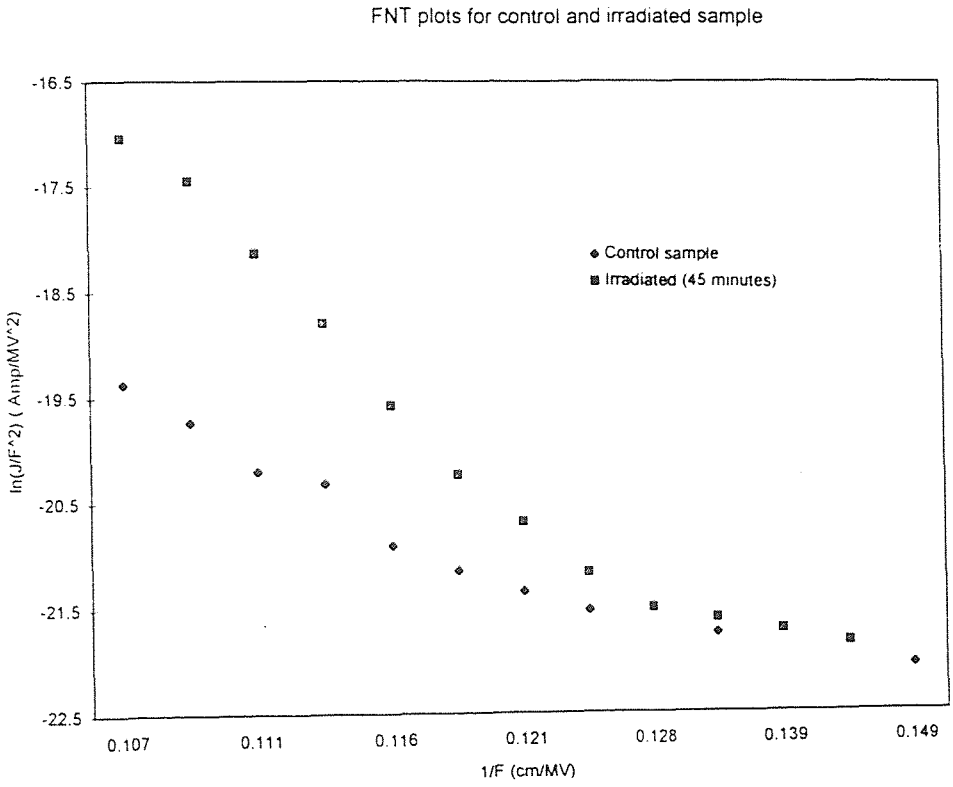


Figure 6.15 Fowler-Nordheim tunneling plot for type I device structure with t_{ox} = 17 nm for control sample and sample irradiated for 45 minutes

Irradiation of MOS structures forms a positive space charge near the SiO_2-Si boundary and, starting at fields greater than 6.5 MV/cm, causes tunnel injection of electrons from silicon to silicon dioxide. Radiation induced current consists of both electron and hole constituents and its dependence on the oxide thickness is due to the absorbed radiation dose in the SiO_2 film.

CHAPTER 7

CONCLUSIONS

In the previous chapter, the experimental results of the electrical characterization of control and irradiated MOS structures formed on p-type Si substrates have been discussed. The characterization techniques employed in the research work are high frequency (HF) and quasi-static (QS) capacitance voltage (CV) analysis and static current voltage (IV) analysis.

Based on experimental results obtained from HF and QS CV analysis, it was observed that the flatband voltage increases with increase in radiation dose for both types of device structures - Al gate capacitors and Al/Poly gate capacitors. There seems to be no change in behavior of flatband voltage with respect to the above gate materials. However, a change has been observed in the past with other gate materials like silicides of tungsten. We have modeled the CV characteristics of the MOS system to be dependent on interface state densities and have not considered the contributions of the other charges in the bulk of the oxide in the present study. With this model in mind, we have found that the interface state generation increases with increase in radiation dose and this behavior is consistent with oxides of varying thicknesses. At very high doses, the shift in flat band voltage saturates more quickly, with respect to radiation dose, for thin oxides than thick oxides. This study had not been performed previously. A critical examination of experimental results presented in this thesis indicate that the radiation behavior of MOS capacitors with Al gates has been similar to the MOS capacitors with Al/Poly gates.

The static IV measurements show a significant role played by radiation induced traps. The currents for a particular thickness of a MOS capacitor at a particular voltage is found to increase with increase in radiation dose. From IV plots, it has been observed that the devices without irradiation have higher breakdown fields than the irradiated devices.

By comparing FNT plots, radiation induced charge is found to contribute to the tunneling component of current. This study has not been reported previously in the literature.

The past research indicates that there is no difference in radiation induced behavior of capacitors with bias when compared to the capacitors without bias for bias voltages that are in the range where most electronic devices operate today. However, from past research, it is not clear about the radiation induced behavior for high bias and further studies are required to explain the behavior of MOS capacitors with high bias applied during irradiation. The radiation hardness of capacitors can be tested for various dielectrics like Si_3N_4 and SiC with different gate materials involved in the modern VLSI processing. A modest approach was made in our study to compare the existing data in the literature and to compile them and compare with our results.

APPENDIX A

HIGH FREQUENCY & QUASI-STATIC CV PLOTS

Here, high frequency (HF) and quasi-static (QS) capacitance voltage (CV) curves for type I and type II device structures are presented. Plots for both control as well as irradiated MOS capacitors are included. The plots are for different oxide thicknesses.

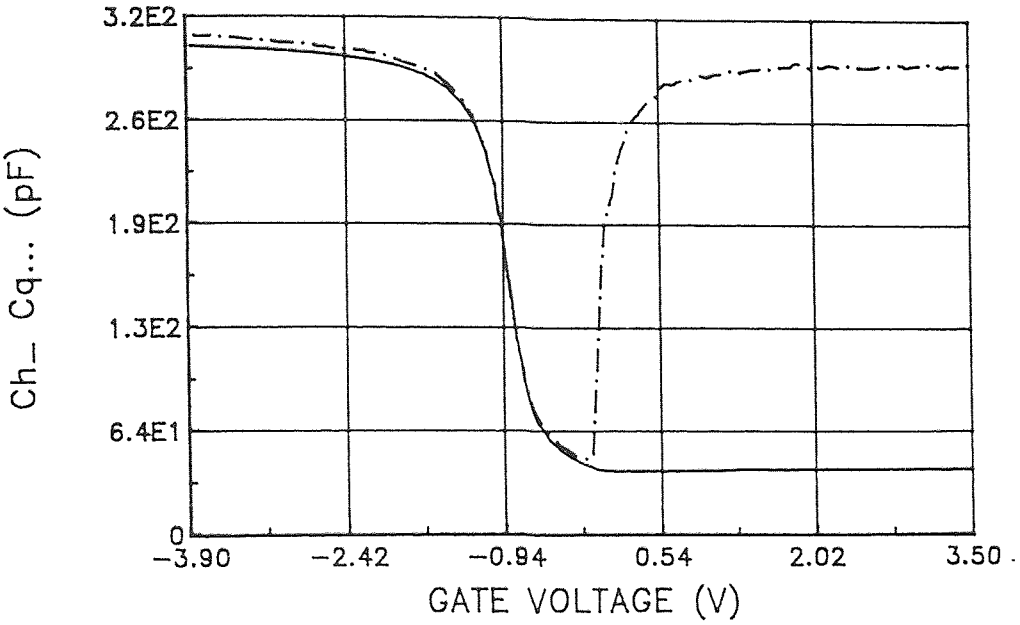


Figure A.1 HF CV and QS CV curves for type I device structure with t_{ox} = 22.1 nm (Control sample).

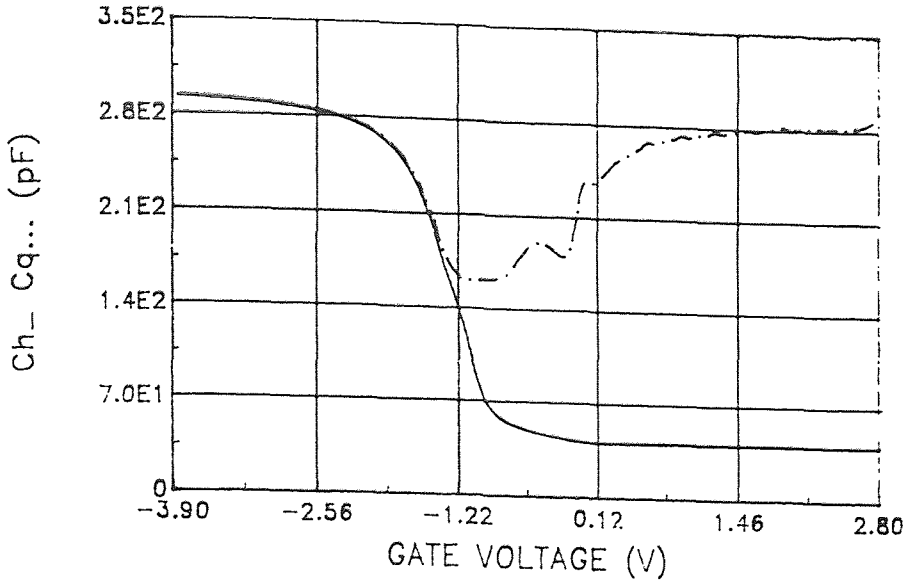


Figure A.2 HF CV and QS CV curves for type I device structure with t_{ox} = 23 nm (sample irradiated for 30 minutes).

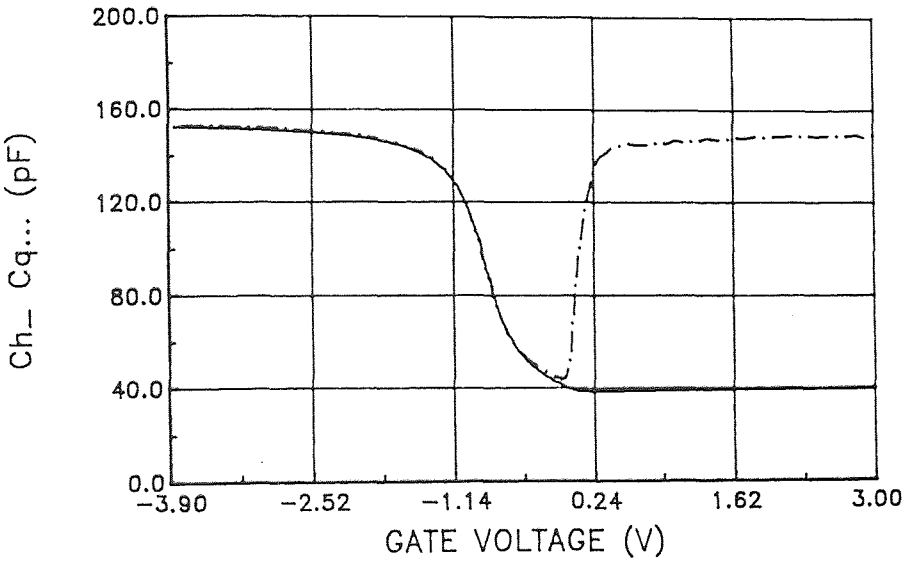


Figure A.3 HF CV and QS CV curves for type I device structure with t_{ox} = 43.8 nm (Control sample).

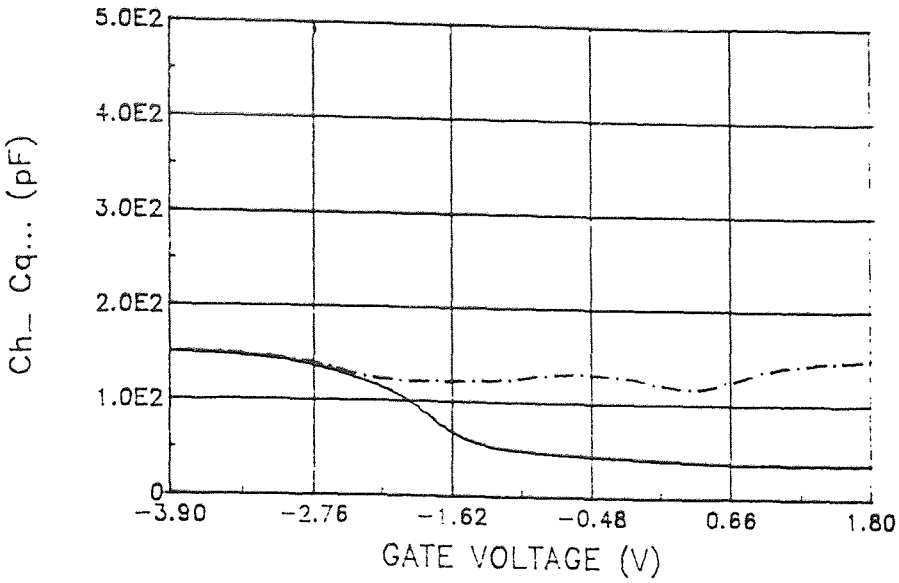


Figure A.4 HF CV and QS CV curves for type I device structure with t_{ox} = 42.9 nm (sample irradiated for 30 minutes).

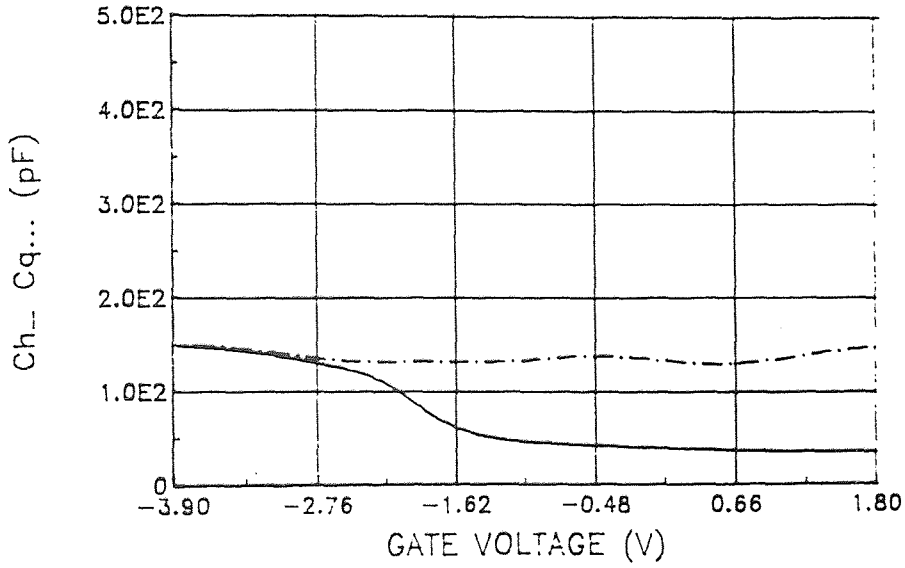


Figure A.5 HF CV and QS CV curves for type I device structure with t_{ox} = 45.3 nm (sample irradiated for 60 minutes).

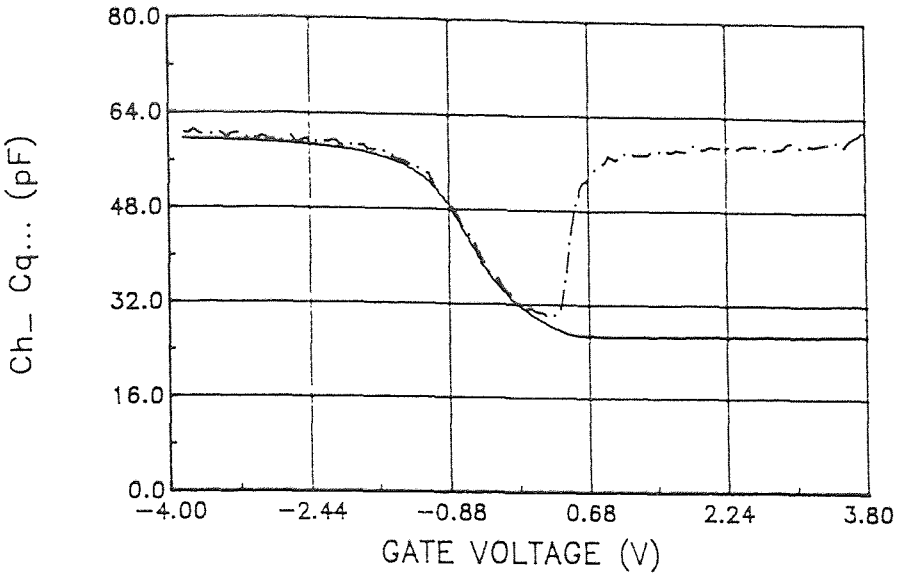


Figure A.6 HF CV and QS CV curves for type I device structure with t_{ox} = 111.8 nm (Control sample).

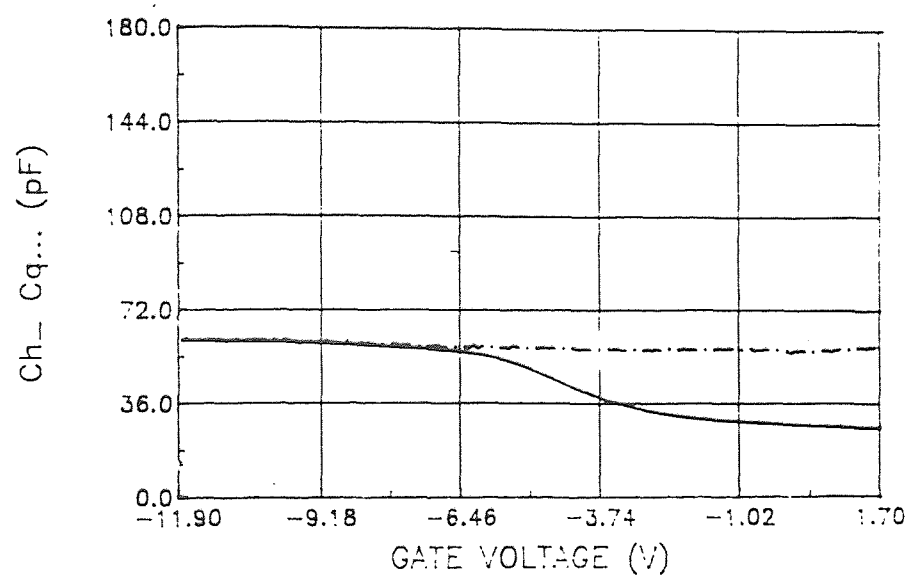


Figure A.7 HF CV and QS CV curves for type I device structure with t_{ox} = 112.3 nm (sample irradiated for 30 minutes).

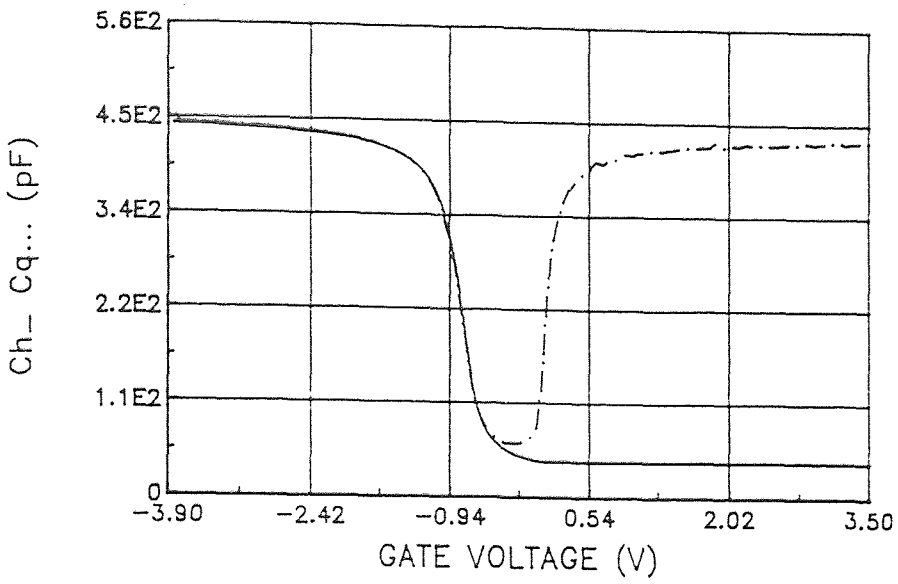


Figure A.8 HF CV and QS CV curves for type II device structure with t_{ox} = 15.1 nm (Control sample).

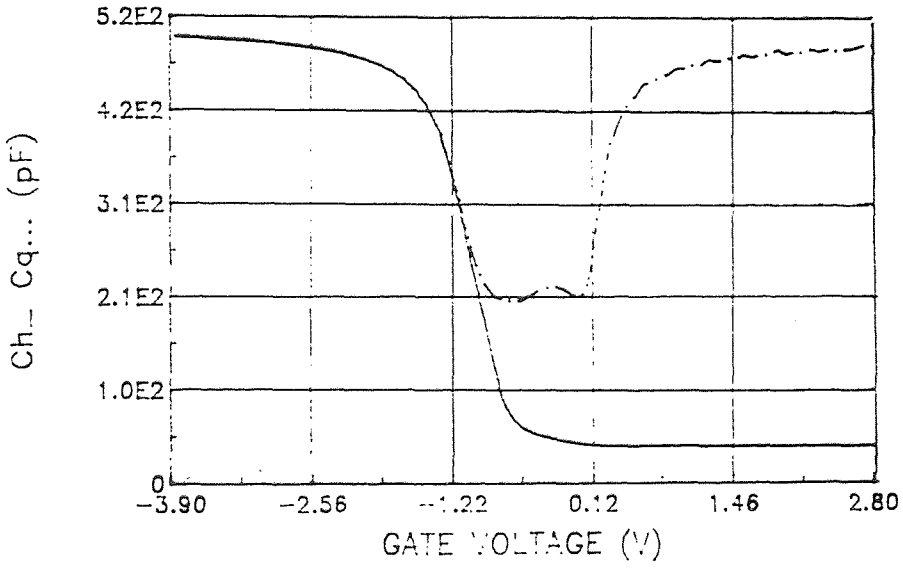


Figure A.9 HF CV and QS CV curves for type II device structure with t_{ox} = 14.5 nm (sample irradiated for 60 minutes).

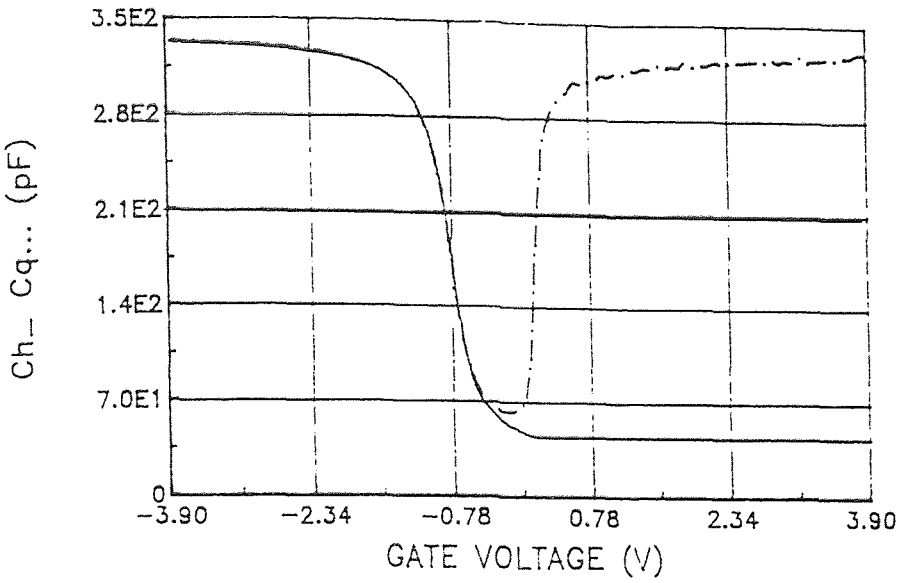


Figure A.10 HF CV and QS CV curves for type II device structure with t_{OX} = 20 nm (Control sample).

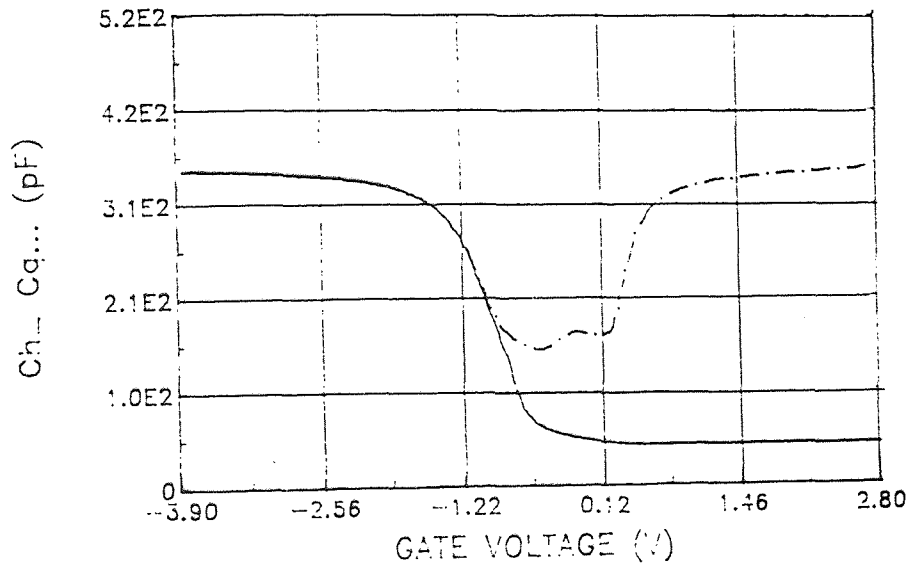


Figure A.11 HF CV and QS CV curves for type II device structure with t_{OX} = 19.3 nm (sample irradiated for 30 minutes).

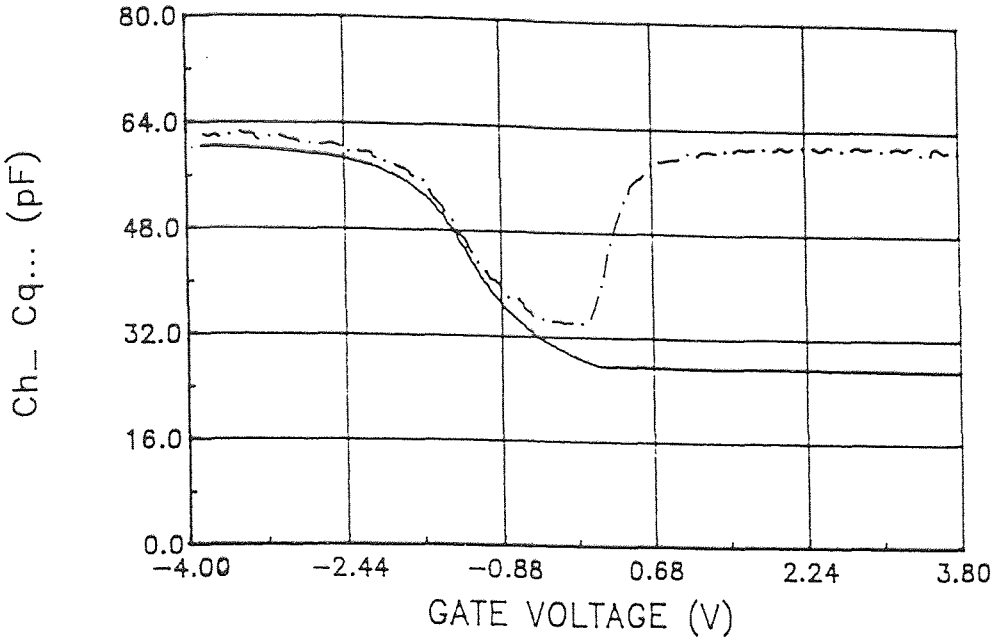


Figure A.12 HF CV and QS CV curves for type II device structure with t_{OX} = 110 nm (Control sample).

APPENDIX B

INTERFACE TRAP DENSITY (D_{it}) PLOTS

Here, Interface state density (D_{it}) plots for type I and type II device structures are included. The plots are for control samples for varying oxide thicknesses.

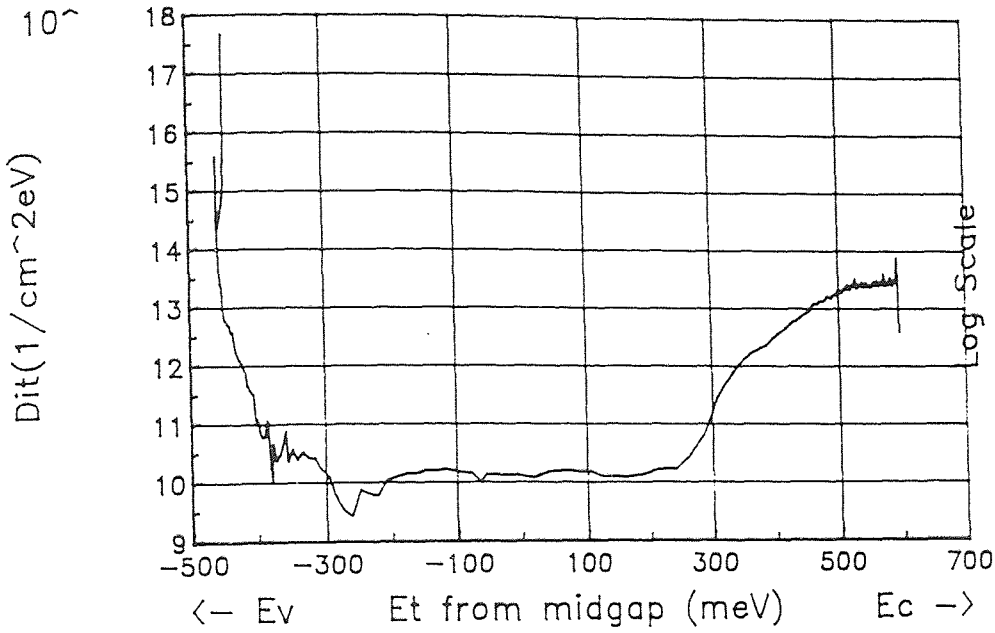


Figure B.1 D_{it} plot for type I device structure with t_{ox} = 22.1 nm (Control sample).

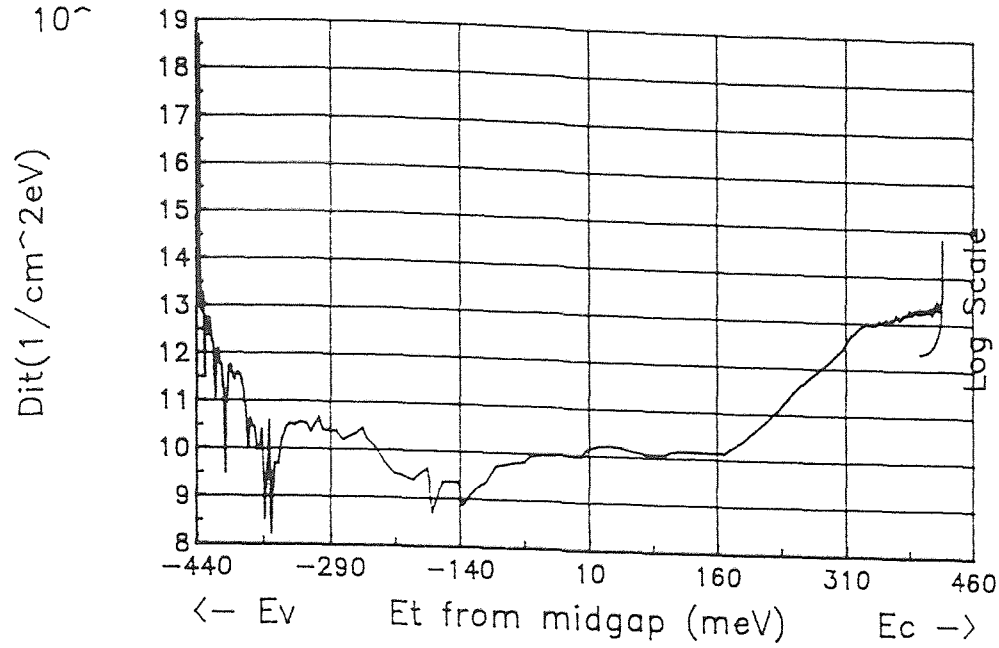


Figure B.2 D_{it} plot for type I device structure with t_{ox} = 43.8 nm (Control sample).

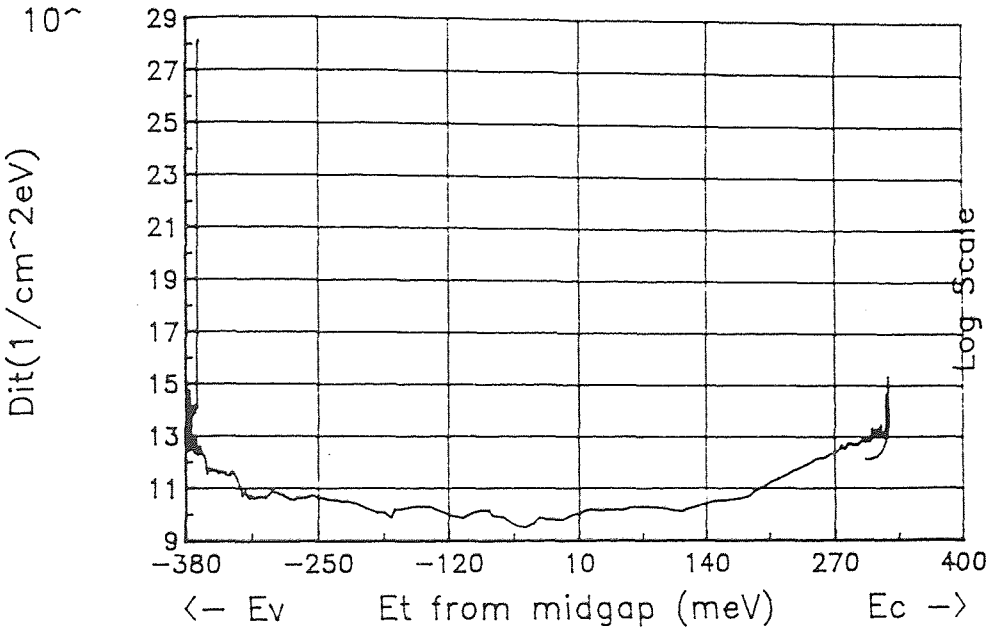


Figure B.3 D_{it} plot for type I device structure with t_{ox} = 111.8 nm (Control sample).

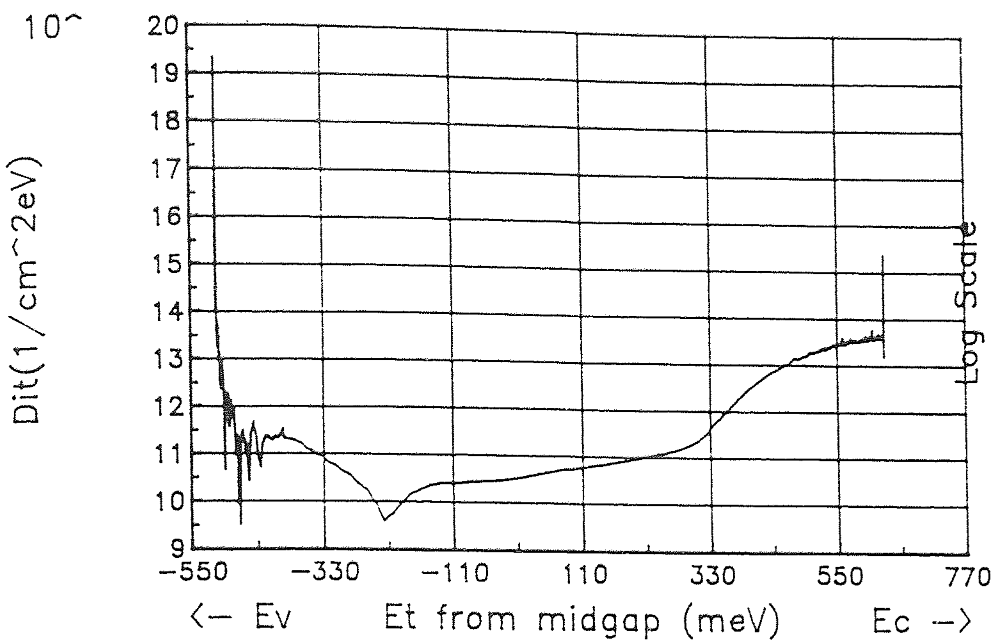


Figure B.4 D_{it} plot for type II device structure with t_{ox} = 17 nm (Control sample).

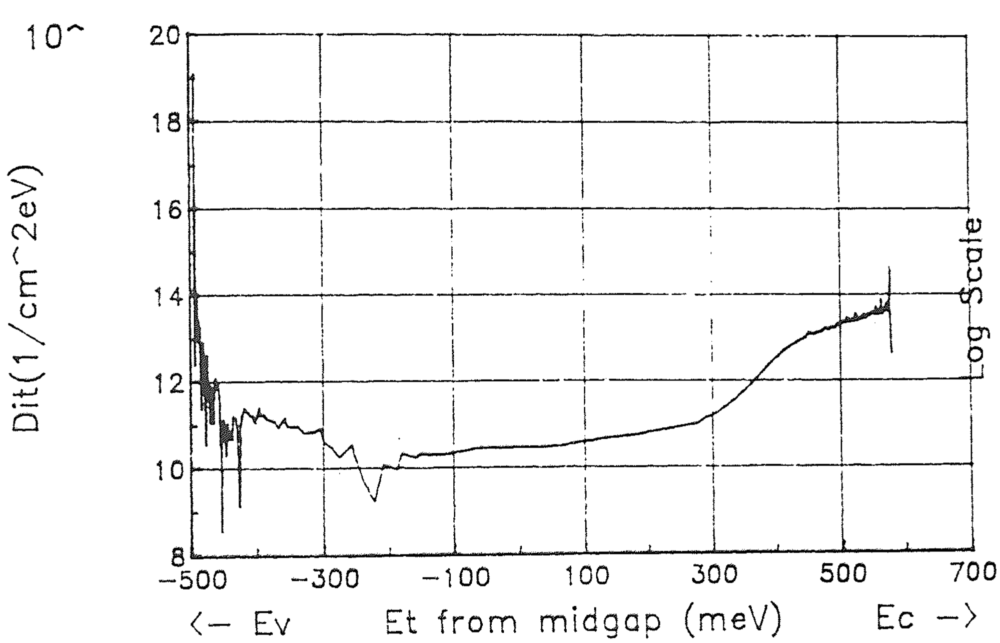


Figure B.5 D_{it} plot for type II device structure with t_{ox} = 21 nm (Control sample).

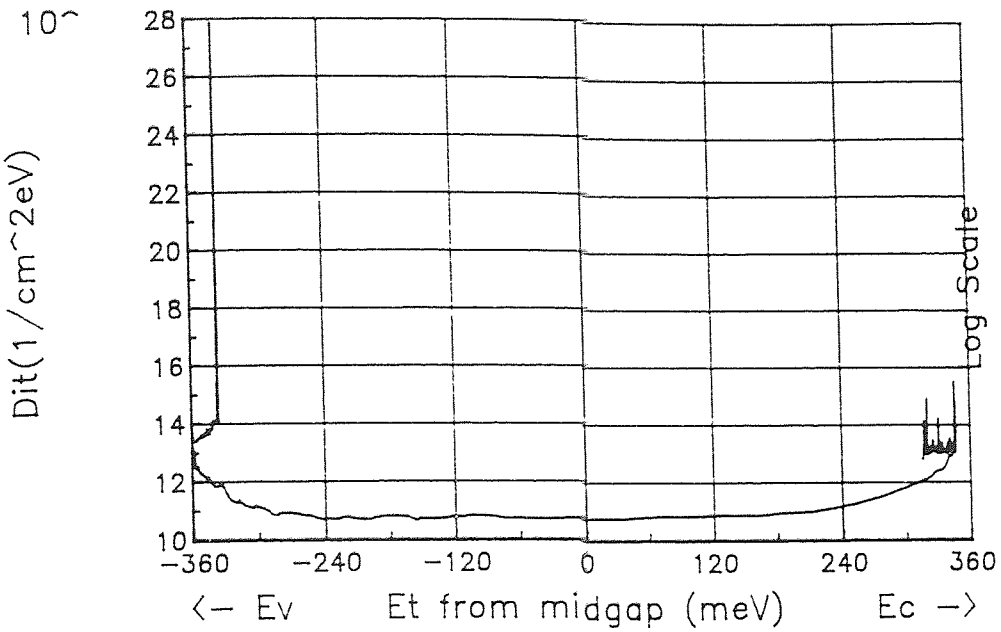


Figure B.6 D_{it} plot for type II device structure with t_{ox} = 110 nm (Control sample).

APPENDIX C

STATIC IV PLOTS

Here, static current voltage (IV) plots for type I and type II device structures for control and irradiated wafers are included. The plots also illustrate IV characteristics for varying oxide thicknesses.

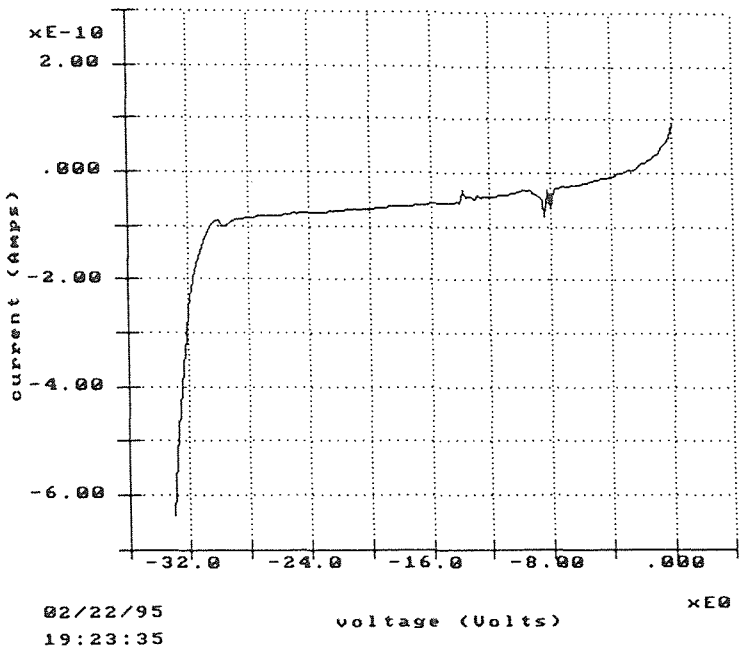


Figure C.1 Static IV plot for type I device structure with t_{ox} = 43 nm (Control sample).

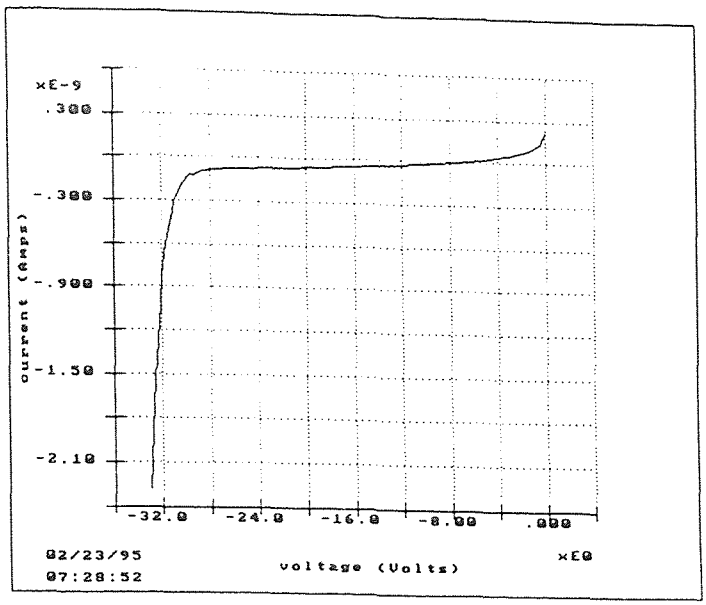


Figure C.2 Static IV plot for type I device structure with t_{ox} = 43 nm (sample irradiated for 15 minutes).

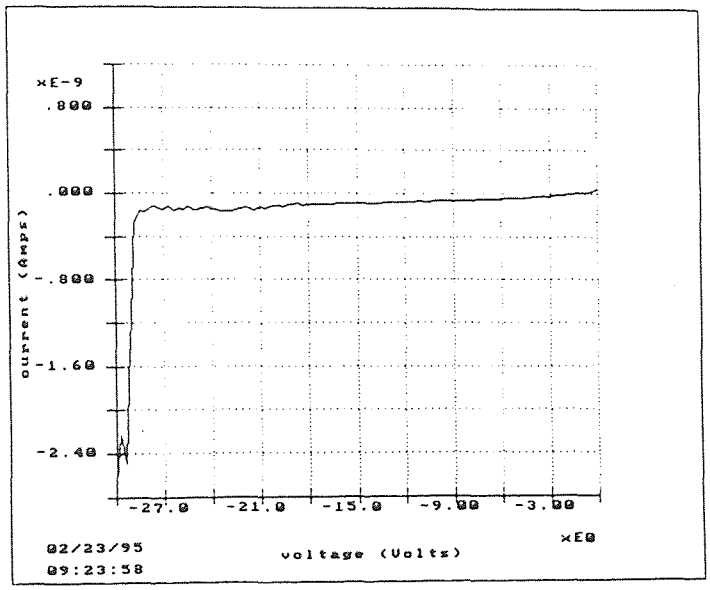


Figure C.3 Static IV plot for type I device structure with t_{ox} = 43 nm (sample irradiated for 45 minutes).

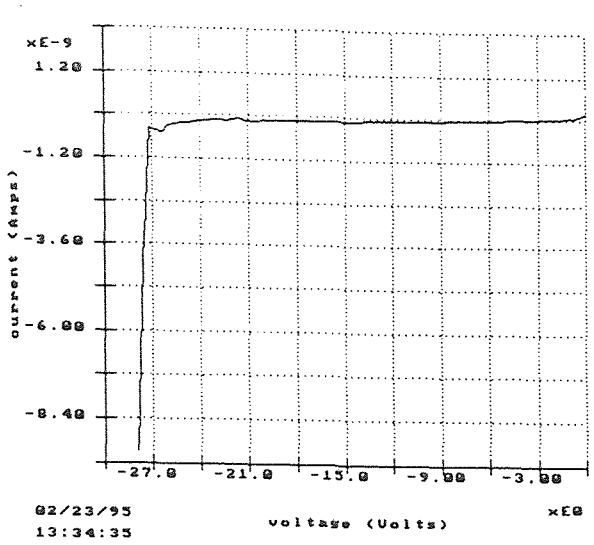


Figure C.4 Static IV plot for type I device structure with t_{OX} = 43 nm (sample irradiated for 90 minutes).

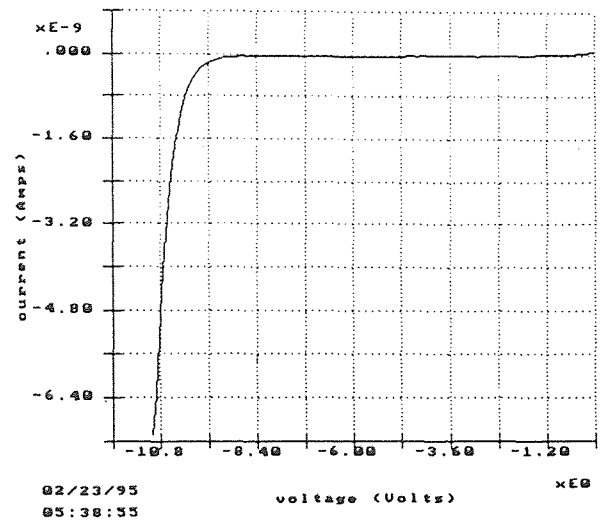


Figure C.5 Static IV plot for type II device structure with t_{OX} = 17 nm (sample irradiated for 15 minutes).

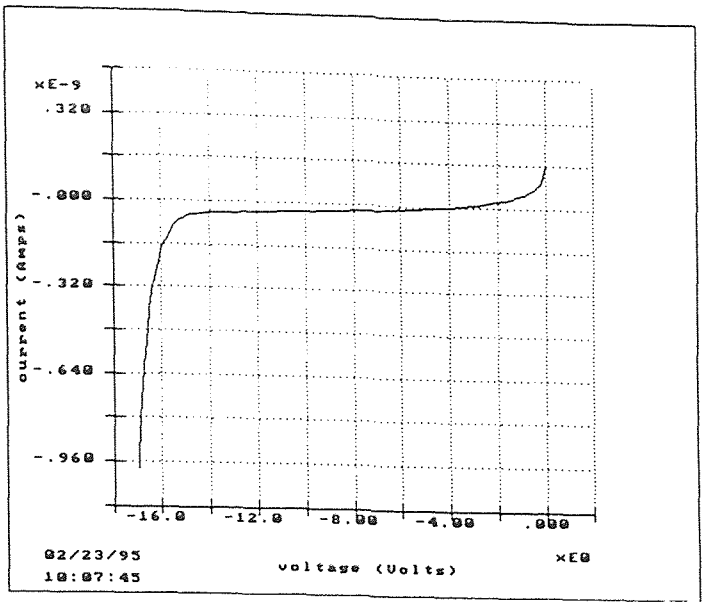


Figure C.6 Static IV plot for type II device structure with t_{OX} = 23 nm (sample irradiated for 45 minutes).

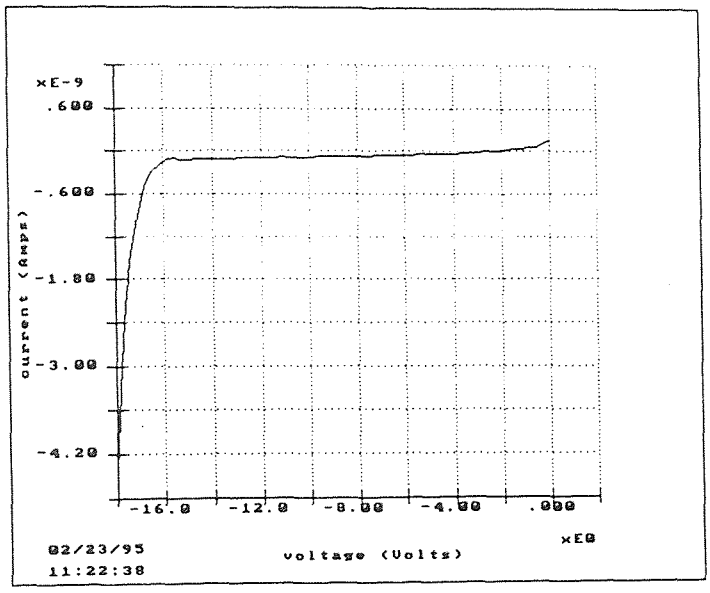


Figure C.7 Static IV plot for type II device structure with t_{OX} = 23 nm (sample irradiated for 75 minutes).

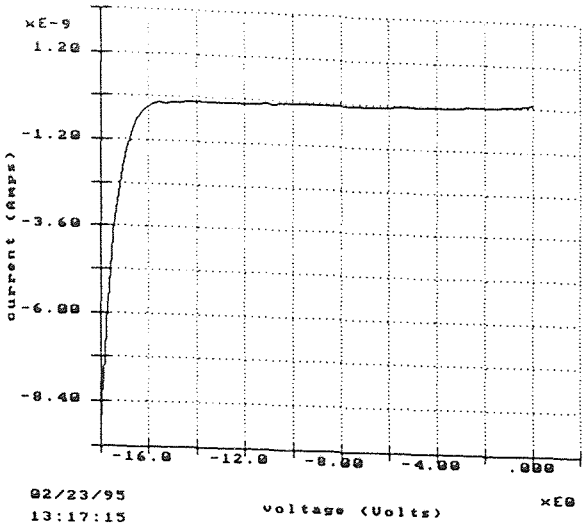


Figure C.8 Static IV plot for type II device structure with t_{OX} = 23 nm (sample irradiated for 90 minutes).

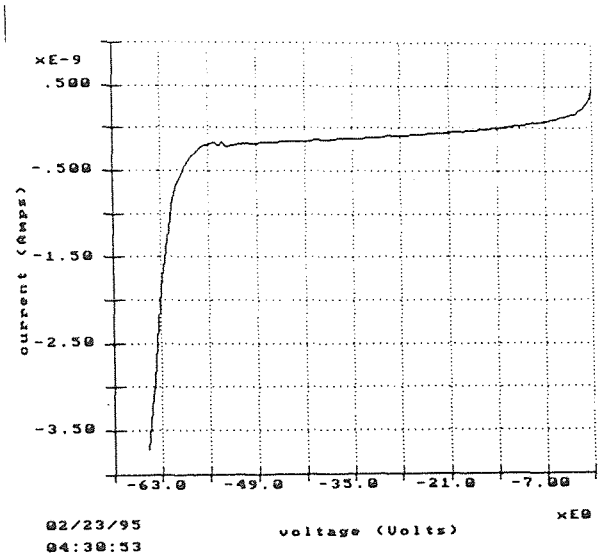


Figure C.9 Static IV plot for type II device structure with t_{OX} = 118 nm (Control sample).

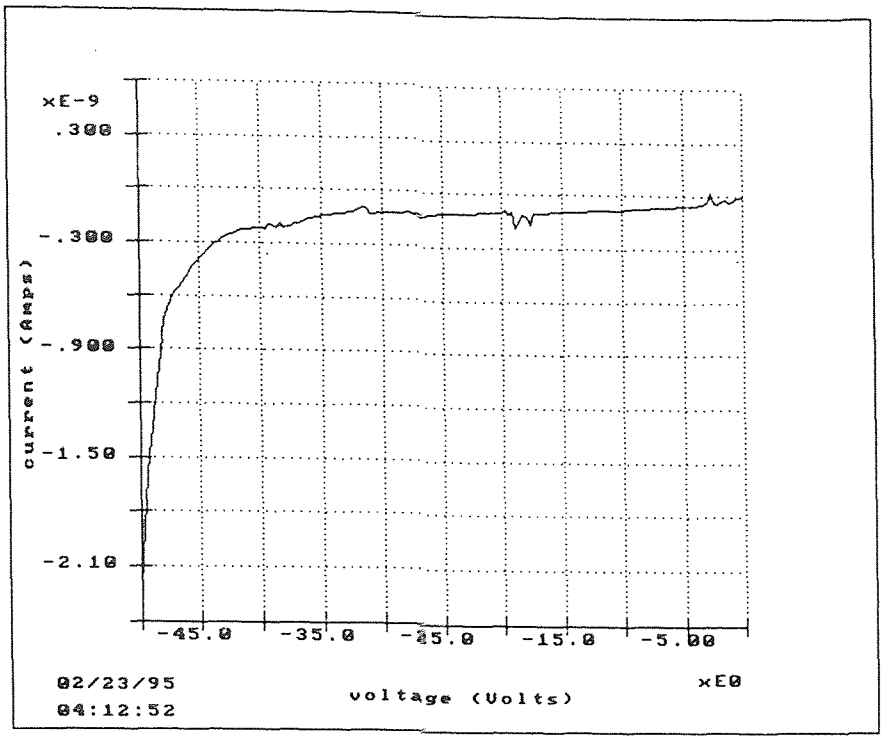


Figure C.10 Static IV plot for type II device structure with t_{ox} = 118 nm (sample irradiated for 45 minutes).

APPENDIX D

PROCESS SUMMARY

The MOS capacitors investigated in this study have been fabricated in the class 10 clean room at New Jersey Institute of Technology. The process details are summarized in the form of tables.

Table D.1 Gate1/LPCVD Polysilicon

SCRIBE ALL WAFERS 1. P-clean 5:1 H_2SO_4:H_2O_2 110°C 10 min
2. Rinse HOT DI 10 minutes
3. Rinse COLD DI 5 minutes
4. Spin dry
5. Furnace pre-clean 100:1 H_2O:HF 1 min
6. Rinse COLD DI 10 min
7. Spin dry
8. Dry Oxidation O_2 : 7.5 SLM Bubbler: 530 sccm Temp: 950°C Time: 00 min
9. Measure thickness of the oxide
10. Deposit LPCVD Poly SiH_4: 300 sccm Temp: 600°C Press: 400 mTorr Time: 2.5 hours
11. Measure (3250 Å target) Mean: 3188 Å Std. Dev: 11 Å

Table D.1 is a representative table for type I device structure for the thinnest (12 nm) oxide. The above process was followed for type I device structures and for type II device

structures, steps 10 and 11 of the above table were not performed, essentially because they had only an Al gate. Step 8 was performed at two temperatures: 950°C and 1050°C. Oxides of thicknesses 12 nm - 45 nm were grown at 950°C and oxide thicknesses in the range of 110 nm - 450 nm were grown at 1050°C. The time of dry oxidation for 12 nm, 20 nm and 45 nm has been 0 min, 10 min and 48 minutes respectively.

Table D.2 Poly doping for type I device structure

1. Strip backside oxide 7:1 BOE (no suds) 1 minute (backside hydrophobic)
2. Rinse COLD DI 10 minutes
3. Spin dry
4. P-clean 5:1 H_2SO_4:H_2O_2 110°C 10 minutes
5. Rinse HOT DI 10 minutes
6. Rinse COLD DI 5 minutes
7. Spin dry
8. Furnace pre-clean 100:1 H_2O:HF 1 minute
9. Rinse COLD DI 10 minutes
10. Spin dry
11. Phosphorus Diffusion / Drive-in Phosphorus Tube 950°C 1 hour
12. Strip oxide 10:1 H_2O:HF 2 minutes. (hydrophobic)
13. Rinse COLD DI 10 minutes
14. Spin dry
15. Measure sheet resistivity (25-30 ohms/square) 5 points/wafer

Table D.2 summarizes the process details for type I device structures for Poly doping.

Table D.3 Aluminum deposition

1. Furnace Pre-clean 100:1 H_2O : HF 30 seconds
2. Rinse COLD DI 5 minutes
3. Spin dry
4. Aluminum deposition: Base pressure: 8.0×10^{-7} torr Temperature: 300° C Dep. Rate 10 Å/sec Thickness: 5,000 Å.

Table D.3 summarizes the process details for Al deposition for type I and II device structures.

Table D.4 Photolithography - Metal

1. Apply Photoresist Program # 9 Shipley 3813
2. Align and expose Mask: DOT Time: 20 seconds
3. Develop Program #2
4. Inspect

Table D.4 summarizes the Photolithography process carried out on both type I and II device structures.

Table D.5 shown in the next page summarizes the wet etching of aluminum on both type I and II device structures.

Table D.5 Wet etch aluminum process

1. Hard bake PR 115°C 60 seconds Program #11
2. Wet etch Aluminum 40°C to completion plus 15 sec
3. Inspect Etched to completion ?
4. Strip PR M-pyrol 95°C 10 minutes PRIMARY 10 minutes SECONDARY
5. Rinse COLD DI 10 minutes
6. Spin dry
7. Inspect.

Table D.6 RIE - Polysilicon

1. Reactive Ion Etch Poly DRIE-100, Process #3 50 sccm SF_6 50 sccm Freon 115 150 m Torr 400 Watts 25°C Time: 3 minutes
2. Inspect Etched to completion?
3. Strip PR M-pyrol 95°C 10 minutes SECONDARY
4. Rinse COLD DI 5 minutes
5. Spin dry

Table D.6 summarizes the reactive ion etching of Polysilicon carried out on both type I and II device structures.

Table D.7 Aluminum (front side protect)

1. Apply PR Program #9 S3813 1KA
2. Strip backside oxide 7:1 BOE (no suds) 5 min (backside hydrophobic)
3. Rinse COLD DI 10 minutes
4. Spin dry
5. Strip PR M-pyrol 95°C 10 minutes PRIMARY 10 minutes SECONDARY
6. Rinse COLD DI 10 minutes
7. Spin dry

Table D.7 summarizes the process of depositing aluminum front side protect on both type I and II device structures.

Table D.8 Aluminum deposition (back side only)

1. M-Pyrol 95°C 10 minutes SECONDARY
2. Rinse COLD DI 10 minutes
3. Spin dry
4. Aluminum deposition: Base Pressure: 8.0×10^{-7} Temperature: 300°C Deposition Rate: 10 Å/sec Thickness: 5000 Å.

Table D.8 summarizes the aluminum deposition steps for backside contact for both type I and II device structures. After the above steps have been carried out , all the wafers are annealed at 400°C for thirty minutes.

APPENDIX E

NANOSPEC / AFT AUTOMATIC FILM THICKNESS MEASUREMENT SYSTEM

The NANOSPEC / AFT is a computerized film thickness measurement system. It includes a spectrophotometer head, which can measure in the wavelength range of 370 to 800 nm, using a computer controlled grating monochromator, photo multiplier tube detector and amplifier. The amplifier output is converted to a digital signal by the computer, which then calculates film thickness with one of several algorithms based on interference patterns. When the MEAS key is pressed, the spectrophotometer head scans from 480 to 800 nm, generating a corrected spectrum by computing a ratio to a bare silicon reference previously stored. The resulting spectral data are analyzed by the computer, which determines the exact film thickness corresponding to the interference pattern. The result is printed out in angstroms or microns.

Steps for measuring Silicon dioxide thickness on Si substrate:

1. Start at the Available Programs screen.
2. Enter program number 1.
3. Choose the objective lens.
4. Perform or bypass a new reference scan.
5. Make certain the objective lens is correct.
6. Enter the sample identification.
7. Enter the refractive index, if the refractive index option is enabled.
8. Locate, focus and take a measurement.

9. Accept or reject the measurement.

Repeat 8 and 9 for more measurements on the same sample or

10. Take a measurement with the same program on a new sample or

11. Select a new program.

APPENDIX F

OXIDE THICKNESS VERSUS TIME PLOTS

We include two plots here to give a comparative study of our wafers with the plots of standard process conditions found in the literature.

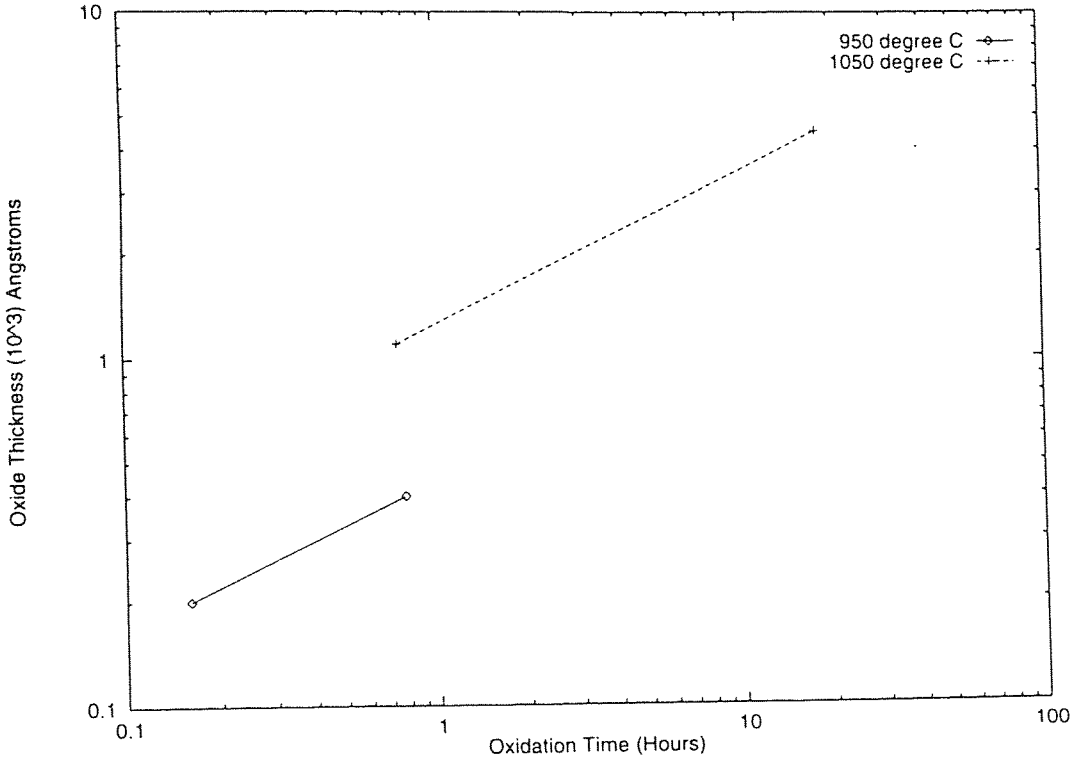


Figure F.1 Oxide thickness versus time (our study).

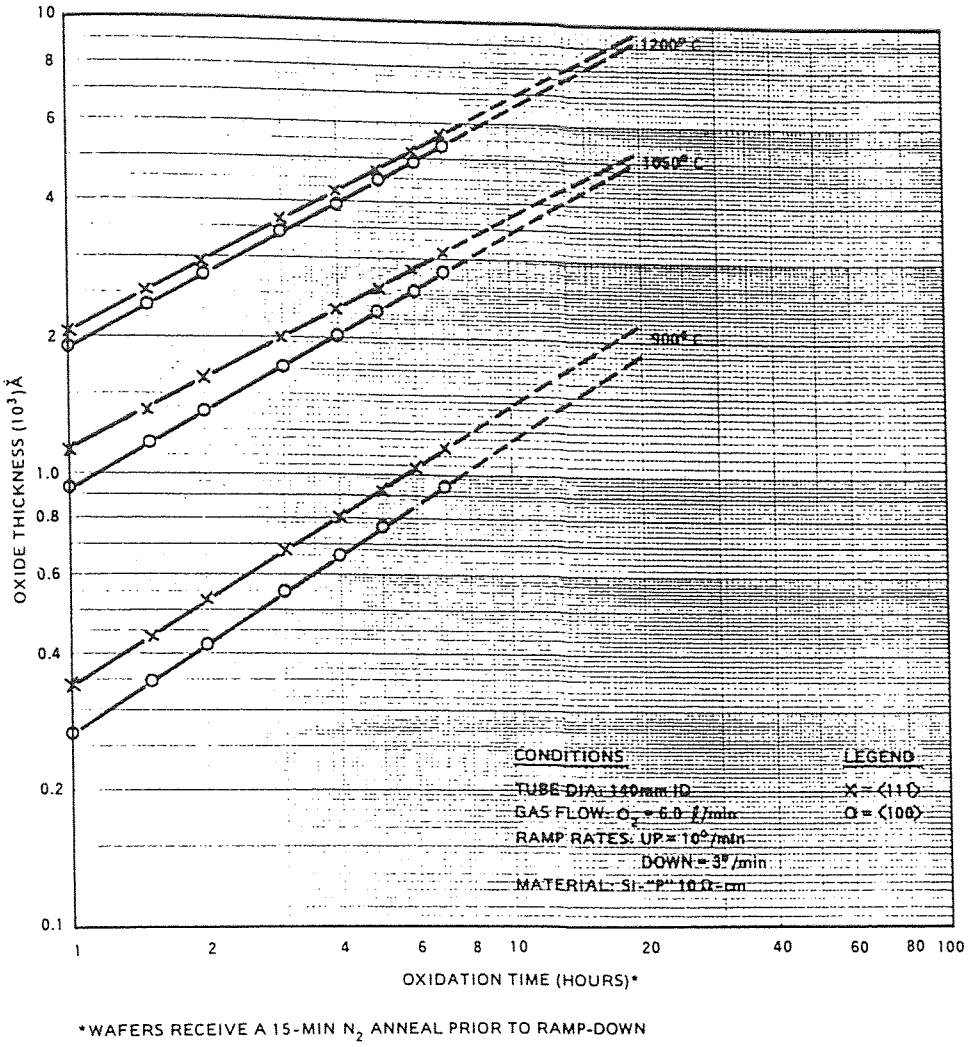


Figure F.2 Oxide thickness versus time found in literature [84].

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