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Design, simulation and fabrication of a mems in-situ contactless sensor to detect plasma induced damage during reactive ion etching

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ABSTRACT

DESIGN, SIMULATION AND FABRICATION OF A MEMS IN-SITU, CONTACTLESS SENSOR TO DETECT PLASMA INDUCED DAMAGE DURING REACTIVE ION ETCHING

by
Subramanian Ganesh

The present trend in the semiconductor industry is towards submicron devices. An inevitable process technique in achieving this is by reactive ion etching of the polysilicon gate. During RIE, the gate oxide may get damaged due to several causes. One of the main causes of the damage is the non-uniformity of the plasma. It is reported that these plasma inconsistencies are mainly due to electrode design and that they create spatial plasma potential fluctuation. These fluctuations are reported to be in the range of 10-20 Volts. By providing an in-situ monitoring of the wafers, the reliability of the device could be established. The purpose of this sensor is to detect the spatial fluctuations. It works on the principle of electrostatic forces. It is made of polysilicon (gate material) and consists of two cantilevers separated by 2μm constituting a parallel plate capacitor configuration. The design, simulation and fabrication of the sensor was carried out. The test results demonstrated that sensors with beam lengths 150μm, 200μm and 250μm deflect by 2μm at externally applied voltages of 65, 56, and 50 volts respectively. Optimized beam dimensions that would deflect by 1.2μm at an applied voltage of 20 Volts is estimated from the experimental results and has the following dimensions: length of the cantilever = 200μm, width = 2μm , the thickness = 1.6μm , and the space between the cantilevers is = 1.2μm.

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by
Subramanian Ganesh

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APROVAL PAGE

DESIGN, SIMULATION AND FABRICATION OF A MEMS IN-SITU, CONTACTLESS SENSOR TO DETECT PLASMA INDUCED DAMAGE DURING REACTIVE ION ETCHING

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To my Parents and Rashmi

"The unreal never is: the Real never is not. This truth indeed has been seen by those who can see the true"

Rig-

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CHAPTER 1

INTRODUCTION

1.1 Overview

The need for large throughput, high resolution and low cost turn the attention of semiconductor manufacturers to the reactive plasma processes. Although there has been a lot of work done in plasma processing, full monitoring of the process, especially in the area of device damage is still lacking. The present trend in the industry is towards submicron devices. As the devices get reduced in size the thickness of gate oxide is also reduced. RIE plays an important role in the definition of small dimensions. This furthers the need for a more accurate and controllable system to be installed, especially in the area of reactive ion etching.

1.1.1 Device Damage from the Plasma

Wafers in a plasma are exposed to energetic particles and photon bombardment. This radiation consists of ions, electrons, ultraviolet photons and soft x-rays. While most ions bombard the surface with energies below a few tens of volts, ion energy on the 'tail' of the distribution can be more than 1000 Volts [1], depending on the sheath potential. Average electron energy in the plasma ranges from a few volts to 10V or more[1], but electrons reaching the walls are thought to have lower energy owing to the plasma potential. When

high energy radiation strikes the wafer surface, it can cause both shallow and deep surface disruption (damage), which alters electrical characteristics and degrades device performance. Both reversible and irreversible device damage can occur. In general the significance of these effects increase with particle energy, and hence with peak RF potential and power. Damage occurs in various forms, atomic displacements caused by ion impact, which have been observed upto 150 A^0 deep [1], electron hole pairs produced by primary ionization from the UV and X-ray photons, and secondary ionization where electrons formed by primary processes create defect centers. The damage can usually be detected by a change in the capacitance-voltage (CV) signature of the MOS capacitors, or in the operating parameters of simple transistor structure, which give threshold voltage, flatband voltage, Q_{SS}, lifetime and other parameters.

1.1.1.1 Reversible Effects: Every plasma process causes surface alteration because of the energetic radiation present in the plasma, and almost any plasma causes some change in measured device parameters. If these changes were always irreversible, it would be hard to make useful semiconductor devices with plasma processing. Miniaturization would have been limited, since plasma processing is essential for fabricating devices with small critical dimensions. Fortunately, much of this radiation can be removed by thermal annealing.

Device damage from UV photons can be removed by a thermal anneal at 350°C [1] (to the point that the original electrical parameters determined by CV measurements are restored). High energy ion bombardment damage, on the other hand is generally

removed by annealing at 650°C [1], while severe x-ray damage is rare, because the sheath and bias potentials in most plasma processes are too low to produce an appreciable x-ray flux. In those cases where x-rays are a problem, changing some metallic parts of the reactor to insulating materials can eliminate x-ray production. Since most device fabrication schedules include thermal cycling to at least 700-900° C after the critical gate levels, much damage from plasma processing is removed naturally, without any special processing.

However, new device designs include shallow junctions, which cannot tolerate high temperature at all. Hence, high energy ion damage is becoming more of a problem. Difficulties also arise with thin gate insulators (<150 A°) that must have extremely good material characteristics for reliable performance. Here the x-ray flux must be reduced to an absolute minimum, so the use of metallic reactor surfaces is minimized and low potentials are used. Remote plasma systems (plasma transport reactors) and magnetron reactors offer a less energetic ion flux and have found increasing use in these applications.

1.1.1.2 Irreversible Effects: Unfortunately, two "killer" effects that can occur in plasma are not reversible. The first of the these is contamination during critical operations such as window and/or via-step etching. If polymer formed by the plasma itself, or foreign materials such as dirt or sputtered reactor material, enters an open contact, it will be covered later by metallization. The result is unexpected doping or an unwanted resistance,

which cannot be corrected. Hence control of reaction products from the plasma chemistry, particularly polymeric products, is essential.

A second, more subtle, source of irreversible damage is electrostatic breakdown of the thin insulating films caused by charge that is deposited during the plasma process cycle. The gate insulator film in many state-of-the-art device structures are becoming extremely thin. (150-250A°). While a high quality silicon dioxide film can withstand about 12-15MV/cm [1] for short periods, this amounts to only 10-15 volts across a 100A thick SiO_2 gate dielectric. Beyond this point there is a catastrophic breakdown, and no way to repair the film.

The mechanism of plasma induced breakdown is illustrated in figure 1.1

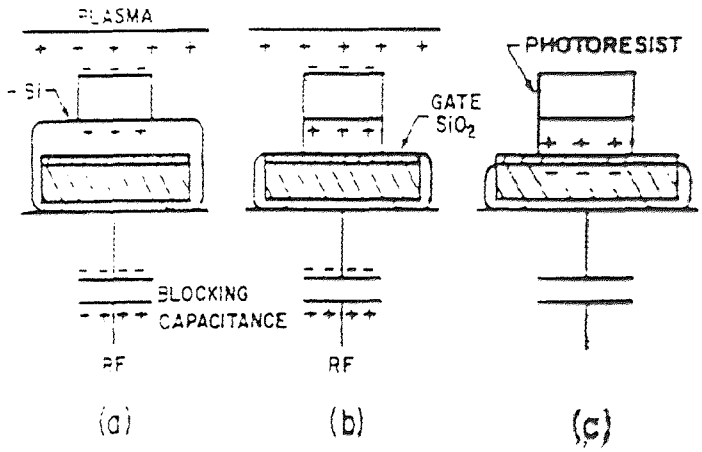

Figure 1.1 Electrostatic breakdown of gate oxide

Fig 1.1a shows a patterned polysilicon-coated wafer placed on the "cathode". When the plasma is turned on, the conductive poly which wraps around the wafer edge shields the gate dielectric and transfers the charge to the electrode and blocking capacitor.

Fig 1.1 b. The poly is patterned and the front to back conductive path is broken.

Fig 1.1c. Charge deposited during the plasma turn-off transient is trapped on the front oxide surface with mirror change below.

If the electric field generated by this charge exceeds breakdown, the thin oxide dielectric will be mechanically disrupted.

A film of conductive polysilicon was deposited over thin gate oxide (SiO_2) and covered with a photoresist mask pattern. The wafer is then placed in a plasma to transfer the mask pattern into the polysilicon film. At the point depicted in Fig 1.1a the plasma has just been struck. As the sheath is established, the smaller electrode (cathode) is negatively charged by electrons until, at a steady state, there are equal fluxes of electrons and ions. Initially, the conductive polysilicon film extends around the wafer and forms a continuous electrical circuit from the front to the electrode underneath. Hence the negative electrode potential appears across the "blocking" capacitance, which is a part of the power supply or matching network. If the plasma were turned off at this point, there would be a transient flow of charge to the wafer and surrounding surface, but this charge would induce no potential across the gate because it is still surrounded by the conducting polysilicon layer. As the mask pattern is etched into the polysilicon, the conductive path at the edge of the wafer is finally broken (Fig 1.1b), and the gate electrode is isolated. Still, at this point, there is little or no potential difference between the gate electrode and substrate below because there was electrostatic equilibrium when the path was broken.

When etching is finished and the plasma is turned off, however, positive ions from the decaying plasma will deposit small amounts of charge on the resist and gate electrode. Meanwhile, the wafer substrate is maintained at the reactor electrode potential. Since the gate oxide dielectric is thin, the charge that collects can induce high transient fields across the gate and cause breakdown. Free charge reaching the reactor electrode

during this transient has little effect on its potential because of the large capacitance to ground through the blocking capacitor and stray coupling.

By contrast, if the wafer is placed on an insulating surface, substrate potential is not held at that of the large electrode and there is less danger of breakdown. In this case, voltage from the turnoff transient will be divided between the gate capacitance and the wafer/insulator/electrode capacitor. Clearly, plasma operation should be characterized with test devices to insure that transient potentials are kept well below the level that produces the electrostatic breakdown.

During photoresist stripping a similar condition can occur. Wafers are put into barrel etchers where the resist collects charge as it approaches the floating point potential of the plasma. For a typical oxygen plasma used for stripping photresist, the floating potential is about -5V. If electrical transients in the system during the resist strip cycle suddenly increase the floating point potential, electrically isolated areas can charge at different rates (because of the geometrical arrangement of wafers with respect to the plasma in the reactor) so that breakdown potential of thin insulators (12-15Vdc) is exceeded.

Another experiment further illustrates these phenomena. Capacitors with 100A [1] dielectrics fabricated on wafers were tested to determine the Fowler-Nordheim tunneling current through the capacitors as a function of impressed voltage. These wafers were divided into two groups with one group loaded into metal support "boats" and the other into quartz boats. Both boats were placed in the commercial resist strip system in which wafer boats are held on a grounded metal support system within a metal reactor chamber.

After resist stripping, the capacitors were tested a second time. Wafers in the quartz were unaffected by the stripping cycle. Tunneling current through almost half the capacitors in the metal boat group, on the other hand, increased from 5-50nA with about a 10V potential difference, to 1-50mA after the strip cycle, a level indicating a device failure (end-of-life is a tunneling current above 1μA).

The results are simply explained. In order for breakdown to occur, a potential difference must exist across the film. Since both sides of the wafers reached the same floating potential in the quartz boat, there was no potential difference. By contrast, the capacitor electrodes connected to the substrate in the metal boat were maintained at a ground potential so that transients in the floating potential during stripping were imposed across the SiO_2 film [1].

One aspect of the plasma process is the uniformity of plasma which requires precise monitoring. It is believed that during polysilicon gate etching the damage to oxide occurs mainly due to plasma non-uniformity [2]. Plasma nonuniformity produces electron and ion current that do not balance locally and can generate oxide damage. There are three main current components at the surface of a wafer placed in an rf plasma. While at 13.56 Mhz the largest is the rf displacement current, this is usualy of secondary importance in surface charging because of the low impedence presented by the oxide. Next there is positive ion flux that is responsible for anisotropic etching. The flux average is nearly constant with time and depends linearly on the local plasma density. The final component, electron flux, flows briefly in every rf cycle to balance the ions lost from the central plasma region. In a uniform plasma, the ion and electron conduction currents

locally balance each other over the rf cycle. Charging is not a problem and the surface potential stays close to that of the substrate.

The situation for a nonuniform plasma differs significantly. Ion and electron currents do not have to balance locally through the rf cycle, although there must be a net balance over the electrode as a whole (refer figure 1.3). Where excess ion current occurs, the imbalance (e.g., net current flux to the wafer) causes wafer surface charging and results in increased voltage across the sheath. The charge build up continues until the currents balance or the oxide begins to conduct. The plasma inconsistencies are mainly due to electrode design which create spatial plasma potential fluctuation. The spatial plasma potential fluctuations are observed in the range of 10-20 Volts [2]. This voltage fluctuation charges the wafer surface. The capacitive coupling of contact pads and the conductors on the wafer surface can develop plasma nonuniformity and thereby create high charging effects in the oxide. The intensity of oxide charging is determined by the net local current imbalance (voltage fluctuation) and area of the gate polysilicon after the end point is reached. Before endpoint the imbalanced current normally flows through the conducting polysilicon film [12]. Because of this current imbalance the oxide goes through nonuniform current stresses that can lead to the oxide failure or initiate degradation (charging) that may cause oxide failure at a later time.

1.2 Objective

A sensor could be fabricated using existing surface micromachining techniques so as to provide manufacturers of VLSI circuits with an in-situ, non-destructive contactless

evaluation, which enables accurate monitoring of the semiconductor wafers undergoing reactive ion etching (RIE). This thesis deals with the operating principle, design, simulation, fabrication and characterization of such a sensor that could detect charging damage caused during reactive ion etching of polysilicon and other films.

In this chapter a general idea of the device principle, material selection, and design considerations is detailed. The second chapter deals with the device modeling and simulation [5,6]. Electrostatic equations and structural bending of beam equations are used to simulate the device [14-20]. The third chapter gives the detailed fabrication and process flow used [13]. The fourth chapter details the testing procedures and methodology followed. The fifth chapter deals with the results obtained from the characterization of the beams and a comparison drawn between the simulation and the actual results obtained. It also deals with the practical limitations of the device and any potential problems that might be expected to encounter during actual application.

1.3 Principle of Operation

It is well known that plasma induced damage causes a spatial voltage to develop in the chamber which leads to a charge build up. The proposed design consists of a set of parallel cantilevers made of Polysilicon. These cantilevers are individually integrated with an antenna structure. These antenna structures support a large surface area so as to sense this charge. The charge thus accumulated by the antenna structure are transferred over the entire length of the polysilicon cantilever. Once there exsists a potential a

potential difference between the pair of cantilevers and as the cantilevers are in close proximity they deflect in accordance with the type of charge accumulated (like charges or unlike charges) during the plasma etching process (Refer figure 1.2).

The cantilevers can be modeled using the analogy of a parallel plate configuration. The capacitance developed in the cantilevers, the induced force and the deflection can be calculated using this analogy. Therefore, the force that drives these set of cantilevers is the electrostatic force, generated as and when the cantilevers are charged.

1.4 Material Selection

This sensor is to be integrated on the wafer on which transistors are fabricated. The standard CMOS process flow includes an oxide deposition and polysilicon deposition to form the gate. A small area on the mask plate that is used to define the polysilicon gate is reserved for the sensor. At all other process steps like well formation, implantation etc. the sensor area is covered with photoresist. This will protect the sensor.

The sensors are constructed during the RIE of polysilicon. Consequently the material of the cantilever was chosen as Polysilicon. Polysilicon is a strong material with a modulus of elasticity of 1.9×10^{11} N/m^2

Highly doped polysilicon acts as a good conductor. To calculate capacitance and electrostatic force, it is assumed that the plates are good conductors and this is necessary as good conductors aid in charge transfer over the plate area in a uniform manner. Hence polysilicon was chosen.

Some of the mechanical properties of Polysilicon are given in the table below.

Table 1.1 Mechanical properties of Polysilicon [3]

Mechanical Property	Value
Yield Strength	$7*10^{10}$ dyne/cm^2
Knoop Hardness	850 Kg/mm^2
Young's Modulus	1.9×10^{11} N/m^2
Density	2.3 g/cm^3

1.5 Design Considerations

In standard CMOS process the standard dimension for the thickness of polysilicon is 0.3 - 0.5μ. The cantilevers are to deflect in a horizontal plane where the width to thickness ratio (aspect ratio) needs to be minimized in order to achieve a larger deflection for a particular voltage. A minimum of 2μ width was chosen due to fabrication constraints. With the width and the thickness dimensions fixed the only available parameter is the length. There are eight sets of cantilevers fabricated, with the width of each ranging from 2μ to 3μ and the thickness 1.5μm . The length of the cantilever vary from 50μm to 250μm in steps of 50μm. Some of the design considerations are based on fabrications limitations and others are based on the simulated values. Cantilevers with varying dimensions of length, width and distance between them are selected in order to get a range of working values. A length of 250μ was selected as the upper limit because a cantilevers with greater length would add significantly to sag. This would cause the

parallality to be lost in the horizontal plane. On the other hand a cantilevers with length less than 50μ would significantly reduce appreciable deflection.

The top view of the proposed structure is shown in figure 1.2

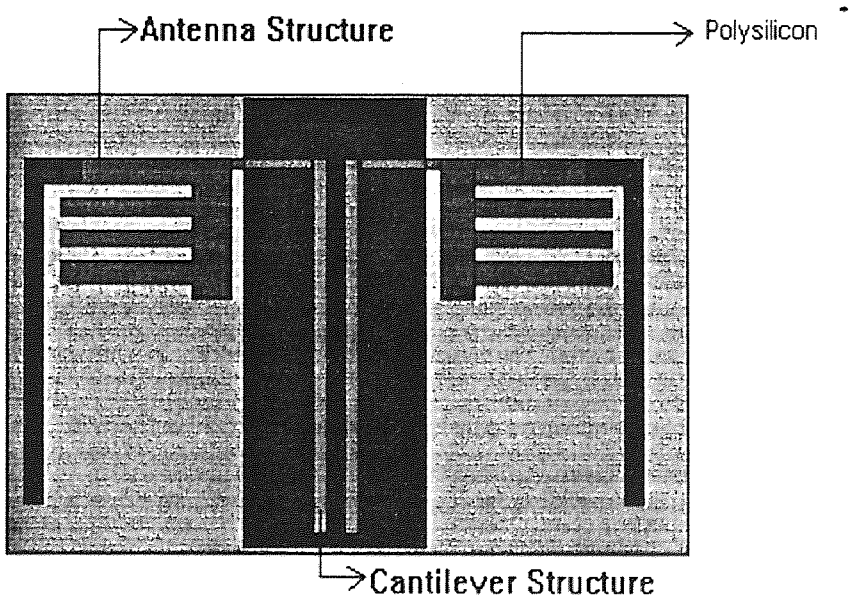

Figure 1.2 Top view of the sensor

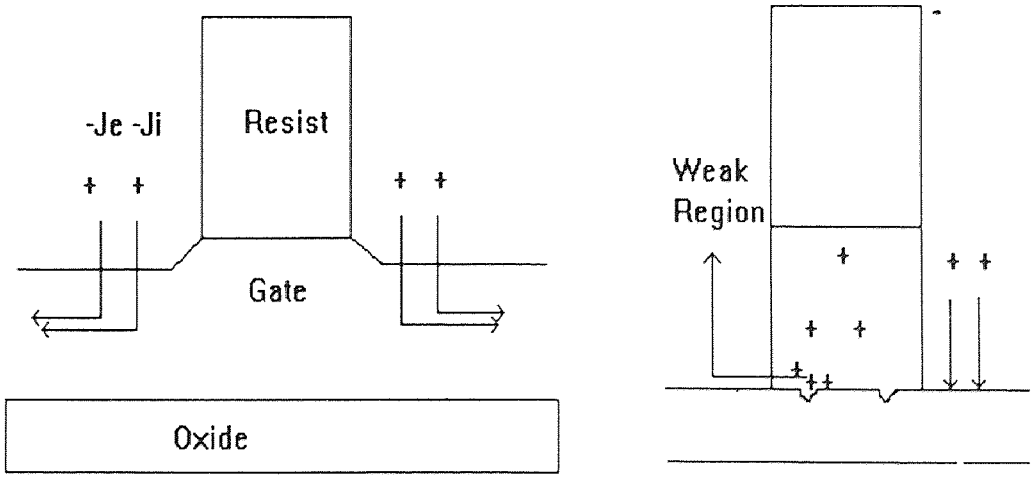

Figure 1.3 Gate oxide damage during etching of the conductive gate electrode

CHAPTER 2

SIMULATION

2.1 Introduction

As explained earlier the sensor works on the electrostatic principle. The basic force that is needed to deflect the cantilevers is obtained from the charges that get accumulated in each individual polysilicon cantilever beam that is isolated from the environment by the gate oxide.

The principle of operation, the dimensional parameters of the beams and the charge build up, force and deflection achievable is detailed. We know that the voltage that is generated in the plasma chamber will be in the range of 10-20 Volts [1,2]. Keeping this in mind simulation is done so as to arrive at a value of beam dimensions that will be able to function in the specified voltage range.

2.2 Basic Electrostatics

The simulation methodology is outlined.

i. The capacitance that is developed when a particular voltage is applied is calculated.

ii. The electrostatic force generated owing to this capacitance is calculated. This is explained in the sub-section Device Simulation.

iii. Deflection achieved is calculated considering parallel plates of cantilever nature (that is free at one end and fixed at the other) This is also outlined in the sub-section Device Simulation.

There are many methods to calculate the capacitance. A few of the approaches are detailed below.

A) By definition of capacitance

$$Q = CV \tag{2.1}$$

where: 'Q' is the charge accumulated,

'C' is the capacitance,

'V' is the impressed voltage.

B) Assuming that the plates are semi-infinite, then

$$C = \varepsilon A/H = \varepsilon WL/H \tag{2.2}$$

where: 'ε' is the dielectric constant of air,

'A' is the effective area of the plates,

'H' the distance between the plates (Refer figure 2.2).

$$C) I = dQ/dT = C\, dV/dT + V\, dC/dT \text{ [4]} \tag{2.3}$$

where I= Transient current. (Refer figure 2.1)

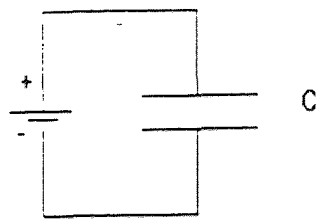

Figure 2.1 Simple schematic showing application of voltage and capacitance build up

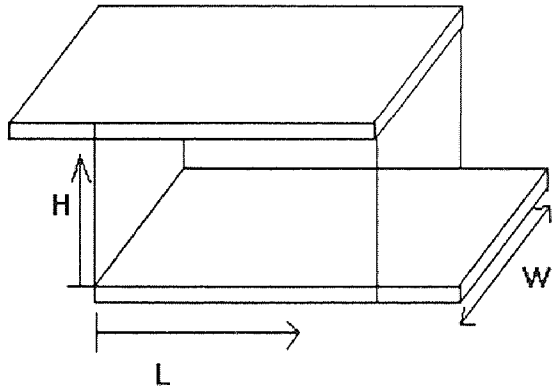

Figure 2.2 Parallel plates with width W, length L and H the distance between the plates

D) The simulation of parallel plate contributions to the capacitance is done. Also the capacitance due to fringing electric fields also constitutes a major contribution to the capacitance of narrow plates. For a 2μ process the fringing capacitance of a poly wire can be as high as the parallel capacitance [5].

The capacitance between a conducting wire and a ground plane or another wire is determined by solving the Laplace's equation. Rather than solve this electric field problem, we will examine two special cases that have well known solutions. The first special case is that of a parallel plate capacitor. The capacitance is

$$C_{plate} = \varepsilon WL/H \qquad (2.4)$$

The capacitance depends linearly on the area WL and the dielectric constant ε, and inversely on the distance H between the two plates. C_{plate} closely approximates the true capacitance when W, L >> H.

The second special case occurs for narrow wires; that is, for L>>H and W ≤ H. A simple expression for the capacitance can be obtained if we approximate the wire as a long cylinder [5]. In this case, we have

$$C = \frac{2\pi\varepsilon L}{\ln(1+\frac{2H}{W}(1+\sqrt{1+\frac{W}{H}})} \qquad (2.5)$$

Note that the capacitance of the cylinder depends only logarithmically on W and H. We have interpreted W as the diameter of the cylinder. An examination of these two special cases illustrates an important implication. For a given insulator of height H, narrowing the wires through better lithographic and etching techniques will linearly decrease the capacitance only until the width of the wire becomes of the same order as its height. After that, further improvements are achieved at only a logarithmic rate. Typically total capacitance is some combination of parallel plate capacitance one calculates using the parallel plate formulae and the fringing or edge capacitance. We can use Equations (2.4) and (2.5) to approximate [5] the total capacitance of the plate. We define

$$C_{wire} = C_{plate} + 2C_{edge} \qquad (2.6)$$

where C_{plate} is given by Equation (2.4). C_{edge} can be approximated as is shown in figure 2.3.

We replace the sides of the wire with half cylinders. The edge capacitance is then approximated by half the cylinder capacitance minus a small portion of the parallel plate solution we have replaced [5].

We have

$$Cedge \approx \varepsilon L\left\{\frac{\pi}{\ln\left(1+\frac{2H}{T}\left(1+\sqrt{1+\frac{T}{H}}\right)\right)}-\frac{T}{4H}\right\} \qquad (2.7)$$

For H = T and $\varepsilon = 3.9\varepsilon o$, we have C edge $\cong$ 0.044fF/μm. This number is independent of T.

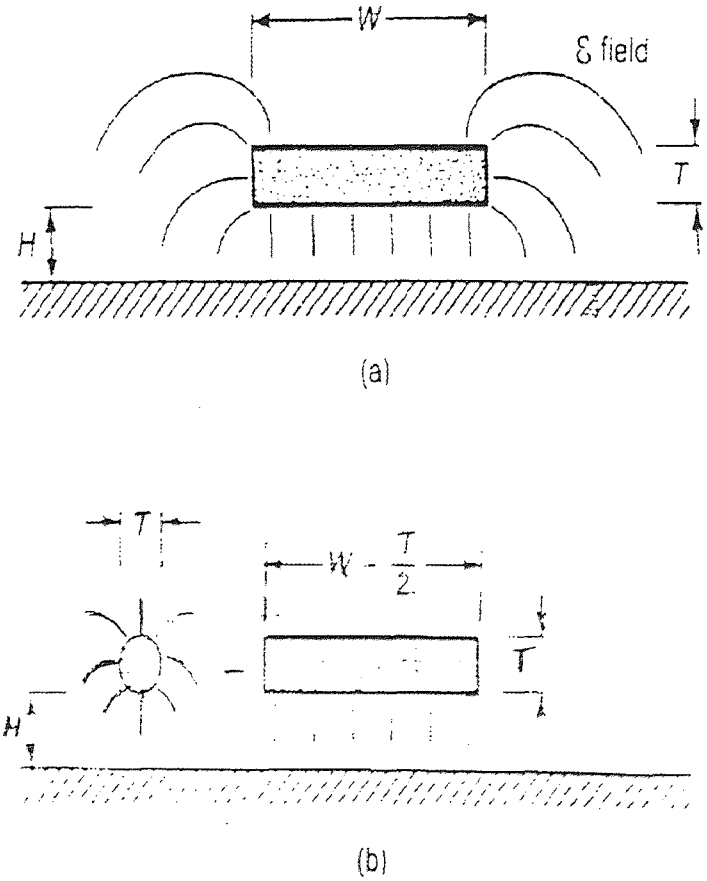

Figure 2.3 Fringing capacitance of narrow wires: (a) fringing electric field lines of a wire; (b) model of a wire as a parallel plate capacitor plus a cylindrical conductor over a ground plane

Equation (2.7) is valid for polysilicon and metal lines.

This approach is used to determine the capacitance that develops between the plates.

Once this capacitance is established then the force developed due to this capacitance is calculated and the same force made use of to determine the deflection that could be generated. This is detailed in the next sub-section.

2.3 Device Simulation

Again for the calculation of force there are two approaches considered.

The force developed due to this capacitance could be calculated from the equation

$$F = \frac{C^2V^2}{2\varepsilon A} \qquad (2.8)$$

where C is the capacitance developed between the plates

V is the voltage applied

A is the effective area between the plates

The value of capacitance is obtained from the latter method explained in sub-section Basic Electrostatics.

The other approach to calculate the electrostatic force is given below.

$$F = (1/2)e_0V^2 (W/H) (L/H) \qquad (2.9)$$

(Refer figure 2.2)

2.3.1 Electrostatic Attraction for Nearly Parallel Plates

In many cases, the structural displacements can be modeled as displacements between nearly parallel plates. Figure 2.4 shows an example this case where two conducting plates are separated by an air (or vacuum) gap and one plate is covered by a thin insulator. In

this case, when the voltage between the plates is held constant, the force between the plates is given by the equation 2.10 [6].

$$P = \frac{F}{A} = \frac{\varepsilon V^2}{2}\left(d_1 + d_2/\kappa\right) - 2 \qquad (2.10)$$

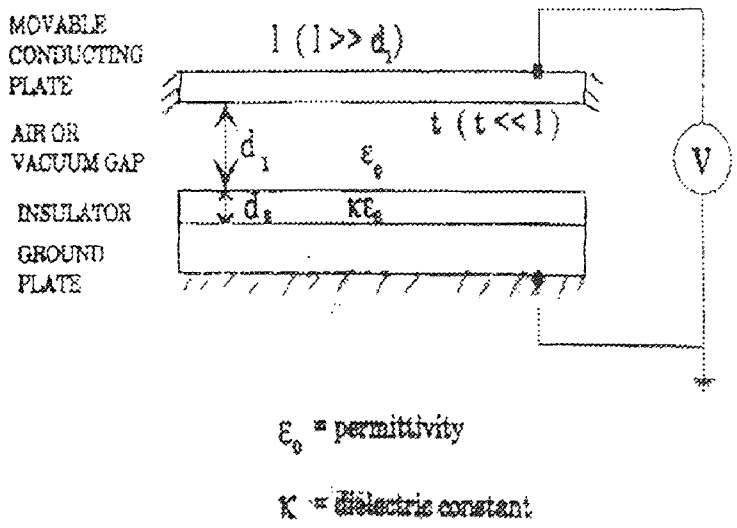

Figure 2.4 Cross-section of a typical MEMS type structure showing a movable conducting plate, air gap, insulator, and immovable ground plate. A voltage, V, is applied between the upper conducting plate and the ground plate

P = Pressure — ε = Permittivity

F = Force — d1 = Distance to insulator

A = Area — d2 = Insulator Thickness

V = Applied Voltage — κ = Insulator Dielectric Constant

Often, one of the conducting plates will be fixed and the other allowed to move but be restrained by mechanical forces. If a voltage is applied between the plates, the

plates will be attracted. At some voltage, the electrostatic attraction between the plates will be sufficient to overcome the mechanical restoring forces and some or all of the upper plate will collapse into contact with the ground plate. This voltage is called pull-in voltage (V_p). If the voltage is now reduced, the upper plate will remain in contact until a second, lower voltage, called release voltage V_r, is reached.

Nathanson [21], first described the pull-in phenomenon for an application called the resonant gate transistor which was modeled using a pair of parallel plates with one plate fixed and the other supported by a simple spring constant K. He showed that for this system the pull-in voltage is given by Equation (2.11)

$$Vp = \sqrt{\frac{8Kd3}{27\varepsilon A}} \qquad (2.11)$$

Once the force is calculated using equation 2.8, the deflection is then calculated. Applying simple beam theory, for a cantilever structure simply supported at one end and free at the other and considering a uniformly distributed load, the deflection is given by

$$= \frac{FL^3}{8EI} \qquad (2.12)$$

Here I is the moment of inertia of the beam taken about the horizontal plane and is given by $I=\frac{WT^3}{12}$ (2.13)

where: 'E' is the Youngs modulus of polysilicon

'F' the force applied on the beams as calculated by equation 2.8

'L' the length of the beam

2.4 Calculations

There are two equations that are used to determine the capacitance namely, 2.4 and 2.5, and two equations available for calculation of force which are 2.8 and 2.9. All four equations are made use of in all combinations and the values obtained are compared.

A) Using equation 2.4 and 2.8 we have

$C_{plate} = \varepsilon WL/H$ and $F = \frac{C^2V^2}{2\varepsilon A}$

$\varepsilon = 8.854 \times 10^{-12}$ F/m

W = 1.6μm. This is the thickness obtained on deposition of polysilicon. Although W is the width of the parallel plates, in our case the effective width is nothing but the thickness of the beams as the parallel plates are in a vertical direction.

L = 75μm, 100μm, 150μm, 200μm. These are the beam lengths considered

H = 2μm is the distance between the beams

V = 10volts. This value is an arbitrary value chosen so as to determine the range in which the deflection would be expected to lie and also because we want the device to operate at this voltage.

Table 2.1 Computed values of capacitance and force using equations 2.4 and 2.8

Lengths (μm)	Capacitance (F/m) $\times 10^{-16}$	Force (N) $\times 10^{-8}$
75	5.312	1.32
100	7.083	1.763
150	10.62	2.64
200	14.166	3.53

B) Using equations 2.4 and 2.9 which are

$C_{plate} = \varepsilon WL/H$ and $F = (1/2)e_0V^2$ (W/H) (L/H) we compute the capacitance and force.

Table 2.2 Computed values of capacitance and force using equations 2.4 and 2.9

Lengths (μm)	Capacitance (F/m) $\times 10^{-16}$	Force (N) $\times 10^{-8}$
75	5.362	1.32
100	7.083	1.77
150	10.62	2.65
200	14.166	3.54

C) Using equations 2.5 and 2.8 which are

$C_{plate} = C = \dfrac{2\pi\varepsilon L}{\ln(1+\dfrac{2H}{W}(1+\sqrt{1+\dfrac{W}{H}})}$ and $F = \dfrac{C^2V^2}{2\varepsilon A}$ we compute the capacitance and force.

Table 2.3 Computed values of capacitance and force using equations 2.5 and 2.8

Lengths (μm)	Capacitance (F/m) $\times 10^{-15}$	Force (N) $\times 10^{-7}$
75	2.16	2.19
100	2.89	2.94
150	4.33	4.411
200	5.782	5.89

D) Using equations 2.5 and 2.9 which are

$C_{plate} = C = \dfrac{2\pi\varepsilon L}{\ln(1+\dfrac{2H}{W}(1+\sqrt{1+\dfrac{W}{H}})}$ and $F = (1/2)e_0V^2$ (W/H) (L/H) we compute the capacitance and force.

Table 2.4 Computed values of capacitance and force using equations 2.5 and 2.9

Lengths (μm)	Capacitance (F/m) $\times 10^{-15}$	Force (N) $\times 10^{-8}$
75	2.16	1.328
100	2.89	1.77
150	4.33	2.65
200	5.78	3.54

The deflection is calculated applying the simple beam equation $\delta = FL^3/8EI$

This equation is considering a uniformly applied load for a cantilever.

$E = 1.9 \times 10^{11}$ N/m^2, the Youngs Modulus of polysilicon

$I = WT^3/12$, the moment of inertia of the beam considered in the vertical axis, T is the width of the cantilever which is 2μm.

The deflection is obtained using all the four combinations

Combination 1 = A, Combination 2 = B, Combination 3 = C, Combination 4 = D

Similarly computation is done for a varying voltage for each beam length. Also the thickness of the beams is changed from 1.6μm to 2μm. The results are tabulated below.

The table 2.6 shows the voltage being increased from 2 volts to 20 volts. The beam length is varied from 100μm to 250μm in steps of 50μm.

Table 2.5 Deflection obtained for various beam lengths using the combination of equations (Computed)

	δ obtained for Combination of Equations (μm)			
Beam Length	A	B	C	D
75	0.0034	0.0034	0.056	0.0034
100	0.0108	0.0108	0.181	0.0108
150	0.0549	0.0549	0.91	0.0549
200	0.174	0.174	2.9	0.174

The deflections are calculated using combination D so as to include the capacitance caused due to the fringing fields. This set of deflections is the theoretical simulation results. Based on this results the dimensions of the beam have been set up.

The dimensions of the beam are as follows:

Length of the beam = Increase from 50μm to 200μm in steps of 50μm.

Width of the beam = Increase from 1.5μm to 3μm in steps of 0.5μm.

Thickness of the beam = 2μm

Space between the beams = 2μm and 2.5μm

The graph (figure 2.5) of beam length versus deflection for a constant impressed voltage of 10 Volts is shown. The graph plots the deflection calculated using the four combination of equations. It is clear that combination A, combination B and combination D match. Using Combination C we get a different set of values. Hence the simulation is done considering equation combination D.

Table 2.6 Varying voltage and deflection simulated for varying beam lengths

Applied Voltage Volts	Beam Length							
	250μ		200μ		150μ		100μ	
	Force $x10^{-8}$(N)	δ (μ)	Force $x10^{-8}$(N)	δ (μ)	Force $x10^{-8}$(N)	δ (μ)	Force $x10^{-8}$(N)	δ (μ)
2	0.221	0.017	0.177	0.0069	0.132	0.002	0.088	0.0004
5	1.38	0.106	1.106	0.043	0.83	0.013	0.55	0.0027
10	5.53	0.426	4.427	0.1743	3.32	0.055	2.21	0.0099
15	12.4	0.956	9.96	0.393	7.4	0.123	4.98	0.024
20	22.13	1.706	17.76	0.69	13.2	0.219	8.85	0.043

The graph (figure 2.6) shows the simulation of deflection versus applied voltage with the voltage increased from 2 Volts to 20 Volts. The graph is plotted over the lengths 100μm to 200μm in steps of 50μm. It is seen that the deflection achieved for a cantilever of length 200μm, width 2μm and for a applied voltage of 20 Volts is 0.69μm.

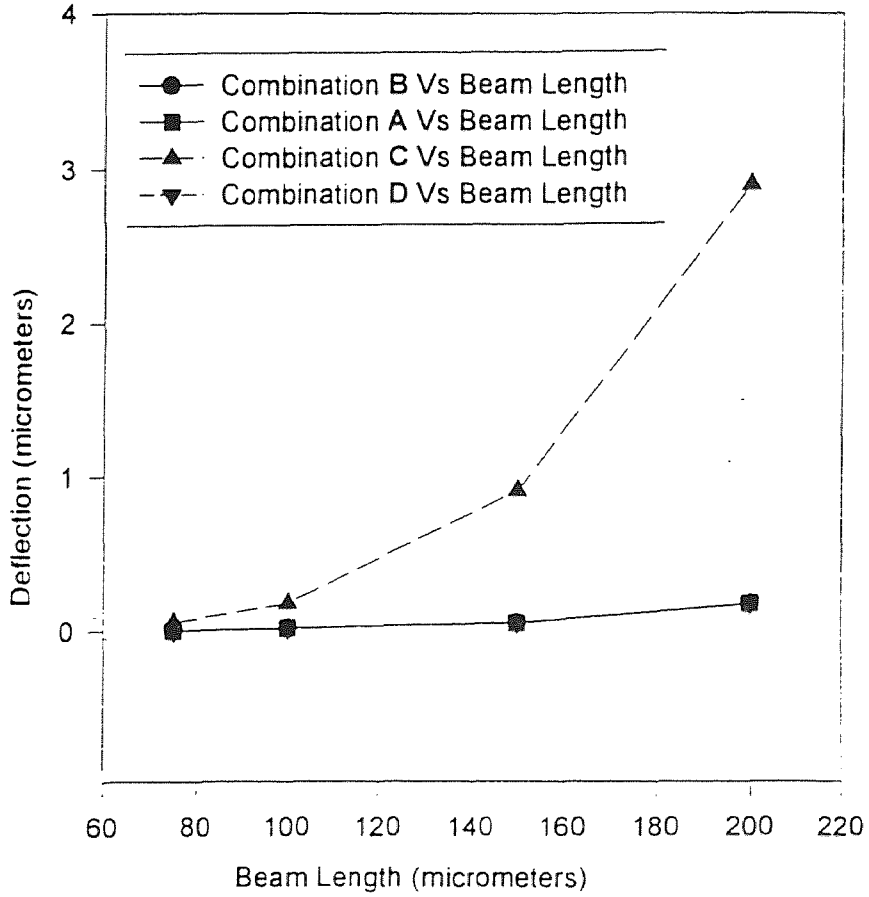

Figure 2.5 Graph showing the deflection calculated for the combination of equations

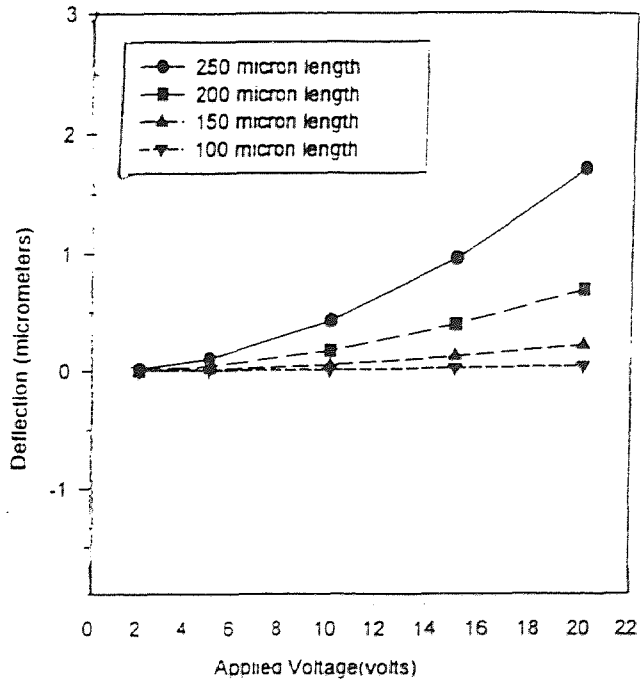

Figure 2.6 Graph showing deflection versus applied voltage for different beam lengths

CHAPTER 3

FABRICATION

3.1 Introduction

In this chapter the detailed fabrication sequence is described. A brief introduction to the particular process step is detailed in the beginning of each process and the actual values during the fabrication given following this. All the defects and problems encountered during each of the processing step is discussed at the end of that particular process and the ways in which to overcome these problems are also detailed.

3.2 NJIT Clean Room

All the process work was done in the NJIT clean-room. NJIT clean room is a 1200-sq.-ft and class 10 fabrication line. It was equipped with all the necessary tools for processing wafers up to 150mm in diameter. These equipment include:

1) Wafer Inspection - microscope, Dektak profilemeter

2) Nanometrics optical line width

3) Wet chemical station Ultratek mask/wafer scrub

4) Semitool spin/rinse dryers

5) Karl Suss exposure system

6) Nanometrics FTM

7) Inspection microscope

8) MTI Coat and develop system

9) Drytek reactive ion etching system

10) Leitz MPV FTM

11) Varian sputtering system

12) BTU diffusion furnace

13) BTU LPCVD furnace

14) MDA toxic gas monitors

15) Tubewash station

16) MG Industries gas cabinets

3.3 Outline of the Process Steps for Fabrication

An outline of the processing steps that need to be followed is outlined. First the flow charts for the fabrication of the device is detailed and following this a schematic of the process is detailed.

3.3.1 Flow Sheet for Fabrication of the Device

Silicon Wafer

↓

Deposition of LPCVD oxide

↓

Deposition of Polysilicon)

↓

Photolithography to pattern polysilicon

(Mask 1)

↓

Reactive Ion Etching(RIE) of Polysilicon

↓

Sputtering of Metal

↓

Photolithography to pattern the Metal

(Mask 2)

↓

Wet Etch of the Metal

↓

Photolithography to define the sacrificial oxide etch areas

(Mask 3)

↓

Wet etch of the sacrificial oxide to release the beam structures

3.3.2 Schematic of the Fabrication of the Device

The figure shows the step by step processes the wafer undergoes. A small description is given as the caption to each figure

Figure 3.1 a A plain silicon wafer is taken and the preliminary steps like denuding and cleaning it in DI water is done

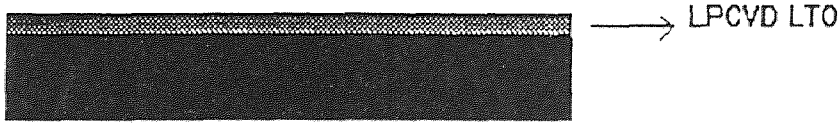

Figure 3.1 b A 1.5μm thick LPCVD LTO is deposited on the wafer

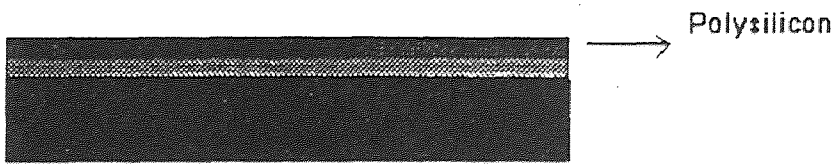

Figure 3.1 c A 1.5μm thick polysilicon is deposited on the LTO

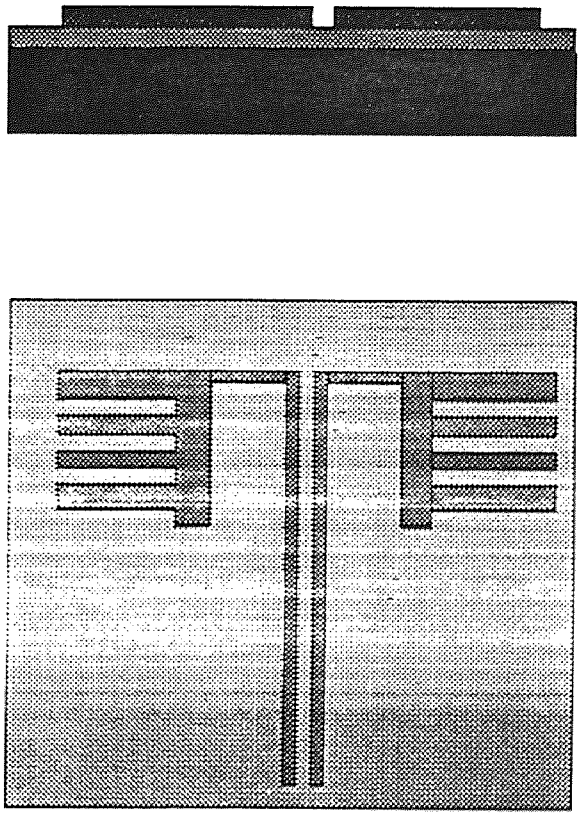

Figure 3.1 d This polysilicon is patterned using Mask 1. Top and side view are seen

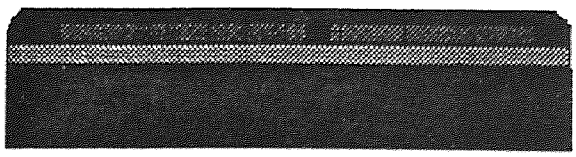

Figure 3.1 e A 0.5μm metal is sputtered on the patterned polysilicon.

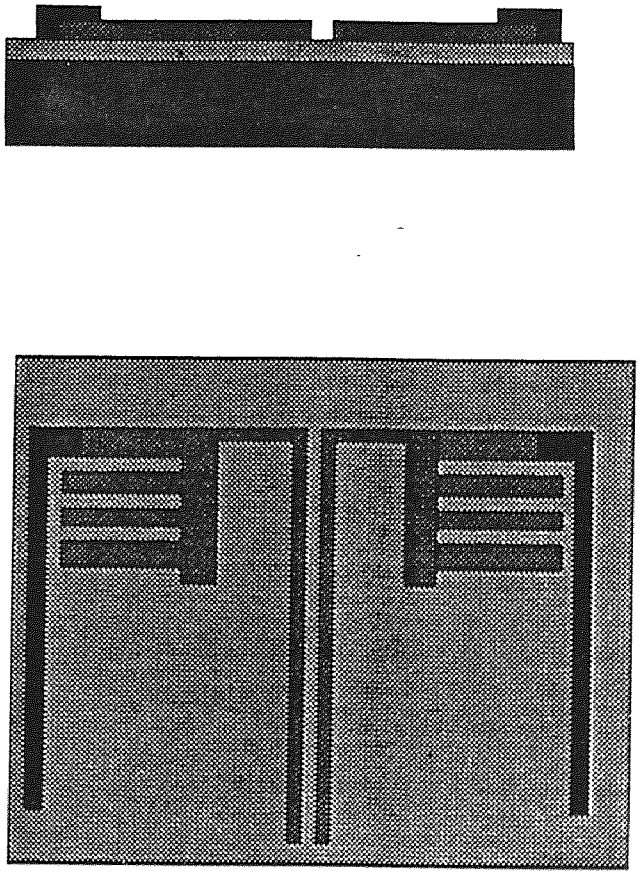

Figure 3.1 f The metal is wet patterned using Mask2 and wet etched as shown in the top and side view

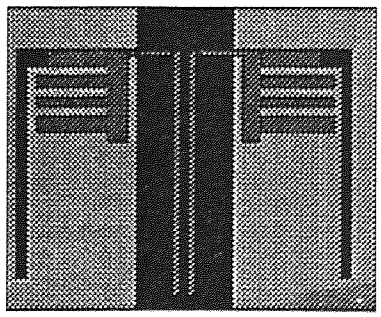

Figure 3.1 g Sacrificial mask # 3 is used to pattern the wafer so as to define the oxide etch regions.

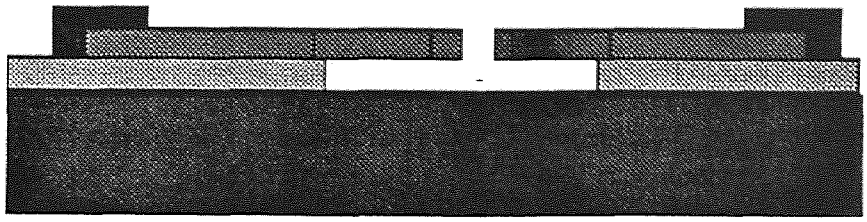

Figure 3.1h The wafer is etched in a wet etch bath so as to release the beams

The mask plates #1,#2 and #3 that are used were fabricated by Photronics Inc. The design of these masks are shown below. Figure 3.2 a shows the mask 1 which is the polysilicon pattern mask. This pattern defines the beam and antennae design. Figure 3.2 b shows the metal routing design. This mask is used to route the metal lines to provide for probing. Figure 3.2 c shows the mask used to define the sacrificial etch oxide in order to release the beams.

3.4 Deposition of SiO_2 by LPCVD

3.4.1 Introduction

Low pressure chemical vapor deposition (LPCVD) of silicon di oxide is generally based on the reaction of SiH_4 and oxygen. The feasibility of using organic liquid sources like tetra ethyl ortho silicate(TEOS), ethyl tri ethoxy silane(ETOS), diacetoxydi-tert-butoxysilane(DADBS), to form silicon di oxide for microelectronics applications has

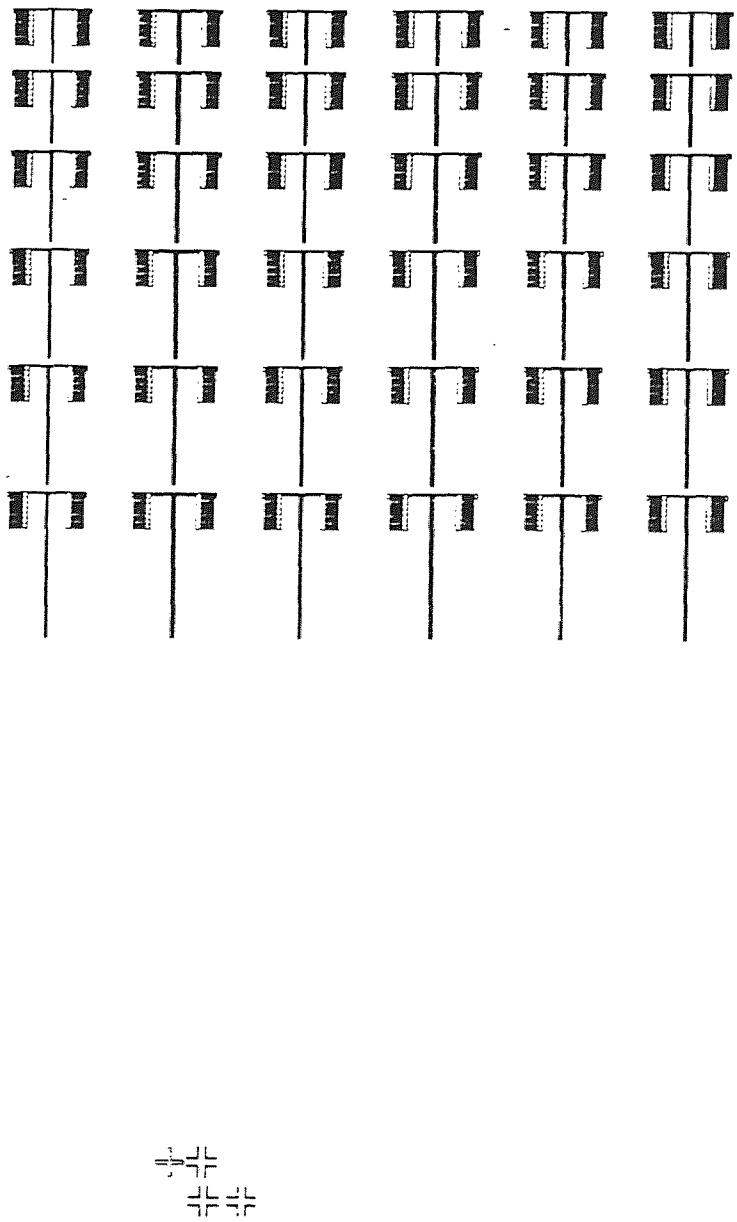

Figure 3.2 a Polysilicon pattern mask design

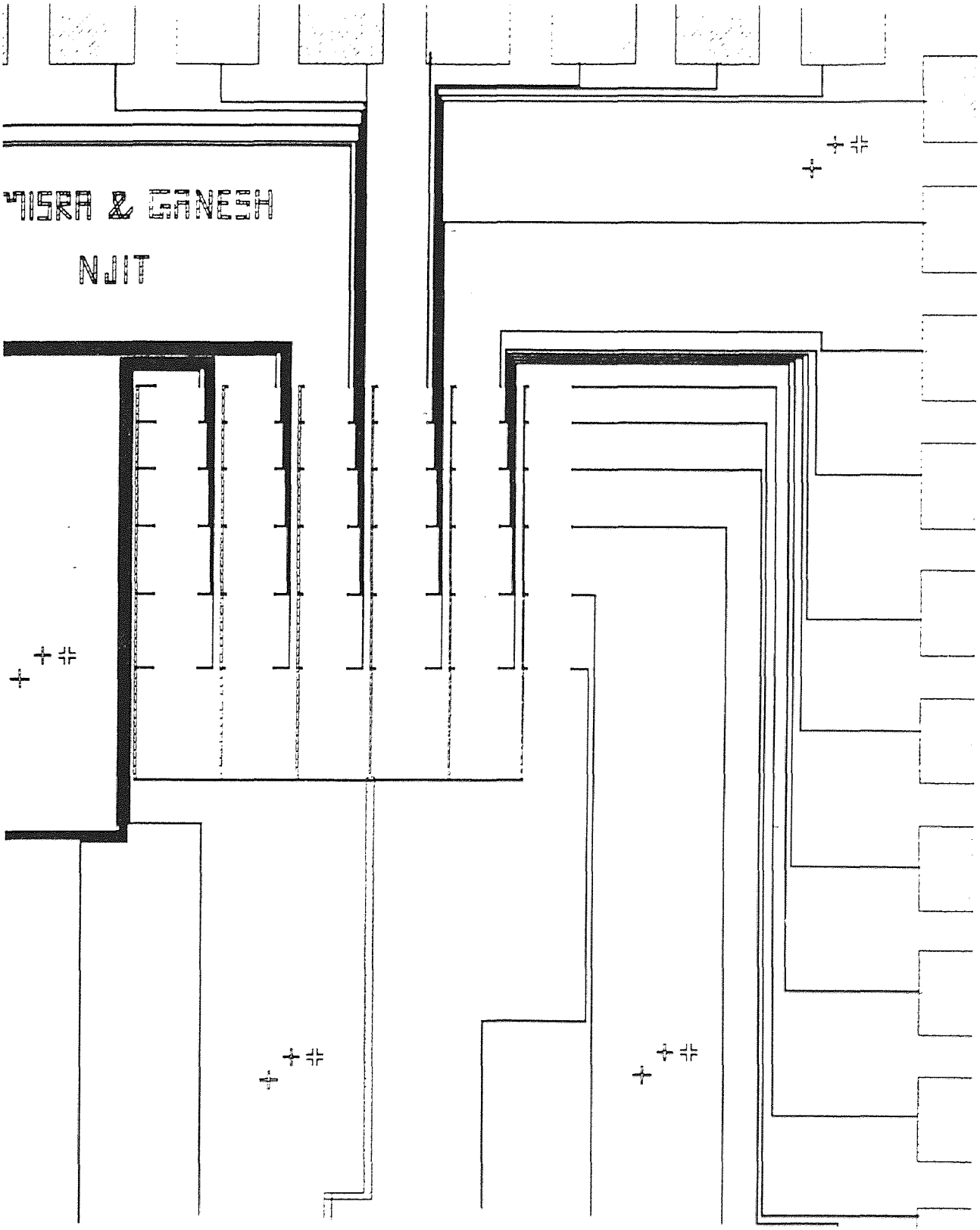

Figure 3.2 b Metal pattern design

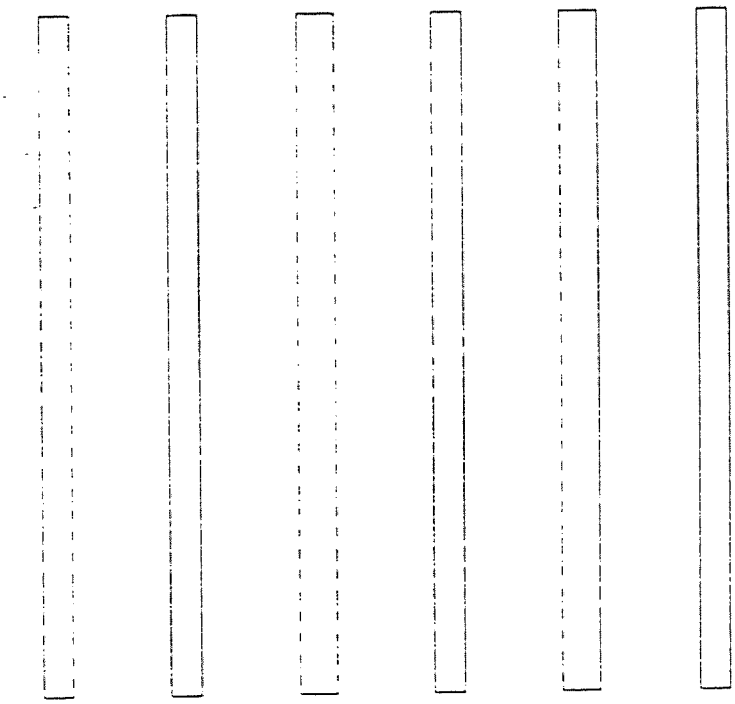

Figure 3.2 c Sacrificial oxide pattern design

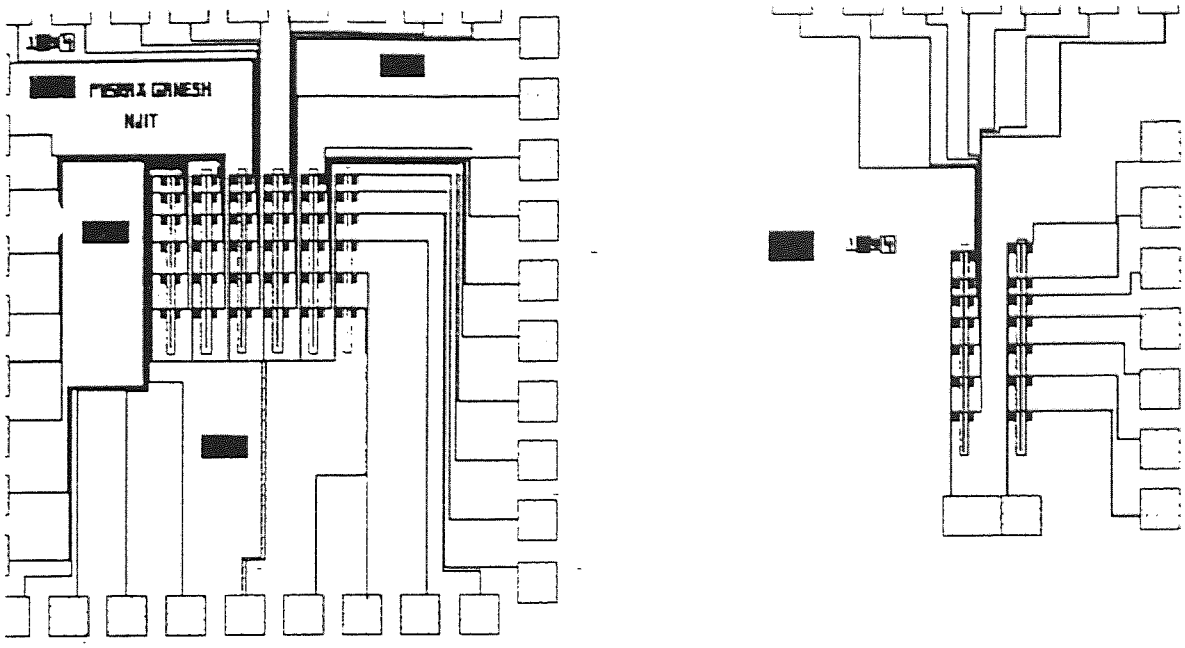

Figure 3.2d All the mask patterns superimposed on one another

demonstrated by several researchers. Such liquid precursors offer numerous advantages over the use of silane including superior step coverage and increased safety.

DES is a precursor capable of producing oxide films at temperatures as low as 350^0C, thus allowing its use as a dielectric between aluminum metallization levels or as a top layer passivation coating. DES has several advantages over silane including superior conformity, low particulate formation, low stress, and high crack resistance. DES is a colorless liquid with a boiling point of 56°C and freezing point less than -76°C at atmospheric pressure. It exhibits a vapor pressure of 207 Torr at 20°C.

The description of the LPCVD reactor is detailed in Appendix A

3.4.2 Experimental Values

The requirement was an oxide of thickness 1.5μm. The wafer underwent the following process steps before loading them into the furnace. A total of 12 wafers of p-type was chosen as the batch. The wafers were purchased from WaferNet Inc. The sheet resistivity of these wafers was 10 Ω/square.

The detailed flow chart of the process and the oxide deposition conditions is detailed in Appendix A2.

The deposition rate of the LPCVD reactor was 600A° /minute. One of the wafers was removed from the furnace after the first 8 hours of deposition and its thickness measured. It was found that the deposition rate had considerably lowered . The new deposition rate was found to be 540 A° /minute. Based on this deposition rate the time to completion was fixed. The entire deposition took 24 hours and 45 minutes resulting in an average oxide thickness of 1.43μ.

An important note here is that the wafers were not removed from the reactor at any point of time. Therefore there was no need for any kind of denuding to be done in between depositions.

The oxide thickness was measured using a Leitz MPV FTM. The oxide thickness were measured at 13 points on the wafer. The points at which the oxide thickness was measured and the thickness is detailed in Appendix A3. The oxide thickness measured was 1.6μm.

3.5 Deposition of Polysilicon

3.5.1 Introduction

Applications of polysilicon to IC construction include its use for leads and MOS gate electrodes, as a fuse material in making ROMs, as load resistors in some MOS circuits, and as a diffusion source for emitter or source/drains. In addition, active devices will occasionally be made in thin-film polysilicon.

All of these applications require layers of polysilicon less than 1μm thick. But polysilicon is an extremely strong material and is very popular as a structural material and is dominating most of the MEMS devices. The mechanical properties of polysilicon is given in Appendix B.

The methods of polysilicon deposition is detailed in Appendix C. The process flow chart and the deposition conditions are outlined in Appendix C1

The polysilicon deposited was measured to be 1.6μm thick.

3.6 Polysilicon Doping

The polysilicon film of thickness 1.5μm had to be doped with Phosphorus so as to achieve a very low resistivity. The process flow of the doping and the process conditions is detailed in Appendix D.

Doping serves two purposes. Firstly as mentioned before we need a very low resistivity of Polysilicon as the polysilicon beams are going to carry charge. The

resistivity being low this will aid in easy charge transfer and will not result in any sort of temperature build up.

Also diffusion is carried out at 950°C. This acts as a thermal mechanism to reduce strain built in the polysilicon while undergoing deposition. It is clearly noticed that polysilicon films that have undergone annealing have considerable reduction in strain. This is well substantiated by the fact that there was no bending or warping of the beams during release. The longest beam is 250μm and as the SEM micrograph 3.5 shows, there is no bending along the entire length. Therefore there was no need to add another anneal step as the diffusion itself took care of this.

Also important to note that after diffusion there is about 1500A° of oxide deposited on the wafer. We used a 1 minute BOE etch to get rid of this oxide layer. This should be done carefully as any remains of oxide will hinder the device working by acting as an insulator.

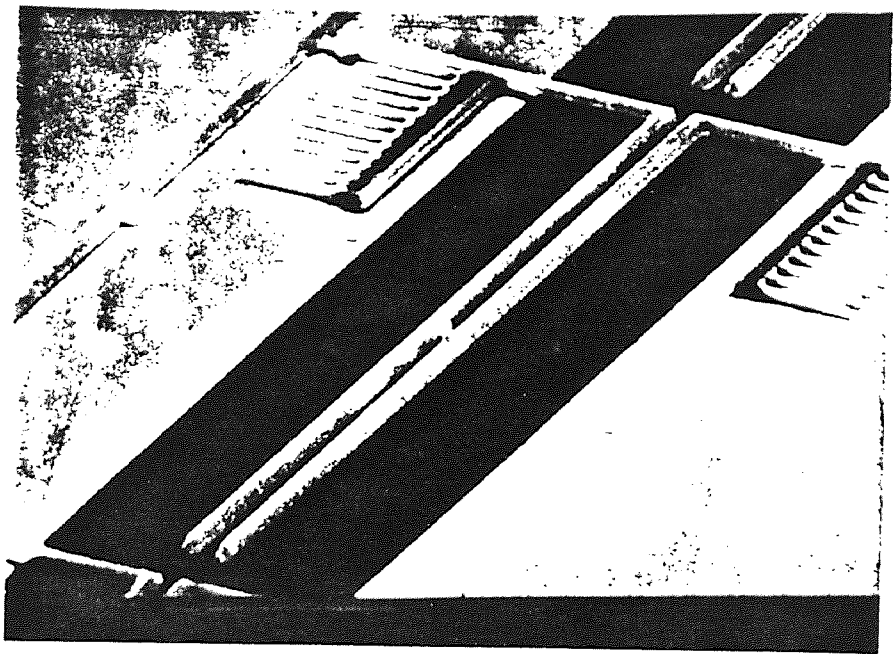

Figure 3.3 SEM micrograph showing horizontal beams with no bending

The Polysilicon resistivity was again measured and found to be 10 Ω/square. This is well within the expected value.

3.7 Photolithography

3.7.1 Introduction

Fabrication of micro electro mechanical devices or optic devices on a silicon substrate requires working on a tiny region of the substrate. The patterns that define such regions are created by lithographic processes. That is layers of photoresist materials are first spin coated onto the wafer substrate. Next the resist layer is selectively exposed to a form of radiation, such as ultra violet light, electrons, or x rays. An exposure tool and mask, or a data tape in electron beam lithography are used to effect the desired selective exposure. The patterns in the resist are formed when the wafer undergoes the subsequent "development" step. The areas of the resist remaining after development protect the substrate regions they cover. Locations from resist has been removed can be subjected to a variety of additive or subtractive processes that transfer the pattern onto the substrate surface.

The basic photoresist terminology and description of the lithographic process is described in Appendix G.

3.8 Etching

3.8.1 Introduction

Etching in microelectronics fabrication is a process by which material is removed from the silicon substrate or from thin films on the substrate surface. When the mask layer is used to protect specific regions of the wafer surface, the goal of etching is to precisely remove the material which is not covered by the mask.

The theory of wet and dry etching is detailed at length in Appendix H.

3.8.2 Description of the RIE Process

The polysilicon was etched using slightly different conditions than the standard conditions followed by the clean room. The clean room standards as well as the conditions that were used are given in the table below.

Table 3.1 Conditions to etch Poly (Standard)

Power	400 W
Pressure	150 mTorr
Flow rate of SF_6	50 sccm
Flow Rate of Freon-112	50sccm
Temperature	25°C

The etch rate for Polysilicon is 388 Å/min under these conditions. Thus the etch time is decided depending on the thickness of the Polysilicon.

The conditions above resulted in polysilicon cantilevers having poor vertical walls. The edges of the cantilever were sloped by at least 15o. This is not acceptable as the effective electrostatic force will reduce in case the walls are not perfectly vertical. To reduce this effect the power of the reactor was maximized and the pressure in the chamber minimized so as to achieve a concentrated etch on the polysilicon resulting in good vertical walls. The table shows the process conditions to etch polysilicon.

Table 3.2 Conditions used for etching of Polysilicon

Power	650 W
Pressure	70 mTorr
Flow rate of SF_6	37 sccm
Flow Rate of Freon-112	37sccm
Temperature	25°C

The etching of polysilicon was done and observed under the microscope. The SEM micrograph shows the polysilicon after the etching is completed. We can clearly see that the etching is uniform and there is a clear gap between the beams.

Another problem that arose due to the increased power was that the part 'A' of the cantilever structure was consistently getting over etched compared to part 'B' (refer figure 3.5). This may be due to localized loading effect and the formation of a retarding potential being developed in the part 'B' of the cantilever. The retarding potential may

develop due to continuous exposure to the plasma and reduces the anisotropic etching effect of the ions. On the other hand part 'B' has another cantilever just 2μm from it. In order to minimize the overetch on 'A' the process was carried out in four etch stages, the time of each etch being 8 minutes. This helped in reducing the effect of the retarding potential. This effective and a uniform etch was obtained.

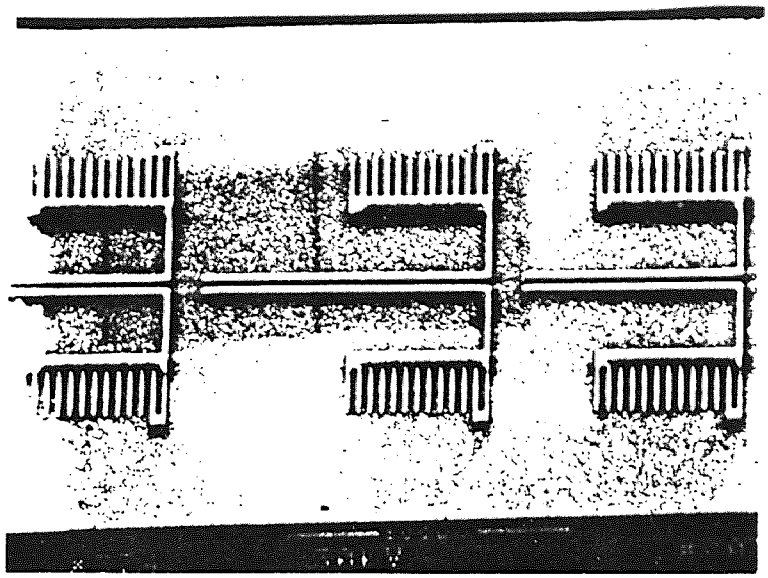

Figure 3.4 Micrograph of the etched polysilicon beams

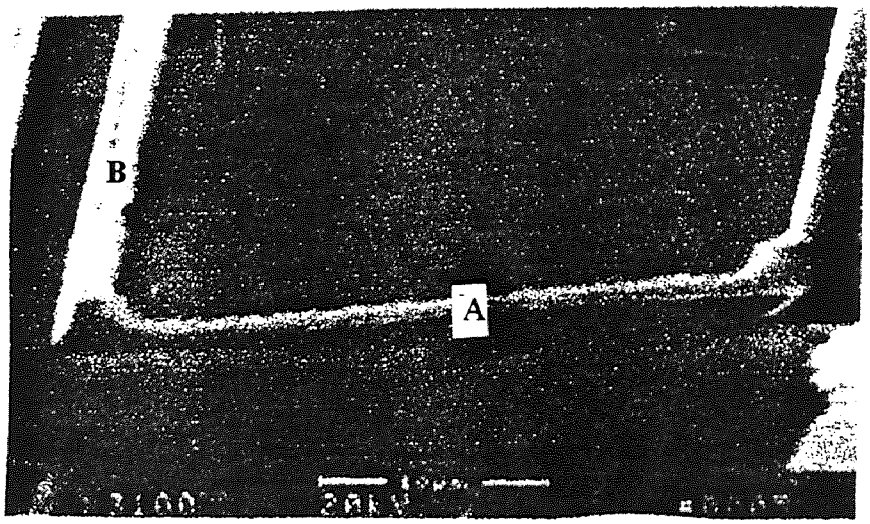

Figure 3.5 Over etch on part 'A' of the cantilever structure

3.9 Metal Sputtering

3.9.1 Introduction

The next step in the fabrication of the device is the metal deposition. Metal is used as the connections of the device. The metal used here was an alloy of Al-Si-Cu.

The most widely used techniques to deposit metals are, evaporation, sputtering, and CVD (chemical vapor deposition). Variations to these techniques are collimated sputtering and selective CVD. Some of the deposition methods are detailed in Appendix E. The flow chart as well as the deposition conditions are also detailed in Appendix E.

3.9.2 Photolithography and Patterning of Metal

After the metal deposition, the sheet resisitivity of the wafer is checked. It should be in the range of 1-2Ω/. The wafer is then taken and photoresist pun on it. This is then patterned using mask #2. The wafer is ready for metal etching. Metal etching was done by a wet etch process.

The wet etch process involves that the wafer be dipped in a solution of etchant which is a combination of sulfuric and nitric acid.

The etch rate at 45°C is 1000 A°/minute. This is a critical step as the aluminum etching solution eats away the metal deposited in 30 seconds as we have a thickness of only 5000 A°

As soon as the 30 seconds is up the wafer is immediately dipped in water so as to stop the reaction. The wafer is then dipped in a photoresist strip bath of M-pyrol. This isn't done

in a conventional p-strip bath as there is metal deposited and the p-strip bath attacks metal. Therefore if there is metal deposited on the wafer then the M-pyrol bath is used. The time of stripping is usually 5 minutes in bath A and 5 minutes in the bath B.

3.10 Sacrificial Oxide Etch

The device is now ready for release of the cantilever structures. Photolithography is done so as to pattern the areas that need to be protected and the areas around the beams exposed. Mask #3 is used for this. Once the patterning is done the wafers are ready for release.

The method of etching followed here is wet etching. We need an isotropic etch so that oxide underneath the beams also is etched. The etching solution for oxide selected was Hydrofluoric Acid (HF). Buffered HF in the ratio 7:1 was selected.

A experiment was set up so as to take care of the following potential problems:

a) In case the time chosen for the etch results in an over etch then there is a problem of the beams collapsing on the substrate.

b) In case of an under etch time, then the beams will not be released from the substrate.

c) One of the major problems facing the release of cantilever or doubly supported beams is the effect of Van der Waals forces that come into play during the phase change from liquid to gas. This occurs when the wafer is washed with water and the water dries in air. The water molecules under the beams pull the beams onto the substrate when they evaporate. Care should be taken to avoid this problem.

The method of avoiding the first two problems is by arriving at a process time that optimally etches the sacrificial oxide layer. This time was experimentally determined to be 8 minutes and 30 seconds. The process steps followed for the sacrificial etch is detailed in Appendix F.

The points to be born in mind while carrying out this process step are:

I) At no point of time should the wafer be allowed to dry. There should always be a film of liquid on the wafer. While transferring from the BHF bath to the DI water bath, a film of BHF must be allowed to remain on the wafer.

ii) A film of M-Pyrol is allowed to remain on the wafer and this is placed as is on the hot plate. The hot plate is kept at 120°C and there is a step increase from room temperature to 120°C. This results in the liquid molecules quickly drying up.

It is observed that there is no collapse of the beams on the wafer on the substrate if the above mentioned points are followed. The SEM micrograph shows the released cantilever beams.

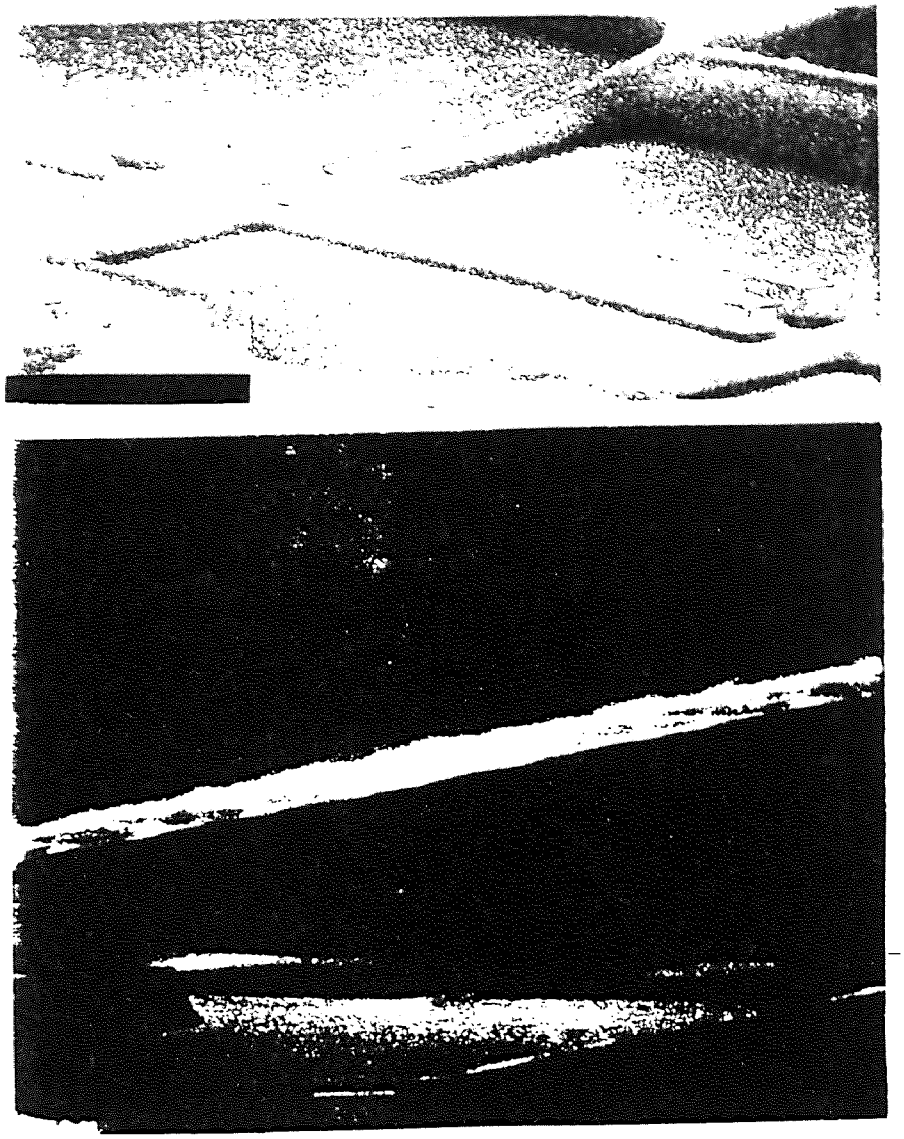

Figure 3.6 SEM micrograph showing the released cantilever beams

CHAPTER 4

TESTING PROCEDURE AND RESULTS

4.1 Introduction

The method adopted in calibrating the sensor is detailed in this chapter. Following this the experimental results are outlined.

As we know the device is based on the electrostatic principle, several methods have been used to test the device. In our case a voltage is applied between the cantilevers. This is done by probing the metal bonding pads. The bonding pads are made of Al-Cu-Si alloy and are routed in such a fashion such that they directly connect to the antennae structures of each individual cantilevers. The routing is designed in such a way that the cantilever pairs i.e. the right cantilever and the left cantilever of each device are electrically isolated. As there are eight columns and six rows of devices on each module the total number of devices on each die is forty eight. Each of the device has two connecting points or probing points so as to power it. That brings the total number of probing pads to ninety six. The size of each module has to be minimized so as to achieve greater packing density on each wafer. The overall size of each module is about ten thousand micron by ten thousand micron. It is not possible to fit in ninety six bonding pads in this limited area considering the fact that the

bonding pads have to be of a minimum of 500μm by 500μm each with a gap of at least 500μm between them.

This problem was solved by connecting all the right cantilevers of each device to one single bonding pad. In this case the voltage will have to be impressed between the left cantilever of the device under consideration and the common bonding pad for that particular module. This has proved to work effectively as we save space on the chip as well as the time of testing is considerably shortened. For testing many devices on each module only the left bonding pad of each device will have to be probed. The right cantilever's bonding pad will remain probed all the time as long as the same module is being tested.

A probe station made by the Micromanupulator company was used. The wafer was split into 6 parts due to space limitations on the microscope. An optical microscope was used to test the device. The wafers are vacuum held on the probe station and are also clamped lightly onto the microscope. A d.c voltage source is applied. The left probe is connected to the +ve of the supply and the right probe connected to the -ve of the supply. The current cut off is kept at a minimum as we are interested in applying a constant voltage with minimum current flow.

4.2 Steps Involved in Testing

A detailed account is given of the steps involved in testing.

The wafer is placed on the microscope base. A thorough survey of the wafer is done. Checks for presence of dirt or any other foreign body is essential as this may lead to

some unforeseen problems. The wafer is scanned and a good module is then selected for experimentation. Selection of a module involves:

i) The polysilicon cantilevers look uniform and are straight, there should not be any curvature along the length of the cantilevers whatsoever. Also the cantilevers must appear released from the oxide underneath. This means that all of the sacrificial oxide should have been etched away. This is difficult to see in an optical microscope as the only view achievable in this case is a top view. Therefore a Scanning Electron Microscope is used. The SEM micrograph gave a very clear indication whether or not the cantilevers are released.

ii) The next step is to check if the cantilevers have collapsed onto the substrate. The problem of cantilevers collapsing onto the substrate can take place due to adhesion of the water molecules present in between the cantilevers and the substrate. The Van der Waals forces present can be very high and even bond the cantilevers onto the substrate. Also the cantilevers may collapse on to the substrate due to self weight. To make sure the cantilevers are released is checked with the help of the SEM. Another method of testing this problem is by checking the connectivity between the cantilevers and the substrate. As shown in figure 4.1 one of the bonding pads is probed and the other probe is connected to the substrate. If the cantilevers have collapsed on the substrate then this acts as a electrical short.. If there is no continuity then this could mean one of two things. Either the cantilevers are upright or there is a electrical break in the metal routing. The SEM micrograph 4.2 shows the cantilever collapsed onto the substrate. This particular device shows a continuity when the test is done.

iii) The metal routing needs to be checked to make sure that the applied voltage on the bonding pad is reaching the cantilevers. As shown in figure 4.3 the bonding pad is probed and the antennae structure is probed. We got a continuity signal.. This proves that there is good contact between the poly and the metal and also that the route is good. One of the problems faced during fabrication is the step coverage occurring between the metal and the poly. The polysilicon is 1.6μm. The metal thickness is 0.5μm and there may be a break in the metal covering the polysilicon. This test ensures that there is good contact between the poly and metal.

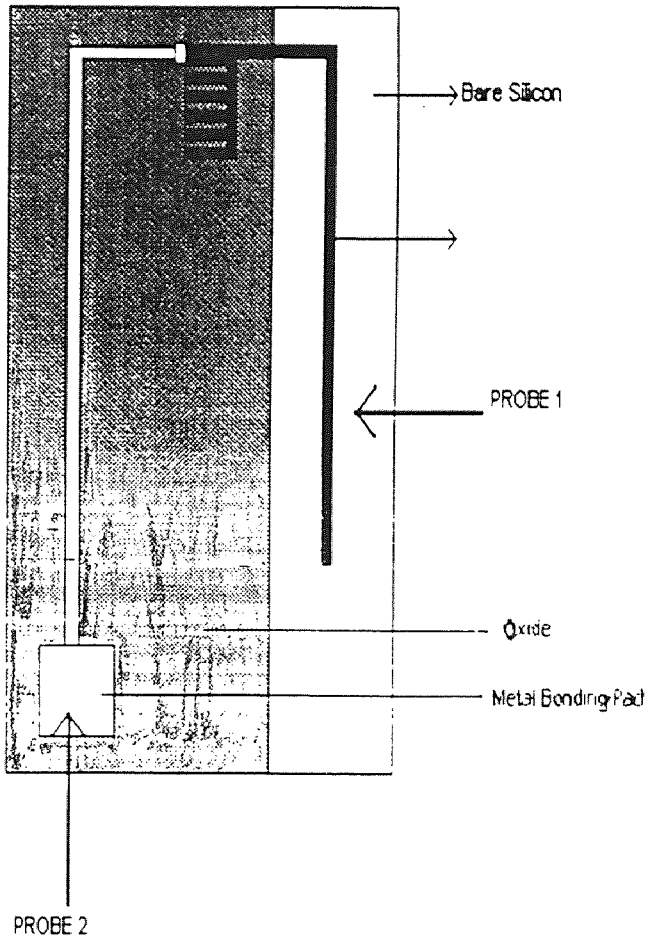

Figure 4.1 Schematic showing the connections made to test the electrical isolation

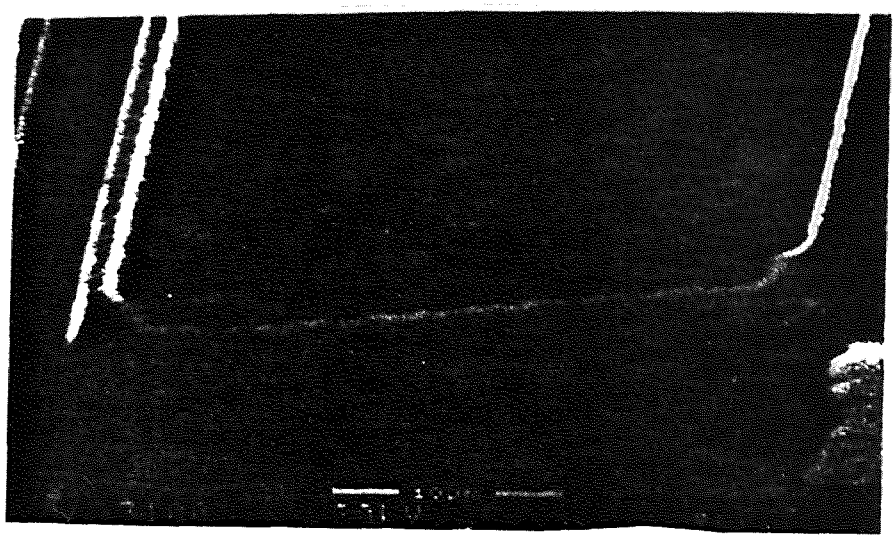

Figure 4.2 SEM micrograph showing the cantilevers collapsed on the substrate.

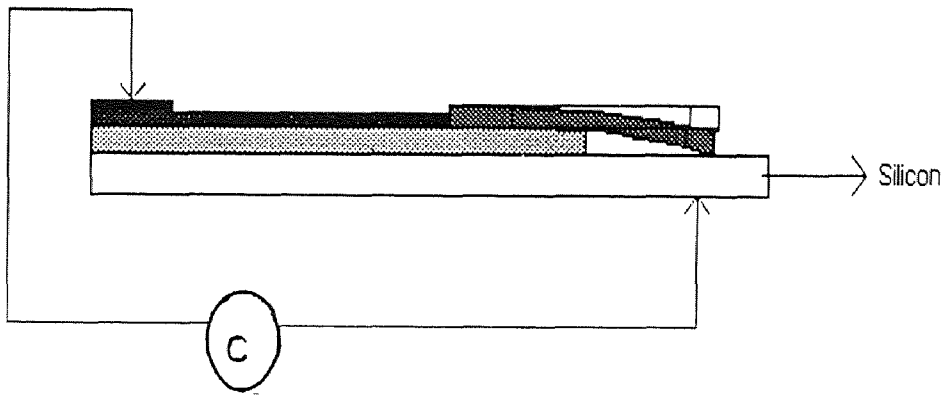

Figure 4.3 Schematic showing the connection made to test continuity

iv) The next step is to apply voltage. The probes are placed on the bonding pads so as to power individual devices. The d.c source is in the 'off' position. After the connections are

made the current is kept at a minimum and the voltage is increased in steps of 2 volts. The microscope is connected to the video monitor and the experiment is recorded.

Some of the points to be noted during testing are:

A) Care should be taken to see that the corresponding device is being tested for the bonding pads that are being probed. Although this seems to be a simple problem it seems to be the most prevalent one.

B) The increase in voltage should be done extremely slowly, about 2 volts every 30 seconds.

C) On the event of any of the probe wires touching ground, it will not be possible to increase the voltage on the source. If such a problem should arise then isolation of the wires are to be checked. This problem may occur also if there has been a localized oxide breakdown. The oxide is about 1.6μm thick. In case we increase the voltage to about 100 volts then there is a possibility of oxide breakdown. This causes a electrical short to the ground and it will not be possible to achieve increase in voltage.

4.3 Experimental Results

The test results obtained are as follows. The cantilever of length 150μm deflected by 2μm for an applied voltage of 65 Volts. As the space between the beams was 2μm, the maximum achievable deflection is also 2μm. It was not possible to record the deflection at incremental steps of applied voltage as the cantilevers were pulled towards each other instantly.

incremental steps of applied voltage as the cantilevers were pulled towards each other instantly.

Similarly beams of length 200μm and 250μm deflected by 2μm for applied voltages of 56 volts and 50 Volts.

4.4 Discussion

The Table 4.1 shows the comparison of the experimental results and the simulated results for the following parameters:

I) The length of the cantilevers : 150μm, 200μm and 250μm

ii) The width of the cantilevers : 2μm

iii) The thickness of the cantilevers : 1.6μm

iv) The space between the cantilevers : 2μm

v) The deflection is set at 2μm

vi) The permitivity of air $\varepsilon = 8.854 * 10^{-12}$

vi) The young's modulus of Polysilicon = $1.9 * 10^{11}$ N/m^2

This is also summarized in figure 4.4

Table 4.1 Comparison of experimental and simulated values

	Voltage (Volts)		Deflection (μm)
Cantilever Length (μm)	Experimental	Simulated	Constant
150	65	60.1	2
200	56	35	2
250	50	22	2

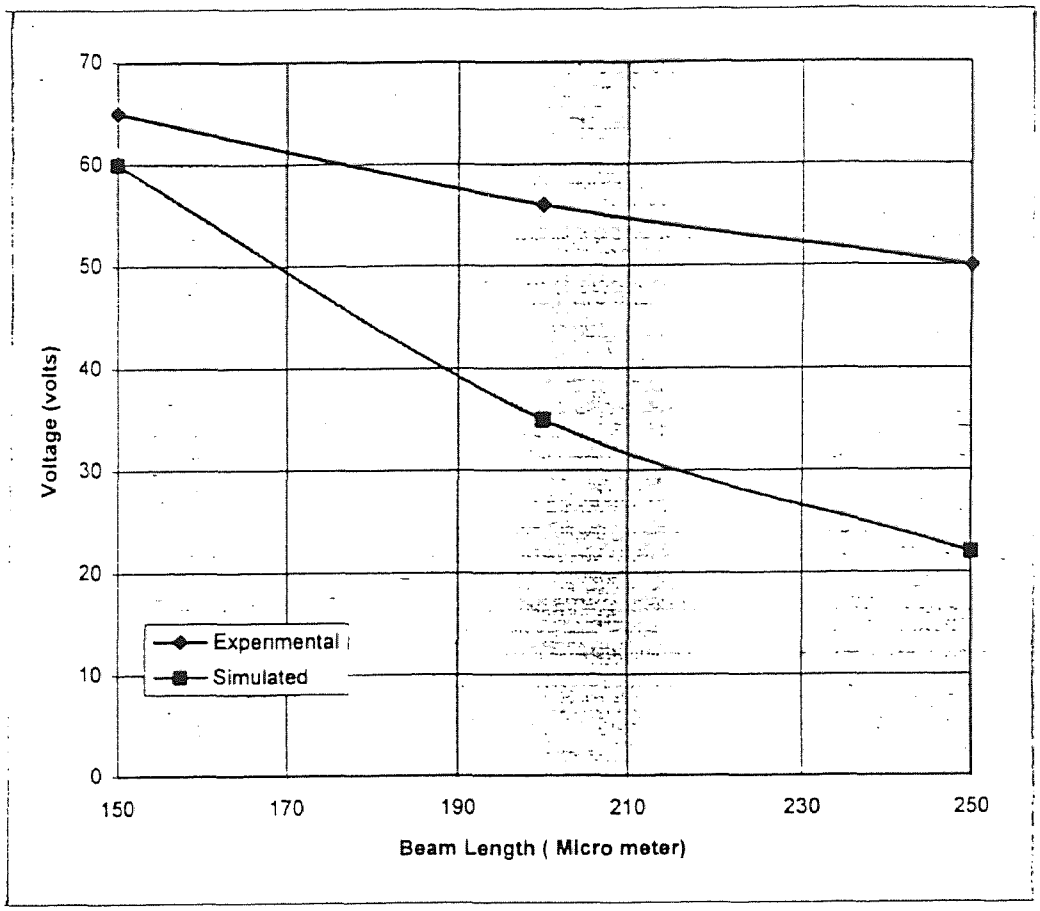

Figure 4.4 Comparison of simulated and experimental values

Estimation of beam length

The effective beam length which would perform the best at an applied voltage of 20 volts was estimated from the extrapolation of the experimental curve.

The slope of the experimental curve is calculated.

$\tan \theta = (250 - 200)\ \mu m / (65-56)$ volts

$\tan \theta = 50/9$

$\theta = \tan^{-1} (50/9) = 79^{\circ}$

Using the slope of the curve, the cantilever length for a voltage of 20 Volts is determined at the same deflection of 2μm.

Therefore,

$\tan 79^{\circ} = (L - 150)/(65-20)$

$L = 400\ \mu m$

Observed deviations of the experimental curve and the simulated curve could be due to the following reasons:

i) An important effect to be considered is the anisotropic etching of the cantilevers. The simulation assumes that the cantilevers have perfectly vertical walls. The etching was not completely anisotropic. The slope of the walls was 8°. This induces a $\cos\theta$ factor in the calculation of the capacitance. This $\cos\theta$ term lowers the capacitance generated to = 0. 98C. As $F = C^2V^2/2\varepsilon_0 A$, the capacitance term now is a square as a function of F. Also $\delta = FL^3/8EI$. Therefore the deflection is lowered by $\delta = 0.98\delta$

As we have assumed constant deflection of 2μm this deflection reduction factor is compensated by the simulation voltage Thus the simulated voltage increases to 61 volts.

ii) The voltage applied at the probe pad is not the same as the potential difference experienced by the cantilevers. This is because there is a drop in potential taking place along the length of the metal routing. This value of voltage drop is estimated as follows:

The length of the metal routing is ≈ 3000μm. The thickness of the routing is 0.5μm.

The resistivity of Al-Si-Cu is ≈ 3×10^{-8} Ω-m

Therefore using $r = \rho L/A$ we measure the resistance due to the routing which is

$= (3 \times 10^{-8}\ \Omega\text{-m}) \times (3000 \times 10^{-6})/(2 \times 0.5) \times 10^{-12} = 90\ \Omega$

The set constant current was 1 mA.

The voltage drop therefore is = 1mA * 90 Ω

Vd = 0.1 volts.

The actual voltage applied at the cantilevers is 58.9 volts instead of the simulated 60 volts. This value of 1.1 volts (including the first correction factor) is added to the simulation and this is "Correction Factor 1." A plot of the Correction Factor 1 included in the simulation versus experimental values is shown in figure 4.5.

iii) Another important effect to be considered is the parallality of the cantilevers. One of the cantilevers measured a sag of 0.1°. This results in the reduction of the effective area between the cantilevers. The calculations show that a 0.1° sag results in a reduction is force build up and deflection by 13% for a beam of length 150μm. As the length increases it is clear that for the same sag more area is lost. This 0.1° sag is considered and a second correction factor introduced in the simulation. This is detailed in Table 4.2 and figure 4.6

Table 4.2 Simulated values including correction factors

		Simulated Values (volts)		
Beam Length Micro meters	Experimental Values	Simulated Values	Correction Factor 1	Correction Factor 2
150	65	60	61.1	65
200	56	35	36.1	42
250	50	22	23.1	38

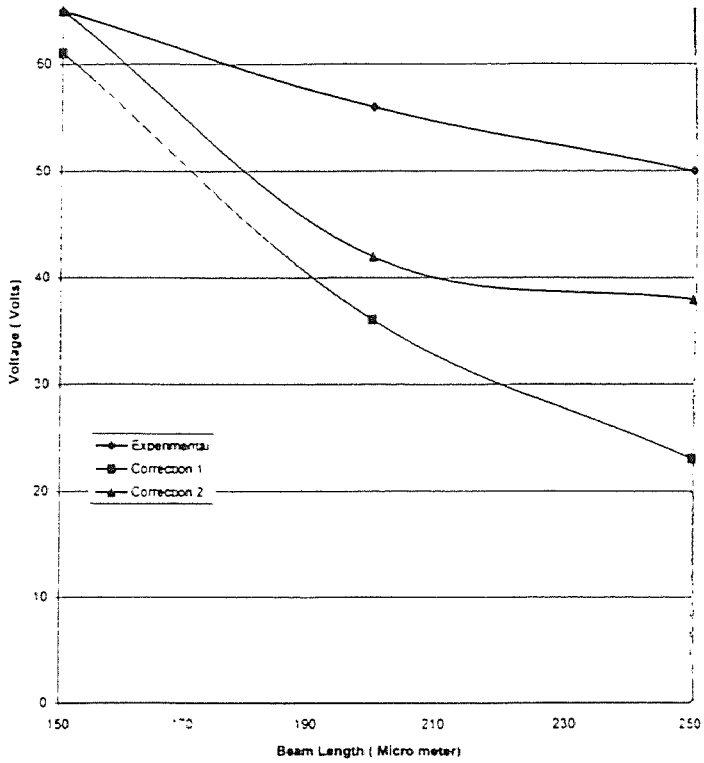

Figure 4.5 Graph of correction factors 1 and 2 considered to the simulated results versus the experimental results

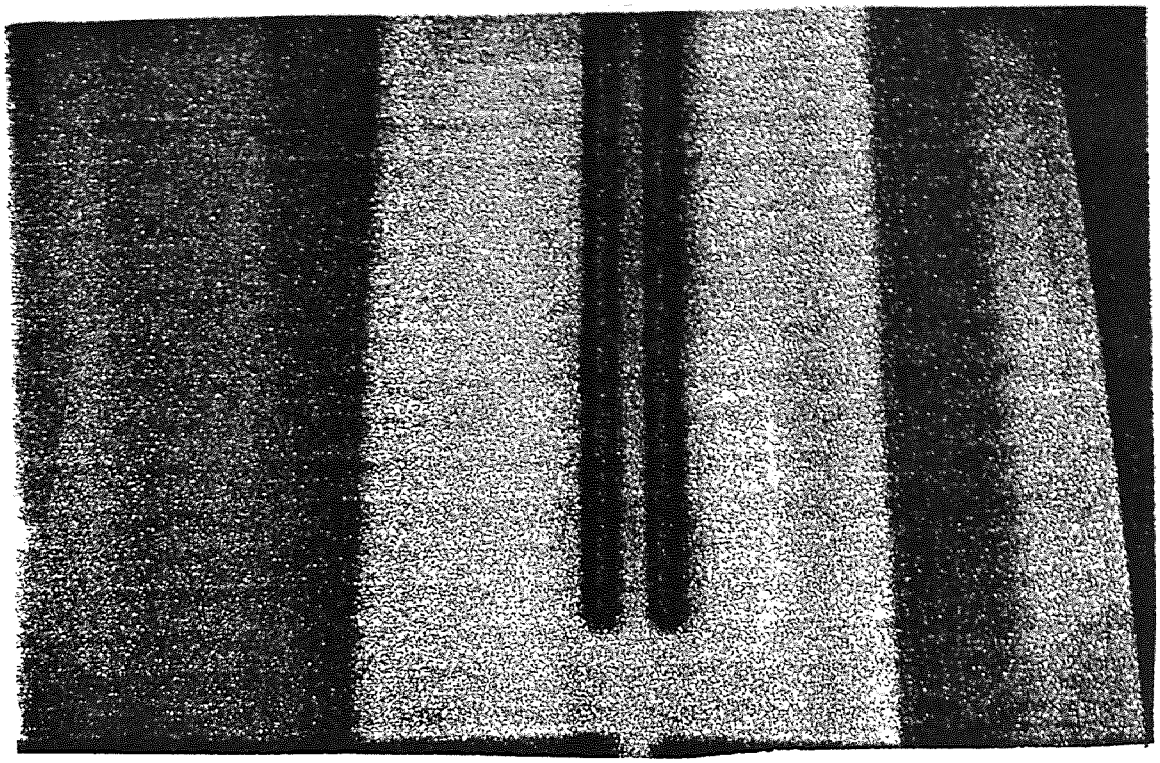

Figure 4.6 Original position of the cantilever

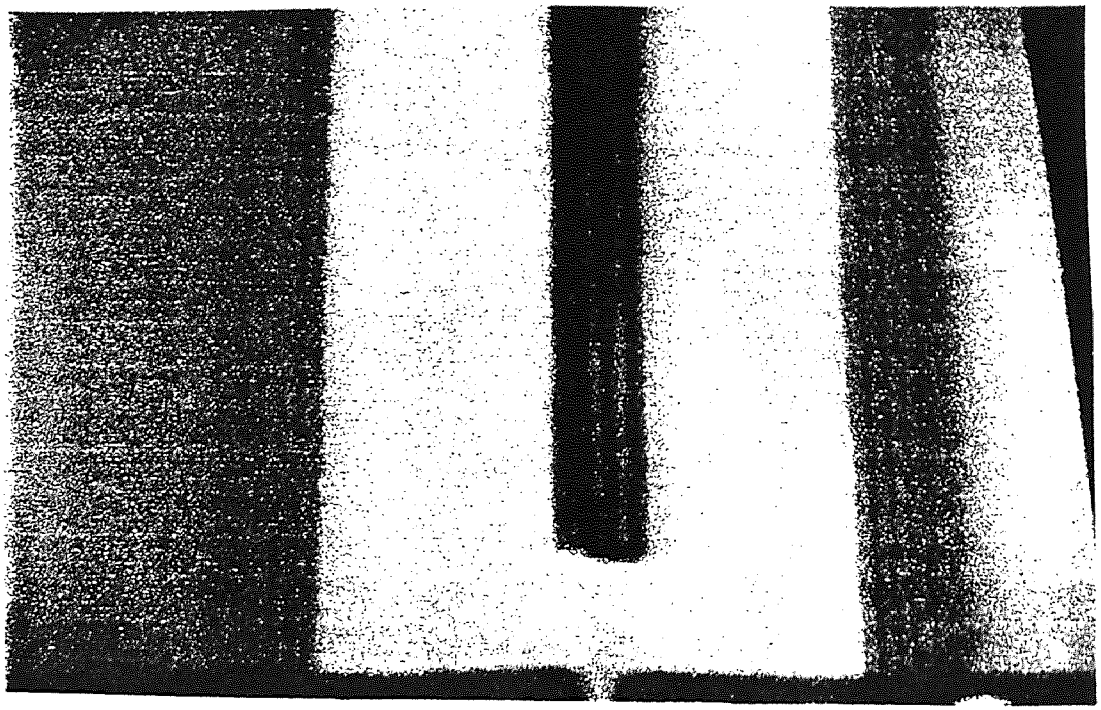

Figure 4.7 Deflected cantilevers on application of potential

CHAPTER 5

CONCLUSION

A novel sensor has been fabricated and characterized that could effectively be used to sense charges that are developed due to plasma non uniformity during the etching of polysilicon. This in turn could be used as an in-situ sensor to detect plasma induced damage to the oxide during gate definition. Plasma non uniformity is known to induce spatial voltage in the range of 10-20 volts. Present investigations carried out on a set of sensors indicate an optimized beam having length 200μm, width 2μm, thickness 1.6μm, separated from one another by 2μm will deflect by a maximum of 2μm for an applied voltage of 56 volts.

5.1 Future Scope

Present investigations indicate a length (μm) 150, 200, 250 deflect by 2μm at an applied voltage of 65 volts, 56 volts and 50 volts thereby agreeing with the fundamental operating principle. Incorporating possible corrections to the model shifts the simulated curve towards the experimental one. A a small, but finite deflection that would occur at an applied voltage of 20 volts could not be sensed due to limitations in the experimental set up. This deflection however has been predicted from the simulations. The gap between the cantilevers could be reduced to 1.6μm such that the cantilevers of length 200μm will deflect by 1.6μm at an applied potential of 20 volts. Precise monitoring of the deflection is essential to predict the spatial voltage fluctuations in the plasma chamber. This can be

achieved by measuring the shift in the diffraction pattern obtained by using a laser beam of suitable wave length on the cantilevers. Research guided by the above considerations are in progress in our laboratory.

APPENDIX A

Oxide Deposition and Reactor Description

A.1 LPCVD Reactor

The deposition reactor is schematically shown in the figure . This reactor was manufactured by Advanced Semiconductor Materials America Inc.(ASM America, Inc.) as a poly silicon micro-pressure CVD system. The horizontal reaction chamber consists of a 13.5 cm diameter fused quartz tube and a 144 cm long encapsulated with a three-zone, 10 kwatt, Thermco MB-80 heating furnace. The process tube door was constructed of a 300 series stainless steel, with a side hinge and sealed with an O-ring.

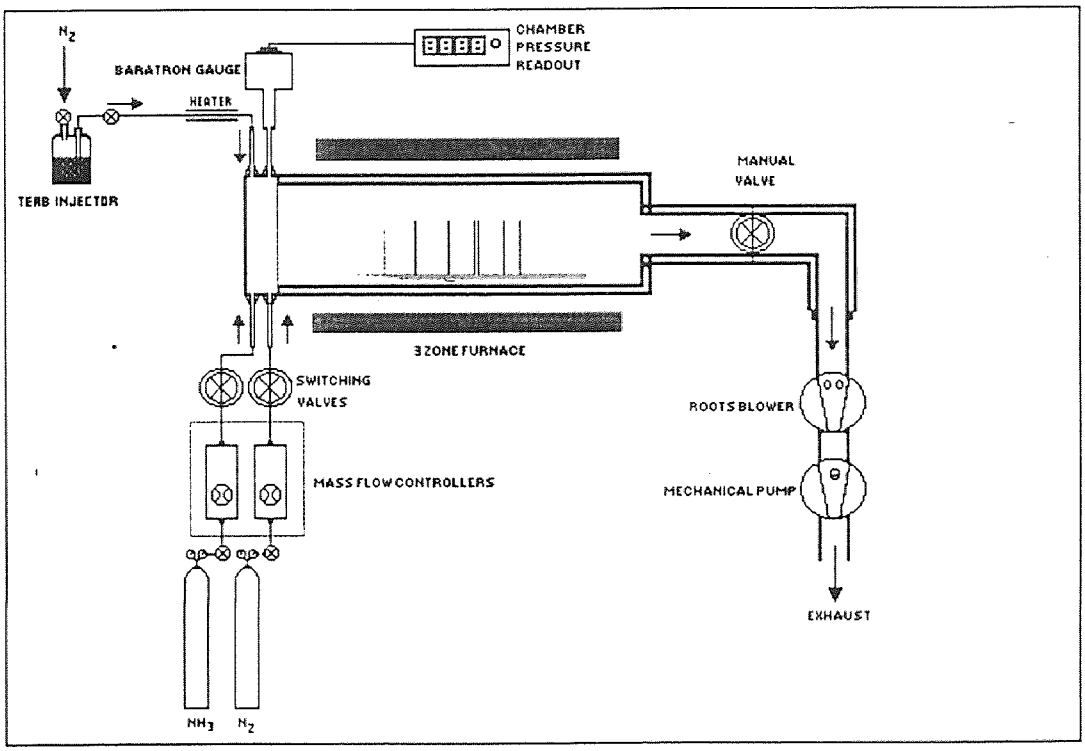

Figure A.1 Schematic representation of the LPCVD reactor

The flow of oxygen into the reaction chamber is controlled by a MKS mass flow controller. The other end of the reaction chamber is connected to a vacuum station comprised of a Leybold-Heraeus Trivac dual stage rotary vane pump backed by a Leybold-Heraeus roots pump to create the necessary vacuum in the system. An oil filter system is used to filter unnecessary particles from oil and thereby increasing the lifetime of the pump.

A.2Flow Chart showing the Oxide Deposition

Starting Material

(N-Type, 1-10 Ω-cm)

↓

Scribe Identification

(#1 - #12)All wafers were scribed so as to be easily distinguishable

↓

P-clean

5:1 H_2SO_4: H_2O_2

110^{O}C, 10minutes

↓

Rinse Hot DI Water

10 minutes

↓

Rinse Cold DI Water

5 minutes

↓

Spin Dry

↓

Furnace Pre-clean

100:1 H_2O:HF

1 minute

↓

Rinse Cold DI Water

10 minutes

↓

Spin Dry

↓

LPCVD LTO

Table A.1 Oxide deposition parameters

SiH_4	300sccm
O_2	7.5sccm
Temp	425°C
Pressure	500m Torr
Time	15 hours

.2 Oxide thickness measured at various points on the wafer

Reading #	Oxide Thickness (μm)
1	1.373
2	1.409
3	1.425
4	1.363
5	1.353
6	1.472
7	1.523
8	1.521
9	1.484
10	1.425
11	1.353
12	1.372
13	1.518

APPENDIX B

Mechanical Properties of Polysilicon

Mechanical Property	Value
Yield Strength	$7 * 10^{10}$ dyne/cm^2
Knoop Hardness	850 Kg/mm^2
Young's Modulus	$1.9 * 10^{12}$ dyne/cm^2

APPENDIX C

Polysilicon Deposition Methods and Conditions

C.1 Methods of Deposition of Polysilicon

Polysilicon can be deposited in a variety of ways and using many types of precursors.

APCVD : Atmospheric pressure chemical vapour deposition

LPCVD : Low pressure chemical vapour deposition

PECVD : Plasma enhanced chemical vapour deposition

Polysilicon occurs on occasion when the growing of single-crystal epitaxial silicon is attempted, and it will generally have large grain size. These occurrences are sporadic and undesirable. When polysilicon films are to be used in their own right, a uniform and generally small grain size is required, which usually implies a considerably lower deposition temperature than that used for epitaxy. Further, the applications themselves normally require relatively low-temperature depositions in order to minimize diffusion and /or wafer damage. Typically, low-pressure tube depositions with silane as the silicon source are now used. An LPCVD reactor provides for a very economical deposition and silane decomposition proceeds at temperatures as low as 400oC. When much thicker polysilicon layers are required-for example, in dielectrically isolated wafers speed of deposition, as well as an inexpensive feedstock is desirable, and the process used is much like that of high-temperature epitaxy.

The deposition rate of LPCVD polysilicon depends on temperature, silane partial pressure, and whether or not doping gas such as phosophine, arsine or diborane is present.

C.2 Flow Chart for Poly Deposition

P-clean

5:1 H_2SO_4:H_2O_2

110°C

10 minutes

↓

Rinse Hot DI

10 minutes

↓

Rinse Cold DI

5 minutes

↓

Spin Dry

↓

Deposit Polysilicon

Target thickness = 1.5μm

Table C.3 Polysilicon deposition conditions

$Si H_4$	300sccm
Pressure	400m Torr
Temp	600oC
Time	15 hours

APPENDIX D

Polusilicon Doping Conditions

D.1 Flow Chart for Poly Doping

P-clean

5:1 H_2SO_4:H_2O_2

110°C

10 minutes

↓

Rinse Hot DI

10 minutes

↓

Rinse Cold DI

5 minutes

↓

Spin Dry

↓

Phosphorus Diffusion

Table D.2 Polysilicon diffusion conditions

N_2	2 sccm
Temp	950oC
Time	1 Hour

APPENDIX E

Evaporation and Sputtering Process and Conditions

E.1 Evaporation

Evaporation of a metal source is performed by heating the metal in an evacuated chamber. A vacuum of 10^{-6} - 10^{-7} torr is required to reduce the collisions of evaporants and the residual gas molecules on their way to the wafers that are placed at a certain distance from the metal source. At such pressures, the mean-free path of molecules is greater than the distance between source and substrate. Residual gas molecules not only deflect evaporants from their straight-line trajectories but can also react with the growing metal film, contaminating it. The rate of evaporation, Ns, from the source is proportional to the equilibrium partial pressure of the metal at evaporation temperature. The wafer is maintained below 250^0C during evaporation. At such temperatures evaporation from the substrate is negligible and the substrate deposition rate is proportional to the source evaporation rate, depending only on the geometry of the evaporation system. If the source is a small crucible placed at the center of a hemisphere (dome) on which the wafers are mounted the substrate deposition rate, D, is defined as $D = R_t / 2 \pi r^2$ where r is the sphere radius and Rt the rate of mass loss from the metal source.

Source heating methods include resistive, induction, e-beam and laser heating. The metal is placed in a non-reactive crucible, typically of boron nitride or a refractory metal. In many applications, different materials are evaporated simultaneously to form a

composite film, such as Al-Cu. Because of the different vapour pressures of the components, separate sources are used and individually controlled to yield the desired composition.

E.2 Step Coverage

In evaporation systems, metal atoms follow essentially straight-line paths from source to wafer. Because of this directionality, shadowing of various degrees is observed in the presence of large steps in patterned films on the wafer. This causes the metal to be thin along shadowed step edges and can seriously degrade the yield and reliability of metal interconnects. An extreme case of discontinuity is shown in figure 3.7. One method of reducing the effect of shadowing is to rotate the wafer holder (dome) in two directions and achieve more uniform coverage for a large number of wafers. Another method is to taper edges of steps and opening, however, at the cost of increasing the metal pitch. Although there are step coverage problems with sputtered films, they tend to be less severe than with evaporated films. Due to the conformal nature of chemical vapor deposition, step coverage is usually not a problem with CVD metal films.

E.3 Sputtering

While evaporation is widely used to deposit aluminum and its alloys, sputtering of these materials has become more practical because of the increased deposition rate and more uniform step coverage and contact hole filling. Also, when refractory metals are used, either sputtering or CVD is required to achieve realistic throughput in manufacturing.

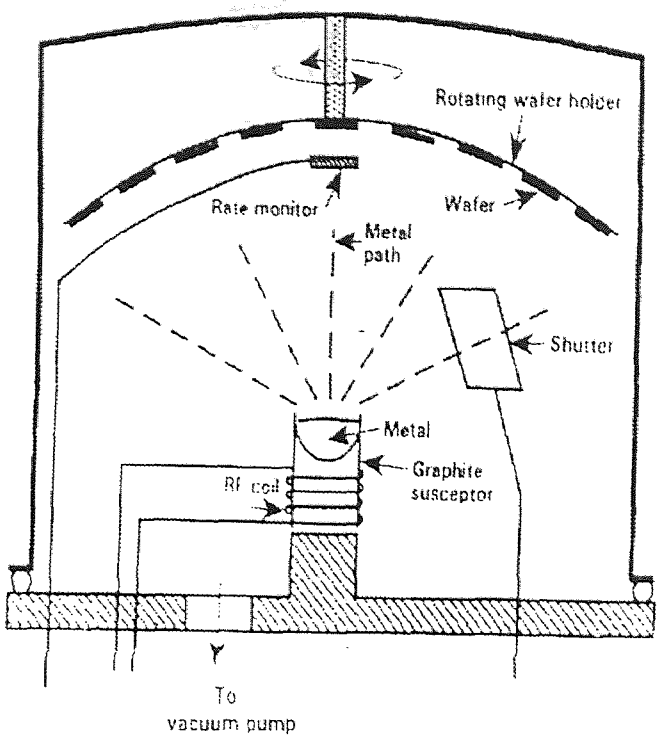

Figure E.1 Schematic of a typical spherical radio-frequency evaporation system

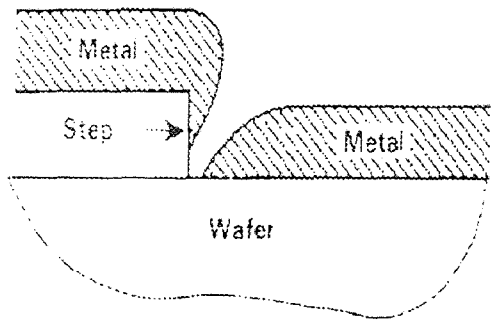

Figure E.2 Metal discontinuity over step caused by shadowing in an evaporation system

Sputter is similar to a billiard-ball event. Ions are accelerated in an electric field toward a target of material to be deposited, where they 'knock-off' (sputter) target atoms. Refer figure E.3. The sputtered ions then deposit onto wafers which are conveniently placed facing the target. Argon is typically used for sputtering because it is inert and readily available in pure form. It is ionized by colliding with high electrons in the

chamber, and then accelerated in an electric field toward the negatively biased target. The momentum of ions incident on the target is then transferred to surface atoms of the target material, causing their ejection. Therefore, during sputter deposition, material is removed from the target and deposited onto the wafers.

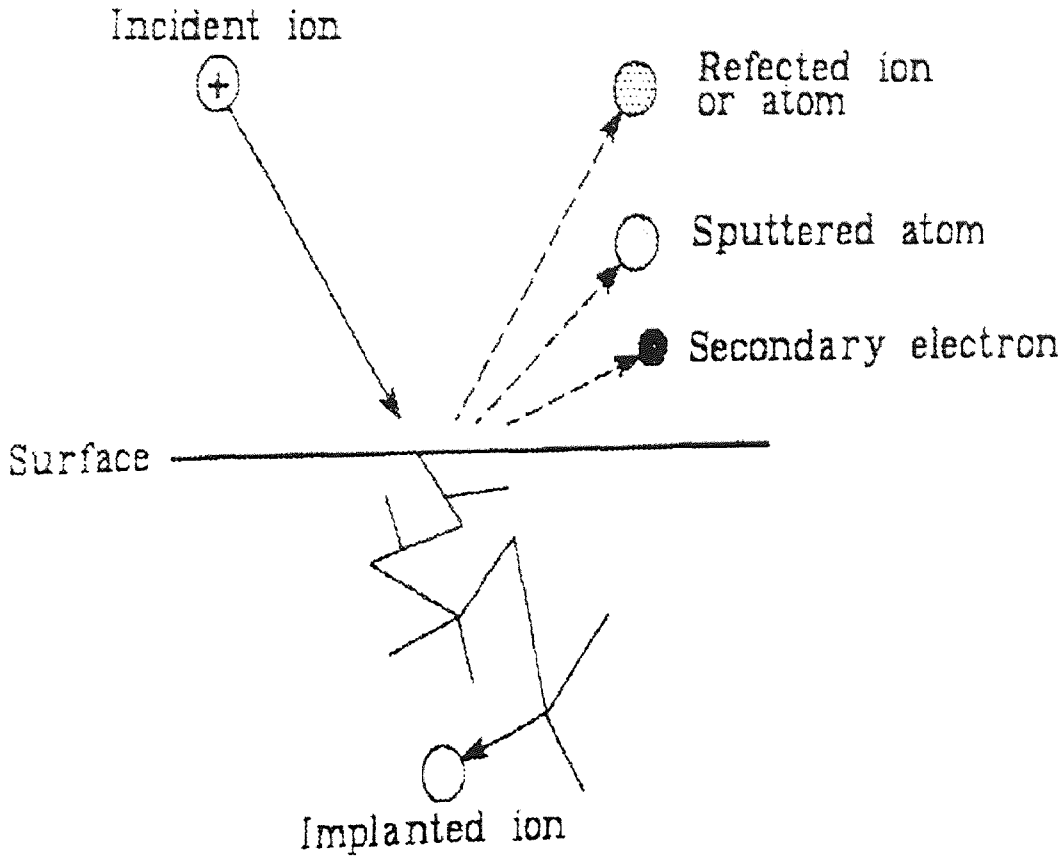

Figure E.3 The sputtering process

The incident energy must be large enough to dislodge target atoms, but not too large to cause penetration into the target material (ion implantation). Typical sputtering ion energies range from 500-5000 eV. The number of atoms sputtered from the wafer surface

per incident ion is defined as the sputter yield. This number varies from 0.5-1.5, depending on the momentum of ions and their angle of incidence.

There are many types of sputtering. They are :

a) Ion beam sputtering

b) Magnetron sputtering

c) Reactive sputter deposition

d) Bias sputter deposition

e) Collimated sputter deposition

E.4 Flow Chart Showing the Sputter Deposition Process

P-clean

5:1 H_2SO_4:H_2O_2

110°C

10 minutes

↓

Rinse Hot DI

10 minutes

↓

Rinse Cold DI

5 minutes

↓

Spin Dry

↓

Deposit Aluminum

↓

Measure sheet resistivity

Table E.1 Sputter deposition of metal

Parameters	Values
Base pressure	8×10^{-7} torr
Temperature	300^{o}C
Deposition rate	10 A^{o}/min
Thickness	5000 A^{o}

APPENDIX F

Sacrificial Oxide Etch

F.1 Process steps followed for the Sacrificial Etch

Buffered HF (7:1)

(9 minutes and 30 seconds)

↓

Wash in DI water

↓

Wash in M-Pyrol

(2 minutes)

↓

Heat on hot plate

(120°C)

APPENDIX G

Photoresist Terminology and Lithography

G.1 Basic Photoresist Terminology

The basic steps of the lithographic process are shown in the figure. The photoresist (PR) is applied as a thin film to the substrate(e.g. SiO_2 on Si), and subsequently exposed through a mask. The mask contains clear and opaque features that define pattern to be created in the PR layer. The areas in the PR exposed to light are made either soluble or insoluble in a specific solvent known as developer. In the case when irradiated (exposed) regions are soluble, a positive image of the mask is produced in the resist. Such material is therefore termed a positive photoresist. On the other hand, if the non irradiated regions are dissolved by the developer, a negative image results. Hence the resist is termed a negative resist. Following development, the regions of SiO_2 no longer covered by resist, are removed by etching, thereby replicating the mask pattern in that oxide layer.

The resist is seen to perform two roles in this process. First, it must respond to exposing radiation in such a way that mask image can be replicated in the resist. Second, the remaining areas of resist must protect the underlying substrate during subsequent processing. In fact the name resist evolved from the ability to resist etchants.

Although both negative and positive resists are used to manufacture semiconductor components, the higher resolution capabilities of positive resists have virtually made them exclusive choice for VLSI applications. Conventional positive

optical lithographic processes and resists are capable of producing images on VLSI substrates with dimensions as small as 0.8-1.5μm. For submicron features, however, diffraction effects during exposure may ultimately cause other higher resolution techniques to replace optical lithography

G.2 Description of Lithographic Process

The first step in this process is the application of photoresist. The photoresist is applied by spin coating technique. This procedure involves three stages : a)dispensing the resist solution onto the wafer; b) accelerating the wafer to the final rotational speed; and c) spinning at a constant speed to establish the desired thickness (and to dry the film).

The dispensing stage can either be accomplished by flooding the entire wafer with resist solution before the beginning the spinning, or by dispensing a smaller volume of resist solution at the center of the wafer and spinning at lower speeds to produce a uniform liquid layer across the wafer.

In the next stage the wafers are normally accelerated as quickly as is practical to the final spin speed and finally spinning at the constant speed to obtain desired thickness.

In this work the rotational speed was maintained at 1500 rpm. The wafers were spun at this speed for a period of 20 seconds. This gave a photoresist of 2μm thickness. Prior to exposure the wafers are baked for one minute at 115°C or for a period of 20 minutes in an air oven maintained at the same temperature in order to remove the moisture present. The baking is done to remove the moisture from the wafer. Moisture can reduce the adhesion.

The exposure was carried out using a SUSS MA6 mask aligner. The lamphouse is equipped with a 350 W mercury high pressure lamp and a SUSS diffraction reducing optics. The usable wavelength falls between 350-450 nm. The lamphouse has an ellipsoidal mirror, and a 45° cold light mirror. The type of exposure lamp depends on the optical range selected. The cold light mirror reflects the desired short wavelength UV light through a fly's lens and transmits the longer wavelengths to a heat sink located in the bottom of the lamphouse. The lamphouse also contains a condenser lens, diffraction reducing lens plates, a 45° turning mirror and a collimation lens. A holder is provided in the mirror house for a filter. SUSS diffraction reducing exposure system provides a high resolution over the entire exposure area, resulting in steep resist edges and small diffraction effects.

The wafers were exposed for 20 seconds in the SUSS MA6 mask aligner. After the exposure the wafer must undergo "development" in order to leave behind the image which will serve as a mask for etching. The developer is poured on the wafer and allowed to develop for 30 second before it is spun at a high rpm(~2000-3000). This procedure is repeated for another 10 seconds of development. The wafer is then washed with DI water and spun again to remove all the water. The wafers are baked as before to rid of the moisture that may been absorbed by the substrate. The windows are then inspected under the microscope for their integrity.

APPENDIX H

Etching

H.1 Etching

In general etching process is not completely attainable. That is etching process are not capable of transferring the pattern established by protective mask into the underlying material. Degree to which the process fail to satisfy the ideal is specified by two parameters: bias and tolerance. *Bias* is the difference between the etched image and mask image. *Tolerance* is a measure of statistical distribution of bias values that characterizes the uniformity of etching.

The rate at which material is removed from the film by etching is known as etch rate. The units of *etch rate* are Å/min, μm/min, etc. Generally high etch rates are desirable as they allow higher production throughputs, but in some cases high etch rates make the control of lateral etching a problem. That is since material removal can occur in both horizontal and vertical directions, the horizontal etch rate as well as vertical etch rate may need to be established in order to characterize an etching process. The lateral etch ratio, L_R, is defined as the ratio of the etch rate in a horizontal direction to that in a vertical direction. Thus:

$$L_R = \frac{\text{Horizontal etch rate of material}}{\text{Vertical etch rate of material}}$$

In the case of an ideal etch process the mask pattern would be transferred to the underlying layer with a zero bias. This would then create a vertical edge of the mask. Therefore the lateral etch rate would also have to have been zero. For nonzero L_R, the film material is etched to some degree under the mask and this effect is called undercut. When the etching proceed in all directions at the same rate, it is said to be *isotropic*.

By definition, however, any etching that is not isotropic is anisotropic. If etching proceeds exclusively in one directions (e.g. only vertically), the etching process is said to be completely *anisotropic*. A typical anisotropic etch profile is shown in the figure.

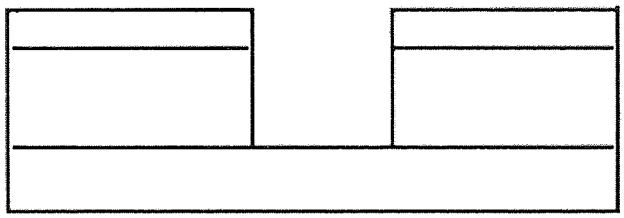

Figure H.1 Anisotropic etch profile

So far it has been assumed that the mask is not attacked by the etchant and did not consider that the layers under the etched film can also be attacked by the etchant. In fact both the mask and the underlying layer materials are generally etchable, and these effects may play a significant role in specifying etch processes. The underlying material subject to attack may either be the silicon wafer itself, or a film grown or deposited during a previous fabrication step. The ratio of the etch rates of different materials is known as

selectivity of an etched process. Thus both the selectivity with respect to the mask material ands the selectivity with respect to the substrate materials are important characteristics of an etch process.

H.2 Wet Etching Technology

Wet etching processes are generally isotropic. They are inadequate for defining features less than 3μm. Nevertheless for those processes that involve patterning of linewidths greater than 3μm, wet etching continues to b a viable technology.

The reason wet etching has found widespread acceptance in micoelectronic fabrication is that it is a low cost, reliable, high throughput process with excellent selectivity for most etch process with respect to both mask and substrate materials.

In general wet etch processes can be broken down into three steps:

- diffusion of the reactant to the reacting surface
- reaction
- diffusion of reaction products from the surface.

The second step can obviously be further differentiated into adsorption prior to, and desorption subsequent to, the actual reaction step. The slowest of the steps will be rate controlling. That is, the rate of that step will be the rate of the overall reaction.

Chemical etching can occur by several processes. The simplest involves dissolution of the material in a liquid solvent without any change in the chemical nature of the dissolved species. Most etching process, however, involve one or more chemical reactions. Various types of reactions my take place, although one commonly encountered

in semiconductor fabrication is oxidation-reduction (redox). That is, a layer of oxide is formed, then the oxide is dissolved and the next layer of oxide is formed, etc.(e.g. wet etching of Si and Al)

In semiconductor applications, wet etching is used to produce patterns on the silicon substrate or in thin films. A mask is typically used to protect desired surface regions from the etchant and this mask is stripped after the etching has been performed. Thus, when choosing a wet etch process, in addition to selecting an etchant, a suitable masking material must be picked to have good adhesion to the underlying films, good coating integrity and ability to withstand attack by etchant. Photoresist is the most commonly encountered masking layer, but sometimes it falls short in this role. Problems involved include loss of adhesion at the edge of the mask-film interface due to etchant attack, and large area failure of the resist. Large area failures of the resist are usually due to differential stress buildups in the substrate and mask layers. Also bubble formation during etching process can lead to poor pattern definition, particularly at the pattern edges.

Wet etching, particularly in MEMS plays a crucial role in that it almost always is used to release structures that are previously defined by RIE. In our case wet etching was used to release the cantilever structures.

H.3 Dry Etching

Wet etching processes are typically isotropic, therefore if the thickness of the film being etched is comparable to the minimum pattern dimension, undercutting due to isotropic

etching becomes intolerable. One alternative pattern transfer method that offers the capability of non isotropic(or anisotropic) etching is "dry etching". As a result, considerable effort has been expended to develop dry etch processes as replacements for wet etch processes.

The overall goal of an etch process, as mentioned earlier, is to able to reproduce the features on the mask with fidelity. This should be achievable together with control of following aspects of etched features:

- the slope of the feature sidewalls(e.g. the slope of the sidewalls of the etched feature should have the desired angle, in some cases vertical)
- the degree of undercutting(i.e. usually the less undercutting the better)

There are a variety of dry etch processes. The mechanism of etching in each type of process can have a physical bias(e.g. glow-discharge sputtering), a chemical bias(e.g. plasma etching), or a combination of the two(e.g. reactive ion etching, RIE, and reactive ion beam etching RIBE).

In processes that rely predominantly on the physical mechanism of sputtering(including RIBE), the strongly directional nature of the incident energetic ions allows substrate material to be removed in a highly anisotropic manner(i.e. essentially vertical etch profiles are produced). Unfortunately such material mechanisms are non selective against both masking material and materials underlying the layers being etched. That is, the selectivity depends largely on sputter yield differences between materials. On the other hand purely chemical mechanisms for etching can exhibit very high selectivity's against

both mask and underlying substrate material. Such purely chemical etching mechanisms, however, typically etch in an isotropic fashion.

By adding a physical component to a purely chemical etching mechanism, however the shortcomings of both sputter based and purely chemical dry etching process can be surmounted. Plasma etching process is a purely chemical process and reactive ion etching processes is a physical/chemical process.

The basic concept of plasma etching is rather direct. A glow discharge is utilized to produce chemically reactive species from a relatively inert molecular gas. The etching gas is chosen so as to generate species which react chemically with the material to be etched, and whose reaction product is volatile. An ideal dry etch process based solely on chemical mechanisms for material removal, can thus be broken down into six steps:

- reactive species are generated in a plasma
- these species diffuse to the surface of the material being etched
- the species are adsorbed on the surface
- a chemical reaction occurs with the formation of a volatile by product
- the by product is desorbed from the surface
- the desorbed species diffuse into the bulk of the gas

If any of these steps fail to occur, the overall etch process ceases. Many reactive species can react rapidly with a solid surface, but unless the product has a reasonable vapor pressure so that desorption occurs, no etching takes place. Reactive ion etching as described before is an anisotropic etching technique. After the lithographic step, windows

are formed on the photoresist layer. The silicon nitride is exposed in these windows. RIE is carried out to remove this silicon nitride and expose the underlying silicon substrate.

H.4 Description of the Reactor for RIE

Plasma etching systems consist of several components: a) an etching chamber, that is evacuated to reduced pressures; b) a pumping system for establishing and maintaining the reduced pressure; c) pressure gauges to monitor the pressure in the chamber; d) a variable conductance between the pump and etching chamber so that the pressure and flow rate in the chamber can be controlled independently; e) an RF power supply to create the glow discharge; f) a gas handling capability to meter and control the flow of reactant gases; and g) electrodes. There are several types of commercially available etching systems. They include

1. barrel reactors
2. "downstrem" etchers
3. parallel-electrode(planar) reactor etchers
4. stacked parallel-electrode etchers
5. hexode batch etchers
6. magnetron ion etchers

The RIE system in the class 10 clean room, where the fabrication of the V grooves was carried out, is a stacked parallel electrode etching system.

The stacked parallel electrode etcher is a small batch machine capable of handling 6 wafers at a time. Its unique design provides an individual pair of electrodes for each

wafer thereby combining some of the advantages of a single wafer and batch etchers. Operating chamber pressures and RF power densities can be kept in the ranges between those of low pressure, low power density hexode batch etchers, and high pressure.

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