Summer 8-31-1999

Study of the effects of deuterium implantation upon the performance of thin-oxide CMOS devices

Sumit Kishore
New Jersey Institute of Technology

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ABSTRACT

STUDY OF THE EFFECTS OF DEUTERIUM IMPLANTATION UPON THE PERFORMANCE OF THIN-OXIDE CMOS DEVICES

by
Sumit Kishore

The use of ultra thin oxide films in modern semiconductor devices makes them increasingly susceptible to damage due to the hot carrier damage. Deuterium in place of hydrogen was introduced by ion implantation at the silicon oxide-silicon interface during fabrication to satisfy the dangling bonds. Deuterium was implanted at energies of 15, 25 and 35 keV and at a dose of $1x10^{14}/cm^2$. Some of the wafers were subjected to N_2O annealing following gate oxide growth. It was demonstrated that ion implantation is an effective means of introduction of deuterium. Deuterium implantation brings about a clear enhancement in gate oxide quality by improving the interface characteristics. N_2O annealing further improves device performance. A reduction of electron traps with deuterium was also observed. A combination of deuterium implantation at 25 keV and a dose of $1x10^{15}/cm^2$, followed by annealing in N_2O was observed to have the most positive influence on device behavior.

Concurrently, MEMS microheaters being fabricated for an integrated VOC sensor were also tested for their temperature response to an applied voltage. Different channel configurations and materials for the conducting film were compared and the best pattern for rapid heating was identified. Temperature rises of upto 390 °C were obtained. The temperature responses after coating spin-on glass in the microchannels were also measured.

STUDY OF THE EFFECTS OF DEUTERIUM IMPLANTATION UPON THE PERFORMANCE OF THIN-OXIDE CMOS DEVICES

by
Sumit Kishore

A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Chemical Engineering

Department of Chemical Engineering, Chemistry and Environmental Science

August 1999

APROVAL PAGE

STUDY OF THE EFFECTS OF DEUTERIUM IMPLANTATION UPON THE PERFORMANCE OF THIN-OXIDE CMOS DEVOCES

Sumit Kishore

Dr. Durgamadhab Misra, Thesis Advisor — Date
Associate Professor,
Department of Electrical and Computer Engineering, NJIT

Dr. Somenath Mitra, Committee Member — Date
Associate Professor of Chemistry,
Department of Electrical and Computer Engineering, NJIT

Dr. Norman W. Loney, Committee Member — Date
Associate Professor of Chemical Engineering,
Department of Electrical and Computer Engineering, NJIT

BIOGRAPHICAL SKETCH

Author: Sumit Kishore

Degree: Master of Science

Date: August 1999

Undergraduate and Graduate Education:

- Master of Science in Chemical Engineering
  New Jersey Institute of Technology, Newark, New Jersey, 1999

- Bachelor of Technology (Honors) in Chemical Engineering,
  Indian Institute of Technology, Kharagpur,
  Kharagpur, India 1997

Major: Chemical Engineering

Presentations and Publications:

S. Kishore and D. Misra, "Thin-Gate Oxides Grown on Light Deuterium Implanted Silicon Substrate", *Poster Session, Electrochemical Society 195th Meeting*, Seattle, WA, May 1999.

ACKNOWLEDGMENT

I would like to express my deep sense of gratitude to Dr. Durgamadhab Misra for his constant guidance, support and encouragement throughout the research.

My special thanks to Dr. Somenath Mitra for participating on my thesis committee and for his invaluable assistance regarding this project and otherwise, throughout the duration of this project.

I would like to take this opportunity to extend my sincere gratitude to Dr. Norman W. Loney for serving on my thesis evaluation committee. I would also like to thank Dr. Dentcho Ivanov and Ken O' Brien for assisting me throughout my work in the cleanroom.

Finally, my thanks to Pradnesh, Minhee, Jason, Kevin and Narahari for their invaluable help at various times during the project.

This thesis is dedicated to my parents

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CHAPTER 1

INTRODUCTION

1.1 Overview

The trend in electronics is towards continuous scaling down of semiconductor devices into the submicrometer range. This in turn calls for the use of very thin gate oxides in these devices. For most MOS (**M**etal **O**xide **S**emiconductor) applications, the primary dielectric is silicon dioxide. The reliability of very thin gate oxides thus becomes an important concern. The smaller thickness of these oxide films results in higher operating fields and larger direct-tunneling currents. Also, very thin oxides have a higher tendency towards anomalous degradation and quasi- to soft breakdown.

The performance and characteristics of MOSFET (**MOS F**ield **E**ffect **T**ransistor) devices, containing an oxide layer as an integral part of the device, are intimately related to the nature of the silicon-silicon oxide interface. This interface represents the transition from the tetrahedral structure of silicon to the polyhedral structure of silicon dioxide. The interface is commonly characterized by a number of dangling bonds, because they represent positions in the silicon lattice where the silicon valencies are unfulfilled. These dangling bonds degrade the performance of the device. There also exist at the interface a number of charged states due to fixed and mobile charges. All of these result in undesirable behavior of thin-gate oxides, particularly under conditions of high current, voltage or temperature stress.

In general, during device fabrication a number of steps are taken to reduce the defects associated with the oxide-silicon interface and the oxide film itself. Commonly, the number of dangling bonds is reduced by annealing the device in a hydrogen ambient, usually forming gas, following oxide growth. The hydrogen atoms diffuse through the silicon dioxide to take up positions in the crystal lattice represented by dangling bonds.

Annealing the devices in a nitrogen ambient also has been observed [*1*] to reduce the number of fixed and mobile charges associated with the oxide. Heat treatment in a nitrogenous ambient leads to improved stoichiometry at the interface. Nitrogen incorporated in the oxide also serves to act as a barrier against the movement of dopant impurities into the oxide.

Recent studies [*2,3,4*] have included the investigation of ion implantation as opposed to heat treatment as a method of introduction of nitrogen into the silicon oxide lattice. Implantation offers a better way to introduce low doses of species into the body of the device with greater control over the concentration profile, and does not require the high temperatures required for diffusion. In other studies [*5,6,7,8*], nitrous oxide (N_2O) has been used during annealing in place of ammonia.

The use of deuterium [*9,10*] in place of hydrogen in annealing to reduce the number of dangling bonds has also been the subject of recent study. The larger mass of deuterium compared to hydrogen makes it more difficult to remove it from place under hot electron bombardment. However, it is necessary to anneal the wafers in deuterium ambient for hours to see any significant result in integrated circuits with multilevel dielectric/metallization layers [*10*]. This happens because deuterium is heavier than

hydrogen and the shadowing effect of multilevel metallization can make it really difficult for deuterium to reach the gate-oxide/silicon interface.

1.2 Objective

This thesis seeks to investigate the characteristics of thin gate oxide MOS devices with oxide grown on the silicon substrate upon implantation of deuterium into the substrate, in order to observe its effect on device performance and lifetime. The study takes the following novel approaches:

(a) the use of deuterium to reduce the number of dangling bonds at the silicon dioxide-silicon interface.

(b) implantation as opposed to annealing as a method of introduction of the deuterium at the interface.

(c) to combine these studies with the use of an ultra-thin (40 Å) gate oxide.

This thesis deals with the fabrication and testing of thin oxide MOS capacitors to establish the appropriate implantation process for incorporation of deuterium for this purpose.

The aim of this thesis was to fabricate the test structures to evaluate the behavior of thin gate oxides grown on silicon substrate implanted with deuterium. For this purpose, MOS capacitors of varying surface areas were fabricated on lightly doped silicon wafers. Different implantation energies of deuterium were tried out to arrive at the optimum energy level. To compare the results obtained with those resulting from annealing in nitrous oxide, wafers with and without deuterium implanted on them were annealed in

nitrous oxide ambient. A control wafer without deuterium or N_2O annealing was also prepared.

This and the following chapter present a general idea of MOS devices, the nature of the silicon dioxide-silicon interface and the problems associated with the oxide film in these devices. A literature review is also presented. The third chapter describes in detail the various process steps used in the fabrication of the device. The fourth chapter presents the results obtained from the tests carried out on the wafers. The fifth chapter summarizes the conclusions from the tests. The simulations carried out for the experiment are reported in the appendix.

The process was simulated using SRIM and SUPREM IV. The fabrication was carried out in the cleanroom at the Microelectronics Research Center, NJIT. The device was tested using HP4140 and HP4145B Semiconductor Parameter Analyzer to evaluate device parameters.

This project was carried out simultaneous with another project, involving the fabrication of a MEMS heater as part of a larger project on the construction of semiconductor microsensor for detection of organic molecules, in which the author was an active participant. The final chapter presents the background of and discusses the results obtained for that project.

CHAPTER 2

BACKGROUND

2.1 Overview of CMOS Technology

Over the past decade, Metal-Oxide-Semiconductor (MOS) technology has played an increasingly important role in the global integrated circuit industry. This is because of a number of reasons: their self-isolation makes it easy to place devices side-by-side on a chip; they can be made considerably smaller than their bipolar counterparts; they can be made in bulk silicon, thus avoiding costly epitaxial growth; they require lesser process steps and they have lower power dissipation. For a combination of these reasons, MOS technology is a prime candidate for large-scale integration purposes in device fabrication.

Silicon forms the basic starting material for a large class of integrated circuits. A MIS (**M**etal-**I**nsulator-**S**emiconductor) structure is created by superimposing several layers of conducting, insulating, and transformer-forming materials to create a sandwich-like structure. These structures are created by a series of chemical processing steps involving oxidation of silicon, introduction of impurities into the silicon to give it certain conduction characteristics, and deposition and etching of aluminum (or other conducting material) on the silicon to provide interconnections. Of the various insulating films used in MIS devices, by far the most important is silicon dioxide, so that the name MOS is extensively used for MIS devices utilizing silicon dioxide as the insulator, and the silicon dioxide is commonly referred to as gate "oxide" only.

After the fabrication steps, the typical MOS structure includes distinct diffusion (doped silicon), polysilicon and aluminum layers, separated by layers of insulating material i.e. oxide.

Physically, a typical MOS transistor consists of regions of heavily doped semiconductor formed in lightly doped semiconductor substrate. The dopant impurities in these regions, called the source and drain respectively, and the substrate are of the opposite types. The source and drain are separated on the surface by the insulating layer. If the substrate is p-doped (excess holes) and the source and drain regions are n-doped (excess electrons), an n-type transistor is formed. With the opposite doping, a p-type transistor results. The structure of an nMOS transistor is shown in Fig. 2.1.

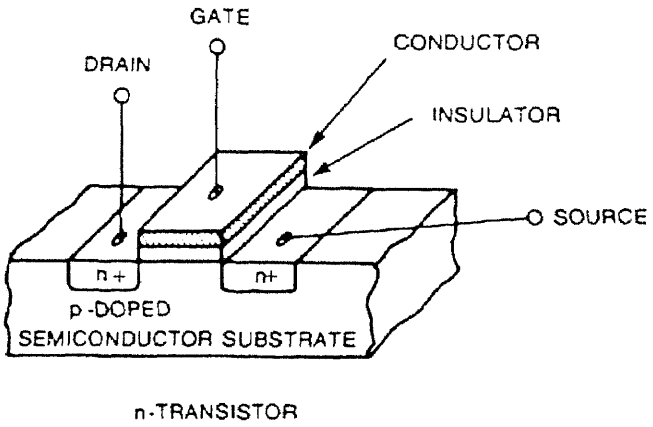


Fig 2.1 nMOS Transistor Structure

A CMOS (Complementary Metal Oxide Semiconductor) transistor is formed by laying an n-type and a p-type transistor side-by-side on the same wafer.

2.2 MOS Capacitors

The core of the MOSFET is the sandwich of metal, silicon dioxide insulator, and silicon semiconductor. This sandwich behaves electrically like a capacitor. While the actual transistor behavior of the MOSFET depends on the channel formed between the source and drain in the semiconductor, and the voltages applied at the gate and the source/drain, the behavior of this metal-oxide-semiconductor sandwich is crucial to the performance and lifetime of the device. For this reason, the MOS capacitor is the subject of much materials research. Accordingly, the current project focussed on the fabrication and testing of MOS capacitors, with the aim of possible extension of results obtained to transistors. As discussed later, a number of tests evaluate and characterize the quality of the oxide in terms of the behavior of this capacitor.

2.3 Oxide Formation

The surface of silicon is covered at all times by a layer of silicon dioxide. This is true even of freshly cleaved silicon, which upon exposure to air gets covered with a few monolayers (≈15-20 Å) of oxide, and gradually thickens with prolonged exposure to an upper limit of about 40 Å. Most silicon microcircuit applications require much thicker oxide films. These oxide films are grown on the wafer by maintaining it in an elevated temperature in an oxidizing ambient, usually dry oxygen or water vapor.

Wet oxidation processes are in general more rapid, but result in relatively low-density silicon dioxide films. The use of live steam leads to poor grades of oxides. Hence wet oxidation is usually accomplished by flowing a carrier gas, generally oxygen or an

inert, through a water bubbler whose temperature is maintained below the boiling point to prevent its undue depletion.

Oxides grown in dry oxygen are extremely dense, and have a relatively low concentration of traps and interface states. Consequently, gate oxides for MOS-based circuits are exclusively made by this process.

2.4 Silicon Dioxide-Silicon Interface

The exact nature of the Si-SiO_2 interface is not completely understood. A somewhat simplified picture of the interface, formed as a result of thermal oxidation, is a single-crystal silicon followed by a monolayer of SiO_x, i.e. incompletely oxidized silicon, then a strained region of SiO_2 roughly 10~40 Å deep, and the remainder stoichiometric, strain-free, amorphous SiO_2.

In an ideal MOS device the oxide film is assumed to have zero conductance because of the absence of any charge carriers. However, for any practical MOS diode, interface traps and oxide charges will exist at the interface, which will, one way or the other, affect the ideal MOS characteristics. They could cause a shift in the normal transistor characteristics with repeated use, or reduce the lifetime of the device, or begin conducting under conditions of strong electric fields or high currents. Some of the primary defects associated with the oxide film leading to degradation in performance are discussed here. The phenomena which lead to anomalous behavior under stressed conditions are also presented.

2.4.1 Hot Electron Effects

The barrier height at the silicon-silicon dioxide interface is about 3.2 eV, sufficiently low so that electrons or holes, generated in silicon by device action, can occasionally have enough energy to surmount this barrier and get trapped in the silicon dioxide layer. This phenomenon of hot carrier trapping is often encountered in high-field regions.

Hot electron effects result in a change in the breakdown voltage of the device, and also the breakage of some of the satisfied silicon bonds at the silicon surface, further increasing the interface trap density. Hot electron effects are of increasing importance in VLSI because of the use of ultra-thin gate oxides and short channel lengths.

2.4.2 Oxide Charges and Traps

These traps and charges can be further classified into

(a) Interface trapped charges: the regular crystal lattice in the silicon bulk is interrupted at the interface with silicon dioxide, as the latter is amorphous. A bare silicon surface carries one unsatisfied charge per atom (1 C/m^2). Even with a good oxide film after annealing, this charge remains at about 10^{-5} C/m^2. The atoms at this interface have energy states in the Si forbidden gap and can exchange charges with silicon in short time. These so-called fast states are responsible for both generation and recombination effects at the surface. They give rise to a number of time-varying phenomena.

The number of these interface states is generally reduced by a wet hydrogen anneal of the surface at temperatures of about 450 °C.

(b) Fixed oxide charge: a layer of charge also exists within the oxide film close to the surface. These are primarily caused by excess silicon ions present within the oxide layer. They are essentially immobile under an applied field.

(c) Trapped oxide charge: these are defects within the SiO_2 layer that could be created, for example, upon x-radiation or hot-electron injection.

These together represent the slow charge states. They do not enter directly into the electronic process, but do so indirectly by establishing a surface potential, thus reducing the surface carrier mobility and altering the surface conductance.

Slow surface states can be minimized by processing the samples so as to reduce the excess ionic silicon in the oxide. This could be effected by high-temperature oxidation in dry oxygen, or, more commonly, by a relatively lower temperature anneal in a dry nitrogen ambient.

(d) Mobile ionic charge: impurities, notably sodium and potassium, can be present in the oxide as positively charged ions. These are primarily introduced as a result of contamination of the oxidation furnace. They can move about within the oxide film in response to applied voltages, leading to a drift in threshold voltage.

Mobile charges can be minimized by oxidizing in dry oxygen ambient, maintaining ultra-cleanliness during the oxidation process, coating a cover layer of silicon nitride as a barrier to ion transport, and, during gate oxidation, using chlorine bearing species to capture sodium ions.

2.4.3 Tunneling

For ultra-thin oxides or under a very high electric field (10^6 V/m for Si), tunneling will occur. This is a quantum electrical effect, wherein current conduction occurs by band-to-band tunneling process. Oxides with thickness in the range of 20~25 Å are more prone to direct tunneling. Though tunneling is possible at the thickness range used in the present work, it is not likely to be a very significant effect.

2.5 Oxide Characterization

The most useful ways to characterize oxide layers for their suitability to device performance all involve electrical techniques. The simplest measurement is the breakdown voltage. In this test, a capacitor is made by forming a conducting electrode (metal/polysilicon) on top of the oxide. The voltage of the capacitor is increased while the electrical current through the oxide film is measured. At smaller electric fields, the only current is leakage current, which is ordinarily too small to measure. When a sufficiently high electric field (about 12 MV/cm for thermal oxide) has been reached, a current will be detected which will rise exponentially with voltage, signaling an irreversible rupture of the oxide.

Another variant of the simple breakdown tests is the charge-to-breakdown test. In this test, the oxide is stressed to a point just below its breakdown field. The stress could be constant current, constant voltage or ramped current or voltage modes. The current vs. time profile shows an increase in current due to trapping of electrons in the bulk of oxide, until breakdown occurs due to accumulation of trapped positive charge near the interface.

Very thin oxides show little evidence of bulk electron trapping, and very large charge to breakdown values.

More sensitive methods of oxide evaluation use capacitance-voltage measurements. A voltage is applied between the capacitor gate and the substrate and ramped from negative to positive values, while the capacitance of the oxide is measured. The capacitance C_{ox} is given by

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} . A}{t_{ox}} \tag{2.1}$$

where C_{ox} = capacitance of oxide film

ε_o = permittivity of vacuum

ε_{ox} = dielectric constant of oxide

t_{ox} = thickness of oxide film

A = area of gate.

Ordinarily, for a p-type doped substrate, a negative voltage at the gate draws holes to the Si-SiO_2 interface, resulting in a condition known as accumulation. As the voltage is ramped, the measured capacitance decreases, because the change in sign of the field repels the charge directly beneath the gate. The resulting capacitance of the depletion region is in series with the gate oxide capacitance and effectively increases the overall capacitance.

The capacitor is said to go through the conditions of accumulation, depletion and inversion. Ideal C-V plot for a p-type capacitors is shown in Fig. 2.2.

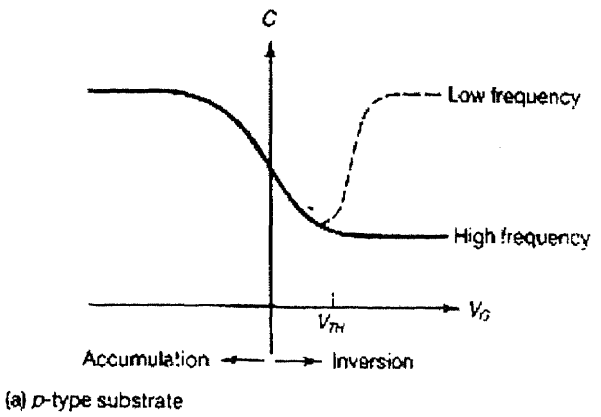


Fig. 2.2 Ideal C/V curve for p-type MOS capacitor

At high frequencies, the inversion layer carriers can't change their numbers fast enough, and the capacitance is frozen at its minimum value. The profile for an n-type semiconductor, shown in Fig. 2.3, shows the same behavior, except for a change in polarity.

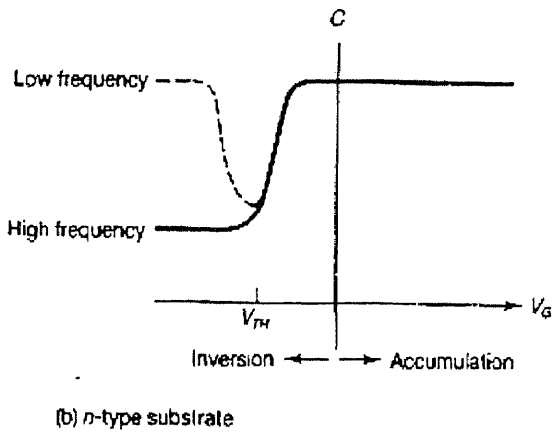


Fig. 2.3 Ideal C/V Curve for n-type MOS Capacitor

The presence of each of fixed oxide charges, mobile ionic charges and interface states, discussed earlier, affects the C-V curve by causing lateral shifts from the ideal curve in characteristic ways, as shown in Fig. (2.4).

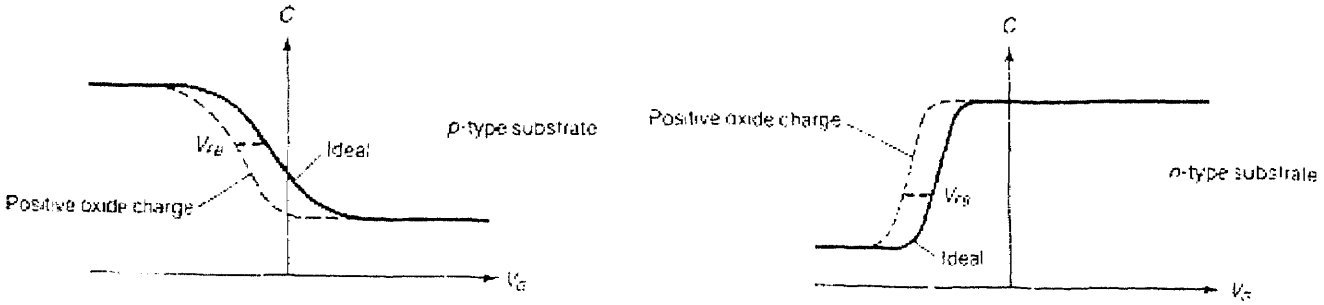


Fig. 2.4 Effect of a positive oxide charge on the C/V response of a MOS capacitor.

This in turn changes the threshold voltage at which the MOS transistor turns on. For a net positive oxide charge, the C-V curve shifts to lower values of V_g and for negative charges, towards higher values of V_g.

2.6 Literature Review

The investigation of new materials and methodologies to reduce the anomalous effects associated with the oxide film in MOS devices is the subject of a large body of research. This research assumes more significance in light of the increasing use of ultrathin oxide films in such devices as a result of overall miniaturization.

2.6.1 Damage Characterization

B. E. Weir *et al.* [*11*] have reported that soft breakdown becomes more likely for thinner oxides and for oxides stressed at lower voltages or current densities. The differences between hard and soft breakdowns of oxide are evident from post-stress I-V curves, with hard breakdown resulting in resistive I-V behavior, while gate current still has an exponential dependence on V_g following soft breakdown. At thicknesses below 20 Å. increase in gate noise becomes only way to observe breakdown. They have estimated

that oxides should undergo hard breakdown at voltages above ~6.5V and soft breakdown below ~5V. In modeling devices with ultra-thin dielectrics, gate noise, which is characteristic of soft breakdown, must be included. Soft breakdown degrades device performance by introduction of noise.

C.T. Liu *et al.* [*12*] have related hard and soft breakdowns to charge traps in the oxides. They used oxides from 23-38 Å in thickness, and measured tunneling currents through the gate to characterize the oxide. They found tunneling current to be the predominant charge transport mode at these thicknesses.

Koji Eriguchi and Masaaki Niwa [*13*] investigated the time-dependent dielectric breakdown of thin gate oxides. They grew gate oxides of thicknesses 40, 60, 100 Å at a temperature of 850 °C. Injected hot electrons break Si-H bonds and liberate H-related species near the interface. The released species diffuse through the oxide and react with precursor defect sites to create traps. The number of hot electrons generated as a function of temperature upon current or voltage stress was found to be dependent on stress polarity. They reported that a gate injection increases the number of hot electrons, while substrate injection diminishes it.

K.P. Cheung *et al.* [*14*] used gate leakage current as a measure for damage. Gate leakage current is not dependent on trapped charges. For gate oxides thinner than 50 Å, measurements relying on trapped charges no longer reliably work due to efficient detrapping by tunneling. Most thin oxide damage analysis studies are sensitive to trapped charges. Their data supported the conclusion that charging damage does not decrease with thinner oxide. This is thought to be due to larger charge-to-breakdown for very thin

oxides, as it helps the oxide withstand charging current better. Nowadays the use of high-current, low voltage plasma supplies renders oxides more prone to charging damage.

2.6.2 Incorporation of Nitrogen in Oxide and at Interface

Nitrogen is commonly incorporated into the gate oxide to reduce interface state generation and to increase the resistance to dopant diffusion. Traditionally a post-oxidation anneal in NH_3 has been used for this purpose. J. Ahn, W. Ting and D.L. Kwong [*6*] have investigated the use of nitridation during thermal oxidation using N_2O as a nitriding medium. They reported improved initial performance and enhanced device reliability due to increased resistance to dopant diffusion and reduced interface state generation. Previously, other approaches have involved the rapid thermal oxidation of silicon in N_2O [*7*] and rapid thermal nitridation of thermal SiO_2 in an N_2O ambient [*15*]. However, rapid thermal processes have been shown [*8*] to exhibit thickness and compositional non-uniformities. Furnace oxidation produces very uniform N_2O oxides across the wafer. Not only does this strengthen the oxide structure, but also acts as an oxidant diffusion barrier thus reducing oxidation rate and hence providing superior thickness control in the ultrathin range. Ahn *et al.* [*6*] also reported significantly improved resistance to charge trapping and interface state generation under hot-electron stressing. The oxide in their research was grown at 850 °C and nitrided at 950 °C for 20 min, followed by a nitrogen anneal for 5 min. They reported tighter distribution and higher endurance in t_{BD} tests, particularly under substrate injection tests. This was probably due to the nitrogen-rich layer near the Si-SiO_2 interface, with nitrogen replacing strained Si-O bonds with Si-N bonds.

G.Q. Lo *et al.* [*16*] have reported improved hot-carrier immunity in CMOS devices with N_2O nitrided oxides. Z.A. Ma *et al.* [*5*] showed suppressed boron penetration as a result of N_2O nitridation.

2.6.3 Implantation as a Means of Incorporation of Species

C.T. Liu *et al.* [*3*] have discussed implantation of nitrogen before the oxide growth as a method of incorporation into the oxide. They reported an improvement in gate oxide's resistance to plasma-charging damage. Both electron trapping and hole trapping was found to be suppressed effectively. However, their earlier work with higher doses damaged the substrate and created dislocation loops after subsequent thermal cycles. The implanted nitrogen was also found to inhibit oxide growth. In a subsequent paper [*4*], they reported successful results with nitrogen implanted at low doses of $5x10^{13}$-$5x10^{14}/cm^2$ and an energy of 25 keV, through a 200 Å screen oxide.

2.6.4 Substitution of Hydrogen with Deuterium at the Interface

Low-temperature post-metallization anneals in hydrogen ambients are critical to CMOS fabrication technologies in reducing Si-SiO_2 interface trap charge densities by hydrogen passivation. I.C. Kizilyalli, J.W.Lyding and K. Hess [*9*] have shown that using deuterium in place of hydrogen improves the hot carrier reliability of NMOS transistors by up to an order of magnitude. This phenomenon was explained in terms of a kinetic isotope effect. Chemical reaction rates involving heavier isotopes are reduced, and consequently, under hot electron stress, bonds to deuterium are more difficult to break than bonds to protium. However, the static chemical binding is evidently the same for both isotopes. Both are

equally effective in reducing interface trap charge densities. Also, transistor function for protium and deuterium post-metal anneal devices are identical. SIMS analysis reveals that at anneal temperatures of 400-450°C, deuterium diffuses more rapidly through oxide to accumulate at the $Si\text{-}SiO_2$ interface.

As per established theory, degradation of MOS performance results from channel hot electrons due to their stimulating the desorption of hydrogen from the $Si\text{-}SiO_2$ interface [*18*]. Post-metallization anneal at low temperatures improves device function by passivating the otherwise electrically active interface traps, but sets the stage for subsequent hot electron degradation. But the role of reactive hydrogen that actually participates in the interface states and trapped oxide charges has been difficult to quantify because of the difficulty in distinguishing them from the background concentration of chemically stable hydrogen in the oxide. Heungsoo Park and C.R. Helms [*10*] used deuterium in place of hydrogen for the annealing in order to distinguish it from background hydrogen. They also studied the effect of annealing in N_2 and D_2 ambient at temperatures from 400-900°C. They showed that in a $Si\text{-}SiO_2$ system, at temperatures of 600 and 800 °C, the implanted deuterium is released from Si-D and Si-OD bonds respectively. Thus the deuterium concentration in silicon decreases with annealing temperature and drops to background levels at about 900 °C. This is an important finding as most thermal oxidation processes are carried out at temperatures in excess of this temperature.

Gale *et al.* [*17*] have shown that there was a difference in the kinetics of bulk electron trapping between oxides diffused in H_2O and D_2O ambients.

2.7 Motivation for Current Work

As stated in the Objective (Sec. 1.2), the study investigates the use of ion implantation as a means of introduction of the deuterium at the silicon-silicon dioxide interface. While annealing in deuterium ambient has been shown to improve device characteristics, it is not suitable for complex integrated circuits with multilevel interconnections. Implantation also offers a much greater level of control over the precision of placement and dosages, which makes it more suitable for modern devices.

Also, thin gates are increasingly used in modern devices because of the tendency towards increasing miniaturization. The current study uses an oxide thickness (40Å) near the current limit of practical device fabrication. Since these thin-oxide devices are more susceptible to hot electron damage, the use of deuterium and other species in reducing hot electron effects is an important subject of study.

CHAPTER 3

FABRICATION

3.1 Introduction

In this chapter the detailed fabrication sequence is presented. The brief process flow is described below. An introduction to the particular process step is detailed in the beginning of each process and the conditions maintained during the fabrication are given following this. All the defects and problems encountered during each of the processing step are discussed at the end of that particular process and the ways in which to overcome these problems are also presented. The process steps, except for ion implantation, were all carried out at the NJIT Microelectronics Research Center. The deuterium implantation was carried out at IICO (Santa Clara, CA), while the polysilicon gate implant was carried out at Ion Implant Services (Sunnyvale, CA). The different deuterium implantation schedules were simulated using the SRIM (Stopping and Range of Ions in Matter) simulation package.

3.2 Outline of the Process Steps for Fabrication

An outline of the processing steps that were followed is presented. This includes a detailed description of each of the process steps, including the conditions maintained during the fabrication and a discussion of its significance and problems associated with it. This is followed by a flow chart for the fabrication of the device, and a schematic representation of the fabrication process.

3.2.1 Process Flow Description

3.2.1.1 Starting Materials: The starting material for the process was p-type (boron doped), <100> oriented CMOS grade silicon wafers, with a sheet resistivity of 1.25-2.0 Ω-cm.

3.2.1.2 Denuding: Each wafer was scribed on the back for identification. An oxide layer of approximate thickness 1000 Å was grown by steam oxidation at 950 °C performed for 40 minutes. This oxide layer was subsequently stripped using 6:1 BOE (buffered oxide etch). This step helped in the removal of impurities and contaminants from the wafer surface prior to actual processing.

Impurities can degrade the performance of circuits or even cause failure. This is even truer of very large scale integrated circuits, with extremely small devices operating at low voltages and the thin films used in them. Hence for high yield and device reliability, it becomes imperative to eliminate all possible sources of contamination. Surface cleaning is especially important prior to high temperature processes because impurities react and diffuse at much higher rates at elevated temperatures. Thus a surface cleaning is performed at the beginning and before any furnace processing. The most commonly used wet chemical cleaning technology is based on hot alkaline or acidic peroxide (H_2O_2) solutions. These are used to remove chemically bonded films from the wafer surface prior to critical steps. RCA cleans, another commonly used process, are based on a two-step process with the wafer etched in succession in two solutions, SC-1 followed by SC-2. Both these solutions incorporate the strong oxidizing capability of H_2O_2. SC-1 is an aqueous alkaline solution which removes organic films, while SC-2 is

an acidic mixture used to remove alkali ions & cations and metallic contaminants. SC-1 is typically a 5:1:1 solution of DI water, "unstabilized" (30%) H_2O_2 and ammonium hydroxide (27%). SC-2 typically consists of a 6:1:1 solution of water, H_2O_2 and hydrochloric acid (37%). The processing temperature is maintained at 80 °C.

3.2.1.3 Sacrificial Oxide Growth: A thin (~200 Å) oxide was grown on the denuded wafer surface prior to implantation of deuterium. This was needed as implantation typically provides a dopant profile with a peak dopant concentration at a certain depth within the substrate. The use of a sacrificial oxide layer thus helps achieve a peak deuterium concentration near the silicon surface. This not only permits doping the wafer while still keeping its surface passivated, it also allows greater control of the charge at the $Si\text{-}SiO_2$ interface.

The conditions for sacrificial oxide growth were

Table 3.1 Sacrificial Oxide Growth Conditions

Type	Steam Oxidation
Oxygen	7.5 SLM
Bubbler	530 scm
Temperature	1050 °C
Time	12 min

3.2.1.4 Deuterium Implantation: Low doses of deuterium were implanted through the sacrificial oxide film. Ion implantation is a process in which energetic, charged atoms or

molecules are directly introduced into a single-crystal substrate. It is ordinarily carried out with ion energies in the range 50-500 keV. An ion source, which can be any ionizable compound of the atom, is vaporized and ionized by passing it through a hot or cold electronic discharge. The ions released by electronic bombardment are extracted and fed to an accelerator column. Mass separation processes are used to generate a monoenergetic, highly pure beam of atoms.

Implantation has a number of advantages over diffusion as a means of introducing impurities in semiconductor technology. A very pure beam, free of contamination, of the dopant can be generated. A wide variety of doses, from 10^{11} to 10^{17} can be delivered, and controlled to within ±1% over this range. The process can be carried out at room temperature. By controlling the energy and dosage of implant, a wide variety of dopant concentration profiles can be obtained. However, implantation is a costly process and results in damage to the crystal structure. A high-temperature anneal can, however, erase most of the damage.

The conditions to be used for the implantation were derived from simulations performed using the SRIM package. The simulation result for implantation carried out at an incident ion energy of 25 keV is presented in Fig. 3.1. From the figure, it is observed that the peak of the as-implanted deuterium concentration distribution is at an approximate depth of 0.5μm within the body of the silicon substrate. The simulation results at the other implantation energies used are presented in Appendix F (Figs. F.1.2, F.1.3). The conditions used for the implantation along with the approximate depth of implantation peak are summarized in Table 3.2.

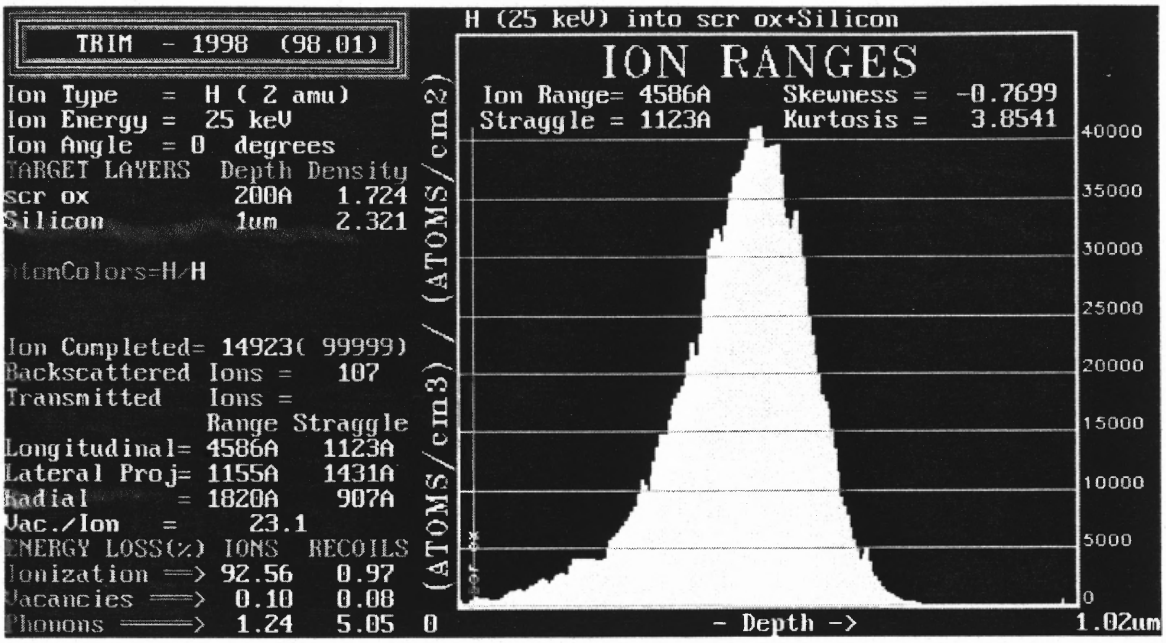


Fig. 3.1 SRIM simulation of implantation of $^{2}H_{1}$ at 25 keV, $1x10^{14}/cm^{2}$.

Table 3.2 Deuterium Implantation Parameters

Species	$^{2}Deuterium_{1}$	Depth of implantation peak (from SRIM simulation)
Energy	15 keV 25 keV 35 keV.	0.50 µm 0.35 µm 0.65 µm
Dose	$1 \times 10^{14} / cm^{2}$	

3.2.1.5 Sacrificial Oxide Strip: The sacrificial oxide film was stripped using 6:1 BOE. The process details are the same as for stripping of the denuding oxide.

3.2.1.6 Gate Oxide Growth: The actual thin gate oxide was grown by dry oxidation at 800 °C for 15 minutes. While steam oxidation is generally faster, it is not suitable for the growth of very thin oxide films. Also, dry oxidation results in oxide of higher density and generally better quality with a lower concentration of traps and interface states. For this reason gate oxide is almost exclusively grown by the dry oxidation method. Prior to the oxidation, the furnace was cleaned with a mixture of oxygen and HCl, followed by a nitrogen purge and cool down. This step was necessary to ensure high purity of the gate oxide layer grown. The conditions maintained for the gate oxidation were:

Table 3.3 Gate Oxide Growth Conditions

Type	Dry Oxidation
Oxygen	7.5 SLM
Temperature	750 °C
Time	30 min

After growing the gate oxide, **S**econdary **I**on **M**ass **S**pectrometry (SIMS) analysis was performed on the wafers to establish the presence of deuterium at the interface. The analysis result for the wafer implanted with deuterium at 25 keV, 1 x 10^{14} / cm^2 is presented in Fig. 3.2. The peak labeled as "D" indicated by the arrow in the figure corresponds to deuterium. Thus the presence of deuterium in the substrate is borne out by the analysis. The SIMS analysis for the wafer without any deuterium implanted is shown in the appendix, Fig. G.1 and lacks a peak corresponding to deuterium.

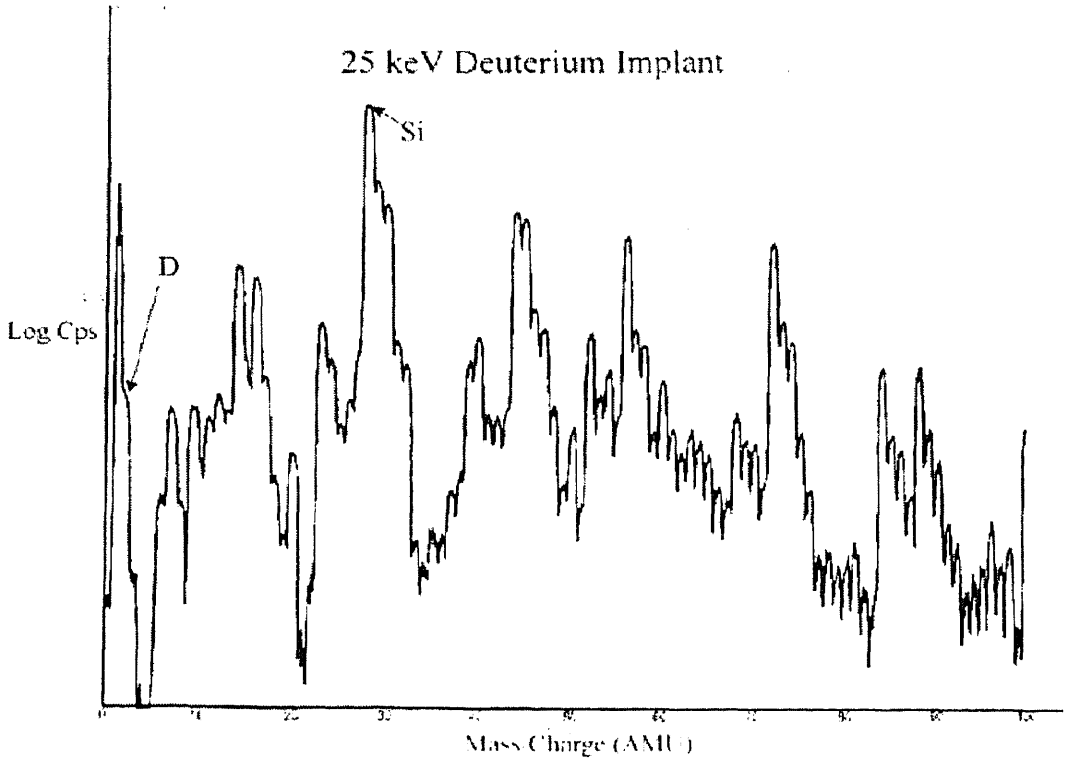


Fig. 3.2 SIMS analysis result for the wafer implanted with D_2 at 25 keV, $1x10^{14}$ / cm^2.

3.2.1.7 Annealing in N_2O Ambient: Control wafers with and without deuterium implanted on them were annealed in nitrous oxide. The conditions used for the process were:

Table 3.4 N_2O Anneal Parameters

Species	N_2O
Flow Rate	7.5 SLM
Temperature	800 °C
Time	24 min

3.2.1.8 Measurement of Oxide Thickness: Because of the very low thickness of the oxide film used, it was imperative to minimize the exposure of the wafers with the thin gate oxide to air, as even a short duration exposure would result in the formation of native oxide film on top of the wafer surface. At the low thickness of the gate oxide being used, even a small amount of native oxide could prove sufficient to alter the nature of the oxide film significantly. Accordingly, wafers for oxide thickness measurement were specially marked out and separated at this stage. The thickness was determined by ellipsometry using an Olympus ellipsometer. Ellipsometry is the only reliable method for thickness determination of such thin films. The thicknesses were determined at 12 points on the wafers, which were averaged to arrive at the final thickness. These readings are summarized in Table 3.5.

Table 3.5 Wafer Thickness Measurements

No. of Wafers	5
Points/wafer	12
Mean Thickness	42.3 Å
Standard Deviation	5.21 Å

3.2.1.9 Deposition of Polysilicon: The gate oxidation was immediately followed by the deposition of polysilicon. The polysilicon was deposited by LPCVD at 600 °C. The conditions maintained during the process are summarized in this table:

Table 3.6 Polysilicon Deposition Conditions

SiH_4	300 sccm
Temperature	600 °C
Pressure	400 mTorr
Time	2 hr 25 min

3.2.1.10 Implantation of Phosphorus: The polysilicon was doped with phosphorus to increase its conductivity. A high implantation dosage and energy, equivalent to a source-and-drain implant, was used.

Undoped polysilicon has a high resistivity of about 500 Ω-cm, and is essentially self-insulating. Doping with either boron or phosphorus results in a sharp reduction in the resistivity of the polysilicon film, making it conducting. For use as gates in MOS transistors, the polysilicon is heavily doped to form n+ or p+ regions. This can be done by diffusion processes, but for heavy doses ion implantation methods are preferred. The implantation turns the film amorphous, and an annealing step is required to recrystallize the film and for dopant activation.

Implantation was used as the doping method in this study. The conditions to be used for the implantation were arrived at by performing simulations using SRIM. These simulations are presented in Appendix F (Fig. F.2.1). The implantation specifications are summarized in Table 3.7.

Table 3.7 Phosphorus Implantation Parameters

Species	Phosphorus[15]	Depth of implantation peak (from SRIM simulation)
Energy	30 keV.	0.1 μm
Dose	$1 \times 10^{16} / cm^2$	

3.2.1.11 Photolithography to Pattern Polysilicon: the mask HMM 3-0520-03 (Device:2 μm MOS tester; Layer: Circles) was used to pattern the wafer with a pattern of circular capacitors of diameters ranging from 50 to 500 μm. The pattern shown in Fig. 3.3 was repeated throughout the surface of the wafers.

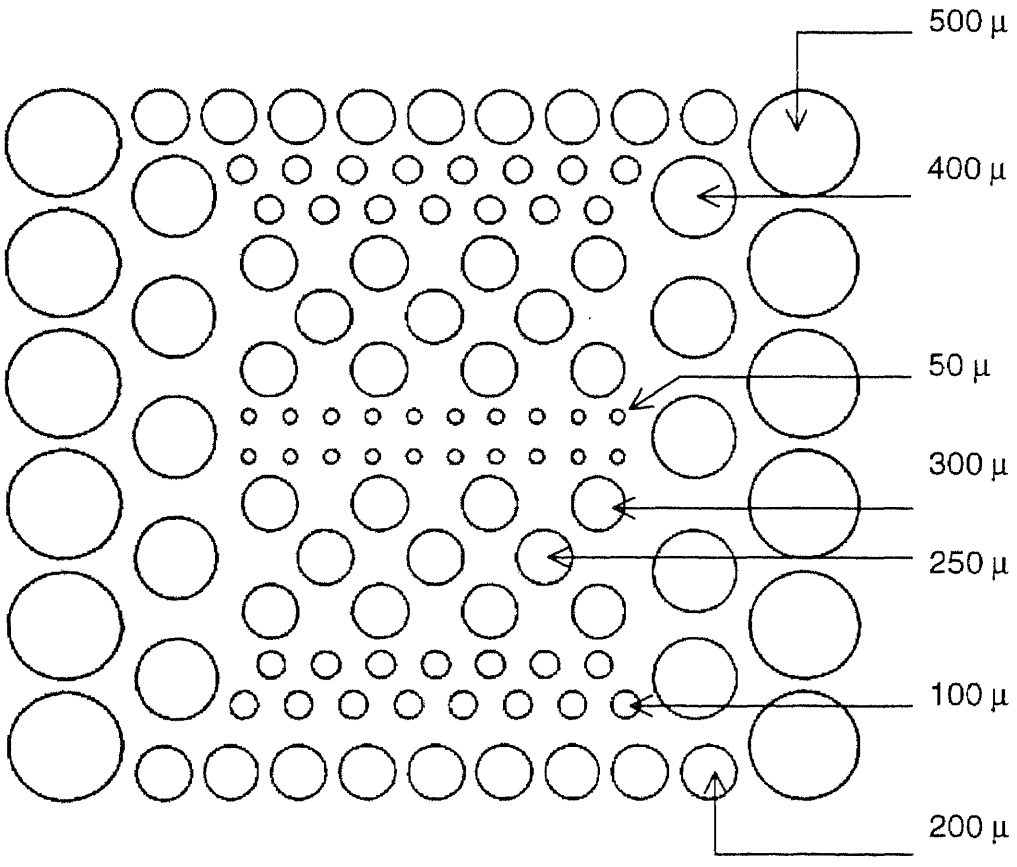


Fig 3.3 Pattern of Capacitors on Wafers

In photolithography, a layer of polymeric photoresist (PR) is applied as a thin film to the substrate and subsequently exposed through a mask. The mask contains clear and opaque features that define the patterns to be created in the PR layer. The areas in the PR exposed to the light are made either soluble (for **positive** photoresist) or insoluble (for **negative** photoresist) in a specific solvent known as developer. Negative PR was used in the current thesis. To start with the wafer was primed with a pre-resist coating of a material designed for better photoresist adhesion. The wafers were then ready to be coated with photoresist. Spin coating is the most widely used technique to apply a uniform and adherent film of desired thickness. This procedure was carried out by dispensing the resist solution on the wafer surface, and then rapidly spinning the wafer until the resist was essentially dry. After the wafers were coated with resist, they were subjected to a temperature step, called soft-bake (or pre-bake). This step accomplishes several important purposes, including driving off solvent from the spun-on resist and improving adhesion of the resist. After the wafer had been coated with resist and suitably soft-baked, it was ready to be exposed to some form of radiation in order to create an image on the resist. The degree of exposure was adjusted by controlling the energy impinging on the resist. Following exposure, the resist film was made to undergo development in order to leave behind the image, which would serve as the mask for etching. The wafer was then spin-dried and transported to the post-bake module. Following development, an inspection was performed. The purpose was to insure that the steps of the PR process up to this point had been performed correctly and to within the specified tolerance. Any inadequately processed wafers detected by this inspection could have their resist stripped and reworked. Post-baking was then performed just prior to etching. Its chief purposes

include the removal of residual solvents, improvement of adhesion, and to increase the etch resistance of the resist.

3.2.1.12 Etching of Polysilicon:

The polysilicon was etched by using Drytek Phantom etch station.

Etching in microelectronics fabrication is a process by which material is removed from the silicon substrate or from thin films on the substrate surface. When the mask layer is used to protect specific regions of the wafer surface, the goal of etching is to precisely remove the material which is not covered by the mask.

The theory of wet and dry etching is detailed at length in Appendix H.

The conditions used during the etching were

Table 3.8 Polysilicon Etch Conditions

Type	Phantom Dry Etch
Temperature	25 °C
Time	60 sec
Pressure	250 mTorr
SF_6 flow rate	40 sccm

At these conditions, the polysilicon etch rate was 3400 Å/min.

3.2.1.13 Photoresist Strip: the remaining photoresist was stripped off using an m-pyrol strip. This is a two-stage process involving immersion into a primary followed by a secondary m-pyrol bath.

3.2.2 Flow Chart for Fabrication of the Device

Silicon Wafer

↓

Deposition of denuding oxide

↓

Stripping of denuding oxide

↓

Deposition of sacrificial oxide

↓

Ion implantation of deuterium

↓

Stripping of sacrificial oxide

↓

Deposition of gate oxide

↓

Annealing of selected wafers in N_2O

↓

Measurement of oxide thickness

↓

Deposition of polysilicon

↓

Source and Drain implantation of phosphorus

↓

Drive - in

↓

Photolithography to pattern polysilicon

↓

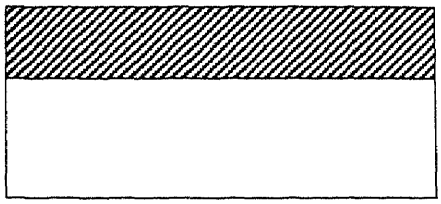
Reactive Ion Etching of polysilicon

↓

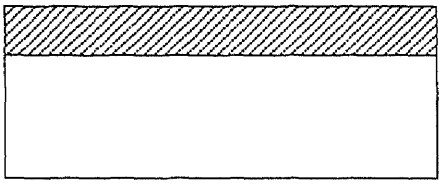
Stripping of photoresist

3.2.3 Schematic Representation of the Device Fabrication Steps

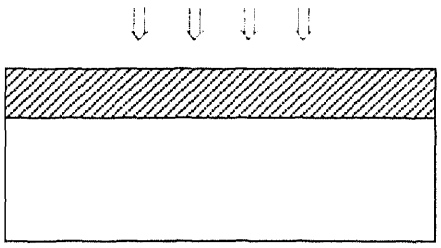
The cross sections of the wafers at different processing steps are shown schematically by means of cut-away profiles of the devices, along with a brief explanation of the step(s) involved.



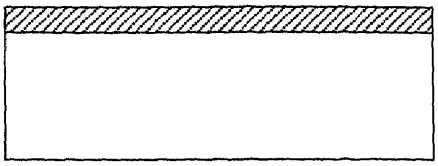
<100> p-type wafer deposited
with 2000 Å oxide, denuded



200 Å sacrificial oxide deposited



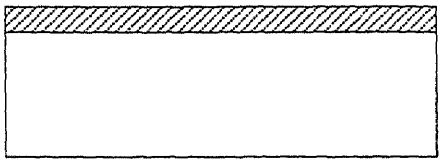
Deuterium implanted at energies
Of 25, 15, 35 keV, dose $1x10^{14}/cm^2$.



40 Å Gate oxide grown

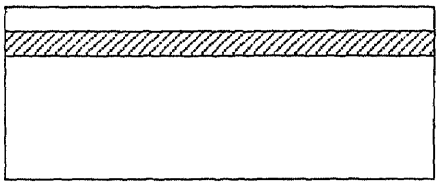
↓

→ N_2O → N_2O →



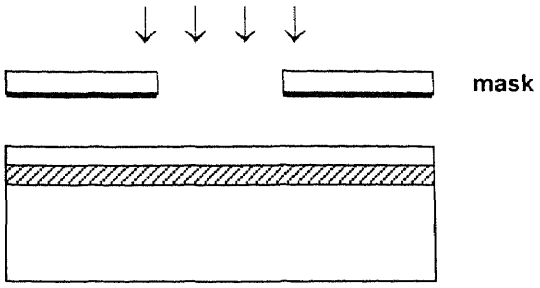
Annealing of selected wafers
in an N_2O ambient

↓

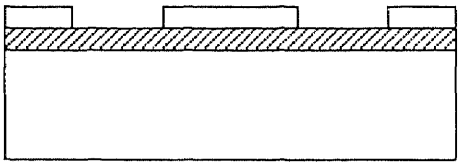


Deposition of polysilicon,
S-&-D implantation of phosphorus

↓



Patterning of polysilicon



Reactive Ion Etching of Polysilicon,
Photoresist strip

Fig. 3.4 Schematic Diagarm of Process Fabrication Steps

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Overview

The results from the various tests carried out on the wafers are presented in this chapter. A discussion of the results is also included.

The capacitors were tested using the HP-4145B Semiconductor Parameter Analyzer. The HP 4145B has four SMUs (Source Monitor Unit), two voltage monitors (V_m) and two voltage sources (V_s). Connections are defined according to the device being measured. However, there are certain basic testing programs already defined like the FET, diode, BJT that can be modified as desired.

The HP-4145B Semiconductor Parameter Analyzer is capable of applying a wide range of currents and voltages through each of the SMU channels and measuring the time-varying or voltage- or current-dependent measurements at different points on the wafer. A probe with tip size of about 50 μm was used to place the probe on the capacitors.

To carry out the tests, a pattern consisting of circular capacitors of different cross sectional areas was formed on the wafers. The capacitor sizes ranged from 50 μm to 500 μm. The pattern shown in Fig. 3.3 was repeated over the entire surface of the wafers. The capacitance depends on the cross sectional area as

$$C_o = \left(\frac{\varepsilon}{t}\right) A \qquad (4.1)$$

where A = area of gate = 1.963×10^{-5} cm^2 to 1.963×10^{-3} cm^2

t = thickness of dielectric $\approx$ 40 Å

and ε_{SisO2}= dielectric constant $\approx 3.5 \times 10^{-13}$ F/cm

Using these values, the average unstressed capacitance of the devices works out to be between 17.18 pF (for 50 μm wafers) and 1718 pF (for 500 μm wafers).

4.2 Methodology

Based on simulations carried out using SRIM, an implantation energy of 25 keV and a dose of 1×10^{14} atoms/cm^2 was selected. However, implantation was carried out on some wafers at energies above and below this energy to arrive at the optimum value. A total of 11 wafers were processed. Improvements in device performance have earlier been reported upon annealing in N_2O. To compare results with annealing, some of the implanted wafers were annealed in N_2O. The scheme for fabrication is given in Table 4.1.

As explained earlier, a silicon surface left exposed to air for even short duration tends to grow a native oxide layer on top of it, or as a thin layer over the previously thermally grown oxide. Native oxide has very undesirable characteristics for MOS devices. In addition, because of the small thickness of gate oxide used, even a small layer of native oxide on the gate could have a significant effect. Hence some wafers were marked out for measurement of the oxide thickness and were separated from the remaining wafers, which were directly processed after growth of the gate oxide.

Table 4.1 Fabrication Scheme for the Wafers.

Wafer	Implant scheme	Anneal scheme	Other details
1.	25 keV, $1x10^{14}/cm^2$	Annealed in N_2O	No gate oxide grown.
2.	25 keV, $1x10^{14}/cm^2$	Annealed in N_2O	
3.	25 keV, $1x10^{14}/cm^2$	None	Taken for thickness measurements
4.	15 keV, $1x10^{14}/cm^2$	Annealed in N_2O	
5.	15 keV, $1x10^{14}/cm^2$	None	Taken for thickness measurements
6.	35 keV, $1x10^{14}/cm^2$	Annealed in N_2O	
7.	35 keV, $1x10^{14}/cm^2$	None	Taken for thickness measurements
8.	35 keV, $1x10^{14}/cm^2$	None	
9.	None	Annealed in N_2O	
10.	None	None	Taken for thickness measurements
11.	None	None	

4.3 Measurements

The primary test applied to compare the wafers was the leakage current density through the capacitor gate when a ramped voltage was applied at the gate. This test was repeated at several different locations and different capacitor sizes on the wafers.

4.3.1 Device Breakdown Characteristics

Typical breakdown characteristics of the wafers with and without deuterium implantation and annealing are presented in Fig. 4.1.

The curve for the implanted and annealed wafer shows close to ideal characteristics. The control wafer (without implant and anneal) breaks down earlier than the ones implanted with deuterium.

Breakdown characteristics of devices are an important indicator of device lifetime. A breakdown is characterized by a sharp increase in the current through the oxide and indicates an irreversible damage to the oxide structure. A broken-down device

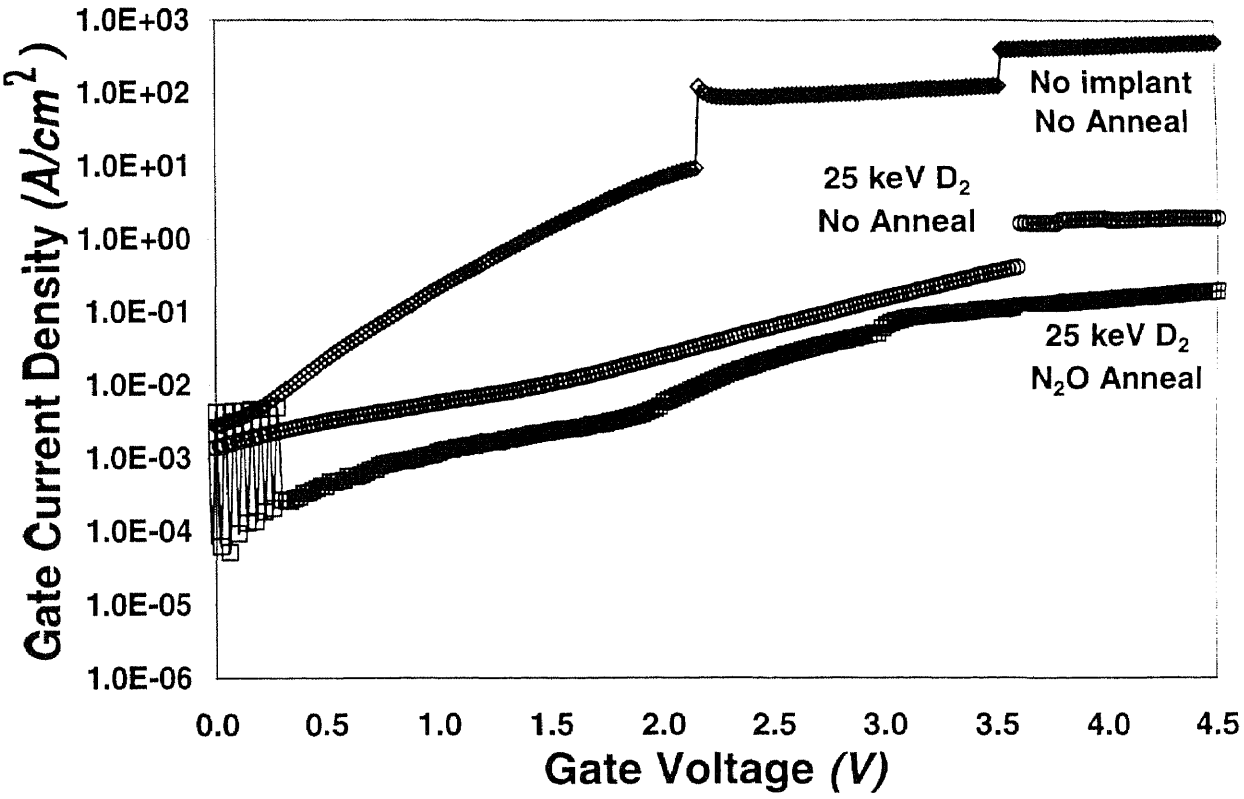


Fig. 4.1 Leakage Current Density Characteristics at Breakdown.

is rendered unusable. The breakdown performance is generally reported in terms of charge-to-breakdown and time-dependent dielectric breakdown, which are statistically

generated from the breakdown current and potential difference respectively under extended voltage or current stress.

Unfortunately, breakdown could not be consistently observed across all wafers in sufficient numbers to generate statistical data. Most of the device characteristics were indicative of post-stress breakdown, and the leakage current was high for a device of this nature.

At extremely low gate oxide thicknesses, there is a greater tendency for devices to exhibit soft rather than hard breakdown. A soft breakdown is characterized by increase in circuit noise near the point of breakdown and lack of a sharply defined current increase. Thus breakdown becomes more difficult to observe. Fig. 4.1 shows two distinct cases of sharply defined breakdowns. This indicates the lowering of interface trap-enhanced breakdown with deuterium implantation. The lack of other breakdown curves could be attributed to the tendency of the devices to break down by soft mechanisms.

4.3.2 Leakage Current with and without Implantation, Annealing

Fig. 4.2 compares the results for the various N_2O annealed wafers. It is seen that all wafers exhibit some leakage current even at low voltages. This could be attributed to the extremely small thickness of the gate oxide.

The results clearly show that the leakage current is the lowest for devices implanted with deuterium at 25 keV with N_2O annealing. The wafer shows no appreciable leakage current until at an applied voltage of 3 V, at which point there is a small leakage current. The difference between wafers without implantation, and with implantation but no annealing was not very large, which suggests that a carefully selected

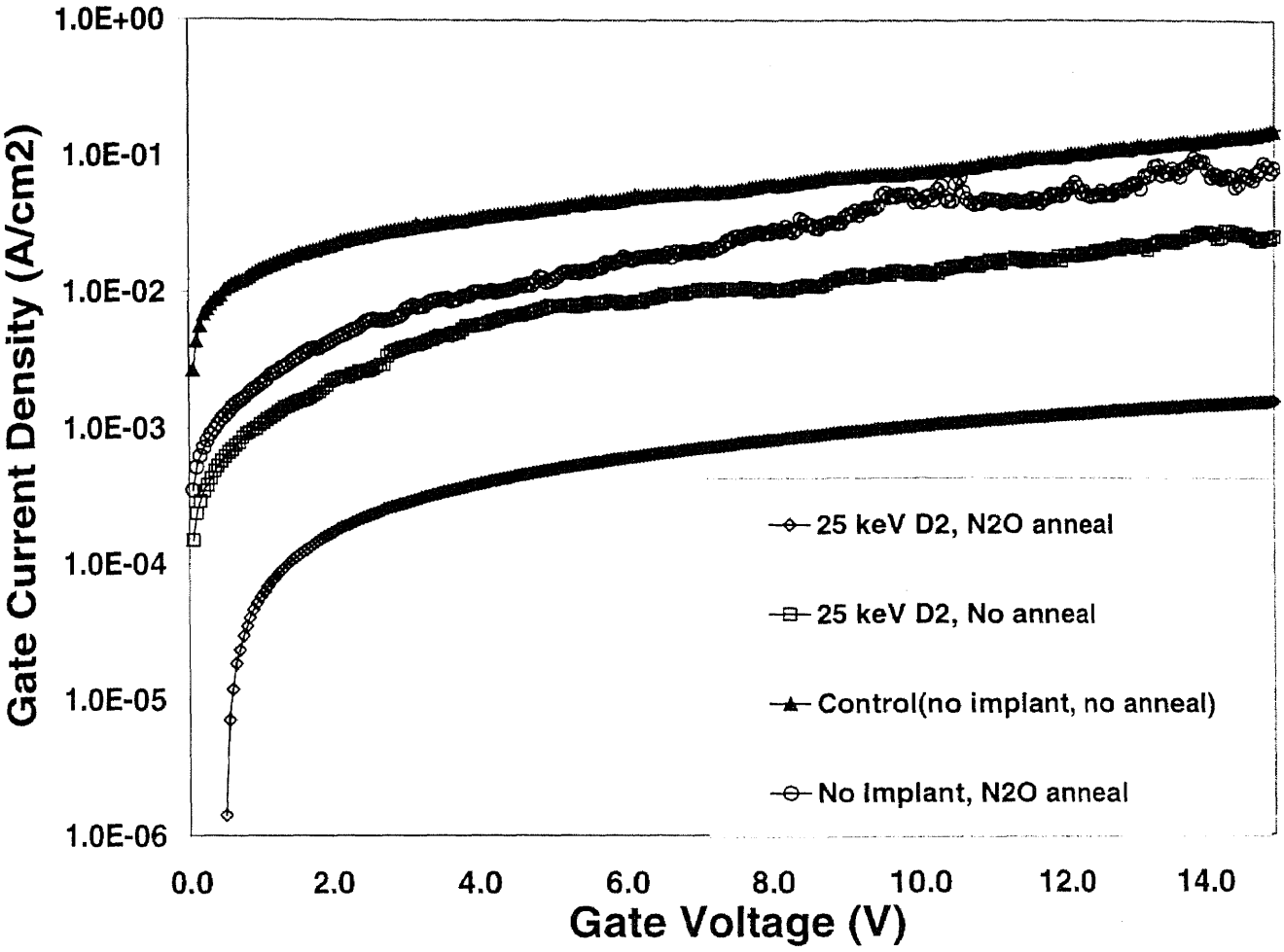


Fig. 4.2 Leakage current density vs. gate voltage for wafers with and without implantation, annealing.

regime of implantation and annealing is the best for improving device performance. The wafers without any implantation or annealing in general showed the worst characteristics.

4.3.3 Comparison of Implantation Energies

Fig. 4.3 compares the results for the wafers implanted with deuterium at different source energies. The experiments are in agreement with the selected design, as the devices implanted with deuterium at 25 keV show the least leakage current. Wafers implanted

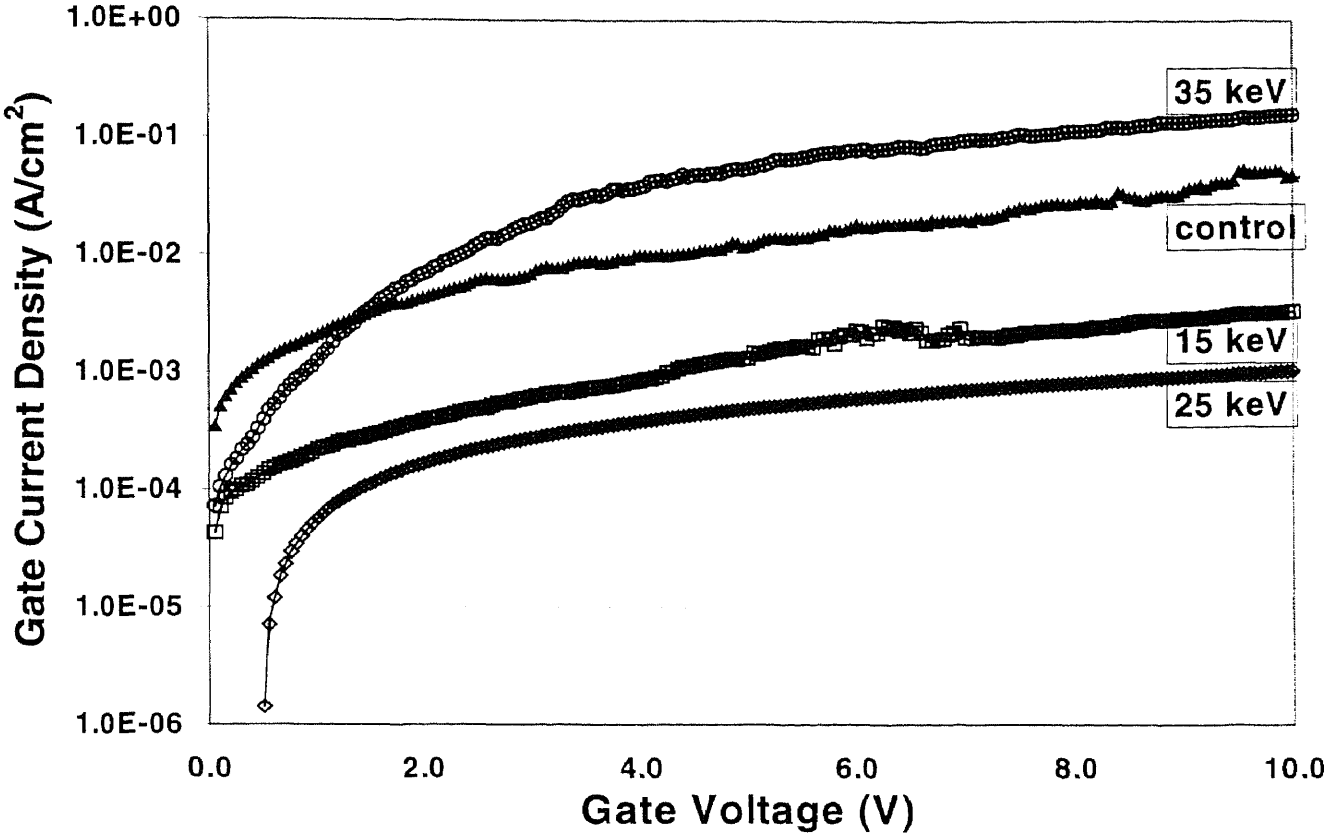


Fig. 4.3: Leakage current density vs. gate voltage for wafers at different implantation energies.

with 15 keV deuterium show slightly worse leakage, while the current is much higher for 35 keV implanted wafer.

Ion implantation typically results in a dopant profile with a peak concentration some depth into the target material. A higher energy of implantation (35 keV) causes amore substrate damage, leading to higher leakage current, that results in a deeper implant peak. On the other hand, a lower energy (15 keV), means that the implant peak is shallow, making the deuterium more susceptible to diffuse out during oxide growth.

A post-implant anneal is commonly used to even out the distribution of implanted ions at the interface, but in this case, because of the risk of outdiffusion of deuterium at

high temperatures, the annealing was limited to the gate oxide growth temperature. The trade-off could be reduced efficiency of redistribution of ions upon annealing.

4.3.4 Voltage Stress under Gate and Substrate Injection

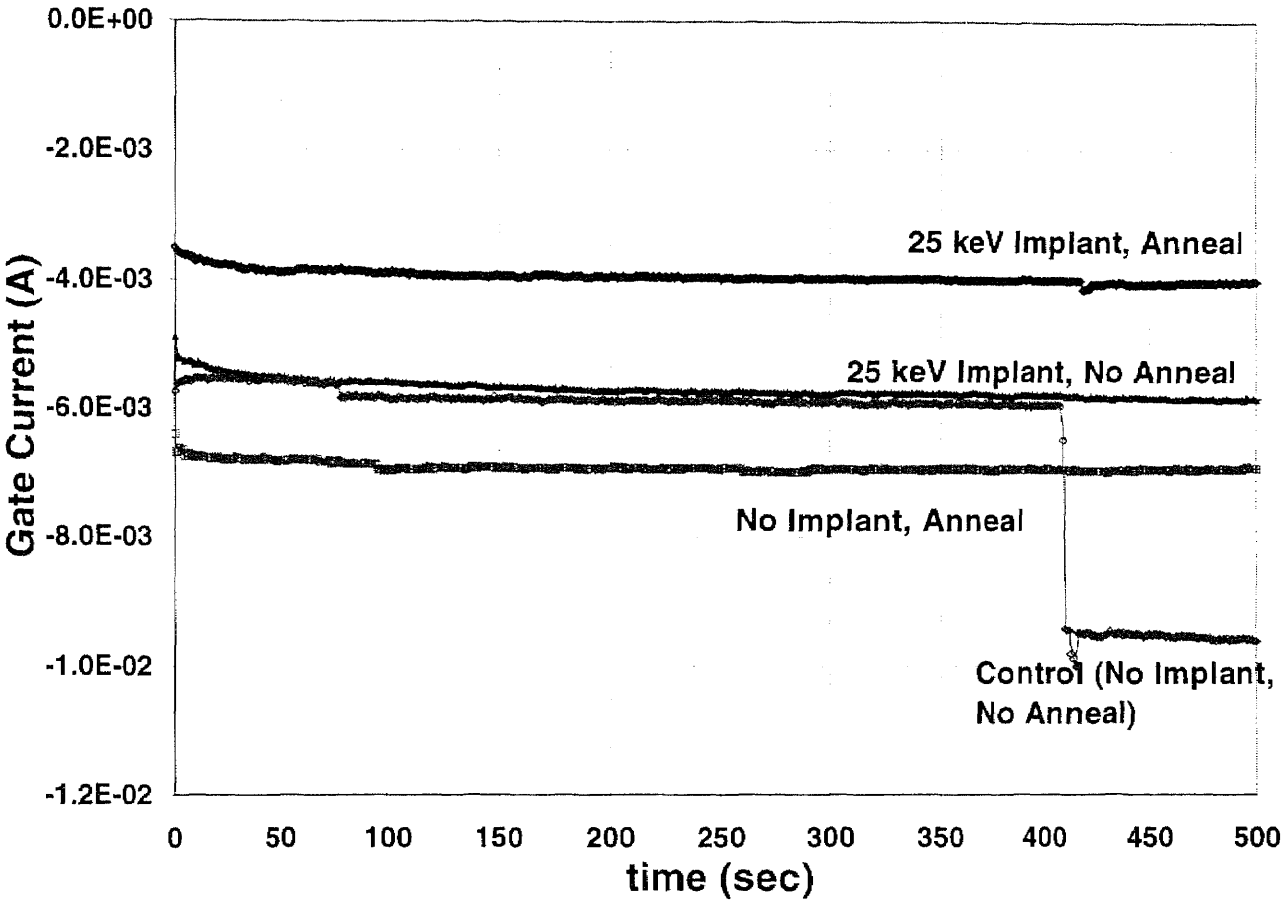


Fig. 4.4 Time-dependent gate current at constant voltage (5 V) under gate injection.

The time-dependent behavior of the leakage current was measured under Gate Injection i.e. with a positive voltage with respect to the substrate applied to the gate electrode, and under Substrate Injection i.e. with the substrate positive with respect to the gate.

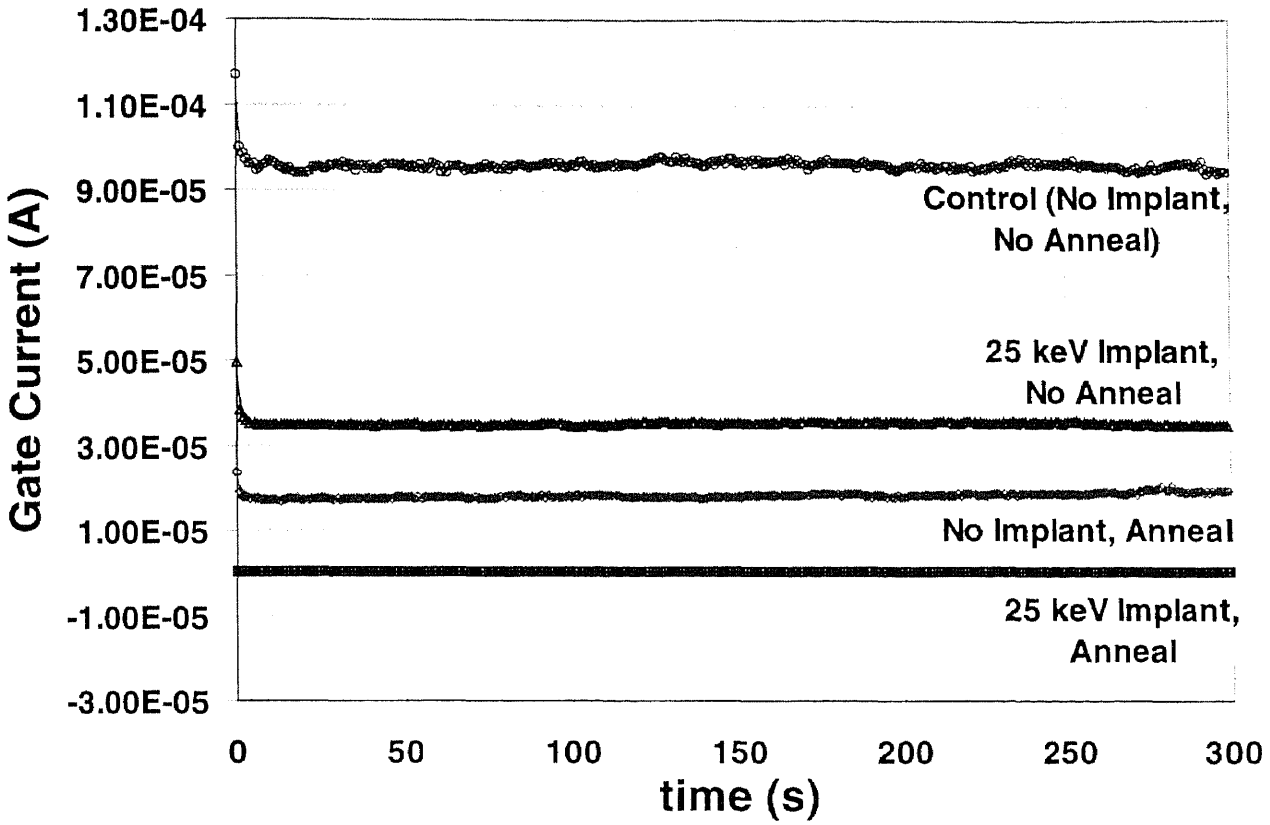


Fig. 4.5 Time-dependent gate current at constant voltage (-5 V) under substrate injection.

A constant voltage stress near the breakdown voltage of the dielectric is applied to the capacitor to get a measure of the stability of the device under continuous voltage stress.

Under conditions of both Substrate injection, shown in Fig. 4.4, and Gate injection, shown in Fig. 4.5, the leakage currents through the devices on the wafer implanted with deuterium and annealed in N_2O was found to be the lowest, and in fact was very small for substrate injection, indicating the reduction in the number of dangling bonds. For the case of gate injection, the leakage current for the control wafer was

initially comparable to that for the unannealed wafer with deuterium, but the oxide exhibited breakdown after 400 sec of operation. The lower currents with gate injection are because the substrate, being p-type, is deficient in electrons.

A lower current for the unimplanted but annealed wafer than the implanted unannealed one under gate injection suggests that stoichiometry at interface is more important under gate injection than it is under substrate injection. Since N_2O brings about an improvement in interface stiochiometry, annealing improves the gate currents realizable more substantially than deuterium implantation.

4.3.5 Initial Electron Trapping Slope

The voltage curve for a typical device subjected to a gate current stress, as shown in the Fig. 4.6, is characterized by an initial stage of reduction of voltage due to dominant electron trapping. The slope of this initial electron trapping region, or the Initial Electron Trapping Slope, is indicative of the electron trap density. Fig. 4.6 shows the IETS profile for the wafer implanted with deuterium at 25 keV, $1x10^{14}/cm^2$ and annealed in N_2O. The IETS lacks a well-defined region of hole trapping, as the trapping of holes takes place over an extremely short interval of time, which is not registered here. This was typical of all the wafers used in the experiment. The value of the IETS is indicated by the slope of the straight line as drawn in Fig. 4.6. The averaged IETS readings for the different wafers are summarized in Table 4.2 and a comparative bar chart drawn in Fig. 4.7.

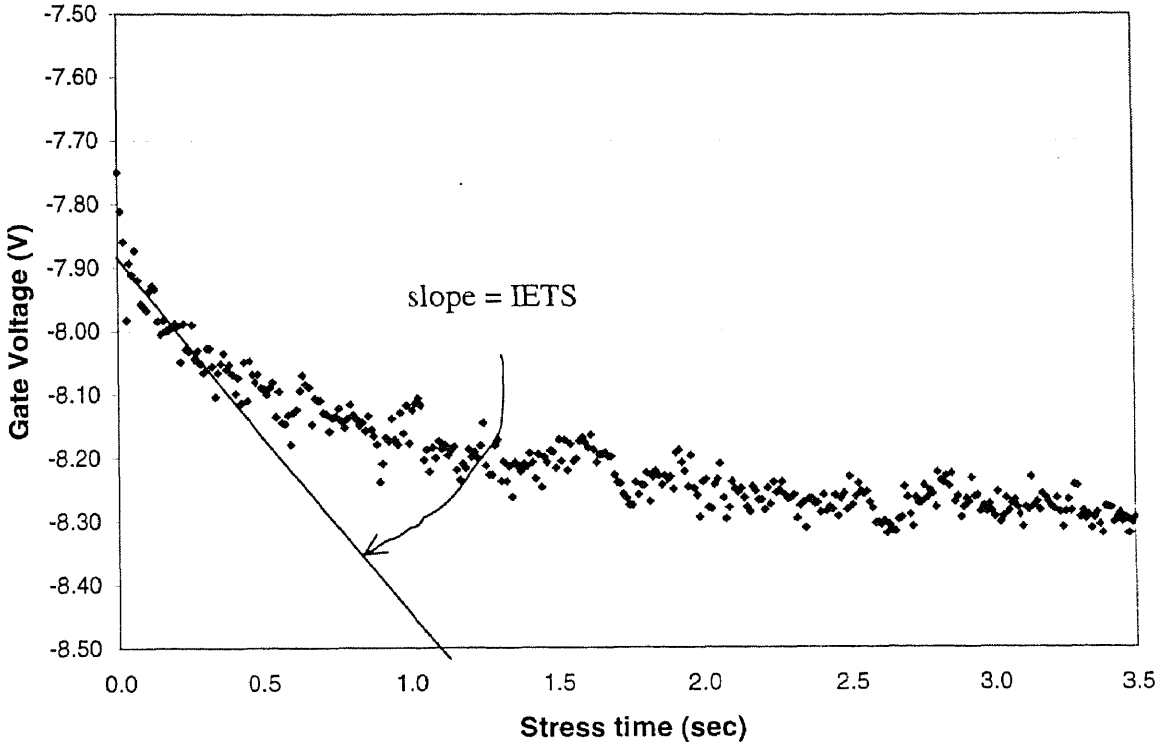


Fig. 4.6 The voltage-time curve for 25 keV deuterium implanted annealed wafer for current stress under gate injection, with IETS indicated.

Table 4.2 IETS values for gate current injection on 100 Å capacitors.

Wafer type	IETS (V/sec)
25 keV implant, anneal	-1.196
25 keV implant, no anneal	-3.498
No implant, anneal	-4.662
No implant, no anneal	-9.100

Table 4.2 presents the average IETS values for the different wafers, and the results are summarized in the form of a bar chart in Fig. 4.7.

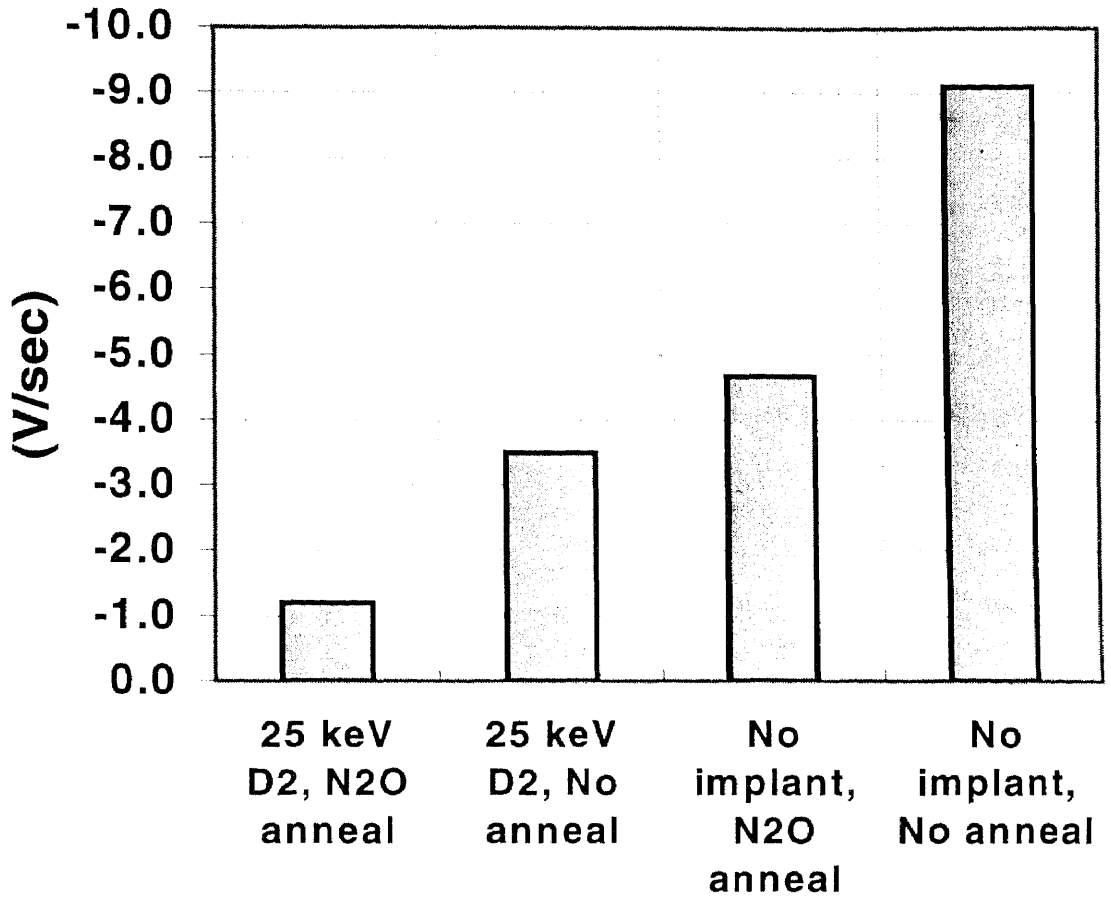


Fig. 4.7 Bar chart of average IETS values for different wafers upon gate injection.

From Fig. 4.7 and Table 4.2, it is clearly seen that the electron trap density is lowest in the deuterium implanted and N_2O annealed wafer, while the control wafers have the highest trap density. The presence of deuterium brings about the reduction in the number of electron traps. There is roughly an order of magnitude improvement in IETS with the use of deuterium. The N_2O annealed wafer also exhibits some reduction in electron traps [2] over the control wafer, but the reduction is higher in the presence of deuterium.

CHAPTER 5

CONCLUSIONS

5.1 Introduction

The reduction in the hot electron degradation in CMOS capacitor devices by incorporating deuterium through ion implantation is borne out by the experimental results. The energy of hot electrons required for desorption of deuterium from the silicon-silicon dioxide interface is believed to be much higher than that for hydrogen. This large isotope effect can significantly enhance the lifetime of the device.

It has been demonstrated that the incorporation of deuterium at the silicon-silicon dioxide interface using ion implantation before gate oxide growth is an effective means and a viable alternative to annealing over extended periods after completion of the device. Deuterium implantation brings about a clear enhancement in gate oxide quality by improving the interface characteristics. Incorporation of nitrogen at the interface through annealing in N_2O further improves device performance because of improved interface stoichiometry. A reduction of electron traps with deuterium implantation is also seen.

The experiments suggest that the selection of an appropriate implantation energy and dose and N_2O annealing conditions is an important factor for optimization of the thin oxide reliability.

The quality of the thermal oxide might have had an impact on the inability to gather comprehensive capacitance-voltage and time dependent breakdown data. This was

a primary concern as the effort to use lower possible temperatures during all process steps to ensure retention of the implanted deuterium at the interface could have resulted in the oxide being of lower quality with an increased tendency for leakage. The low thickness (40 Å) of the oxide also makes it more susceptible to tunneling.

Because of the concern for lower temperatures used during processing, the drive-in step following implantation to homogenize the distribution of phosphorus at the gate elecrode could only be carried out at 600 °C. A drive-in at this temperature is of only partial benefit.

5.2 Future Scope

The experimental results indicate that deuterium implantation coupled with N_2O annealing brings about the most improvement in device performance. However, there was a significant variation between the results for different implantation conditions. Further research might be required to arrive at the optimum implant-anneal regime.

The low thickness of the gate oxide could have resulted in lowered oxide quality. It might prove beneficial to validate the results for higher thicknesses, such as 100 Å.

The use of a metal film in place of the polysilicon as the gate electrode could prove useful, as the process temperature required for metal deposition is much lower for aluminum. Further, alternative methods of oxide growth such as plasma deposition could be tried.

Finally, the experiments need to be extended to MOSFET devices to fully utilize the benefits of hot electron degradation resistance.

CHAPTER 6

REVIEW OF MEMS HEATER

6.1 Background

The author was a participant in another project being carried out at the NJIT, involving the design and testing of MEMS microheaters for the development of a FET-based chemical sensor device. This chapter presents a brief introduction to and description of the project and the preliminary results obtained so far using the fabricated heaters. This part of the project was aimed at the validation of the design of microchannel heaters to serve as microtraps for the accumulation and release of organic compounds.

6.2 Introduction

The detection and quantitative measurement of volatile organic compounds (VOCs) at trace levels in air emissions is of considerable importance in view of the hazard they pose to public health and their contribution to the formation of ozone in the troposphere. The development of analytical instrumentation which is rapid and sensitive, while at the same time being cheap and portable, is necessary to monitor VOCs in the environment and emission sources. This has traditionally involved collecting the sample in the field using whole air samplers like Tedlar bags or canisters, and analysis of the sample in the laboratory. This makes for a significant delay between sampling and analysis. A technique for the continuous on-line monitoring of VOCs using the concentration and injection of VOCs collected by membrane extraction by means of a microtrap has been

developed [*18*]. The microtrap consists of a small diameter (0.50 mm ID) metallic tube packed with an adsorbent. VOCs passed along with a stream of carrier gas are adsorbed by the microtrap. Electrical heating of the microtrap releases the adsorbed gases as a concentration pulse, which is injected into a gas chromatograph column. The small size makes for low response time.

The aim of this project is to combine the principle of automated online chemical analysis using a microtrap with routine microelectronic technologies to exploit the advantages offered by semiconductor technology. Specifically, microelectromechanical system (MEMS) devices offer the advantage of easy miniaturization, the capability to include multiple sensors on a single chip, integration of different devices on the same substrate to fabricate an integrated sensor, and once the design has been validated, cost reduction through mass fabrication.

The project draws on many demonstrated technologies. Insulated Source Field-Effect Transistor (ISFET) based sensors have been used [*19,20*] to measure individual gases in air and water. Localized heating to temperatures upto 400 °C, and the sensing of this heating using integrated sensors has been demonstrated [*21,22*], as has been the manipulation of extremely small volumes of samples using microfabricated pumps.

It is envisaged to fabricate a microconcentrator with micromachined channels etched into silicon wafer and then coated with thin-film stationary-phase adsorbent to act as the microtrap [*18*]. The carrier gas, also known as the mobile phase, is a high-purity gas that transports the gas sample of interest through the column; it is usually selected to maximize its chemical inertness with respect to the sample gas and the stationary-phase column coating.

The column is coated with a stationary phase that chemically interacts with the injected gas sample to produce a propagation delay for each of its components based upon their heat of adsorption and vapor pressure. This phenomenon results in the physical separation of the individual constituents along the length of the channel.

The microconcentrator is used to concentrate analytes and then rapidly heated to desorb the organics as a concentration pulse which acts as a GC injection. In a later stage of the project, the desorbed gases are proposed to be detected as the change in work function of a CHEMFET made by depositing chemical-sensitive polymers on the gate of a FET transistor.

The microconcentrator can be electrically heated with a pulse of electric current so that the analytes desorb as a concentration pulse sharp enough to serve as an injection for GC separation or detection by a transistor sensor.

6.3 Objective

The objective during this initial phase of the project was to

(1) fabricate the microchannels serving as microtraps in the sensor

(2) incorporate a resistance heater in the microchannel for heating of the channels

(3) test the channels for their temperature characteristics under different applied voltages

(4) compare the heating characteristics of channel heaters formed using doped silicon and metal as the conducting film in the channels.

Channels of different dimensions were fabricated on silicon wafers by etching them in the silicon substrate. This was followed by deposition of metal/boron doping and

patterning to form the conducting layer. Spin-on glass was deposited on the metal deposited wafer after its design had been validated.

6.4 Fabrication

6.4.1 Process Flow

The process flow for the fabrication is described in the flow diagram below. Since the microchannels were fabricated by both boron doping and metal deposition, both the processes are presented in the flow diagram.

Starting material
(5" silicon wafer, p-type, <100> orientation, 1-5 Ω-cm resistivity)

↓

Deposition of denuding oxide

↓

Stripping of denuding oxide

↓

Deposition of oxide

↓

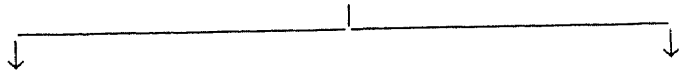
LPCVD deposition of silicon nitride

↓

Photolithography to pattern nitride to form channels

↓

KOH Etching of silicon



Patterning for boron implantation

↓

Boron implantation through photoresist

↓

Stripping of photoresist

↓

Annealing

Deposition of Al-Cu-Si by sputtering

↓

Patterning of metal

↓

Etching of metal

↓

Stripping of photoresist

↓

Spinning - on of glass

6.4.2 Simulations

Two different approaches to forming the conducting layer in the microconcentrator channel were tried out. On the one hand, metal was deposited in the channels by sputtering and on the other, the silicon substrate was heavily doped with boron by implantation to increase its conductivity. The second approach has the advantage of simplicity as it does not require an additional conducting layer and allows for easier adhesion of polymer layer. Furthermore, success in achieving elevated temperatures with this approach has been demonstrated [22].

In order to arrive at the proper energy and dose of the boron source for the implantation, simulations were carried out using SUPREM (**S**tanford **U**niversity **PR**ocess **EM**ulator). The conditions utilized for the initial implantation schedule are presented in Table 6.1, and the simulation is presented in Fig. 6.1.

Table 6.1 Initial Implantation Schedule

Implantation energy	80 keV
Implantation dose	1 x 10^{14} atoms / cm^2
Anneal	40 min
Additional anneal	20 min

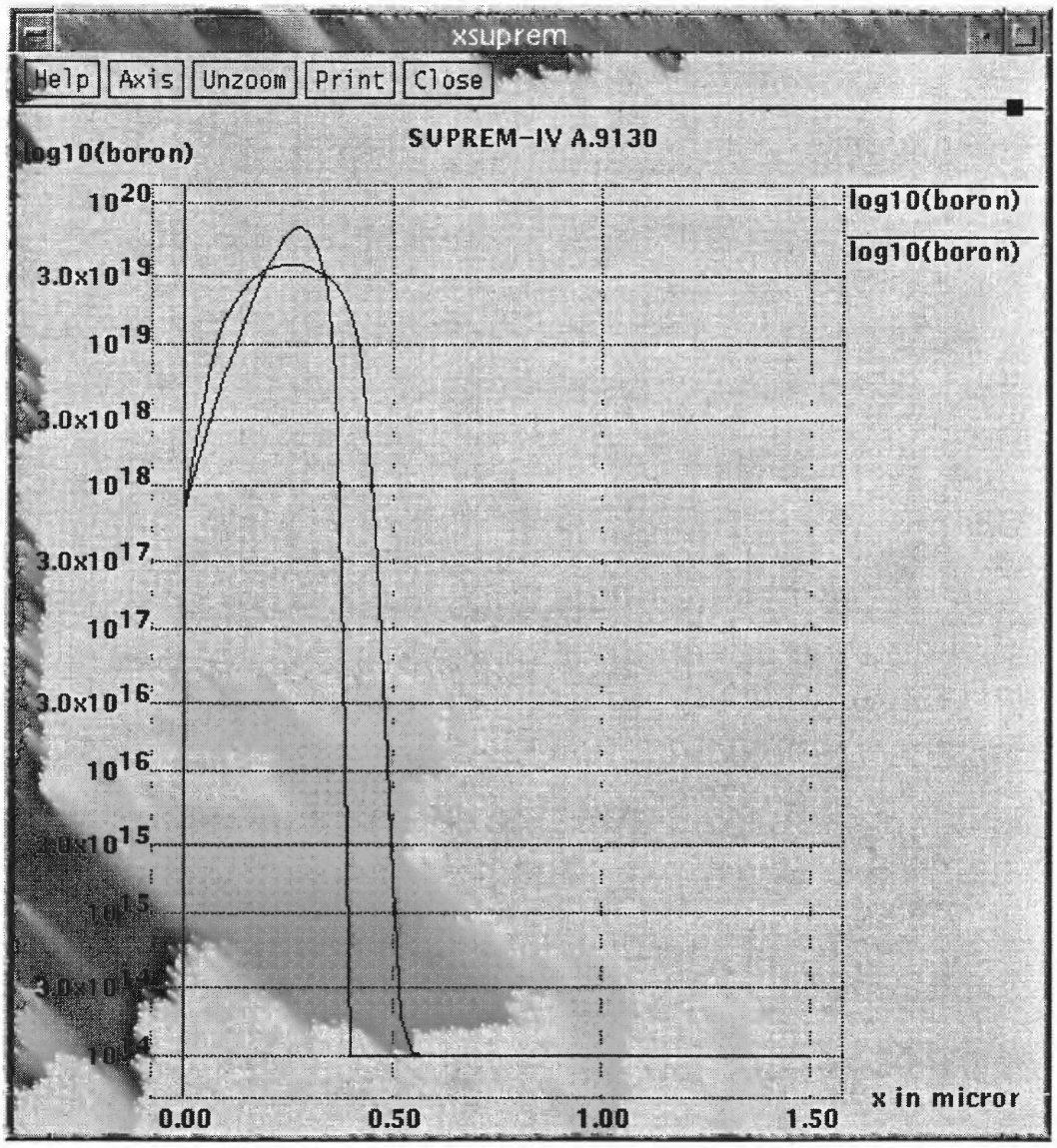


Fig. 6.1 Boron concentration profile in silicon after implantation and annealing

Since the measurement results obtained from this wafer were not very favorable, a second implantation schedule involving a higher dose and energy was also tried out. The conditions used in the implantation are summarized in Table 6.2.

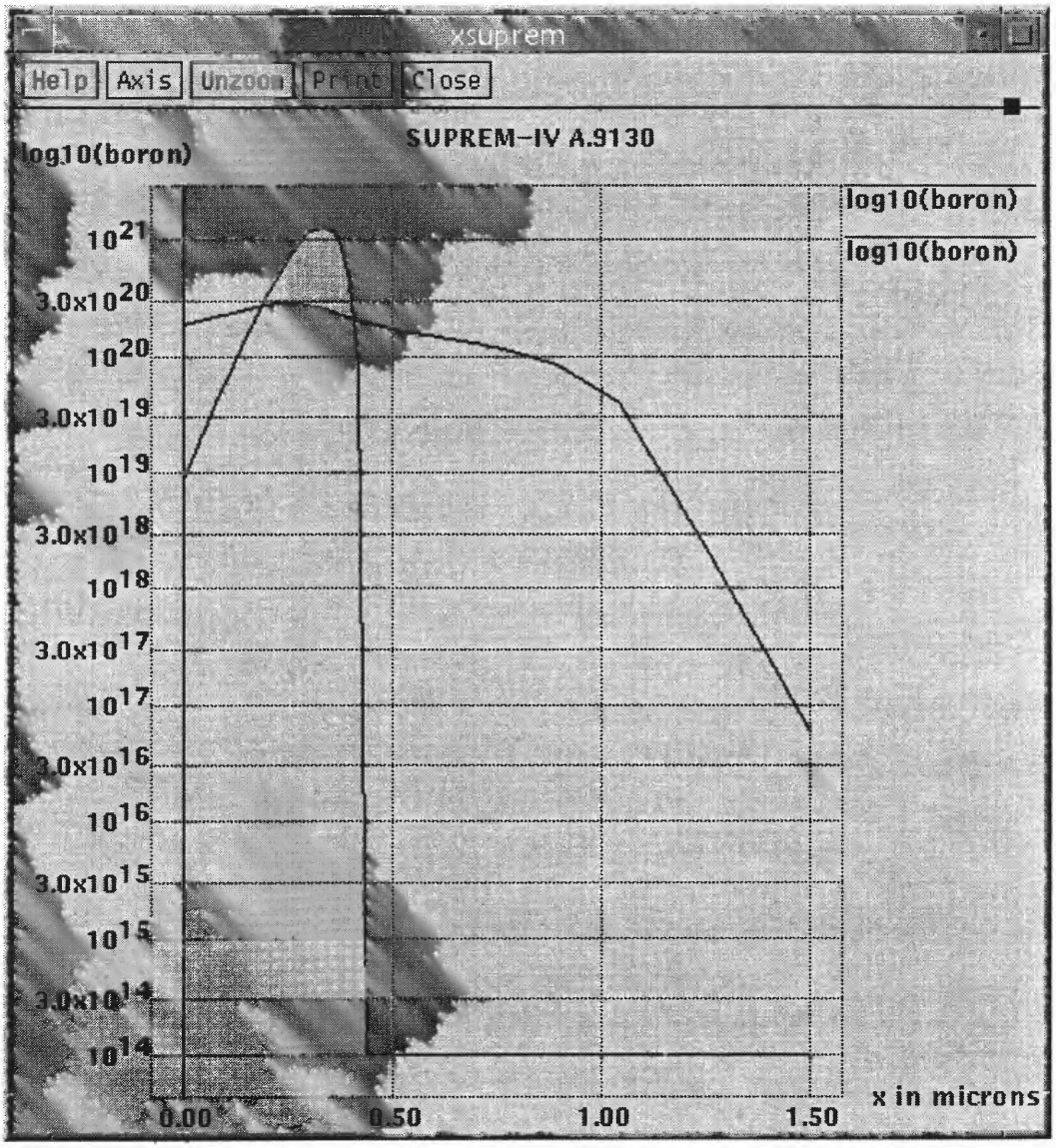


Fig. 6.2: Boron concentration profile in silicon following implantation and annealing; alternative implantation regime

The simulation results are presented in Fig. 6.2. As can be seen, this results in a higher implanted concentration of dopant and a much more uniform distribution upto a greater depth within the substrate following annealing.

Table 6.2 Second Implantation Schedule

Implantation energy	100 keV
Implantation dose	2×10^{15} atoms / cm^2
Anneal	20 min
Additional anneal	20 min

6.5 Measurements

6.5.1 Measurement Methodology

Channels of different *L/W* ratios were formed on the wafer. The ratio *L/W* refers to the ratio of length to width of a component, and is an important determinant for the resistance of a circuit element, as the resistance is given by

$$R = \rho \frac{1}{t}\left(\frac{L}{W}\right) \tag{6.1}$$

where R = resistance of element

ρ = resistivity

t = thickness of conducting film

L/W = total length to width ratio

The L/W ratios used were

Table 6.3 *Microconcentrator channel L/W ratios*

Channel Designation	Overall L (μm)	W (μm)	L/W
A	60668	456	133
B	186620	456	409
C	133892	46	2911
D	104446	30	3481.5
E	192996	12	16080.5
F	197950	12	16496
G	81956	4	20489

A Micromanipulator probe station was used to probe the wafers. Enlarged contact pads formed at the ends of channels were used to supply electric signals to the channels. The signal was applied through 0.5 mm tip stainless steel probes. A HP Harrison 6200B DC Power Supply was used as the power source. The Tegam 871 Digital Thermometer in conjunction with Kapton P-08505-86 K thermocouple probes (tip diameter 0.254 mm) was used to measure the temperatures in the channels.

Different voltages were applied to the individual channels and the current through the channel and the temperature as a function of time were recorded. An analysis of the results obtained is presented in the next section.

6.5.2 Experimental Results

6.5.2.1 Comparison of Boron Implanted and Metal Deposited Microconcentrators:

A comparison was made of the temperature rise attainable in the microheaters under similar conditions of applied voltage for the wafers with boron implantation and metal deposition. Implantation rather than thermal diffusion was used to achieve higher doses of boron. Following the implantation, the wafer was annealed in a nitrogen ambient to homogenize the boron distribution within the substrate.

It was observed that the temperature rise obtainable with the boron doped wafer was not appreciably high. Since the surface conductivity depends on the dopant concentration, and inadequate annealing can result in a bulk of the implanted ions being distributed too deep into the substrate to contribute to conductivity, two different implantation regimes were tried out. Furthermore, each was subjected to two different anneal times to seek to improve the heating characteristics. The comparison of the maximum obtainable temperature rises at an applied voltage of 40 V for each channel type are summarized in Table 6.4.

It is apparent that for the range of the *L/W* ratios chosen, the temperature rise realizable by using boron-doped silicon is much lower than that using metal. As discussed in section 6.5.4, the resistance of the channels formed in boron doped channels is very high, resulting in extremely low currents and hence low heating. This could be the result of insufficient implant dose or anneal time, or inadequate distribution along the walls of the channel. With the design used, heating the microchannel using doped silicon was not practicable because the small temperature rise is going to be insufficient to

sufficiently desorb gases for injection, more so as the silicon is to be further coated with the stationary phase adsorbent.

Table 6.4 Maximum Temperature Rise Measured for all Channels at 40 V

Channel Type	L/W	Temperature Rise (°C)				
		METAL	BORON Implanted, Annealed			
		Metal (Al)	80 keV $1x10^{14}/cm^2$ 40m ann.	80 keV $1x10^{14}/cm^2$ +20m ann.	100 keV $2x10^{15}/cm^2$ 20m ann.	100 keV $2x10^{15}/cm^2$ +20m ann.
Thickness		1μm	0.3 μm	0.4 μm	1μm	1.2 μm
A	133	156.6	7.9	2.1	17.9	2.0
B	409	362.7	7.8	11.6	39.3	37.0
C	2911	6.1	0.0	1.1	19.0	13.1
D	3481.5	0.0	1.7	1.7	0.0	1.3
E	16080.5	29.7	0.0	1.9	15.3	15.4
F	16496	4.2	0.0	0.0	5.5	4.1
G	20489	0.0	0.0	0.0	10.9	7.0

6.5.2.2 Comparison of Channel Configurations: Table 6.3 shows the effect of channel dimensions on the results. From eq. (6.1), a larger *L/W* ratio results in a higher resistance for the channel. Under an application of the same external voltage, this would cause a smaller current through the channel. Since the joule heating upon passage of a current depends upon the square of the current, as

$$P = I^2 R. \tag{6.2}$$

where P = power

I = current

R = resistance

Hence a smaller current results in lower heating of the microheater. Based on this, the temperatures attained should have been in order of decreasing *L/W*. However, while a general trend of this nature was observed, this could not be comprehensively established. Except for the channels A and B, and to a lesser extent E, all other temperature rises were small.

The deviation from expected results was more true of the narrower channels. Even for channels with the same width, the temperatures attained were widely varying. For some of the narrowest channels, viz. D and G, a current was undetectable. These phenomena suggest that the anomaly in temperatures recorded could possibly have to do with improper placement of probes due to inadequate design, as the probe tip was of a size approaching the channel width.

Table 6.5 Maximum Temperature Rise at 40 V with and without Spin-on Glass

Channel Type	L/W	Temperature Rise (°C)	
		Uncoated metal (1 μm thickness)	Metal with spin-on glass (1 μm thickness)
A	133	362.7	115.8
B	409	156.6	27.0
C	2911	6.1	3.9
D	3481.5	0.0	0.0
E	16080.5	29.7	17.9
F	16496	4.2	3.5
G	20489	0.0	0.0

6.5.2.3 Temperature Profile for Metal-Deposited Channels with and without Spin-on Glass: Of the seven channel configurations made on the wafer, significant temperature rise could not be realized on four of the channel types. For this reason, the following data is presented only for three significant channels.

The sensor design requires the adsorbent species to be lining the channels. Since organic polymers have a low adhesivity for silicon or metal, a coat of glass of approximate thickness 0.5 μm was specially applied on the channels by spinning them over the surface of the wafer. The initial temperature rises with and without the spun-on glass coating are presented in Fig 6.3 for an applied voltage of 30 V (except for channel B, where the voltage is 34 V).

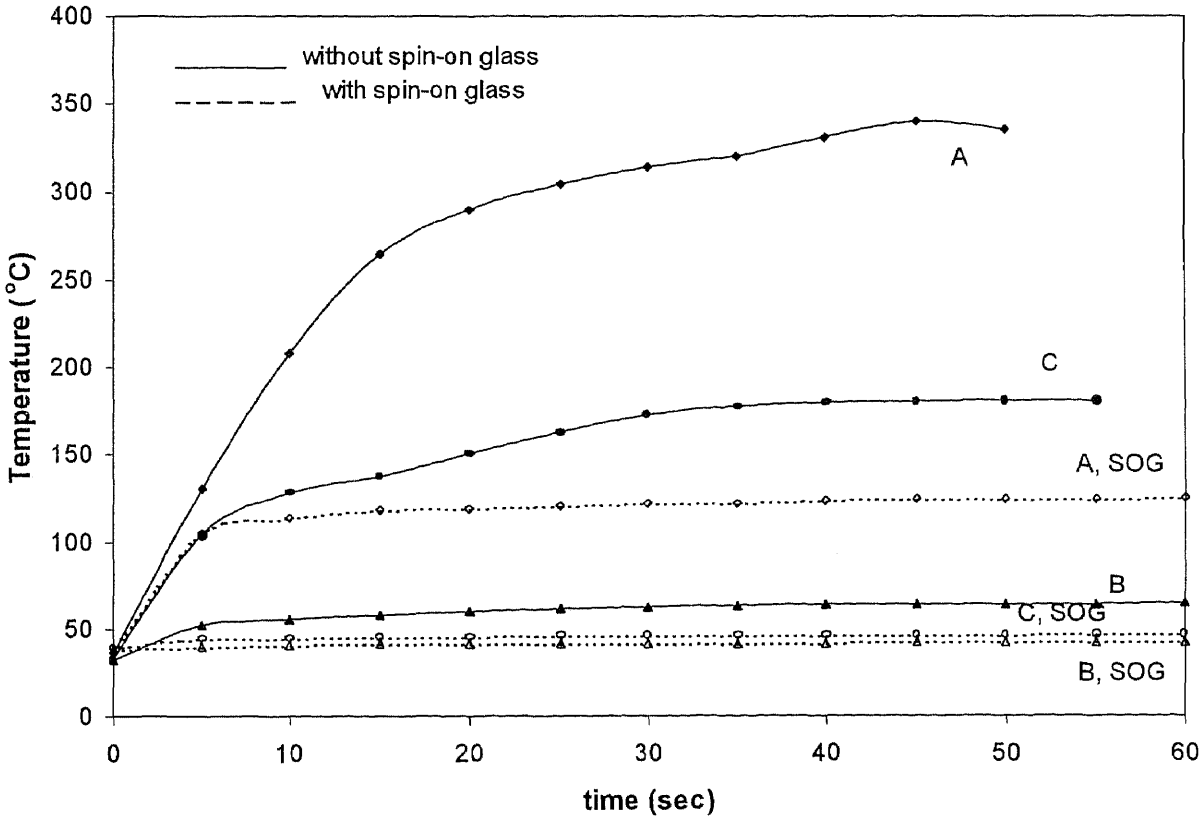


Fig 6.3 Initial temperature rise for channels A,B and C with and without spin-on glass deposition at an applied voltage of 30 V

For most cases, the temperature stabilizes much before a one minute duration. This is important, as for the power supplied to serve as an injection to release a pulse of trapped gases, the temperature rise has to be in the form of a sharp spike.

For an applied voltage of 30 V, temperatures of upto 390 °C are realized in the absence of spin-on glass coating. The maximum temperature attained on any channel was 392°C at 43 V.

The channel type A proves to be the best configuration for attaining high temperatures because of its low *L/W* ratio and hence higher current, combined with a relatively large width (456 μm) making for more precise placement of probe tips. Even with the coating of spin-on glass applied, a temperature of up to 125 °C is attained.

In general, the temperatures attained with the spin-on glass coated were significantly lower than in without it, except for channel type B where they were comparable. Since the final sensor is to have a further adsorbent layer on top of the glass coat, it is imperative to identify and improve upon the best design for the channel.

6.5.3 Voltage Dependence of Temperature Rise

The temperature rises were recorded at different applied voltages for the metal-deposited wafers with and without spin-on glass deposition. Voltages from 15 upto 50 V were applied to the channels. Voltages lower than 15 V did not produce appreciable currents in a majority of the channels. Usually the maximum current carrying capacity and hence the temperature rise was exhibited at a voltage in the vicinity of 40 V. The use of higher voltages did not appreciably increase the current, but sometimes caused a termination of conduction upon continued use.

In general, the temperature attained by a channel increases with the applied voltage, both for wafers without spin-on glass (Fig. 6.4) and with spin-on glass (Fig. 6.5).

The only exception was channel type C on the bare wafer, where the temperature attained at 40 V was less than that 25 V. This could possibly be attributed to experimental error.

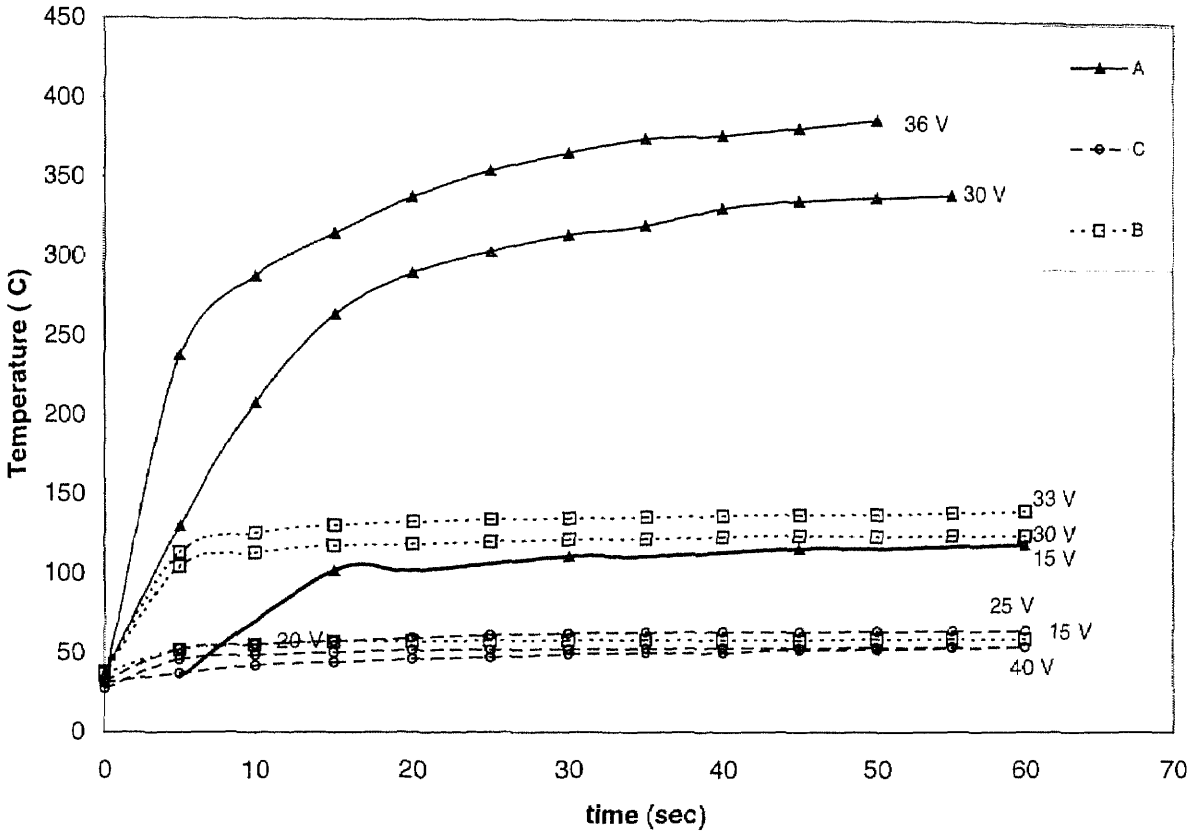


Fig 6.4 Initial temperature rise for channels A,B and C without spin-on glass as a function of applied voltage.

The temperatures at voltages near 30 V were significantly larger than at 15 V. However, the rate of this increase fell at higher voltages.

The wafers with and without spin-on glass deposition show the same trends of incraese of temperature with an increase in applied voltages. However, the temperatures

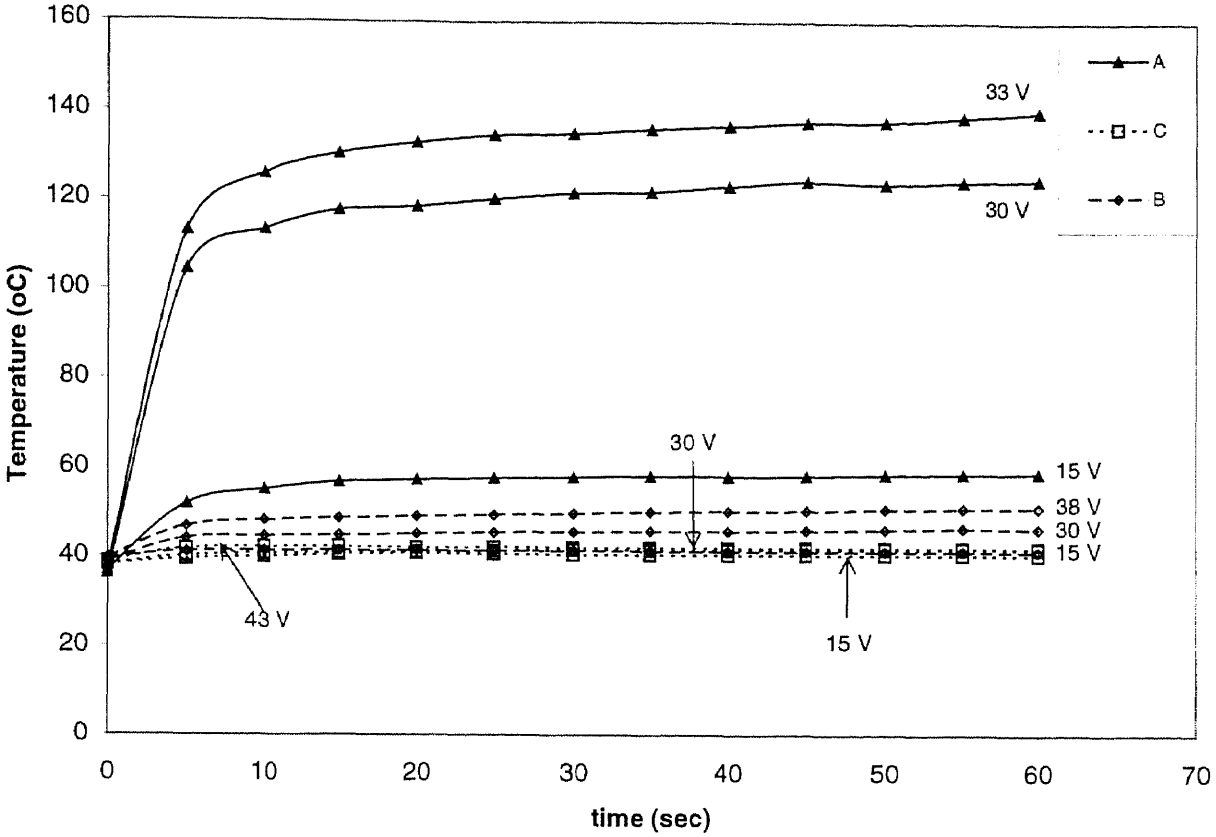


Fig 6.5 Initial temperature rise for channels A,B and C with spin-on glass deposited as a function of applied voltage.

realized with spin-on glass were in each case lower than at comparable voltages for the wafer with no glass deposition.

6.5.4 Resistance and Power Calculations

The resistance of a microtrap channel can be calculated from the resistivity of the material if the thickness of deposit and the L/W ratio are known, from the relation given by eq. (6.1).

For the boron-deposited wafer, the resistivity of the material is a function of the mean impurity concentration in the material. The concentration following annealing was

determined from SUPREM simulations (Figs. 1,2). The resistivity for this concentration was read off from Fig. 21, *Physics of Semiconductor Devices, 2nd ed.* by S. M. Sze. The resistances thus derived for the different channels and the experimentally obtained resistances are detailed in Table 6.3.

For the initial implant (80 keV, 1×10^{15} / cm^2, 40 min anneal at 900 °C),

Concentration = 5×10^{19} / cm^3 at depth 0.4 μm

$\Rightarrow \quad \rho \cong 1.8 \times 10^{-3}\ \Omega$ - cm

For the second implant (100 keV, 2×10^{16} / cm^2, 20 min anneal at 1050 °C)

Concentration = 1×10^{20} / cm^3 at depth 1 μm

$\Rightarrow \quad \rho \cong 5 \times 10^{-4}\ \Omega$ - cm

The second implant scheme brings about an order of magnitude improvement in the conductivity of the channels. However, even this does not prove to be sufficient, suggesting that if boron doping of polysilicon is to be used, a complete redesign of the channel dimensions might be required to make the device workable.

Tables 6.2 and 6.3 together indicate that extra annealing usually improves the conductivity of the polysilicon. The annealing serves to bring more impurity ions closer to the surface, thus aiding in conduction.

The measured resistivities are often an order of magnitude lower than the calculated ones. This indicates that the theoretically derived values are conservative estimates.

Channel type	L/W	Boron Implant at 80 keV, 1 x 10^{15} / cm^2			Boron Implant at 100 keV, 2 x 10^{16} / cm^2		
		Calc.	Expt.		Calc.	Expt.	
		Resistance (kΩ)	Resistance (kΩ)	Power (W)	Resistance (Ω)	Resistance (Ω)	Power (mW)
A	133	6.0	0.54	.34	665	66.7	41.69
B	409	18.4	1.95	1.22	2000	125	78.12
C	3481	156	25.5	15.94	17400	1600	1000
D	2911	131	-	-	14600	73	45.62
E	16080	724	-	-	80400	80	50
F	20490	922	-	-	102500	100	62.5
G	16500	742	-	-	82500	1000	625

Table 6.6 Calculated and measured resistances and measured power for individual channels

The measured resistivities were not in complete agreement with the design channel L/W parameters. This was truer of the smaller channels. Inadequate channel dimensions resulting in improper placement of the probe tips on the channel ends were the probable cause. Future design needs to incorporate well-defined larger areas for placement of probes.

6.6 Conclusions

The experiments validate the principle of a microconcentrator which can be heated to release the adsorbed species. Sufficiently high temperatures and short temperature rise times were observed using microchannels deposited with metal. However, since the final

unit would have the adsorbent phase deposited over the spin-on glass layer, the temperature available to the trapped gases is going to be much reduced from the temperatures generated in the metal. The temperatures realized with spin-on glass were significantly less than for bare metal, suggesting that the most efficient channel structure for heat generation has to be identified and further refined.

In a large number of cases, the voltage required to generate sufficiently high temperatures was of the order of 30-40 V, which means the power requirement was in the range of 30-40 W. This is a rather large power requirement and further research might be necessary to lower this requirement.

The next part of the experiment would be to form a complete channel by bonding two separate wafers and performing the temperature rise measurements after depositing the adsorbent phase by spin-on methods.

APPENDIX A

LPCVD THEORY AND DEPOSITION CONDITIONS

A.1 LPCVD Reactor

The LTO deposition reactor is schematically shown in the figure A.1. This reactor was manufactured by Advanced Semiconductor Materials America Inc. (ASM America, Inc.) as a polysilicon micro-pressure CVD system. The horizontal reaction chamber consists of a 13.5 cm diameter fused quartz tube and a 144 cm long encapsulated with a three-zone, 10 kwatt, Thermco MB-80 heating furnace. The flow of oxygen into the reaction chamber is controlled by a MKS mass flow controller.

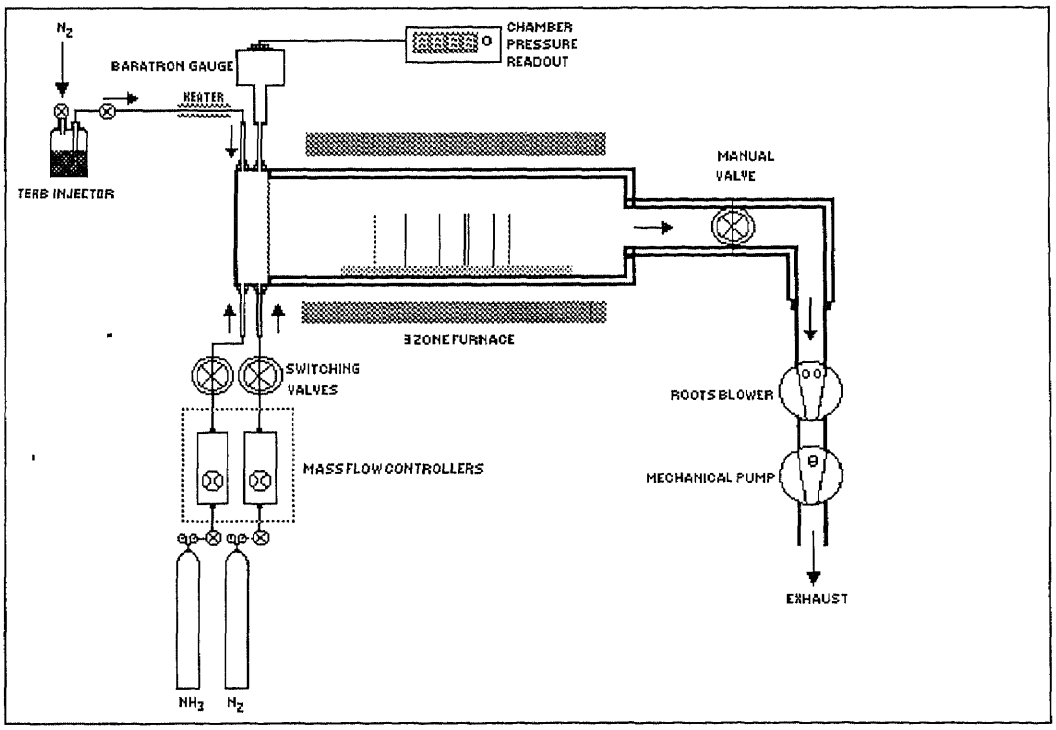


Fig. A.1 Schematic representation of the LPCVD reactor

The other end of the reaction chamber is connected to a vacuum station comprised of a Leybold-Heraeus Trivac dual stage rotary vane pump backed by a Leybold-Heraeus roots pump to create the necessary vacuum in the system. An oil filter system is used to filter unnecessary particles from oil and thereby increasing the lifetime of the pump.

A.2 Flow Chart Showing the Oxide Deposition

P-clean

5:1 H_2SO_4: H_2O_2

110^{O}C, 10minutes

↓

Rinse Hot DI Water

10 minutes

↓

Rinse Cold DI Water

5 minutes

↓

Spin Dry

↓

Furnace Pre-clean

100:1 H_2O:HF

1 minute

↓

Rinse Cold DI Water

10 minutes

↓

Spin Dry

↓

LPCVD LTO

APPENDIX B

POLYSILICON DEPOSITION AND DOPING METHODS

B.1 Methods of Polysilicon Deposition

Polysilicon can be deposited in a variety of ways and using many types of precursors.

APCVD : Atmospheric pressure chemical vapor deposition

LPCVD : Low pressure chemical vapor deposition

PECVD : Plasma enhanced chemical vapor deposition

Polysilicon occurs on occasion when the growing of single-crystal epitaxial silicon is attempted, and it will generally have large grain size. These occurrences are sporadic and undesirable. When polysilicon films are to be used in there own right, a uniform and generally small grain size is required, which usually implies a considerably lower deposition temperature than that used for epitaxy. Further, the applications themselves normally require relatively low-temperature depositions in order to minimize diffusion and /or wafer damage. Typically, low-pressure tube depositions with silane as the silicon source are now used. An **LPCVD** reactor provides for a very economical deposition and silane decomposition proceeds at temperatures as low as 400°C. When much thicker polysilicon layers are required-for example, in dielectrically isolated wafers speed of deposition, as well as an inexpensive feedstock is desirable, and the process used is much like that of high-temperature epitaxy.

The deposition rate of LPCVD polysilicon depends on temperature, silane partial pressure, and whether or not doping gas such as phosphine, arsine or diborane is present.

B.2 Flow Chart for Polysilicon Deposition

P-clean

5:1 H_2SO_4:H_2O_2

110°C

10 minutes

↓

Rinse Hot DI

10 minutes

↓

Rinse Cold DI

5 minutes

↓

Spin Dry

↓

Deposit Polysilicon

Target thickness = 3200 Å

B.3 Flow Chart for Polysilicon Doping

P-clean

5:1 H_2SO_4:H_2O_2

110°C

10 minutes

↓

Rinse Hot DI

10 minutes

↓

Rinse Cold DI

5 minutes

↓

Spin Dry

↓

Phosphorus Diffusion

APPENDIX C

SPUTTERING

C.1 Sputtering

While evaporation is widely used to deposit aluminum and its alloys, sputtering of these materials has become more practical because of the increased deposition rate and more uniform step coverage and contact hole filling. Also, when refractory metals are used, either sputtering or CVD is required to achieve realistic throughput in manufacturing.

Sputter is similar to a billiard-ball event. Ions are accelerated in an electric field toward a target of material to be deposited, where they 'knock-off' (sputter) target atoms. The sputtered ions then deposit onto wafers, which are conveniently placed facing the target. Argon is typically used for sputtering because it is inert and readily available in pure form. It is ionized by colliding with high electrons in the chamber, and then accelerated in an electric field toward the negatively biased target. The momentum of ions incident on the target is then transferred to surface atoms of the target material, causing their ejection. Therefore, during sputter deposition, material is removed from the target and deposited onto the wafers.

The incident energy must be large enough to dislodge target atoms, but not too large to cause penetration into the target material (ion implantation). Typical sputtering ion energies range from 500-5000 eV. The number of atoms sputtered from the wafer surface per incident ion is defined as the sputter yield. This number varies from 0.5-1.5, depending on the momentum of ions and their angle of incidence.

There are many types of sputtering. They are:

a) Ion beam sputtering

b) Magnetron sputtering

c) Reactive sputter deposition

d) Bias sputter deposition

C.2 Flow Chart Showing the Sputter Deposition Process

P-clean

5:1 H_2SO_4:H_2O_2

110°C

10 minutes

↓

Rinse Hot DI

10 minutes

↓

Rinse Cold DI

5 minutes

↓

Spin Dry

↓

Deposit Aluminum

↓

Measure sheet resistivity

APPENDIX D

PHOTOLITHOGRAPHY

D.1 Introduction

The basic steps of the lithographic process are shown in the figure. The photoresist (PR) is applied as a thin film to the substrate(e.g. SiO_2 on Si), and subsequently exposed through a mask. The mask contains clear and opaque features that define pattern to be created in the PR layer. The areas in the PR exposed to light are made either soluble or insoluble in a specific solvent known as developer. In the case when irradiated (exposed) regions are soluble, a positive image of the mask is produced in the resist. Such material is therefore termed a positive photoresist. On the other hand, if the non-irradiated regions are dissolved by the developer, a negative image results. Hence the resist is termed a negative resist. Following development, the regions of SiO_2 no longer covered by resist, are removed by etching, thereby replicating the mask pattern in that oxide layer.

The resist is seen to perform two roles in this process. First, it must respond to exposing radiation in such a way that the mask image can be replicated in the resist. Second, the remaining areas of resist must protect the underlying substrate during subsequent processing. In fact, the name resist evolved from the ability to resist etchants.

Although both negative and positive resists are used to manufacture semiconductor components, the higher resolution capabilities of positive resists have virtually made them exclusive choice for VLSI applications. Conventional positive optical lithographic processes and resists are capable of producing images on VLSI

substrates with dimensions as small as 0.8-1.5μm. For submicron features, however, diffraction effects during exposure may ultimately cause other higher resolution techniques to replace optical lithography

D.2 Description of Lithographic Process

The first step in this process is the application of photoresist. The photoresist is applied by spin coating technique. This procedure involves three stages: a)dispensing the resist solution onto the wafer; b) accelerating the wafer to the final rotational speed; and c) spinning at a constant speed to establish the desired thickness (and to dry the film).

The dispensing stage can either be accomplished by flooding the entire wafer with resist solution before the beginning the spinning, or by dispensing a smaller volume of resist solution at the center of the wafer and spinning at lower speeds to produce a uniform liquid layer across the wafer.

In the next stage, the wafers are normally accelerated as quickly as is practical to the final spin speed and finally spinning at the constant speed to obtain desired thickness.

In this work, the rotational speed was maintained at 1500 rpm. The wafers were spun at this speed for a period of 20 seconds. This gave a photoresist of 2μm thickness. Prior to exposure the wafers are baked for one minute at 115°C or for a period of 20 minutes in an air oven maintained at the same temperature in order to remove the moisture present. The baking is done to remove the moisture from the wafer. Moisture can reduce the adhesion.

The exposure was carried out using a SUSS MA6 mask aligner. The lamphouse is equipped with a 350 W mercury high pressure lamp and a SUSS diffraction reducing

optics. The usable wavelength falls between 350-450 nm. The lamphouse has an ellipsoidal mirror, and a 45° cold light mirror. The type of exposure lamp depends on the optical range selected. The cold light mirror reflects the desired short wavelength UV light through a fly's lens and transmits the longer wavelengths to a heat sink located in the bottom of the lamphouse. The lamphouse also contains a condenser lens, diffraction reducing lens plates, a 45° turning mirror and a collimation lens. A holder is provided in the mirror house for a filter. SUSS diffraction reducing exposure system provides a high resolution over the entire exposure area, resulting in steep resist edges and small diffraction effects.

The wafers were exposed for 20 seconds in the SUSS MA6 mask aligner. After the exposure the wafer must undergo "development" in order to leave behind the image which will serve as a mask for etching. The developer is poured on the wafer and allowed to develop for 30 second before it is spun at a high rpm(~2000-3000). This procedure is repeated for another 10 seconds of development. The wafer is then washed with DI water and spun again to remove all the water. The wafers are baked as before to rid of the moisture that may been absorbed by the substrate. The windows are then inspected under the microscope for their integrity.

APPENDIX E

ETCHING

E.1 Introduction

In general etching process is not completely attainable. That is etching process are not capable of transferring the pattern established by protective mask into the underlying material. Degree to which the process fail to satisfy the ideal is specified by two parameters: bias and tolerance. *Bias* is the difference between the etched image and mask image. *Tolerance* is a measure of statistical distribution of bias values that characterizes the uniformity of etching.

The rate at which material is removed from the film by etching is known as etch rate. The units of *etch rate* are Å/min, μm/min, etc. Generally high etch rates are desirable as they allow higher production throughputs, but in some cases high etch rates make the control of lateral etching a problem. That is since material removal can occur in both horizontal and vertical directions, the horizontal etch rate as well as vertical etch rate may need to be established in order to characterize an etching process. The lateral etch ratio, L_R, is defined as the ratio of the etch rate in a horizontal direction to that in a vertical direction. Thus:

$$L_R = \frac{\text{Horizontal etch rate of material}}{\text{Vertical etch rate of material}} \qquad \text{.....(eq. E.1)}$$

In the case of an ideal etch process the mask pattern would be transferred to the underlying layer with a zero bias. This would then create a vertical edge of the mask.

Therefore the lateral etch rate would also have to have been zero. For nonzero L_R, the film material is etched to some degree under the mask and this effect is called undercut. When the etching proceed in all directions at the same rate, it is said to be *isotropic*.

By definition, however, any etching that is not isotropic is anisotropic. If etching proceeds exclusively in one directions (e.g. only vertically), the etching process is said to be completely anisotropic. A typical anisotropic etch profile is shown in the figure.

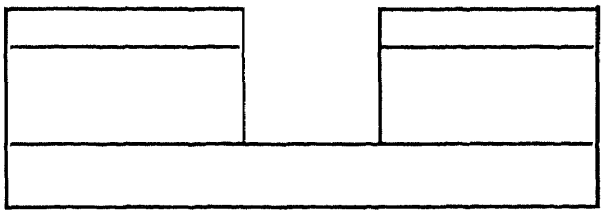


Figure E.1 Anisotropic etch profile

So far it has been assumed that the mask is not attacked by the etchant and did not consider that the layers under the etched film can also be attacked by the etchant. In fact both the mask and the underlying layer materials are generally etchable, and these effects may play a significant role in specifying etch processes. The underlying material subject to attack may either be the silicon wafer itself, or a film grown or deposited during a previous fabrication step. The ratio of the etch rates of different materials is known as *selectivity of an etched process*. Thus both the selectivity with respect to the mask material ands the selectivity with respect to the substrate materials are important characteristics of an etch process.

E.2 Wet Etching Technology

Wet etching processes are generally isotropic. They are inadequate for defining features less than 3μm. Nevertheless for those processes that involve patterning of linewidths greater than 3μm, wet etching continues to b a viable technology.

The reason wet etching has found widespread acceptance in microelectronic fabrication is that it is a low cost, reliable, high throughput process with excellent selectivity for most etch process with respect to both mask and substrate materials.

In general wet etch processes can be broken down into three steps:

- diffusion of the reactant to the reacting surface
- reaction
- diffusion of reaction products from the surface.

The second step can obviously be further differentiated into adsorption prior to, and desorption subsequent to, the actual reaction step. The slowest of the steps will be rate controlling. That is, the rate of that step will be the rate of the overall reaction.

Chemical etching can occur by several processes. The simplest involves dissolution of the material in a liquid solvent without any change in the chemical nature of the dissolved species. Most etching process, however, involve one or more chemical reactions. Various types of reactions my take place, although one commonly encountered in semiconductor fabrication is oxidation-reduction (redox). That is, a layer of oxide is formed, then the oxide is dissolved and the next layer of oxide is formed, etc.(e.g. wet etching of Si and Al)

In semiconductor applications, wet etching is used to produce patterns on the silicon substrate or in thin films. A mask is typically used to protect desired surface

regions from the etchant and this mask is stripped after the etching has been performed. Thus, when choosing a wet etch process, in addition to selecting an etchant, a suitable masking material must be picked to have good adhesion to the underlying films, good coating integrity and ability to withstand attack by etchant. Photoresist is the most commonly encountered masking layer, but sometimes it falls short in this role. Problems involved include loss of adhesion at the edge of the mask-film interface due to etchant attack, and large area failure of the resist. Large area failures of the resist are usually due to differential stress buildups in the substrate and mask layers. Also bubble formation during etching process can lead to poor pattern definition, particularly at the pattern edges.

E.3 Dry Etching

Wet etching processes are typically isotropic, therefore if the thickness of the film being etched is comparable to the minimum pattern dimension, undercutting due to isotropic etching becomes intolerable. One alternative pattern transfer method that offers the capability of non-isotropic(or anisotropic) etching is "dry etching". As a result, considerable effort has been expended to develop dry etch processes as replacements for wet etch processes.

The overall goal of an etch process, as mentioned earlier, is to be able to reproduce the features on the mask with fidelity. This should be achievable together with control of following aspects of etched features:

- the slope of the feature sidewalls(e.g. the slope of the sidewalls of the etched feature should have the desired angle, in some cases vertical)

- the degree of undercutting(i.e. usually the less undercutting the better)

There are a variety of dry etch processes. The mechanism of etching in each type of process can have a physical bias (e.g. glow-discharge sputtering), a chemical bias (e.g. plasma etching), or a combination of the two (e.g. reactive ion etching, RIE, and reactive ion beam etching RIBE).

In processes that rely predominantly on the physical mechanism of sputtering (including RIBE), the strongly directional nature of the incident energetic ions allows substrate material to be removed in a highly anisotropic manner (i.e. essentially vertical etch profiles are produced). Unfortunately, such material mechanisms are non-selective against both masking material and materials underlying the layers being etched. That is, the selectivity depends largely on sputter yield differences between materials. On the other hand, purely chemical mechanisms for etching can exhibit very high selectivity against both mask and underlying substrate material. Such purely chemical etching mechanisms, however, typically etch in an isotropic fashion.

By adding a physical component to a purely chemical etching mechanism, however the shortcomings of both sputter based and purely chemical dry etching process can be surmounted. Plasma etching process is a purely chemical process and reactive ion etching processes is a physical/chemical process.

The basic concept of plasma etching is rather direct. A glow discharge is utilized to produce chemically reactive species from a relatively inert molecular gas. The etching gas is chosen so as to generate species, which react chemically with the material to be etched, and whose reaction product is volatile. An ideal dry etch process based solely on chemical mechanisms for material removal, can thus be broken down into six steps:

- reactive species are generated in a plasma
- these species diffuse to the surface of the material being etched
- the species are adsorbed on the surface
- a chemical reaction occurs with the formation of a volatile by product
- the by product is desorbed from the surface
- the desorbed species diffuse into the bulk of the gas

If any of these steps fail to occur, the overall etch process ceases. Many reactive species can react rapidly with a solid surface, but unless the product has a reasonable vapor pressure so that desorption occurs, no etching takes place. Reactive ion etching as described before is an anisotropic etching technique. After the lithographic step, windows are formed on the photoresist layer. The silicon nitride is exposed in these windows. RIE is carried out to remove this silicon nitride and expose the underlying silicon substrate.

E.4 Description of the Reactor for RIE

Plasma etching systems consist of several components: a) an etching chamber, that is evacuated to reduced pressures; b) a pumping system for establishing and maintaining the reduced pressure; c) pressure gauges to monitor the pressure in the chamber; d) a variable conductance between the pump and etching chamber so that the pressure and flow rate in the chamber can be controlled independently; e) an RF power supply to create the glow discharge; f) a gas handling capability to meter and control the flow of reactant gases; and g) electrodes. There are several types of commercially available etching systems. They include

1. barrel reactors
2. "downstream" etchers
3. parallel-electrode(planar) reactor etchers
4. stacked parallel-electrode etchers
5. hexode batch etchers
6. magnetron ion etchers

The RIE system in the class 10 clean room, where the fabrication of the V grooves was carried out, is a stacked parallel electrode etching system.

The stacked parallel electrode etcher is a small batch machine capable of handling six wafers at a time. Its unique design provides an individual pair of electrodes for each wafer thereby combining some of the advantages of a single wafer and batch etchers. Operating chamber pressures and RF power densities can be kept in the ranges between those of low pressure, low power density hexode batch etchers, and high pressure.

APPENDIX F

SIMULATION

F.1 SRIM Simulation

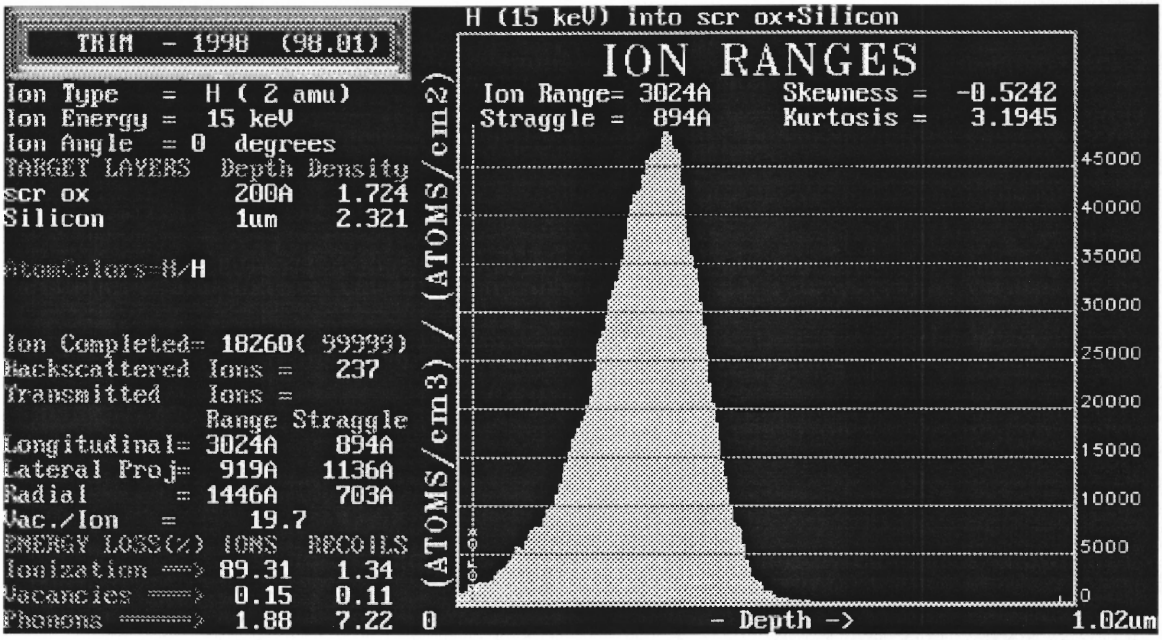


Fig. F.1.1 SRIM simulation of implantation of $^{2}H_{1}$ at 15 keV, $1x10^{14}/cm^{2}$.

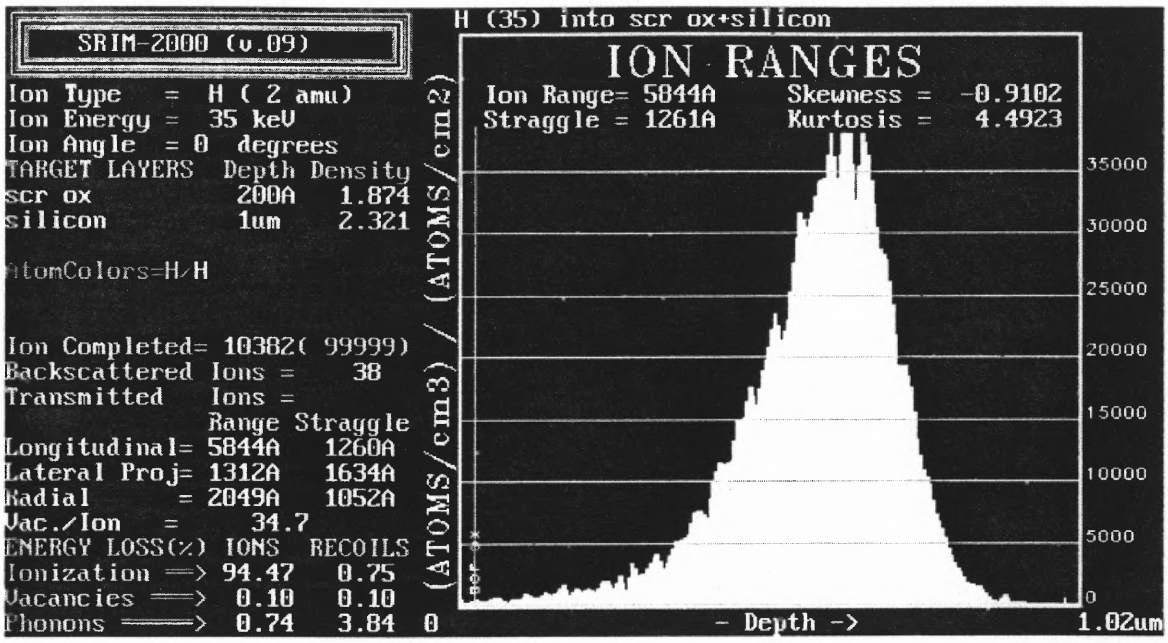


Fig. F.1.2 SRIM simulation of $^{2}H_{1}$ at 35 keV, $1x10^{14}/cm^{2}$.

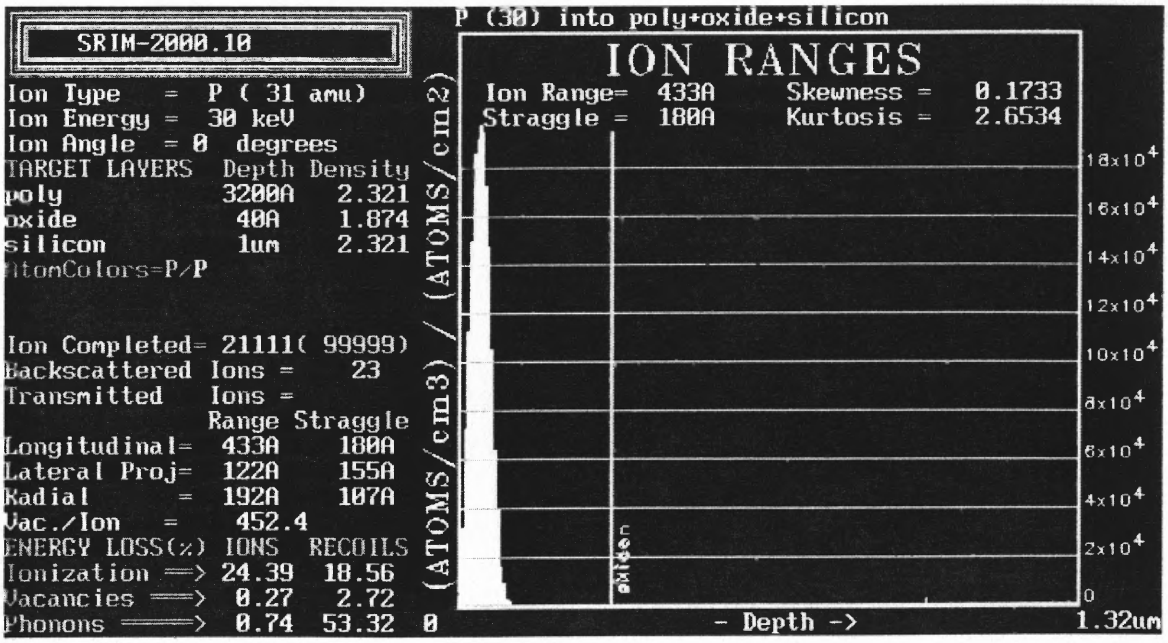


Fig. F.2.1 SRIM simulation of P^{15} implantation of polysilicon at 30 keV, $1x10^{16}/cm^{2}$.

APPENDIX G

SIMS ANALYSIS

G.1 SIMS Analysis in Absence of Deuterium

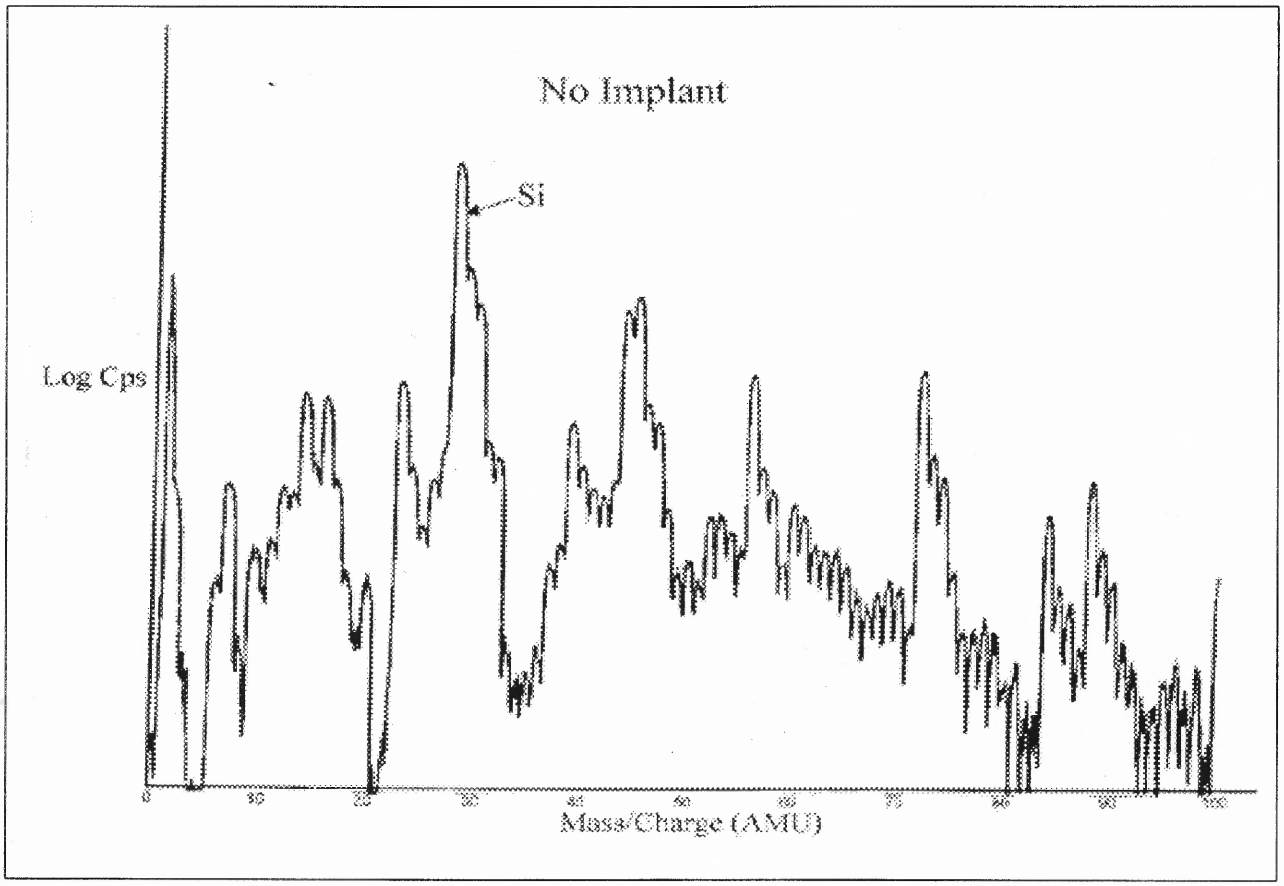


Fig. G.1 SIMS analysis for wafer with no deuterium implanted. There is no peak corresponding to deuterium in the analysis.

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