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Electrical characteristics of novel heterojunction diodes of thin relaxation semiconductors/p-Si/

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ABSTRACT

ELECTRICAL CHARACTERISTICS OF NOVEL HETEROJUNCTION DIODES OF THIN RELAXATION SEMICONDUCTORS / P-Si

by
Hyung Joo Lee

The relaxation semiconductor is defined as one in which the dielectric relaxation time (τ_d;resistivity times permittivity) is greater than lifetime (τ_o). Non-hydrogenated amorphous Silicon Carbide (SiC) and KrF excimer laser induced disordered Si were used for the relaxation semiconductors. Both semiconductors have high resistivity, wide energy gap, and numerous defects. A novel heterojunction diode, consisting of those semiconductors on p-type crystalline Silicon (c-Si), was fabricated. In the diode structure, an injecting contact was made on the relaxation material and a Schottky barrier contact was made on the c-Si.

Electrical characteristics of both diodes were found to have interesting effects: negative capacitance, negative resistance, space charge limited current, and bistable switching with long term memory. During the C-V measurement of a disordered Si/c-Si heterojunction diode, for the first time, a constant negative capacitance of 1520pF was observed from - 10v to 10v at 1MHz. This negative capacitance was considered as an inductive behavior. The measured inductance value was approximately 16.7μH at 1MHz. The inductance was proportional to $1/\omega^2$ in the variation of frequency and 14.74mH at 30KHz as measured by a LCR analyzer. In an a-SiC/c-Si heterojunction diode, a negative capacitance was also observed in both biases. The inductance value was 36μH above 3.5v and below - 3.5v at 1MHz. The shape of negative capacitance between - 3.5v and 3.5v was

parabolic and the inductance, near zero bias, was 30μH. The inductance was almost constant between 1MHz and 30KHz.

An inductive part of the heterojunction diode was derived theoretically using the relaxation theory and Shockley theory. The inductance was either constant if $\omega\tau_d < 1$, or proportional to $1/\omega^2$ if $\omega\tau_d > 1$. Moreover, a circuit model of the heterojunction diode was also developed. The negative capacitance, C_{test} showed $|C_{test}| = 1/\omega^2 L_{test}$ at the circuit model. Computer simulation also showed negative capacitance similar to that of the experiment.

It was proposed that conductivity modulation, by carrier injection in a thin relaxation semiconductor, causes an inductive behavior, and the relaxation would be more pronounced by the carrier screening of impurities. The novel heterojunction diode may replace a physical inductor in microelectronics.

ELECTRICAL CHARACTERISTICS OF NOVEL HETEROJUNCTION DIODES OF THIN RELAXATION SEMICONDUCTORS / P-Si

by
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APPROVAL PAGE

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K. Sohn and H. Lee. "Electrical Characteristics of Thin Metal/Semiconductor Junction with a Thin Disordered Layer Induced by Excimer Laser." *Symposium-Crystallization and Related Phenomena in Amorphous Materials, Materials Research Society.*, Boston. MA. Nov. 29-Dec. 3, 1993.

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This dissertation is dedicated to
Jesus Christ and my parents

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CHAPTER 1

INTRODUCTION

The objective of this dissertation is to investigate the electrical characteristics of novel heterojunction diode structures consisting of excimer laser induced disordered Si on c-Si, as well as non-hydrogenated amorphous SiC on c-Si. The electrical characteristics of I-V and C-V demonstrated interesting negative capacitance and negative resistance effects, as well as space charge limited current and bistable switching with long term memory. Disordered Si and amorphous SiC are called relaxation semiconductors. They were proposed by van Roosbroeck in 1970 [1], although the relaxation theory was not popular at that time. The relaxation state is obtained when the dielectric relaxation time $\tau_d = \rho\varepsilon$, (the resistivity, ρ and the dielectric constant, ε are material constants), exceeds the carrier lifetime τ_o. The opposite inequality holds for the conventional or lifetime semiconductor. Typical examples of a relaxation semiconductor are high-resistivity wide-energy-gap materials and amorphous alloys. The usual condition of local electrical neutrality is no longer obeyed in the relaxation semiconductors, and it is replaced by the condition of near-zero net recombination in space charge regions.

In both diodes structures, injecting contacts (Ohmic contacts) are made on the relaxation materials (disordered Si, and a-SiC), and Schottky barrier contacts are made on the p type c-Si substrate. This structure, with regard to contacts, is opposite to that of a conventional thin-film epitaxial diode [2]. In a thin-film epitaxial diode, usually a Schottky barrier contact is on the epitaxial layer and an Ohmic contact is made on the substrate.

The development of excimer lasers, which generate powerful ultraviolet light, has enhanced their potential use in technological application, e.g., as a lithography in ultra large-scale integration, and recrystallization technology etc. Laser-recrystallized silicon thin films are of technological interest for fabricating high performance thin film transistors, silicon-on-insulator devices, and 3-D integration [3]. A KrF (248nm) excimer laser was used to make an epitaxial disordered Si irradiating on a p-type c-Si surface. It was also used for Ohmic contact with formation of the p^+ layer between the Al contact and p-type Si irradiating on the Al contact.

A model, of effective barrier reduction, due to the p^+ layer, was developed under thermionic field emission mechanism using WKB approximation [4], and tunneling theory [5]. Computer simulation, with the model, showed that at least 4nm of p^+ layer would be needed for a complete Ohmic (field emission) contact in Si with doping of $10^{18}/cm^3$. When a strong laser output (excitation voltages of 24kv) was irradiated on the Al contact, a high resistivity disordered Si was made just below the thin p^+ layer.

During the I-V measurements, Ohmic behavior, negative resistance, space charge limited current, and bistable switching with memory were observed. The phenomenon of negative resistance is explained by both the modification of band structure, due to the strain effect from laser induced damage, and the decrease of carrier density due to the capture of the carrier by the defect which is generated with laser irradiation. The switching phenomenon is explained by carrier trap and release by the defect.

During the C-V measurements, for the first time, a very interesting negative capacitance was discovered from -10V to 10V in both heterojunction diodes. This negative capacitance phenomenon was proved to be an inductive behavior through the use of a LCR-Analyzer. This means that the novel heterojunction diode acts as

an inductance diode. An inductive part of the diode was derived theoretically using the relaxation theory and the Shockley theory. Moreover, A circuit model of the diode was derived and had good agreement with both experiments when appraised by a LCR analyzer, C-V measurement and computer simulation.

It is proposed that conductivity modulation, by carrier injection in a thin relaxation semiconductor, would result in the inductive behavior of a diode. When the inductive behavior is dominant for the junction capacitance of a diode, negative capacitance, which is an inductive behavior, is demonstrated by the C-V measurement. In ordinary diodes, it is difficult to produce the inductive reactance. Even though it is developed, the junction capacitance of the diodes normally masks the inductive effect.

In the past, there has been considerable interest in possible ways to simulate inductors with semiconductor devices. Inductive behavior for forward bias was simulated theoretically in a narrow base PIR diode (P stands for an emitter which is well doped with acceptors, I stands for a high resistivity intrinsic base, R stands for a high recombination contact) by Ladany [6] in 1960. A decreasing negative capacitance was observed in a $NiSi_2$-Si diode above 0.48V at 200K by Wu [7] in 1990.

Inductance coils, that defy miniaturization efforts, are an order of size larger than those of other passive and active components. One way to circumvent this problem is to design all inductances out of conventional circuits before constructing the integrated analogs. As an example, the transistor oscillators with resonant L-C circuits has been replaced by an R-C phase-shift oscillator. This procedure is not satisfactory in all cases. Through the use of this novel heterojunction diode, the possibility of using the negative capacitance effect, to simulate inductance, is presented on the bases of theoretical and experimental results.

CHAPTER 2

DEVICE STRUCTURE AND FABRICATION METHODS

2.1 Experimental Preparation

P-type (100) Si wafers (doping of $10^{18}/cm^3$, and $2 \cdot 10^{15}/cm^3$) were used for the substrates of devices. The wafers were cleansed chemically to remove grease, and oxide in P-clean and HF-clean stations of the 'NJIT MICROELECTRONICS CENTER'. In the P-clean station, wafers were immersed into H_2O_2 : H_2SO_4 (100:1) at 110° C for 10 minutes, and they were then washed with hot (80° C) DI water. In the HF-clean station, H_2O : HF (100:1) was used for 1 minute to remove oxide. Wafers were also washed with DI water (23.7°C)for 2 minutes. After cleaning the wafers, the wafers were dried by a spindryer for 3 minutes.

A pulsed KrF (248nm) excimer laser (Lambda-Physik, EMG 101E) was used for irradiation on both the c-Si surface and Al dot contacts (diameters of 1 to 3 mm) on c-Si with excitation voltages of 20 - 24 kv, and 1-10 pulses per second. The laser spot size was approximately 1-3 mm x 10 mm. Laser focus was adjusted to avoid Al contact evaporation.

A rough and abraded surface can be achieved with the irradiation on c-Si. It results in an Ohmic contact due to tunneling though the Schottky barrier by high surface recombination, and the laser induced numerous defects. Also, a high resistivity, disordered Si layer just below the rough surface can be made due to the damage. During the irradiation on the Al contact, the localized heat treatment leads to the formation of a thin p^+ layer between the Al and p-Si. P-Si is dissolved in the Al, up to its solubility limit, and Al is diffused into Si, and the thin p^+ layer results in an Ohmic contact. Figure 2.1 shows a KrF excimer system.

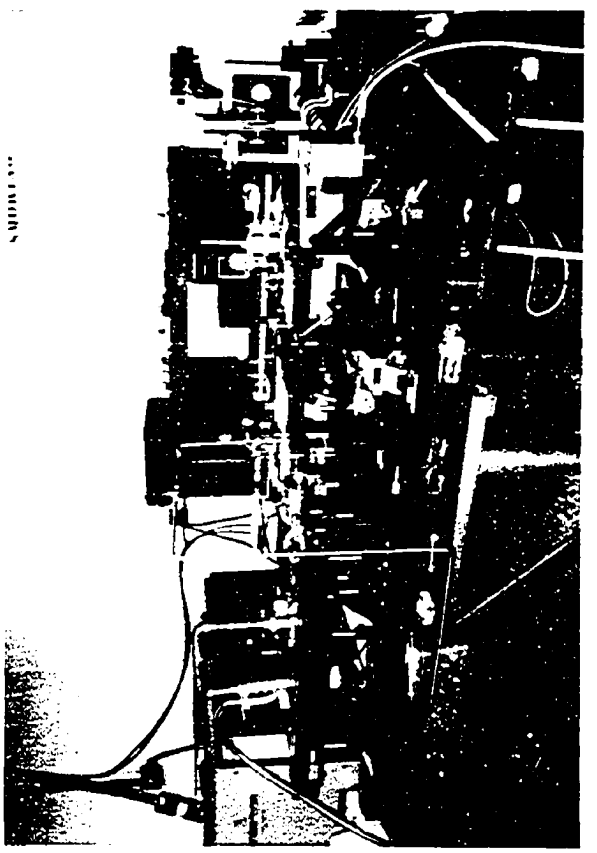


Figure 2.1 A KrF excimer laser system

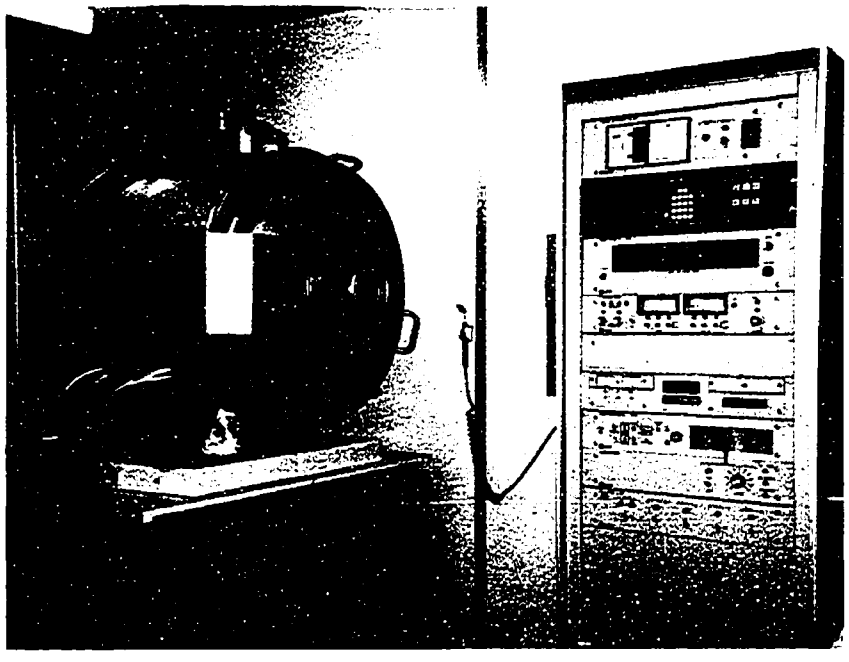


Figure 2.2 A magnetron sputtering system (VARIAN 3125)

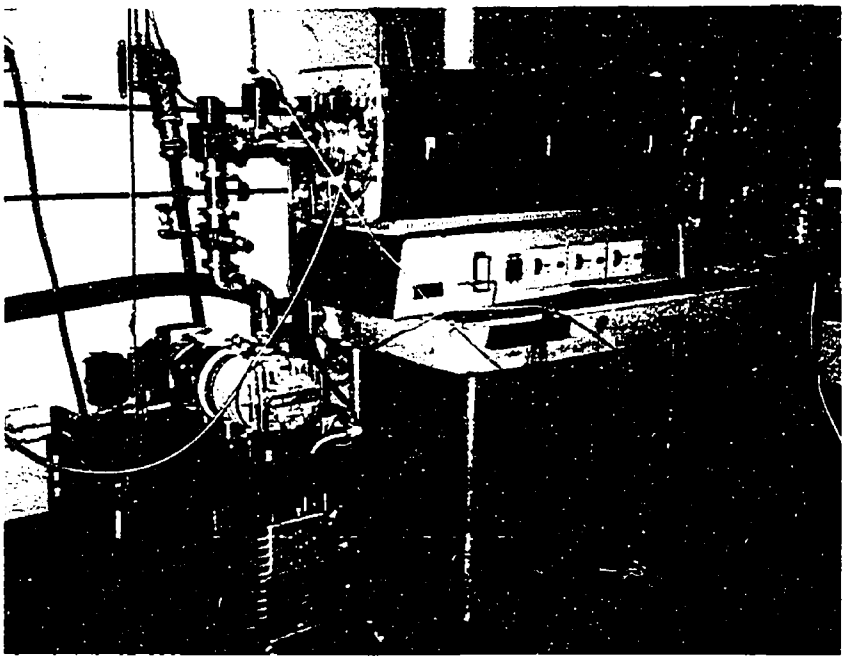


Figure 2.3 A LPCVD system (Linderberg)

A 'VARIAN 3125' magnetron sputtering system was used for pure Al (99.9999 %) deposition. The first base pressure was $7.0 \cdot 10^{-7}$, and the second base pressure was $1.0 \cdot 10^{-6}$. The pressure of deposition was 2.0 mTorr, and the deposition rate was 1nm/sec. The substrate temperature was 100°C, and although the substrate temperature is usually set to 300° C, it was set to 100°C to avoid an Al spike and to increase the Al nucleus density. Figure 2.2 shows the 'VARIAN 3125' sputtering system.

An LPCVD (Low Pressure Chemical Vapor Deposition) system (Linderberg) was used for non-hydrogenated amorphous SiC deposition. DTBS (Di-Tertiary Butyl Silane) was decomposed for amorphous SiC deposition. The deposition temperature was about 825°C, and pressure was 100 mTorr. Wafers were put far away from the gas inlet to make a thin a-SiC deposition. Figure 2.3 shows the 'Linderberg' LPCVD system.

The measurements of electrical characteristics (I-V, C-V) were obtained through the use of a 'KEITHLEY 236', and a 'HP-4145B Semiconductor Parameter Analyzer'. Interesting negative capacitance was measured by a 'HP-4145B semiconductor Analyzer', a 'HP-4284A LCR Analyzer' and a 'PAR 410 C-V Plot system'.

A 'KRATOS X-SAM 800' AES (Auger Electron Spectroscopy), a SEM (Scanning Electron Microscopy), a AFM (Atomic Force Microscopy), and an Ellipsometry were used to acquire the structural characteristics.

2.2 Fabrication Procedure

1. The device was made by deposition of pure Al (99.9999%) on p-type (100) Si (doping of $10^{18}/cm^3$) with a VARIAN-magnetron sputtering system. The diameters of the Al dot contacts were approximately 1 mm. One side of the Al

contacts was irradiated by a pulsed KrF Excimer laser (excitation voltages of 20-22kv, period of 1 sec) to achieve a p^+ layer.

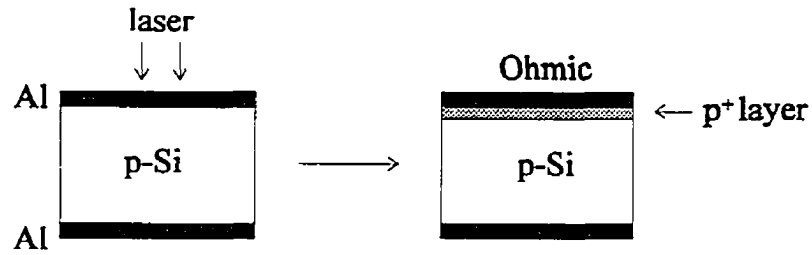


Figure 2.4 One side laser-Ohmic contact

2. The Excimer laser with a higher power output (excitation voltages of 24 kv, period of 1 sec, 200mJ/pulse) was used. A high resistivity-disordered layer (20 nm) was made underneath the Ohmic layer contact. The thickness of the p^+ (8 nm) and high resistivity layer were obtained by C-V doping profile.

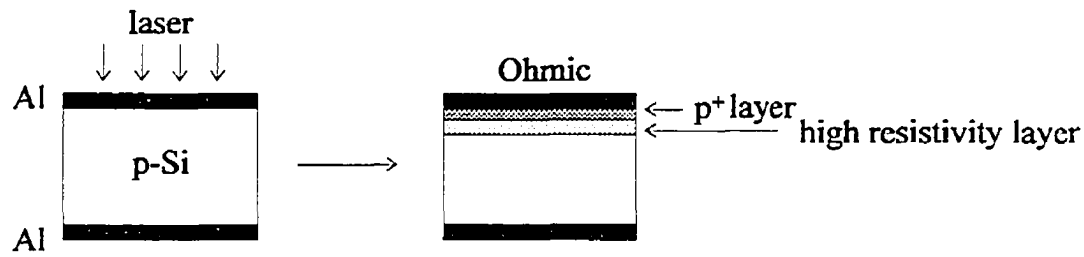


Figure 2.5 One side laser-Ohmic contact with a high resistivity layer

3. A device structure without the p+ layer was made by high power laser irradiation (excitation voltages of 24kv, period of 0.1 sec) on one side of the Si wafer (10^{15} / cm^3, (100)). Using this technique, Al-spike effect, Al-evaporation, and the effect of non-uniform Al thickness in structure 2 can be avoided.

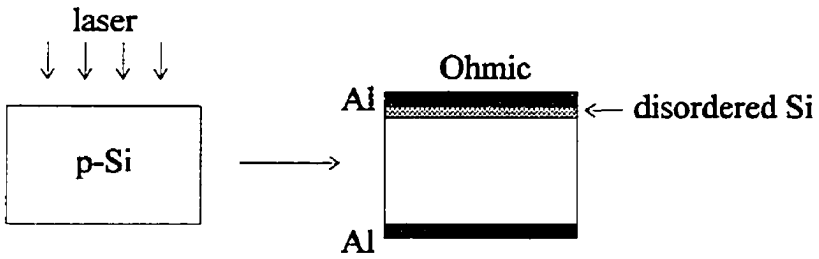


Figure 2.6 A disordered Si/c-Si heterojunction diode

4. Thin non-hydrogenated intrinsic amorphous SiC, which has lot of defects, was deposited on one side of the Si (10^{15} / cm^3, (100)) by LPCVD. The Al contacts were sputtered on after LPCVD. The thickness of the a-SiC was much less than 100 nm according to a measurement made at the AT&T Bell Lab. and my best estimate of the thickness is 20 nm through the use of Ellipsometry.

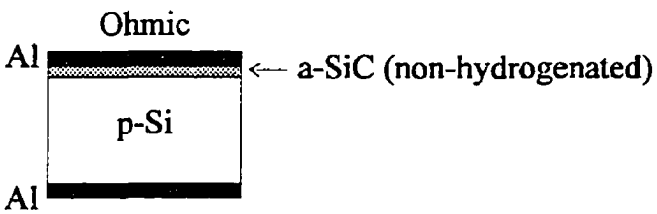


Figure 2.7 An amorphous SiC/Si heterojunction diode

CHAPTER 3

THEORETICAL WORK

3.1 Background

3.1.1 Relaxation Theory

Dielectric relaxation time (resistivity times dielectric constant), greater than diffusion-length life time, defines the relaxation semiconductor. Typical examples include high-resistivity, wide-energy-gap materials, as well as, amorphous materials. Van Roosbroeck [1] was the first to point out the difference in behavior, under minority carrier injection, between conventional lifetime semiconductors and relaxation semiconductors, although his suggestions were not immediately popular. In the relaxation case, the usual condition of local electrical neutrality is no longer obeyed, and it is replaced by the condition of near-zero net local recombination, in space-charge regions, whose decay depends on dielectric relaxation. A principal result of the analysis by van Roosbroeck, of carrier transport in relaxation-case semiconductors, is the prediction of recombinative injection. This effect is manifested by reduction of the density of majority carriers through the injection of minority carriers. The characteristic approximation of nearly zero recombination can actually be realized, in a stable steady-state space charge region, through the carrier injection. Minority carrier injection can accordingly give substantial depletion of majority carriers. The space charge may be largely that of fixed charges: ionized donors or acceptors that have become uncompensated and any traps that have become occupied. This depletion effect is directly connected with recombination = 0. Through the use of Boltzmann statistics, the product NP, of the electron and hole concentrations, then equals its thermal equilibrium value, the square of the intrinsic concentration, $N_0 P_0 = n_i^2$.

In terms of excess concentration ΔN and ΔP, it follows that $N_0\Delta P+P_0\Delta N+\Delta N\Delta P$ is zero. Then, an injected steady state electron concentration ΔN gives $\Delta P = - P_0\Delta N/(N_0+\Delta N)$. In a p-type semiconductor with $P_0>>N_0$, for example, $\Delta P = - P_0$, or substantially complete depletion of majority carriers, thus results for ΔN after recombination that need merely be large compared with the equilibrium concentration n_0. This major effect, essentially non-linear and large signal, can occur whether or not there is trapping. Consider the diagram on the left of Figure 3.1. Here, we have rectangular hyperbola, PN = constant. The starting point is N_e, the equilibrium concentration of electrons, P_e, the equilibrium concentration of holes. We shall suppose an increase in hole concentration by ΔP_0 has been brought about. We would now have a positive space charge. In a traditional material, like Si, in which the dielectric relaxation time is very small, that extra positive charge will almost immediately attract an extra negative charge consisting mainly of free electrons, of equal magnitude, into the neighborhood. Then, the extra electrons and holes (an equal number) will recombine in a time corresponding to the lifetime. This is the behavior that we traditionally associate with a lifetime semiconductor. Now let us consider something non-traditional, a dielectric relaxation time greater than lifetime. Again, let us contemplate an increase in the hole concentration by ΔP_0. Once more, there is a positive space charge, but the recombination time is now very small. Very quickly, recombination will take us to the rectangular hyperbola, because that curve defines the locus where no further recombination can take place. The reason for this is that the recombination rate depends directly on the product PN. However, at this stage, the system is not yet neutral. It regains neutrality by creeping back to the starting point along the rectangular hyperbola, and that will happen roughly within a dielectric relaxation time.

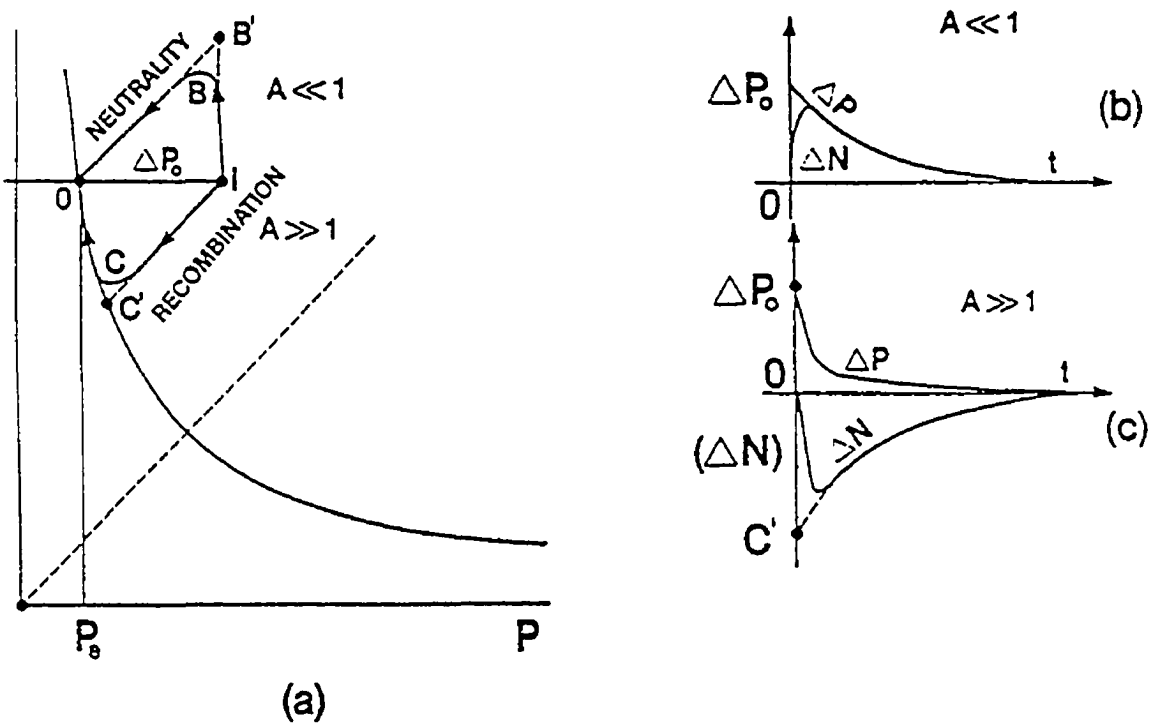


Figure 3.1 Minority carrier augmentation in a homogeneous space element. $A = \tau_D/\tau_0$. (a) Relationship between electron and hole concentration. (b) Time dependences. A << 1, lifetime semiconductors. (c) A >> 1, relaxation semiconductor. N = normalized n; P = normalized p. [8]

Thus, the behavior is essentially different in the two cases; the majority carrier concentration is diminished here. The relaxation case is expected whenever a sufficiently short life time occurs in conjunction with sufficiently high resistivity. For a dielectric constant of 12, the dielectric relaxation time, in seconds, is about 10^{-12} times the resistivity in Ωcm. Thus, with lifetime equal to 10^{-8} sec, a resistivity somewhat higher than 10^{4} Ω cm. would be required. At room temperature, such conditions may be met with Si, and are usually readily met with GaAs, GaP, and other semiconductors whose energy gaps are appreciably wider than about 1eV. Although difficult to determine with any precision in GaAs and GaP, lifetime is generally less than 10^{-8} sec in these materials. Since most studies have not utilized GaAs or GaP in the high resistivity range [9], the lifetime case, rather than the relaxation case, is the one that has usually been observed with crystals of these or any semiconductors. The amorphous materials [10-11], however, are quite generally relaxation semiconductors; through short range order, an energy band model applies, although with certain significant modifications. Typical of many are high, near-intrinsic resistivities that are generally not very impurity sensitive, and have very short carrier lifetimes with pronounced trapping that strongly limits drift mobilities. In materials that can also have a crystalline form, resistivities are usually orders of magnitude higher than for the crystals, and conductivity band gaps are wider. Disordered semiconductors are qualitatively somewhat similar to the amorphous ones, and means for producing relaxation semiconductors include subjecting crystals to beam of neutron, electrons, or other radiation.

3.1.2 Injecting Contact and Space Charge Limited Current

We use the terminology, Ohmic contact, reservoir contact, and injecting contact interchangeably. They all denote contacts capable of current injection with only a

relatively small fraction of the applied voltage absorbed across the contact. The energy-band basis, for the injection of electrons into an insulator or a wide-bandgap material, is easily understood by simply inspecting the relevant energy-band diagram. Figure 3.2(a) shows a metal vacuum contact and Figure 3.2(b) an electron injecting, metal-insulator contact, both contacts being in thermal equilibrium. F_0 is the Fermi level, E_{vac} the lowest vacuum level, and E_c the lowest conduction band level. The two diagrams are clearly very similar. Electrons will boil off from the metal into the conduction band of the insulator just as they do from the heated cathode into vacuum. The electrons, in the metal available for emission, are those thermally excited to an energy sufficiently large to overcome the energetic barrier at the emission surface. The interface dipole energy barrier Ψ, at the metal insulator contact, can be substantially smaller than the corresponding work function barrier Φ for the metal vacuum contact. As a result, even at room temperature or lower, there maybe a sufficient number of electrons available at the contact to support space charge limited electron flow into the insulator. In Figure 3.3, tunneling type metal-insulator injecting contact is shown. E_t is a trap energy level. This contact, in thermal equilibrium, is a thin blocking contact. A large density, of neutral state, near the interface can be ionized, and this creates a thin depletion layer and a high field for the carrier's tunneling through the empty traps due to the field [12]. Space charge limited current injection into a insulator, via a tunnel-emission contact, has been studied theoretically by Adirovich [13].

The idea of space charge limited current was first discussed in 1940 by Mott and Gurney [15]. They made simple and approximate calculations to show that it should be possible to achieve reasonably large current by injection of mobile electrons into the conduction band of an insulator.

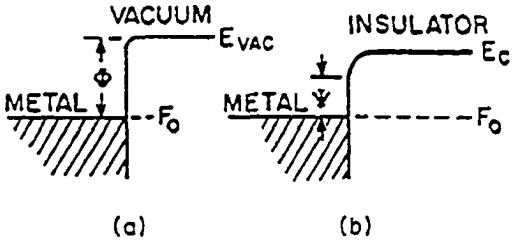


Figure 3.2 Schematic energy band diagrams for: (a) the contacts of a metal to the vacuum; (b) the contact of a metal to an insulator [14]

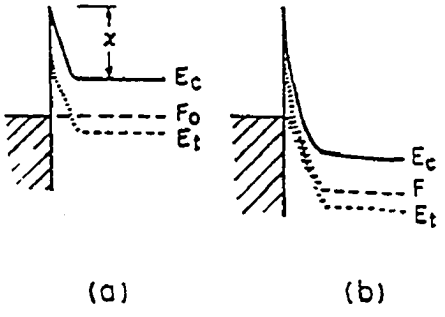


Figure 3.3 Schematic energy band diagrams for electron tunneling (field emission) metal-insulator contacts: (a) in thermal equilibrium; (b) under applied voltage, biased for injection [14]

When the injected carrier density rises to a value comparable to the impurity density, the space charge limited effect, due to repulsion of carriers, causes the current to vary less rapidly with the applied voltage. The space charge limited current for the trap-free case is proportional to the square of the applied voltage. At low voltage, current is carried by the thermally excited carrier hopping from one isolated state to the next. This mechanism yields an Ohmic characteristic exponentially dependent on temperature. A significant departure from Ohm's law will be observed only when the injected carrier concentration becomes comparable to the thermal concentration or, when the quasi-Fermi level, F, moves up into the forbidden gap from thermal equilibrium Fermi level, F_0, by approximately an amount kT. Let $n_{t,x}$ denote the total average change in occupancy of all electron traps due to this upward motion of the Fermi level. Then, the voltage V_x required to support the total trapped space charge $Q = en_{t,x}L$ per unit area (e is electron charge and L is the length), which is the onset voltage for space charge limited current flow, is $V_x \approx en_{t,x}L^2/\varepsilon$ where ε is dielectric constant. The contributions to $n_{t,x}$ are approximated: from, (1) traps lying above F_0 (shallow traps), the thermal concentrations electrons in such traps, (2) traps lying within kT of F_0, the total concentrations of such traps, and (3) traps lying below F_0 (deep traps), the thermal concentrations of vacancies in such traps. Any one of the three contributions can dominate $n_{t,x}$.

The potential value of space charge limited current, for exploitation in devices, has seldom been recognized. The existence of high carrier velocities, relative temperature insensitivity of current, low noise, and unnecessary defect free materials, inherently available under SCL conditions, suggests that SCL solid-state devices should be superior in several ways to conventional semiconductor junction devices. A direct quantitative comparison between diffusion-limited devices and space charge-limited devices has been discussed briefly by Wright [16] for the

semiconductor and dielectric diodes. Diffusion-limited solid state devices are particularly suitable for power applications, whereas SCL solid state devices are particularly for electronics applications.

3.1.3 Negative Capacitance, Equivalent Inductive Behavior

A negative capacitance effect, which can be an equivalent inductive behavior, above a certain forward bias, was simulated with a Schottky diode by M.. A. Green and J.Shewchun in 1973 [17]. It was also observed, in a $NiSi_2$-Si diode above 0.48 V. at 200 K, by X. Wu [7] in 1990. Figure 3.4 shows the negative capacitance under forward bias. Also, above a certain forward bias, inductive behaviors were simulated with a planar PIR (P stands for emitter so well doped with acceptors, I stands for intrinsic narrow base, and R stands for infinite recombination contact) diode by I. Ladany in 1960 [6] and for three layer diodes in 1961 [18], and 1963 [19]. A simple lumped component diode model by A. A. Barna [20] was shown to be an inductive impedance at high forward current.

Where does the negative capacitance come from? A negative capacitance indicates that the current variation in a device lags behind the voltage agitation. One possibility for this is that the alignment of the electron spin, or orbital magnetic momentum at the interface of metal/semiconductor makes the device act like an inductor under ac influence. However, this hypothesis was ruled out by an electron spin resonance measurement, where no appreciable enhancement of the negative capacitance signal was observed [7]. Another possibility, which was presented by the above authors, is the so-called bulk conductivity modulation. Specifically, it means that the bulk conductivity of the semiconductor is modulated by the minority carrier injection [17] which results in a phase-delayed reduction of resistance. However, X. Wu proposed a charge delocalization mechanism under the impact of hot electrons. This theory is established by the following arguments.

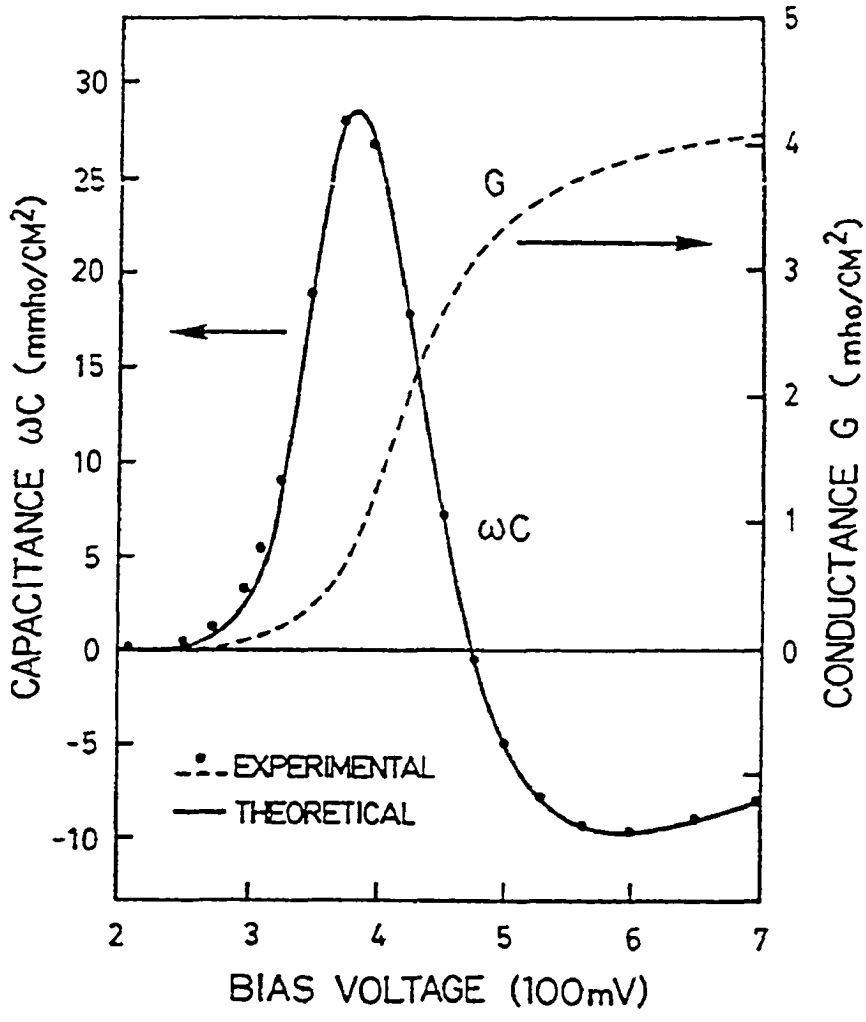


Figure 3.4 Susceptance and conductance as a function of bias measured at 200 K and 108 Hz from a $NiSi_2$-n-Si Schottky diode [7]

Electrons that surmount the Schottky barrier, under forward bias, do fill up the empty states at the interface, but because they possess excess energy, when they collide with the electrons trapped at the interface states, they could also knock electrons out of traps, provided that the binding energy of these traps is smaller than the Schottky barrier energy. This mechanism is similar to the impact ionization process [21] and electron multiplication in a superlattice [22]. But, at high temperatures, the disturbance of the hot electrons, to the local distribution, is relatively small. The empty states, created by electron impact, are quickly refilled by the electrons from the metal. In such a case, the occupancy below the Fermi level of metal is virtually unaffected by the ionization process; hence, no negative capacitance is observed. However, to date, the cause of negative capacitance is not clear even though conductivity modulation, by the minority carrier injection and charge delocalization at interface traps, has been proposed.

Previously, there had been considerable interest in possible ways to simulate inductors with semiconductor devices. A mechanism, which causes an inductive effect in the forward biased junction diode, may be conductivity modulation as mentioned above. If a diode contains one lightly doped region, this region, usually called the base, can experience considerable conductivity modulation due to the injection of minority carriers at the junction. The effect of conductivity modulation is too small in ordinary diodes to produce useful inductive reactance. The junction capacitance normally masks the inductive effect except at high bias levels.

3-2 Thermionic Field Emission Model with Laser Induced Thin P^+ Layer After Al Deposition

3.2.1 Introduction

In Schottky barriers, on highly doped semiconductors, the depletion region becomes so narrow that electrons can tunnel through the barrier near the top (see

Figure 3.5). This process is called thermionic field emission. In degenerate semiconductors, especially in semiconductors with small electron effective mass, such as GaAs, electrons can tunnel through the barrier near the Fermi level. The width of the depletion region becomes so narrow that direct tunneling from the semiconductor to metal takes place, and this phenomenon is called field emission. The current-voltage characteristics of a Schottky diode, in the case of thermionic field emission or field emission, was calculated by evaluating the product of the tunneling transmission coefficient and the number of electrons as a function of energy [23,24].

A new method, to obtain the effective barrier height of the metal-semiconductor with a thin highly doped surface layer (p+), is proposed. A thin, highly doped layer was induced by a KrF excimer laser with several pulses. During high temperature (350°C - 577°C) [25], the Silicon is dissolved in the Aluminum film. The Al takes up to Si to its solubility limit [26]. On fast cooling, this dissolved Si recrystallizes epitaxially in the Al-Si interface, but the recrystallized Si is heavily doped with Al and is therefore strongly p-type. This process is solid state epitaxy. Above the eutectic temperature (577°C), a thin highly doped layer is also formed by liquid phase epitaxy.

3.2.2 Model

A new model is proposed to obtain an effective reduced barrier height of a metal-semiconductor Schottky barrier diode, with a thin highly doped surface layer. Poisson's equation, Harrison's tunneling theory [5], and WKB approximation were used to calculate a tunneling transmission probability and tunneling current under thermionic field emission. An effective, reduced Schottky barrier is derived from the calculation of a minimum tunneling current and a position of maximum tunneling distance. The formation of a thin high doping layer by Excimer Laser,

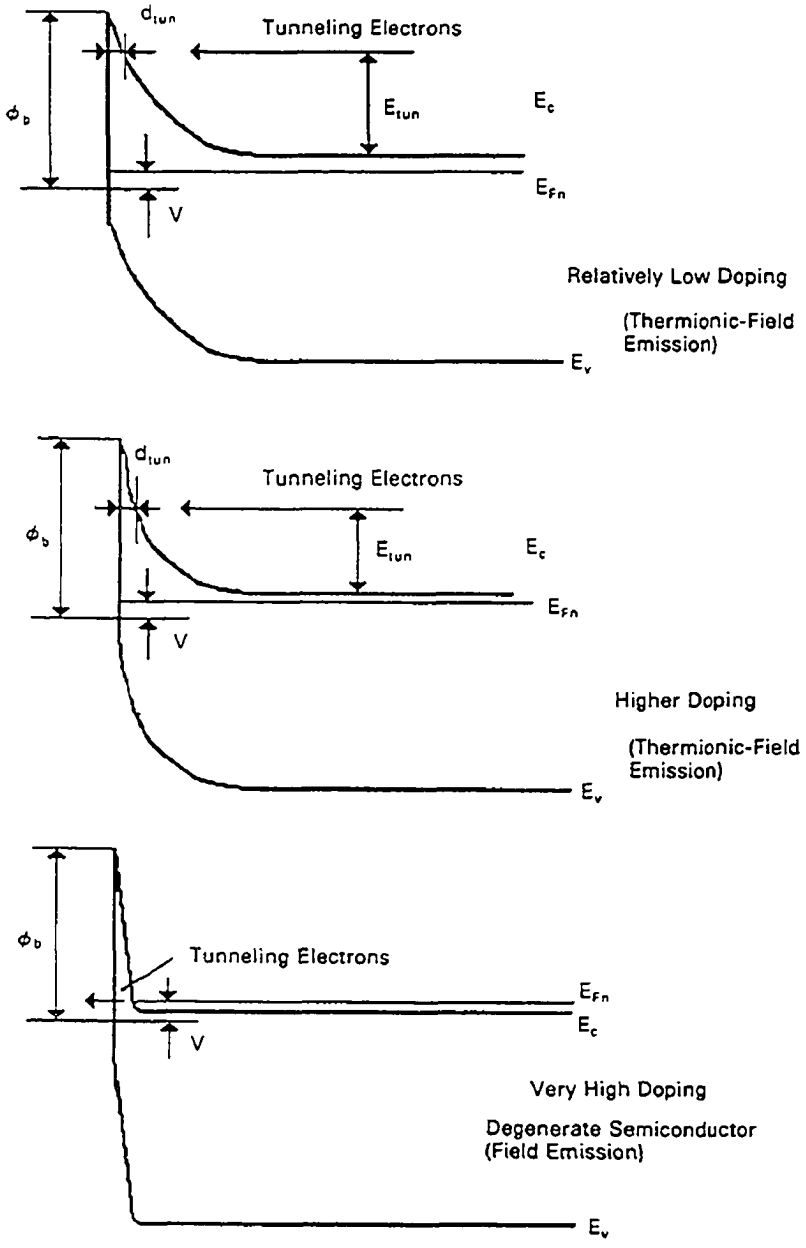


Figure 3.5 Thermionic field and field emission under forward bias. d_{tun} is the characteristic tunneling length. [27]

rather than conventional annealing [25] or ion implementation [28-31], results in the reduced barrier during transition from the Schottky barrier to the Ohmic contact. This model has some assumptions, and simplifications. The recrystallization is assumed to be uniform although it is almost non-uniform in a actual device. Image force lowering, interface states, and minority carrier injection is neglected.

The potential and electric field distribution at thermal equilibrium can be solved using the following Poisson's equations.

$$\frac{d^2V_1(x)}{dx^2} = \frac{q}{\varepsilon_s}(N_{a1} + N_{a0}) \qquad 0 \le x \le x_1 \qquad (3.1)$$

$$\frac{d^2V_2(x)}{dx^2} = \frac{q}{\varepsilon_s} N_{a0} \qquad x_1 \le x \le x_2 \qquad (3.2)$$

The energy band diagram of a diode under the forward bias is given in Figure 3.6. Using the continuity of electric field at $x = x_1$, and boundary conditions $\partial V_2(x)/\partial x|_{x\ x2} = 0$, $V_1(x)|_{x=x1} = V_{bi}$, $V_2(x)|_{x=x2} = 0$ at thermal equilibrium, the potential under forward bias is

$$V_1(x) = V_{bi} + V + \frac{q}{\varepsilon_s} N_{a1}\left(\frac{1}{2}x^2 - x_1 x\right) + \frac{q}{\varepsilon_s} N_{a0}\left(\frac{1}{2}x^2 - x_2 x\right) \qquad 0 \le x \le x_1 \qquad (3.3)$$

$$V_2(x) = \frac{q}{2\varepsilon_s} N_{a0}(x_2 - x)^2 \qquad 0 \le x \le x_2 \qquad (3.4)$$

where

$$x_2 = \left[\frac{2\varepsilon_s}{qN_{a0}}(V_{bi} + V - \frac{q}{2\varepsilon_s} N_{a1} x_1^2)\right]^{1/2}$$

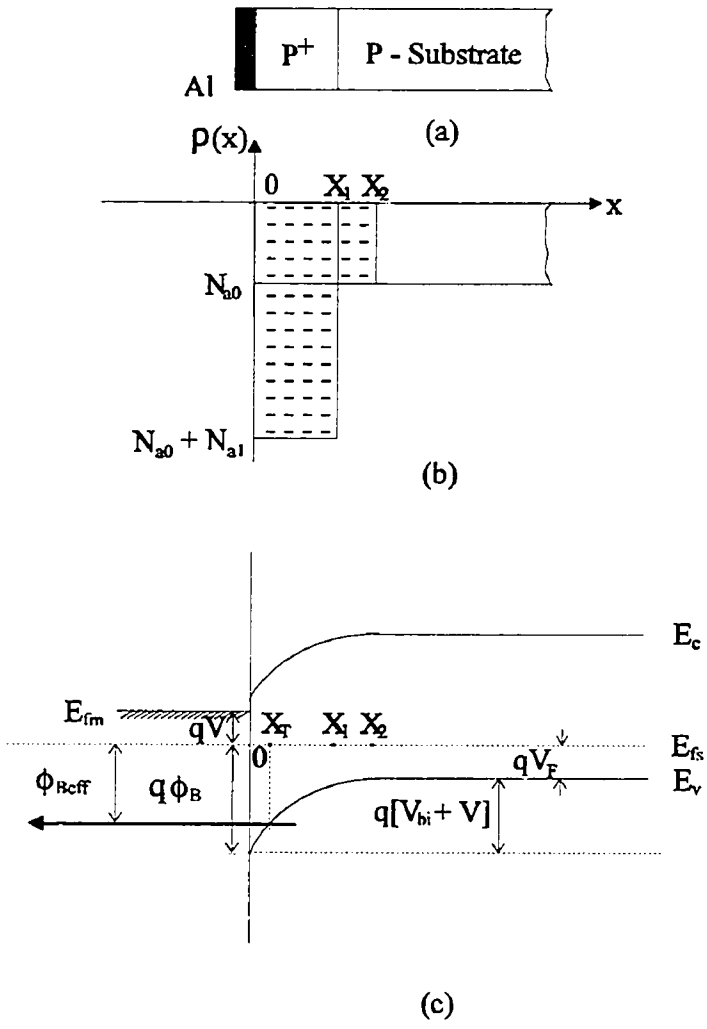


Figure 3.6 (a) Schematic diagram, (b) doping profile (c) energy band diagram under forward bias in metal / p^+ / p -Si

Using the result of Harrison, and assuming the tunneling position x_T is less than x_1, the one dimensional tunnel current is

$$J_x = \frac{4\pi q}{\hbar} \sum_{K_t} \int_0^\infty |M_{sm}|^2 \rho_s \rho_m (f_s - f_m)\, dE_x \tag{3.5}$$

where subscript s and m refer to the semiconductor and metal $|M_{sm}|^2$ is the matrix element for the transition from the semiconductor to the metal. ρ_s, and ρ_m are the density of states factors, and f_s and f_m are the Fermi function, K_t is the crystal momentum component transverse to the barrier. E_x is the contribution to the energy due to the component of momentum perpendicular to the barrier. Using WKB approximation for the transmission coefficient, U

$$|M_{sm}|^2_{s=x_T} = \frac{1}{\rho x_T \rho_m} \frac{1}{(2\pi)^2} \cdot U$$

$$= \frac{1}{\rho x_T \rho_m} \frac{1}{(2\pi)^2} \exp\left[-2 \int_{x_T}^{0} |K_{x_1}| dx\right] \tag{3.6}$$

$$U = \exp\left[\frac{\sqrt{4m}}{\hbar} \sqrt{\frac{q}{\varepsilon_s}} \left\{-\frac{N_{a1}x_1 + N_{a0}x_2}{N_{a1} + N_{a0}} x_T + \frac{1}{2} x_T^2\right\} \sqrt{N_{a1} + N_{a0}}\right] \tag{3.7}$$

From $\frac{dU}{dx_T} = 0$, we get the minimum of the transmission coefficient, U at

$$x_{T_{\max}} = \frac{N_{a1}x_1 + N_{a0}x_2}{N_{a1} + N_{a0}} \tag{3.8}$$

From equation (3.5), the method of Gray [32] is followed, which utilizes the transformation

$$\sum_{k_t} \rightarrow \frac{1}{(2\pi)^2}\int dk_y dk_z \rightarrow \frac{1}{2\pi}\int k_t dk_t \rightarrow \frac{1}{2\pi}\frac{m_t}{\hbar^2}\int dE_t \tag{3.9}$$

where k_t, E_t and m_t are the components of momentum, energy and effective mass for valance holes with momentum transverse to the barrier. Applying the transformation equation (3.9) to Harrison's equation (3.5), the expression for the one-dimensional tunnel current becomes

$$J_x = \frac{2m_t q}{\hbar^3}\int_0^\infty\int_0^\infty \left|M_{sm}\right|^2_{s=x_T} \rho_{x_T}\rho_m\left(f_{x_T} - f_m\right) dE_t dE_x \tag{3.10}$$

For forward bias, $f_m \approx 0$ and

$$f_s \approx \exp\left(-\left(E_x + E_t - E_{fs}\right)/KT\right) \tag{3.11}$$

E_{fs}, is the energy of the semiconductor Fermi level. The equation (3.10) becomes

$$J_x = A^* T^2 e^{\frac{1}{2}x_T^2 - x_1 x_T} e^{-q\phi_B/KT} e^{-qV/nKT} \tag{3.12}$$

where

$$A^* = \frac{mq}{2\pi^2\hbar^3}\cdot\exp\left[\frac{2\sqrt{m}}{\hbar}\cdot\sqrt{N_{a1}+N_{a0}}\right]$$

If N_{a1} is much greater than N_{a0}, then $x_T \approx x_1$, equation (3.12) becomes

$$J_x = A^* T^2 e^{\frac{1}{2}x_T^2} e^{-q\phi_B/KT} e^{-qV/nKT} \tag{3.13}$$

Reduction of effective barrier height is

$$\Delta\phi_B = (V_T + V_{bi} + V) - (V(x_1) + V_T)$$

$$= \frac{q}{\varepsilon_s}\left(\frac{1}{2}x_{T_{max}}^2 (N_{a1} - N_{a0}) + N_{a0}x_2 x_{T_{max}}\right) \tag{3.14}$$

using $x_{T\max} = \dfrac{N_{a1}x_1 + N_{a0}x_2}{N_{a1} + N_{a0}}$ and

$x_2 = \sqrt{\dfrac{2\varepsilon_s}{qN_{a0}}\left(V_{bi} - \dfrac{q}{2\varepsilon_s}N_{a0}x_1^2\right)}$ under quasi-equilibrium,

the barrier reduction is

$$\Delta\phi_B = \frac{q}{\varepsilon_s}\left\{\frac{1}{2}\left(\frac{N_{a1}x_1 + N_{a0}x_2}{N_{a1} + N_{a0}}\right)^2 (N_{a1} - N_{a0}) + N_{a0}\left(\frac{2\varepsilon_s}{qN_{a0}}\left(V_{bi} - \frac{q}{2\varepsilon_s}N_{a0}\varphi_1^2\right)\right)^{\frac{1}{2}}\left(\frac{N_{a1}x_1 + N_{a0}x_2}{N_{a1} + N_{a0}}\right)\right\} \tag{3.15}$$

And, ideality factor, n becomes

$$n = \left(1 + \frac{d\Delta\varphi_B}{dV}\right)^{-1}$$

$$\approx \left(1 + \frac{x_1}{x_2}\right)^{-1} \tag{3.16}$$

≈ 1, when $x_2 >> x_1$

Figure 3.7 ,and 3.8 show the barrier reductuction, $\Delta\phi_B$ of equation (3.15) , and effective barrier height (0.6 eV - $\Delta\phi_B$ eV) vs. thickness of p+ layer by computer simulation when $N_{a1} = 10^{19}/cm^3$, $N_{a0} = 10^{18}/cm^3$, $V_{bi} = 0.5$ eV, and $E_f - E_v = 0.1$

eV under quasi-equilibrium. The effective barrier height is zero at 4nm of p+ layer using simulation. Therefore, above 4nm of p+ layer, a complete ohmic contact would be formed. The current mechanism is changed to field emission from thermionic field emission.

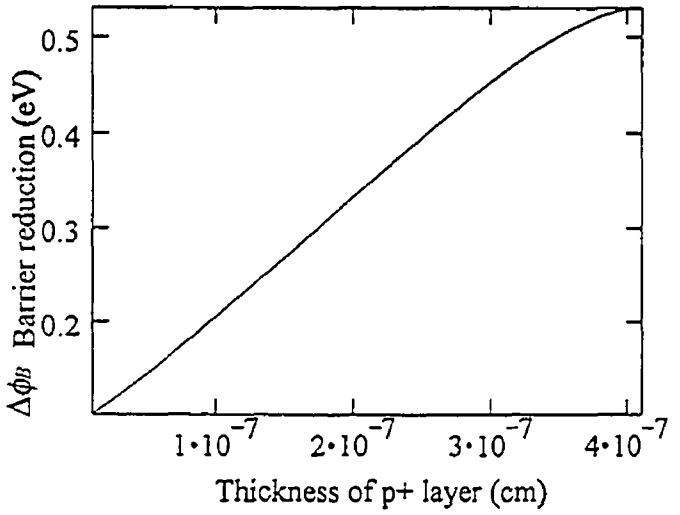


Figure 3.7 Computer simulation of barrier reduction , $\Delta\phi_B$ vs. thickness of thin p+ layer when $N_{a1} = 10^{19} / cm^3$, $N_{a0} = 10^{18} / cm^3$, and $V_{bi} = 0.5$ eV

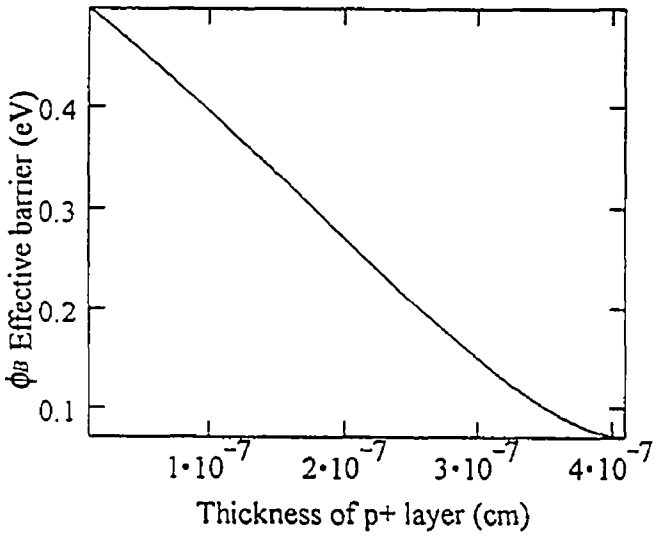


Figure 3.8 Computer simulation of effective barrier height vs. thickness of p+ layer when $N_{a1} = 10^{19} / cm^3$, $N_{a0} = 10^{18} / cm^3$, and $V_{bi} = 0.5$ eV

3.3 Derivation of Inductive Behavior of a Novel Heterojunction Diode

Figure 3.9 shows an a-SiC/Si diode with d.c bias V on the injecting contact. When sinusoidal a.c. voltage is applied, the a.c. current i, becomes

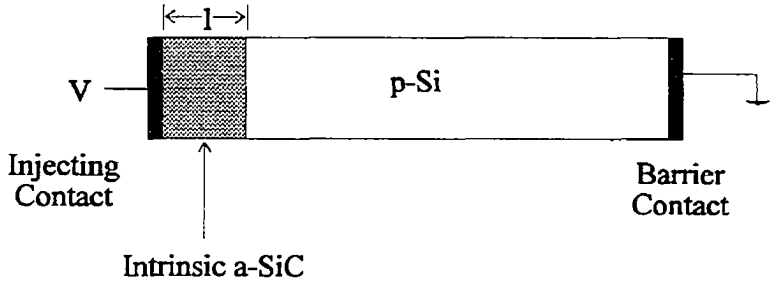


Figure 3.9 An a-SiC/Si heterojunction diode

$$i = \Delta n(\Delta p) q \mu_{n(p)} E \tag{3.17}$$

where

$\Delta n(\Delta p)$; the total number of injected electrons (holes) in the a-SiC.

$\mu_{n(p)}$; the mobility of electrons (holes)

E; constant electric field, assuming only drift current

Using Shockley Theory [33], with sinusoidal small a.c. voltage $ve^{i\omega t}$,

the injected electron density is

$$ne^{i\omega t} = \left(\frac{qn_i}{kT}\right) e^{\frac{qV}{kT}} ve^{i\omega t} \tag{3.18}$$

where

n_i; electron density in a-SiC

V; the d.c. bias voltage

and

$$\Delta n(i\omega t) = A \int_0^{v_d \tau_t} ne^{i\omega(t-t')} e^{-\frac{t'}{\tau_d}} v_d dt'$$

$$= Ane^{i\omega t}\frac{v_d\tau_d}{1+i\omega\tau_d}\left[1-\exp\left(\frac{-\tau_t}{\tau_d}-i\omega\tau_t\right)\right] \tag{3.19}$$

where

A; the cross section of a-SiC

τ_d; the dielectric relaxation time in a-SiC

v_d; the velocity of the injected electron in a-SiC

τ_t;transit time across the a-SiC

The decay of excess carrier in the relaxation semiconductor depends on the dielectric relaxation time, τ_d. Using eq.(3.17), (3.18), and (3.19),
with $\tau_t < \tau_d$ and $\omega\tau_t < 1$

$$Z = \frac{ve^{i\omega t}}{i} \approx \frac{\left(1+\omega^2\tau_d^2+i\omega\tau_t\right)}{Aq\mu_n El\left(\frac{qn}{kT}\right)e^{q|V|/kT}\left(1+\omega^2\tau_d^2\right)} \tag{3.20}$$

i) If $\omega\tau_d << 1$,

$$Z \approx \frac{1+i\omega\tau_t}{Aq\mu_n El\left(\frac{qn}{kT}\right)e^{q|V|/kT}} \tag{3.21}$$

therefore, inductance, L is

$$L = \frac{\tau_t}{Aq\mu_n El\left(\frac{qn}{kT}\right)e^{q|V|/kT}} \tag{3.22}$$

ii) If $\omega\tau_d >> 1$

$$Z = \frac{\omega^2\tau_d^2 + i\omega\tau_t}{Aq\mu_n El\left(\frac{qn}{kT}\right)e^{q|V|/kT}\omega^2\tau_d^2} \tag{3.23}$$

therefore, inductance L is

$$L = \frac{1}{\omega^2}\cdot\frac{\tau_t}{Aq\mu_n El\left(\frac{qn}{kT}\right)e^{q|V|/kT}\tau_d^2} \tag{3.24}$$

Also, we can define inductance by means of

$$V = L\frac{di}{dt} \tag{3.25}$$

which states that if the application of a voltage V cause the current to increase at the rate $\frac{di}{dt}$ the proportionality constant is called the inductance. The initial current I_i is given by $\frac{V}{R_i}$. After a transit time τ_t, the current has increased to $I_f = \frac{V}{R_f}$. Thus, $\frac{di}{dt}$ can be approximated by

$$\frac{di}{dt} \approx \frac{I_f - I_i}{\tau_t} = \frac{V}{\tau_t}\left(\frac{1}{R_f} - \frac{1}{R_i}\right) \tag{3.26}$$

With light doping, $\frac{1}{R_i}$ is negligible compared to $\frac{1}{R_f}$, we have

$$L \approx \tau_t R_f \tag{3.27}$$

R_f is expected to have the form $Cf(v)$, where C is constant then

$$L = \tau_t C f(v) \tag{3.28}$$

This form corresponds to equation (3.23, or 3.25). Therefore, it is reasonable to suppose that the inductive behavior is due to the conductivity modulation caused by the carrier injection through the high resistivity relaxation material.

3.4 Circuit Model of a Novel Heterojunction Diode

3.4.1 Injecting Contact

Figure 3.10 shows the device structure and the energy band diagram, in equilibrium, of a novel heterojunction diode. Al was deposited for both sides of the contacts. One Al contact on the relaxation semiconductors (laser induced disordered Si and non-hydrogenated a-SiC) can be an injecting contact.

At low voltage, current is carried by thermally excited carriers hopping from one isolated state to the next. This occurrence results in an Ohmic characteristic. Above a certain threshold voltage, the space charge limited current is the result of a carrier injected into relaxation semiconductors, where no compensating charge is present. Hopping in the localized (band tail) states, and hopping in deep defect states (such as dangling-bond states), can be treated as carriers moving via phonon-assisted tunneling events.

Figure 3.11 shows a carrier's hopping mechanism through an Al injecting contact. When the depletion region of thin film is very small, due to numerous defective states, the carrier can be tunneled by field emission or direct tunneling. An direct tunnel process can occur by the hopping process *abd* or *acd* or *abcd*, as shown in Figure 3.11(a). Such processes modify the transparency of the barrier quite markedly from that condition which corresponds to a direct transition. Also, they will normally be associated with the emission or absorption of a phonon

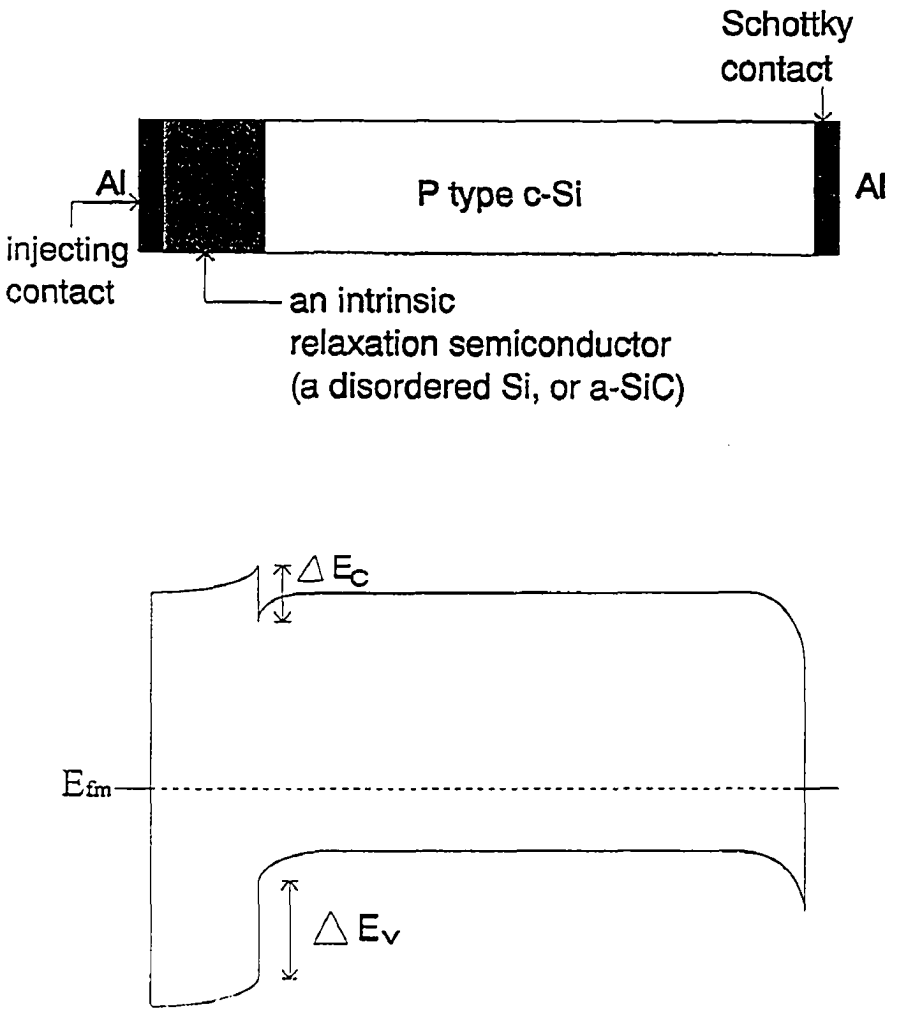


Figure 3.10 A device structure and energy band diagram under equilibrium in a novel heterojunction diode

(phonon assisted tunneling). A second process that can take place is that of indirect tunneling into a trap, followed by a thermal leap over the barrier, as indicated by the path *ace* in Figure 3.11(b).

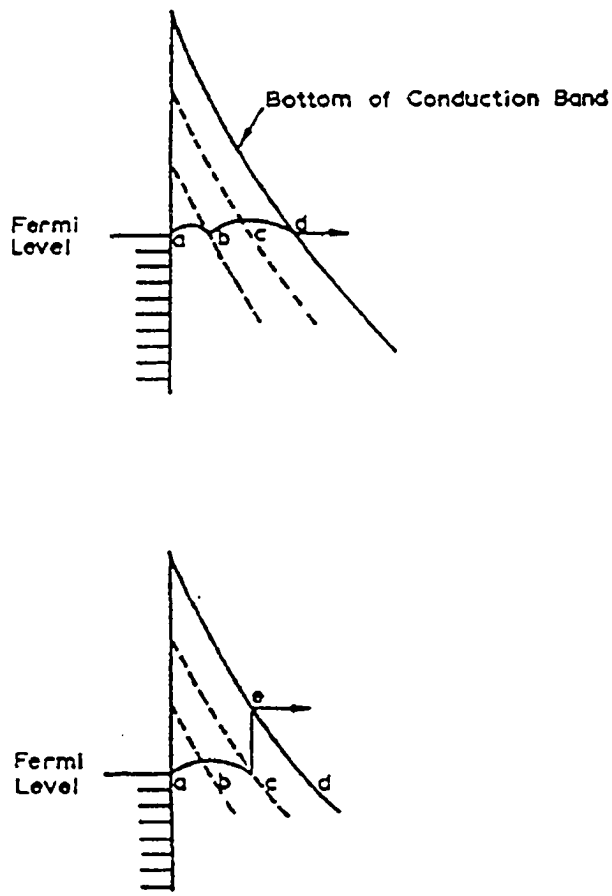


Figure 3.11 Energy diagrams illustrating (a) the direct tunnel process *abd* through the interface barrier; and (b) the combined indirect tunneling and thermal activation process *ace* through the barrier [34]

This processing will have a thermal activation energy that reflects the depth of the trap or donor, that is, $I = I_T \exp\left(-\frac{\varphi}{kT}\right)$, where I_T is the tunneling component of current and φ represents the donor or trap depth-depending on the center from which thermal activation takes place.

For an excimer laser induced disordered Si, Al was deposited after laser irradiation on the Si surface. A good injecting contact can be made because of the high surface recombination velocity [35] due to the surface roughness. Also, carrier tunneling, via hopping mechanism in the disorder layer, can be realized..

3.4.2 Model

Single-crystalline heterojunctions have been extensively studied [36-38] from the view point of understanding the fundamental device physics, as well as their applications to many devices. Some of these are, wide band-gap emitters, majority carrier rectifiers, high-speed wide bandpass photodetectors, beam-of-light transistors, indirect gap injection lasers, and solar cells. Amorphous heterojunctions might also be used for some of these application. However, the physics of amorphous heterojunctions is clearly far from being understood; even the amorphous homojunctions are not yet completely understood. The study of amorphous-crystalline heterojunctions can thus be a first step towards understanding amorphous-amorphous junctions. Anderson [36], Rediker et al. [37], Riben et al. [38], and other groups have reported the electrical properties of heterjunctions of crystalline materials. Anderson initially proposed an energy band diagram which assumed no interface states and an extremely abrupt change from one material to the other. Rediker et al., and Ribon et al. reported the experimental evidences for supporting the abrupt heterojunction model (Anderson's model) through their C-V measurements. With regard to the current transport mechanism

of heterojunctions, Anderson [36] puts the basis of his calculation on a Shockley diffusion model [39] and a Schottky emission model [40], respectively, while Riben et al., and Rediker et al. have independently published tunneling models to explain their own data.

Conversely, there are very few reports, concerning amorphous-crystalline heterjunctions, after the first report of Grigorovici on a-Ge/c-Ge junction [41]. According to Stourac [42], for the case of chalcogenide material, the junction is approximately the abrupt heterojunction, and the current transport mechanism is based on the space-charge-limited currents in the amorphous material.

Figure 3.12 shows the energy band diagram, in both forward bias and reverse bias, of a novel heterojunction diode. The hole current is injected with positive V at the injecting contact. Inductive behavior is developed due to the conductivity modulation in the disordered Si region or amorphous SiC. The inductance is dominant for the large series depletion capacitance near the p-Si/Al interface. The current mechanism, near the p-Si/Al interface, becomes thermionic field emission and finally, field emission even with the high barrier (0.75 eV). The hole current in the opposite direction is almost zero because of the high energy step of the valence band in the heterojunction. The band discontinuity, which is one of the most important parameters, is not well understood. Matsura et al. [43] demonstrated the conduction-band discontinuity (ΔE_c) measured from the capacitance-voltage (C-V) curves of glow discharge (GD) a-Si:H/c-Si junctions to 0.2 ± 0.07 eV, and thus, that the band discontinuity was mainly at the valence-band side. In contrast, Cuniot and Manfaing [44] showed $\Delta E_c = 0.55 \pm 0.7$ eV and the valence-band discontinuity $\Delta E_v \leq 0.15$ eV from the internal photoemission of sputtered a-Si:H/c-Si, thus insisting that the band discontinuity existed mainly at the conduction band side. Here, we assume that the valence band discontinuity is mainly at the valence-band side.

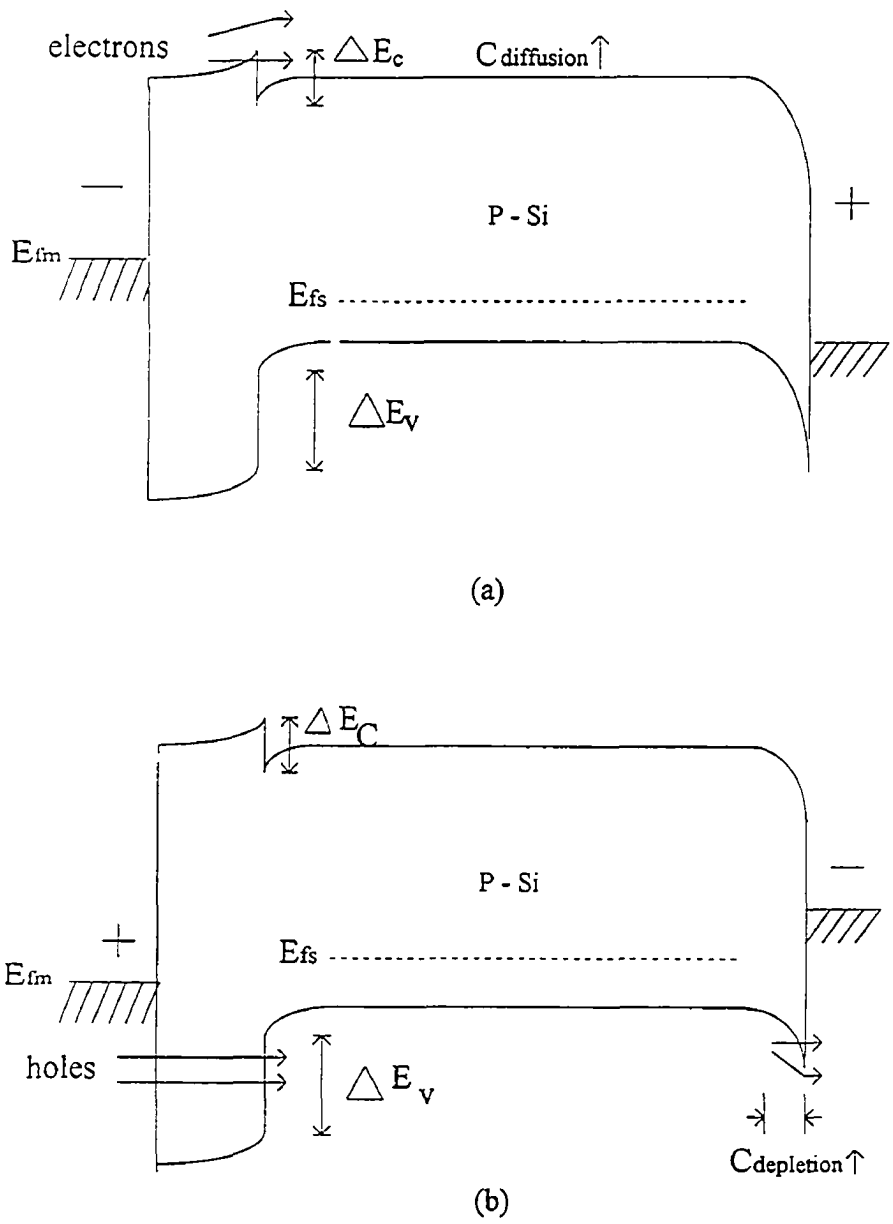


Figure 3.12 Energy band diagram in forward bias (a) and reverse bias (b) in a novel heterojunction diode

With negative V at the injecting contact, only electron current is injected. Again, inductance, which is developed, is dominant for the large diffusion capacitance in the bulk of p-Si. The electron current has no barrier near the reverse biased p-Si/Al interface. Therefore, a current mechanism, in both biases, is an ohmic behavior like a resistor. Sometimes, space charge limited current will appear, in both or either bias above a certain threshold voltage.

A current, through the heterojunction, might tunnel through the thin spike-shaped barrier. The simplest tunneling mechanism consists of the tunneling of carriers through the spike-shaped barrier in the conduction band (Figure 3.13). According to Riben et al. [38], predominant tunnel flux takes place at an energy close to the peak of the barrier within an energy difference of approximately 0.1 eV for the crystalline heterojunction, and this is indicated by path "A" in the figure. In the present heterojunction, however, the tunneling process, at an energy range far below the barrier peak, indicated by path "B" in the figure, is quite possible because the localized states are quasi-continuously distributed within the gap of the disordered Si or a-SiC spatially, as well as energetically.

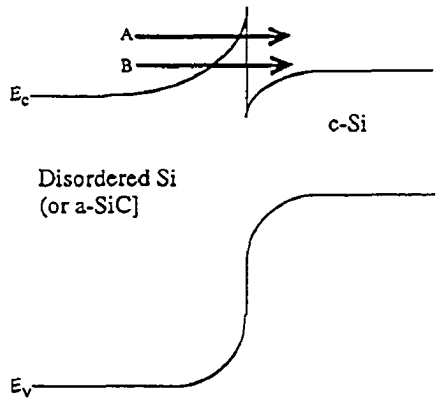


Figure 3.13 Tunneling for heterojunction of a-SiC /Si or disordered Si/Si

Figure 3.14(b) shows a simplified small signal diode model. A small parallel geometric capacitance is neglected. Reactance $X(V)$ is

$$X(V)=\frac{\omega\left(L(V)+\omega^2 L(V)R^2C^2(V)-R^2C(V)\right)}{1+\omega^2R^2C^2(V)} \tag{3.29}$$

Where

R; Differential resistance of a heterojunction diode

$L(V)$; inductance developed in a disordered Si or a-SiC layer,

$C(V)$; diffusion capacitance under electron injection in bulk Si, or depletion capacitance near Si-Al interface under hole injection

Reactance $X(V)$ is inductive if

$2\omega L(V) \geq R$ or,

$2\omega L(V) < R$ and

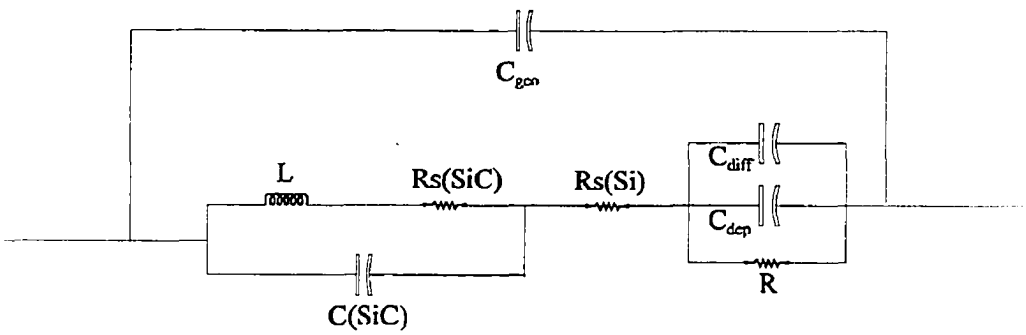
a) $$C(V) < \frac{R^2-\sqrt{R^4-4\omega^2L(V)^2R^2}}{2\omega^2L(V)R^2} \approx 0$$

b) $$C(V) > \frac{R^2+\sqrt{R^4-4\omega^2L(V)^2R^2}}{2\omega^2L(V)R^2}$$

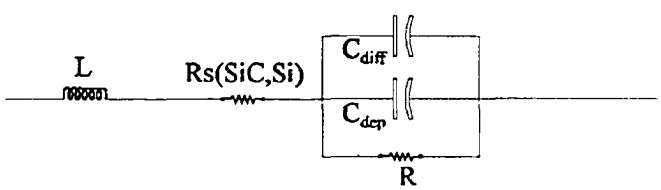
$$\approx \frac{1-\omega^2L(V)^2}{\omega^2L(V)}$$

The, measured capacitance, C_{Test} follows as the relation

$$C_{Test}=-\frac{\left(1+\omega^2R^2C(V)^2\right)}{\omega^2\left(L(V)(1+\omega^2R^2C(V)^2)-R^2C(V)\right)} \approx -\frac{1}{\omega^2L(V)} \tag{3.30}$$



(a)



(b)

Figure 3.14 (a) A small signal circuit model for a heterojunction diode of a-SiC (or disordered Si)/c-Si, (b) A simplified circuit model

3.5 The Effect of Carrier Screening of Impurity in the Thin Relaxation Layer

When the electron density is much higher than the donor impurity density, each impurity can then be electrically screened by many electrons and this weakens the donor impurity potential to bind or trap an electron. When the electron concentration is sufficiently high, there is no bound state solution of the Schrödinger equation. This gives an estimate of the critical electron concentration at which the impurity activation energy drops to zero.

This carrier screening is known as Debye-Huckle screening [45] in dilute electrolytes and semiconductors with low electron concentration. It is known as the Fermi-Thomas screening in degenerate semiconductors and metals. The 1/r Coulomb impurity potential is screened and reduced by an exponential function, $\exp(-k_s r)$ where $k_s^{-1} = r_s$ is known as the screening length. The screening length is the distance at which the potential drops by 1/e. The screened Coulomb potential energy of an electron is then

$$V(r) = - \frac{q^2}{[4\pi\varepsilon_s r]} \exp\left(-r/r_s\right) \tag{3.31}$$

Note there are two screening sources: (i) the valence electrons denoted by the dielectric constant, ε_s, known as dielectric screening and (ii) the carriers or conduction band electrons and valence band holes, denoted by r_s. Figure 3.15 illustrates carrier screening. Notice the tremendous reduction of the range of the Coulomb potential from carrier screening. The screened potential has the appearance of a square well.

In the case of carrier screening of impurity, the variation of the lifetime with the injection level δp (or δn) can be examined. The lifetime τ is

$$\tau = \tau_0 \left[\frac{1+\dfrac{(\tau_{po}+\tau_{no})\delta p}{\tau_{po}(n_0+n_1)+\tau_{no}(p_0+p_1)}}{1+\dfrac{\delta p}{n_0+p_0}} \right] \tag{3.32}$$

where $\tau_0 = \dfrac{\tau_{po}(n_0+n_1)+\tau_{no}(p_0+p_1)}{n_0+p_0}$ and

$$\begin{aligned} n_0 &= N_c e^{-(E_c-E_f)/KT} \\ p_0 &= N_v e^{-(E_f-E_v)/KT} \\ n_1 &= N_c e^{-(E_c-E_t)/KT} \\ p_1 &= N_v e^{-(E_t-E_v)/KT} \end{aligned} \tag{3.33}$$

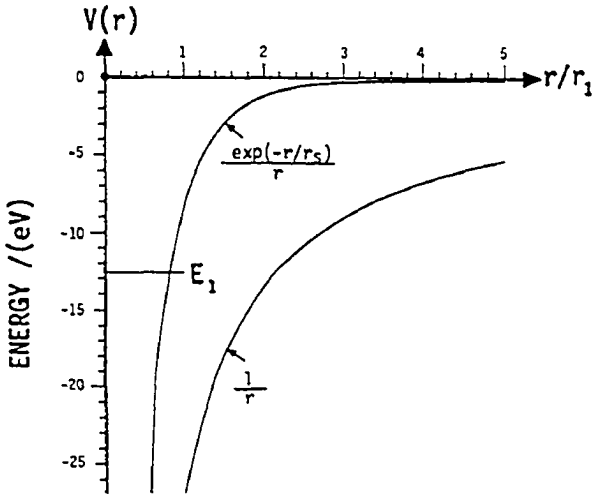


Figure 3.15 Effect of carrier screening on the electron potential energy in the Coulomb electrostatic force field of a positive point charge. The screening length is equal to the critical length, $r_s = a_1/1.19$, at which the Bohr bound states disappear. [45]

where N_c , N_v is the effective densities of states at the conduction and valence band edges. n_0 , p_0 are equilibrium electron and hole concentration. δn , δp are excess electron and hole concentration. n_1 is the electron concentration which would be present in the conduction band if the Fermi level were to coincide with the trap E_t. P_1 is the hole concentration which would be found in the valence band if the Fermi level were at the energy of the trapping level. τ_{p0} represents the lifetime of excess holes in highly extrinsic n-type material and τ_{n0} represents the lifetime of excess electrons in highly extrinsic p-type material. When holes or electrons are injected into an intrinsic relaxation semiconductor, the holes or electrons are released from traps due to the carrier screening. Excess carrier injection, by carrier release in forward bias from the trap, will change the carrier lifetime. The variation of the lifetime with both the excess hole injection (δp), and hole concentration in the valence band (P_1) can be simulated. If δp is sufficiently small, the lifetime will have τ_o independent of δp. For larger values of δp, the lifetime will depend on δp, and may decrease or increase from τ_o to τ_∞ ($= \tau_{po} + \tau_{no}$) with increasing values of δp. But, in the intrinsic relaxation semiconductor, the lifetime will decrease because of $P_1 > P_0$, and $n_1 > n_0$. Figure 3.16 shows, through computer simulation of equation (3.32), that the decrease of the lifetime with an increase of both injection level δp, and holes concentration P_1, in the valence band due to the holes release from traps. With P_0, $n_o = 10^4 / cm^3$ and τ_{po}, $\tau_{no} = 10^{-10}\ sec$, the lifetime was decreased in the ranges of $10^8 / cm^3 < P_1 < 10^{11} / cm^3$, and $10^4 / cm^3 < \delta p < 10^7 cm^3$. Therefore, in a low doping, high resistivity relaxation semiconductor, lifetime can be much shorter under high excess carrier injection due to the carrier screening of impurity. This can lead to a more pronounced relaxation.

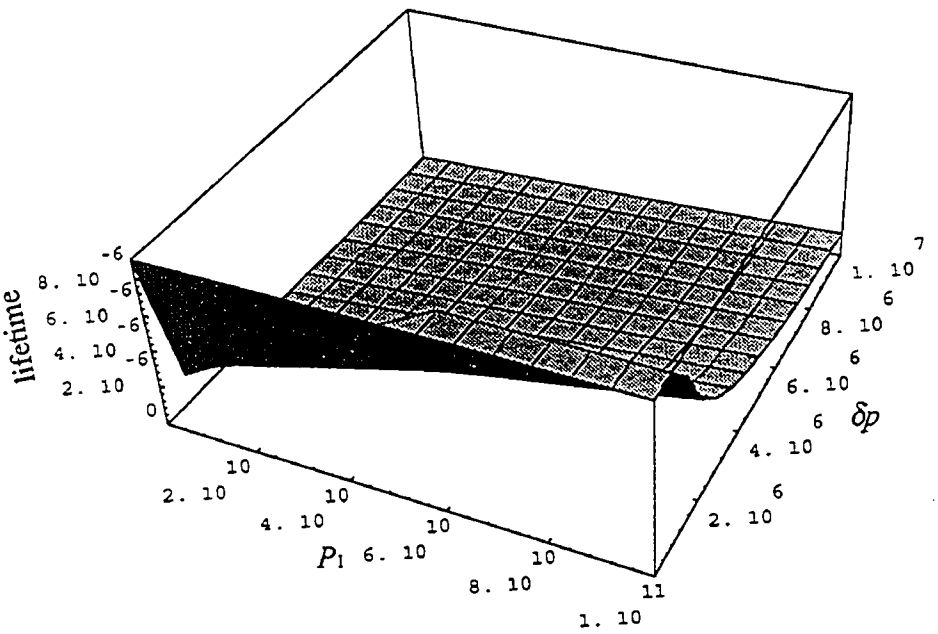


Figure 3.16 Variation of the lifetime with excess injection, δp and carrier concentration in the valence band, P_1, by computer simulation

CHAPTER 4

EXPERIMENTAL RESULTS AND DISCUSSION

4.1 I-V and Structural Characteristics

4.1.1 Ohmic Behavior with Excimer Laser Irradiation on Al Contacts

The formation of Ohmic contacts on semiconductor surfaces is essential to the operation of most semiconductor devices. In general, for a semiconductor with a large band gap, such contacts are produced by alloying or sintering suitable metals on its surface. This produces a degenerate layer on the surface where contact is made. The degenerate layer makes the depletion layer, on the semiconductor surface, thin enough to allow sufficient tunneling [46,47]. The contact region then appears 'Ohmic'. A pulsed KrF excimer laser can be used as a heat source to form a degenerate layer on p-Si with an Al contact. The development of excimer lasers, which generate powerful ultraviolet, have enhanced their potential use in technological application, e.g., as a lithography, in ultra large-scale integration technology. Laser-recrystallized silicon thin films are of technological interest for fabricating high performance thin film-transistors, silicon-on-insulator devices, and 3-D integration. Ohmic contacts on III-V compound semiconductors using a pulsed ruby laser (694 nm), and YAG laser (1060 nm) were successfully made in 1973 [48]. And, Ohmic contact was formed on InP using a pulsed ArF laser (193nm) in 1980 [49].

In my experiment, after chemical cleaning of the wafer, pure Al (99.9999%) was deposited on p-type (100) Si (doping of $10^{18}/cm^3$, thickness of 60 μm) by a 'VARIAN 31-25' magnetron sputtering system. Al thickness, of deposited films, are approximately 150 nm and 700 nm. The diameters, of the Al dot contacts, were between 0.5mm and 1.5mm. A pulsed KrF excimer laser (248nm) was irradiated

on both sides of the Al dot contacts with excitation voltages of 20-22 kv, and a pulse period of 1 sec. I-V characteristics were measured by a 'KEITHLEY 236' ,and a HP-4145B Analyzer at room temperature. During the localized heat treatment, by the pulsed excimer laser irradiation, p-Si is dissolved in the Al up to its solubility limit. A metallurgical reaction, between Al and p-Si, leads to the formation of a thin p^+ layer near the interface, and this produces an Ohmic contact. However, when the laser intensity was sufficient and well focused, the Al surface evaporated. To avoid the Al evaporation, both laser intensity and focus were adjusted. Figure 4.1 shows the cross section of Al/c-Si after laser irradiation on the Al contact by SEM (1000X). The roughness of the Al surface, due to the laser irradiation, is shown. Figure 4.2 shows the damage in the boundary of the Al contact taken by SEM. In Figure 4.3, Al evaporation, inside the Al contact, due to the very strong power of the well-focused laser pulses (excitation voltage 25kv) is shown.

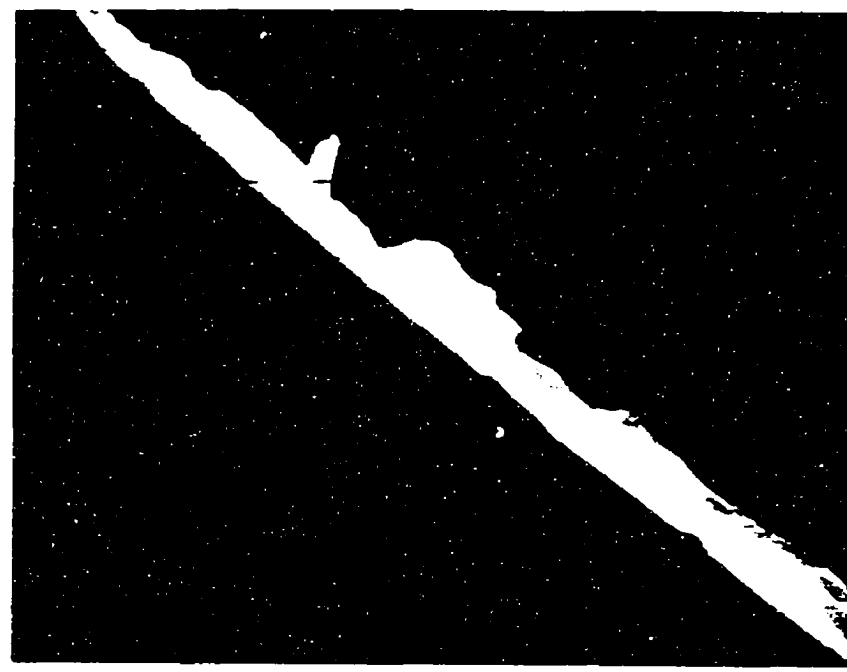


Figure 4.1 SEM (1000X) cross section of Al/c-Si after laser irradiation (excitation voltage of 22kv, period of 1sec)

Figure 4.2 SEM Al contact after laser irradiation
(excitation voltage of 24kv, period of 1sec)

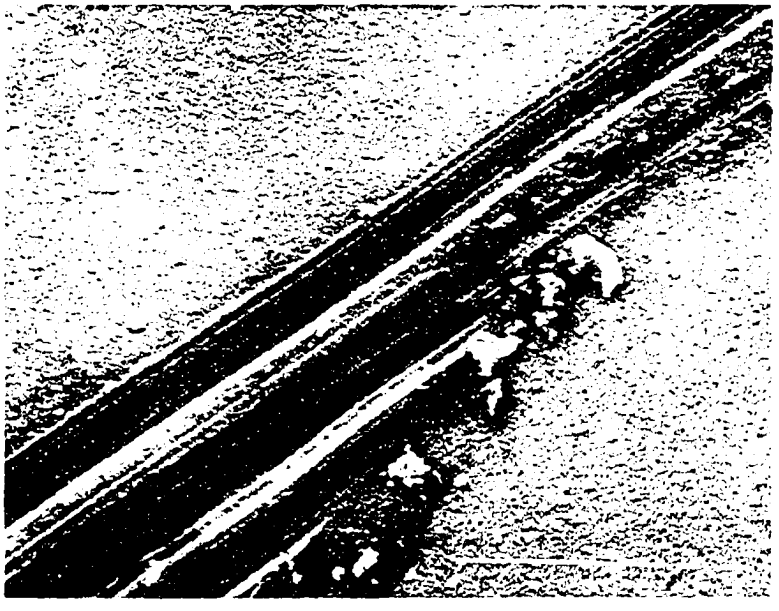


Figure 4.3 SEM (2000X) Al evaporation inside the Al contact after strong laser irradiation (excitation voltage of 25kv, period 0.5 sec)

Figure 4.4 shows the Al surface ($1\mu m^2$) before laser irradiation through the use of AFM (Atomic Force Microscope). The grain boundary, of polycrystalline Al, due to sputtering is shown. The maximum distance between the dark and the bright side in the picture is 50 nm. After uniform laser irradiation (excitation voltage of 20.3kv) on the Al contact surface, grain boundary disappeared as shown in Figure 4.5. The maximum distance between the dark and the bright side is 10 nm. Formation of crystalline Al from polycrystalline Al might be possible with excimer laser irradiation.

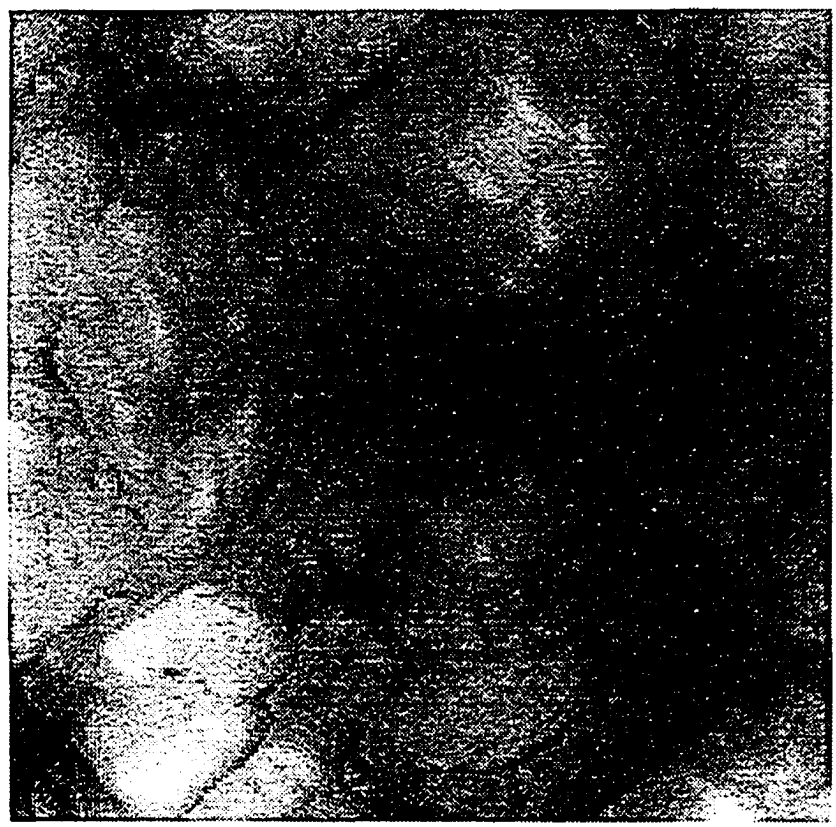


Figure 4.4 AFM Al contact surface before laser irradiation

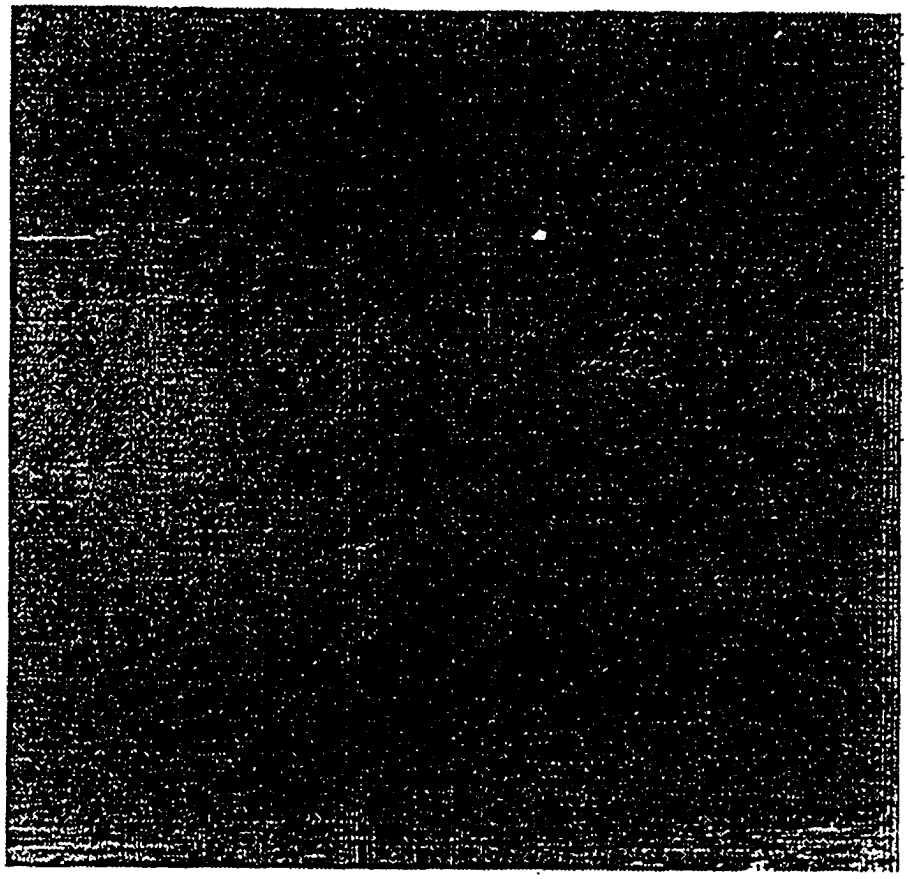


Figure 4.5 AFM Al contact surface after laser irradiation
(exciting voltage of 20.3kv, period of 1 sec)

Figure 4.6 shows ohmic behavior after several laser irradiations (excitation voltage of 20.3 kv) on both sides of the Al contacts. The contact resistance is 1000Ω. Increasing the number of laser pulses, by a factor of 10, caused a decrease in contact resistance of up to 35Ω. Figure 4.7(a), shows ohmic characteristic with a 50Ω contact resistance, and Figure 4.7(b) shows ohmic characteristic with a 35Ω contact resistance.

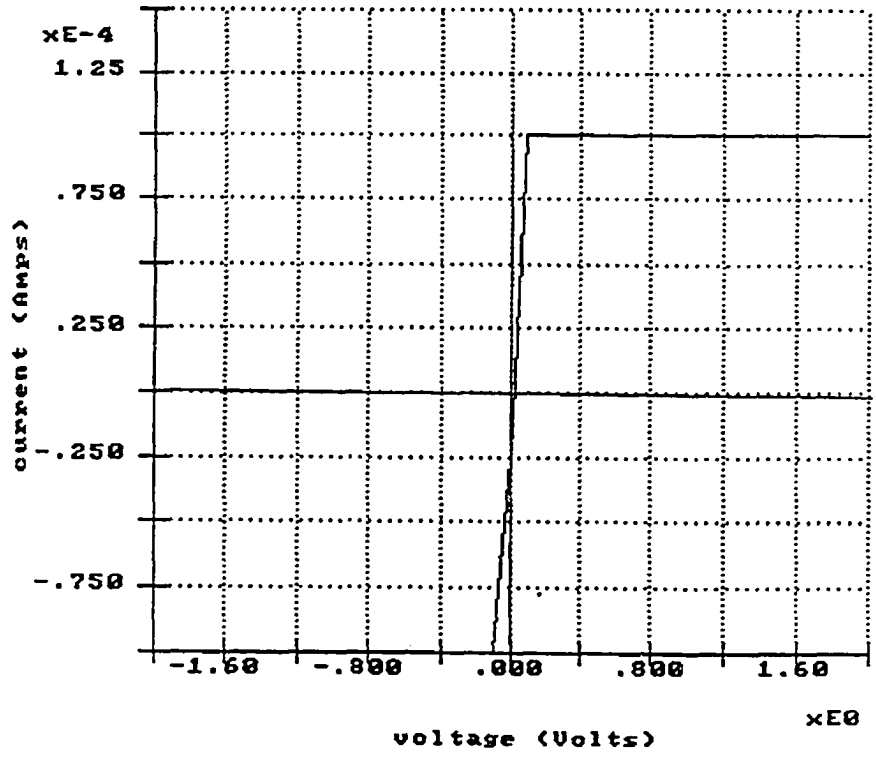
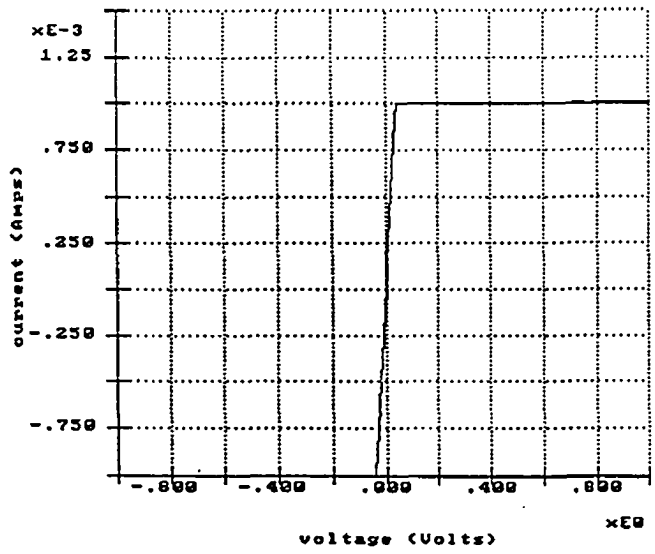
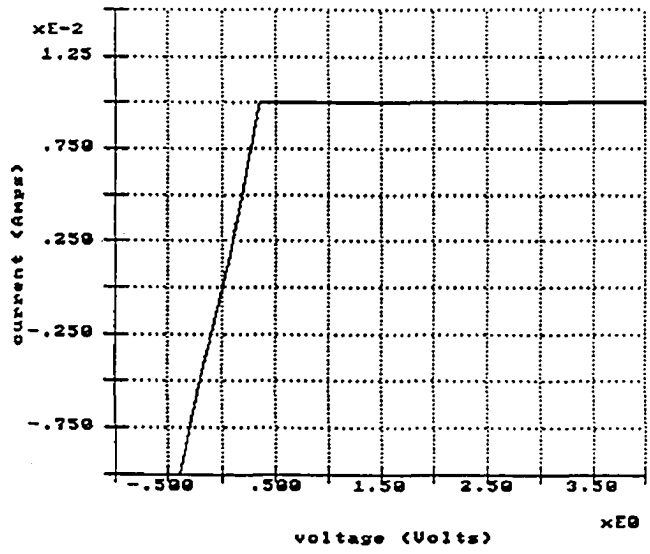


Figure 4.6 Ohmic behavior after several pulsed laser irradiation (excitation voltage of 20.3 kv) on both Al contacts



(a)



(b)

Figure 4.7 Ohmic behavior after 10 pulsed laser irradiation (excitation voltage of 20.3kv) on both Al contacts. Contact resistance is (a) 50Ω, (b) 35Ω

Figure 4.8 and Figure 4.9 show Auger analysis before and after laser irradiation on the Al contact. Depth-concentration profiles of Al and Si near the Al/Si interface is shown. The Al thickness of the deposited film is about 700nm, and the diameter of the Al dot contact was about 1mm. For in-depth Auger analysis, a KRATOS X-SAM 800 system was used. After laser irradiation, the Al was diffused up to approximately 200nm from the Si surface. A thin high doping layer of 200nm was formed near the Al/Si interface.

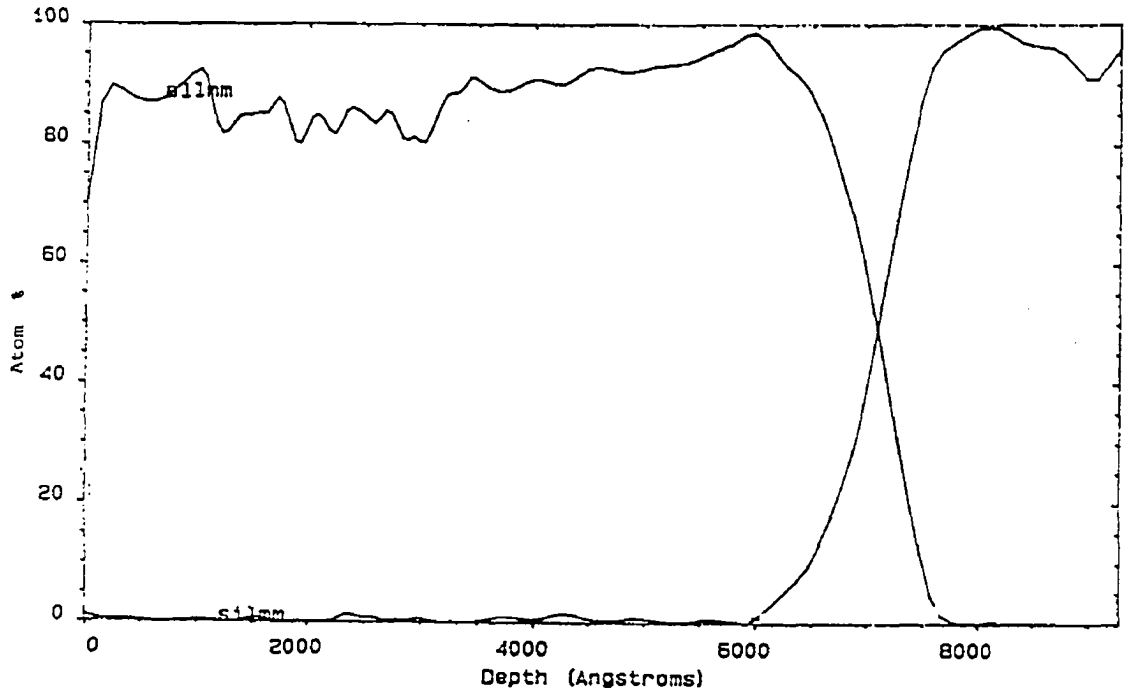


Figure 4.8 AES depth in profiles near the Al/Si interface, before laser irradiation (excitation voltage of 20.3kv) on an Al contact

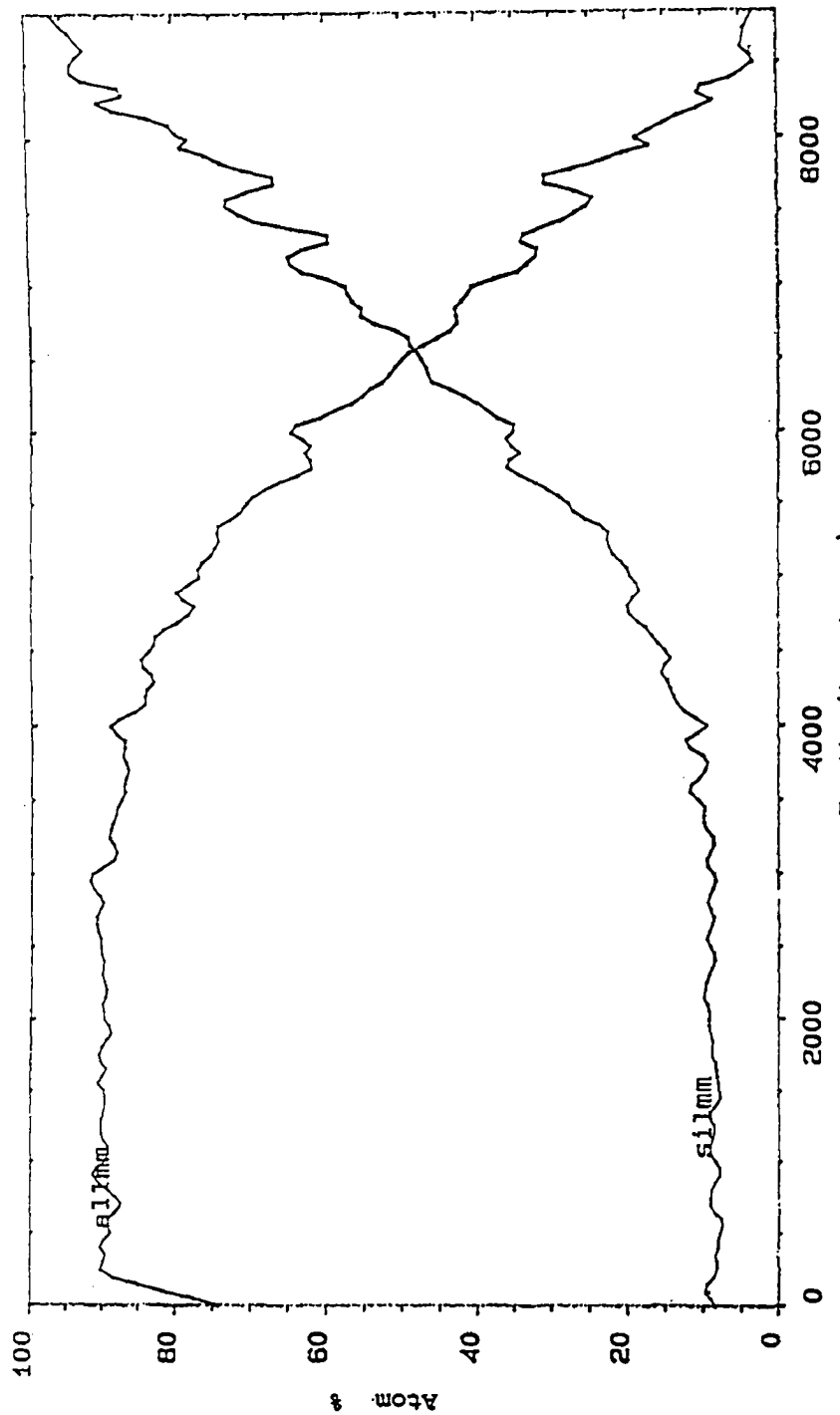


Figure 4.9 AES depth in profiles near the Al/Si interface after Al irradiation (excitation voltage of 20.3kv) on an Al contact

4.1.2 Space Charge Limited Current, with Excimer Laser Irradiation on c-Si Surface, before Al contacts deposition

The C-V doping profile is shown in Figure 4.10 after strong laser irradiation (excitation voltage of 24 kv, period of 1 sec) on an Al contact. A high resistivity layer of about 20nm was formed underneath a high doping P^+ layer (8 nm). It is probably a result of the formation of a high density of point defects and dislocation, which are due to the damage incurred during the rapid freeze portion of the alloying process. Figure 4.11 shows a schematic drawing of the high resistivity damaged layer after the alloying of GaAs with Ag/In/Ge contacts at 630 °C for 30 seconds [50]. Strain producing thermal gradients encountered in the alloying process can be large.

To avoid an Al spike and a non-uniform high resistivity layer due to the non-uniform Al thickness, the excimer laser was used to irradiate the c-Si surface before Al contact deposition. This Si surface is rough and abraded. Due to high surface recombination, an Ohmic contact can be achieved with this rough surface. And, a disordered, high resistivity Si layer can be made due to the damage from the laser irradiation. Dopant impurity is activated only in the substitutional site (i.e., at regular lattice site). Through the use of the laser irradiation, the dopant impurity can be moved from a substitutional site to a interstitial site (i.e., between regular lattice site). This results in a high resistivity, disordered layer. A diode structure, which is made using this technique, is similar to the previous diode which has a high resistivity layer beneath a Ohmic contact due to the thin high doping layer.

Figure 4.12(a) - 4.12(d) show AFM pictures of the disordered Si-surface after excimer laser irradiation (excitation voltage of 24kv, period of 0.1 sec) on the c-Si before Al deposition.

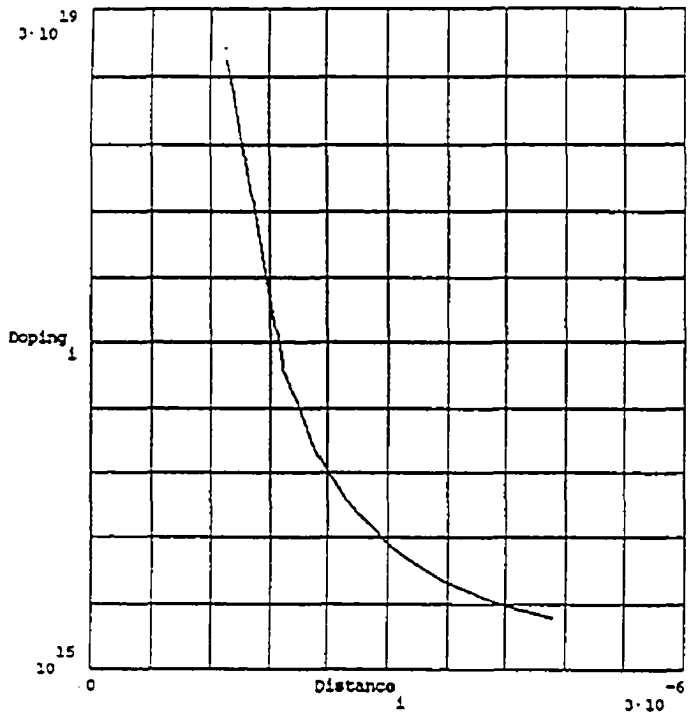


Figure 4.10 C-V doping profile after strong laser irradiation (exciting voltages of 24kv, period of 1sec) on Al contacts

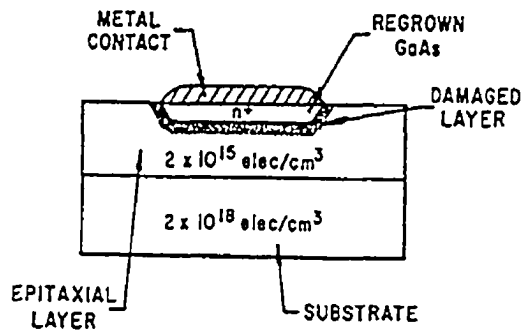
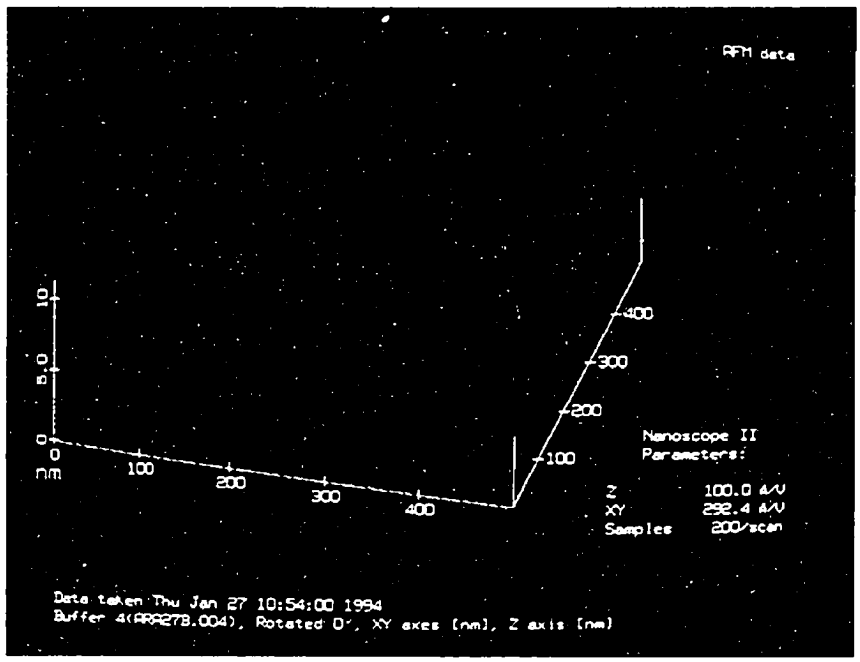
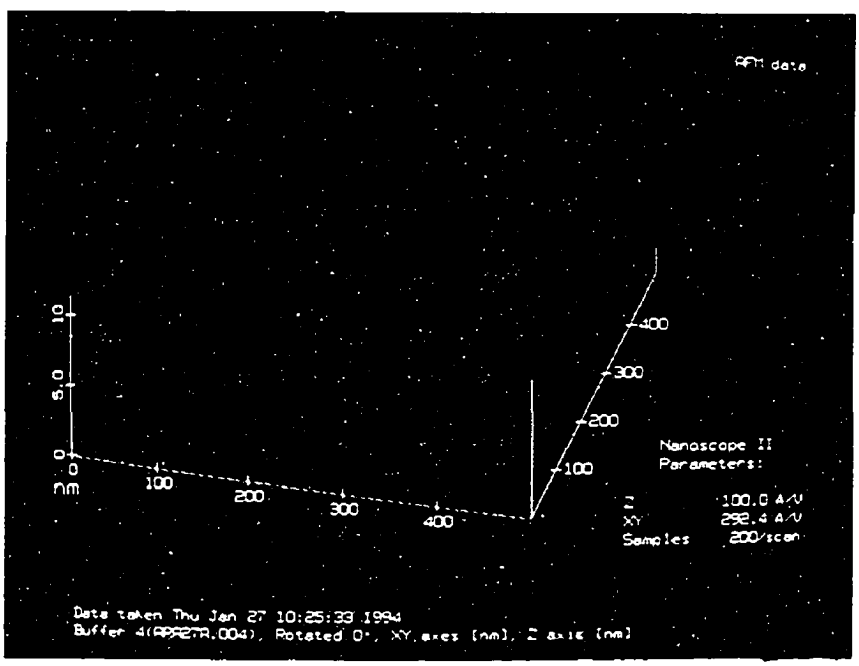


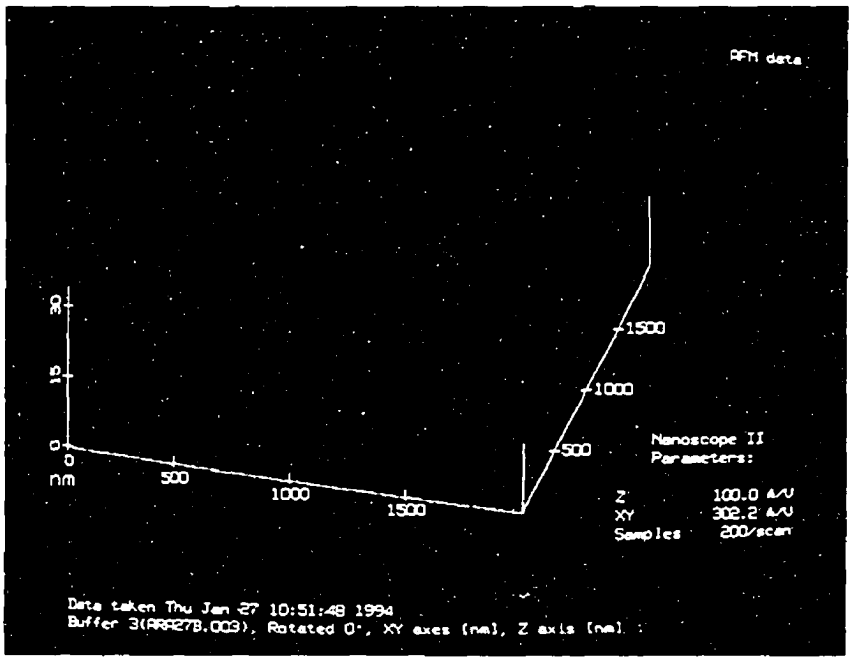
Figure 4.11 A Schematic drawing of a damaged region produced by the alloying contact of GaAs at 630°C for 30 seconds [50]



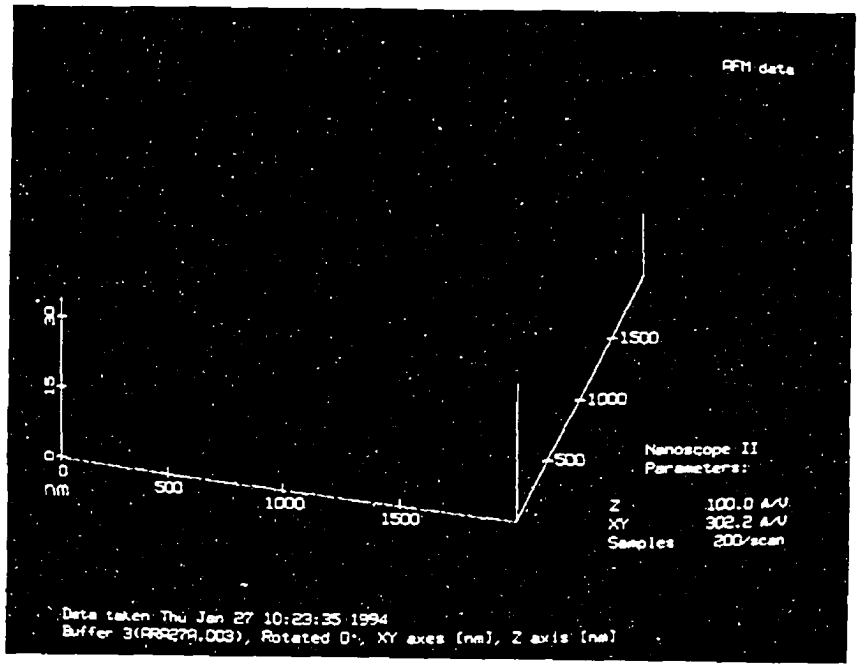
(a) before laser irradiation



(b) after laser irradiation



(c) before laser irradiation



(d) after laser irradiation

Figure 4.12 AFM disordered Si surface after laser irradiation (excitation voltage of 24 kv, period of 0.1sec) on Si before Al deposition

Figure 4.13 shows a typical I-V characteristic of a disordered Si/c-Si heterojunction diode. It shows the Ohmic behavior of large current in negative bias and rectification behavior of space charge limited current, after Ohmic behavior up to approximately 0.5V. In the space charge limited region, according to the relation $I = k (V-V_{th})^m$, the exponent m was determined to be 2.4. Threshold voltage, V_{th} is 0.5V and proportional to L^2[51], where L is the thickness of the disordered Si layer. Figure 4.14 shows in semi-log plot the I-V characteristics of another sample. Schottky barrier height, Φ_B is

$$\Phi_B = \frac{kT}{q} \ln(\frac{A^{**}T^2}{J_s}), \tag{4.1}$$

where A^{**} is a Richardson constant of 120 $A/cm^2/K^2$, and the extrapolated value of current density at zero voltage is the saturation current, J_s. From Figure 4.14, I_S is 1.61E-06. Using T = 300K, and contact area = $\pi(0.14)^2$, Φ_B = 0.64 eV. In Al/p-Si contact without annealing, the barrier height which has been reported [52] is about 0.75eV. There is small difference of 0.11eV in Schottky barrier height.

From the straight line portion of the plot, I_S (1.61E-06) can be determined by extrapolation when V=0, and it gives ideality factor n, from the slope S = d log(I)/dV.

$$n = \frac{1}{2.3}\frac{q}{kT}\frac{d\log(I)}{dV} = \frac{1}{2.3SkT/q} \tag{4.2}$$

The slope, S is 3.32 in Figure 4.14. Therefore, the ideality factor n, is 5 near 0V. Above 0.4V, n is bigger than 5. Considering the ideality factor to be 1 to 2, this big ideality factor means that the current is limited as voltage increases. In some samples, space charge limited currents were not observed, but Ohmic behaviors

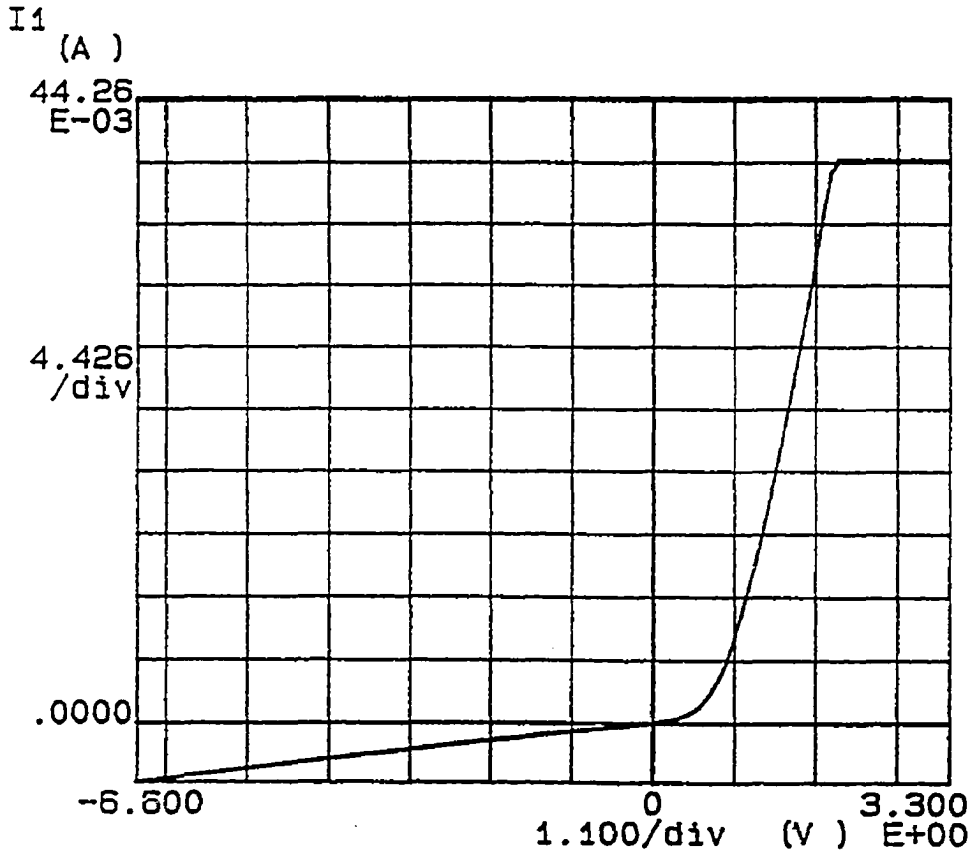
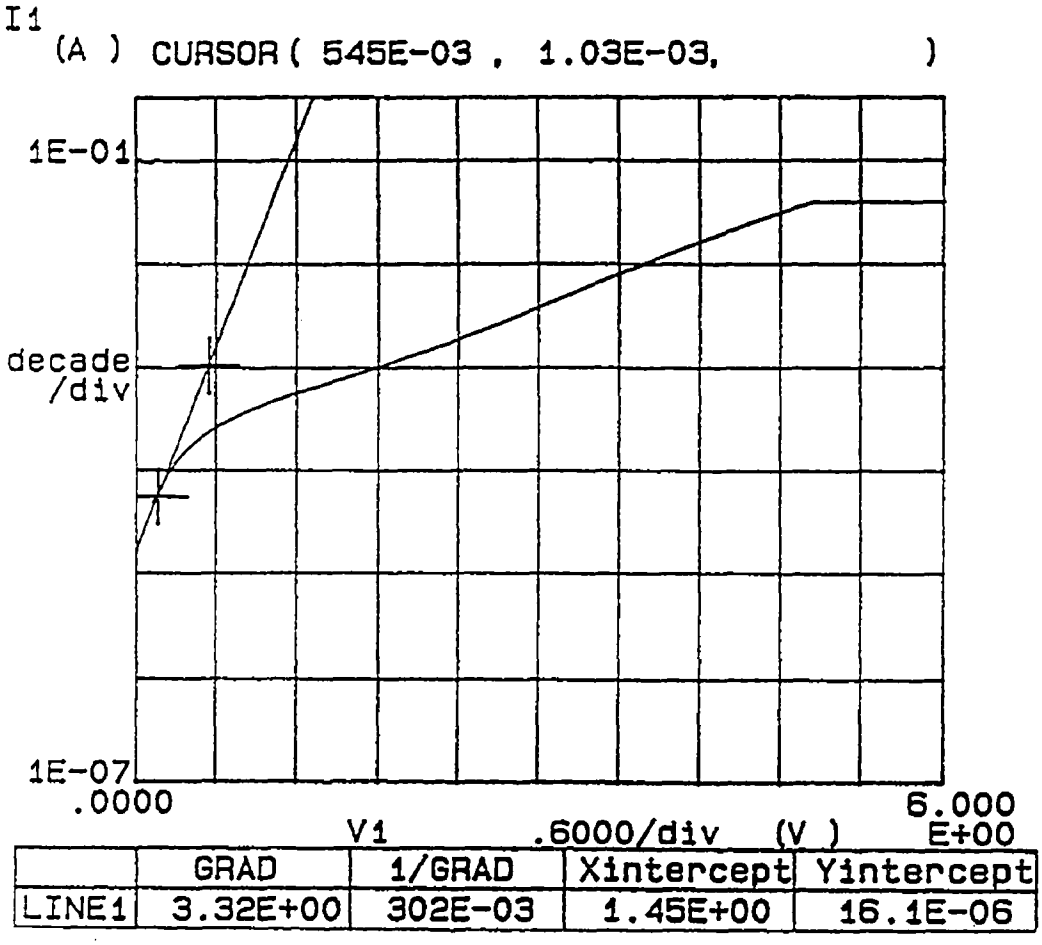


Figure 4.13 I-V characteristic of a disordered Si/c-Si heterojunction diode



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	3.32E+00	302E-03	1.45E+00	16.1E-06

Figure 4.14 I-V characteristic on semi-log plot of a disordered Si/c-Si heterojunction diode

were observed in both biases. This means that the threshold voltage of the space charge limited current will be high. Figure 4.15 shows the space charge limited current after ohmic behavior in both biases. Threshold voltage is 0.6V and -0.6V in both biases.

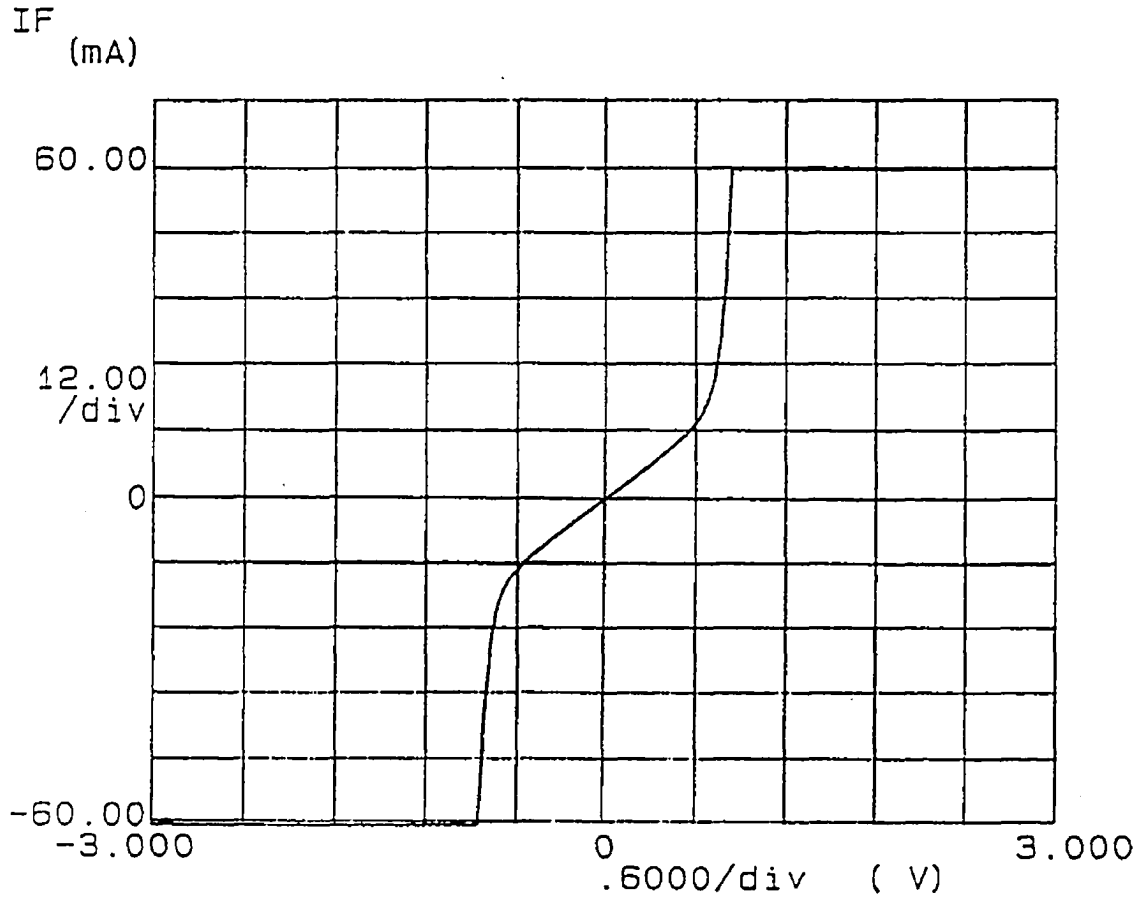


Figure 4.15 A space charge limited current after ohmic behavior in both biases with a disordered Si/c-Si heterojunction diode

4.1.3 Negative Resistance after Strong Laser Irradiation on Al Contacts

Figure 4.16 shows an excellent N-type negative resistance, after strong laser irradiation (excitation voltage of 24kv, period of 1 sec), on an Al contact. The peak current is approximately 27mA at 1.4v and the slope in the negative resistance region is 79Ω. Figure 4.17 also shows another excellent negative resistance, after the same strong laser irradiation, on contacts of both sides. But, those negative resistances were unstable and only maintained for a few days.

The requirements of a material, to show negative resistance, may be broadly divided into two categories, one containing intrinsic and one containing extrinsic properties. The intrinsic requirements concern the band structure and the scattering mechanisms in the material. It is apparent from what has gone before that the band structure should be such that hot electrons (or holes) move quickly from a high mobility state to a low mobility state as the field is increased. The higher energy band should therefore have a high density of states or, if ellipsoidal, at least have a very high effective mass in the field direction relative to the lower band.

It is possible that uniaxially strained p-type silicon has the necessary structure. The strained region can be induced by a laser-alloying process. Under uniaxial strain, the degeneracy of the 'light' and 'heavy' valence bands at $k = 0$ is removed and two ellipsoids, with their major axes at right angles to one another, appear separated in energy at $k = 0$. When holes become hot, they will tend to move from the lower ellipsoid into the 'heavier' upper ellipsoid. Hensel and Feher [53] have measured inverse-mass parameters in silicon for strains in the [001] and [111] directions; so taking their interpretation of the band structure as being reasonable, and assuming that the ellipsoids actually intersect one another in the strain direction, we can make an estimate of the possibility of negative resistance.

The Extrinsic requirements concern the carrier density in the main. The capture of an electron by a negatively-charged impurity center in a semiconductor

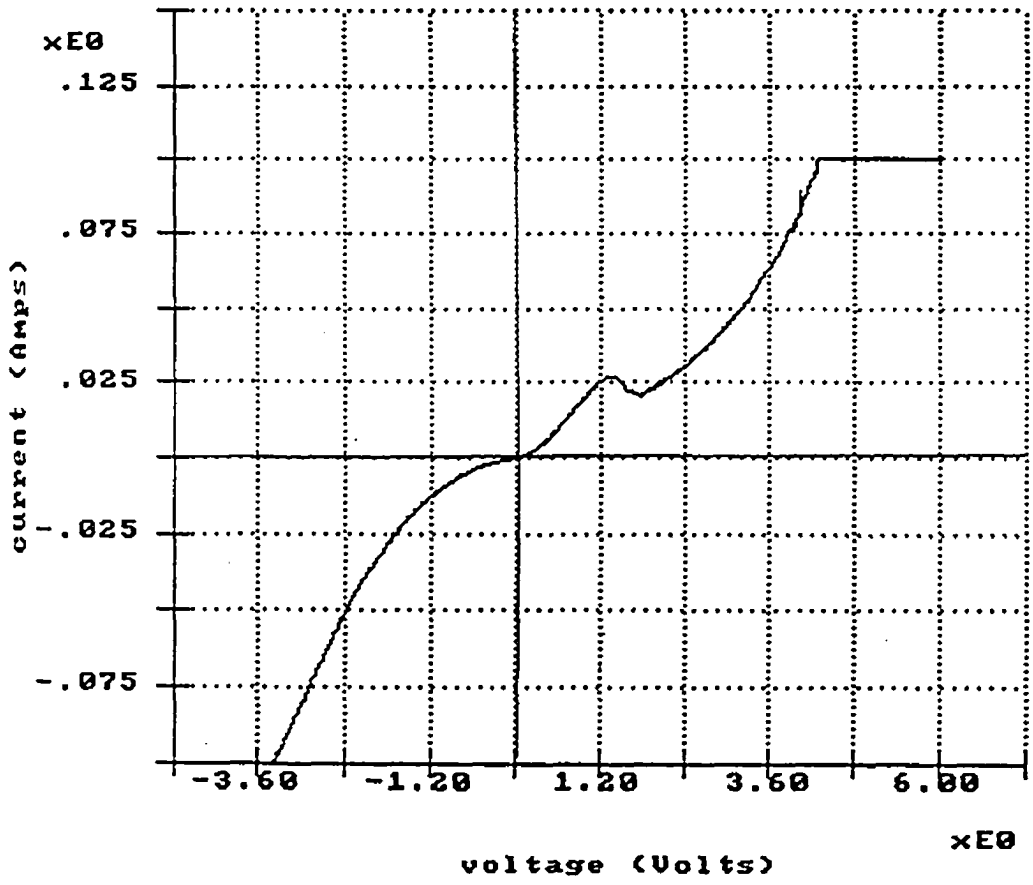


Figure 4.16 A negative resistance after strong laser irradiation (excitation voltage of 24kv, period of 1 sec) on an Al contact

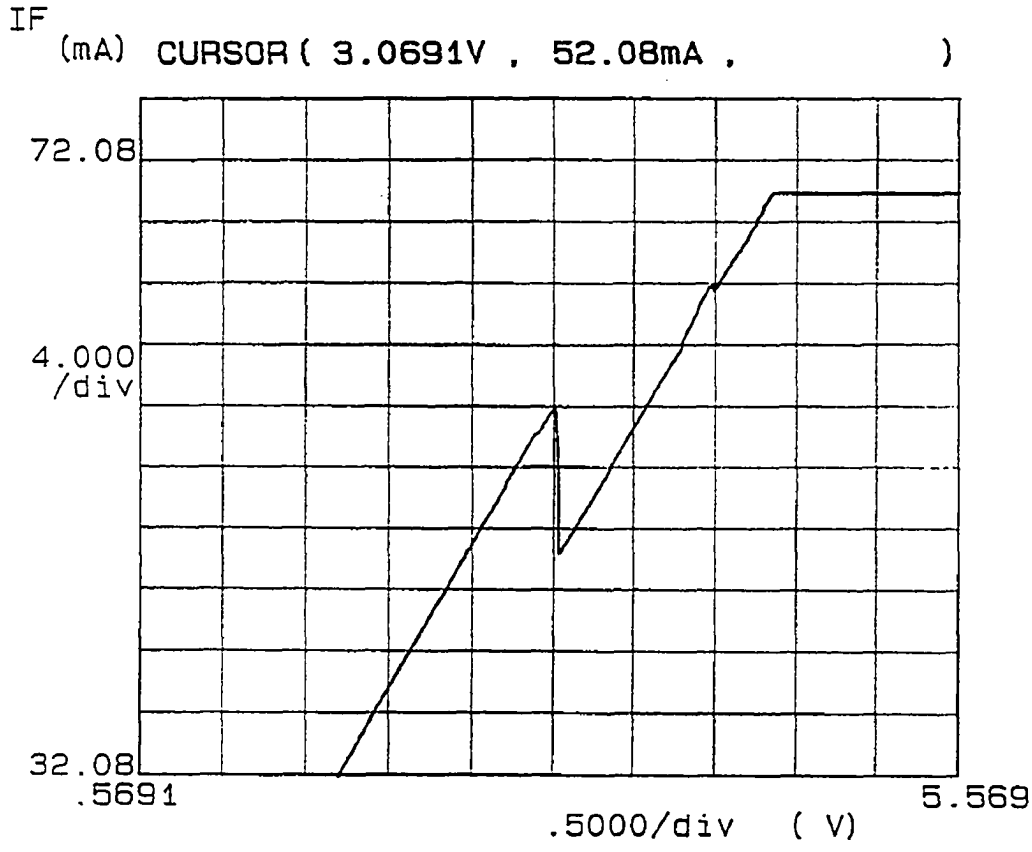


Figure 4.17 A negative resistance after strong laser irradiation (excitation voltage of 24kv, period of 1 sec) on both sides of the Al contacts

is strongly influenced by the presence of the potential barrier, arising out of the Coulomb repulsion. The lower the temperature, the smaller the electronic thermal energy and the effect on the barrier will be greater. Heating the electrons by an electric field will tend to increase the probability of tunneling through the barrier, and so increase the capture rate. The resultant fall of electron density as the field increases, if great enough, will cause a bulk differential negative resistance to appear. We find that this effect, the possibility of which was discussed by Ridley and Pratt [54], occurs in n-type gold-doped germanium at 20°K. Also, we find that instability, associated with the negative resistance, causes the specimen to split up into high field and low field regions in the manner described by Ridley and Watkins [55].

Let us consider the conduction band to consist of two sub-bands which may be represented in the (ε , k) diagram, as shown in Figure 4.18. The lower band is denoted 'a' and the upper 'b'. The energies of the minimum are $\varepsilon_{a,b}$ and their energy difference E. Their effective density of states are $N_{a,b}$. We assume that the k direction is along a principal axis which is parallel to the electric field E, and the effective masses and mobilities are $m_{a,b}$. and $\mu_{a,b}$. The numbers of electrons per cubic centimeter in the bands are $n_{a,b}$. The conductivity is then given by

$$G = e (\mu_a n_a + \mu_b n_b) \qquad (4.3)$$

When a sufficiently high electric field is applied to the crystal, the electrons are accelerated and their effective temperature rises above the lattice temperature, and in most cases, we must also expect the lattice temperature to increase. The effect of this will be not only to alter the mobilities, but also to alter the electron densities in the bands. The incremental variation of conductivity with field may be written.

$$\frac{dG}{dE} = e\left(\mu_a \frac{dn_a}{dE} + \mu_b \frac{dn_b}{dE}\right) + e\left(n_a \frac{d\mu_a}{dE} + n_b \frac{d\mu_b}{dE}\right) \tag{4.4}$$

or, putting $n_a + n_b = n$, where n is constant, and taking $\mu_{a,b} \propto F^p$,

$$\frac{dG}{dE} = e(\mu_a - \mu_b)\frac{dn_a}{dE} + e(\mu_a n_a - \mu_b n_b)\frac{p}{E} \tag{4.5}$$

Since the current density

$$J = GF \tag{4.6}$$

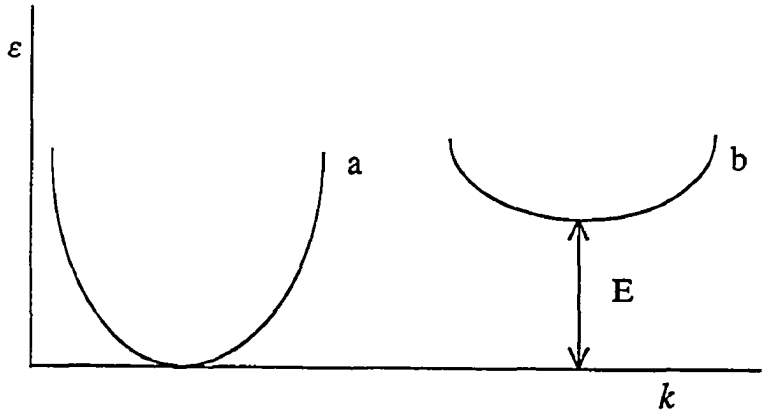


Figure 4.18 Two sub-bands in a semiconductor

and $$\frac{dJ}{dE} = G + F\frac{dG}{dE} \tag{4.7}$$

the condition for negative resistance is

$$-\frac{\frac{dG}{dE}}{\frac{G}{E}} > 1 \tag{4.8}$$

or, from Eqns (1) and (2) with $f = \frac{n_b}{n_a}$,

$$\left[\left(\frac{\mu_a - \mu_b}{\mu_a + f\mu_b}\right)\left(-\frac{E}{n_a}\frac{dn_a}{dE}\right) - p\right] > 1 \tag{4.9}$$

The field exponent p is a function of the scattering mechanism and should be negative and large. This makes impurity scattering quite undesirable since, when this is dominant, the mobility rises with increasing field and thus p is positive. When lattice scattering is dominant, however, p is negative and will depend on the lattice and carrier temperatures. The first bracket in equation (4.9) is straightforward - we must have $\mu_a > \mu_b$. Electrons must begin in a low mass band and transfer to a high mass band when they are heated by the field. The maximum value of this term is unity i.e. when $\mu_a >> \mu_b$. The second bracket is not so easy to deal with. It represents the rate at which electrons transfer to the upper band with field and this will depend upon differences between the bands of effective density of the states, electron temperature, and the energy gap between the sub-bands. To obtain an idea of its value, let us assume a common electron temperature T_e and a Maxwell - Boltzmann distribution. If we have $T_e \propto E^q$ then

$$-\frac{E}{n_a}\frac{dn_a}{dE} = -q\frac{T_e}{n_a}\frac{dn_a}{dT_e} \tag{4.10}$$

If E is the band separation it may be shown that with $f = \left(N_b / N_a\right)\exp\left(-E / kT_e\right)$

$$-\frac{T_e}{n_a}\frac{dn_a}{dT_e} = \frac{f}{1+f}\left(\log\frac{N_b}{N_a} - \log f\right), \tag{4.11}$$

where $N_{a,b}$ are the effective densities of states, which has a maximum value where

$$\log\frac{N_b}{N_a} - \log f = 1 + f \tag{4.12}$$

4.1.4 Bistable Switching with Memory in Both a Disordered Si/c-Si Diode and an Amorphous SiC/c-Si Diode

Bistable switching, between a stable low-conductivity state and a stable high-conductivity state, has been observed in both non-hydrogenated amorphous SiC/c-Si diodes and disordered Si/c-Si diodes. To make a disordered Si layer, an excimer laser was used to irradiate uniformly the surface of c-Si before Al deposition. Typical switching I-V characteristics of both diodes are shown in Figure 4.19 and Figure 4.20. In a disordered Si/c-Si diode (Figure 4.19), a rectifying state was observed in the range between 0V and 3V. While the voltage was 4V, switching from a rectifying state to Ohmic state was observed. Either state was maintained over several months without bias. In a amorphous SiC/c-Si diode (Figure 4.20), after a threshold voltage of approximately 3V was applied, switching between a stable low-conductivity state and a stable high-conductivity state via a transient on state [56], was observed. Either state was also maintained for several months like a disordered Si/c-Si diode. The difference of switching behavior in both diodes would depend on defect densities and resistivity of an amorphous SiC and a disordered Si layer.

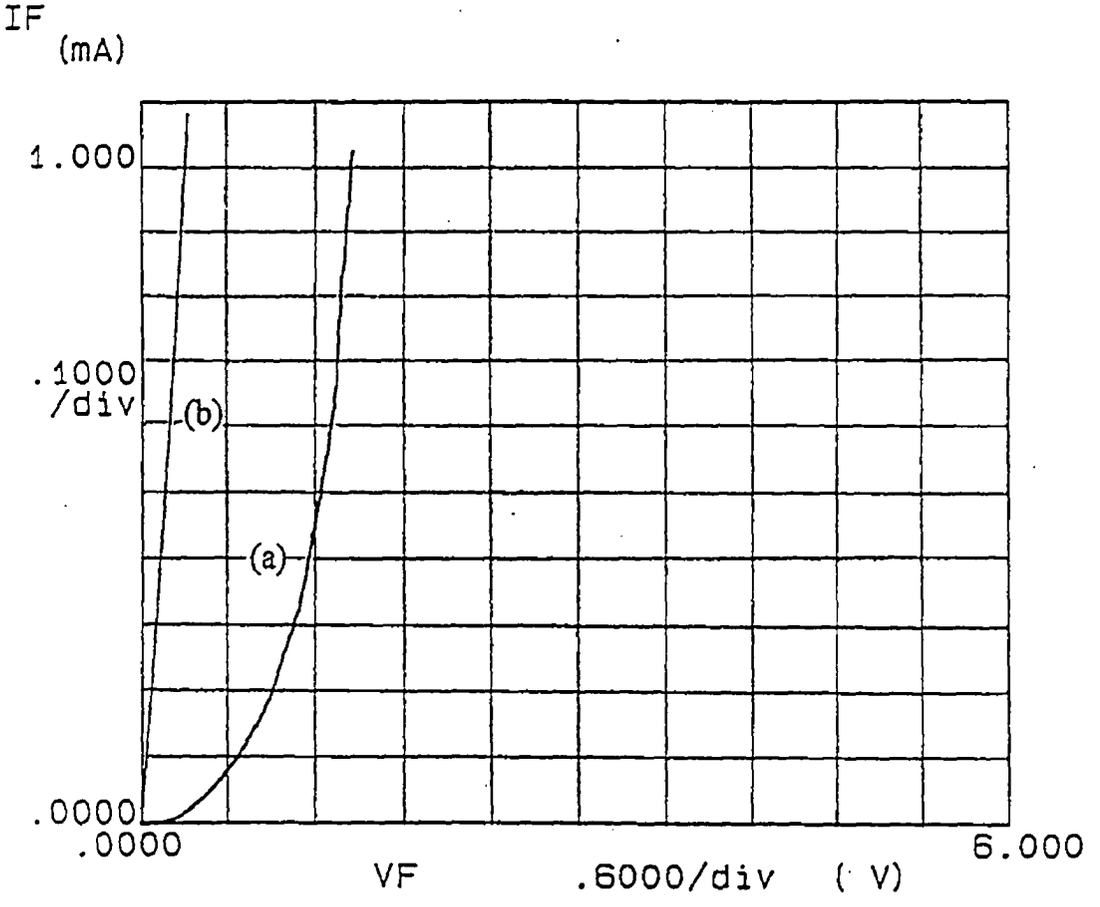


Figure 4.19 Bistable switching in a disordered Si/c-Si heterojunction diode (a) rectifying state (b) ohmic state

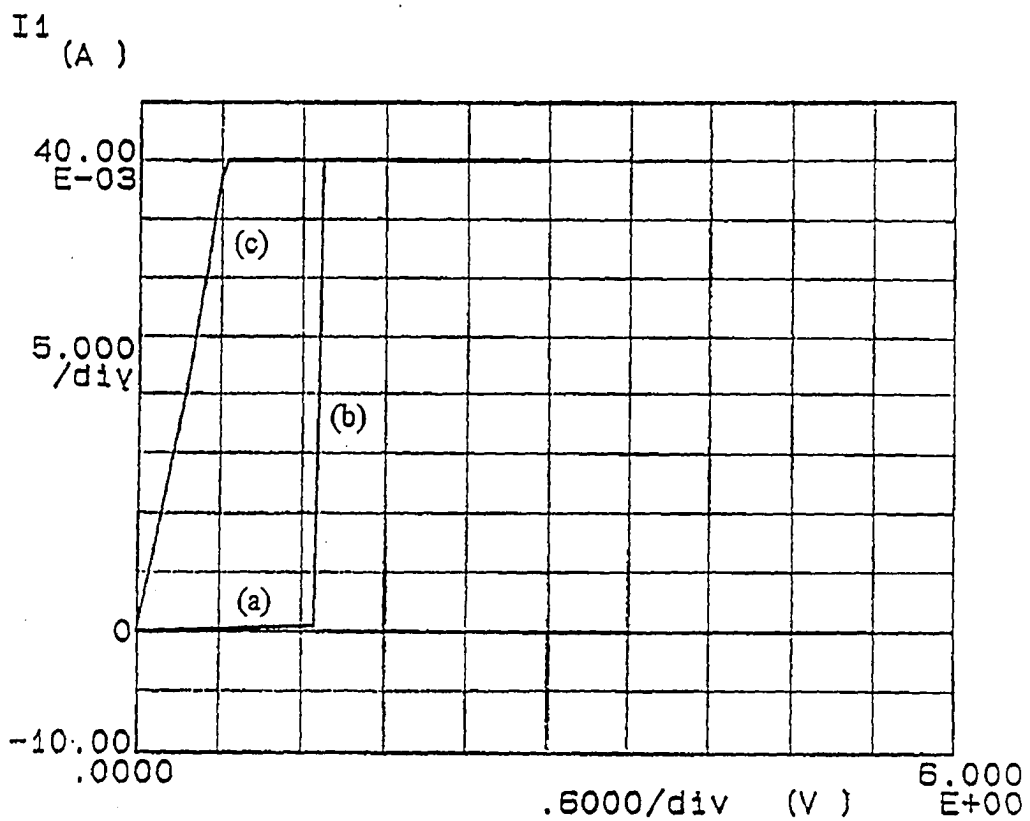


Figure 4.20 Bistable switching via the transient on state in an amorphous SiC/c-Si heterojunction diode
(a) low-conductivity (b) transient-on (c) high-conductivity

There have been several two- state nonvolatile memory devices made from a variety of materials and operating under a variety of physical mechanisms. The presence of several conductive states, in low-melting point chalcogenides [57,58], is generally attributed to phase transformations, while electronic mechanisms such as, field and impact ionization of traps are often proposed in the crystalline solid [59-61]. Bistable switching, with memory, was observed in various n-type GaAs Schottky contacts and n-type Si Schottky contacts doped with trap impurities of Ni, Au, Pt [62]. The same general type of phenomenon was observed in ZnSe-GaAs [59], GaP-Ge [59], and GaP-Si [59] heterojunctions. It was postulated that the switching and memory behavior is the result of field or impact ionization of traps, causing a transition to a low-resistance state, and the resetting to high resistance when carrier injection, from the metal contact, results in refilling the traps. These two terminal switching devices offer the potential advantages for computer memory systems of simplicity, high packing density, and low cost.

The high, intermediate and low resistance states, and threshold voltage all depend to some degree on the nature of the amorphous SiC, and disordered Si films. And, they depend on the details of the fabrication process such as, the growth temperature, the growth rate, and the cooling rate. Such a dependence might be expected in any heterojunction device, since the two materials making up the heterojunction have certain natural differences, e.g., lattice constants, thermal expansion coefficients, elastic coefficient, etc. The stress, which results from the growth, is accommodated partly by strain, partly by bending and residual stress, and even in some cases by cracking [63,64]. The bistable switching in both the non-hydrogenated amorphous SiC/c-Si diode and the disordered Si/c-Si diode is believed to be governed by the presence of defects such as traps. The defects consist of both intrinsic defects in the amorphous SiC, the disordered Si and

extrinsic defects which come from lattice mismatch, and the fabrication process as mentioned above.

Numerous densities of neutral states near the interface of the heterojunction can be ionized, and this creates a high-field region through which the carrier can readily tunnel, probably in a multistep process through the empty traps. This transforms the high impedance state to an Ohmic behavior. Carrier release, due to both field and impact ionization of the trap could be responsible for the trap emptying. Tunneling through an interface, due to traps, has been proposed as an explanation for the conduction through metal-insulator-metal structures [12,65], and can lead to both Ohmic behavior [65] and low activation energy. In addition to the interface transformation of the heterojunction, traps can be ionized in both the amorphous SiC and the laser induced Si, thus freeing electrons (or holes) into either an impurity below the conduction band edge or into the conduction band itself. These electrons then provide the necessary conductivity.

Either state, of the bistable switching, was maintained at zero bias for several months. Since the ionized traps in the bulk must remain empty with time, in spite of the high free electron density, it seems necessary that they be Coulombic-repelling states, doubly negatively charged before ionization, and singly negatively charged after, so that the barrier they present to the electrons prevents them from refilling immediately and eliminating the memory. In Figure 4.21, switching from a low impedance state to a high impedance state was instantly observed after a 3mA current pulse for 1 sec. The traps in the amorphous SiC were filled by the increased charge and the high impedance was attained. After that, switching from the high impedance state to the low impedance state was again observed above 2V as shown in Figure 4.22. But, the low impedance state in Figure 4.22 was not returned back to the original low impedance state in Figure 4.20.

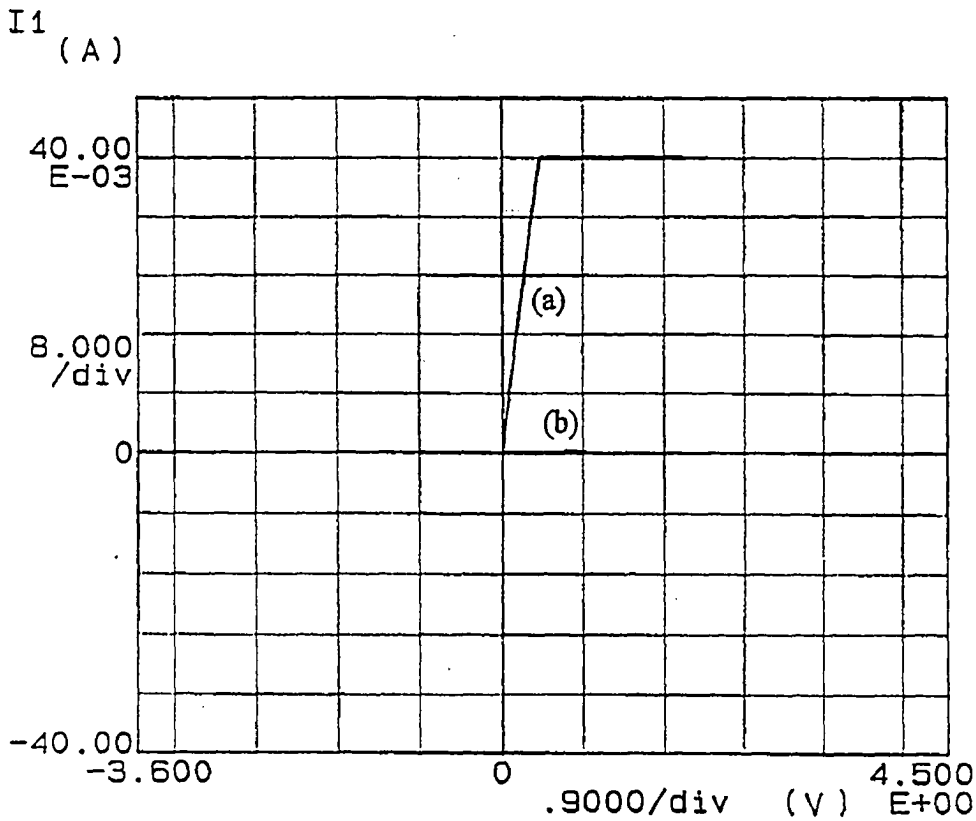


Figure 4.21 Switching from a low impedance state (a) to a high impedance state (b) after a current pulse of 3mA for 1 sec in an a-SiC/c-Si heterojunction diode

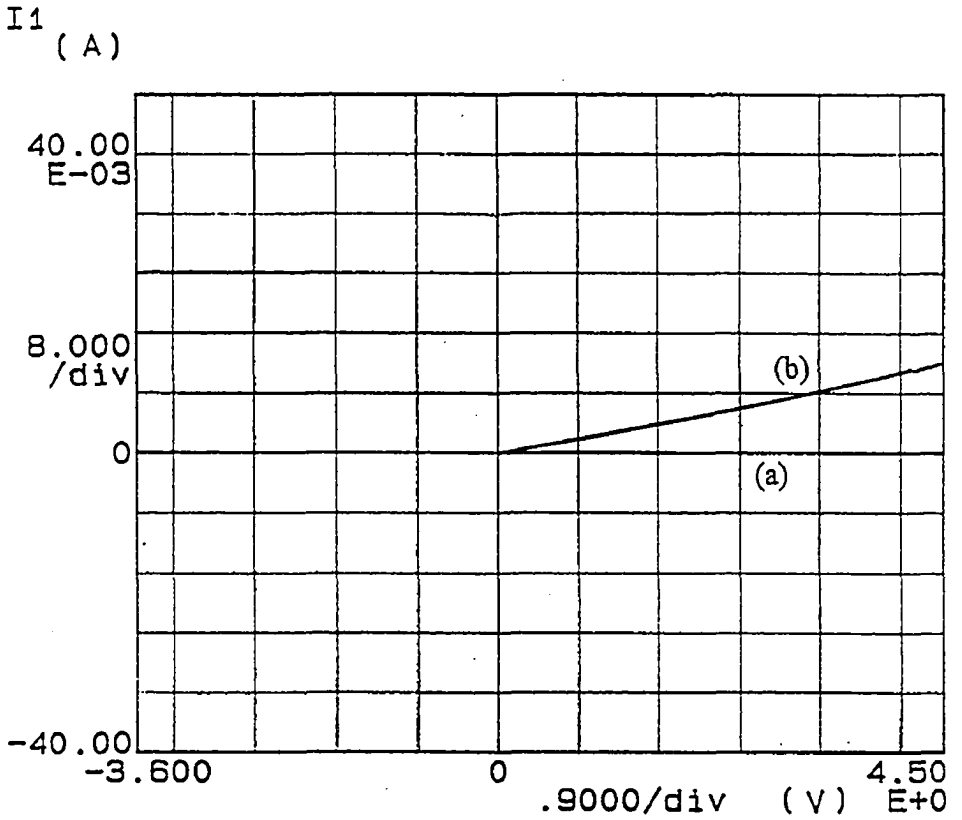


Figure 4.22 Switching from a high impedance state (a) to a low impedance state (b) at 2v in an a-SiC/c-Si heterojunction diode

This phenomenon means that trap emptying is not complete because of abundant carrier filled by the current pulse.

Finally, it should be noted that this trap model for the switching and memory is speculative, and although it describes the experimental result well, other models may also be proposed. A dielectric relaxation model of van Roosbroeck is a notable example. And, An injection model was proposed by Gary Vezzoli [56].

4.2 Novel Negative Capacitance in C-V and Comparison with the Model

4.2.1 Negative Capacitance in Laser Induced Disordered Si/c-Si Diode and Comparison with the Model

A heterojunction diode, with a disordered Si which was induced by excimer before Al deposition, showed a constant negative capacitance of - 1950pF at 1MHz from - 5V to 5V in C-V measurement (Figure 4.23). This phenomenon, of the constant negative capacitance has not yet been reported. The measured negative capacitance was derived from the circuit model described in section 3.4.

From the circuit model a depletion capacitance, near the interface of c-Si/Al, is increased in forward bias. And, a diffusion capacitance, in the bulk of c-Si, is increased in reverse bias. In the both biases, inductance, which is developed by the carrier injection through the disordered Si, is dominant for the large series-capacitance. The measured capacitance follows the relation of equation (3.30),

$$C_{test} = - \frac{1}{\omega^2 L_{test}} \tag{4.13}$$

Therefore, according to the above equation, inductance is 13μH. The inductance value of this diode, measured by a LCR analyzer at 1MHz, was also 13μH. The theoretical circuit model had good agreement with this experiment.

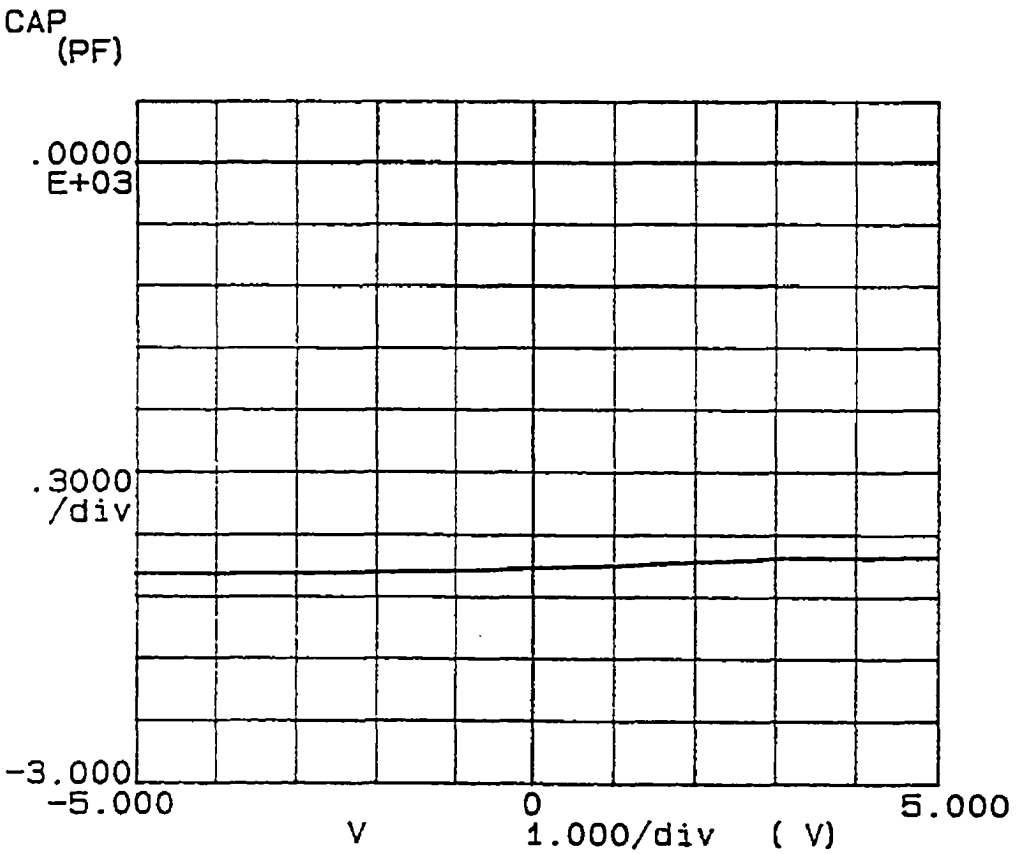


Figure 4.23 Negative capacitance in a disordered Si/c-Si heterojunction diode

In Figures 4.24, and 4.25, negative capacitances are also shown and their inductance values were approximately 17μH, and 23μH at 1MHz.

In a real inductor, the series-capacitance of the circuit model is very small in both biases. A constant negative capacitance of the real inductor was shown in C-V measurement, and the magnitude of the negative capacitance followed the same relation of equation (2), and this experiment conformed the theory. In Figure 4.26, a real inductor, of which inductance is 100μH, shows a negative capacitance. Its magnitude of negative capacitance is approximately - 237pF at 1 MHz. From the relation of $L_{test} = 1/\omega^2|C_{test}|$, the inductance of 100μH can be derived with capacitance of - 237pF at 1MHz.

This constant negative capacitance of a semiconductor device was discovered for the first time. The C-V characteristics, of a novel heterojunction diode, is the same as that of a real inductor. And, Inductance values of both a diode and a real inductor follow the relation of $L_{test} = 1/\omega^2|C_{test}|$. In the comparison of the diode with a real inductor, intrinsic capacitance (depletion capacitance or diffusion capacitance) of the diode is very large in both biases although that of a real inductor is very small. So far, a negative capacitance was simulated and observed in a Schottky diode only above a certain bias. In X. Wu's paper, he reported a phenomenon observed during the experiment that, under forward bias, some Schottky diodes manifest a negative capacitance in response to an ac signal. A new hypothesis, of charge delocalization at the interface of a metal/semiconductor, was proposed to explain this effect. It was suggested that the Shockley-Read model [66] was inadequate in describing the occupancy probability of interface states at a high incidence of hot carriers. Under this circumstance, the impact ionization process above a certain forward bias was taken into consideration. But, with this hypothesis, the negative capacitance in both biases, even at zero bias, can not be

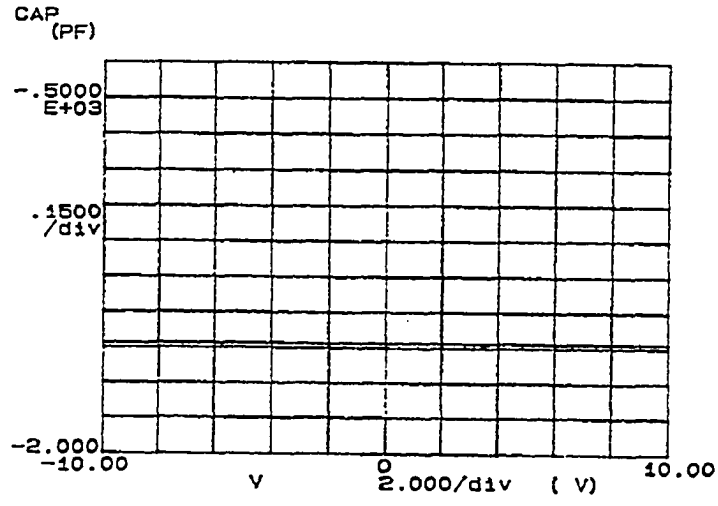


Figure 4.24 Negative capacitance, equivalent inductance of $17\mu H$ in a disordered Si/c-Si heterojunction diode

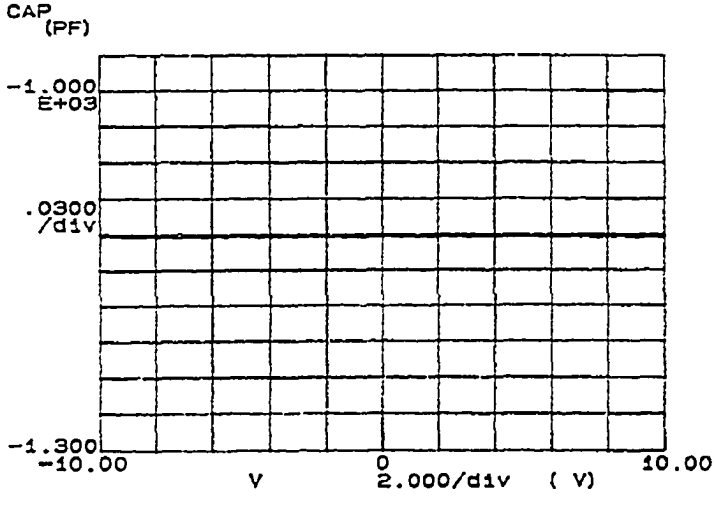


Figure 4.25 Negative capacitance, equivalent inductance of $23\mu H$ in a disordered Si/c-Si heterojunction diode

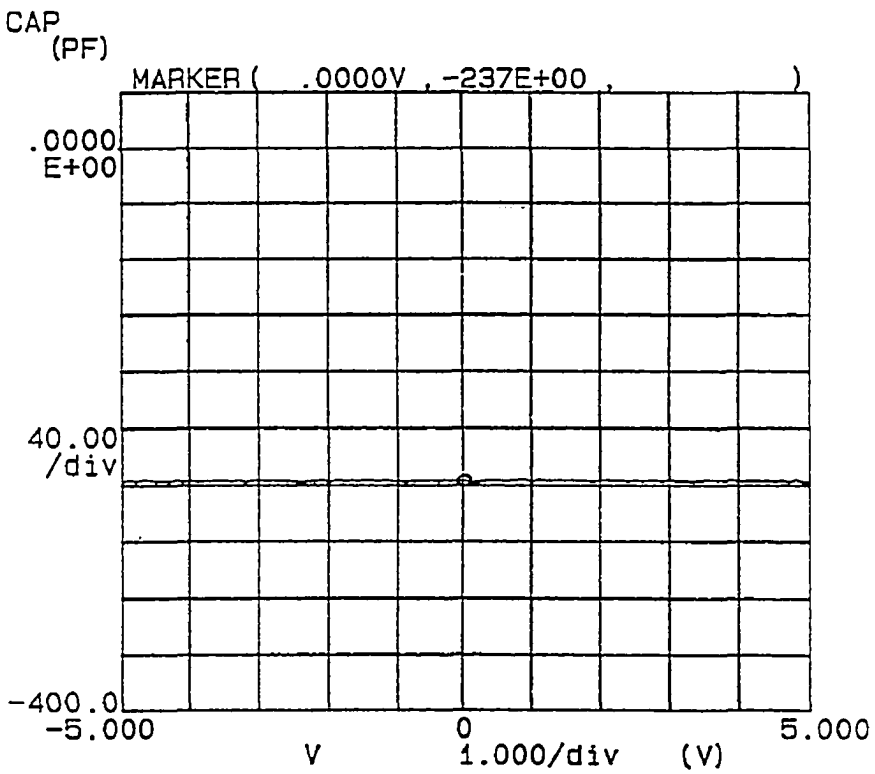


Figure 4.26 C-V measurement of a real inductor of $100\mu H$

explained. As I mentioned in Ch. 3, this negative capacitance can be explained by the conductivity modulation through a high resistivity-relaxation semiconductor with carrier injection in both biases. Inductive reactance is developed due to the conductivity modulation. When the inductance is dominant for a large depletion capacitance or diffusion capacitance in both biases, this novel diode shows inductive behavior and constant negative capacitance in both biases. In ordinary diodes, the effect of the conductivity modulation is too small to produce useful inductive reactance. The junction capacitance normally masks the inductive effect, except at high forward bias, even though the inductive reactance appears in a low doping diode. In a few samples, a negative capacitance was observed only in negative bias as shown in Figure 4.27. This means that a large series capacitance was developed in only the negative bias. Near zero bias, the diode shows resonance ,and behaves as a pure resistance. The negative capacitance, in Figure 4.27, is similar to that which X.Wu observed in a $NiSi_2$-Si diode at 200K.

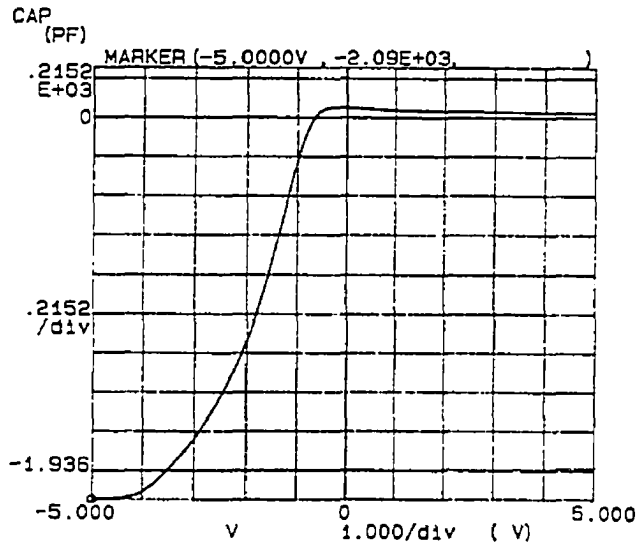


Figure 4.27 Negative capacitance only in forward bias with a disordered Si/c-Si diode

In Figure 4.28, The C-V measurement of a real diode is shown. Figures 4.29 and 4.30 show the C-V measurement of the diode connected in series with real inductors of 2μH, and 100μH. A resonance is shown at approximately 0.5V. The diode by itself has a large capacitance of 3800pF in positive bias. But, with the series connection of real inductors, negative capacitance is shown only in positive bias. It means that owing to a big series capacitance of a diode in positive bias, an inductive effect was shown as a phenomenon of negative capacitance only in positive bias.

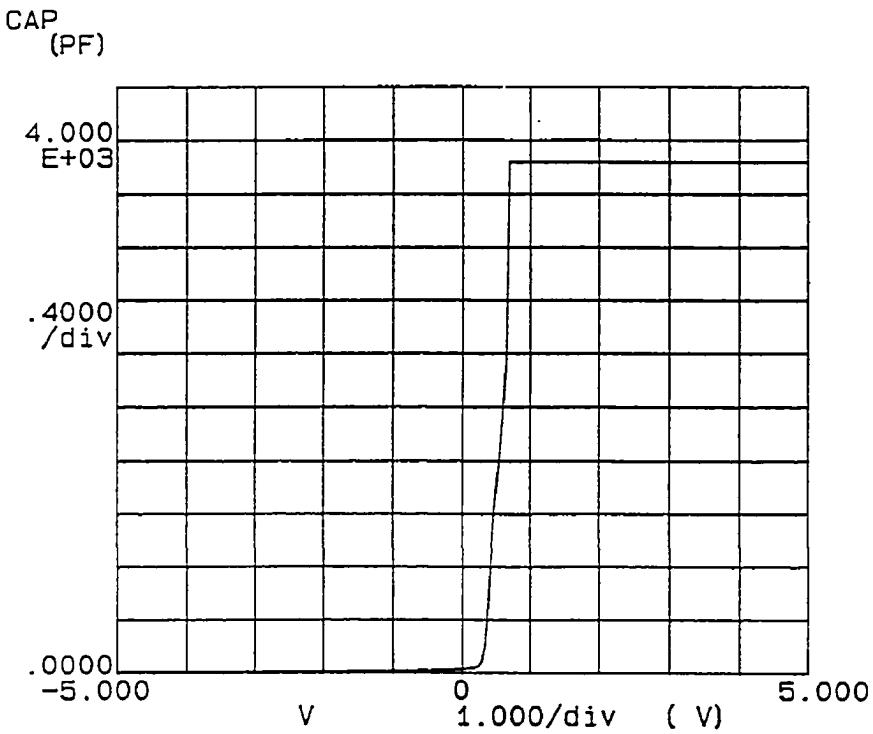


Figure 4.28 C-V measurement in a real diode

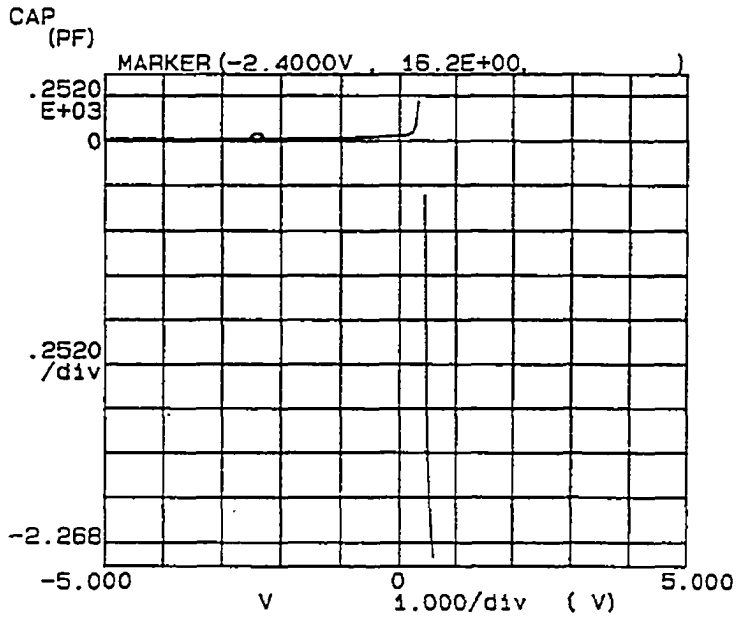


Figure 4.29 C-V measurement in a real diode with the series connection of a real 2μH inductor

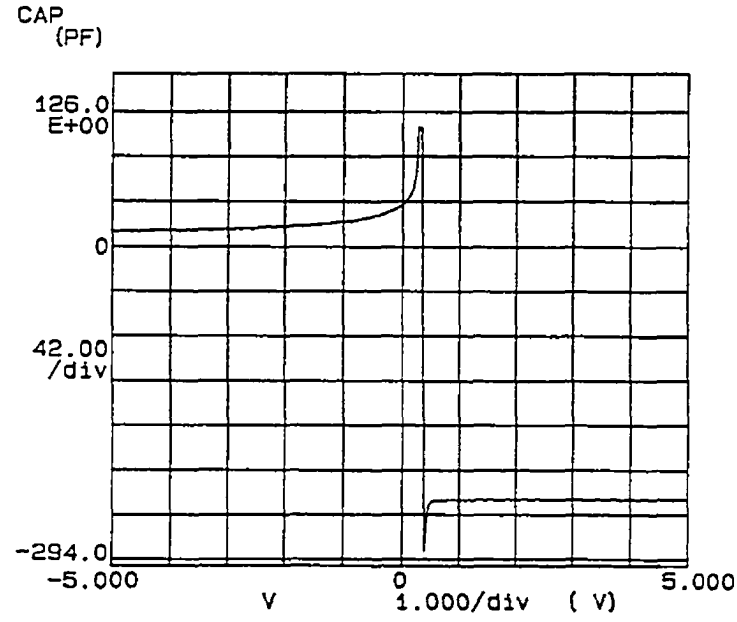


Figure 4.30 C-V measurement in a real diode with the series connection of a real 100μH inductor

Table 1 shows variation of negative capacitance, and equivalent inductance, in a disordered Si/c-Si heterojunction diode listed according to various frequencies at zero bias, as measured by a HP-LCR Analyzer. Inductance is almost constant even with the variation of frequency like the characteristic of a real inductor. This is a case of $\omega\tau_d < 1$, where τ_d is dielectric relaxation time, as mentioned in 3.3. Approximately, 80 % of the samples showed this constant inductance even with the variation of frequency.

Table 1 Data - I of LCR Analyzer with a Disordered Si/c-Si Diode

Frequency	R(Ω)	X(Ω)	C	L
1MHZ	16.76	12.25	-12.98nF	1.95μH
800KHz	16.61	9.86	-20.16nF	1.96μH
500KHz	16.45	6.24	-50.94nF	1.98μH
300KHz	16.35	3.8	-139.5nF	2.01μH
100KHZ	16.24	1.3	-1.219μF	2.07μH
60KHz	16.22	0.79	-3.35μF	2.09μH
10KHz	16.22	0.13	-117μF	2.15μH
6KHz	16.21	0.08	-325μF	2.16μH

Table 2 shows the variation of inductance with a 50% decrease in frequency starting at 1MHz. Inductance was increased four times with a 50% decrease in frequency. This is a case of $\omega\tau_d > 1$, where τ_d is dielectric relaxation time, as mentioned in section 3.3. Inductance, L, is proportional to $1/\omega^2$ under the condition of $\omega\tau_d > 1$. This inductance has a non-linear characteristic, not a linear characteristic like a real inductor. A large inductance value was demonstrated at low frequency. Approximately 20% of the samples, of disordered Si/c-Si diodes, showed this non-linear inductive characteristic.

Table 2 Data - II of LCR Analyzer with a Disordered Si/c-Si Diode

Frequency	L (sample 1)	L (sample 2)	C (sample 2)
1MHz	10μH	16.713μH	-1.52nF
500KHz	37.4μH	60.35μH	-1.684nF
250KHz	140μH	230.12μH	-1.766nF
120KHz	585μH	962.02μH	-1.832nF
60KHz	2.29mH	3.76mH	-1.874nF
30KHz	8.99mH	14.74mH	-1.915nF

4.2.2 Negative Capacitance in a Non-Hydrogenated Amorphous SiC/c-Si Diode and a Comparison with the Model

The electrical characteristics of a non-hydrogenated amorphous SiC/c-Si diode and a disordered Si /c-Si are very similar in switching, and negative capacitance. Both diodes are a heterojunction; one has a wide energy gap semiconductor and the other has a small energy gap semiconductor. Numerous defective states exist in both non-hydrogenated amorphous SiC and Si disordered by an excimer laser. Both of two materials are relaxation semiconductors.

Figure 4.31 shows the negative capacitance of the C-V measurement in a non-hydrogenated amorphous SiC/c-Si diode (thickness of 20nm in a-SiC). Above 4V and below -4V, the negative capacitance is constant. The inductance value is approximately 20.2μH above 4V, and 20μH below -4V. Between -4V and 4V, the shape of the negative capacitance is parabolic. At zero bias, inductance is approximately 15.5μH. The difference of maximum and minimum inductance is approximately 5μH. From the circuit model in section 3.4, the difference of measured inductive reactance is

$$L_{test} = L - \frac{R^2 C}{1+\omega^2 R^2 C^2} \tag{4.14}$$

$$\Delta L(C) = \frac{R^2 C(0)}{1+\omega^2 R^2 C^2(0)} = 5\mu\text{H} \tag{4.15}$$

where C is a junction capacitance , and R is a differential resistance at 0V

In Figure 4.32, computer simulation, with ω=1MHz, and R=100Ω, shows two solutions at point a, and b which satisfy equation (4.1) Since the inductive reactance, L_{test} increases from 0V to 4V ($L_{test} = 1/\omega^2 |C_{test}|$), only the capacitance at point b ($4.417 \cdot 10^{-9}$F) should be chosen.

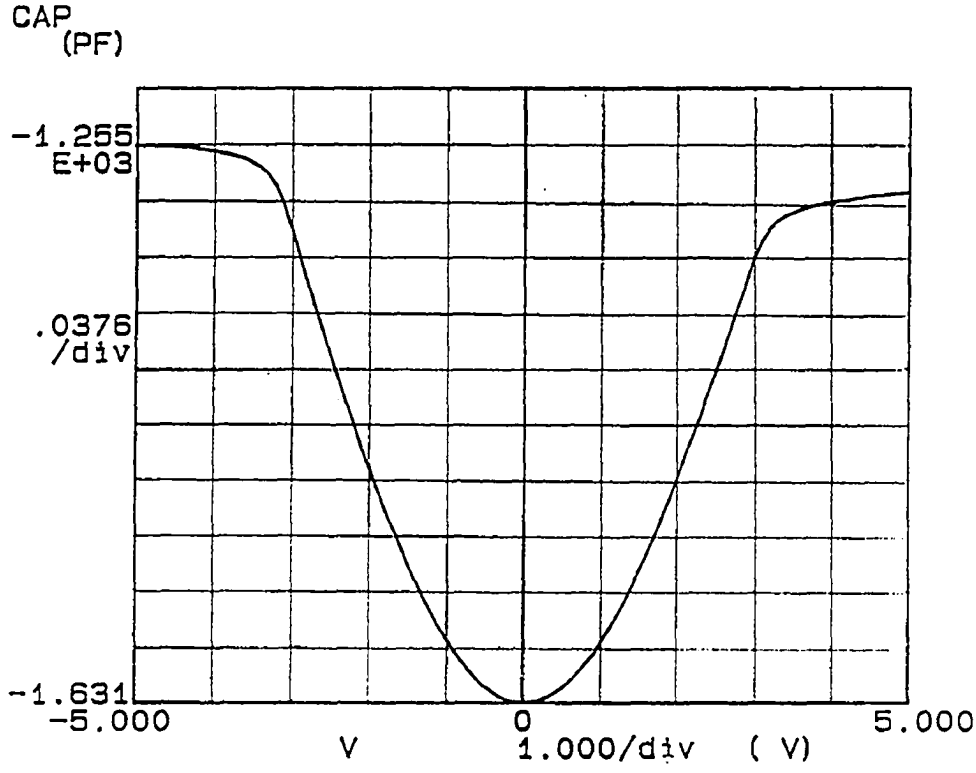


Figure 4.31 Negative capacitance in an amorphous SiC/c-Si heterojunction diode

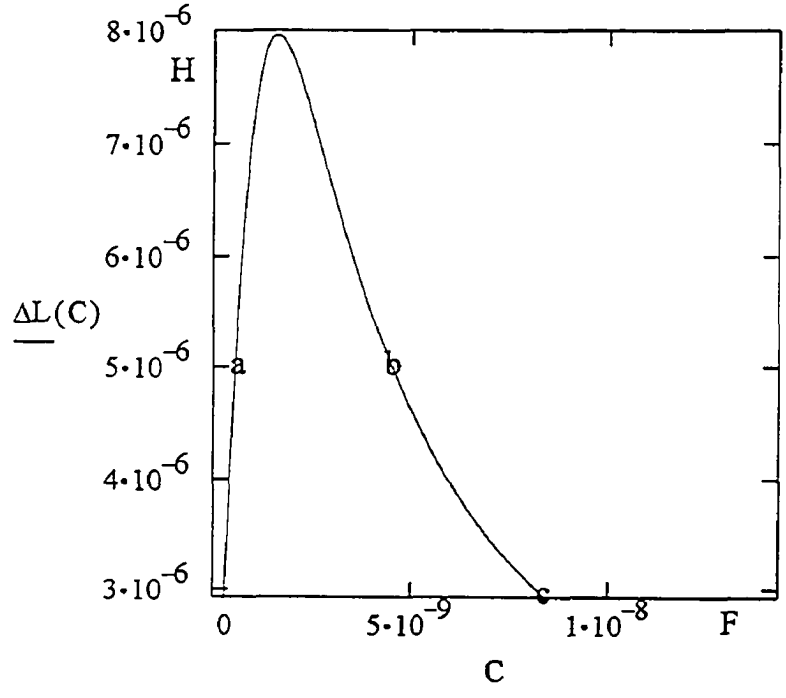


Figure 4.32 Computer simulation of $\Delta L(C)$ according to the variation of C, where $\Delta L(C) = R^2C/(1+\omega^2R^2C^2)$ with ω=1MHz, and R=100Ω. $a = 4.963 \cdot 10^{-10}$, $b = 4.417 \cdot 10^{-9}$, $c = 8.45 \cdot 10^{-9}$

When junction capacitance is larger than the capacitance at point c ($8.45 \cdot 10^{-9}$F), the second term of equation (4.2) disappears. A measured inductive reactance is the same as the intrinsic inductance which is developed in the relaxation layer ($L_{test} \approx L$). Assuming a increasing diffusion or depletion capacitance is

$$C(V) = A \exp(qV / BkT) \tag{4.16}$$

From $C(0) = 4.417 \cdot 10^{-9}$ F, and $C(4) = 8.45 \cdot 10^{-9}$ F

$$C(V) = 4.417 \cdot 10^{-9} \exp(0.16\, V) \text{ F} \tag{4.17}$$

Using the above capacitance, which increases with voltage, and proper inductance which decreases exponentially with voltage (see section 3.1), computer simulation of capacitance vs. voltage can be obtained from the equation (3. 30). Figures 4.33, 4.34, and 4.35 show the results of the computer simulation (C_{Test}(V) vs. V) using MATHCAD 5.0. In Figure 4.33 and Figure 4.34, the simulation of C-V is almost the same negative capacitance shape as the experiment of C-V with the a-SiC/c-Si diode shown in Figure 4.31. An approximate 50% decrease of differential resistance, and a small increase of the inductance value, resulted in an almost constant capacitance of -1500pF even with a change in voltage. This is shown in Figure 4.35. This phenomenon of constant negative capacitance with a change in voltage is the same as the experiment of the C-V with a disordered Si/c-Si diode as shown in Figure 4.23. Therefore, the difference of the C-V measurement between a disordered Si/c-Si diode and a a-SiC/c-Si diode depends on resistivity, and the inductance which is developed in thin relaxation layer.

Figure 4.36 also shows the negative capacitance of an amorphous SiC /c-Si diode (thickness of about 60nm in a-SiC). Between -3.5V and 3.5V, the shape of

negative capacitance is also parabolic, and inductance is 30μH near zero bias. Inductance is a constant 36μH above 3.5V, and below -3.5V. The variation of inductance with a variation of frequency in a-SiC/c-Si was also examined by a LCR Analyzer. The inductance was almost constant between 1MHz and 50KHz, and this is the same result as that of a real inductor But, the inductance value which is proportional to $\frac{1}{\omega^2}$ was not observed. A better injecting contact on the non-hydrogenated amorphous SiC, proper control of a-SiC thickness, and better barrier contact on the crystalline Si, might help to find the inductance which is proportional to $\frac{1}{\omega^2}$.

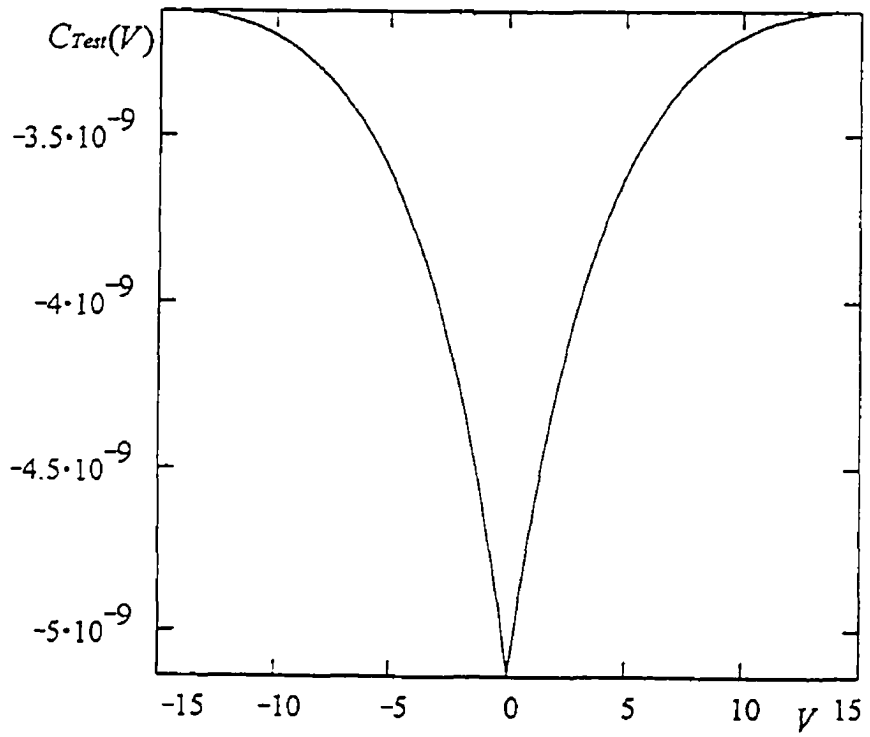


Figure 4.33 Computer simulation of a circuit model (Ch.3.4) in C-V when frequency=1MHz, and the differential resistance, R=100Ω, $C(V) = 4.417 \cdot 10^{-9} \exp(0.16\,|V|)$ F, $L(V) = 10^{-5} \cdot e^{-(0.01\cdot|V|)}$H,

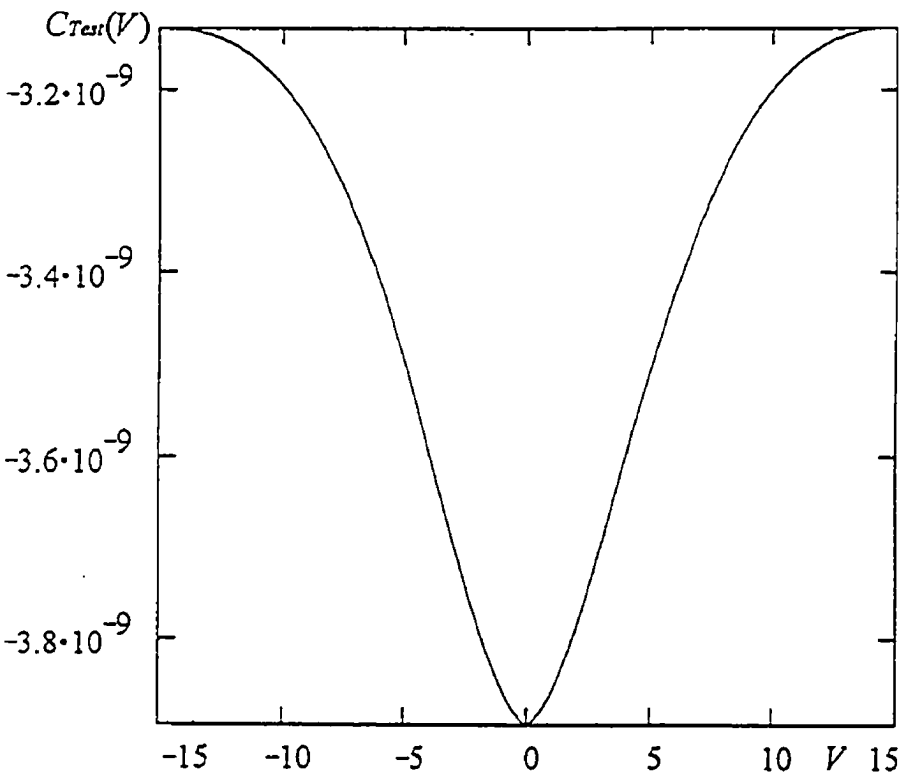


Figure 4.34 Computer simulation of a circuit model (Ch.3.4) in C-V when frequency=1MHz, and the differential resistance, R=45Ω, $C(V) = 4.417 \cdot 10^{-9} \exp(0.16\,|V|)$ F, $L(V) = 10^{-5} \cdot e^{-(0.01\,|V|)}$H

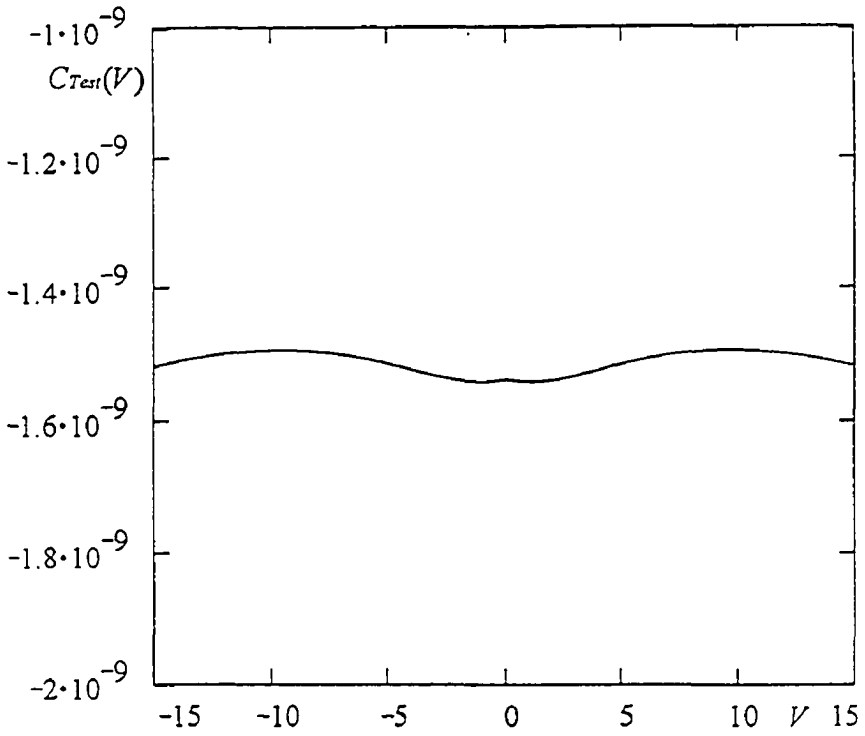


Figure 4.35 Computer simulation of a circuit model (Ch.3.4) in C-V when frequency=1MHz, and the differential resistance, R=45Ω, $C(V) = 4.417 \cdot 10^{-9} \exp(0.16\,|V|)$ F, $L(V) = 10^{-4.7} \cdot e^{-(0.01 \cdot |V|)}$H

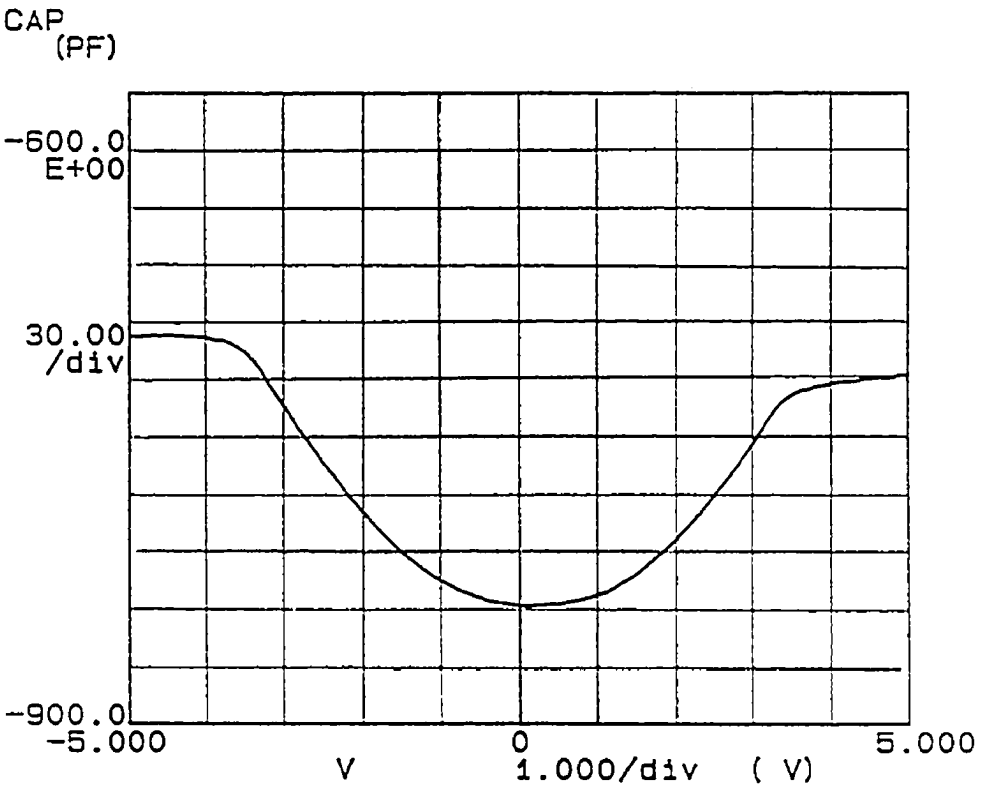


Figure 4.36 Negative capacitance of an amorphous SiC/c-Si diode. Inductance is 30μH near zero voltage

CHAPTER 5

SUMMARY OF RESULTS AND CONCLUSIONS

5.1 Summary of Results

A novel heterojunction diode, consisting of excimer laser-induced disordered Si on crystalline Si, was fabricated. A second type of heterojunction diode structure of non-hydrogenated amorphous SiC on crystalline Si was also fabricated. Both disordered Si and non-hydrogenated a-SiC are high resistivity, wide energy gap relaxation semiconductors. Compared to ordinary heterojunction diode structures, these heterojunction diodes have injection contacts on the relaxation semiconductors and Schottky barrier contacts on the c-Si.

Interesting negative capacitance effect, negative resistance, space charge limited current, and bistable switching with long term memory were observed in the electrical characteristics of I-V and C-V. The phenomena of negative capacitances were discovered in both heterojunction diodes from - 10v to 10v for the first time, and these phenomena were shown to have an inductive behavior by a HP-LCR analyzer. A theoretical model was developed to explain this phenomenon and it was compared experimentally. The possibility of using the negative capacitance effect to simulate inductance is proposed.

The excimer laser process was done at excitation voltages of 20 - 24kv with a pulse period of 0.1 - 1 second. The laser irradiated the c-Si surface before, as well as, after Al contact deposition by magnetron sputtering. With the irradiation of the c-Si surface, an injecting contact was made with the rough surface which results in a high surface recombination effect. A disordered Si was made due to the damage from the laser irradiation. The location of dopant impurity would be changed from a substitutional site to a interstitial site due to the laser irradiation, and this results

in a high resistivity disordered layer. AFM pictures, of the disordered Si surface, were taken. With the irradiation of the Al contact on the p-Si, laser induced Ohmic contact was also achieved with a thin p+ layer. During the localized heat treatment by the pulsed laser irradiation, the p-Si was dissolved in the Al up to its solubility, and the Al was diffused into Si. A metallurgical reaction between Al and p-Si led to the formation of a thin p+ layer near the interface and produced an Ohmic contact. A new theoretical model, to obtain the reduction of Schottky barrier height with this thin p+ layer, was proposed. Poisson's equation, Harrison tunneling theory, and WKB approximation were used to calculate a tunneling transmission probability and tunneling current under thermionic field emission. From the calculation of a minimum tunneling current, and the position of maximum tunneling distance, an effective reduced Schottky barrier was derived. Computer simulation with this model showed that, at least, a 4nm of p+ layer would be needed for a complete Ohmic (field emission) contact in Si with doping of $10^{18}/cm^3$. With strong laser irradiation (excitation voltage of 24kv, period of 1sec) on the Al contact, a high resistivity layer (20nm) was observed just below the p+ layer (8nm) by the C-V doping profile. Damage would be incurred during the rapid freeze portion of the alloying process with strong laser irradiation.

Excellent negative resistance phenomenon was observed, after the strong laser irradiation on the Al contacts, through the use of I-V measurements. The peak current was approximately 27mA at 1.4v and the slope in the negative resistance region was 79Ω. The reasons for the negative resistance were explained by the intrinsic and extrinsic properties. In the case of the intrinsic property, there would be a modification of the Si band structure due to the strained region that was induced by the laser irradiation. With the modified band structure, carriers would transfer from a lower valley, where carriers have high mobility and small effective mass, to an upper valley where carriers have low mobility and large

effective mass. This decrease of mobility will result in a negative resistance like that shown in GaAs. In case of the extrinsic property, the negative resistance would be related to the change of carrier density due to the carrier capture of the laser induced trap. The capture of an electron (hole), by a negatively (positively) charged impurity center, is strongly influenced by the presence of the potential barrier arising out of the Coulomb repulsion. Heating the carriers by an electric field will tend to increase the probability of tunneling through the barrier, and so increase the capture rate. The resultant fall of carrier density, as the field increases, will cause a bulk negative resistance.

Bistable switching, between a stable low-conductivity state and a stable high-conductivity state, which was maintained without bias for several months, was observed in both non-hydrogenated a-SiC/c-Si diodes and disordered Si/c-Si diodes. This switching phenomenon is believed to be governed by the presence of defects. The defects consist of intrinsic defects in the non-hydrogenated amorphous SiC, and disordered Si, as well as, extrinsic defects which come from lattice mismatch between the relaxation materials and c-Si. Carrier capture and release by the traps could be responsible for the switching. After a current pulse of 3mA for 1 second, a low-impedance state was immediately switched to a high-impedance state. Carriers would be captured by the filling of the traps. Carrier density was decreased, which resulted in a switching to the high-impedance state. In the memory condition of the switching, it seems necessary that the ionized traps be Coulombic repelling states, doubly negative charged before ionization and singly negative charged after, so that the barrier they present to the electrons prevents them from refilling immediately and eliminating the memory.

Very interesting negative capacitances were discovered from - 10v to 10v in both disordered Si/c-Si diodes and a-SiC/c-Si diodes through the use of the C-V measurements. This negative capacitance phenomenon was proved to be an

inductive behavior by a LCR Analyzer. These heterojunction diodes acted as inductance diodes. The C-V measurement of a real inductor also showed a negative capacitance in both biases. An inductive part of the heterojunction diode was derived theoretically using the relaxation theory and the Shockley theory. A circuit model of the diode was derived and it had good agreement with both the experiment of C-V and a LCR analyzer measurement and also with the computer simulation.

5.2 Conclusions

It was shown that it is possible to make a heterojunction diode structure that has small signal inductive behavior using a thin, less than 100nm, high resistivity region. One type inductive diode had a thin region of disordered Si made using an excimer laser. It was also demonstrated that an inductive diode behavior could be obtained with a thin layer of non-hydrogenated amorphous SiC made by LPCVD. In the device structure of both heterojunction diodes, an injecting contact was made on the relaxation semiconductor, and a Schottky barrier contact was made on the substrate, c-Si.

It was shown that a negative resistance, space charge limited current, and bistable switching with long term memory could be obtained with diodes having high resistivity regions. An interesting small signal negative capacitance effect was discovered by C-V measurement over the -10v to 10v bias range. This was the first reported measurement of negative capacitance for negative as well as positive bias. An inductive behavior was demonstrated with the negative capacitance effect using a LCR analyzer. In a disordered Si/c-Si heterojunction diode, a constant negative capacitance of 1520pF was observed from - 10v to 10v at 1MHz. The measured inductance value was approximately $5.5\mu H/mm^2$ at 1MHz. This inductance value was increased as $1/\omega^2$ from 1MHz to 30KHz. Compared to a

microstripline-inductor in MMIC (Monolithic Microwave Integrated Circuit), this inductance diode could have a large inductance per area (1mH/mm^2 at 30 KHz). The device concept could also be employed to make a inductor below microwave frequency range. Approximately 20% of the samples of the disordered Si/c-Si diodes showed this inductive dependence on frequency while 80% of the samples showed a constant inductance even with the variation of frequency. In an a-SiC/c-Si heterojunction diode a negative capacitance was also observed in both biases. The measured inductance value was 12μH/mm^2 above 3.5v and below - 3.5v and 10μH/mm^2 near zero bias at 1MHz. The inductance was almost constant between 1MHz and 30KHz.

A negative capacitance effect was observed in a $NiSi_2$-Si diode only above 0.48v at low temperature, 200K by Wu [7] in 1990. But, his charge delocalization theory can not explain negative capacitance obtained with both biases at room temperature for this research.

The small signal inductive behavior of this diode was shown to be possible theoretically using the dielectric relaxation theory of Roosbroeck. Requirements of the inductive behavior were τ_t (transit time) < τ_d (dielectric relaxation time), τ_o (lifetime) < τ_d and $\omega\tau_t < 1$. The derived inductance value was constant with changes in frequencies if $\omega\tau_d < 1$ and proportional to $1/\omega^2$ if $\omega\tau_d > 1$. This dependence of L on frequency was measured with a LCR analyzer. The theoretical results using a circuit model showed that the negative capacitance followed the relation of $|C_{test}| = 1/(\omega^2 L_{test})$. This relation had good agreement with the LCR analyzer measurement. Moreover, computer simulation of the circuit model also showed similar negative capacitance behavior.

It was concluded that effective inductive behavior is caused by conductivity modulation due to carrier injection in a thin relaxation semiconductor. In a circuit model, when the inductance is connected with a large series junction capacitance,

the current lagging effect is dominant. As a result, this inductive effect can be demonstrated by C-V measurements. It was also pointed out that the lifetime can be decreased by injecting excess carriers, with carrier delocalization due to carrier screening of impurity, into a low doped relaxation semiconductor. This would lead to a more pronounced relaxation behavior.

It is suggested that a novel heterojunction diode may be suitable for an inductor of Integrated Circuits and an better inductance diode can be made by optimum thickness control of the relaxation material with a large permittivity, high resistivity, and short lifetime. It is also suggested that when the heterojunction diode has its stable negative resistance property, a low loss inductance diode with very high quality factor can be achieved.

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