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ABSTRACT

A NOVEL READOUT METHOD FOR FOCAL PLANE ARRAY IMAGING IN THE PRESENCE OF LARGE DARK CURRENT

by
Changqing Qiu

This research was an investigation of a novel readout method for focal plane array (FPA) optical imaging, especially for very sensitive detectors with large dark current. The readout method is based on periodically blocking the optical input enabling the removal of the dark current integration from the output. The research demonstrated that it is feasible to modulate the optical input with the designed readout circuit and thus achieve longer signal integration time to enhance the signal-to-noise ratio.

Study of a proposed circuit model showed that in theory the correlated readout method could increase the output voltage swing and reduce the noise level by attenuating low frequency noise, thereby effectively improving the FPA dynamic range. Circuits based on standard CMOS circuitry were designed, simulated by PSpice, fabricated using Orbit 2μm n-well technology, and tested with a PI-4000 system. In the circuit evaluation, the output noise due to the clock switching phenomena, the gate signal feedthrough and the charge relaxation, was considered to be the critical problem. The most promising design for minimizing this problem had a CMOS current steering circuit at the input of a high CMRR operational amplifier. Simulation and test results showed that a modified capacitive transimpedance amplifier (CTIA) could subtract dark current output and reduce the output signal due to any difference between the frequencies of the optical input modulation signal and the switch modulation signal. In conclusion, the correlated readout circuit was shown to be a promising approach for advancing FPA technology.

A NOVEL READOUT METHOD FOR FOCAL PLANE ARRAY IMAGING IN THE PRESENCE OF LARGE DARK CURRENT

by
Changqing Qiu

A Dissertation
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy

Department of Electrical and Computer Engineering

January 1999

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To my parents, my wife and
my daughter Shela

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CHAPTER 1

INTRODUCTION

Infrared sensors are used to detect, measure and image the thermal radiation emitted by all objects. The possibility of mass fabrication of two-dimensional arrays, based on advances in photolithography, increased the possible application areas and performance of infrared focal plane array (FPA) [1]. Further advances will be accelerated by higher pixel density, the capability to do on-chip processing, improved materials with lower cooling requirements, and higher sensitivity. However, some FPA performance limitations can be traced to the readout electronics rather than the detectors [2], [3].

This research investigated the feasibility of a novel readout concept recently proposed for FPA optical imaging. The method discriminates against background noise due to various dark current sources and is especially useful for very sensitive detectors with large dark current. Named correlated readout, the method is based on periodically blocking the optical input enabling the subtraction of the output component of the current integration due to dark current sources such as large background photon noise that irradiates the detector circuitry and electron motion fluctuations inherent in the FPA components. State-of-the-art readout circuits developed from mature hybrid readout circuits were selected and redesigned for this research. The modified circuits were both simulated and experimentally tested. The results showed that it is feasible to modulate an optical input with the designed readout electronics and thus achieve longer signal integration time to enhance the FPA signal-to-noise ratio. The results of the thesis will be useful for long wavelength infrared (LWIR) sensing applications and particularly for

special scientific measurements, such as solar magnetography where large background is present.

Since the 1940's, photon detectors have been extensively developed. Because of their fast response time, high sensitivity and the ease of fabricating the required large 2D arrays in semiconductors, photon detectors, especially photovoltaic (PV) detectors, are expected to be used in almost all advanced infrared FPA systems. Many materials and detector structures are being developed to cover all the spectral bands, such as extrinsic silicon and germanium, Schottky-barrier photoemissive junctions, III-V, $Hg_{1-x}Cd_xTe$, IV-IV and multi-quantum well detector arrays [4]. The applications of the monolithic, hybrid, and monolithic heterostructure FPAs using these materials can be found in astronomy, military, environmental monitoring, law enforcement, and many other scientific research and surveillance purposes [5]. Unfortunately, photon and thermal noise sources limit the applications of infrared photon detectors. For long wavelength detection, such as the wavelength window 8 to 14μm (LWIR) and 14 to 30μm (VLWIR), background flux may become much stronger than signal flux because of black body radiation from the ambient. In detection at relatively high temperatures, such as 77°K (maintained by liquid nitrogen), 105°K (obtained in space by passive radiation cooling), and even room temperature, a detector's R_oA will be decreased drastically for all the materials mentioned above [6]. In addition, the large background problem exists in other imaging applications where wavelength and temperature are not particularly important. For example, in the measurements for solar magnetograph, the signal is the difference of two circularly polarized light sources and the background is one of the primary sources. Due to the effect of Zeeman splitting this primary source can be 4 orders as high as the

real signal [7]. All these detection conditions pose an important question: How does one read out the image signal in the presence of large background noise.

To design a FPA for working in the presence of large background noise which results in a large dark current, saturation of the image storage capacitors must be given primary consideration. Saturation would limit the signal integration time so that the array's signal-to-noise ratio will not be enough to reveal the image. This is because a FPA has very limited charge handling capacity [8], especially in 2D arrays. A large capacitor in each pixel is not only restricted by available real estate; it will also contribute a large reset noise that should be eliminated in the design. At the FPA level, the dynamic range, which is defined as the ratio of the maximum achievable output voltage swing to the output noise level of the imager, can be the most important device characteristic [9]. An ideal readout method would be one that both can increase the signal output voltage swing and reduce the noise level. This was the major goal of this research.

If there is not a breakthrough in detector materials or FPA architecture, conventional imaging methods will not solve the problem in the applications mentioned above, although second-generation FPA with hybridized readout electronics promise significantly higher performance and design flexibility [10-13]. Imaging an object in the presence of large dark current with a modulated source has been proposed recently [14]. The readout method developed in this thesis is the first to realize this new imaging approach [15]. The basic principle of this method is to demodulate the photon signal by charging the signal integration capacitor in one modulation phase and discharging the capacitor in the following phase to remove dark current signal. By processing the current from the detector in this way, it was shown that the correlated readout approach could

significantly subtract dark current integration and attenuate its associated noise. This results in an increase in the dynamic range and signal-to-noise ratio of the FPA.

In the next chapter, the hybrid readout method, which represents the state-of-the-art of readout electronics, will be reviewed. Some newly proposed research will also be discussed. In chapter 3, the correlated readout method is presented, including the methodology, signal processing model and circuit implementation. The principle of phase sensitive detection is described to illustrate the noise reduction capability of the method. The possible application to the measurement of solar magnetograph and other imaging applications are also presented in this chapter. Chapter 4 discusses the design of correlated readout circuits using the standard CMOS process. Switching signal feedthrough is addressed as a serious problem in the correlated readout circuit design. For developing readout circuits based on the capacitive transimpedance amplifier concept a higher than normal common-mode rejection ratio of the operational amplifier is required. Finally, the design of a 16 by 16 silicon imager for the experimental study of this thesis is presented. The test chip was designed and fabricated by using Orbit 2μm n-well technology through MOSIS. Chapter 5 presents test results for the chip. The experimental methodology is discussed first, followed by a description of the test equipment. The experiments tested the correlated function, the frequency response and the switching feedthrough. The conclusions for the thesis are given in chapter 6. It was concluded that the correlated readout circuit is a promising approach for advancing FPA technology.

CHAPTER 2

A REVIEW OF INFRARED READOUT ELECTRONICS

2.1 Introduction

Historically, the development of infrared sensors has concentrated on the growth, fabrication, measurement and optimization of IR materials and detectors. First-generation devices are fundamentally a monolithic FPA, which consists of a detector array, and the readout multiplexer integrated on the same substrate. Most of the readout techniques and device architectures were originally introduced from visible silicon imagers, such as charge coupled device (CCD) and charge injection device (CID) [16].

With the advancement in microlithography feature size reduction and the requirements of increased array size and performances, hybrid IR FPAs have developed rapidly in recent years. These second-generation FPA typically consists of a detector array chip bump-bonded on a silicon readout multiplexer. Because it allows independent optimization of the detector array and the readout, hybridized readout electronics that perform the function of detector interface, signal processing, and video multiplexing, represents the state-of-the-art for IR FPA readout technology.

Early hybrid readouts were still either CIDs or CCDs because of their success in visible imaging applications. With the Active Pixel Sensor (APS) technology stepping into the stage of scientific image acquisition [17], [18], x-y arrays addressed MOSFET switches, or direct readout (DRO) FET arrays, start to dominate today's infrared readout electronics for reasons of yield, design flexibility, and simplified interface. The APS concept is expressed as: One or more active transistors are integrated into the pixel of an

imaging detector array, and buffer the photo signal as well as drive the readout lines. The DRO architecture consists of an array of FET switches. The basic multiplexer has several source follower stages that are separated at the cell, row, and column levels by MOSFET switches which are enable and disable to perform pixel access, reset, and multiplexing (Figure 2.1).

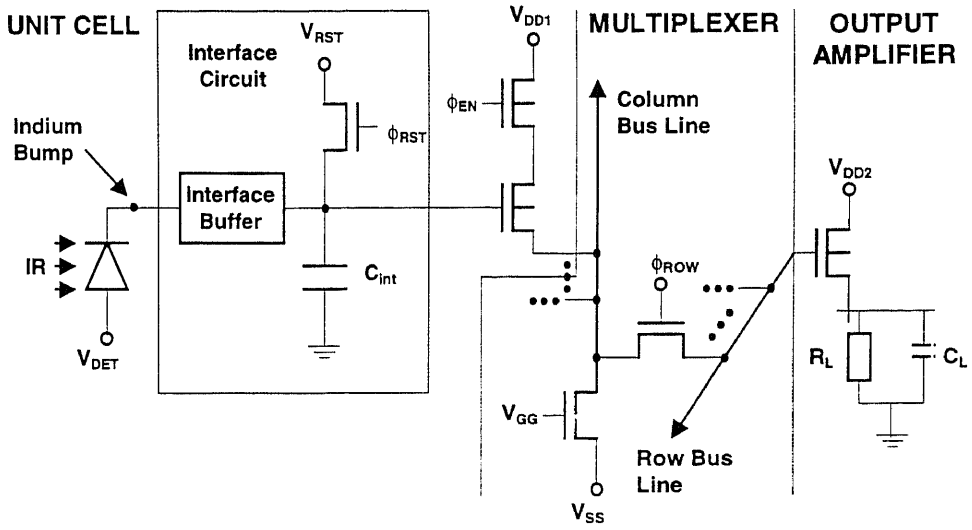


Figure 2.1 Direct readout (DRO) architecture consists of an array of switches and detector interface circuits.

This review will concentrate on various readout methods with DRO schematic, which represent today's IR readout technology. It is well know that currently matured circuits are source follower per detector (SFD) [19], buffered direct injection (BDI) [20], gate modulation [21], and capacitive transimpedance amplifier (CTIA) [22], while many other methods are still in the conceptual stages. New proposed research on background suppression will be described in a separate section. The noise process is specially discussed, since noise figure is an important issue of focal plane array and signal-to-noise-ratio (SNR) is the prime design driver in most sensor systems. The important

conclusion is that it is the time to trade circuitry complexity with other performance characteristics. However, the existing readout methods will have difficulties to succeed for the detection conditions considered by this thesis research.

2.2 Matured Hybrid Readout Circuits

The general requirements of infrared FPAs fall into broad categories of array size, pixel pitch, charge handling capacity, integration time, noise, dynamic range, readout rate, operating temperature, power dissipation, radiation hardness, and detector bias control. Although many circuits can be used for interfacing discrete photon detectors, only a few have been successfully applied in FPA readout circuits, and the following four methods are matured so far.

2.2.1 Self-Integration Readout

To integrate charges on detector itself is a most commonly used design where the charge accumulation element is a capacitor or a CCD. Usually, this method is referred as direct detector integration (DDI), or source follower per detector (SFD) in active pixel sensor technology. The simple unit cell electronics still makes self-integration readout attractive because of the achievable small cell area and low power dissipation, although it can only be applied in low background detection.

Figure 2.2 is a most simple photodiode DDI/SFD circuit with the illustration of detection principle. When the reset MOSFET is pulsed on, the photodiode capacitor, along with the sense node stray capacitor, will be charged from reset voltage (V_{RST}) through its drain-to-source channel resistance, to approach the voltage level of V_{RST} - V_T,

where V_T is the MOSFET threshold voltage for channel formation. Photo-generated minority carriers, together with the thermally generated minority carriers, will diffuse and drift across the PN junction to result in a current flow of $I_{photo} + I_{dark}$ which acts to discharge the capacitor C. If the MOSFET is kept off for a time t_{OFF}, the change of the stored charge ΔQ at the end of this time period will be given by the time integral of the combination of the photocurret I_{photo}, the dark current I_{dark}, and the MOSFET leakage current $I_{DS(OFF)}$:

$$\Delta Q = \int_0^{tOFF} (I_{photo} + I_{dark} + I_{DS(OFF)})dt \,. \tag{2.1}$$

The corresponding change in the voltage across the sense node will be $\Delta V = \Delta Q/C$. The voltage is buffered by the source-follower MOSFET and then multiplexed to a common bus prior to the video output amplifier.

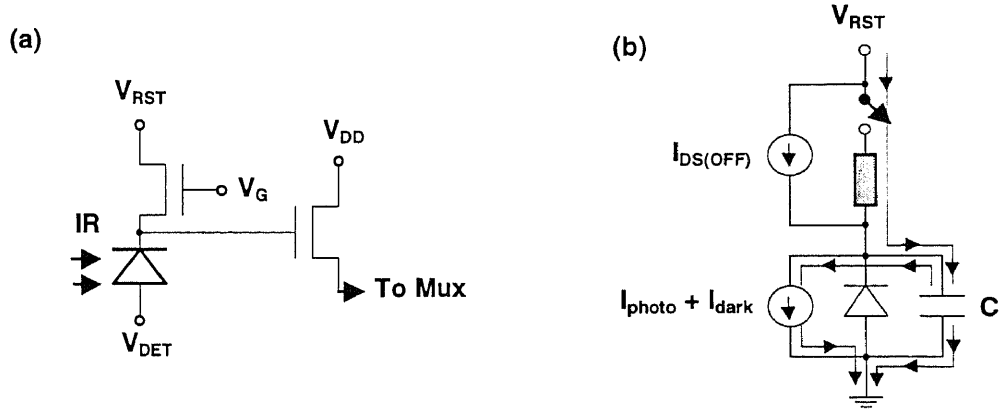


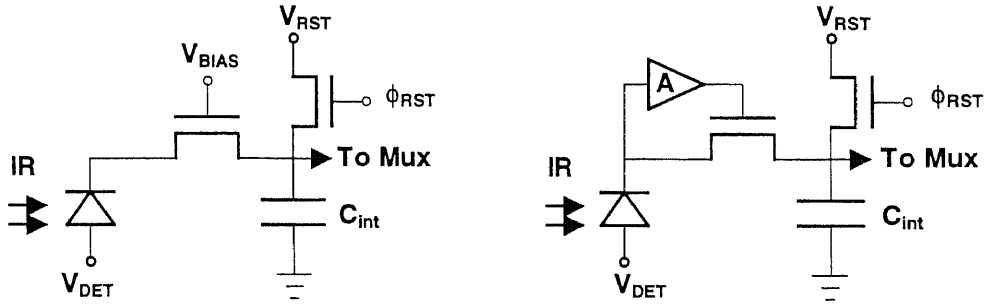
Figure 2.2 Topology of direct detector integration (DDI) and source follower per detector (SFD): (a) simplest circuit schematic, and (b) principle of signal detection.

DDI/SFD topology is particularly susceptible to 1/f noise. This is due to the fact that the time period for which the source-follower transistor turns on during multiplexing is longer than the response time of the source-follower. This effect enhances the low frequency noise contribution, and limits the utilization of an integration capacitor for long

time integration applications. For noise figure consideration, it was concluded that the optimum sense node capacitance other than the detector capacitance occurs at the point where it is equal to the detector capacitance [3].

2.2.2 Injection Circuits

Instead of resetting the detector node directly, injection circuits accumulate charges on a separate integration capacitor C_{int}, and periodically reset the capacitor. Two popular injection circuits, direct injection (DI) and buffered direct injection (BDI), are shown in Figure 2.3. The direct injection circuit typically consists of an integration capacitor, an injection transistor, a reset transistor, and an output selection transistor (not shown in the figure). It is a widely used interface circuit because of its simplicity and high performance. The detector directly modulates the source of a MOSFET, and the photo-generated current directly couples into the storage capacitor for charge integration. This requires that detectors with N-on-P polarity interface N-type FETs (and vice versa) for carrier collection in the capacitor.



(a) Direct Injection (b) Buffered Direct Injection

Figure 2.3 Schematic of injection circuits.

An important issue of using an integration capacitor is injection efficiency η_{inj}, which represents the percentage of detector generated current that can be stored. It may

vary across an FPA due to FET threshold, detector bias, and detector resistance non-uniformity. For DI circuit, the injection efficiency is calculated as [1]

$$\eta_{inj,DI} = \frac{g_m R_{det}}{1+g_m R_{det}} \left[\frac{1}{1+\frac{j\omega C_{det} R_{det}}{1+g_m R_{det}}} \right], \tag{2.2}$$

where R_{det} and C_{det} are the detectors' dynamic resistance and capacitance, respectively, and g_m is the transconductance of the injection FET.

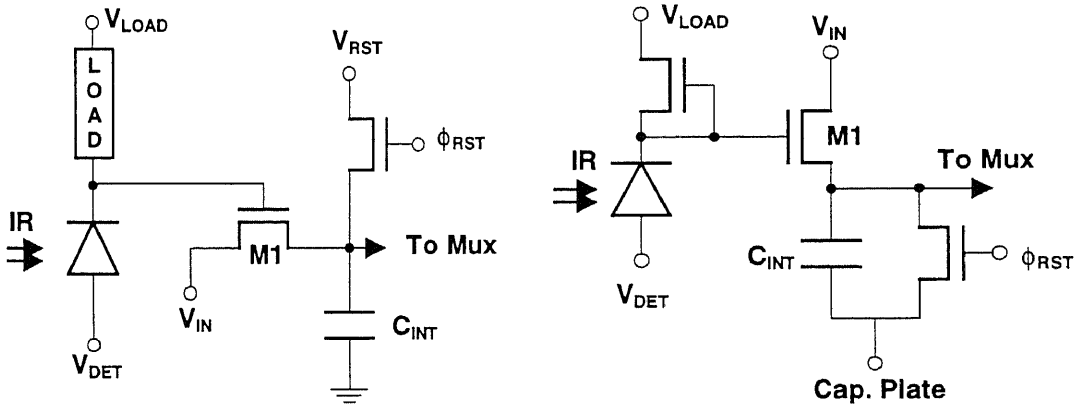
The advantage of using the integration capacitor is to increase the integration time so that the signal-to-noise ratio will be improved. However, poor injection efficiency makes the MOSFET noise a serious problem. One approach to improve the direct injection current is to use buffered direct injection (BDI) configuration as shown in Figure 2.3b. The detector is connected to both the input diffusion and the input of a feedback amplifier with open-loop gain $-A_v$. The effective g_m is increased by a factor of $(1+A_v)$ and the injection efficiency becomes

$$\eta_{inj} \cong \frac{g_m R_{det}(1+A_v)}{1+g_m R_{det}(1+A_v)+j\omega R_{det}[(1+A_v)C_{amp}+C_{det}]}, \tag{2.3}$$

where C_{amp} is the Miller capacitance of the amplifier. Apart from an improvement in the injection efficiency, the inverting gain in BDI also yields better control over the detector bias at different photocurrent levels and helps to reduce the saturation frequency compared with DI circuit, thereby allowing longer integration time. In spite of these improvements, BDI still shares the same limitation with DI in terms of low background applications. Another common drawback of injection circuits is a frame-to-frame crosstalk, since the detector is not directly reset; residual photon-induced charge from one frame time can be integrated into the next frame time.

2.2.3 Gate Modulation

Gate modulation circuits utilize photon current to modulate the gate voltage of an input MOSFET and then induce an output current in the transistor. The principle of gate modulation input (GMI) structure is shown in Figure 2.4. The detector current, including photon current and dark current, flows through the load device. A gain-proportioned current flows into the integration capacitor from the input MOSFET (M1). The gain and dc level are adjusted by varying the source voltage V_{IN} of the input MOSFET and setting the detector bias via V_{DET}, so that the output is in proportion to the ac component of the signal. Good injection efficiency of the ac signal requires a high value of detector resistance with a greater load resistance value. Thereby, active load gate modulation, with a current mirror configuration, is often used in modern GMI design.



(a) Passive load approach (b) Active load approach

Figure 2.4 Gate modulation input structure.

In GMI circuits, the differential gate voltage applied to the input FET varies for a change in photon current (ΔI_{photo}) as

$$\Delta V_G = R_{LOAD}\eta_{inj,DI}\Delta I_{photo}\,. \tag{2.4}$$

The current injected into the integration capacitor is

$$I_{input} = g_m R_{LOAD} \eta_{inj,DI} \Delta I_{photo} \cdot \tag{2.5}$$

The ratio of I_{input} to I_{photo} is the current gain, A_I, which is

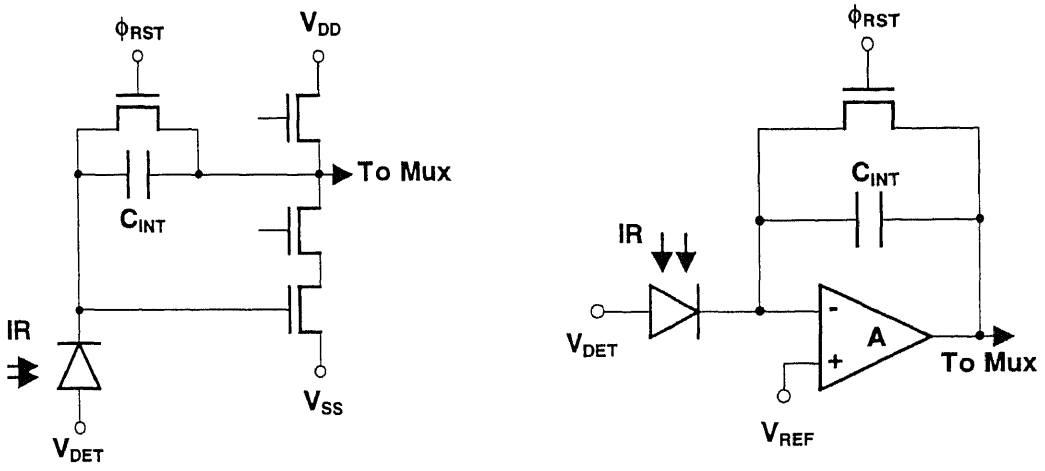
$$A_I = \frac{g_m}{g_{m,LOAD}} \eta_{inj,DI} \cdot \tag{2.6}$$

The current gain, expressed by equation 2.6, can self-adjust depending upon the background flux by orders of magnitude. It also allows GMI to operate with a large integration capacitor compared to injection circuits, and still obtains low noise performance and high charge sensitivity. These features indicate its capability of background suppression, which leads to higher dynamic range. Unfortunately, gate modulation is only successfully applied to the detection condition when signal radiation is stronger than the background. The major problem comes from the requirement of detector bias reset as scene-induced current changes. To stabilize detector bias by using large reverse bias causes large 1/f noise and dark current non-uniformity. In addition, since the MOSFETs in gate modulation are normally operation in weak inversion, the threshold variations of the transistors become a more serious problem than injection circuits. Also from the current gain expression, GMI has a potential shortcoming for imaging application because the transfer characteristic is nonlinear, particularly when the current in the load and input FETs differ drastically.

2.2.4 Capacitive Transimpedance Amplifier

Capacitive transimpedance amplifier (CTIA) is a near ideal circuit for coupling an IR detector to a multiplexer. It consists of an inverting amplifier with a gain of A, an integration capacitor C_{int} placed in a feedback loop, and a reset transistor in parallel with the integration capacitor, as shown in Figure 2.5. The amplifier in the circuit can be a

simple CMOS inverter as feedback amplification (Figure 2.5a), or a more elaborated differential amplifier (Figure 2.5b). The choice of the approach depends on the requirement of open-loop gain, bandwidth, power dissipation, and cell real estate.



(a) Inverter approach (b) Differential Amplifier approach

Figure 2.5 Circuit schematic of CTIA.

In interfacing by the CTIA, when photon charge causes a slight change in voltage on the inverting input node of the amplifier, the amplifier, with open-loop gain in the hundreds to tens of thousands, responds with a sharp reduction in output voltage. This change in output is coupled back to the input node through the feedback capacitor, causing photon-induced charge to flow onto the feedback capacitor and oppose the initial effects of charge on the input node. At the end of integration process, the output voltage is sampled and multiplexed to the output video drivers, and the switch across the feedback capacitor is pulsed to reset. The CTIA gain, assuming a large open loop amplifier gain, is

$$V_{out} = \frac{I_{ph} T_{\text{int}}}{C_{fb}} \text{ [V]}, \tag{2.7}$$

where C_{fb} is the feedback capacitor and the CTIA transimpedance is often expressed over a single frame of data as

$$Z_t = \frac{V_{out}}{I_{ph}} = \frac{T_{\text{int}}}{C_{fb}} \text{ [V/A]}. \tag{2.8}$$

The CTIA allows extremely small current to be integrated with high injection efficiency. It also can provide a highly stable detector bias, high gain and low noise, and ensure that the detector with low resistance can function as a current source if a well-designed differential amplifier is used. A recent report showed that the CTIA had the best overall performance characteristics compared to other readout methods at low backgrounds by state-of-the-art CMOS submicron technology [22]. Its attractiveness will continue to increase in the future.

2.3 Noise in Hybrid Infrared FPA

Like all the other imaging systems, the noise sources in infrared FPAs have two general forms: temporal and spatial (or pattern) noise. Temporal noise is characterized by collecting sequential samples for each detector channel and calculating standard deviations and power spectral densities. Typical mechanisms found in FPA technology literature includes detector thermal noise, shot noise, readout noise, and flicker (1/f) noise. The measurement of pattern noise is more difficult. It requires accurate and uniform calibration sources, and often needs very long laboratory time. Therefore pattern noise has received much less attention in the literature. In most time this issue has been left to post image processing. In this section, the noise sources inside the array are reviewed in detail since large dark current is considered as the major problem for this thesis research, while many other noise sources are considered as trivial.

2.3.1 System Characterization

An imaging system can be considered as ideal elements with the noise introduced at appropriate locations. Figure 2.6 illustrates the noise transfer diagram. The total FPA noise consists of unit cell detector and electronic noise, and downstream noise contributed by the multiplexer and the driver.

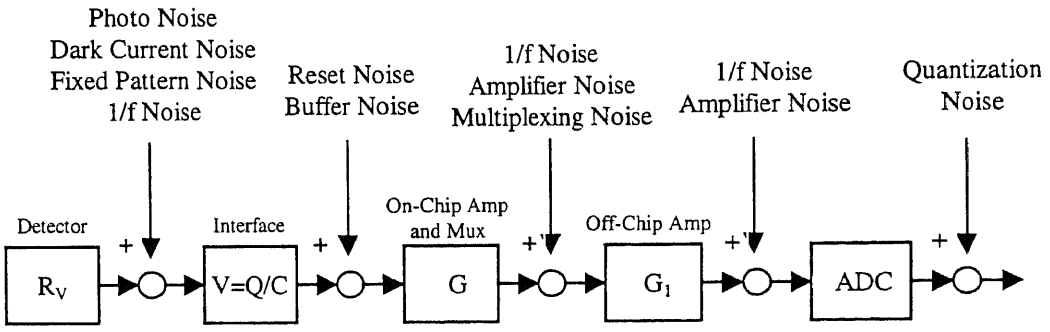


Figure 2.6 Noise transfer diagram for an imaging system.

For single detector, specific detectivity (D*) and noise equivalent power (NEP) offer the noise figure. D* is the signal-to-noise ratio normalized to the electrical bandwidth and detector area. It is simply the reciprocal of the normalized NEP and has units cm-Hz/W (or Jones):

$$D^* = \frac{1}{NEP}(cm - \sqrt{Hz}\,/\,W) \tag{2.9}$$

D* and NEP are useful specifications for finding detection limitation. At the FPA level, however, they are difficult to relate to system performance. The best description for temporal noise of a photovoltaic hybrid FPA is in terms of noise equivalent irradiance (NEI) in photons/cm^2-s, which is described as FPA output noise normalized to responsivity:

$$NEI = V_n / R_v, \tag{2.10}$$

where V_n is FPA total noise at operating background (in volts) and R_v is the responsivity in V/(photons/cm^2-s):

$$R_v = \eta_m A_{opt} e \eta_{inj} T_{int} G_{elc} N_{TDI} / C_s, \tag{2.11}$$

where η_m is the mean quantum efficiency, A_{opt} the detector optical area, e the electronic charge, η_{inj} the circuit injection efficiency, T_{int} the integration time, C_s the effective sense node capacitance, G_{elc} electronic gain past the sense node, and N_{TDI} is the number of time delay integration (TDI) stages.

For thermal imaging of the object temperature distribution, NEI is related to noise equivalent temperature difference (NEΔT) by the relation

$$NE\Delta T = \frac{NEI}{\tau_{opt} \Omega_t \partial R_{ap}(T) / \partial T}, \tag{2.12}$$

where τ_{opt} is optical system transmission, Ω_t is the projected solid angle of the telescope clear aperture with respect to the detector array, and $\partial R_{ap}(T)/\partial T$ is the temperature derivative of the in-band source radiance, projected to the sensor aperture for a source temperature T. The detailed calculation can be found in reference [23].

NEI, along with NEΔT, can give a good point of view for the consideration of temporal noise of the FPA. However, since the final output is an image, the ultimate figure of merit for an infrared imaging system should be how well the objects of varying size are resolved in the displayed image. The minimum resolvable temperature (MRT), which is a function of spatial resolution and is defined as the signal-to-noise ratio required for an observer to resolve a series of standard four-bar targets, is thus considered as a key specification for infrared FPA [1]. The inconvenience to follow MRT is that it can not be applied until the imaging system is really developed.

2.3.2 The Dark Current Noise

Among the three types of noise in the photodetector, the dark current induced shot noise usually gives its limit of detection sensitivity. In most literature, the dark current is only used to describe the detector current in the dark. However, from a technical point of view, the dark current should be considered as the current inside a detector before it is exposed to a scene. Thus, the response to background radiation on the detector site should be counted as an important part of the dark current. As is well known, environment illumination can be very strong for LWIR because black body radiation peaks at 10 μm for room temperature. Therefore, the following definition is used in this thesis:

The dark current = The detector dark current + The background photo current.

The detector dark current is the superposition of current contributions from three diode regions: bulk, depletion region and surface. The physical mechanisms include [5]:

1. Thermally generated current in the bulk and depletion region

- diffusion current in the bulk P and N region,
- generation-recombination current in the depletion region,
- band-to-band tunneling,
- intertrap and trap-to-band tunneling,
- anomalous avalanche current,
- ohmic leakage across the depletion region.

2. Surface leakage current

- surface generation current from surface states,
- generation current in a field-induced surface depletion region,]
- tunneling induced near the surface,

- ohmic or nonohmic shunt leakage,
- avalanche multiplication in a field-induced surface region.

For an ideal diode exposed to background flux density ϕ_b, the dark current is the combination of thermal and shot noise, and can be expressed by [4]

$$i_n^2 = 2q[\frac{kT}{qR_0} + \frac{kT}{qR_0}\exp(\frac{qV}{kT}) + q\eta A\Phi_b]\Delta f\ , \tag{2.13}$$

where k is Boltzmann constant, T absolute temperature, q the charge of electron, V bias voltage, Δf electronics bandwidth, η quantum efficiency, A the area of the diode, and R_0 the dark resistance which is defined as

$$R_0 = (\frac{dI}{dV})^{-1}_{|v=0}, \tag{2.14}$$

where I is the dark current and V is the diode's bias voltage. Background photo flux ϕ_b can be expressed by

$$\Phi_b = \frac{\Omega}{\pi}\int_0^{\lambda_c} \frac{2\pi c}{\lambda^4[\exp(hc/\lambda kT) - 1]}d\lambda \tag{2.15}$$

where Ω is the field of view in radians of the detector and λ_c is the cutoff wavelength.

For the FPA working at short (1 to 3 μm) and medium (3 to 5 μm) wavelengths, the dark current noise is generally small compared to readout electronic noise, and usually is not considered in the readout circuit design. However, for the detection at LWIR and high temperature, the detection may reach two important limitations:

- background limited performance; if $4kT/RoA << 2q^2\eta\Phi_b$, then

$$D^*_{BLIP} = \frac{(A\Delta f)^{1/2}}{P_{NEP}} = \frac{\lambda}{hc}(\frac{\eta}{2\Phi_b})^{1/2}; \tag{2.16}$$

- thermal noise limited performance; if $4kT/RoA >> 2q^2\eta\Phi_b$, then

$$D^* = \frac{\eta\lambda q}{2hc}\left(\frac{R_o A}{kT}\right)^{1/2}. \tag{2.17}$$

The dark current results in fixed pattern noise (FPN). The fixed pattern noise is the variation from pixel to pixel in the camera display, but does not vary from frame to frame. It is primarily due to the dark current differences, which is caused by the differences in detector size, doping density, and foreign matter getting trapped during fabrication. Usually, it can be compensated by post imaging processing. But it may arise again because the calibration and equalization models cannot adequately model actual response, or the drift of the channels is beyond the capability of practical recalibration schemes.

The 1/f (flicker) noise level in photovoltaic detector is believed to be proportional to dark current [23], although it is also alias with biasing provided by input circuit or come from readout circuits. Whatever the source of 1/f noise in a detector or readout channel, the result is time varying offset drift. It is very nonuniform within a single chip for some narrow-bandgap detector materials. The issues in 1/f noise tend to be difficult because little theoretical basis exists for its rigorous definition. The dependency of 1/f noise with dark current indicates a background-driven 1/f drift, a less tractable process.

2.3.3 Readout Noise

Readout noise is usually referred as noise floor. It may include multiplexer and timing effects, reset noise, amplifier 1/f noise, and circuits nonlinearities. With the same readout architecture, the main difference for different readout method will be the noise of the interface circuit, while the reset noise may only related with storage capacitance no matter what kind of methods is used.

Reset noise (commonly referred as KTC noise) is thermal noise stored on the capacitor at the moment the switch is closed. The same as in any resistor-capacitor circuit with a resistance R_{on} and capacitance C, the rms noise on the capacitor can be calculated by integrating the thermal noise of the resistor over all frequencies through the transfer function of the RC circuit, and expressed as

$$v_c^2 = 4KTR_{on}\int_0^{\infty}\frac{1}{1+(2\pi fCR_{on})^2}df \quad [V^2]. \qquad [2.18]$$

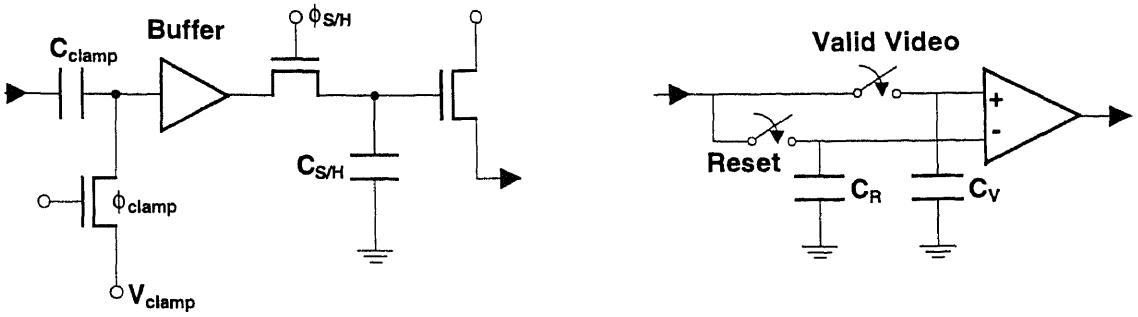
Equation 2.18 can be rewritten as

$$v_c = [4KTR_{on}\frac{\pi}{2}f(-3dB)]^{1/2} = (\frac{KT}{C})^{1/2} \quad [\text{volts rms}]. \qquad [2.19]$$

The expression in terms of the noise charge stored on the capacitor is

$$q_C = (KTC)^{1/2} \quad [C]. \qquad [2.20]$$

The reset noise, along with some of 1/f noise and fixed pattern noise, can be reduced via correlated double sampling (CDS). CDS may be performed by a clamping circuit with a delay line processor (Figure 2.7a), or by a differential sampling circuit illustrated in Figure 2.7b. The principle of CDS is based on correlation technique. The assumption is that the same voltage fluctuations will present on both video and reset levels. That is, the reset and video signals are correlated in that both have the same fluctuation. The performance of the CDS circuit depends on the product of the correlation time which is defined as the time interval between the two data samples, and the output amplifier cut-off frequency. Therefore, the 1/f noise reduction potential is somewhat limited, especially when the integration time is long, while the data rate is high.



(a) Clamping and delay approach (b) Differential sampling approach

Figure 2.7 Correlated double sampling circuitry: (a) clamping and delay line processor; (b) differential sampling approach.

To improve the 1/f noise reduction, a modified CDS is often used. In the modified CDS circuit [24], two sets of closely spaced double samples are collected as shown in Figure 2.8. Prior to photocurrent integration, the reset noise and the offset is measured by computing the difference between the reset level before and after the reset transistor is shut off. The signal is measured at the end of the integration period by computing the difference between the data level before and after the unit cell is reset:

$$V_{mcds} = V_1 - V_2 + V_3 - V_4 . \tag{2.21}$$

As can be seen from Figure 2.8, the conventional CDS simply samples V_2 and V_3, and has the output of (V_2 - V_3).

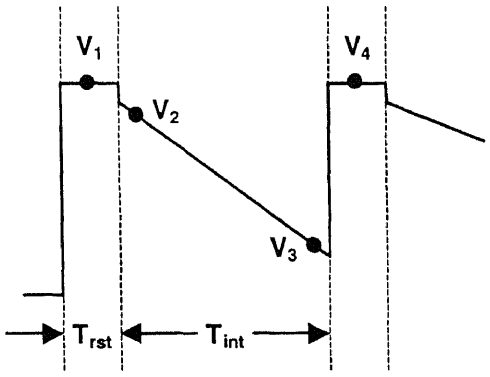


Figure 2.8 Schematic showing modified CDS readout data construction.

After the sense node is reset to a fixed level, photocurrent is integrated on the capacitor. The voltage generated is expected to be linear with time under constant illumination. However, due to the circuit transimpedance and charge injection efficiency, combined with the integration capacitor and detector parameters, a voltage deviation will appear at the sense node. This circuit noise may be modeled by Laplace-domain small signal analysis, in which electrical transfer functions are determined for each component in the signal chain. Noise sources can be described by power spectral densities, and its propagation is described by transfer functions [25]. A more widely used technique of circuit noise analysis is to study input-referred circuit noise. The results for various readout circuits can be found in reference [1], and some of them are listed in Table 2.1.

Table 2.1 Input-referred circuit noise in mature readout circuits

Input Circuit	Input-referred Circuit Noise
Direct Detector Integration	$N_{sf} = \frac{\sqrt{2}}{S_v}[\int^{\Delta f} V_n^2(f)\frac{(1-\cos 2\pi ft)}{[1+(2\pi fT_D)]}df]^{1/2}$
Direct Injection	$\sigma^2_{input,ir} = \int[\frac{1+\omega^2 C_{det}^2 R_{det}^2}{g_m^2 R_{det}^2}(\frac{8}{3}kTg_m + \frac{K_{FET}}{f^\alpha})]df$
Buffered Direct Injection	$\sigma^2_{input} = \int^{\Delta f}[\eta^2_{noise}(\frac{8}{3}kTg_m + \frac{K_{FET}}{f^\alpha}) + \Lambda^2_{amp}\langle e^2_{amp}\rangle]df$
Gate Modulation	$\sigma^2_{input.ir} = \int^{\Delta f}\frac{1}{A_I^2}(2qI_{input} + \frac{K_{FET,input}}{f^\alpha})]df$
Capacitive Transimpedance Amplifier	$N_{amp,1/f} \approx \frac{C_{det}K_{amp}\sqrt{2}}{q}[\ln\frac{5\tau_{int}}{\tau_{amp}}]$ $N_{amp,white} \approx \frac{C_{det}}{q}\sqrt{\frac{8}{3}\frac{kT}{g_m\tau_{amp}\pi}}$

The amplifiers exhibit 1/f noise because they are formed from MOSFETs. If an operational amplifier is designed as the amplifier, the input offset voltage due primarily to device and bias mismatches in the input stage would be another noise source. To

enlarge MOSFET gate area by using MOS input transistors in the lateral bipolar mode is one approach to reduce 1/f noise. The mismatch will also be reduced by increasing the input stage device geometry and size. If circuit real estate is available, chopper stabilization can be applied to reduce amplifier 1/f noise and correct the input offset voltage [26]. A simplified schematic of a chopper stabilized buffered direct injection design is shown in Figure 2.9 [27]. The chopping process shifts the amplifier's operating frequency to higher frequencies where the amplifier's noise is governed by white noise, not 1/f noise. Since the amplifier becomes ac coupled, the dc-offset components are removed and the amplifier is zero referenced. After amplification of the chopped or modulated signal, synchronous demodulation is applied to return the signal of interest to its original spectrum.

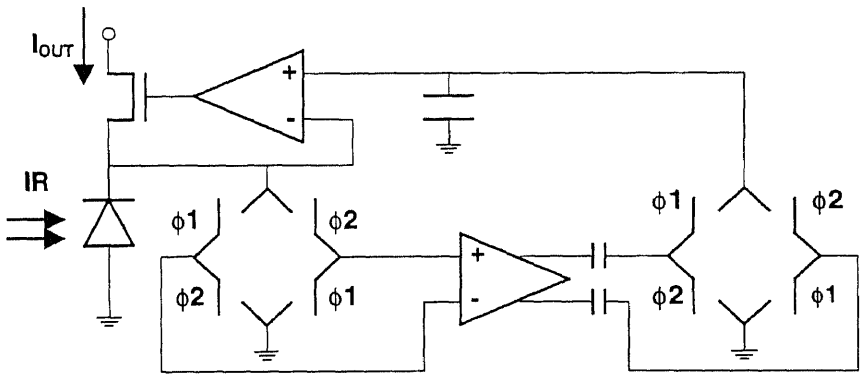


Figure 2.9 Buffered direct injection circuit using chopper stabilization to reduce detector bias offsets and amplifier 1/f noise.

The chopper stabilized unit cell circuits offer two significant improvements over conventional linear amplifiers: An effect of MOSFET threshold mismatch is vastly reduced and 1/f noise performance of the amplifier is improved. Disadvantages include high circuit complexity and the possibility of generating excess detector noise via clock feedthrough induced excitation, particularly with narrow band-gap photovoltaic detectors.

2.4 The Research on Background Subtraction

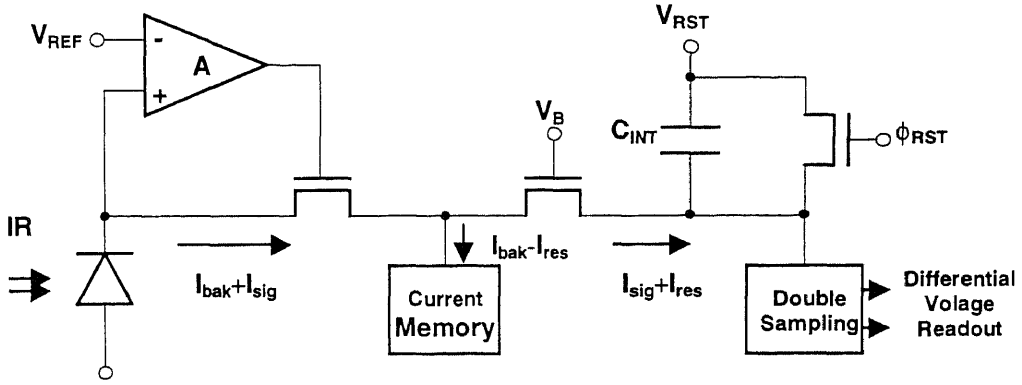
To image a scene in the presence of large dark current is usually referred as background suppression in the field of infrared FPA. It is an important future direction in both scientific and defense applications. Generally, to suppress background by interface circuits, two techniques, named charge domain background suppression circuit [28] and current memory based background suppression circuit [29], can be employed. However, the charge domain circuit cannot alleviate the charge handling capacity problem because it integrates both signal and background charges prior to the background suppression. On the other hand, the current memory circuit needs complicated unit cell circuit, therefore it is difficult to use in a 2D array.

2.4.1 A Unique Current Memory Circuit

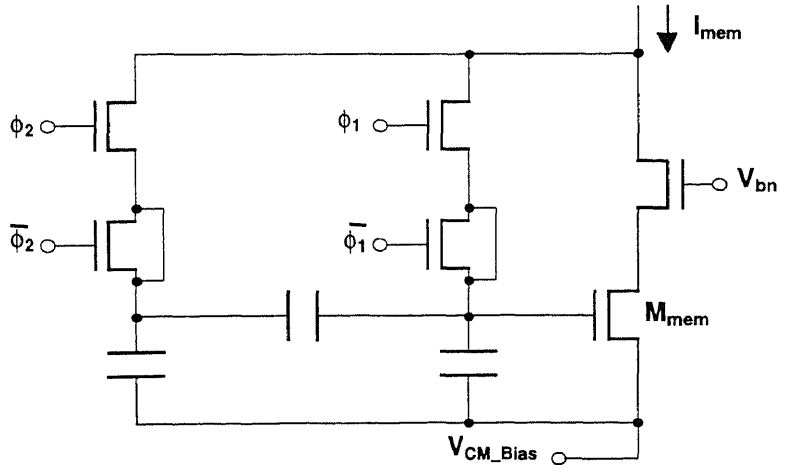
A unique current memory circuit was proposed by NASA Jet Propulsion Laboratory. It utilizes a high accuracy current memory in the feedback loop of a BDI circuit enabling the measurement of small signals below the dark current level. Recently, a 2×130 array with 50μm×400μm unit cell size was designed for an imaging system operating in very long wavelength (VLWIR) region (12-18μm). The circuit measurements indicated an effective charge handling capacity of over 5×10^9 charges/pixel with less than 10^5 electrons of input referred noise.

Figure 2.10a shows the circuit schematic of the unit cell. The circuit performs automatic dark current suppression by first sampling and holding the dark current during the calibration cycle, and then subtracting the same during the imaging phase. A BDI input circuit is used to provide both the required bias stability for the detector and a high

input impedance enabling operation with high injection efficiency. The current mode pedestal subtracting is comprised of a cascode current memory, as shown in Figure 2.10b, with switch-feedthrough reduction and an isolation FET(M_{read}). A double-sampled differential readout (DSDR) is employed to readout the differential infrared signal (Isig), while virtually eliminate the background. The reset noise from the current memory and integration capacitance are removed by the correlated double sampling (CDS) operation inherent in the DSDR.



(a)



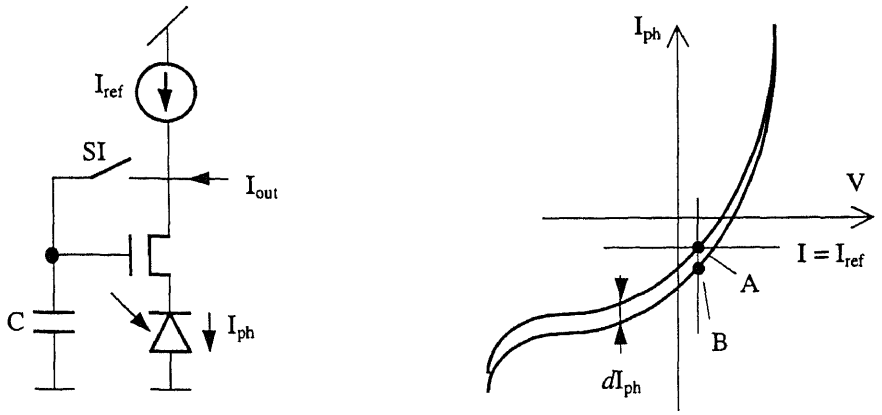
(b)

Figure 2.10 (a) Circuit implementation of current mode background subtraction and (b) Circuit schematic of current memory with feedback suppression.

The dark current memorization includes two steps. During the calibration cycle, the current memory is firstly enabled to memorize the dark current I_{bak}, which consists of the detector dark current as well as the current due to the background ($I_{bak} = I_{dark\text{-}det} + I_{dard\text{-}bak}$). After the memorization is over, the current flowing through the current memory (I_{mem}) is nearly the dark current (I_{bak}), except for a small error current $I_{res} = I_{bak} - I_{mem}$ that flows into the integration node. The pedestal due to the error current is then estimated in the voltage mode by integrating the error current on the integration capacitor (C_{int}), and sampling the resultant voltage onto one of the capacitors C_R of the DSDR. In imaging phase, signal current (I_{sig}) plus the offset current (I_{mem}) are integrated in integration node. After the exposure is over, the resultant voltage is sampled on the other capacitor (C_S) in the DSDR. The difference between the potential of the two capacitors then proportional to the differential infrared signal (I_{sig}), while background is virtually eliminated.

2.4.2 Dynamic Current Mirror Buffered Direct Injection

To develop a readout multiplexer for liquid nitrogen operated LWIR HgCdTe FPA, an offset-calibration current readout method was proposed [30]. The core of this readout method is a dynamic current mirror buffered direct injection (DCM-BDI). The principle of DCM-BDI can be described through Figure 2.11. When switch SI is in closing, the circuit self biases the photodiode in background (point A in Figure 2.11b) by charging the capacitor C to make the reference current I_{ref} equal to the current flowing inside the detector. During integration time with the switch is open, only the photon current (dI_{ph} in Figure 2.11b) will output to an integration capacitor. The background current is cancelled by I_{ref} since the gate voltage of the input FET is fixed by capacitor C.



(a) Circuit schematic (b) Bias principle

Figure 2.11 Detection principle of dynamic current mirror buffered direct injection

A practical DCM-BDI circuit (not shown in the figure) had a buffer to keep the injection linear, and a capacitor to integrate the output current. A 100μm×100μm pixel had been laid out for 3-4 μm p-well CMOS process. The simulations showed that the circuit had good IR background and dark current suppression capability. The integration time, if compared with conventional BDI or CTIA, was increased by 25 times. However, this method needs forward bias of the detector to cancel out the dark current. For very high background, it was concluded that the optimum reference was about one half of the background current. Therefore, the injection efficiency became 50%.

To consider DCM-BDI as a current memory type of circuit, one can see that a forward bias on the detector offers a negative current to cancel out the background current, so that it is not integrated by the integration capacitor and the signal integration time is extended. However, when another dc current is flowing through the detector, extra shot noise will be introduced and the total noise level will be increased by square of 2, since the bias current is not correlated with the shot noise generated by the background radiation. Therefore, the improvement in FPA dynamic range and signal-to-noise ratio is limited.

2.4.3 Buffered Gate Modulation

Buffered gate modulation input (BGDI) is developed from the gate modulation input (GMI) which was discussed in chapter 2.2.3 [31]. An experimental 128×128 chip with 50μm×50μm pixel size was designed and fabricated in 0.8μm double-poly-double-metal n-well CMOS technology. Figure 2.12 is the circuit schematic and the chip architecture of BGDI. To suppress the background on chip using a shared current-mode background suppression circuit, this proposed BGDI method was concentrate on solving the problems of GMI unit cell, such as detector bias uniformity, injection efficiency and current gain stability, so that a 2D array with large FPA format could be realized.

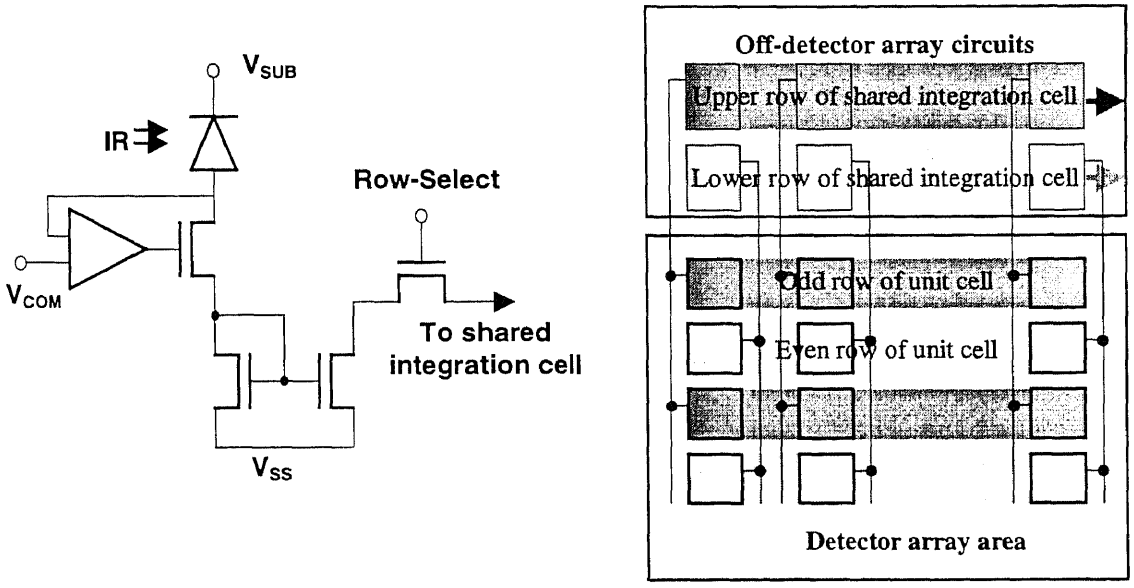


Figure 2.12 Input circuit and chip architecture of buffered gate modulation.

As shown in Figure 2.12, the BGMI circuits integrates the buffered direct injection (BDI) technique with a GMI-like current gain configuration to form the unit cell input stage. The current gain is realized by a new unbalanced current mirror configuration. A current-mode background suppression circuit is implemented with shared integration capacitor unit to suppress the background current before integration.

Moreover, the dynamic charging output stage with CDS circuit can be included to decrease the power dissipation of the output stage and reduce noise.

Through the BDI input stage and the current mirror, the output current is sent to the shared integration cell through the row select switch. The effective current gain $A_{I,BGMI}$ of the BGMI circuit becomes

$$A_{I,BGMI} = \frac{g_{m,input}}{g_{m,load}} \eta_{inj,BDI}, \tag{2.22}$$

and the injection efficiency is changed from $\eta_{inj,DI}$ to $\eta_{inj,BDI}$. Thus, the current gain in the BGMI can be stable without the difficulties in adjusting and stabilizing the external bias voltage while keeping the circuit in low noise. The injection efficiency becomes stable because of a stable detector bias can be achieved. These improvements result in the feasibility of using the shared current-mode background suppression.

2.5 Conclusions

Today's infrared FPA readout technology is still dominated by the matured readout methods. They are direct detector integration (DI) or source follower per detector (SFD), direct injection (DI) and buffered direct injection (BDI), gate modulation, and capacitive transimpedance amplifier (CTIA). The choice of the readout circuit is determined by system parameter, in which detector's characteristics play the most important role. The detector R_0A so that the thermal noise, cutoff wavelength so that the background photon shot noise, and detector bias so that 1/f noise give the bottom line of the readout circuit design. A good design is expected to reduce these noise sources without introduce additional noise problems. The real difficulty of the readout circuit design is to complete

the interfacing task with minimum circuit nonlinearity, threshold voltage variation, 1/f noise, and power dissipation.

The existing literature reveals that, in lower and mid wavelength applications, it is readout circuits that limited the FPA performance. This is because matured readout methods are based on dc measurement technique, and this kind of circuit is susceptible to 1/f noise, drift, and the dark current. When the detector is near perfect, the device will be dominated by readout noise, which is usually referred as noise floor. However, for high background applications, or more generally, for the detection in the presence of large dark current, matured readout circuits will not success because the charge handling capacity is a serious problem. Simply increasing storage capacitor is not only impractical because of limited real estate, it will also cause large reset noise shown by equation 2.20 and reduce the transimpedance as equation 2.8 states. A new readout technology must be developed if there is no breakthrough in detector materials.

The research of on-chip background subtraction has been initiated recently. The common technique is to source or drain a reference current which is equal to the dark current, so that only the signal photocurrent will be accumulated in the storage capacitor. Although it is too early to predict which method may success, two conclusions can be drawn from current research. First, the circuitry complexity was drastically increased. This demonstrated that with the advancement of VLSI technology it is the time to trade circuitry complexity with other characteristic performances. The second trait was that all the new circuits were developed from matured readout methods. This is because infrared FPA is still a very expensive device, and any new technology must be integrated with the existing systems finally. A whole new circuit is in danger of not intimate by the field.

The performance of a FPA with the large dark current can be best characterized by dynamic range. The signal-to-noise ratio actually is the instantaneous dynamic range when all the noise sources are included. The definition of dynamic range DR is the ratio of output voltage swing to the noise level [32], and can be written in decibels as

$$DR = 20 \times \log[\frac{N_{\max} - N_{dark}}{\sqrt{n_{ro}^2 + n_{dark}^2}}], \tag{2.23}$$

where N_{max} is the maximum number of electrons that a unit cell can handle; N_{dark} the number of electrons generated by the dark current; n_{ro} the number of electrons representing readout noise; n_{dark} the number of electrons representing the noise due to the dark current. An ideal readout method should be able to increase the output voltage swing and decrease the noise level at the same time. To keep this standard in mind, the existing readout methods, which are based on dc measurement technique, will not succeed in principle.

CHAPTER 3

THE PRINCIPLE OF CORRELATED READOUT

3.1 Correlated Readout Methodology

Circuit theory indicates that it is often convenient to work with an alternating current (ac) signal instead of a dc signal: Amplifier stability is easier to maintain and both amplifier noise and detector noise are lower. More importantly, the dark current will be filtered out simply because it is a dc signal. However, to use an ac amplifier in a passive system, the constant optical incidence must be converted into an alternating source. The process so called the source modulation is available in several ways. Many circuit schematics can be used in the detection of this modulation signal for discrete detector [33]. Usually, lock-in amplifier is a most widely used instrument in modulated measurement, and is considered as the best equipment to measure the small signal from large noises. Unfortunately, all the circuits used for discrete detector are not ready to be applied in focal plane arrays because of limited real estate and high demand of uniformity in readout circuit design.

To take advantage of optical modulation without violating readout circuit design constraints, especially the unit cell area, a method of correlated readout has been proposed [15]. This thesis investigated the feasibility of this concept. The principle of imaging with modulated source by the correlated readout can be shown by Figure 3.1. An optical modulator is placed in front of the detector to modulate the photon flux from the scene. When the modulator is on in one phase ($\phi 1$ in the Figure), the current generated by the detector will be the photocurrent corresponding to the target photo flux and the dark current that include detector dark current and the radiation not being modulated

(deductible background). When the modulator blocks target flux in another phase ($\phi 2$), only the dark current is in the detector. By controlling the correlated readout circuit synchronically with the modulation control signal, the interface buffer charges the integration capacitor with the signal current and the dark current in $\phi 1$ and discharges it with the dark current only in $\phi 2$. The modulation frequency is selected so that in each cycle of modulation, the integration capacitor is charged only to a part of the saturation level. Since the dark current integration on the capacitor is subtracted by the discharging process, more signal charges will be collected. The signal-to-noise ratio and dynamic range can be improved.

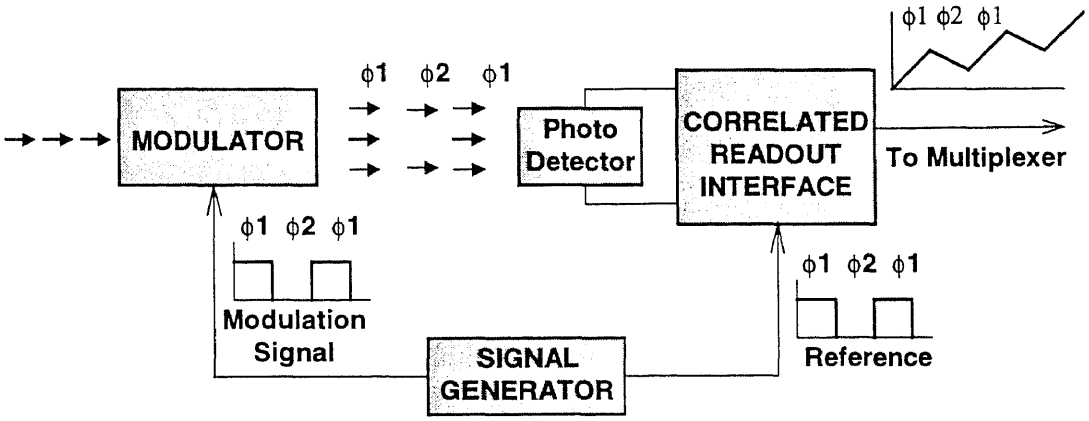


Figure 3.1 The principle of correlated readout method.

The capability of correlated interface circuitry on subtraction of the dark current can be illustrated by Figure 3.2 for the ideal case. In this first order model, the input is considered as a dark current I_{dark} plus a target photocurrent I_{ph}; the readout capability is described as a capacitor C_{int} with a saturation voltage V_{sat} (charge handling capacity $Q = V_{sat} C_{int}$). The maximum signal integration time T_{int} and output voltage swing V_{ovs} can be estimated through $V \cdot C = I \cdot T$. By assuming 100% charge injection efficiency, direct

current coupling readout methods, such as the buffered direct injection (BDI) and the transimpedance amplifier (CTIA) described in chapter 2.2, simply integrate I_{dark} and I_{ph} and have results as

$$T_{int\_D} = \frac{V_{sat} C_{int}}{I_{dark} + I_{ph}}; \tag{3.1a}$$

$$V_{ovs\_D} = \frac{I_{ph}}{I_{dark} + I_{ph}} V_{sat}. \tag{3.1b}$$

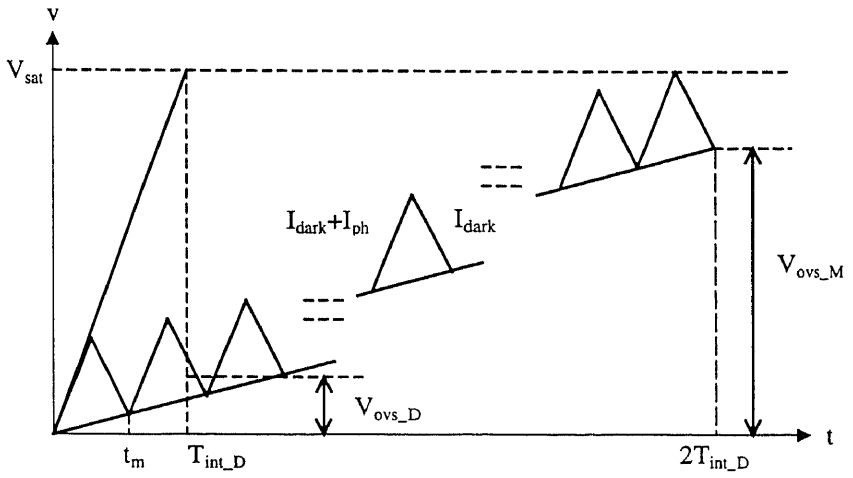


Figure 3.2 DC model for the process of correlated interface circuits.

Instead of directly charging the capacitor to the saturation level, the correlated readout circuit discharges C_{int} by the dark current in a mid-level before saturation, and charges it again to achieve more signal charge collection. This process can be controlled by signal modulation and synchronized readout. The maximum integration time and output voltage swing by the correlated readout method, V_{ovs_M} and T_{int_M}, will be in terms of the period of the control signal t_m ($t_m = 1/f_m$, where f_m is the modulation frequency), and can be calculated by

$$T_{int\_M} = \frac{C\,int}{I_{ph}} V_{sat} - \frac{I_{dark} t_m}{2 I_{ph}}; \tag{3.2a}$$

$$V_{ovs\_M} = V_{sat} - \frac{I_{dark} t_m}{2C_{\text{int}}}. \tag{3.2b}$$

The ratio of the output voltage swing or the signal integration time of the correlated method to the dc-coupled method can be expressed as

$$Ratio = (1 - \frac{I_{dark} t_m}{2C_{\text{int}} V_{sat}})(1 + \frac{I_{dark}}{I_{ph}}). \tag{3.3}$$

3.2 Signal Processing by Correlated Readout

3.2.1 Basic Techniques

From a circuitry point of view, signal processing of a FPA first occurs at signal integration for achieving better signal-to-noise ratio (S/N) before multiplexing the image signal, although this process is usually considered as signal detection in the research of sensors. Basically, there are three such techniques for optical sensing. They are photon counting, dc measurement and phase sensitive detection [34]. The applications are dependent on detection conditions.

Photon counting is a technique that has been employed for many years with photomultpliers when the light intensity is low. Its analysis methodology based on Poisson statistics has been inherited by FPA technology to represent S/N and dynamic range although photodetection processed by photogate and photodiode are more complicated. When photon flux is low, the light incident on the detector is considered as the form of individual photon events. Photon counting simply counts all the pulses of the signal and the dark current in a time period. The S/N is calculated by a number of signal counts N_s, dark current counts N_d, and integration time T_{int} as

$$\frac{S}{N} = \frac{N_s}{(N_s + N_d)^{1/2}} \cdot T_{\text{int}}^{1/2}. \tag{3.4}$$

Equation 3.4 shows that S/N can be improved to an acceptable level by extending the integration time, no matter how small the signal counts are compared to the dark current counts. However, the integration time is limited by the charge handling capacity in the FPA technology.

When a photo diode works in current mode [35], the photo current plus the dark current become essentially large, therefore, dc measurement technique should be applied. In dc measurement technique, current from the detector is considered as a dc signal with noise superimposed on it. To integrate the signal is similar to improve S/N by passing the signal through a low pass filter. To achieve longer integration time is equivalent to having a large RC constant that narrows the output bandwidth. More accurately, a reset integrator can be modeled to give the scenario of dc measurement technique in the application of readout circuitry, which is illustrated in Figure 3.3.

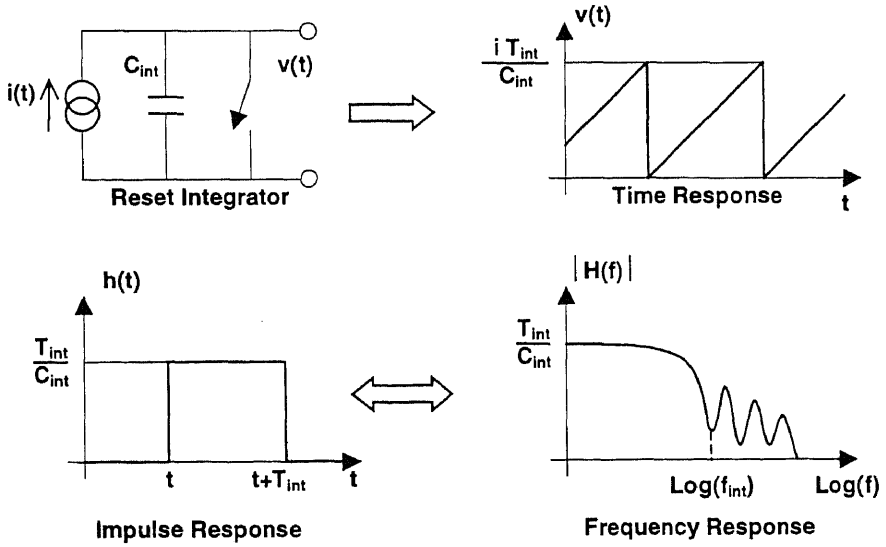


Figure 3.3 The reset integrator action can be modeled as a continuous integrator that is sampled and subtracted as discrete time increment.

The voltage on the input node, shown as a continuous ramp, is the integral of the detector current i(t). The resulting output voltage v(t) can be expressed in terms of the convolution of the input current and the impulse response h(t):

$$v(t) = i(t) * h(t) \quad [\mathrm{V}]. \tag{3.5}$$

The impulse response of the reset integrator h(t) over the integration period T_{int} is

$$h(t) = \frac{1}{C_{\mathrm{int}}} \int_{t^-}^{t^-+T_{\mathrm{int}}} \delta(x)dx \quad [\mathrm{V}], \tag{3.6}$$

which is a step to amplitude of $1/C_{int}$ at the beginning of the integration, and returns to zero after sampling and resetting at T_{int}. The frequency response of the reset integrator can be determined by evaluating the Laplace transform:

$$V(f) = I(f)H(f) \quad [\mathrm{V}], \tag{3.7}$$

where the Laplace transform of h(t) of equation (3.7) is

$$H(f) = \frac{T_{\mathrm{int}}}{C_{\mathrm{int}}} \frac{\sin(\pi f T_{\mathrm{int}})}{\pi f T_{\mathrm{int}}} = \frac{T_{\mathrm{int}}}{C_{\mathrm{int}}} \frac{\sin(x)}{x} \quad [\mathrm{V/A}]. \tag{3.8}$$

The derivation of above expression is strictly valid for an ideal reset integrator. In practice, however, some dead time exists between the reset and the onset of integration (due to switching time). Equation 3.8 provides a good approximation in case where the dead time is a small fraction of the integration time.

The sinc function, which is defined as

$$sinc(x) = \frac{\sin(x)}{x}$$

in equation 3.8 indicates the fact of attenuating at frequency higher than Nyquist limit, while passing the dc and low frequency signal. The high frequency ac component could

be signal, noise, or interference picked up on the input node. In signal accumulation, high frequency components tend to cancel out its own excursions above and below the dc signal, thus resulting in a significant reduction in amplitude. Since the integration time is assumed to be nearly equal to the time between frames, the only unaliased frequencies that can pass through the reset integrator are those less than half the frame rate, if sampling is performed just before reset.

When the detection is dominated by low frequency noise, such as 1/f noise and dc drift, the reset integrator is in principle not feasible. In fact, if the signal-to-noise ratio is very low, such as the detection condition considered by this thesis research, other methods must be resorted. The phase sensitive detection is one such approach [36], [37].

3.2.2 The Phase Sensitive Detection

The phase sensitive detection (PSD) is the core of lock-in amplifier that has been widely used to detect the weak signal from large noise. The principle of PSD is shown in Figure 3.4. The key to the operation is a commutating switch that is controlled from a reference voltage. As the reference changes polarity, the switch changes position between A and B to give a change of gain between +1 and -1 in the signal path. The output of the switch is then applied to a low pass filter to deliver a dc voltage output. If the input signal has the same frequency and phase as the reference voltage, there will have a dc output that is proportional to the input signal amplitude. Otherwise, due to the combination of switching operation and low pass filtering, the input signals tend to cancel out by themselves and can not establish a dc output.

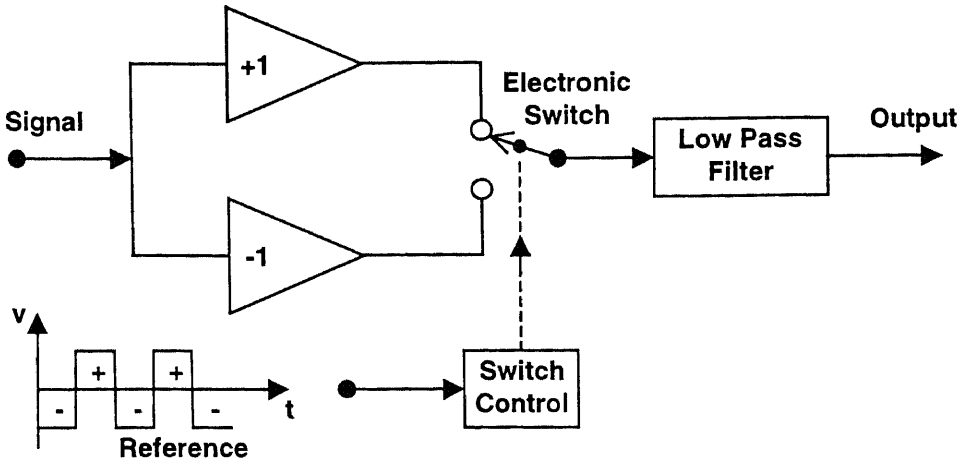


Figure 3.4 The principle of phase sensitive detection.

To determine the exact relationship between signal and reference, the switching operation can be modeled as a multiplication of the signal by a square wave that has the Fourier series representation of

$$r(t)=\frac{4}{\pi}[\cos(\omega_R t+\varphi_R)-\frac{1}{3}\cos 3(\omega_R t+\phi_R)+\frac{1}{5}\cos 5(\omega_R t+\phi_R)-\ldots]. \quad (3.9)$$

Thus, the output of the switches $V_p(t)$, which is the product of signal input s(t) and reference r(t), will be

$$V_p(t)=r(t)s(t)=r(t)\cdot V_s\cos(\omega_s t+\phi_s). \quad (3.10)$$

The result of the derivation can be expressed as

$$V_p(t)=\frac{2V_s}{\pi}[\cos(\varpi_R t\pm\omega_s t\pm\phi_R\pm\phi_s)-\frac{1}{3}\cos(3\omega_R t\pm\omega_s t+3\phi_R\mp\phi_s)$$

$$+\frac{1}{5}\cos(5\omega_R t\pm\omega_s t+5\phi_R\pm\phi_s)-\ldots]. \quad (3.11)$$

For the signal that has the same frequency as reference, a dc component will be obtained:

$$V_{out}=\frac{2V_s}{\pi}\cos(\phi_R-\phi_s)\ +\text{terms of order } 2\omega_R \text{ and higher frequencies.} \quad (3.12)$$

If the signal and reference have different frequencies, then, the output is the form of

$$V_{out} = \frac{2V_s}{\pi}\cos[(\omega_R - \omega_s) + (\phi_R - \phi_s)] + \text{terms of higher frequency.} \qquad (3.13)$$

By passing these outputs through a low pass filter, only the signals have the frequency of ω_R, and close of it, will build up a dc output, while the signals away from ω_R will be filtered out. In other words, the PSD is in effect a band pass filter whose bandwidth is dependent on the output low pass filter. If in the detection the signal is modulated to produce a dc output, and the noise is unmodulated to produce only ac voltage that could be attenuated on passing through the low pass filter, the signal-to-noise ratio of a input signal can be improved.

The further complication of PSD is harmonic transmission windows. If the signal frequency contains an odd multiple of the reference frequency, a dc output will be obtained from the PSD. This can be seen from the other term of equation (3.11). When

$$\omega_s = (2n+1)\omega_R,$$

there will have dc output of

$$V_{out} = \frac{2V_s}{(2n+1)\pi}\cos[(2n+1)(\phi_R - \phi_s)] + \text{frequency-dependent terms.} \qquad (3.14)$$

In practical instrumentation, such as lock-in amplifier that is shown in Figure 3.5, the harmonic transmission is avoided by putting a band pass filter before PSD and an ac-coupled preamplifier can be applied at the input to reject dc component. To eliminate all the signals with the frequency other than modulation frequency, lock-in amplifier can achieve significant improvement of SNR. Unfortunately, lock-in amplifier can not be applied for focal plane array technology because of circuitry complexity. The proposed correlated readout method is an approach to realize PSD function with simple circuits.

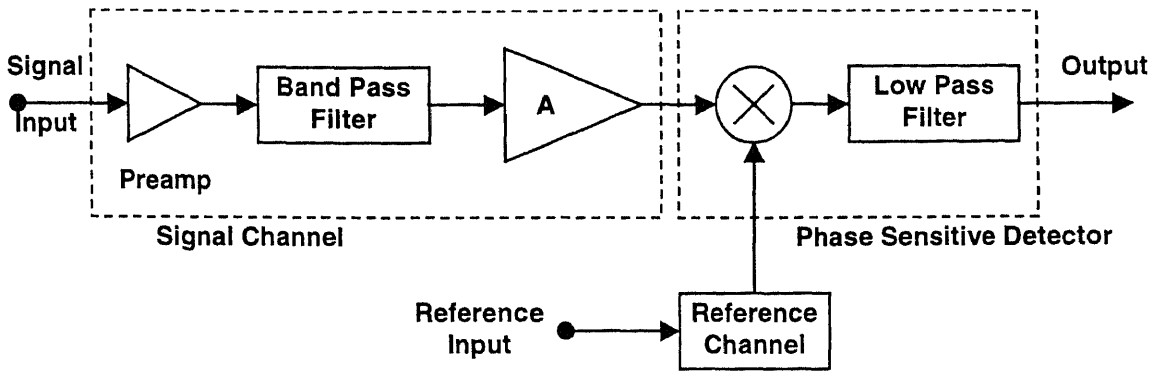


Figure 3.5 A basic lock-in amplifier.

3.2.3 A Correlated Reset Integrator (CRI)

As in the case of the reset integrator where the theory of low pass filter is applied, the idea of the correlated readout is based on the phase sensitive detection. However, to apply the principle of PSD for focal plane array technology, a conventional multiplier is restricted by the readout circuit design constraints because there is no simple circuit that can change the polarity of the signal. In addition, any signal conditioning circuit (such as a band pass filter and ac-coupled preamplifier) before demodulation process is almost not possible with today's IC technology. Therefore, the correlated readout method was proposed and a different detection model must be established.

Since the correlated readout circuits perform demodulation by switching 'raw' current from the detector, the assumption of time invariant system behind the derivation of PSD will not be strictly applicable. The principle of correlation technique [38], which has been applied in correlated double sampling (CDS), should be used to justify the following analysis (The correlation is the internal relationship between two measurements for the mean value). In the case of the correlated readout method, the current from the detector at different times will be correlated because they are generated from the same

source. As described at the beginning of this chapter, dc component of the dark current can be canceled out by discharging since the dc level does not change in two modulation phases. In other words, two current signals are one hundred percent correlated. For the ac fluctuation, one may expect that slowly changed signals (low frequency noise) will be reduced to a factor because their correlation coefficient can be enlarged to cause cancellation, if the modulation frequency is relatively high (shorter correlation time).

A derivation of low frequency noise reduction based on correlation technique can be found at reference [39]. Here an approach for the signal processing of the correlated readout using system theorem is presented. The transfer function of the reset integrator is inherited to model the correlated readout method as a correlated reset integrator (CRI). Figure 3.6 illustrates this proposed model in time and frequency domains. In the model of the CRI, the process of each modulation phase is considered as a reset integrator with integration time of t_p ($2t_p = t_m$ where t_m is the period of the modulation signal). To refer to the first charging phase, the other processes are delayed time of kt_p. Therefore, the correlated reset integrator can be modeled as a set of parallel delay processors followed by a reset integrator, as Figure 3.6b shown. According to the time shift theorem (pure delay by t seconds has the transfer function of $e^{-j\omega t}$) each delay processor has the transfer function of $e^{-jk\omega tp}$. In addition, the negative sign due to discharging at the summing junction can be absorbed as a gain of -1. Figure 3.6c shows such a model in the frequency domain. For the convenience of analysis, the total integration time T_{int} is assumed to be an integer N multiplied by the modulation period ($T_{int} = Nt_m = 2Nt_p$), as shown in Figure 3.6a.

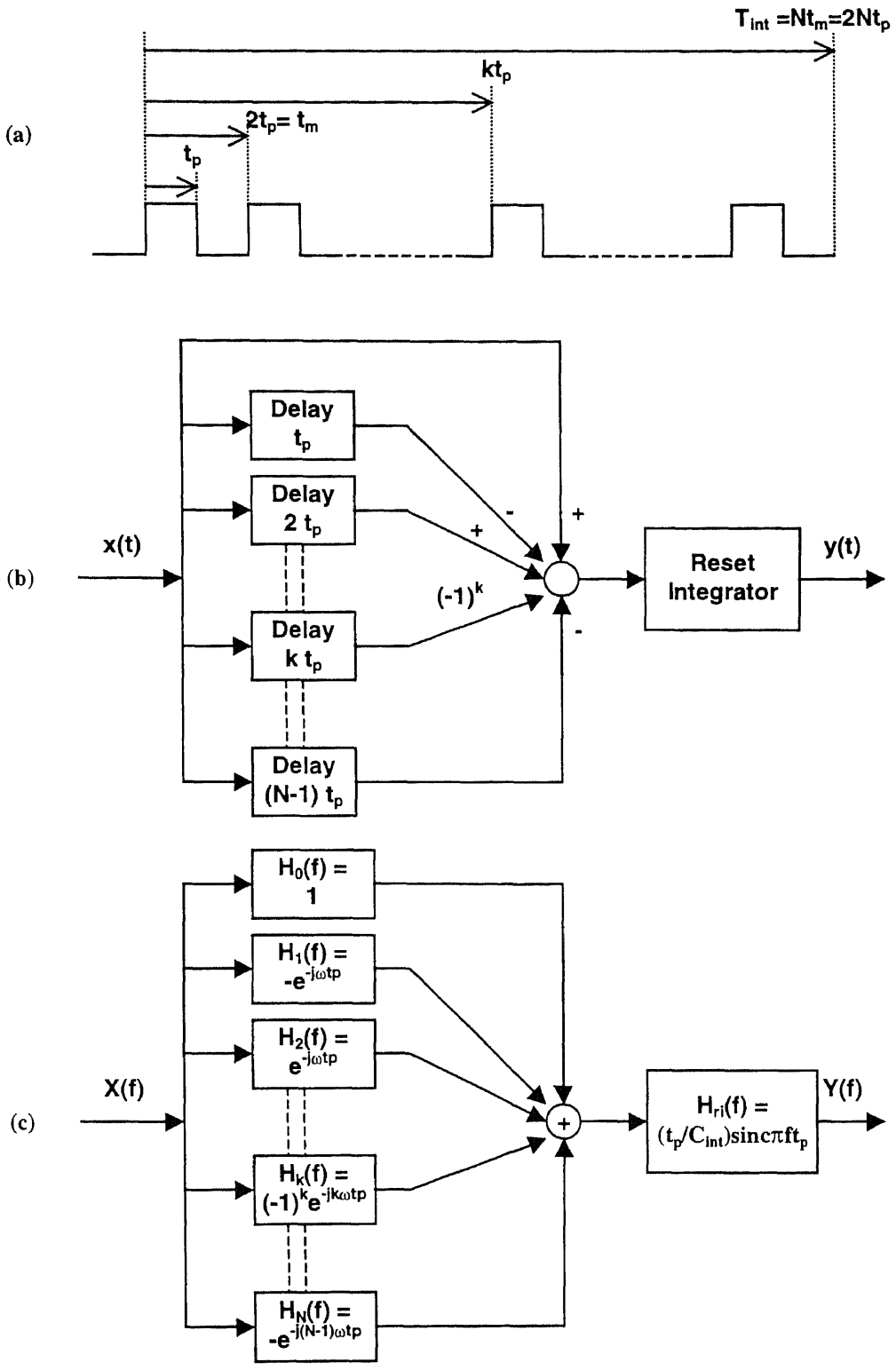


Figure 3.6 The correlated reset integrator is modeled as a parallel delay processor followed by a reset integrator with integration time of t_p. (a) Timing. (b) Simulation diagram. (c) Frequency domain block diagram

By applying the rule of parallel and cascade systems [40], the transfer function of modeled system $H_{cri}(\omega)$ can be found as

$$H_{cri}(\omega) = [H_0(\omega) + H_1(\omega) + H_2(\omega) + ... + H_{2N-1}(\omega)] \cdot H_{ri}(\omega). \qquad (3.15)$$

The summation of the delay system can be calculated by

$$\sum_0^{2N-1} H_k(\omega) = \sum_0^{2N-1} (-1)^k e^{-jk\omega t_p} = \frac{1 - e^{-j2N\omega t_p}}{1 + e^{-j\omega t_p}}$$

$$= \frac{\sin(2N\omega t_p/2)}{\cos(\omega t_p/2)} e^{-j(2N+1)\omega t_p/2}.$$

To multiply sinc function of the reset integrator for finding system's amplitude ratio, the frequency response of the CRI can be expressed by

$$H_{cri}(f) = \frac{\sin(2N\pi f t_p)}{\cos(\pi f t_p)} \cdot \frac{t_p}{C_{\text{int}}} sinc(\pi f t_p) = \frac{t_p}{C_{\text{int}}} \frac{\tan(\pi f t_p)}{\pi f t_p} \sin(2N\pi f t_p).$$

Reorganizing the above expression, there is

$$H_{cri}(f) = \frac{2Nt_p}{C_{\text{int}}} \frac{\sin(2N\pi f t_p)}{2N\pi f t_p} \tan(\frac{2N\pi f t_p}{2N}) = \frac{T_{\text{int}}}{C_{\text{int}}} sinc(\pi f T_{\text{int}}) \tan(\frac{\pi f T_{\text{int}}}{2N}). \qquad (3.16)$$

To set $x = \pi f T_{int} = 2N\pi f t_p$, equation (3.16) can be written as

$$H_{cri}(f) = \frac{T_{\text{int}}}{C_{\text{int}}} sinc(x) \tan(\frac{x}{2N}). \qquad (3.17)$$

Correspondence to the sinc function that is used to express the frequency response of the reset integrator, a function that has the similar form as sinc function is obtained to express the frequency response for the correlated reset integrator. This function f(x) can be called as correlated sinc function and can be written as

$$f(x) = sinc(x) \tan(\frac{x}{2N}).$$

The above expression is simple in form, however, since the T_{int} is determined by both the modulation frequency f_m and the number of switching times N ($T_{int} = Nt_m = N/f_m$), to demonstrate the characterizations of this correlated sinc function, the f(x) should be written as

$$f(x) = \frac{\sin(\pi N x)}{\pi N x} \tan(\frac{\pi x}{2}),$$

where $x = f/f_m$ and f_m is the modulation frequency. Figure 3.7(a) shows the plots of the f(x) for N equal to 5, 10 and 15, and Figure 3.7(b) shows the plots of the regular sinc(x) with the same processing time (the same N). By comparing the plots of sinc function that represents the reset integrator, one can see that the primary peak of the correlated sinc function has about the same shape as sinc function, but is shifted to center at the modulation frequency f_m (x = 1). For a certain f_m, each peak in the f(x) plots becomes narrower if the number of switching times is increased (large N). Actually, this is because the total signal integration time is extended so that a better signal-to-noise ratio is achieved. However, with longer integration time, the peaks of the regular sinc function are also narrowed. If two processors have the same integration time and the noise input is a pure white noise, the total noise power transmission will remain the same. An important issue here is that the increase of N, so that the total processing time, must be limited by the saturation of the capacitor, otherwise, all the derivations are not valid. When large dark current is present, the CRI can subtract the dc component of the dark current to achieve longer integration time. This means the CRI has better noise reduction capability due to the extension of the integration time. More importantly, low frequency noise such as dc drift and 1/f noise will be reduced in the process.

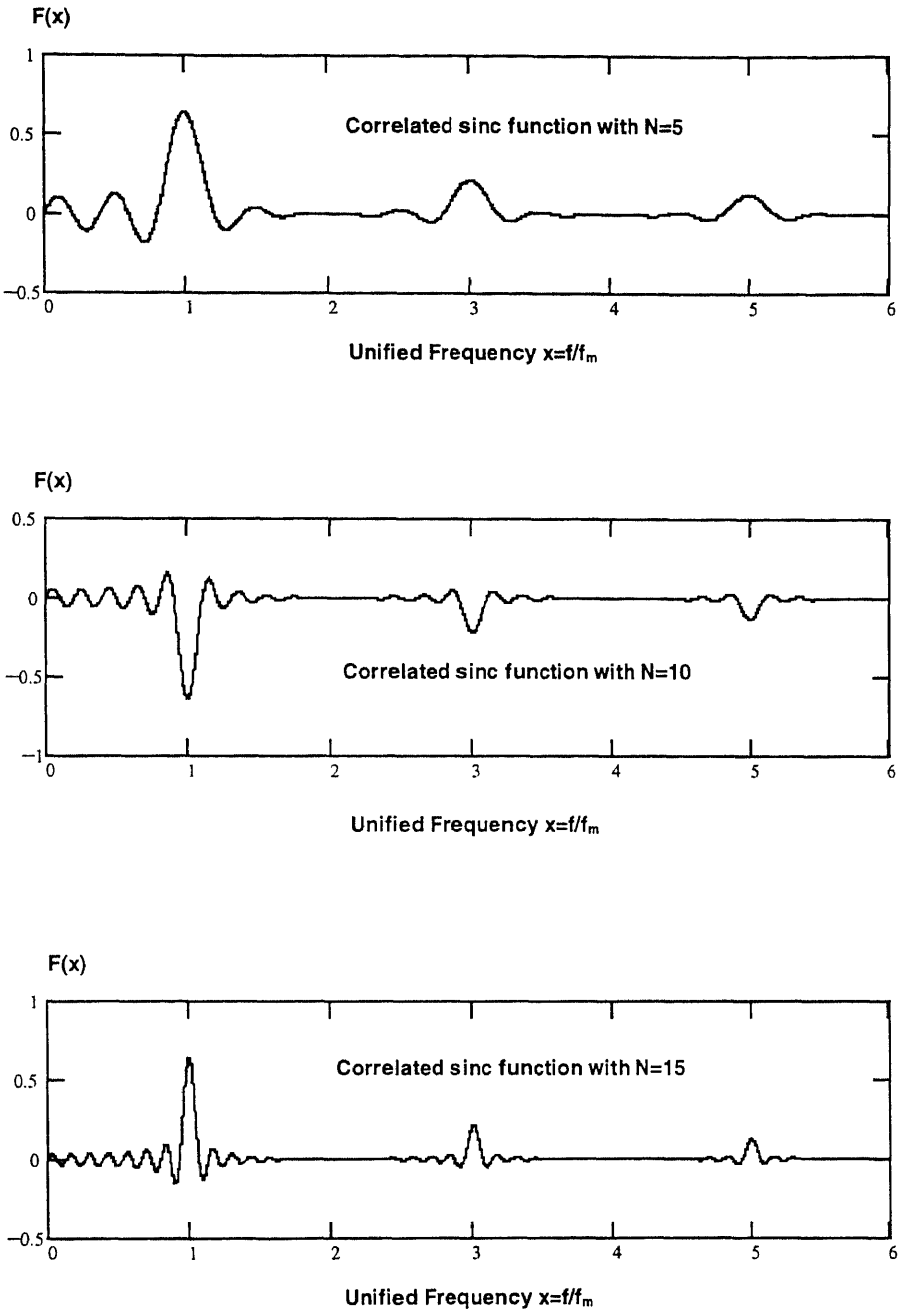


Figure 3.7(a) The plots of the correlated sinc function f(x) against f/f_m with N equal to 5, 10 and 15. To compare with the Figure 3.7(b) one can see that f(x) has about the same shape with the sinc(x), but the primary transmission window is shifted to the modulation frequency f_m, and additional odd harmonic transmission windows are opened.

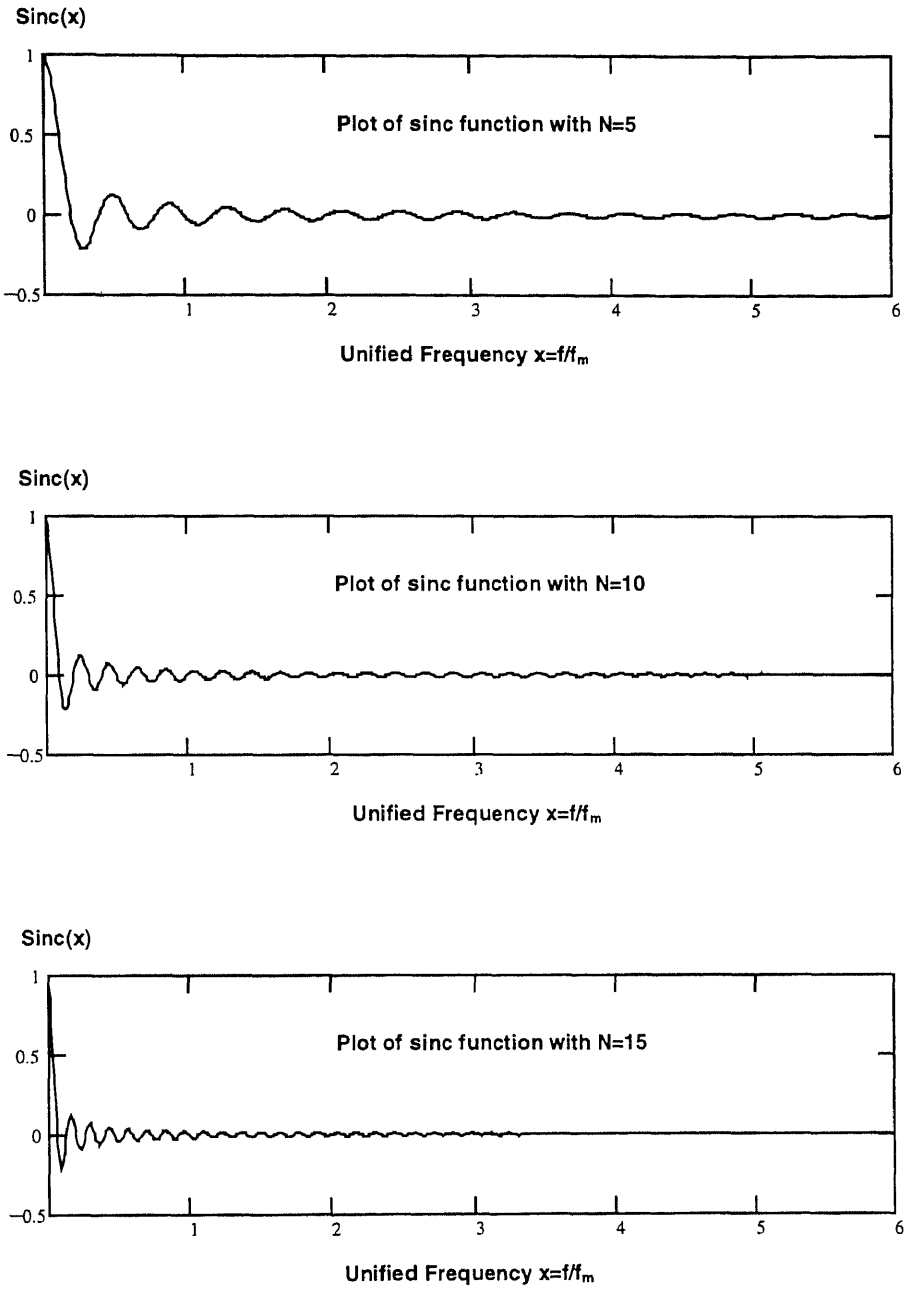


Figure 3.7(b) The plots of the sinc function with the correspondence processing time with the plots in Figure 3.7(a). N equal to 5, 10 and 15 means the integration times are $5/f_m$, $10/f_m$ and $15/f_m$ where f_m is the modulation frequency if a CRI is used to process the same input signal.

Figure 3.7(a) also shows that the CRI has odd harmonic transmission windows as the case of phase sensitive detection, because tangent function goes to infinity at half π and once again after each π. In addition, the negative primary peak for an even number of N demonstrates that the signal transmission can also be affected by the phases that correspondence with the modulation signal. All these symptoms show that the correlated reset integrator is behaved like a PSD processor. If the noise input is a pure white noise, the output noise level will not improved referred to the reset integrator. However, if the features in the lock-in amplifier can be added on the CRI, a very high signal-to-noise ratio can be expected.

3.3 Correlated Interface Circuits

As mentioned in last chapter, the readout circuit design is constrained by unit cell area, power dissipation, threshold sensitivity, operation temperature, and fabrication yield. The majority of transistors in the circuit will perform low noise analog function rather than high-speed digital logic, memory and computing functions. To realize a new readout method early and economically, the interface circuit should be developed from that mature readout methods, so that in a practical device design all the readout architectures and even unit cell design may be inherited. Many performance characteristics, such as the power dissipation and nonnuiformity, may reach the same level as those original circuits. This section would be a presentation of the correlated interface circuits developed from the mature methods reviewed in chapter 2.2. The circuits developed from capacitive transimpedance amplifier were discussed first and followed by the circuits developed from direct detector injection, buffered direct injection and gate modulation.

3.3.1 Circuits Developed from CTIA

Because a differential amplifier can integrate current in two directions, the capacitive transimpedance amplifier (CTIA) is the most ideal circuit to develop a correlated readout circuit. The recent report also showed that the CTIA has the best overall performance characteristics compared to other IR detector interface circuits at low backgrounds [40]. For the applications of large dark current, a well-designed differential amplifier will be able to ensure that the detector with low resistance still functions as a current source. The problems remaining are charge handling capacity, dc drift and 1/f noise.

At this point, it appears that the best circuit developed from the CTIA is a correlated CTIA. From Figure 3.8 one can see that four switches and two control lines are added to a conventional CTIA circuit for it to be become the correlated CTIA. Synchronized with a modulation signal, M1 and M3 turn on while M2 and M4 stay off in $\phi 1$ when the detector is responding to the source signal and backgrounds so that all the current will be integrated in the integration capacitor. When the optical modulator blocks the source radiation in $\phi 2$, M2 and M4 turn on while M1 and M3 become off, the capacitor will be discharged this time by the dark current only. This process can be repeated until the operation amplifier saturation level is reached. By using an optimized modulation strategy, large dynamic range is expected. The additional advantage of this circuit is that conventional readout architecture can be used to design a 2D array and the correlated double sampling (CDS) can still be applied to eliminate reset noise. However, it will introduce new engineering difficulties. First, it requires that the detectors be processed in isolated well so that discharging can be performed symmetrically as charging

process. Secondly, one more bonding pad is needed for each pixel of hybrid FPA. This means doubling the difficulty of indium bonding if a 2D-hybrid array is fabricated.

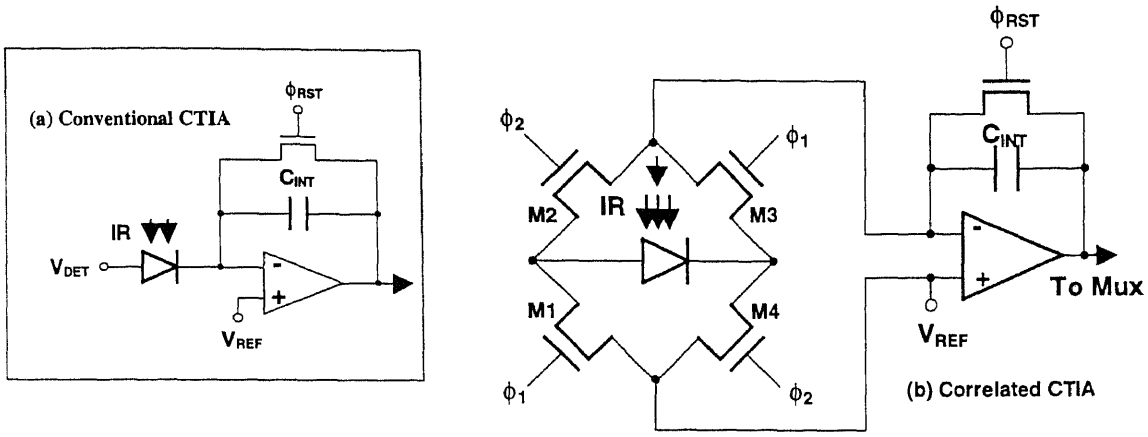


Figure 3.8 Circuit schematic of (a) Conventional CTIA and (b) Correlated CTIA.

The second approach, named twin CTIA, is a standard synchronizing detector as shown in Figure 3.9. Only two switches are needed if the CTIA design is done. One channel will be used to integrate the signal and the dark current while the other channel will integrate the dark current only. A shared differential amplifier will perform the dark current subtraction after differential readout. This circuit does not need any modification on detector array and bonding technology, and a simple amplifier like an inverter mentioned in chapter 2.2.4, may be feasible when the detection conditions are not very critical. The main drawbacks of this approach include the limitation on dynamic range and the difficult to use correlated double sampling. The first problem is because the integration capacitors will not be discharged and reused again. The second problem is because two capacitors can not establish the correlation relationship; the reset noise in each capacitor will add up in rms at the output of the differential amplifier. In addition, even without any other circuits, two amplifiers and two capacitors will make this approach very difficult to design a 2D array.

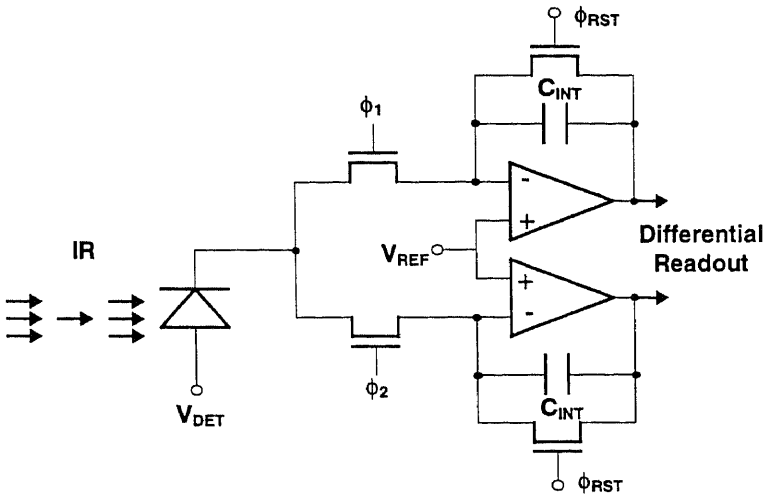


Figure. 3.9 Circuit schematic of twin CTIA.

To save the unit cell area in the twin CTIA and process the dark current subtraction within the pixel, especially when sophisticated operational amplifier becomes necessary, a differential integrator can be applied (Figure 3.10). Besides the same disadvantages of dynamic range and reset noise as in the twin CTIA, this circuit will have the difficulty of bias adjustment (V_{ref} in Figure 3.10). However, like the gate modulation (which is described in chapter 2.2.3) when this problem is solved, it may benefit to fixed pattern noise reduction.

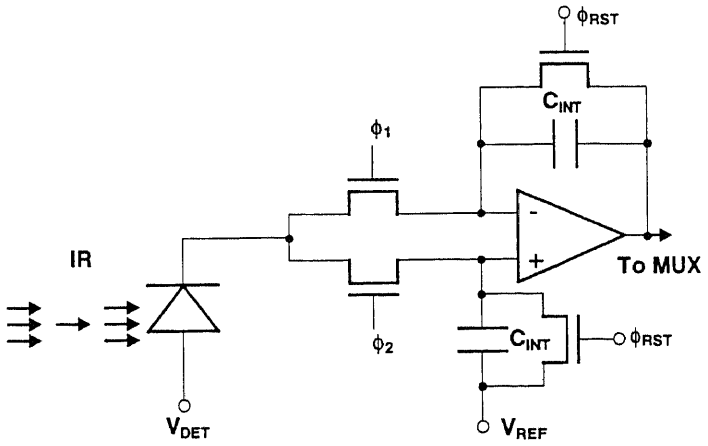


Figure. 3.10 The circuit schematic of the differential integrator.

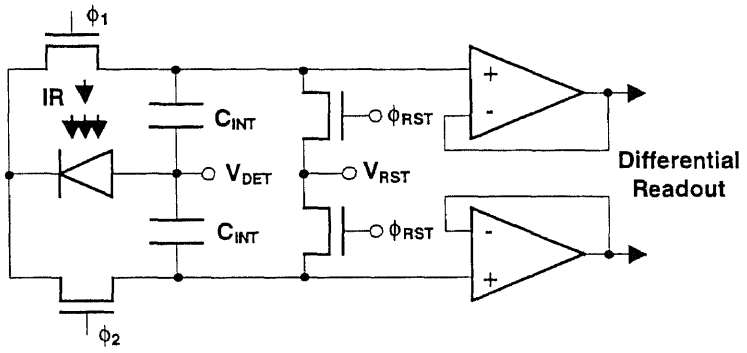
3.3.2 Circuits Developed from Other Methods

A practical FPA finally must be integrated into existing equipment. This means that in most of the time a designer must use the previous design architecture. If detection conditions allowed, to develop a correlated interface circuit from an existing method instead of designing an unfamiliar readout circuit will be the best approach for solving the problems. The ideas for developing the correlated readout circuit from other readout methods are discussed below.

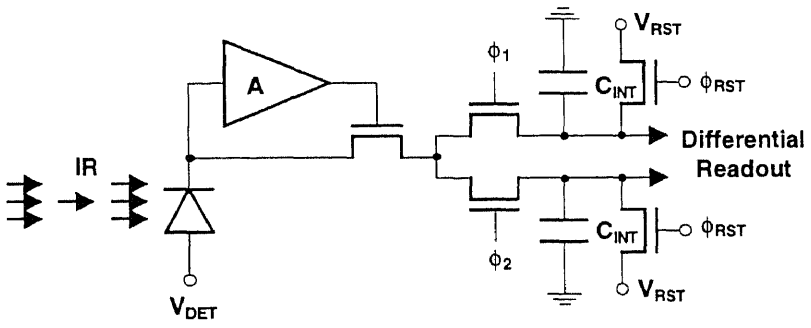
It is well known that the other readout methods (which have been reviewed in chapter 2.2) are inherited from charge coupled devices (CCD). Although active pixel has more design flexibility, the principle of on-chip signal processing in charge domain is still applied -- there is only one charge polarity for processing! This means that to charge and discharge (by change the charge polarity) the integration capacitor as the correlated CTIA is not possible in principle. The only way of performing correlated subtraction is to use the structure like the twin CTIA. To compare with many other approaches in CCD technology, such as dark pixel technology, the correlated readout approach will achieve better signal-to-noise ratio because low frequency noise, such as dc drift and 1/f noise, can be reduced significantly.

Following the same idea in developing the twin CTIA, direct detector integration (DDI) can be developed to a twin DDI and buffered direct injection (BDI) can be developed to a twin BDI, as shown in Figure 3.11. The same as the twin CTIA, a differential readout technique must be used for these circuits and the CDS becomes not necessary. For the hybrid FPA architecture, bonding strategy will keep the same as the conventional methods. By reducing 1/f noise, large capacitors can be used in twin DDI

for long integration time applications. With only two switches are added in each unit cell, the circuitry is still very simple compared with other methods. However, in practical design, there will have some other issues that need to be solved, since DDI usually works in voltage mode. Compared with the twin CTIA and DDI, the advantage of the twin BDI can be seen from the pixel area concern since only one buffer amplifier is added to the BDI for it to become the twin BDI.



(a) A twin DDI



(b) A twin BDI

Figure 3.11 Correlated readout circuits developed from the direct detector integration (DDI) and the buffer direct injection (BDI).

Gate modulation does not integrate photocurrent directly. Therefore, it should have more design flexibility to become a correlated interface circuit by adjusting current gain and bias. Unfortunately, since the gate modulation is very difficult to control itself,

to develop a correlated gate modulation in standard CMOS technology becomes extremely difficult. It is not hard to imagine how to make up a correlated gate modulation using two storage capacitors like the twin CTIA. The question is that is it possible to realize the circuit as shown in Figure 3.12. By modulating the gate of two switches, the integration capacitor is charged by one source V_{IN} and discharged by another source V_{OUT}. The price is one more power supply. The benefit will be a large dynamic range with simple circuitry.

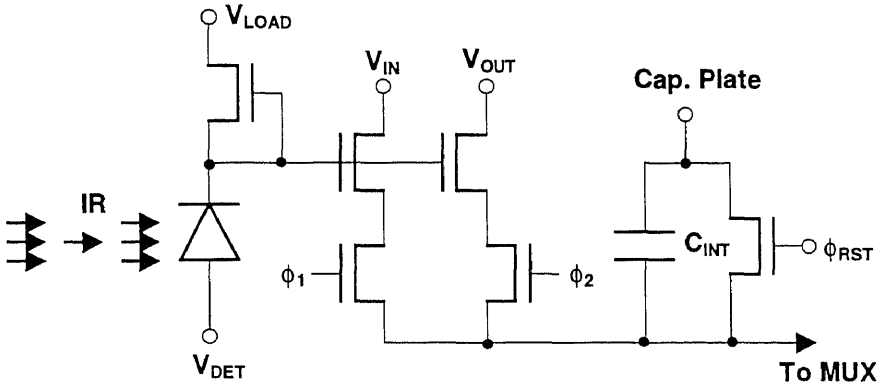


Figure 3.12 An ideal circuit for a correlated gate modulation topology.

Analog switches had been used in new proposed methods to select calibration and integration modes, such as current memory and DMI-BDI described in chapter 2.4. The calibration mode is the same as one phase when signal flux is blocked by the modulator. If these kinds of methods succeed, they may be transferred into the correlated readout method quickly. The best approach might be the combination of these two methods such as a current memory – twin BDI. The current memory can be used to drain the dc component of the dark current. The twin BDI is then applied to minimize the ac fluctuation due to dc drift and 1/f noise. A better dynamic range characteristic may be expected.

3.4 The Applications

3.4.1 Passive Imaging

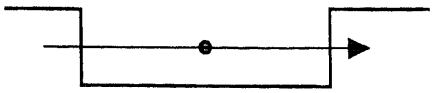
A direct application of the correlated readout on passive infrared imaging is to recover the image when large dark current is present. For the detector dark current due to low R_0A, the position of the optical modulator will not affect the result. However, when this method is used to subtract the background due ambient radiation, the location of the modulator must be considered and it may result in redesigning the optical system. In principle, only the radiation behind the modulator can be considered as deductible background. For instance for a ground based system, the modulator at most can be placed in front of the telescope; it is impossible to eliminate the background due to the radiation of atmosphere, except that the disturbance can be distinguished (modulated) from the image signal.

If a mechanical chopper is to be used as the modulator, the effect of the chopper configuration on the image signal must be studied. The further question will be how to integrate the chopper into an imaging system. It is known that there are five basic chopper configurations for discrete detectors, as shown in Figure 3.13. The most important concern for these chopper designs is the modulation factor MF, which is defined as

$$MF = \frac{\text{rms of fundamental component}}{\text{peak - to - peak value of total waveform}}.$$

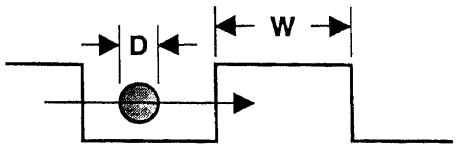
Some published results show that the MF varies with the configurations. From existing data one can see that a practical mechanical chopper, such as Case III of Figure 3.13, may bring some noise due to the two-dimensional effect.

Case I: square wave chopping



$$MF_1 = \frac{\sqrt{2}}{\pi} \cong 0.4502$$

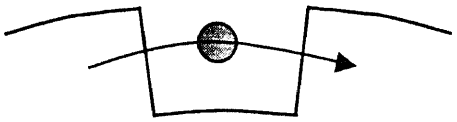
Case II: rectangular teeth, linear motion, circular aperture



$$MF_2 = \frac{\sqrt{2}}{\pi} = [J_0(z) + J_2(z)]$$

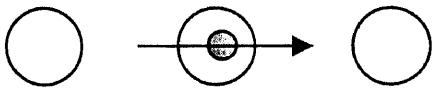
Where $z = \frac{\pi D}{2W}$

Case III: radial teeth, circular motion, circular aperture



$$MF_3 = \frac{\sqrt{2}}{\pi} F[\frac{-N}{2}, \frac{+N}{2}, 2, (\frac{d}{D})^2]$$

Case IV: circular chopper holes, linear motion, circular aperture



Case V: circular chopper holes, circular motion, circular aperture

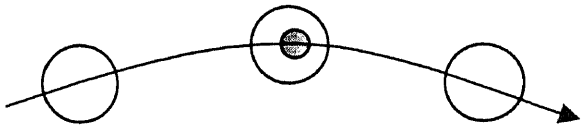


Figure 3.13 Basic mechanical chopper configurations.

Other approaches besides the mechanical chopper are acousto-optical (AO) modulator [41] and electro-optical (EO) modulator [42]. The AO devices are based on the phenomenon of AO diffraction. When an acoustic wave propagates in an optically transparent medium, it produces a periodic modulation of the index of refraction via the elasto-optical effect. This provides a moving phase grating that may diffract portions of an incident light into one or more directions. To apply the AO modulator for linear array with a scanning system, the image can be made stationary by directing the image through a deflector that scans with equal and opposite velocity. However, further study is required

for applying it to the correlated readout since in each frame time the image needs to be modulated.

The EO modulator is a device with operation based on an electrically induced change in the index of refraction or change in nature birefringence. The basic idea behind the EO devices is to alter the optical properties of a material with an applied voltage in a controlled way. The changes in the optical properties, particularly the permittivity tensor, translate into a modification of some parameter of a light wave carrier, such as phase, amplitude, frequency, polarization, or position as it propagates through the device.

Comparing two modulators, the AO modulator has many advantages on intensity modulation that include low drive power, high extinction ratio, insensitivity to temperature change, simple drive electronics, and high safety factors. However, the EO modulator can give some other information, such as phase and polarization. With the property of phase and polarization modulation, many scientific measurements become possible, such as solar magnetography described below.

3.4.2 Solar Magnetography

The measurement of solar magnetography is a good example to demonstrate how the correlated readout method can be used to some special passive imaging for improving the image quality. To image solar magnetic field by measuring its Zeeman effect, current imaging technology of solar magnetography (as shown in Figure 3.14) is to take thousands of frames by a general-purposed focal plane array, and then reveal the image by off-chip signal processing. An electro-optical modulator is used to select the polarization of the light for detection.

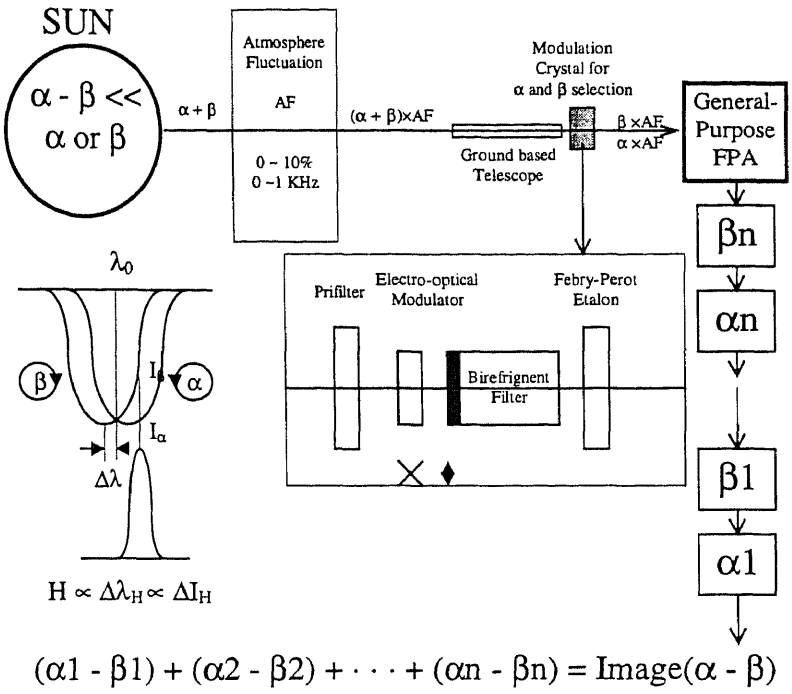


Figure 3.14 Scenario of solar magnetography.

A particular difficulty of this measurement is that the useful image signal (α-β), which is the difference of two circularly polarized light signals (α and β) due to Zeeman splitting, is orders weaker than primary intensities: (α-β) << α or β. In addition, since this measurement is performed by using a ground-based telescope, an atmospheric turbulence may cause a transmittance fluctuation so that all the light signals may vary as large as 10 percent in magnitude with the frequency as high as 1 Khz. As can be seen, this detection condition is equivalent to a very large background with a large low frequency noise superimposed on it, although the detector dark current is very small because the wavelength is near infrared or visible.

In existing imaging strategy, small SNR problem is approached by taking the average of a large amount of frames, and the atmospheric transmittance problem is solved by consecutively switching different circularly polarized light signals (α and β) for

detection. A better signal-to-noise ratio is expected by this strategy since the atmospheric fluctuation fundamentally causes low frequency noise, and it will not change significantly in two frame times. In other words, the noise in two frame times is correlated; therefore, it will be attenuated in a factor.

Although signal and background are from the Sun, since the EO modulator can separate them, this background (β) will be subtracted more effectively if the correlated readout method is used for the measurement. By synchronizing polarization selection with switching control of the readout circuit by a signal generator, the image can be acquired by charging the capacitor with the current due to right circularly polarized light (α) in one phase, and discharging with left circularly polarized light (β) in another phase. The image of α - β can be read out from a correlated focal plane array. The principle of this approach is shown in Figure 3.15.

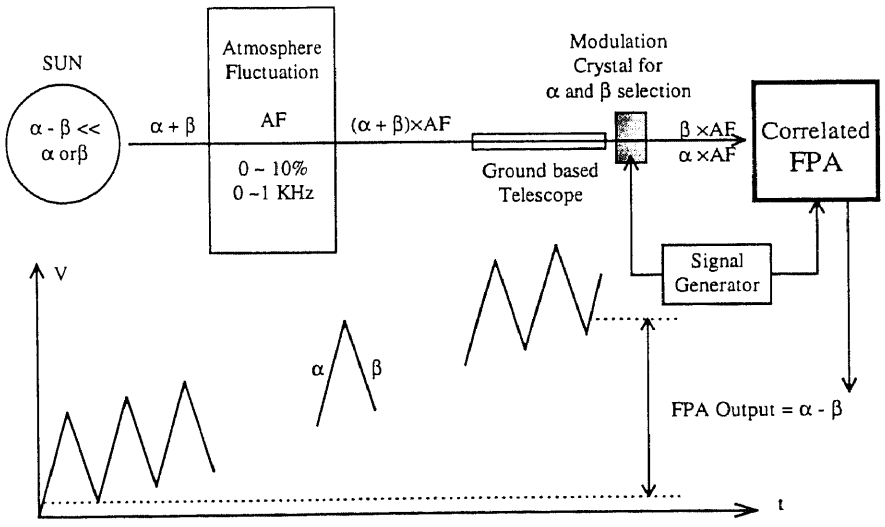


Figure 3.15 Solar magnetography by correlated readout method.

Comparing with the off-chip imaging processing methodology currently used in the measurement of solar magnetograph, main advantages of the correlated method are

threefold. First, it does not need to suffer from the readout noise each time when signal is read out. For a high sensitive detector, readout noise can be very large. Second, an optimized frequency can be used to reduce some particular low frequency noise. For example here, the noise due to atmospheric turbulence which have the frequency up to 1 KHz can be effectively reduced by using 10 KHz of modulation frequency. Last, low bit ADC can be used due to the increasing of output voltage swing. This not only means that the quantization noise is avoided, but also means that on chip ADC may become feasible.

3.4.3 Active Imaging

The capability of on-focal plane array processing by correlated readout method indicates the potential applications of active imaging using external excitation, such as laser radar and microwave radar. The optical modulator becomes not necessary if the excitation light source is modulated. The correlated readout circuit can directly synchronize with the source so that all the radiation not related with the source will be treated as background. A very high sensitivity can be expected.

An evidence detector currently studied for law enforcement can be a good example to illustrate the application of the correlated readout for active imaging. The objective of the evidence detector is to image the illumination of organic material, such as fingerprints, at the crime scene based on most organic molecules absorb light and then emit some of the light as fluorescence. Unfortunately, these fluorescent emissions are normally difficult to detect because various light sources are surrounded. If a FPA with the correlated readout method is used in this detection, an investigator can illuminate the crime scene with a modulated lamp; the background lights will be subtracted if they are

not flash as the same frequency as the light source. With the same idea, one can see that the correlated readout method can found many applications in other field, such as medical research where the image usually is static and is performed in the laboratory.

The capability of on-focal plane array processing by the correlated readout method may also find the applications on information technology. As well known, today's imaging processors demand complex communication input/output networks that are expensive and often unable to handle the required data load. However, on-focal plane array processing applications do not need to process all of the available raw pixel data. To work within the limitations of existing communication system, sensor output bandwidths can be reduced by several orders of magnitude, or more information can be packed into each byte.

In summary, on-chip processing is one of the important future trends in the development of focal plane arrays. The correlated readout method is an approach to process optical information within the pixel. It will not only alleviate the load of off-chip imaging processing but also achieve higher detection sensitivity. Therefore, there will have more applications on scientific research, and commercial product as well.

CHAPTER 4

CORRELATED READOUT CIRCUIT DESIGN IN STANDARD CMOS

4.1 CMOS Design Through MOSIS Service

As the minimum feature size scales down into the submicron regime, the definition of 'standard' CMOS becomes less clear. Usually, the CMOS processes provided by the MOS Implementation System through the Information Sciences Institute at the University of Southern California (MOSIS) are considered as the standard CMOS process [43]. MOSIS is a low cost prototyping and small-volume production service for VLSI circuit development. Several CMOS processes are offered through the access of different foundries, as shown in Table 4.1.

Table 4.1 Current CMOS processes in MOSIS

VENDOR	*FEATURE SIZE (μm)*	*PROCESS*	*NOTES*
AMI	0.08	CWL	2-metal, poly cap option (n-well)
AMI	1.20	ABN	5-metal, 1 poly (n-well)
HP	0.25	CMOS07	4-metal, 1-poly (n-well)
HP	0.35	GMOS10QA	3-metal, 1-poly (n-well)
HP	0.50	AMOS14TB	3-metal, 1-poly, linear cap and silicide block options (n-well)
HP	0.80	CMOS26G	2-metal, 2-poly, NPN options (n-well)
Orbit	2.00	SCNA20	2-metal, 2-poly (n-well)

MOSIS can support a variety of CAD tools and libraries, both foundry-specific and vendor-independent. Unfortunately, there is no special tool for readout circuit design. SPICE is still the best tool for simulation of circuit performance. Table 4.2 lists some major SPICE model parameters provided by MOSIS for Orbit 2μm n-well process. The

values in the table are average results from 10 most recent runs. All the model parameters can be found in the simulation program, which is attached in Appendix A.

Since in this research the first correlated readout demo chip was designed using the Orbit SCNA20 process, all the SPICE simulations are based on the MOSFET parameters listed in Table 4.2. The possible advantages to design the correlated readout circuits using other processes will be discussed in chapter 6. As will be shown, the design of readout circuits can not fully take advantage of submicron technology, since each pixel in the array performs mainly analog signal processing rather than simple flip-flop operations as in logic and memory chips. Recent research also showed that standard CMOS technology could not be used for imaging in the deep sub-micron regime without some process modification [44]. Actually, no matter what kind of process is used, the fundamental design issues will remain the same, although HSPICE is believed to be more accurate for predicting the chip performance. Decisions with respect to transimpedance, power dissipation, threshold voltage uniformity, and switching feedthrough will have to be made. As will be shown in later sections, the switching feedthrough is the most important design issue for the correlated readout circuit and it will not be solved by using the submicro process. Other design decisions, such as pixel size, may strongly depend on the minimum feature size of the technology available.

By using the parameters listed in Table 4.2, the basic building blocks (N and P MOSFETs) can be characterized by SPICE simulation. Figure 4.1 gives the results for a N-channel and a P-channel transistor, with L = 4μm and W = 4μm, along with the characterization circuits. In following sections, the most important design issues are studied and the design of the first correlated demo chip is described.

Table 4.2 Major SPICE Model Parameters

Symbol	Name	Description	Value(N)	Value(P)	Units
$2\|\phi_F\|$	PHI	Surface to bulk potential	0.700000	0.700000	V
t_{ox}	TOX	Gate-oxide thickness	3.9900	3.9900	1E-08m
	XJ	Metallurgical junction depth	0.200000	0.200000	1E-06m
	TPG	Type of gate material	1	-1	
V_{T0}	VTO	Zero-bias threshold voltage	0.7905	-0.9003	Volts
	DELTA	Width effect on threshold voltage	3.4630	2.1870	
L_D	LD	Lateral diffusion	2.1350	3.3360	1E-07m
K_P	KP	Transconductance parameter	6.2743	1.7075	1E-05A/V^2
μ_O	UO	Surface mobility	725.7	197.3	cm^2/Vs
	UEXP	Critical field exponent in mobility degradation	1.2910	3.0750	E-01
	UCRIT	Critical field for mobility degradation	1.8587	12.820	E04V/m
	RSH	Sheet resistance of drain & source diffusions	7.3590	6.3330	Ω/sq
γ	GAMMA	Body-effect parameter	0.5585	0.7086	V$^{1/2}$
N_A	NSUB	Substrate doping	7.1180	11.380	1E15/cm^3
	NFS	Fast surface state density	1.9700	5.9920	E11/cm^2
V_{MAX}	VMAX	Maximum carrier drift velocity	0.53840	9.9990	E05m/s
λ	Lambda	Channel-length modulation	3.6900	5.1960	1E-02/V
C_{GDO}	CGDO	Gate-drain overlap capacitance	2.7678	1.9755	E-10F/m
C_{GSO}	CGSO	Gate-source overlap capacitance	2.7670	3.2011	E-10F/m
C_{GBO}	CGBO	Gate-bulk overlap capacitance	3.4784	3.7541	E-10F/m
	CJ	Bottom zero-bias depletion capacitance	1.2324	3.1534	E-04F/cm^2
	MJ	Bulk junction bottom grading coefficient	6.0152	6.1026	E-01F/cm^2
	CJSW	Sidewall zero-bias depletion capacitance	5.5311	4.0364	E-10F/m
	MJSW	Bulk junction sidewall grading coefficient	2.6600	2.1751	E-01F/m
ϕ_B	PB	Bulk junction potential	5.4439	9.0000	E-01V

* Weff = Wdrawn - Delta_W

* The suggested Delta_W(N) is 2.0000E-09 and Delta_W(P) is 2.00E-08

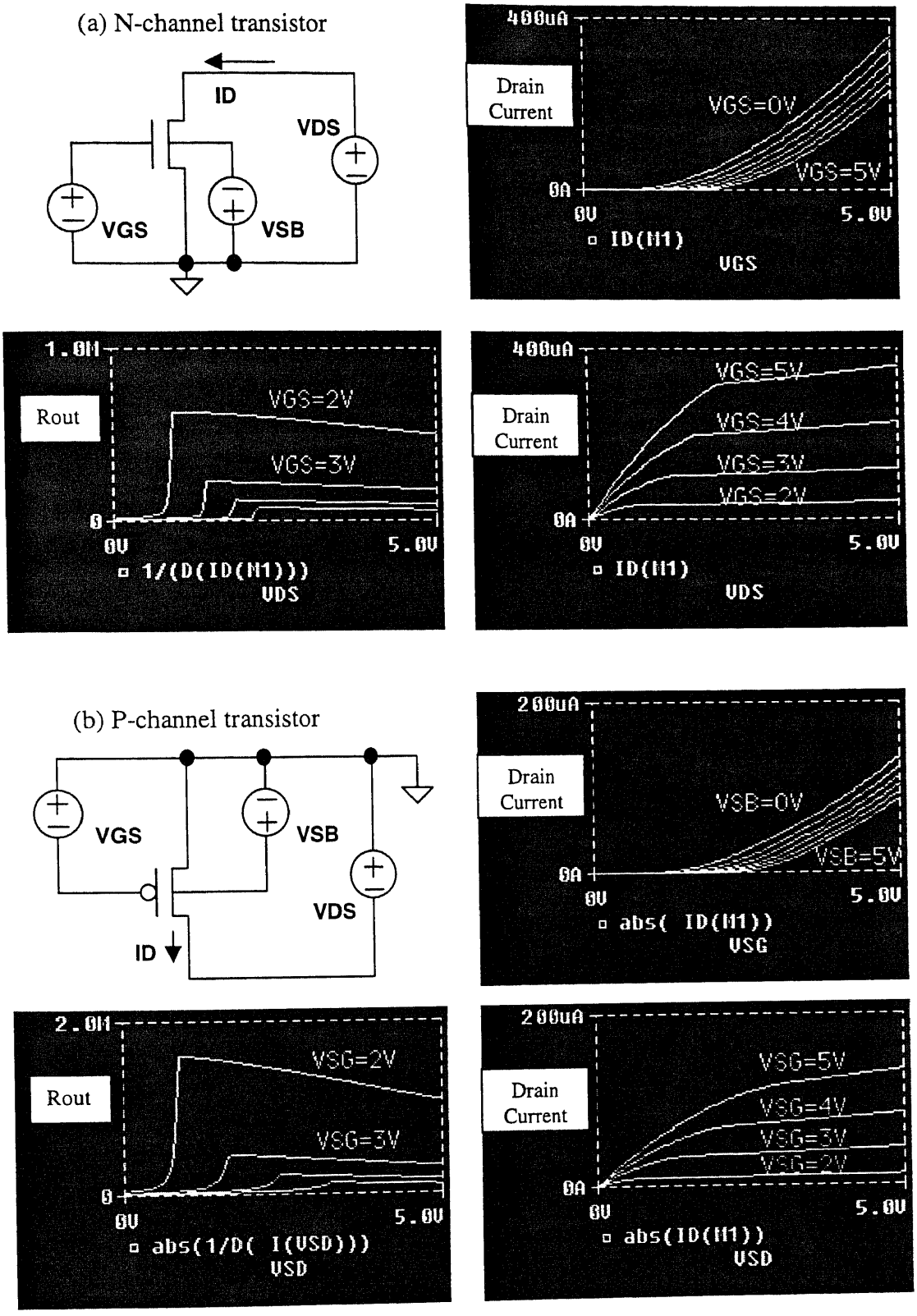


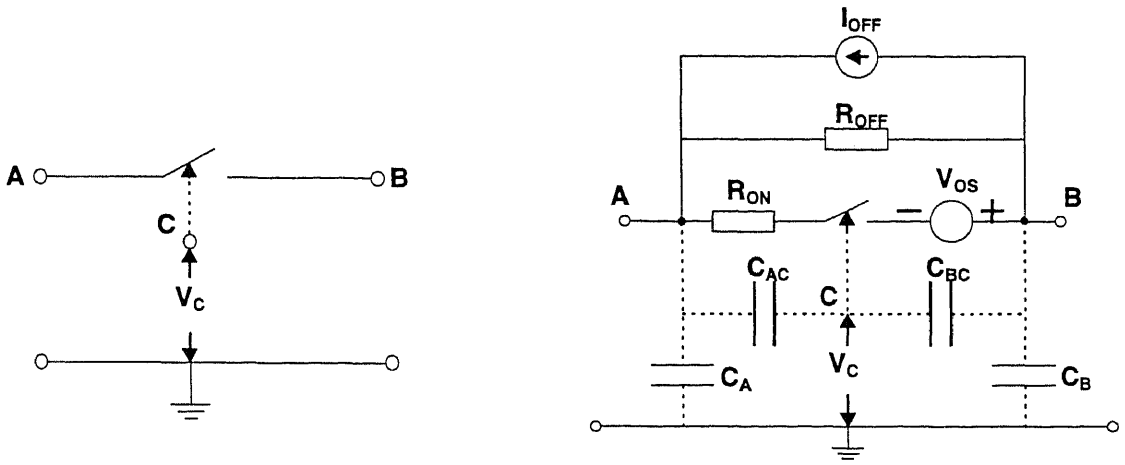
Figure 4.1 Characteristics of MOSFET from Orbit 2μm n-well process with L = 4μm and W= 4μm.

4.2 Switching System Design

The analog signal switch is a basic building block for analog circuits, and plays an important role in CMOS readout circuits for sense node resetting and x-y addressing. In the correlated readout circuit, the switching system formed by analog switches is the heart of the signal demodulation. The success of the correlated readout method strongly depends on the performance of each analog switch. Unfortunately, even with today's state-of-the-art submicron process technology, the MOS switch is still far from ideal because most sub-micron processes are designed for digital circuits. The most important design issues of the switching system will be studied in this section.

4.2.1 Basic MOS Switch Model

Figure 4.2 shows a model for a MOS switch. R_{ON} is a resistor that represents the small but finite resistance between the switch terminals A and B when the switch is on. R_{OFF} represents the large but not infinite resistance when the switch is off. V_{OS} is an independent voltage source to model the offset voltage when the switch is on while the current through it is zero. I_{OFF} is an independent current source to model the offset current when the switch is off while the voltage across the terminal is zero. C_A, C_B and C_{AB} are the parasitic capacitors associated with the switch terminals A and B and ground. C_{AC} and C_{BC} are parasitic capacitances that may exist between the voltage-control terminal C and the switch terminals A and B. Note that in this model some other non-ideal characteristics of the switch such as linearity, commutation time, noise, etc. are not included although they may become the most important issues in practical readout circuit design.



(a) Ideal (b) Nonideal

Figure 4.2 A model of a MOS switch.

For readout circuit applications, R_{ON}, and offset sources as well, are desired to be as small as possible to benefit injection efficiency, while R_{OFF} is as large as possible to reduce leakage current. For example, for a reset MOS switch, small R_{ON} will make it possible to dump charge quickly; large R_{OFF} may improve the saturation level of the integrator, especially in a long integration time application where the problem of leakage from the reset switch is much more serious than usual. However, when design requirements are set and the process is chosen, an optimized switch size can be easily found by simulation if only R_{ON} and R_{OFF} are the considerations. Actually, in most conventional readout circuit designs, the minimum available feature size is usually used for reset and x-y selection simply because of consideration of chip area minimization.

Unfortunately, in the correlated readout circuits designed for this thesis research, a problem of switching feedthrough, which can be due to charge injection and capacitive feedthrough, was found to be a serious problem. Since an integration capacitor is always followed by the switching system, injected charges and feedthrough signals will

accumulate and be presented on the sense node as a noise output. Therefore, a particular challenge in the design of the readout circuitry switching system is the minimization of these noise signals.

4.2.2 Charge Injection and Capacitive Feedthrough

Figure 4.3 shows the basic charge injection effect. When the MOSFET is on and V_{DS} is small, some charges are present under the gate oxide resulting from the inverted channel. When the switch turns off, these charges will be injected into the capacitor and added to V_{in}. For a NMOSFET the charge under the gate can be estimated by

$$Q_{IN} = -C_{ox} \cdot W \cdot L \cdot (V_{GSN} - V_{THN}), \tag{4.1a}$$

and for a PMOSFET the channel charge is

$$Q_{IP} = -C_{ox} \cdot W \cdot L \cdot (V_{GSP} - V_{THP}), \tag{4.1b}$$

where C_{ox} is oxide capacitance and W*L the gate area.

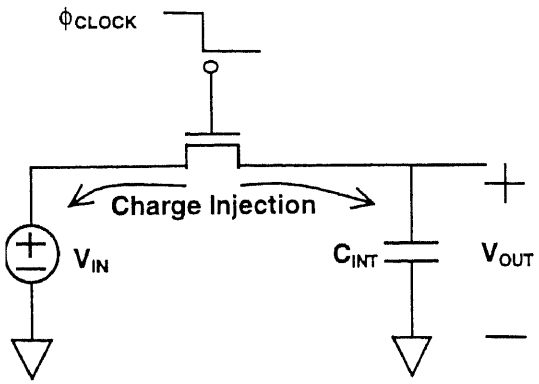


Figure 4.3 Simple configuration using an NMOS to show charge injection.

For the Orbit n-well 2μm process, C_{ox} is given by

$$C_{ox} = \frac{3.97\varepsilon_0}{T_{ox}} = \frac{3.97 \times 8.85 \times 10^{-12}}{3.99 \times 10^{-8}} = 880(aF/\mu m^2).$$

By using the other process parameters listed in Table 4.2: V_{THN} = 0.7905V, V_{THP} = -0.9003V, VDD = 5V, and VSS = 0V, so that V_{GSN} = 5V and V_{GSP} = -5V, the channel charges can be calculated by Equations 4.1 and 4.2. Figure 4.4 gives the calculation results by converting the charge into the number of electrons. The summation of Q_{IN}+Q_{IP} is also plotted in the figure for later reference.

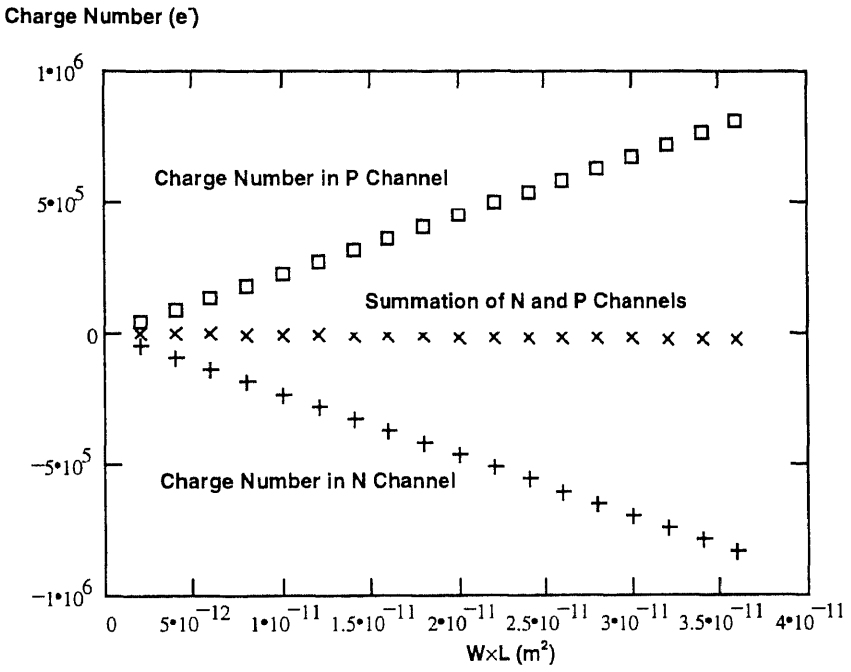


Figure 4.4 The channel charge is calculated with the size of W×L and converted into number of electrons.

It has been shown that if the clock signal turns off fast and the charge distributions are fairly uniform between the adjacent nodes, half of the channel charge will be injected onto C_{int} [45]. If this is true, the injected charge will be in the range of 10^5 electrons, as shown in Figure 4.4. For a readout circuit, this is a very large noise. For example, by applying the principle of random walk, the total noise collected in the integration capacitor will be equal to the square root of the total current integration. This theory can be expressed as (by converting the charge into a number of electrons)

$$e_n = \sqrt{\frac{I \cdot T_{int}}{q}}[e^-], \tag{4.2}$$

where I can be the total current from the detector, which includes the dark current I_d and the signal current I_s, T_{int} the integration time, and q the electron charge. For the detection condition of $I \cong I_d \cong 1nA$, and the integration time of 0.2ms, which is the period of a 5KHz modulation frequency, the number of noise electron becomes

$$e_n = \sqrt{\frac{10^{-9} \times 0.2 \times 10^{-3}}{1.6 \times 10^{-19}}} = 1.12 \times 10^4 [e^-].$$

This noise will increase as the square root of the total integration time, while the charge injection is only a matter of the number of switching times. Therefore, the charge injection is a relatively large noise for the correlated readout circuits.

A simplified model using NMOSFET for the study of capacitive feedthrough is shown in Figure 4.5. During the rising edge of the $\phi 1$ phase, the gate starts at 0 volts and heads toward 5 volts. In the transition from 0 to $V_{in}+V_T$, M1 is off. Consequently, this part of the clock waveform can couple to C_{int} via C_{GS}. As a result, a portion of the clock signal, ϕ, appears across C_{int} as

$$\Delta V_{out} = \left(\frac{C_{GS}}{C_{int} + C_{GS}}\right)(V_{in} + V_T). \tag{4.3}$$

The remainder of the rising clock waveform is not coupled to C_{int} because M1 turns on and connects C_{int} to the low-impedance voltage source V_{in}. If we assume that $C_{GS} = C_{ox}*W*L/2$, $C_{int} >> C_{GS}$ when a relatively large integration capacitor is realized, and $V_{in} << V_T$ for the current mode detection, the capacitive feedthrough can also be expressed by the charge collected in the integration capacitor, which is given by

$$Q_{cf} = C_{\text{int}} \Delta V_{\text{int}} = C_{ox} \cdot W \cdot L \cdot V_T .$$

As can be seen by comparison with Equation 4.1, the capacitive feedthrough has a smaller effect than charge injection, but is in about the same range.

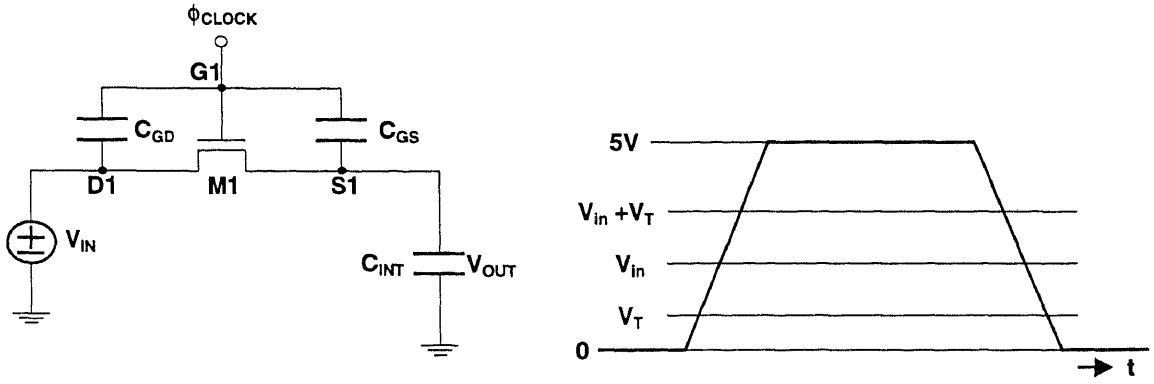


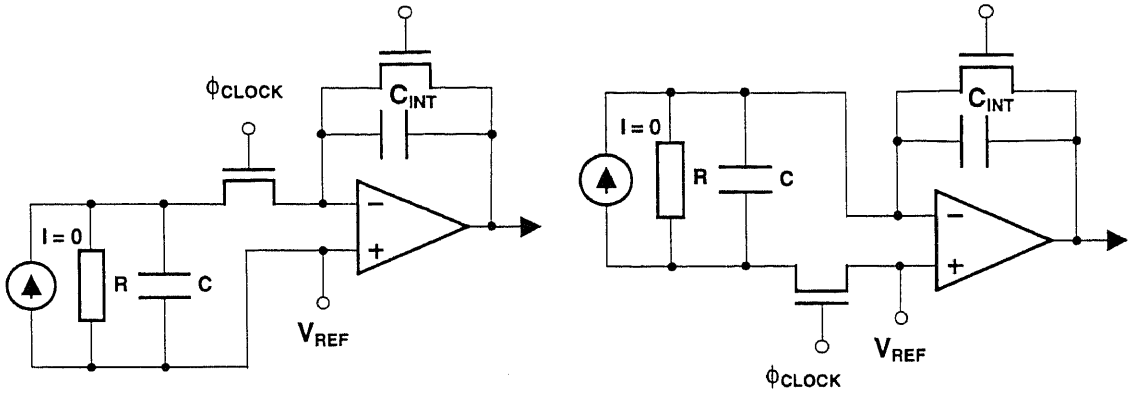
Figure 4.5 Illustration of capacitive feedthrough and the clock waveform.

When M1 turns off, the feedthrough occurs once again as the clock goes from $V_{in}+V_T$ to zero volts. If the voltage change due to the on transition still remains on the integrator, ideally the feedthrough due to the off transition will cancel it out if the switching process is completely symmetric. However, if the feedthrough effect due to the on transition is discharged through the low impedance voltage source V_{in}, the feedthrough result in a complete clock period will be the voltage change expressed by equation 4.3.

4.2.3 SPICE Simulation of the Switching Feedthrough

Although the switching feedthrough had been extensively studied for sample and hold circuits [46], only the effect due to the off transition was considered because the low impedance voltage source V_{in} makes the switching feedthrough during the on transition have a negligible effect on the capacitor. However, in the correlated readout circuits, the feedthrough events will happen many times during one frame integration. In the SPICE

simulation, the switching feedthrough is observed twice in each clock phase, and the accumulation of charge on the integration capacitor is seem to contribute to the voltage output. Figure 4.6 shows the conventional CTIA circuit schematics used to study the effect of switching feedthrough. The feedthrough from the positive Op Amp input is also considered because in the correlated CTIA configuration the switches are also connected to the positive input node.



(a) The circuit schematic for the study of the effect of the switching feedthrough from inverting input.

(b) The circuit schematic for the study of the effect of the switching feedthrough from noninverting input.

Figure 4.6 Circuit model used to simulate switching feedthrough on CTIA.

Figure 4.7 shows the basic effect of the switching feedthrough on conventional CTIA. In this simulation, the switch sizes were W = L = 2μm for all N and P transistors, the integration capacitor was 5pF, the amplifier for the CTIA was an ideal operational amplifier, and the rise and fall times of the clock signals were 200ps. Additional simulations showed that the factors that can significantly affect the influence of the switching feedthrough include:

- Switch configuration – transistor channel and size;

- Clock frequency – number of cycles in the total integration period and rise/fall times of the clock signal;
- CTIA – amplifier open loop gain and total feedback capacitance;
- Detector characteristics – junction capacitance and dynamic resistance.

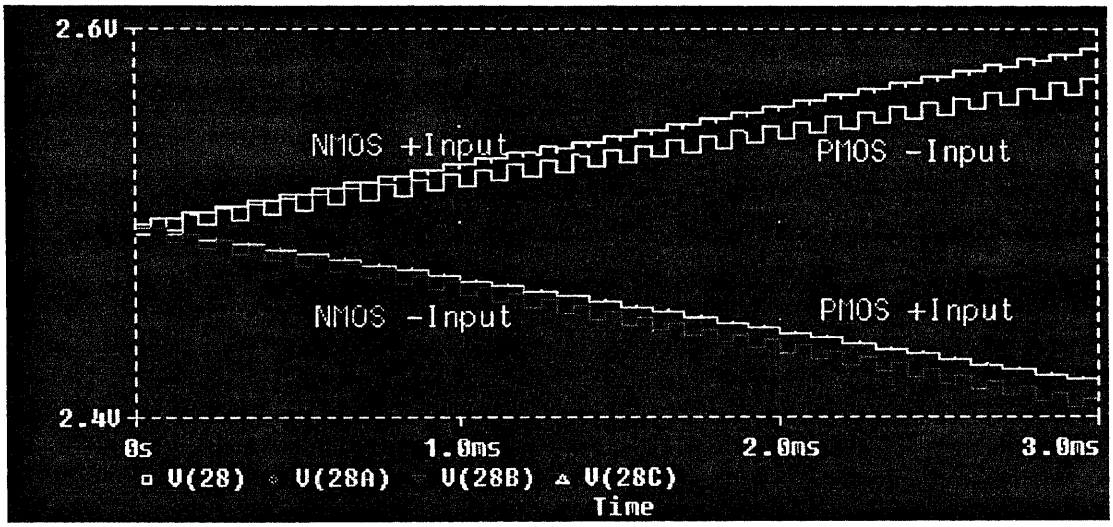


Figure 4.7 PSpice simulation of the effect of switching feedthrough on CTIA.

From Figure 4.7, one can see that the P channel transistor feedthrough has the opposite effect on the output than the N channel transistor feedthrough, as can be expected because the gate-drain voltages have opposite polarities. It also has a somewhat smaller effect than the N channel transistor most probably because the PMOS has a smaller C_{GS} since the lateral diffusion during the P+ doping step for the source and drain is larger. However, this can not lead to the conclusion that the PMOS switch will be the better choice for correlated readout circuits, since in n-well process for the PMOS transistors will consume more layout area, which is often the dominant factor in readout design. Another straightforward simulation result was that smaller W×L fundamentally

had smaller feedthrough simply because of smaller C_{GS} and C_{GD}. However, the effect of transistor size is not shown in Figure 4.7 although it is easy to demonstrate.

In the simulation by changing the switching strategy, two effects were observed. First, for a fixed integration time, a high modulation frequency would result in large total feedthrough accumulation because of the larger number of feedthrough cycles. This means that to use high modulation frequency for resolving small signal from large dark currents will be also limited by the switching feedthrough. However, if the detection condition is not very critical, it is still possible to use high modulation frequency if a large low frequency noise is the problem. The second important result is that the rise and fall time of the clock signal could affect the feedthrough significantly. Theoretically, this is because charge injection will decrease with decreasing dV/dt when the switch transition time becomes long.

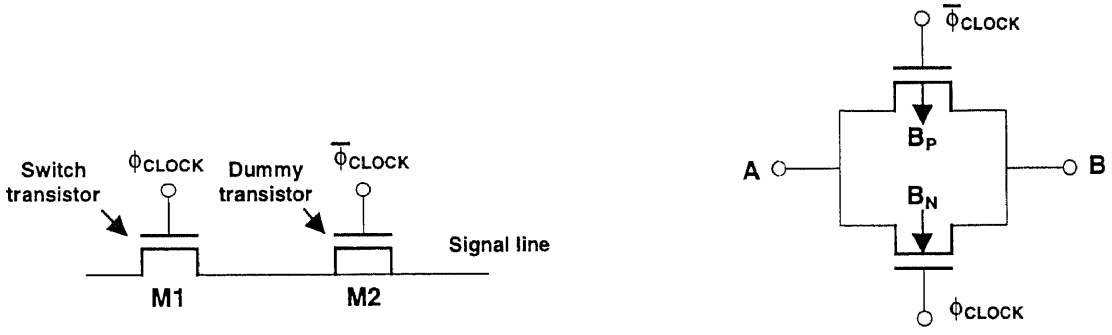
The effect of CTIA on the switching feedthrough is complicated because it involves many CTIA specifications and the strategy for canceling charge injection and capacitive feedthrough, which will be discussed later in the next section. The capacitance and resistance of the detector also affect the result significantly, which could be shown by changing their values and examining the simulation results. However, since the simulation is not based on the specifications of real photon detector, those results would be only helpful for comprehension of the effect but not for selecting the design approach.

Finally, the simulations, as well as the calculation of the charge injection and capacitive feedthrough, showed that the switching feedthrough could be reduced through circuit design. Although the theory of switching feedthrough on the correlated readout

circuits was not well established, the SPICE simulation results should be accurate enough for starting the circuit design.

4.2.4 Methods for Canceling the Switching Feedthrough

Classical methods for reducing switching feedthrough, a dummy transistor and a CMOS current steering circuit, are shown in Figure 4.8 [46], [47]. The dummy transistor is a MOS transistor that is the same as the switch transistor with source and drain both attached to the signal line and the gate connected to the inverse clock. The CMOS current steering circuit, also known as a CMOS transmission switch, is constructed by paralleling P and N channel transistors.



(a) The use of a dummy transistor (b) CMOS current steering circuit

Figure. 4.8 Classical methods for canceling out the switching feedthrough.

The theoretical optimum size of the dummy transistor is one-half of the size of the prime transistor for canceling the charge injection. As shown in Figure 4.8a, when M1 turns off, half the channel charge is injected toward the dummy switch, which is essentially matched by the charge induced by M2, and the overall charge injection is canceled. Unfortunately, the simulation showed that this technique could not be applied to the correlated readout method because the effect of capacitive feedthrough was

increased due to the presence of the dummy transistor. The reason is that the difference of the rise and fall times is accumulated during the integration process, while the dummy transistor is only good for canceling the feedthrough from a single edge of the clock.

The CMOS current steering circuit can diminish both the charge injection and the capacitive feedthrough through cancellation because the two transistors have opposite channel charges and clock signal couplings, as can be seen from Figure 4.4 and 4.7, especially when the transistor areas are carefully chosen. Therefore, the CMOS current steering circuit is the best choice for implementing a switching system if chip area is available. More sophisticated design of CMOS current steering circuit involves three other transistors to control the substrate connection. However, this needs a twin well process that is usually not considered available for FPA technology.

Fully differential circuit topologies can be used to cancel the switching feedthrough effect to the first order, as shown in Figure 4.9. Since the non-ideal charge injection and capacitive feedthrough effects appear as a common-mode signal to the amplifier, they will be reduced by the common mode rejection ratio (CMRR) of the amplifier. The correlated readout circuits fundamentally are in the differential topology. For the twin CTIA, the switching feedthrough is collected in two integration capacitors and they can be cancelled by a differential amplifier after being multiplexed out. The correlated CTIA is a compact circuit. Besides the functions of demodulation and signal integration, it will also perform switching feedthrough reduction if the common-mode rejection ratio of the differential amplifier is high enough, because the switches are connected both to inverting and noninverting inputs.

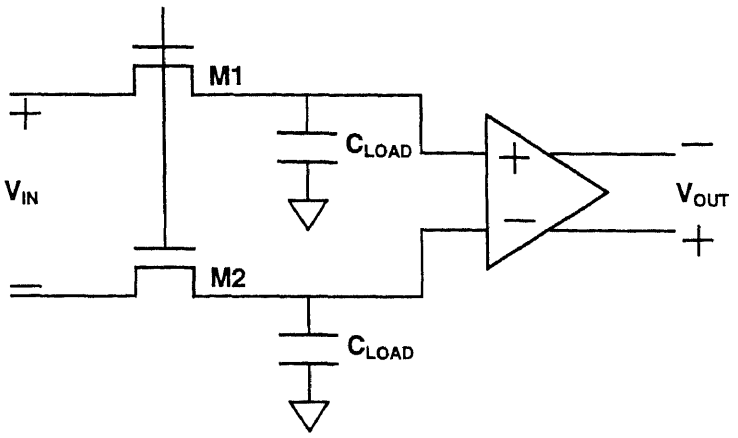


Figure 4.9 Minimization of switching feedthrough by a fully differential circuit.

From the analysis above one can see that using complex switch configurations to cancel switching feedthrough consumes design real estate. However, the sacrifice of chip area can be worthwhile for the twin CTIA because achieving high dynamic range is an important goal. On the other hand, designing an off-array differential amplifier is not very difficult. For the correlated CTIA, minimizing feedthrough inputs will ease the design of the operational amplifier. It may finally result in saving total pixel area.

4.2.5 Noise in the Switches

In addition to unwanted switching feedthrough, switches also generate thermal and flicker noise by themselves. The rms thermal noise current generated by the parasitic drain (R_D), source (R_S), gate (R_G), and substrate (R_B) resistance is given by [43]

$$\sqrt{\overline{i_{RD,S,G,B}^2}} = \sqrt{\frac{4kT}{R_{D,S,G,B}}}.$$

The thermal noise due to the channel effective resistance, modeled by a resistor of $2/(3g_m)$ in the saturation region [43], is given by

$$\sqrt{\overline{i_{therm}^2}} = \sqrt{4kT \cdot \frac{3g_m}{2}} = \sqrt{6kT \cdot \sqrt{2\beta \cdot I_D}} \,. \tag{4.4}$$

The 1/f noise can be modeled by a rms noise source, which is given by [43]

$$\sqrt{\overline{i_{1/f}^2}} = \sqrt{\frac{KF \cdot I_D^{AF}}{f \cdot C_{ox}^{'} \cdot L^2}}, \tag{4.5}$$

where KF is the flicker noise coefficient with a typical value of $10^{-25}V^2F$, I_D is the DC drain current, AF is the flicker noise exponent which has a value ranging from 0.5 to 2, and f is the frequency variable to integrate over. A complete noise model for the MOSFET is shown in Figure 4.10. All noise sources are rms.

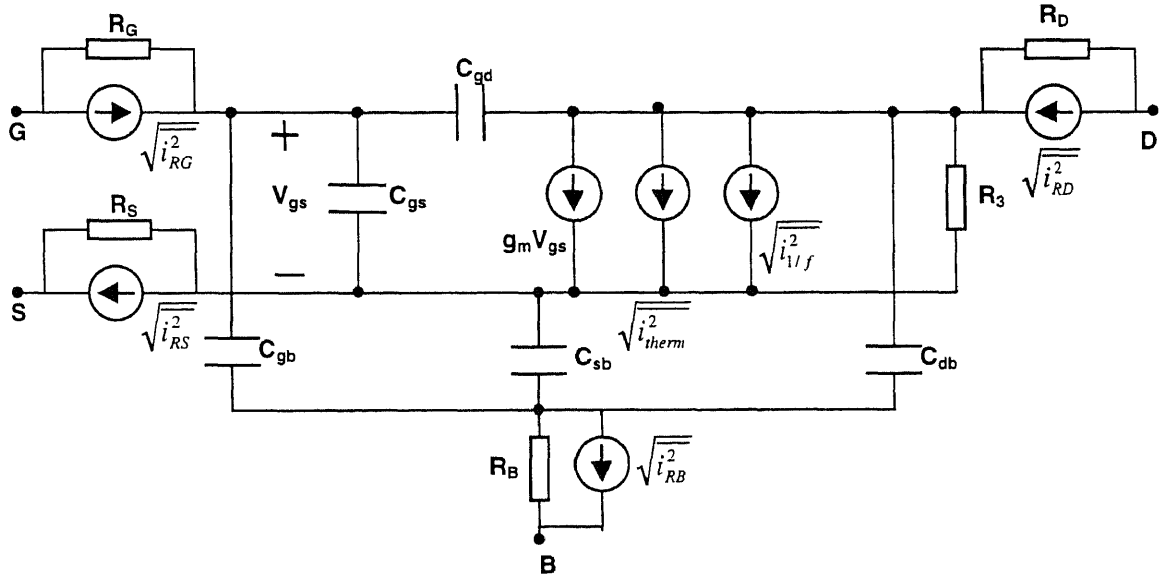
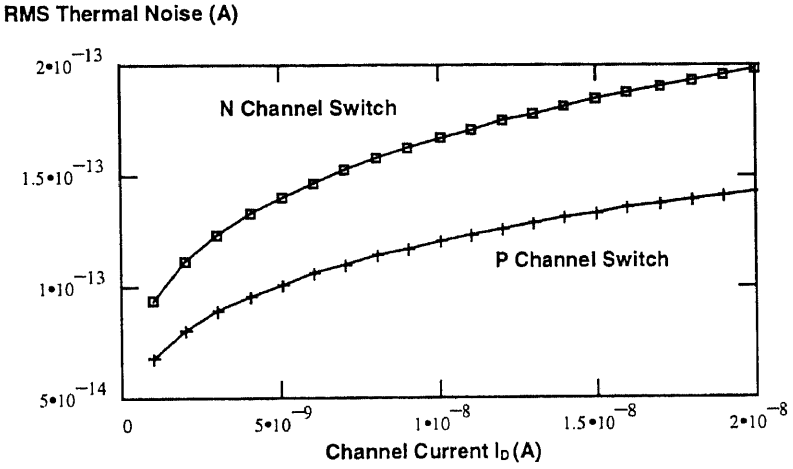


Figure 4.10 Noise model for MOSFET.

Usually, the thermal noise effects due to the parasitic resistance are negligible for CMOS circuit design. If this is the case, we can estimate the switch noise by calculating the channel thermal and flicker noise contributions. Figure 4.11a shows the calculated values of thermal noise for N and P channel switches on drain current I_D, varying from 1nA to 20nA; the transistor size is W = L = 4μm, temperature T = 300°K, and the

transconductance parameter $\beta_n = 62.743\mu A/V^2$ and $\beta_p = 17.075\mu A/V^2$ (from Table 4.1). The figure shows that the thermal noise is of the order of 100fA, which is relatively small compared to the I_D. Figure 4.11b shows the calculated value of 1/f noise for I_D = 10nA, KF = $10^{-25}V^2F$, AF = 1.3, and f from 1 to 60 Hz. Low frequency noise can reach 10pA. These results show that the major noise sources due to the switches themselves are still in low frequency range. However, these noise sources can not be reduced by the correlated readout method because they are generated in different switches.

(a)



(b)

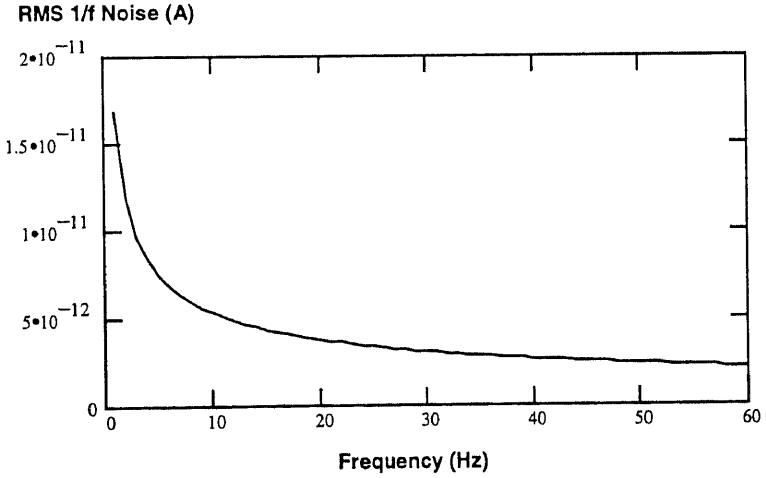


Figure 4.11 Calculation of (a) RMS thermal noise due to the channel effective resistance and (b) RMS 1/f noise in MOS switches.

4.3 The CTIA Design

If the unit cell area is limited, a simple inverting amplifier as shown in Figure 2.7a can be used for a conventional CTIA. However, for the correlated CTIA described in chapter 3.3.1, a differential amplifier is required to realize charging and discharging the same capacitor. In the design of the amplifier, besides the most common specifications such as open-loop gain and frequency response, the common-mode rejection ratio (CMRR) becomes more important than usual due to the requirement for canceling the switching feedthrough. Thus the problems associated with designing a CTIA for the application of the correlated readout method, especially the correlated CTIA, must be studied.

4.3.1 The Transimpedance Amplifier (TIA)

CTIA is a special case of a transimpedance (shunt-shunt feedback) amplifier. Figure 4.12 is an ideal configuration of transimpedance amplifier (TIA) with open-loop gain A_{OL}, feedback factor β, input resistance R_i, and output resistance R_o. In this ideal case, the input resistance of the feedback loop $R_{\beta i}$ is infinite and the output resistance $R_{\beta o}$ is zero. The β network shunts the basic amplifier; therefore, the input variable is a current. Looking into the output of the amplifier, the feedback path is in parallel with or shunts the output signal. Therefore, the output signal is a voltage. The close-loop gain is

$$A_{CL} = \frac{v_o}{i_s} = \frac{A_{OL}}{1 + A_{OL}\beta} \tag{4.6}$$

The input and output impedance of the transimpedance amplifier can be calculated by applying a test current source to the input of the amplifier. Assuming that the β network does not load the basic amplifier, the close-loop input impedance R_{if} becomes

$$R_{if} = \frac{R_i}{1 + A_{OL}\beta}, \tag{4.7a}$$

and output impedance R_{of} is

$$R_{of} = \frac{R_o}{1 + A_{OL}\beta}. \tag{4.7b}$$

The ideal transimpedance amplifier should have zero input resistance and zero output resistance. The above equations show that feedback helps to make the basic amplifier appear to be close to ideal.

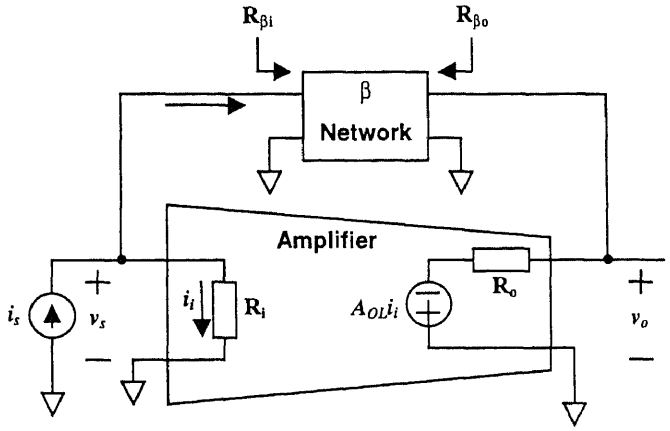


Figure 4.12 An ideal transimpedance (shunt-shunt feedback) amplifier.

The most common application of TIA in sensor preamplifier circuits is to a resistor transimpedance amplifier (RTIA), which is shown in Figure 4.13. The output response of the RTIA to a photon-generated current, or to any input current including noise, is [3]

$$Z_t(f) = \frac{V_{out}}{I_{ph}} = \frac{R_{fb}}{[1 + (2\pi f R_{fb} C_{fb})^2]^{1/2}} \text{ [V/A]}. \tag{4.8}$$

The low-frequency transimpedance Z_t is set by R_{fb}, which is selected to provide sufficient gain to the system and to optimize the signal-to-noise ratio.

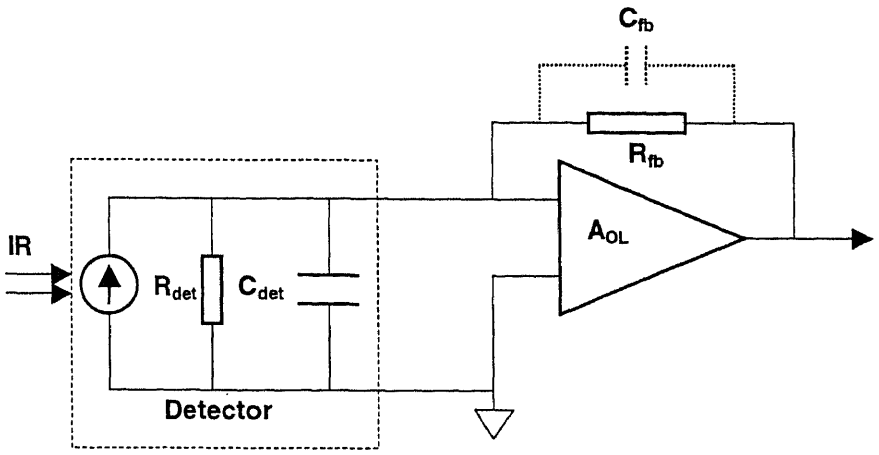


Figure 4.13 Resistor transimpedance amplifier (RTIA).

The CTIA is constructed by replacing R_{fb} with an integration capacitor C_{int} and a reset switch. By applying the theory of switched capacitor, charging the capacitor with a time of T_{int} is equivalent to a resistor with the resistance of

$$R'_{fb} = \frac{T_{\text{int}}}{C_{\text{int}}}, \tag{4.9}$$

if C_{int} is reset before saturation occurs. The transimpedance of such a capacitive TIA becomes

$$Z_t(f) = \frac{V_{out}}{I_{ph}} = \frac{T_{\text{int}}}{C_{\text{int}}} \frac{1}{[1+(2\pi f T_{\text{int}})^2]^{1/2}} \tag{4.10}$$

To ensure that the CTIA possesses the transimpedance expressed by equation 4.10, an amplifier with large enough open-loop gain must be used. This amplifier will determine most of the specifications of the CTIA, since only a capacitor and a reset switch are in the feedback loop. As mentioned at the beginning of this section, an operational amplifier (Op Amp) must be used as the amplifier for the correlated CTIA. The following sections discussed basic design rules for the CMOS Op Amp, which was used in the demo chip design.

4.3.2 Important Specifications of a CMOS Op Amp

A basic CMOS Op Amp that can be fabricated by the n-well process is shown in Figure 4.14. Generally, an Op Amp consists of a differential amplifier with gain A_1, a common source stage with a large gain A_2, and an output buffer [48]. Other configurations are available for various applications, but are considered to be not suitable for the readout circuit design.

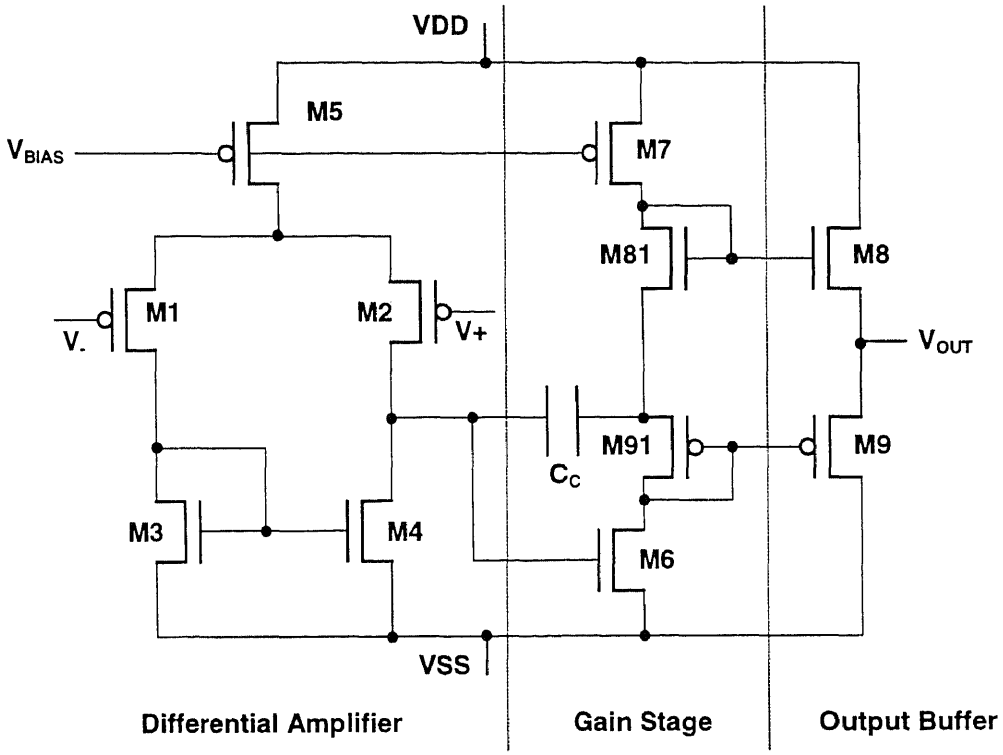


Figure 4.14 A basic CMOS operational amplifier for n-well process.

The general requirements for a CMOS Op Amp include: Open-loop gain, frequency response, settling time, slew rate, common-mode input range (CMR), common mode rejection ratio (CMRR), power dissipation, output voltage swing, output impedance, offset, noise, and layout area. In readout circuit applications, layout area, noise, and power dissipation are much more important than usual. For the correlated

CTIA design, high CMRR is particularly desirable for canceling out the charge injection and the capacitive feedthrough as discussed previously. For the circuits using the twin CTIA configuration, CMRR is only important for the off-array amplifier design.

The common-mode rejection ratio is defined as the magnitude of the ratio of the differential-mode gain to the common-mode gain:

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|.$$

For a basic Op Amp as the one shown in Figure 4.14, the CMRR can be calculated by multiplying the common-mode gain, A_{cm}, of the input differential amplifier by the gain of the second stage and dividing the result into the open-loop gain A_{OL}. The CMRR of an Op Amp in dB is given by

$$CMRR = 20\log(\frac{A_{OL}}{A_{cm}A_2}) = 20\log(\frac{A_1}{A_{cm}}). \tag{4.11}$$

Equation 4.11 shows that the Op Amp CMRR is determined by the differential stage. Figure 4.15 is the circuit to determine the first stage CMRR. The first stage consists of a source coupled pair (M1 and M2) with current source load (M3 and M4). The current source (M5 in Figure 4.14) at the source of M1 and M2 has been replaced with its small-signal output resistance r_{05}. Since the circuit is symmetric and $g_{m3} = g_{m4}$ can be assumed, the common-mode gain is

$$A_{cm} = \frac{V_{out}}{v_c} = -\frac{1}{2g_{m4}r_{05}}. \tag{4.12}$$

Since the difference-mode gain is $A_v = g_{m1}(r_{02}//r_{04})$, the CMRR is given by

$$CMRR = 20\log\left|2g_{m1}g_{m2}(r_{02}//r_{04})r_{05}\right|. \tag{4.13}$$

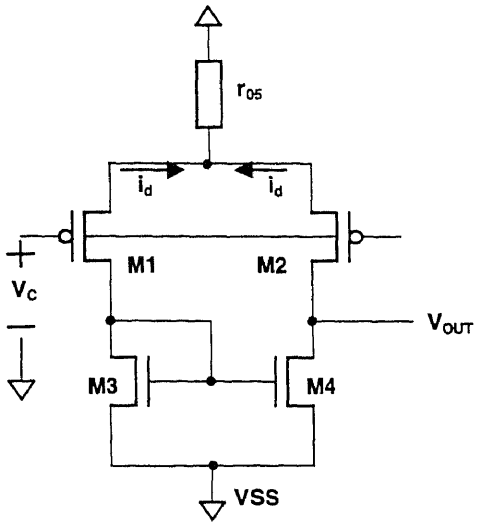


Figure 4.15 A differential amplifier configuration for determining input CMRR.

Equation 4.12 and 4.13 show that the common-mode gain can be decreased, therefore increasing the CMRR, by increasing the output resistance of the current source that connected to the source coupled pair. Therefore, by using a cascode current source, with high output impedance, the CMRR can be greatly increased. The tradeoff results in a more complicated circuit with a larger layout area by at least a factor of 4. This result probably is not feasible for readout circuit design.

4.3.3 The Design of a Two Stage CMOS Op Amp

Although an ideal Op Amp is expected to enhance the FPA performance, two is most probably the largest number of stages that could be used with today's processing technology for the readout circuit design. Figure 4.16 shows a two stage CMOS Op Amp compatible with n-well processing (Orbit technology). The output stage of the Op Amp is not necessary since the source follower in the direct readout architecture (Figure 2.1) will be able to handle the output signal buss with some parasitic capacitance. If the differential amplifier can achieve acceptable gain, the second stage should not be used to save area

and ease the pixel design. Whatsoever, when the circuit configuration is chosen and the Op Amp specifications set, the design of a CMOS Op Amp would involve the selection of the bias current, a selection of device sizes, and the compensation of the amplifier. SPICE simulation could be used to fine-tune the design.

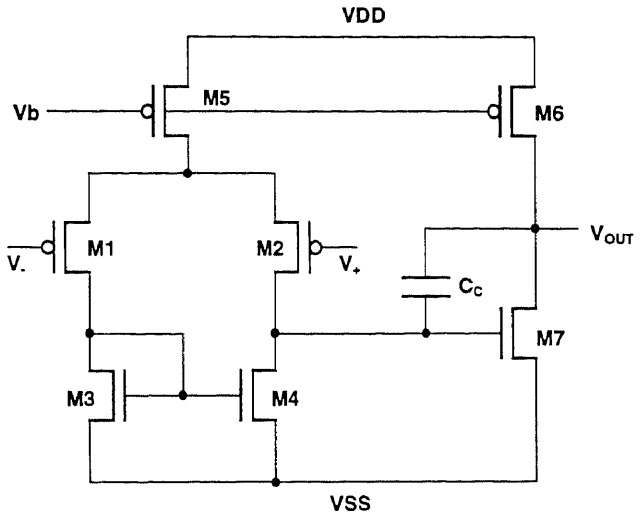


Figure 4.16 A two stage CMOS Op Amp can be at most applied to pixel design because of area and circuitry complexity considerations.

Figure 4.17 shows the small signal model of the Op Amp that was shown in Figure 4.16. The value of R_I, R_{II}, C_I, and C_{II} in Figure 4.17b are give as

$$R_I = r_{ds2} \,//\, r_{ds4} \tag{4.14}$$

$$R_{II} = r_{ds6} \,//\, r_{ds7} \tag{4.15}$$

$$C_I = C_{gd2} + C_{gd4} + C_{gs5} + C_{gd2} + C_{db4} \tag{4.16}$$

and

$$C_{II} = C_{gd6} + C_{db7} + C_{db6} + C_L \tag{4.17}$$

The key equations pertaining to the design are given as

$$A_{OL} = g_{mI}\, g_{mII}\, R_I R_{II} = \frac{g_{m1} g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}$$

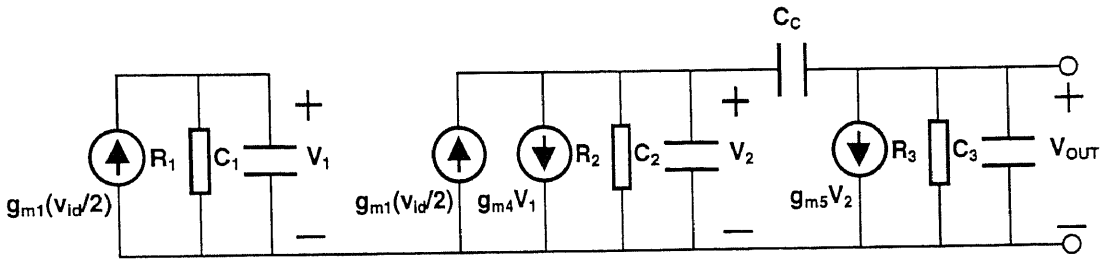
$$= [(\frac{1}{\lambda_2 + \lambda_4})(\frac{2K_P' W_1}{I_{D1} L_1})^{1/2}][(\frac{1}{\lambda_6 + \lambda_7})(\frac{2K_N' W_5}{I_{D6} L_6})^{1/2}]$$

$$\cong \frac{1}{2\lambda^2}(\frac{K_P' K_N' W_1 W_6}{I_{D1} I_{D6} L_1 I_6})^{1/2}, \tag{4.18}$$

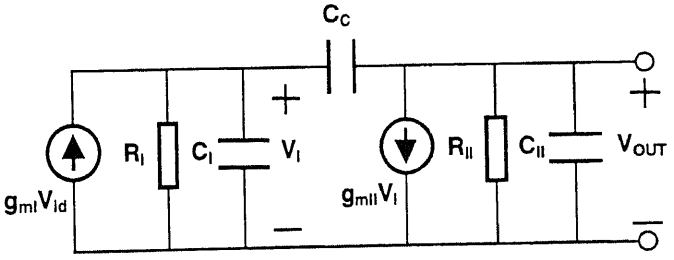
$$GB = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{1}{C_c}(\frac{2K_P' W_1 I_{D1}}{L_1})^{1/2}, \tag{4.19}$$

and

$$\frac{g_{mII}}{g_{mI}} = \frac{g_{m6}}{g_{m1}} = \frac{K_P' I_{D1}(W_1 / L_1)}{K_N' I_{D5}(W_5 / L_5)}. \tag{4.20}$$



(a)



(b)

Figure 4.17 (a) Small signal model of a two stage Op Amp, (b) Simplified model of (a).

Equations 4.18 through 4.20 reveal that the performance of the CMOS Op Amp is dependent on the geometry of the devices. This gives more freedom to meet the specifications of the design. However, the constraint is to ensure that all MOS devices operate in saturation with wide variations in processing parameters. For matching and

symmetry, there must have $W_1/L_1 = W_2/L_2$ and $W_3/L_3 = W_4/L_4$. By the following relationship

$$\frac{W_3}{L_3} = \frac{W_6}{L_6}(\frac{I_3}{I_6}), \tag{4.21}$$

V_{GS3} will be equal to V_{GS5}. Then since $I_6 = I_7$, $I_3 = I_4$, and W3/L3 = W4/L4, the above expression becomes

$$\frac{W_4}{L_4} = \frac{W6}{L_6}(\frac{L_4}{L_7}). \tag{4.22}$$

Because $I_4 = 0.5I_5$, the condition for M4 to remain in saturation becomes

$$\frac{W_4}{L_4} = \frac{(W_6 / L_6)}{2}(\frac{W_5 / L_5}{W_7 / L_7}) = \frac{(W_6 / L_6)}{2}(\frac{I_5}{I_7}). \tag{4.23}$$

The selection of the differential amplifier biasing current is determined by gain, CMR, CMRR, power dissipation, noise, matching consideration and slew rate. It would be an iterative process through adjusting V_b and the size of M5 for meeting those characteristics. In general, the larger the W/L ratio of M1 and M2 in the differential pair at a given biasing current, the higher the gain will be. The drawbacks are increased layout area and parasitic capacitance.

The biasing current of an amplifier stage is determined by the same considerations above. Open loop gain is the major driver of the design. As shown in equation 4.18, the larger the W/L ratio of M6, the higher the open loop gain with fixed biasing current will be. However, the gain of this stage is not helpful for the CMRR, which is particularly important in the correlated readout circuit.

Compensation of the Op Amp by capacitor Cc is used for stability and phase response by avoiding two poles at $-1/(R_IC_I)$ and $-1/(R_{II}C_{II})$. The basic constraint is Cc >

$0.22C_L$ where C_L is the load capacitance [46]. As mentioned before, the load of each pixel will be a common signal line with small parasitic capacitance. Because of two additional considerations that correlated readout will be working in the low frequency range and that there is a relatively large integration capacitor in the feedback loop, compensation for this application is not a major concern.

4.4 A 16×16 Demo Chip Design

To experimentally study the correlated readout method, a 16×16 demo chip was designed for fabrication by the Orbit 2μm n-well process. In this demo chip design, all the transistor sizes were determined by PSpice simulation based on the theory described previously. The layout of the chip was drawn using Mentor Graphic 8.2 and a Sun Work Station.

4.4.1 General Description

The size of the designed demo chip is 2200μm×2000μm with 40 standard MOSIS pins. The circuit schematic of the chip is shown in Figure 4.18. A four input decoder for performing random access in the test was used as column and row shift register. Each pixel of the 16×16 detector array contained a p on n diode and two switches for x and y addressing. The diodes were placed in isolated wells for the correlated CTIA approach. Four different correlated circuits, shown in Figure 4.18, were built in the chip. They were the correlated CTIA (CC), the differential integrator (DI), the twin CTIA (TC), and the correlated direct readout (CDR). The purpose of putting all four circuits on the same chip

was to setup an identical process and test condition, so that the different correlated readout circuits could be compared fairly. Transmission gates were used to connect these circuits with the detector array. Another 3-input decoder was used to select the readout circuit. The switching systems were constructed by CMOS current steering circuits to reduce the switching feedthrough. The input pads were protected by a diode pair and the output pads had no protection.

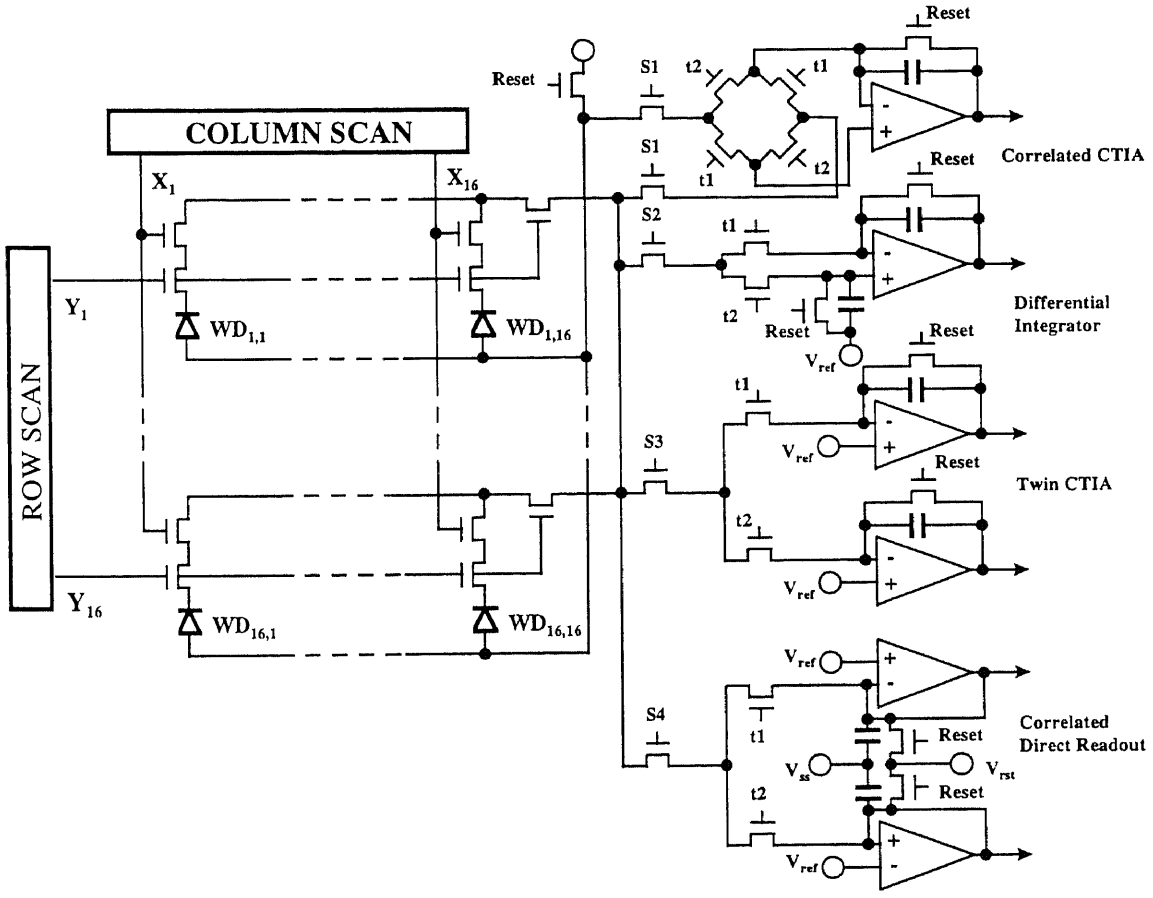


Figure 4.18 The first correlated readout test chip included a 16×16 diode array, four kinds of interface circuits, two 4-input decoders for row and column access, and a transmission gate switching system.

4.4.2 PSpice Simulation

Following the design procedure described in chapter 4.3.3, two groups of device sizes were finally selected from PSpice simulation; they are listed in Table 4.3. The first group was good for performing good open-loop gain and the correlated signal processing function. However, it could only be applied for pixel design if another video amplifier were used on the chip. For driving a load without changing the Op Amp configuration, the transistor sizes of the second stage had to be enlarged. The second group of transistor sizes could be used for such an application.

Table 4.3 Device sizes for a two stage CMOS Op Amp

Device	*M1*	*M2*	*M3*	*M4*	*M5*	*M6*	*M7*
W(μ)/L(μ)	70/4	70/4	30/4	30/4	20/4	160/4	60/4
W(μ)/L(μ)	70/4	70/4	30/4	30/4	20/4	16/4	7/4

Figure 4.19 shows the simulation result for the Op Amp frequency response and its dependency on bias voltage Vb. Both groups of device sizes listed in Table 4.3 could have the same performance if they are not loaded. The open-loop gain reached 67dB (2240) when Vb was 3.24V, and dropped quickly for further increase in the bias voltage. The gain was obtained by calculating the ratio of output voltage to the input voltage. For the simulation shown in Figure 4.19, 1 mV was used as the input voltage and the gain was calculated as V(8)/V(6), which is plotted in the figure. The -3dB frequency was located at 120KHz and was not affected by the change of Vb. As can be seen, this frequency range is sufficient for the correlated readout circuits. In the simulation study of the differential amplifier, the differential-mode gain was found to be about 40 while the common-mode gain was only 10^{-2}, corresponding to a CMRR of 4,000.

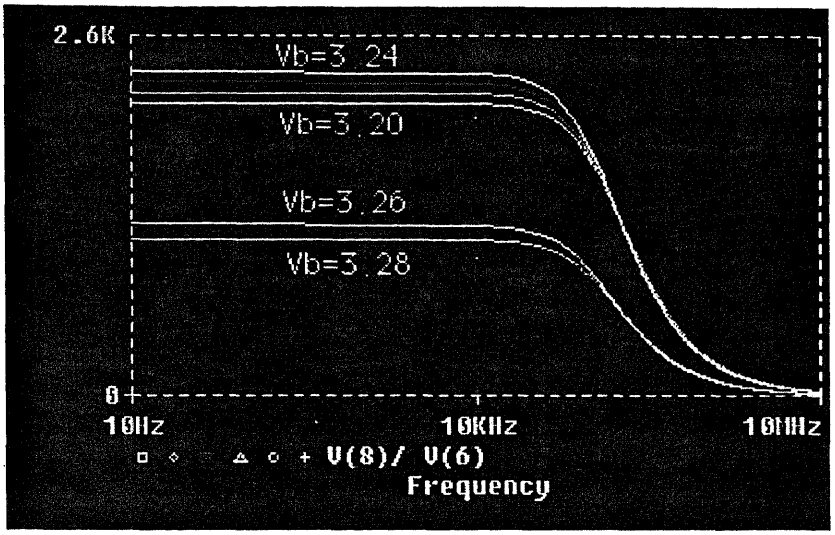


Figure 4.19 The demonstration of Op Amp simulation for frequency response with the change of bias voltage. The open-loop gain was 67dB and -3db frequency was 120KHz.

Figure 4.20a shows the simulation result of a correlated CTIA that is constructed by the Op Amp described above, a 5pF feedback capacitor, and four CMOS switches. The performance of conventional CTIA is also shown in the figure for comparison. In this demonstration, the background was set at 10nA, and the signal was 1nA. The result is near ideal because not only was the condition not critical but also noise was not considered. However, from the result one can see that the conventional CTIA could not be applied for such detection conditions because of its very low output voltage swing. To demonstrate the low frequency noise reduction capability of the correlated CTIA, the simulation was carried out by inputting a low frequency signal, and then studying the output and comparing with conventional CTIA. From Figure 4.20b one can see that the low frequency signal would not lead to a high voltage at the output node of the correlated CTIA, while conventional CTIA might have a large voltage at the output.

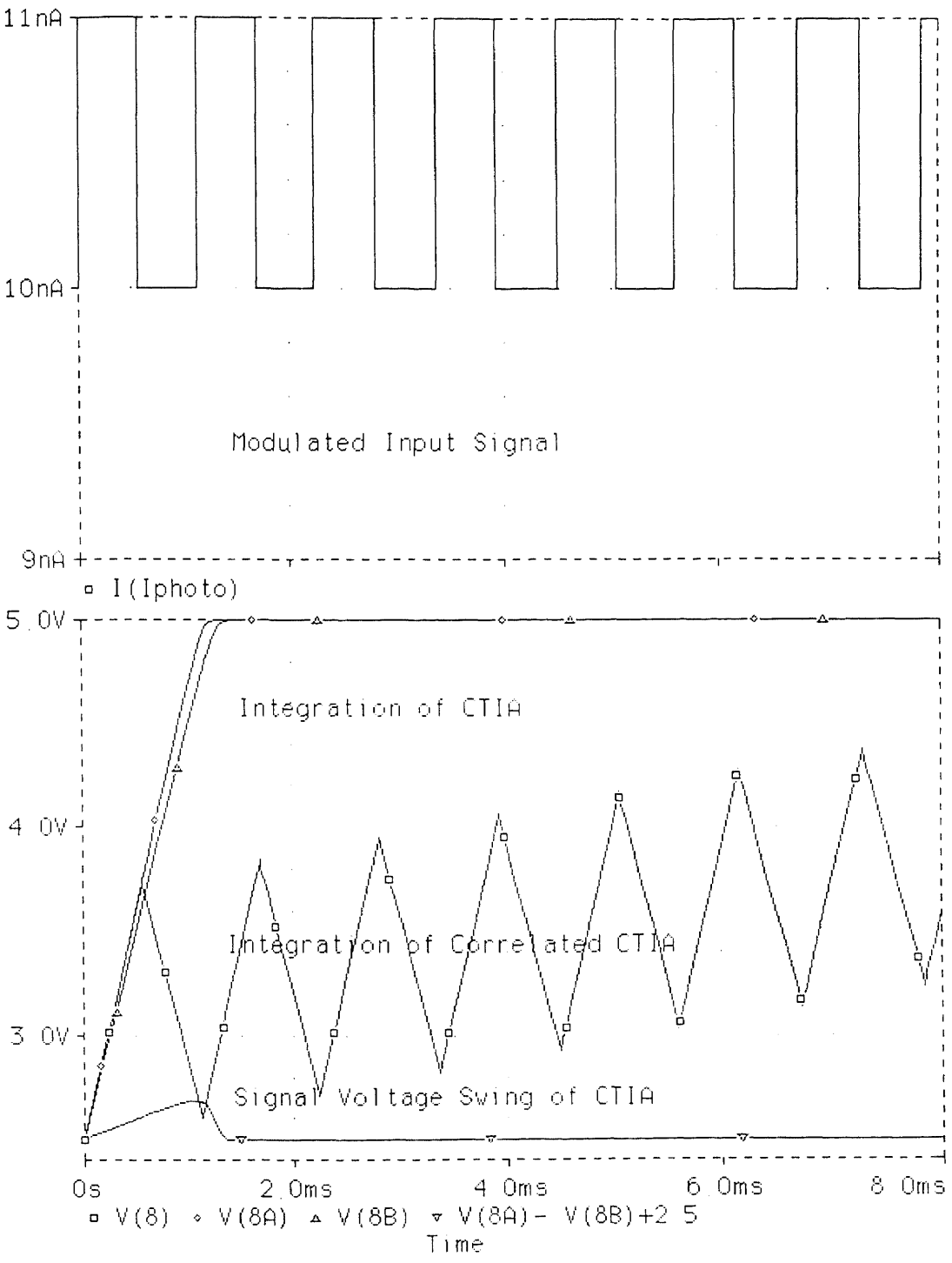


Figure 4.20(a) The increasing in the output voltage swing by the correlated CTIA can be demonstrated by inputting the dark current that is 10 times as large as signal and comparing the result with conventional CTIA. In this simulation, the dark current was 10nA and the signal was 1nA.

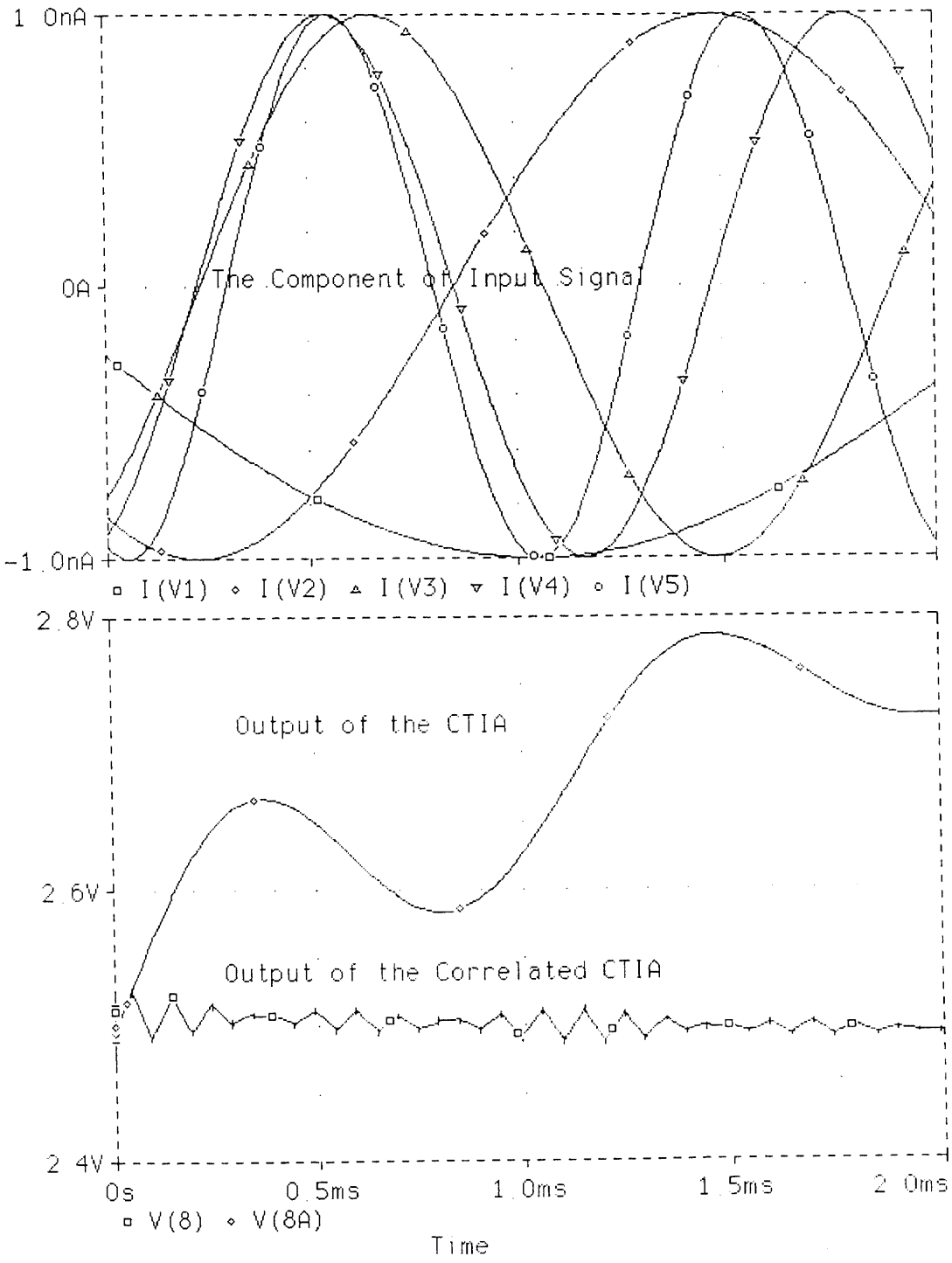


Figure 4.20(b) The noise reduction capability by the correlated CTIA can be demonstrated by inputting ac signals and comparing the result with the conventional CTIA. In this simulation, the input signal is the supposition of five relatively low frequency signals (400 to 1200 Hz) and the modulation signal was set as 10 KHz.

In the simulation of the correlated CTIA, the switching feedthrough was found to be not significant. This was probably because of the CMOS current steering circuit for the switching system and the 4,000 CMRR of the Op Amp minimized this effect, according to the analysis in previous sections. On the other hand, 20nA of dark current is very large compared with the switching feedthrough. However, we can not conclude that this design will meet the requirement because the SPICE model on the effect of charge injection is not clear, especially in the application of photon sensing.

Another important result from the simulation was that the correlated CTIA had a fundamentally lower saturation level than the conventional CTIA. The study showed that this problem might come from the leakage current due to the reset switch. This was proved by increasing the length of the reset switch to improve the saturation level, although it is not practical for the readout circuit design. The last important result was that this correlated CTIA could resolve the signal from the dark current that was about 300 times stronger than the signal. As mentioned above, this result was obtained when noise was not considered.

The chip performance by selecting the correlated CTIA as the signal processing circuit is shown in Figure 4.21. The Pspice program is listed in appendix A. For studying the timing for the correlated readout circuit, the integration results were sampled by a sample-and-hold circuit that was not included in the chip. From the sampling output shown in the Figure 4.21, one can see the expected video output from the correlated CTIA. In addition, the 4-input decoder used for row and column access at the gate and transistor level is shown in Figure 4.22. Since the ratio of the transconductance parameter for N and P MOS is about 3 to 1 as shown in Table 4.2, about the same ratio of W/L for P

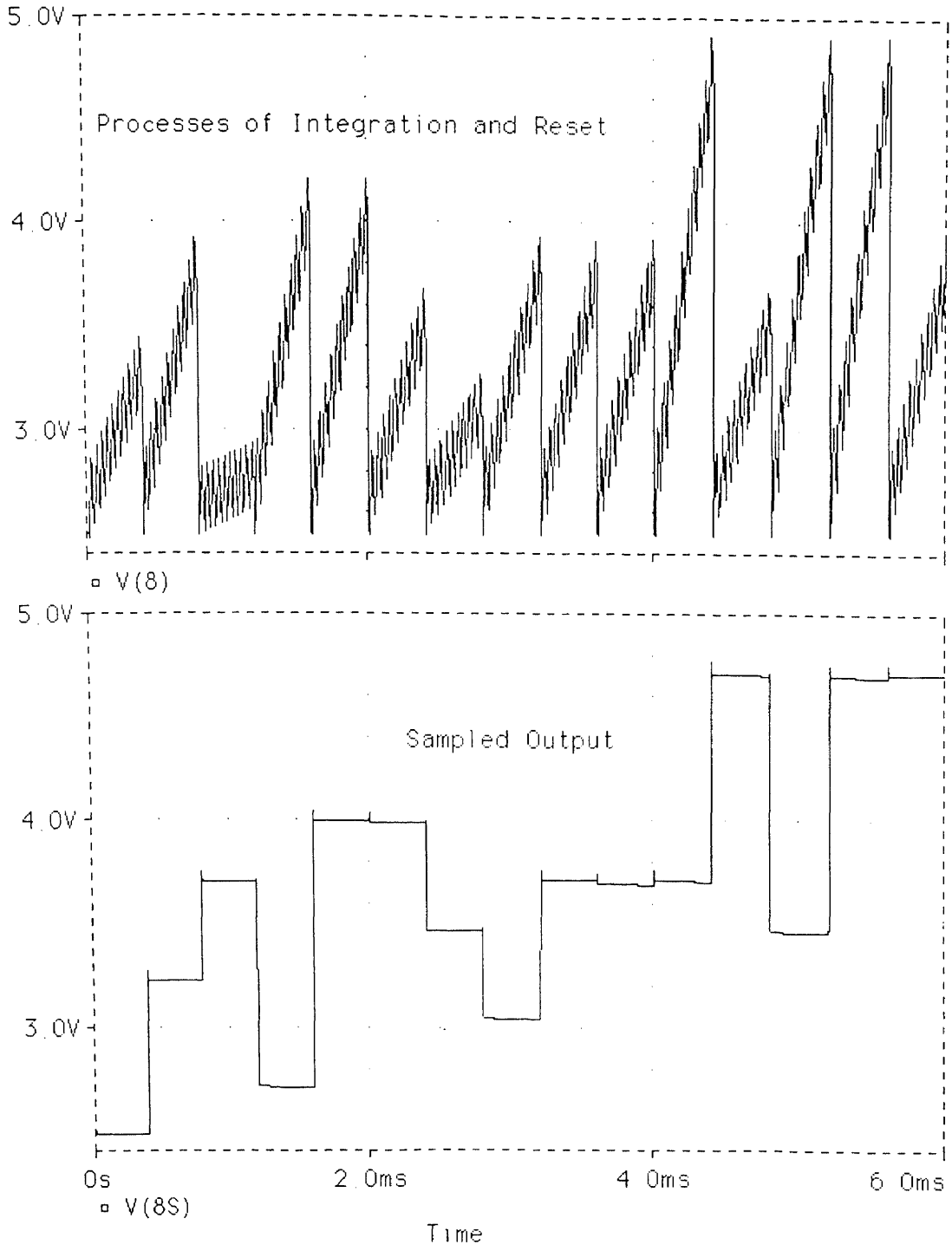


Figure 4. 21 The performance of the first correlated demo chip simulated by Pspice.

and N transistor was chosen to achieve symmetric rise and fall times for the waveforms in this logic circuit.

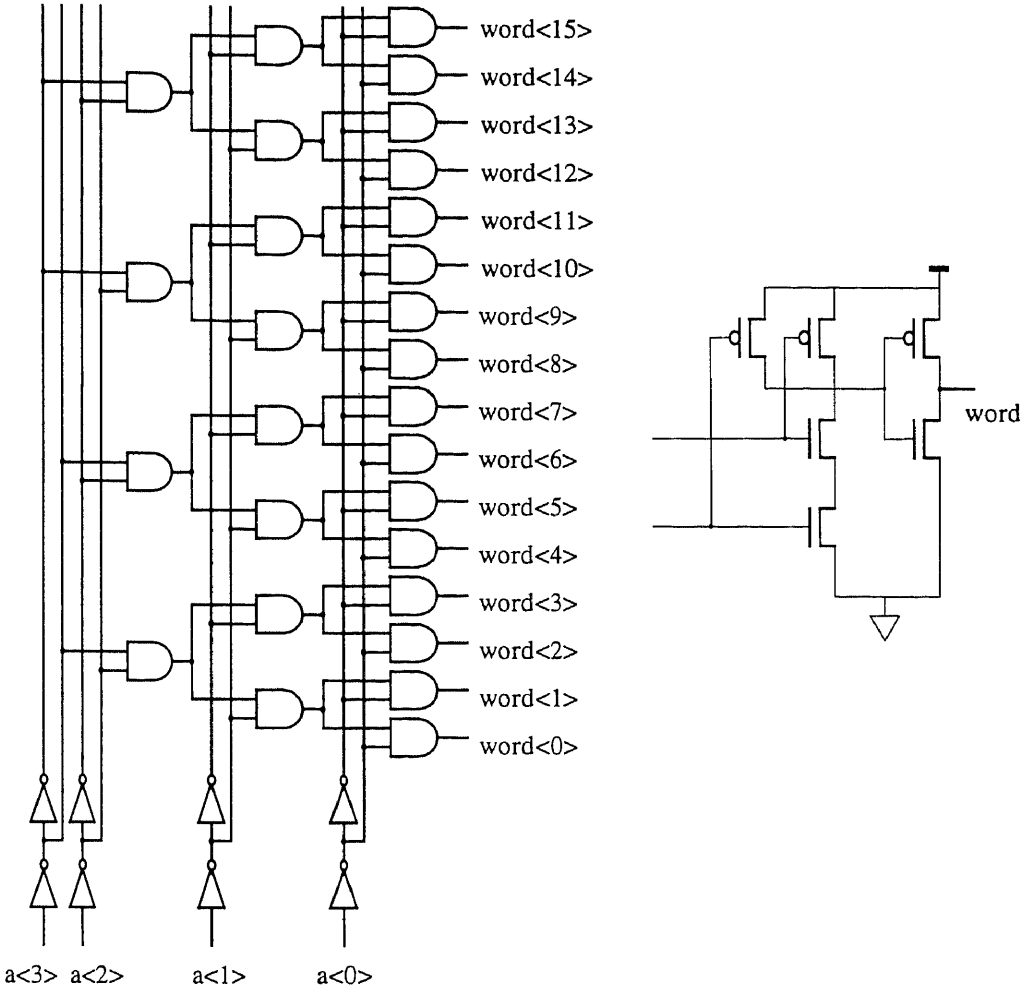


Figure 4.22 (a) The circuit diagram of the 4-input decoder at the gate level and (b) The AND gate in the 4-input decoder

4.4.3 Layout

Figure 4.23 shows the floor plane of the demo chip. The transmission gates that connect the detector array to each interface circuits are not shown in the figure. The mask layout

for fabrication by Orbit 2μm n-well process can be found in Appendix B, along with the layouts for the switching system and the CTIA.

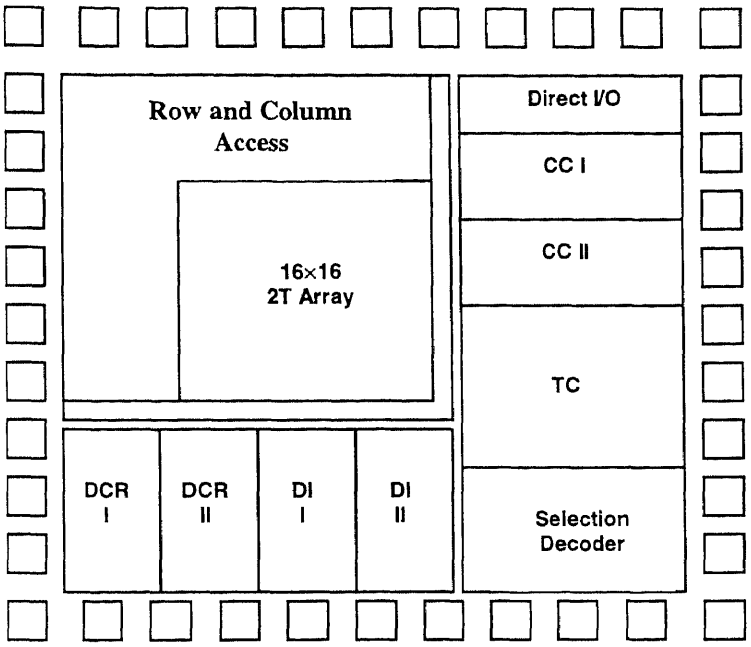


Figure 4.23 Floor plane of the first correlated readout demo chip.

For the layout of such a chip, there were some considerations that resulted in this final version. First, to realize the correlated CTIA, the diode must be placed inside the well. For a n-well process, the P on N diode must be used. If it is not for the correlated CTIA, it is not necessary to fabricate the diode in isolated well. A shared well will not only save the area, but also ease the layout. Next, because the size of the shift register must be matched with the detector array, the automatic layout approach could not be considered, although there were a number of standard unit cells of AND gate. Also, the layout of this 4-input decoder could not be used to build a high input decoder by parallel architecture. Thirdly, since it was too difficult to build a video amplifier on this chip, the signal from the output of each interface circuit was designed to directly output to the test system. Therefore, the first group of sizes listed in Table 4.3 was finally used for a low

output impedance to drive the line capacitance and sampling circuit. Finally, separate power supplies were used for the row and column registers, the digital circuits, and the correlated interface circuits, the analog circuits.

4.5 Summary

In the study of the correlated readout circuits using standard CMOS, the switching feedthrough was found to be the most important issue in the design. Theoretical analysis and SPICE simulation showed that this effect could be very large for most of the detection conditions and must be minimized through circuit design. A CMOS current steering circuit was found to be a better approach than the dummy transistor for reducing the charge injection and capacitive feedthrough at the same time. The price was, of course, increased chip area and increased parasitic capacitance. The differential amplifier topology could further cancel out switching feedthrough by its common-mode-rejection ratio (CMRR). The penalty would be additional consideration of CMRR in the Op Amp design. To balance those requirements with limited real estate and other constraints of the focal plane array becomes the real challenge of the correlated readout circuit design.

The first correlated readout test chip designed was based on the Orbit 2μm n-well process. Four different interface circuits, mainly developed from the conventional CTIA, were built on the chip. The operational amplifier consisted of seven optimized transistors in a two-stage configuration. The open loop gain reached 67dB and the -3 dB frequency was 120 KHz. With the correlated CTIA built by this Op Amp, it was possible to resolve a signal from the background that was 300 times stronger than the signal based on the Pspice simulation, if the noise figure was not considered. The simulation also showed that

with 20nA of dark current the switching feedthrough becomes insignificant. However, the effect of charge injection remains unknown because it is not in the SPICE model. By using the Orbit 2μm n-well technology, this correlated CTIA could at most be realized for a linear array, because the required readout circuit area per pixel was about $200\times300\mu m^2$.

CHAPTER 5

TESTING OF THE CORRELATED READOUT CIRCUITS

5.1 The Experiment Methodologies

Generally, there are two methods for testing the FPA readout circuitry. They are electrical injection and optical injection. The electrical injection method requires a power supply and a resistor network to generate a designed input signal for the readout circuit. It has been employed by others for testing current memory chips [29]. To simulate the multi-quantum well infrared detector by a resistor network, a pulse voltage source and a resistor were used to generate a signal current and a DC bias and another resistor was connected in parallel to generate a background current. The experimental results showed that this method was very successful for testing the readout circuit that was designed for large background subtraction. Most importantly, it could easily give the minimum resolvable signal for a certain dark current level. Unfortunately, the grounding of the power supply was a serious problem for applying this method to the test circuits for correlated CTIA. Battery driven circuitry may solve the grounding problem; however, the required synchronization would be troublesome. From the practical experience of this research, it is believed that the optical injection method, that is using a photo detector as the input circuitry, is the best way to test the correlated readout circuit. Because of optical modulation, there are three ways to realize the optical injection method. They are the passive imaging, active imaging and direct modulation methods. The following describes the concepts for these methods.

Figure 5.1 shows the experimental setup based on passive imaging applications. An optical modulator is placed in front of the focal plane array (FPA) with the correlated

readout circuit, and both the modulator and the FPA are controlled by the same signal generator. To use a visible FPA (which fundamentally has very small dark current) for the study of a correlated readout circuit designed for large dark current applications, a light source could be placed between the modulator and the FPA to simulate dark current. As discussed in chapter 4.4, the mechanical chopper can be replaced by an acousto-optical or an electro-optical modulator for simplifying optical design. However, from the practical experience of this thesis research, such a system should not be used in the beginning stage of the research unless the optical system has been well developed.

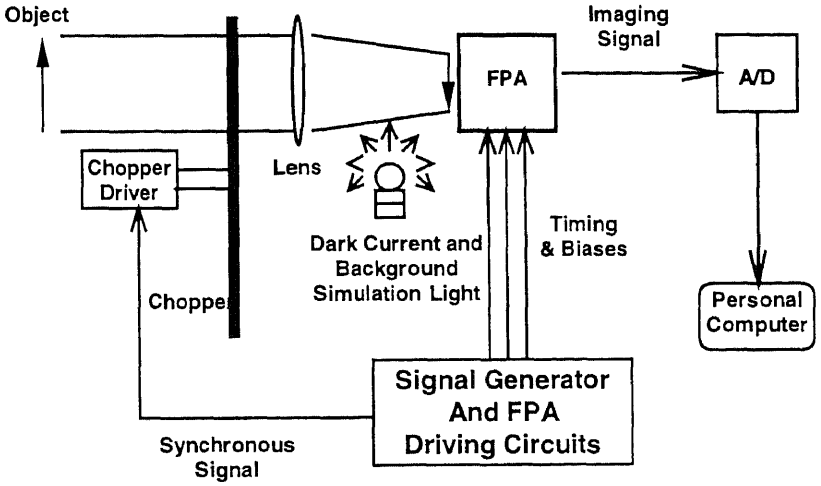


Figure 5.1 In passive imaging applications, the modulation signal will control the optical modulator. Such an approach is not suggested in beginning of the research.

In active imaging applications, the modulation signal will directly control the light source instead of controlling the modulator. The corresponding experimental setup is shown in Figure 5.2. This approach does not need an optical modulator in the detection system so that the optical system is drastically simplified. In addition, the dark current and background simulation light can be placed anywhere around the FPA so that it will ease the experiment operation. However, what kind of excitation source is appropriate for this research remains not clear.

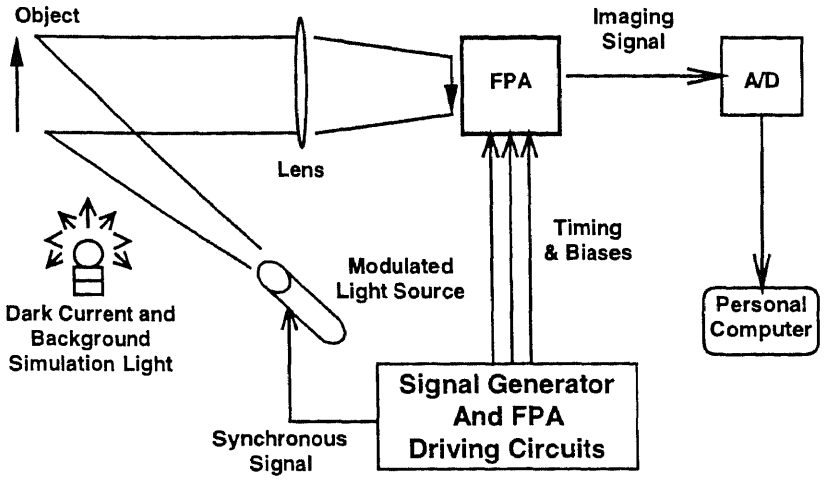


Figure 5.2 In active imaging approach, the modulation signal controls a light source instead of controlling the modulator in front of the FPA.

To test the correlated readout circuits in its beginning stage, the direct modulation method was used and proposed for later research. Figure 5.3 shows the principle of this approach. The control signal directly modulates the object that is a light emitting diode (LED), so that the light from the object is a modulated signal. Any light from the environment will be count as background. An extra light source to simulate the possible background is still applied. With this setup, one can concentrate on the circuits by excluding possible optical effects from any additional optical system.

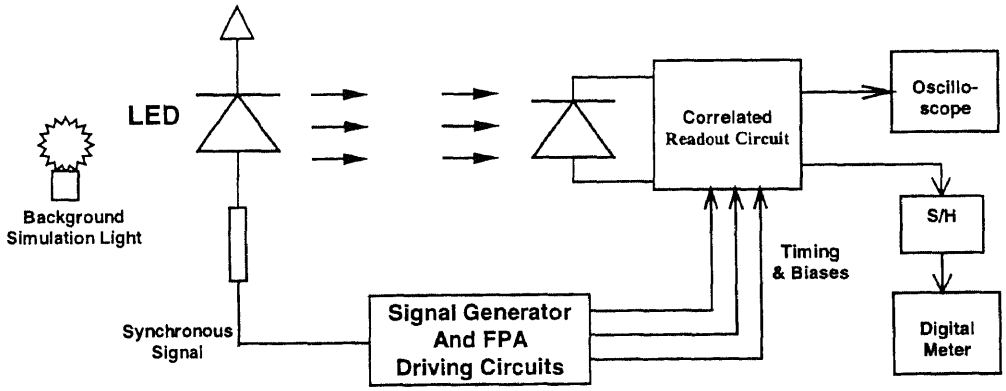


Figure 5.3 A direct modulation method using light emitting diode (LED) as the object was used in this research for the correlated readout circuit characterization.

5.2 Measurement System

A Pulse Instruments product, the 4000 Series Low Noise Focal Plane Array Test System, was used to characterize the correlated readout circuits by providing the important modulation signal as well as the DC biases and timing signal. This system uses a mainframe approach that separates the digital electronics from the bias and drive circuitry, both optically and through the use of separate power sources, so that a very high level of noise immunity can be achieved. It is the best equipment known for the readout circuit test. However, this is the first time it was used for a correlated readout circuit study.

The major output controls are 40460 dual channel driver PC cards and 40750 low noise DC bias PC cards. The 40460 driver PC card consists of two channels of 10MHz drivers. The output voltage capability is ±20V, and the input from the Data Generator is optically isolated. The PC card also contains the circuitry for the programmable rise and fall times, and voltage and current sensing. The 40750 low noise DC bias cards each contain four channels of ±20V DC bias outputs. The bias supplies contain voltage and current sensing, and are floating with respect to the ground of the Control Mainframe.

Figure 5.4 shows the block diagram of the test system based on the PI-4000. It consists of one PI-5800A Data Generator, one PI-4001 Control Mainframe, two PI-4002 Instrument Mainframe, one PI-4007 Preamplifier and one PI-4005 Acquisition Mainframe. All the components are controlled by a Compaq Computer. The PI-5800A and PI-4001 are controlled through an IEEE-488 bus and the PI-4005 is controlled through an EISA/VME bus for increased system speed. The other components are controlled through an internal bus among the instrument. This system can be operated by

programming in a computer or by the soft key on the instrument panel. It can be used to test the focal plane array with a size from 1×1 to 2048×2048 pixels. The data acquisition speed can reach up to 40MHz with 10 bit accuracy, or 10 MHz with 12 bit accuracy, or 2 MHz with 16 bit accuracy. The timing pulses generated by PI-5800A and the video output signal from the readout circuit can be monitored by a Type 454 Oscilloscope.

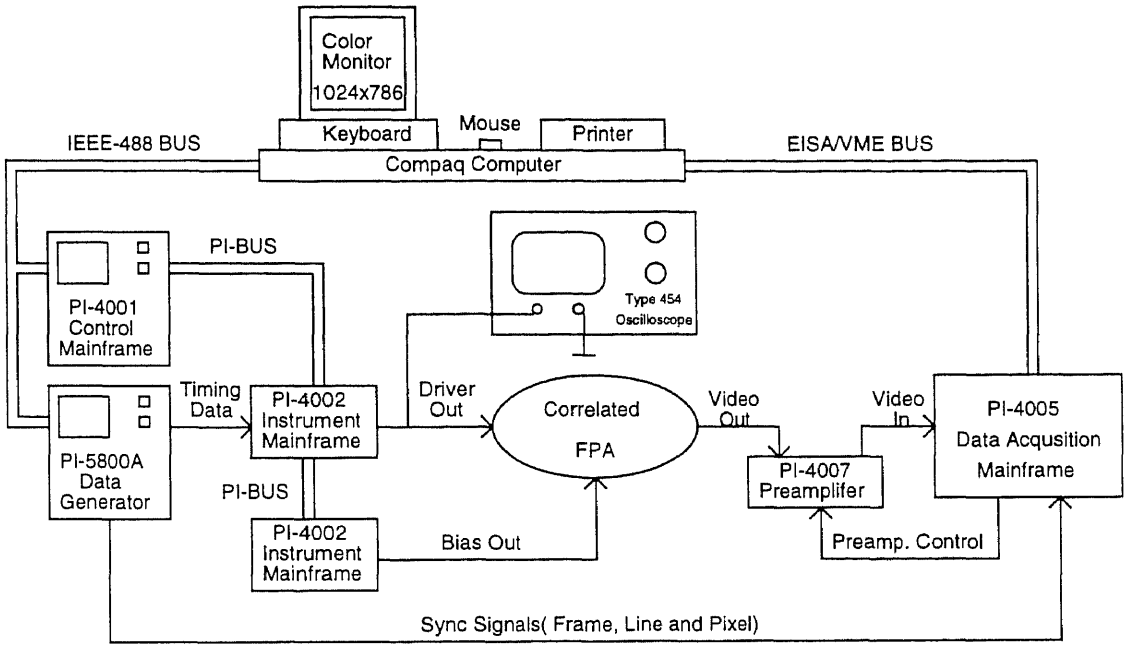


Figure 5.4 The measurement system for the correlated readout circuit is based on a Pulse Instruments System 4000 Series Automated FPA Test System.

To connect the output connector of the PI-5800 Data Generator, the PI Company recommends that all outputs should be wired with a 50ohm coaxial cable and shorter than 4 feet in length. Otherwise, serious signal degradation could occur at high frequencies. A PI cable 88000050 is used in this test system to connect the pulses output from PI-5800A to 40460 Clock Driver of PI-4002 Instrument Mainframe. Figure 5.5 shows its output connections. The cable is a 16-Channel output, 4 feet in length, BNC terminated, and 50ohm coaxial ribbon cable. The same cable is also used as the output of the driver signal to the tested devices with longer length.

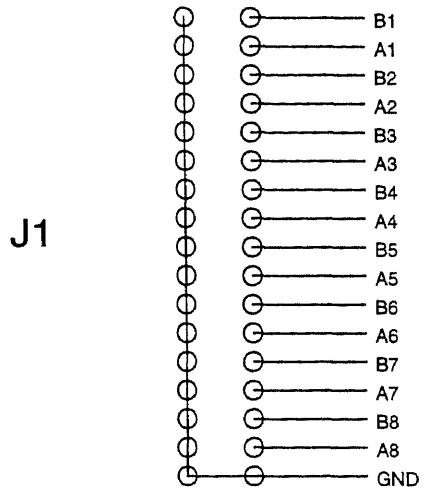


Figure 5.5 Output connector of PI-5800A data generator.

Figure 5.6 is the connection diagram of the input/output connectors of 40460 Clock Driver in PI-4002 Instrument Mainframe. All these input/output connectors are BNCs. The input of the card must be a TTL level and the output polarity is either a normal or inverted output that can be selected either by the front panel or IEEE-488 Bus. Two rows of clock outputs of the card are connected to the other end of PI-88000050 cable.

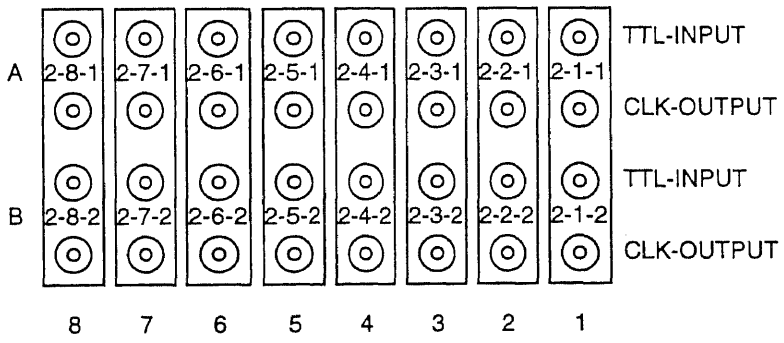


Figure 5.6 Input/output connectors of 40460 clock driver.

Figure 5.7 shows the connection diagram of the output connectors of 40750 bias supply card in PI-4002 Instrument Mainframe. All the output connectors are BNCs. The output voltages of the card are selectable from the front panel control or programmable

via IEEE-488 Bus. In this experimental setup, a PI-88000050 cable is also used to connect these bias outputs to the tested devices.

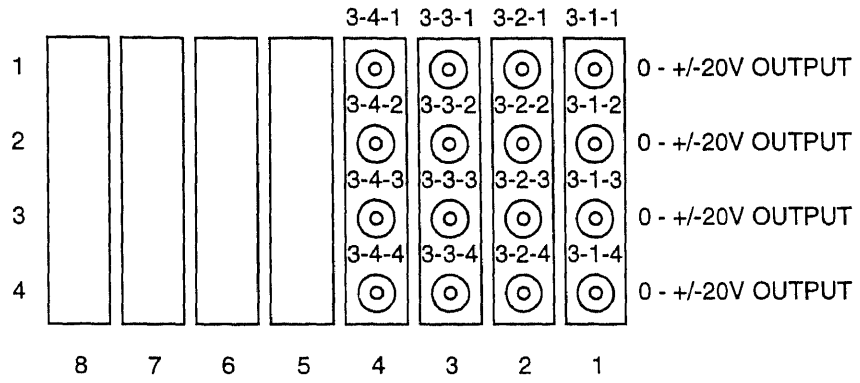


Figure 5.7 The output connectors of 40750 bias supply card.

Figure 5.8 shows the pin diagram of the first correlated demo chip. It is packaged as the MOSIS standard 40 pin configuration. To use PI 4000 for the test of such a packaged-chip product by using PI-88000050 cable as the output connector, an interface board that connects the cables and the chip must be implemented first. In this experimental setup, a commercial PC board is used to construct the interface. The diagram of this interface can be found in Appendix C.

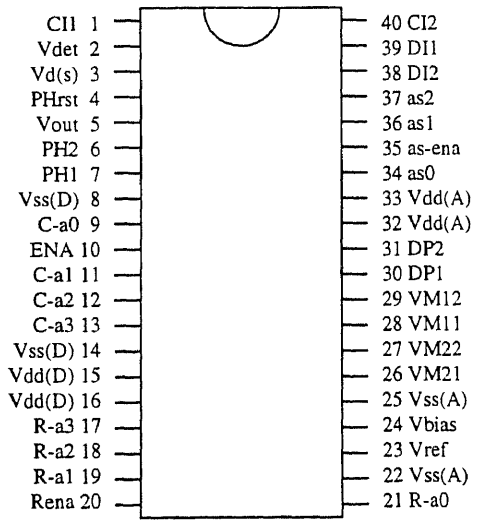


Figure 5.8 The pin diagram of the first correlated readout demo chip.

5.3 Circuit Biases and Timing

With the system software package provided by PI Company, it is convenient to supply circuitry DC biases and timing through computer programming, instead of using the soft keys in the equipment front panel. The system software allows the set up of all the functions of the 4000 test system, and the PI-5800A Data Generator over the IEEE-488 Bus and the RS-232-C Interface. The programming of the biases and timing mainly includes two parts: (1) Set DC biases and the amplitudes of the pulses using PI-STIM and (2) Design subpattern of the pulses and compile the output through instructions programming. This section presented how to program DC biases and timing for testing.

- The important steps for the operation of PI-STIM are listed below:

(1.1) To create a Mnemonic File: Select 'Mnemonic Table' from the main window 'File' menu and in the Open file dialog box type in a file name with the extension '.MNE'. Manually enter each channel definition by using Add, Type, Mainframe, Slot and Channel from the menu. The Mnemonic Table is the link between each bias and driver channel to the chip variable. Therefore, it must be exactly matched with interface board and pin diagram. The following lists the example of the mnemonic table for testing the demo chip:

Signal Name	Type	Address	Loc/Chan.
PHrst	40460 20V Driver	PI4000	MF: 2 Slot:1 Chan: 1
Vref	40750 20V LN Bias	PI4000	MF: 3 Slot:2 Chan: 1

and the complete table can be found in Appendix C. After the Mnemonic Table is completed, it should be set as default Mnemonic File that can be done by clicking on 'Default mne file' from the 'File' menu and select the file from the dialog box.

(1.2) To create a data file for the 40750 bias card: Click on 'Bias Supplies' from the main window 'File' menu and type in a file name with the extension '.BIA'. Select 'Append' from the definition file window menu, and fill in the default data by clicking on the 'Mnemonic/type name' list box button to display the channels currently available for this particular type of card and by selecting one from the list. Suitable DC operation voltages for optimizing chip performance are signed in this application. However they can be changed later by clicking 'modify' and cancelled by clicking 'delete'. An example of Bias Supplies is shown below:

Signal Name	**Volt**	**Loc.**	**Type**
Vref	2.500000	321	40750 20V LN Bias

(1.3) To create a data file for the 40460 driver card: Click on 'Clock Driver' from the main window 'File' menu and type in a file name with the extension '.clk'. The same as the DC biases, the Type and Channel of the clock pulses can also be appended by clicking 'Mnemonic/type name' and be modified and deleted with the same manner. The amplitudes of the pulses should also be matched with DC biases. For example in this test, 5V as VDD and 0V as VSS are used for the bias of the operational amplifier, thus the amplitudes for reset and modulation pulses should also be 5V. The rise and fall times of the pulses are also set in this application. If not particularly chosen, they are automatically set at up limit (10ns). However, in most time the equipment can only reach 20ns. An example of Clock Driver is shown below:

Signal Name	**Hlv**	**Hlv**	**Loc.**	**Type**
PHrst	5.000	0.000	211	40460 20V Driver
PH1	5.000	0.000	212	40460 20V Driver

- The following are the important steps for the operation of PI-PAT:

(2.1) To set the length for each subpattern: Click on 'subpatterns' from the main window 'Edit' menu and type in the starting unit and the length for each subpattern. The minimum length of the subpattern is 12 unit. The real time length for each unit is determined later by setting the system clock period. In total, 255 subpatterns and 4096 units can be defined. The upper limit for each subpattern is the available units to the maximum length.

(2.2) To design the subpattern and program the instructions: After checking 'pattern' from the main window 'Edit' menu, subpattern can be designed using left key of the mouse. The next step is to program the instructions by clicking 'instructions' from the 'Edit' menu. The basic syntax for instruction programming is:

Begin i

Subpattern j×k

Repeat From L m to L n,

where i to n are all integers to represent the subpattern and instruction lines and the repeating numbers.

(2.3) To run the program: No matter if the program is new, generated, or opened from file, it should be written to PI-5800A by clicking 'write' from main window. After the writing is done, the expected pulse output can be displayed on the front panel of PI-5800A. It will not have any output from the cable until a 'Run i' is flashing on top of the screen. To start running the program, one can simply click on 'Run' from the main window, or click on 'system' and using 'run' and 'stop' in the menu. The clock time, which determines the real frequency of the pulse, can be set from this menu.

Figure 5.9 gives the simplest timing for the correlated readout circuit. Without using an inverter on the chip, two clock signals, PH1 and PH2, must be used. The LED is synchronized with one of the clock signal to become a modulated source. Note that here one timing pattern can be implemented by different combination of the subpatterns and the instructions program. The experience of this research shows that the best approach should be started at the circuit design. A well-designed chip will result in simple timing. However, no matter what kind of approach is used, the correct timing is unique and can be tested by the oscilloscope before applying to the chip. This is an important step in the circuit measurement, since sometimes the output from the 40750 driver may be not the same as the pattern shown in the front panel. As shown in Figure 5.4, a Type 454 Oscilloscope was setup for this measurement and for the test of the circuit output as well.

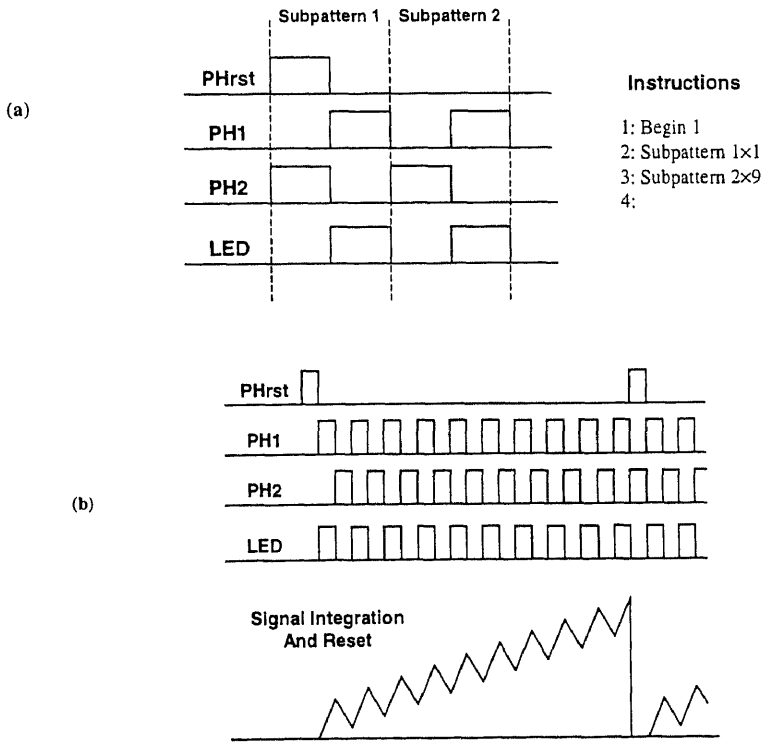


Figure 5.9 The simplest subpatterns and instructions program for timing the correlated readout circuit: (a) The subpatterns and the instruction program and (b) The clock output and the expected signal integration and reset.

5.4 The Correlated Readout Circuit Characterization

In this section we report the test results based on the setup described above. After the interface board was completed, and each channel of the biases and timing were examined, all the efforts on testing were focused on finding the expected function by optimizing the timing. The modulation frequency was the most important parameter to adjust in this test. However, the amplitudes of the LED pulse and the background light must be matched with an available working frequency. The correlated function, which is to charge the capacitor by the signal and the dark current and discharge by the dark current only, became clear on the screen of the oscilloscope at a relatively low modulation frequency (<3KHz). The frequency response and the effect of the switching feedthrough were also studied under the same test conditions.

5.4.1 The Correlated Function

The correlated function, both by the correlated CTIA and twin CTIA, was found when the modulation frequency was decreased to about 3KHz. It became clear on the Type 454 oscilloscope when the frequency was set at 500Hz and in each integration cycle there were about 10 phase shifts. Figure 5.10 shows a photo taken from the screen of the oscilloscope. When only the background was present, the integration on the capacitor was cancelled and the output became zero. Note that in this photo, because the reset occurred in the end of a charging phase, the output before reset was not zero; it was the result of integration during one clock phase, as shown in Figure 5.10(a). Figure 5.10(b) and 5.10(c) show what occurred when the LED was synchronized with PH1 and PH2. Since the reference voltage of the operational amplifier was set at 2.5V while Vdd was 5V, the

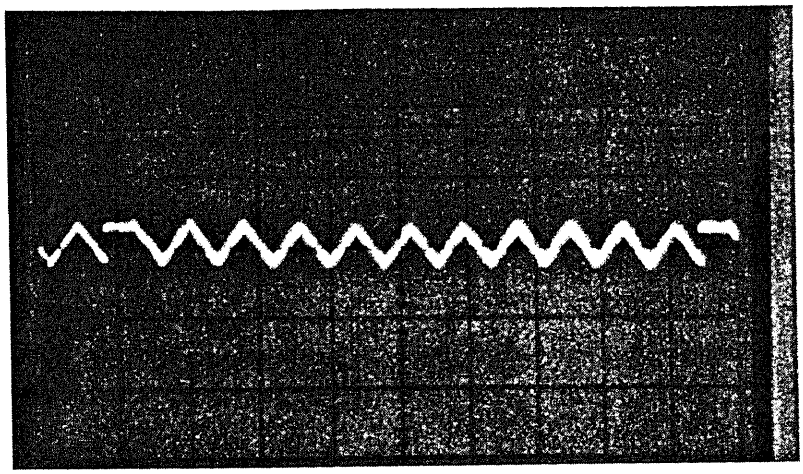


Figure 5.10(a) The correlated function when only the background is present.

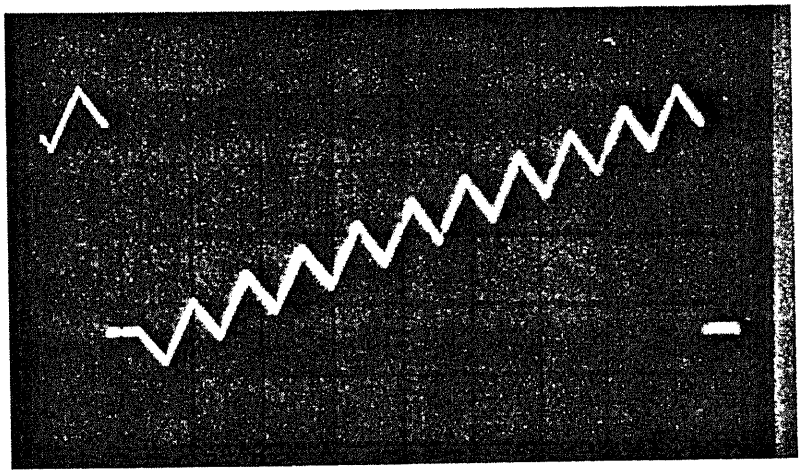


Figure 5.10(b) The correlated function when the LED signal is synchronized with $\phi 1$.

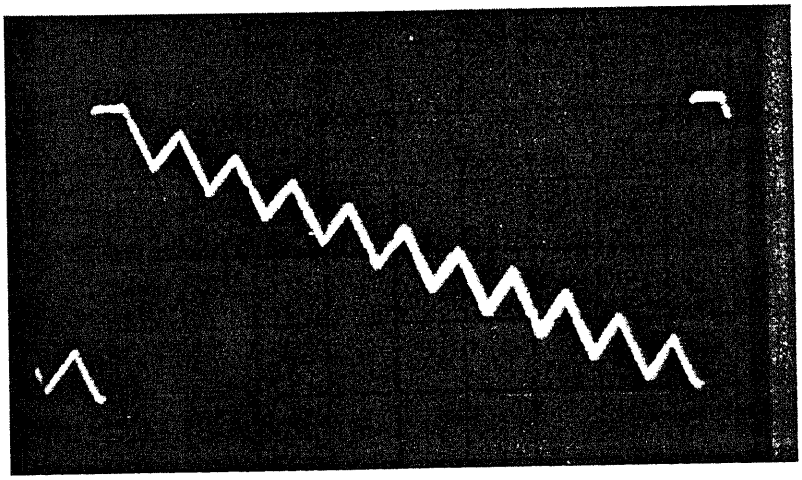
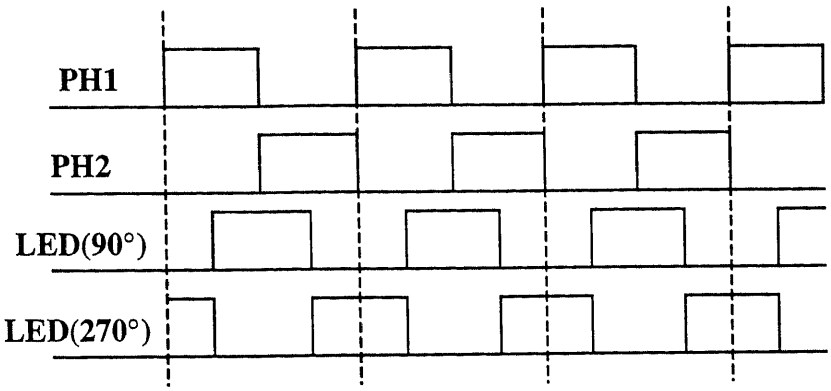


Figure 5.10(c) The correlated function when the LED signal is synchronized with $\phi 2$.

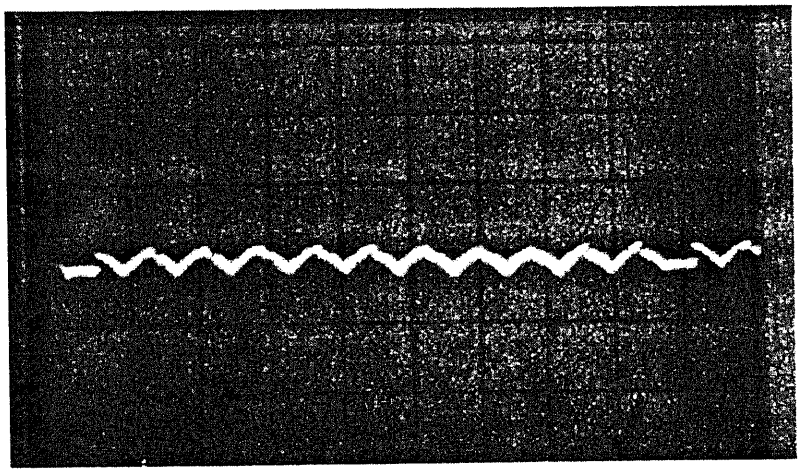
output could be made positive or negative by adjusting the phase between the LED and the switches. These results demonstrated that the correlated CTIA and the twin CTIA could charge and discharge a capacitor using switching system.

Under the test condition described above, the outputs of the correlated CTIA and the twin CTIA were not different. However, for the twin CTIA, a differential amplifier was used. Figure 5.11(a) shows the output for one of the CTIA under switching and Figure 5.11(b) shows the result when the detector's polarity is changed. Note that here the detector was zero biased because the detector bias was set the same as the Op Amp reference voltage (2.5V); therefore, the switch of the polarity of the detector just change the polarity of the output but with the same property. The process looked like a 'integration and hold' circuit. It integrated the current from the detector when the switch was on and held it when the switch was off. This function matched the simulation result very well, since the resolution of the oscilloscope prevented the observation of higher order effects. For example, when the switching feedthrough was superimposed on these outputs, but was relatively small under the test conditions, feedthrough effects were not observed at the input of the differential amplifier.

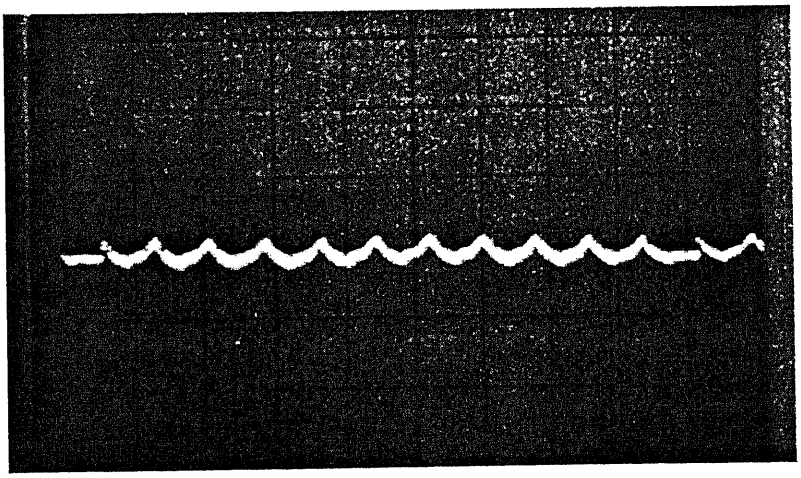
The differential integrator and the correlated direct readout circuits did not functioned as expected. For the differential integrator, the technical difficult was to find an optimized reference voltage, since it was necessary to write the program to the Data Generator every time the frequency or voltage was changed. The reference voltage seemed more sensitive to the output than what the simulation indicated. However, it is too early to conclude that the differential integrator will not function at all. For the



(a)



(b)



(c)

Figure 5.12 The demonstration of the phase effect. (a) The timing sequence, (b) The output for phase shift of 90°, and (c) The output for the phase shift of 270°.

correlated direct readout, the test results demonstrated that it would not perform the correlated function unless the design or the process was changed.

5.4.2 The Frequency Response

In the study of the frequency response of the correlated readout circuits, we tried to excite the LED with a signal that had a different frequency and phase than the switching signal and measure the results at the circuit output. To change the phase of a certain channel of the PI-4000 is simple and can be done by changing the delay time for that channel. Figure 5.12 shows the outputs when the LED excitation signal was shifted 90° and 270° from the switching signal when the background light was turned off. These results matched with the simulation very well and confirmed that the correlated readout circuit can behave similar to a phase sensitive detector.

To excite the LED with a signal that has a different frequency than the switching signal using the PI-4000, it is relatively simple only for some special frequencies, such as frequencies that are an integer times to the reference. For most cases, especially when the frequency of this particular channel is close to the reference channel, it usually needs to reset the length of the subpatterns and/or the system clock period, and rewrite the instructions program again. As an example, Figure 5.13 shows the timing sequence for the first three cycles when the switching signals are 500Hz (2000μs) and the LED signal is 502Hz (~1992μs). After a half period time of the switching signal, which is 1000μs, the difference of the LED to the PH1/PH2 is about 4μs. The pattern repeats itself with 200 cycles. A simple method to generate this timing sequence by PI-4000 has not been found so far.

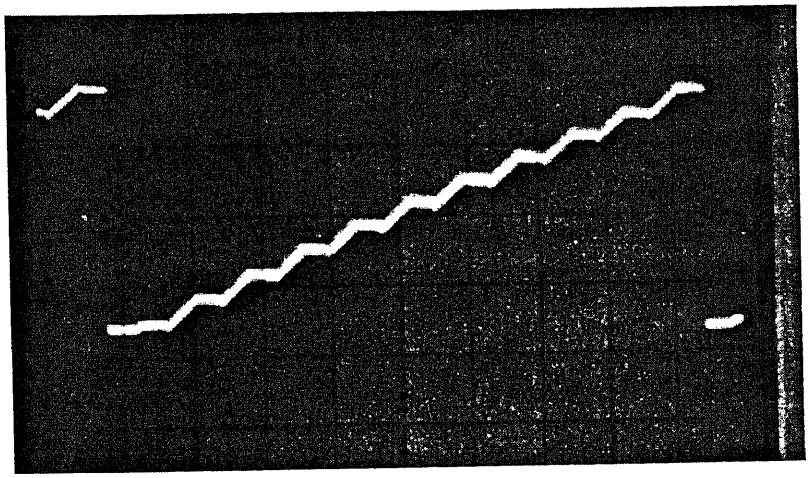


Figure 5.11(a) The output for one of the twin CTIA was functioned as an 'integration and hold' circuit. The clock feedthrough was superimposed on the outputs, but was not significant compared to signal current under the test condition to get this photograph

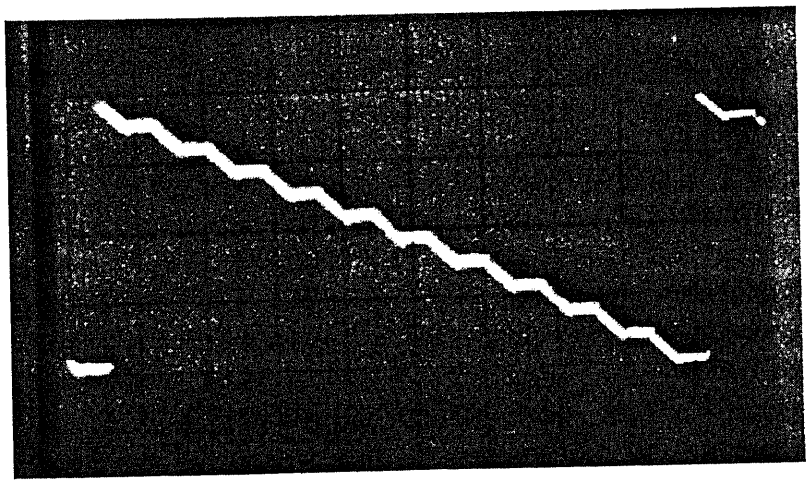


Figure 5.11(b) When the photon detector polarity was changed, the polarity of the input current was changed but the circuit still function as an 'integration and hold' circuit, because the detector is zero biased and the reference voltage of the Op Amp was set at the middle of the Vdd.

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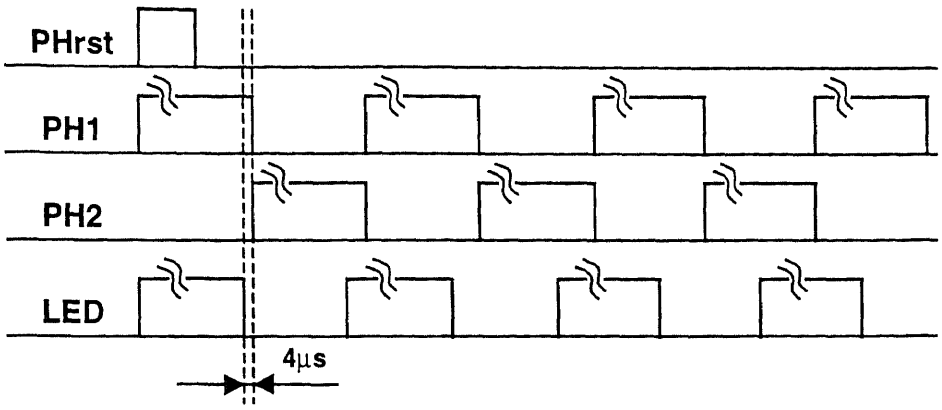

Figure 5.13 The clock relationship when the switching signals are 500Hz and the LED exciting signal is 502Hz. Only first three cycles are shown in the figure.

As shown in Figure 5.10, in the correlated function test the integration capacitor was reset when the number of switching times was ten (N=10). Therefore, in the quantitative measurement of frequency response an 'incomplete period' method for the circuit timing was used. Instead of considering the whole 200 cycles, only first 10 cycles were programmed. Although there are many other ways to program this first 10 cycles, especially for the special frequencies, the basic subpatters as shown in Figure 5.14 for the instructions programming were used. By setting the clock period as 200ns and the length of the subpattern as 20 units, the instructions program used for PH1 as 500Hz and LED as 502Hz was the one shown in Table 5.1.

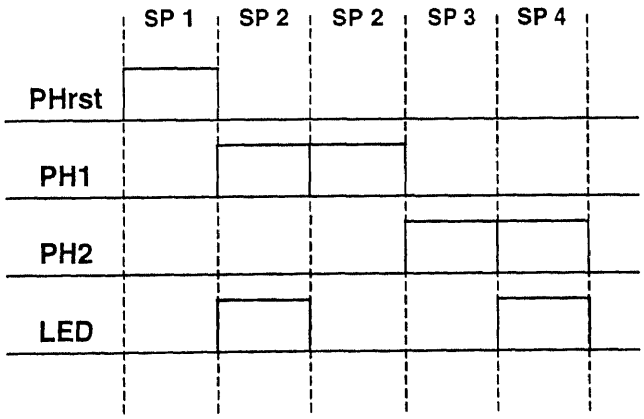

Figure 5.14 Basic subpatterns in Figure 5.13.

Table 5.1 Instructions program for generating Figure 5.13 for 10 cycles

1: Begin 1	15: Subpattern 2×243	29: Subpattern 4×236
2: Subpattern 1×20	16: Subpattern 3×7	30: Subpattern 5×14
3: Subpattern 2×249	17: Subpattern 4×242	31: Subpattern 2×235
4: Subpattern 3×1	18: Subpattern 5×8	32: Subpattern 3×15
5: Subpattern 4×248	19: Subpattern 2×241	33: Subpattern 4×234
6: Subpattern 5×2	20: Subpattern 3×9	34: Subpattern 5×16
7: Subpattern 2×247	21: Subpattern 4×240	35: Subpattern 2×233
8: Subpattern 3×3	22: Subpattern 5×10	36: Subpattern 3×17
9: Subpattern 4×246	23: Subpattern 2×239	37: Subpattern 4×232
10: Subpattern 5×4	24: Subpattern 3×11	38: Subpattern 5×18
11: Subpattern 2×245	25: Subpattern 4×238	39: Subpattern 2×231
12: Subpattern 3×5	26: Subpattern 5×12	40: Subpattern 3×19
13: Subpattern 4×244	27: Subpattern 2×237	41: Subpattern 4×230
14: Subpattern 5×6	28: Subpattern 3×13	42: Subpattern 5×20

By using the timing strategy described above, the outputs of the circuits were measured for particular frequencies. Some data are listed in Table 5.2 and the unified values are plotted in Figure 5.15 with the correlated sinc function f(x). Since in these measurements we did not change the 2.5V reference voltage of the Op Amp and the maximum output voltage was 3.84V, the definition of unified value becomes

$$Value(unified) = \frac{V(output) - 2.5}{3.84 - 2.5} \times 0.637 = 0.4754 \times [V(output) - 2.5]$$

The coefficient of 0.637 is the maximum value of equation 3.17 when T_{int}/C_{int} is set as 1.

Table 5.2 Some measurement results for the frequency response

Period (μs)	Frequency (Hz)	Output Voltage (V)	Unified Value
2168	461	2.801	0.143
2120	471	3.270	0.366
2096	477	3.335	0.397
2048	488	3.737	0.588
2040	490	3.756	0.597
2008	498	3.840	0.637
1984	504	3.804	0.620
1952	512	3.623	0.534
1920	521	3.436	0.445
1888	530	3.133	0.301
1824	548	2.542	0.020

* The complete data for Figure 5.15 can be found in Appendix C.

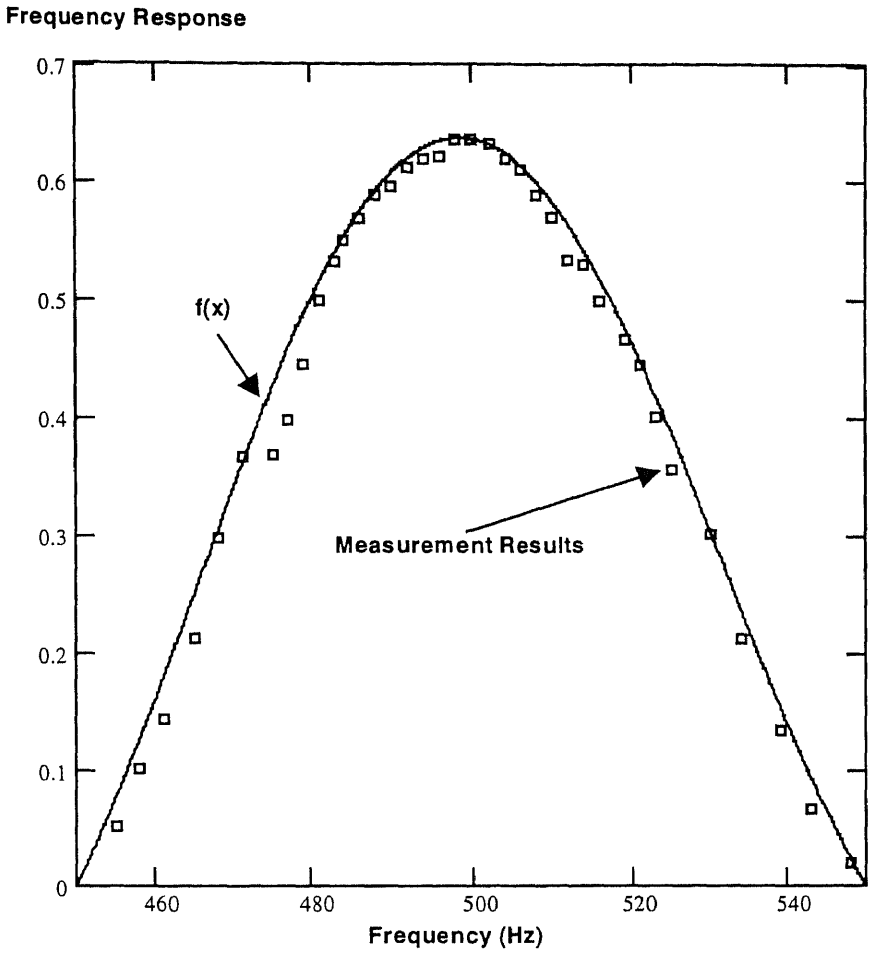

Figure 5.15 The plot of frequency response from 450Hz to 550Hz when the modulation frequency is 500Hz. The solid line is the absolute value of the correlated sinc function when T_{int} is 2ms, N equal to 10, and T_{int}/C_{int} equal to 1. The box is the unified measurement results listed in Table 5.2.

As shown in Figure 5.15, the measurement results agreed with the theoretical calculation very well in the frequency range we studied. The higher order harmonic windows were also observed but not plotted. The experimental results showed better noise reduction capability than the theoretical calculations since the measured voltages decreased faster when the frequency was shifted away from the modulation frequency. This is because only the first 10 cycles in the time domain was used to study the frequency response. Each time a measurement was made, the phase of the input signal was adjusted to find the maximum output in that frequency. As shown in Figure 5.12,

even with the same frequency, the output could be zero if the phase was shifted. Actually, to obtain a higher output was more difficult because the phase must be optimized. Whatsoever, this result strongly indicates that the correlated readout circuit is capable of reducing the output when the frequency is away from the modulation frequency. It proved again that the correlated readout circuit has the same function as the phase sensitive detector.

5.4.3 The Switching Feedthrough

Although this research was not designed for the study of the switching feedthrough, some information from the circuit characterization was obtained because this issue is believed to be critical in the design of correlated readout circuit. The result of switching feedthrough was first observed at each output of the twin CTIA, when the detector was completely shielded while the modulation signals were applied. The signal on the oscilloscope was not clean but an output was clearly shown. By changing the system clock period without changing the subpatterns and the program, the output would not change for the frequency range studied, as shown in Figure 5.16 by SF1. This result showed that the accumulation of the switching feedthrough is determined by the number of switching times, since in this operation the total number of switching times between two resets remained constant although the modulation frequency was changed. To set the signal integration time as a constant by increasing the repeating line in the instructions program, the output became higher simply because the high modulation frequency results in a large number of switching times. At the frequency range studied, this result was also linear and is shown in Figure 5.16 as SF2.

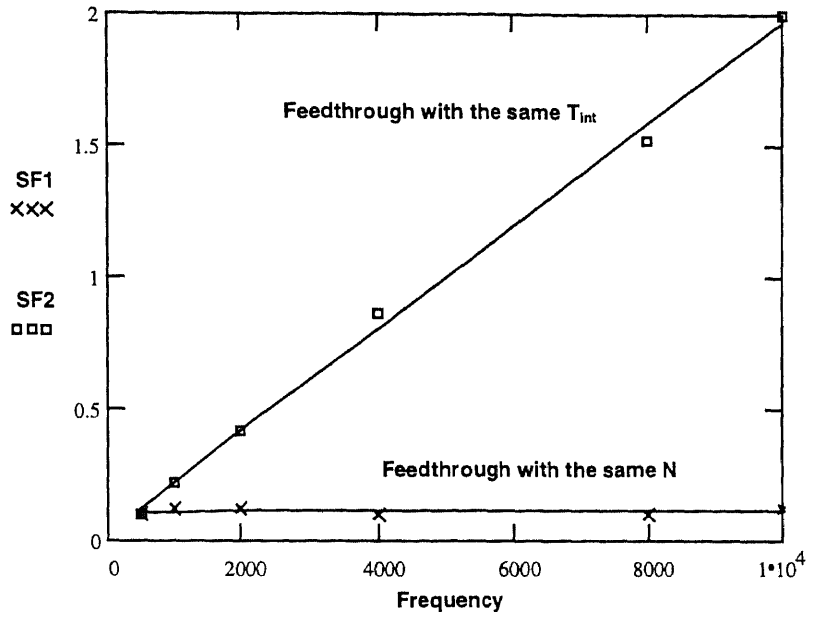

Figure 5.16 The output voltages at each twin CTIA due to the switching feedthrough. The cross (SF1) represents the results when number of switching time is fixed at 10 and the box (SF2) represents the results when integration time is fixed at 20MS.

Another important factor that affects the switching feedthrough is the rise and fall times of the clock signal. When these times were small, a high output was observed. But there was no significant change when this time was greater than 20NS. Since the limitation of this time is 10NS for the PI-5800A Data Generator, not enough information was obtained to model its effect.

At the output of the differential amplifier for the twin CTIA, the switching feedthrough was cancelled out and the output became clean as shown in Figure 5.10. Also, when the photon current was present, the switching feedthrough seemed to disappear as shown in the Figure 5.11, although it was still existing as shown by the saturation of the integration capacitor. Theoretically, the feedthrough would not vanish when photocurrent is present. However, if only the switching feedthrough was the concern, saturation seemed to happen too early according to the results measured from

each twin CTIA. In other words, when the detector current is present, the effect of the switching feedthrough is not clear so far.

For the correlated CTIA, this effect can not be studied separately like the twin CTIA. Under the same conditions for the study of each twin CTIA, the voltage measured at the output of the correlated CTIA was relatively small with increasing number of switching cycles. However, when the signal and background were added up, the effort to increase the number of switching cycles was not successful; however, the detection conditions were not kept constant. The reason fo early saturation must be more complicated than the switching feedthrough; however, the reason for this could not be found from the test. Although complete quantitative results for the circuits studied were not yet obtained, from the phenomena observed during this research it was concluded that the correlated CTIA and the twin CTIA would have their own advantages in different detection applications.

5.5 Summary

In this chapter, the methodology for the experimental study of the correlated readout method was presented first. Since this research is in its initial stages, a direct modulation method was proposed and used for the characterization of the correlated readout circuits. In the direct modulation experimental setup, the signal generator controlled the object and the circuit synchronously so that optical modulator was not necessary. By excluding all the possible optical factors, one could concentrate on characterization of the circuits. However, after the circuits are completely characterized, active and passive imaging methods should be investigated.

The test equipment was presented in chapter 5.2 and the method for creating the bias and timing was discussed in chapter 5.3. The PI-4000 Low Noise Focal Plane Array Test System was used for the circuit testing. The system can provide 16 channels of low noise pulses and 16 channels of accurate DC biases. The heart of the system is a programmable PI-5800A Data Generator. The choice of the timing sequence depends on the length of the subpatterns, the system clock period, the particular shape of the waveform of the subpatterns, and the instructions program.

The results for the correlated function, the frequency response, and the switching feedthrough characterized the correlated readout circuit. The correlated function, both for the correlated CTIA and the twin CTIA circuits, was observed clearly on the oscilloscope when the modulation frequency was decreased below 500Hz and the proper LED and background light intensity were set. However, the differential integrator and the correlated direct readout did not function as expected. In the study of the frequency response, an incomplete period timing method was used. The voltage measurement results showed that the correlated readout circuits would reduce the output if the signal had a different frequency than the modulation frequency. The switching feedthrough effect was studied by turning off the optical input by shielding the detector, while keeping the modulation signal on. The number of switching cycles and the rise/fall times of the clock signal were two factors that had a strong influence on the switching feedthrough effect. However, there are other factors, not yet studied experimentally that are expected to be important. The results of these experiments strongly indicate that the correlated readout circuit can behave as a phase sensitive detector.

CHAPTER 6

SUMMARY AND CONCLUSIONS

6.1 Summary

To solve the problem of focal plane array (FPA) imaging in the presence of large dark current, imaging with a modulated source was proposed for this research. This thesis research investigated the feasibility to realize this new imaging method using a novel readout method – correlated readout. The following summarizes the thesis research:

- Review of recent publications in the field of FPA imaging revealed that hybrid infrared electronics is the dominant readout approach. The large background subtraction circuit approaches of this thesis were based on these previously developed hybrid readout electronics: direct detector input (DDI), direct injection (DI), buffered direct injection (BDI), gate modulation, and capacitive transimpedance amplifier (CTIA) [1-3]. In principle all these readout circuits would have difficulty succeeding in applications where large dark current is present since dc measurement techniques are susceptible to dc drift and 1/f noise, although the current memory based readout methods showed significant progress in subtracting the dc component of large background current [29, 34].
- This thesis implemented a correlated readout method [14] that involved charging an integration capacitor with photo-detected signal and the dark current in one modulation phase, and discharging the capacitor with the dark current only during the following phase. A correlated reset integrator was developed to model the frequency response based on the principle of the correlation technique and phase sensitive

detection. The system theory and the transfer function for a reset integrator were utilized to derive the transfer function of the correlated reset integrator.

- Correlated interface circuits based on presently commercially available hybrid readout electronics were suggested. Using these circuits, the existing readout architecture can be inherited and utilized to design effective correlated readout circuits. The circuits thus designed from the capacitive transimpedance amplifier (CTIA) were studied theoretically and experimentally. The correlated CTIA, which consisted of four switches and one conventional CTIA, was considered the most promising circuit to realize the correlated readout approach since it was possible to charge and discharge the same integration capacitor. The other methods were based on integrating the charge in separate capacitors whose dark current charge was cancelled by a differential amplifier.
- The possible applications of the correlated readout method in passive and active imaging, especially for the measurement of solar magnetograph [7], were studied. The challenges in designing an optical system were considered and different optical modulation schemes for passive imaging were discussed.
- The design of the correlated readout circuit in standard CMOS was studied and the first demo chip, which consisted of a 16×16 isolated detector array and four interface circuits, was designed and fabricated by the Orbit 2μm n-well process. PSpice was used for the simulation of the operational amplifier, the correlated CTIA, and the entire demo chip. The MOSFET parameters for the Orbit 2μm n-well process provided by MOSIS were also used for all simulations of this thesis research and the

values used in the SPICE program are the average results from recent 10 runs.

- The problems introduced by the switching system were studied through the dc model, the switching feedthrough, and the noise model. The switching feedthrough, which results from both charge injection and capacitive feedthrough, was addressed as the key issue in the correlated readout circuit design. A method to study switching feedthrough using PSpice was proposed and used in the research. The possible factors that influence the result of switching feedthrough were simulated and the results were reported. Classical methods for reducing the switching feedthrough effect by circuit design, which included a dummy transistor, a CMOS current steering circuit and a fully differential topology, were studied in theory and by PSpice simulation.
- The methodology for testing the correlated readout circuit was experimentally studied. A direct modulation method, which used a light emitting diode (LED) as object and synchronously controlled the LED and modulation signal, was suggested and used for the circuit test. A Pulse Instrument 4000 Series Low Noise Focal Plane Array Test System was used for the first time for biasing and timing the correlated readout circuits.
- The correlated function, both by the correlated CTIA and the twin CTIA, was experimentally demonstrated for the modulation frequency of 500Hz. An incomplete timing period strategy, which used first N cycles (N = 10 in the test) to modulate the LED and switches, was suggested and used to measure the frequency response of the correlated readout circuits. The effect of the switching feedthrough was studied by shielding the detector and keeping the modulation signal on.

6.2 Conclusions and Suggestions for Future Studies

The overall goal of this project was to develop a readout method that can read out a photo detected image signal in the presence of a large detector dark current. The basic concept is to discriminate against the dark current by modulating the optical flux and demodulating the output signal with the interface circuit. This thesis research led to the following conclusions:

1. Commercially available circuits for optical sensing with a modulated source, such as the lock-in amplifier, can not be applied in focal plane array technology because of their circuitry complexity relative to the limited chip area. The correlated readout method was shown to be feasible both theoretically and technically for discriminating against dark current. However, some relatively straightforward engineering design problems remained to be addressed before FPA could be manufactured. Also it was concluded that the principle of phase sensitive detection should be further investigated to reveal other, even better, approaches for future FPA technology.
2. The signal processing for the correlated readout can be successfully done with a correlated reset integrator. The transfer function of the correlated reset integrator developed using system theory showed that the primary transmission window was shifted to the modulation frequency so that the dc component of the dark current would be rejected; the attenuation of low frequency noise, such as dc drift and 1/f noise, was dependent on the modulation frequency and the number of switching cycles. Therefore, an optimized modulation frequency, which depends on the

background noise for particular detection conditions, could be designed to achieve a high signal-to-noise ratio and large dynamic range.

3. The switching feedthrough was the most important problem in the circuit design. The factors that can influence the feedthrough included the switch configuration, modulation strategy, Op Amp characteristics, and the detector quality. A useful circuit approach to minimize the feedthrough effect was a CMOS current steering circuit (with four CMOS switches) driving a high common-mode rejection ratio Op Amp. The dummy transistor circuit, a popular method for canceling the feedthrough in sample and hold circuits, was found to be not applicable to the correlated readout circuit design.
4. Direct modulation method, versus using an optical modulator, was preferred for the circuit characterization since optical modulator effect could be neglected. The PI-4000 series was found to be suitable for testing the correlated readout circuit. To study the frequency response, an incomplete period method was a good method since it eased the timing programming. However, the equipment should have more features that can be applied to the correlated readout circuit characterization.
5. Modified capacitive transimpedance amplifier (CTIA), correlated CTIA and twin CTIA circuits, demonstrated promise for practical FPA. The correlated direct readout circuit must be redesigned if the Orbit 2μm n-well process is used for fabrication.

For future research, both theoretical and experimental works should be continued before a practical FPA is designed. The suggestions are listed below.

a) The correlated reset integrator model should be improved by adding the effect of

switching feedthrough. It is possible that understanding and control of the switching feedthrough effect on readout circuits will require a major effort. This understanding is necessary for applying the correlated readout method to the various possible detection conditions.

b) Besides the pixel area minimization, other advantages and problems of using submicron technology should be investigated. Possible limitations on the approaches for canceling the switching feedthrough by circuit design should be given high priority.

c) The test architecture should be chosen before designing the circuits. The library for the common cell, such as row and column shift registers, should be well established before concentrating on the design of the interface circuits.

d) To effectively evaluate the various possible readout circuit designs, a standard experimental condition should be selected. For characterization of the test chip using the PI-4000 system, a standard interface board and timing program should be chosen so that the designs can be compared experimentally.

e) Finally, how to best apply the correlated readout method to existing imaging systems should be studied. Each system may require a different readout method to achieve optimum performance. Such a study would lead to a more complete understanding of the effectiveness of the proposed modulated source approach to FPA photon detectors.

APPENDIX A

SPICE PROGRAM FOR DEMO CHIP SIMULATION

In this appendix, the PSpice program for demo chip simulation is listed. The source codes for the simulation of the operational amplifier and the capacitive transimpedance amplifier can be found in this program.

```
Chip Performance Simulation

*Chip bias
VDD 1 0 5V
VSS 4 0 0V
VD 10B 0 PULSE(0V 5V 20US .1US .1US 19.9US 40US)
XS 1 4 10B 10C INV
V+ 10 0 1V
V- 10A 0 4V
R- 10A 6A 20MEG
VREF 7 0 2.5V
VBIAS 9 0 3.24V
.TRAN .1U 6MS
.PROBE V(8) V(02R) V(03R) V(01C) V(8S)

*Signal integration and processing by the correlated CTIA
MS1 6 10B 6B 0 MN L=4U W=4U
MS2 6A 10C 6B 0 MN L=4U W=4U
X1 1 4 6B 7 8 9 OPAM
CINT 6B 8 5PF
MRST 8 20 6B 0 MN L=10U W=4U
VRST 20 0 PULSE(5V 0V 20US .1U .1U 389.9US 400US)

*Sampling circuit which was not processed in the chip
XSA 1 4 8S 7S 8S 9 OPAM
"
CSA 7S 0 300FF
"
MSS 8 8SA 7S 0 MN L=4U W=4U
"
VSA 8SA 0 PULSE(5V 0V 8US .001US .001US 398.49US 400US)
"

"
*Detector Array
"
R11 10 01I 17MEG
"
XI11 01I 01R 01C 01E PCS
"
```

```
R12 10 02I 15MEG
"
XI12 02I 02R 01C 01E PCS
R13 10 03I 20MEG
XI13 03I 03R 01C 01E PCS
R14 10 04I 14MEG
XI14 04I 04R 01C 01E PCS
M01 01E 01C 6 0 MN L=2U W=4U

R21 10 21I 14MEG
XI21 21I 01R 02C 02E PCS
R22 10 22I 16MEG
XI22 22I 02R 02C 02E PCS
R23 10 23I 18MEG
XI23 23I 03R 02C 02E PCS
R24 10 24I 15MEG
XI24 24I 04R 02C 02E PCS
M02 02E 02C 6 0 MN L=2U W=4U

R31 10 31I 15MEG
XI31 31I 01R 03C 03E PCS
R32 10 32I 15MEG
XI32 32I 02R 03C 03E PCS
R33 10 33I 12MEG
XI33 33I 03R 03C 03E PCS
R34 10 34I 16MEG
XI34 34I 04R 03C 03E PCS
M03 03E 03C 6 0 MN L=2U W=4U

R41 10 41I 12MEG
XI41 41I 01R 04C 04E PCS
R42 10 42I 12MEG
XI42 42I 02R 04C 04E PCS
R43 10 43I 15MEG
XI43 43I 03R 04C 04E PCS
R44 10 44I 15MEG
XI44 44I 04R 04C 04E PCS
M04 04E 04C 6 0 MN L=2U W=4U

*Row Shift Register control signal input
VC0 50 0 PULSE(5V 0V 20U .1U .1U 399.9U 800U)
VC1 51 0 PULSE(5V 0V 20U .1U .1U 799.9U 1600U)
VC2 52 0 0V       * To save the simulation time these two
VC3 53 0 0V       * column may not be used.
X50 1 4 50 60 INV
X51 1 4 51 61 INV
X52 1 4 52 62 INV
X53 1 4 53 63 INV

X60 1 4 60 70 INV
X61 1 4 61 71 INV
X62 1 4 62 72 INV
X63 1 4 63 73 INV

*Column Shift Register control signal input
VC6 56 0 PULSE(5V 0V 20U .1U .1U 1.6M 3.2M)
VC7 57 0 PULSE(5V 0V 20U .1U .1U 3.2M 6.4M)
```

```
VC8 58 0 0V        * To save the simulation time these two
VC9 59 0 0V        * rows may not be used.
X56 1 4 56 66 INV
X57 1 4 57 67 INV
X58 1 4 58 68 INV
X59 1 4 59 69 INV
X66 1 4 66 76 INV
X67 1 4 67 77 INV
X68 1 4 68 78 INV
X69 1 4 69 79 INV

*Pre-decoder for row decoder
*60 --72 are 3 code input and 30 --37 are 8 words
XPDR 1 4 60 61 62 70 71 72
+30 31 32 33 34 35 36 37 PDECODE

* Row decoder output by AND
XR00 1 4 30 63 01R AND
XR01 1 4 31 63 02R AND
XR02 1 4 32 63 03R AND
XR03 1 4 33 63 04R AND

*Pre-decoder for column decoder
*66 -- 78 are 3 code input and 40 --47 are 8 words
XPDC 1 4 66 67 68 76 77 78
+40 41 42 43 44 45 46 47 PDECODE

* Column decoder output by AND
XC00 1 4 40 69 01C AND
XC01 1 4 41 69 02C AND
XC02 1 4 42 69 03C AND
XC03 1 4 43 69 04C AND

*SUBCIRCUIT OF THE CHIP

*Operational Amplifier
*6 is the - input, 7 is the + input, 8 is the output
*and 9 is the current source bias
.SUBCKT OPAM 1 4 6 7 8 9
M1 3 6 2 2 MP L=4U W=70U
M2 5 7 2 2 MP L=4U W=70U
M3 3 3 4 4 MN L=4U W=30U
M4 5 3 4 4 MN L=4U W=30U
M5 2 9 1 1 MP L=4U W=20U
M6 8 5 4 4 MN L=6U W=160U
M7 8 9 1 1 MP L=6U W=60U
.ENDS OPAM

*Photo diode cell
*ONLY switching system for photo-current simulation.
*A resister can be connected in node 11
.SUBCKT PCS 11 12 14 15
M1 11 12 13 0 MN L=2U W=4U
M2 13 14 15 0 MN L=2U W=4U
.ENDS PCS

.SUBCKT PDECODE 1 4 60 61 62 70 71 72
```

```
+30 31 32 33 34 35 36 37

X1P0 1 4 60 61 40 AND
X1P1 1 4 70 61 41 AND
X1P2 1 4 60 71 42 AND
X1P3 1 4 70 71 43 AND

X2P0 1 4 40 62 30 AND
X2P1 1 4 41 62 31 AND
X2P2 1 4 42 62 32 AND
X2P3 1 4 43 62 33 AND
X2P4 1 4 40 72 34 AND
X2P5 1 4 41 72 35 AND
X2P6 1 4 42 72 36 AND
X2P7 1 4 43 72 37 AND
.ENDS PDECODE


.SUBCKT AND 1 4 3 5 8
M1 6 3 1 1 MP L=2U W=10U
M2 6 5 1 1 MP L=2U W=10U
M3 6 3 2 4 MN L=2U W=6U
M4 2 5 4 4 MN L=2U W=6U

M5 8 6 1 1 MP L=2U W=10U
M6 8 6 4 4 MN L=2U W=4U
.ENDS AND

*Inverter for register control signal input
*2 is input, 3 is output
.SUBCKT INV 1 4 2 3
M1 3 2 1 1 MP L=2U W=10U
M2 3 2 4 4 MN L=2U W=4U
.ENDS INV

*MOS model parameters are the average of most recent 10 runs
*provided by MOSIS
.MODEL MN NMOS LEVEL=2 PHI=0.70000 TOX=3.9900E-8 XJ=0.20000U
+TPG=1.00
+ VTO=0.7095 DELTA=3.4630E+00 LD=2.1350E-07 KP=6.2743E-05
+UO=725.7 UEXP=1.2910E-01 UCRIT=1.8587E+04 RSH=7.3590E+00
+GAMMA=0.5588 NSUB=7.118E+15 NFS=1.9700E+11 VMAX=5.3840E+04
+LAMBDA=3.6900E-02 LAMBDA=3.6900E-02 CGDO=2.7678E-10
+CGSO=2.7670E-10 CGBO=3.4784E-10 CJ=1.2324E-04 MJ=0.60152
+CJSW=5.5311E-10 MJSW=0.26600 PB=0.54439
*
.MODEL MP PMOS LEVEL=2 PHI=0.700000 TOX=3.9900E-08 XJ=0.200000U
+TPG=-1.000
+VTO=-0.90030 DELTA=2.1870E+00 LD=3.3360E-07 KP=1.7075E-05
+UO=197.3 UEXP=3.0750E-01 UCRIT=1.2820E+05 RSH=6.3330E+00
+GAMMA=0.7086 NSUB=1.1380E+16 NFS=5.9920E+12 VMAX=9.9990E+05
+LAMBDA=5.1960E-02 LAMBDA=5.1960E-02 CGDO=1.97550E-10
+CGSO=3.2011E-10 CGBO=3.7541E-10 CJ=3.1534E-04 MJ=0.61026
+CJSW=4.03640E-10 MJSW=0.217510 PB=0.900000

.END
```

APPENDIX B

CELL LAYOUTS IN DEMO CHIP

The mask layouts for switching system and capacitive transimpedance amplifier are shown in this appendix.

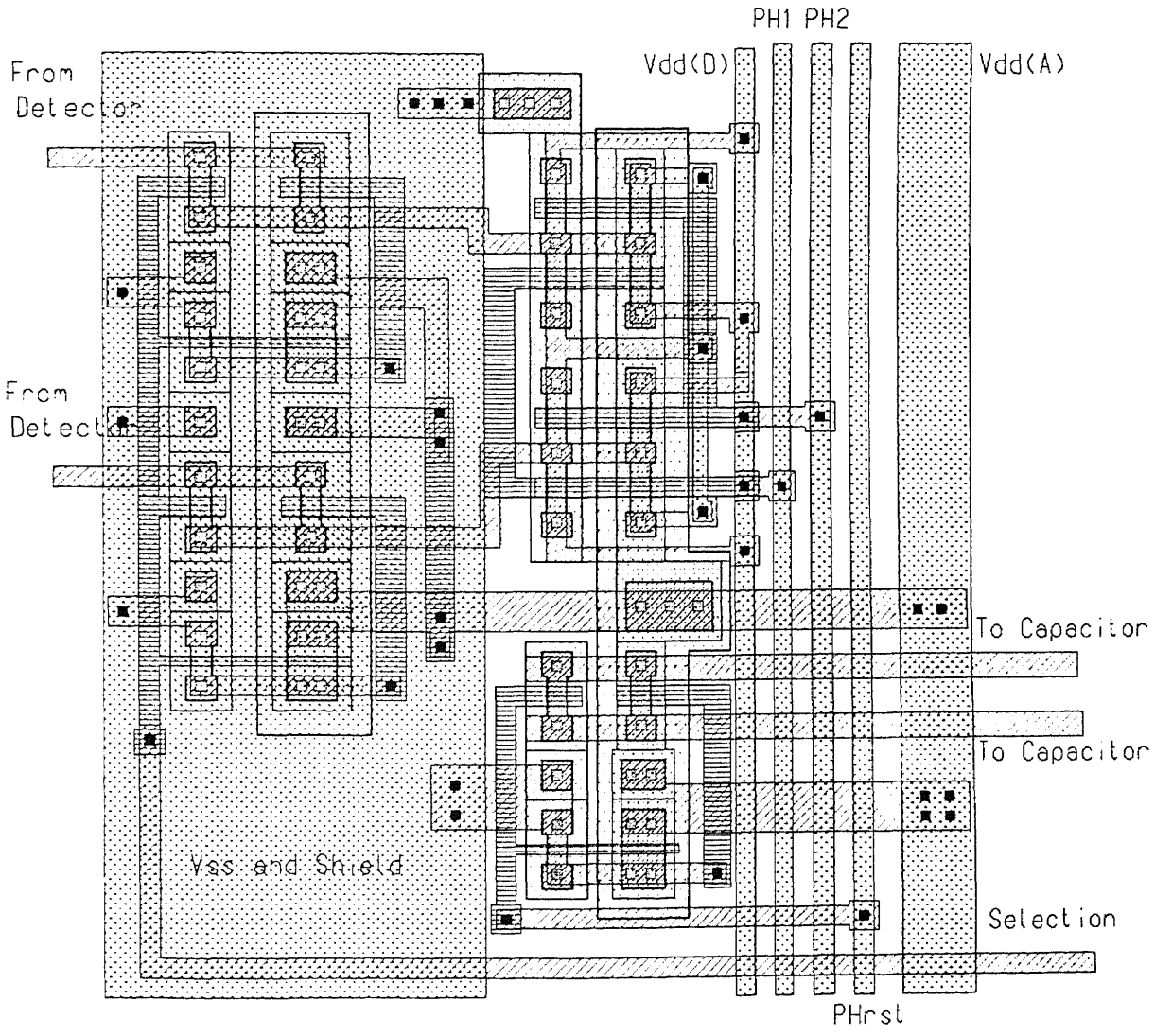

Figure B.1 Mask layout for the switching system.

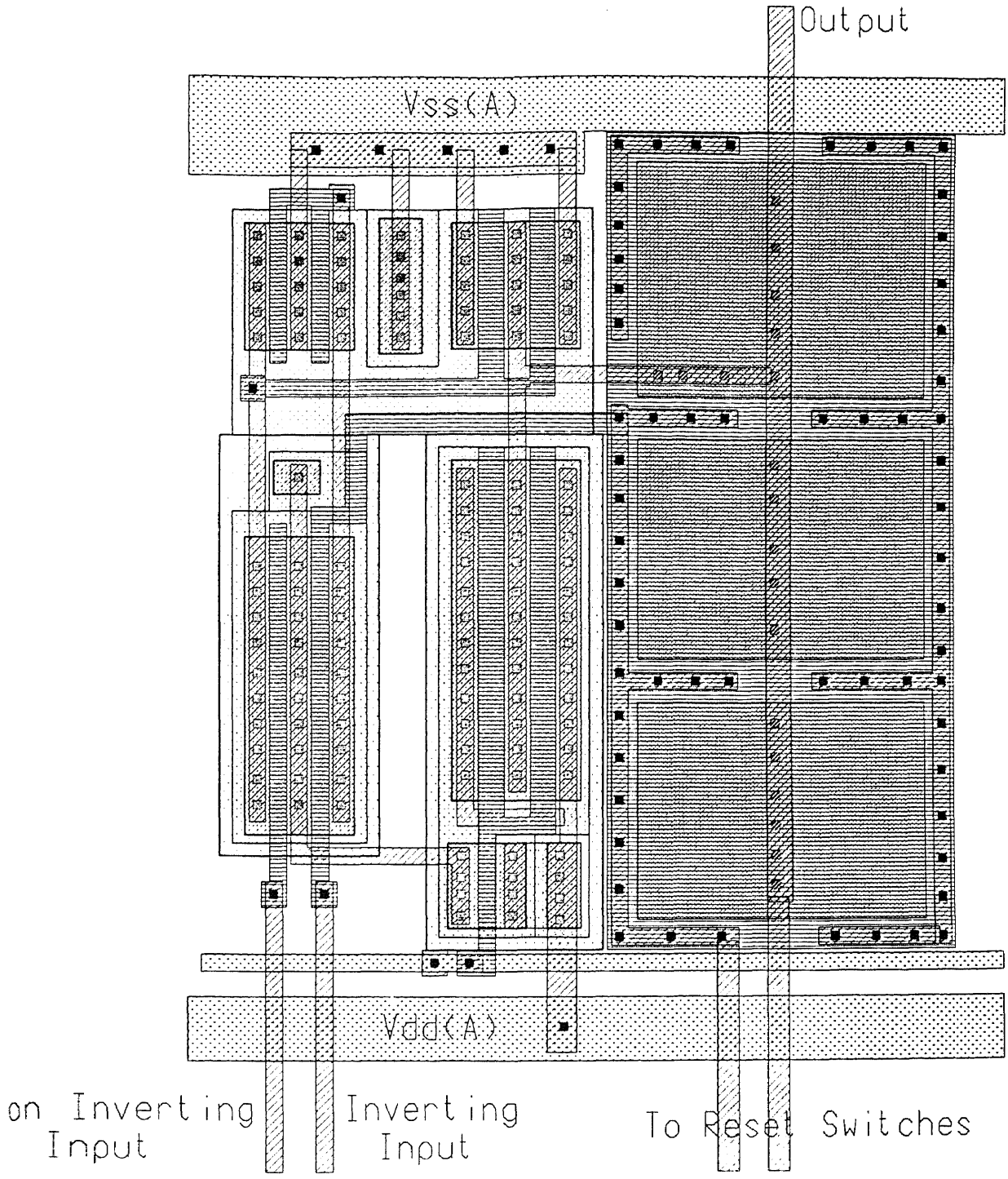

Figure B.2 Mask layout for the CTIA.

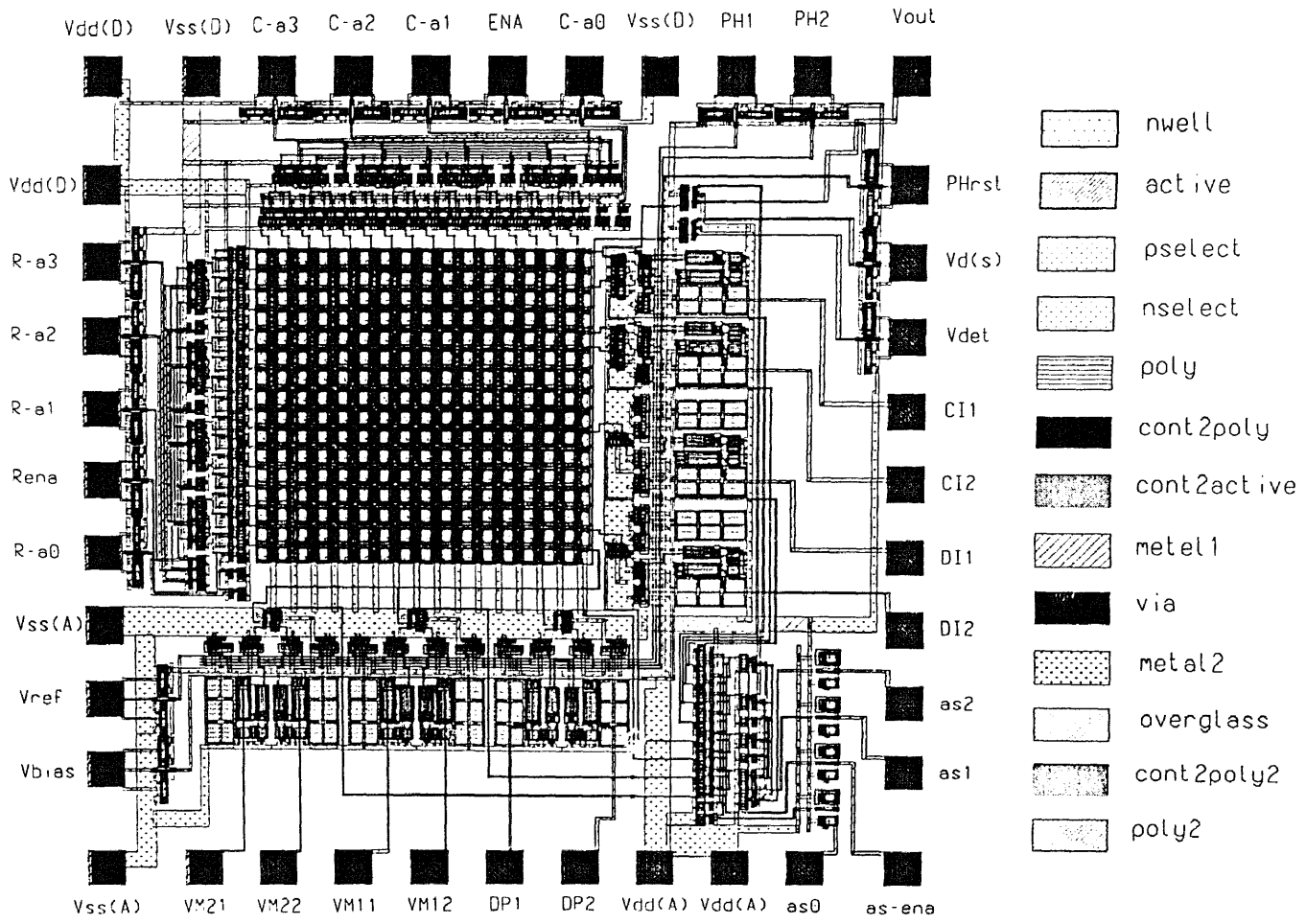

Figure B.3 Layout of the first readout demo chip.

APPENDIX C

DOCUMENTS FOR DEMO CHIP TEST

Some important documents for testing the correlated readout demo chip using PI 4000 system are shown in this appendix.

Table C.1 Mnemonic list for the correlated readout demo chip testing

Signal Name	Type	Address	Loc/Chan.
PHrst	40460 20V Driver	PI4000	MF: 2 Slot: 1 Chan.: 1
PH2	40460 20V Driver	PI4000	MF: 2 Slot: 1 Chan.: 2
PH1	40460 20V Driver	PI4000	MF: 2 Slot: 2 Chan.: 1
C-a0	40460 20V Driver	PI4000	MF: 2 Slot: 2 Chan.: 2
C-a1	40460 20V Driver	PI4000	MF: 2 Slot: 3 Chan.: 1
C-a2	40460 20V Driver	PI4000	MF: 2 Slot: 3 Chan.: 2
C-a3	40460 20V Driver	PI4000	MF: 2 Slot: 4 Chan.: 1
R-a3	40460 20V Driver	PI4000	MF: 2 Slot: 4 Chan.: 2
R-a2	40460 20V Driver	PI4000	MF: 2 Slot: 5 Chan.: 2
R-a1	40460 20V Driver	PI4000	MF: 2 Slot: 6 Chan.: 1
R-a0	40460 20V Driver	PI4000	MF: 2 Slot: 6 Chan.: 2
Rena	40750 20V LN Bias	PI4000	MF: 3 Slot: 1 Chan.: 4
Vref	40750 20V LN Bias	PI4000	MF: 3 Slot: 2 Chan.: 1
Vbias	40750 20V LN Bias	PI4000	MF: 3 Slot: 2 Chan.: 2
Vss(A)	40750 20V LN Bias	PI4000	MF: 3 Slot: 2 Chan.: 3
as0	40750 20V LN Bias	PI4000	MF: 3 Slot: 2 Chan.: 4
as-ena	40750 20V LN Bias	PI4000	MF: 3 Slot: 3 Chan.: 1
as1	40750 20V LN Bias	PI4000	MF: 3 Slot: 3 Chan.: 2
as2	40750 20V LN Bias	PI4000	MF: 3 Slot: 3 Chan.: 3
Vdd(D)	40750 20V LN Bias	PI4000	MF: 3 Slot: 3 Chan.: 4
Vss(D)	40750 20V LN Bias	PI4000	MF: 3 Slot: 4 Chan.: 1
ENA	40750 20V LN Bias	PI4000	MF: 3 Slot: 4 Chan.: 2
Vd(s)	40750 20V LN Bias	PI4000	MF: 3 Slot: 4 Chan.: 3
Vdet	40750 20V LN Bias	PI4000	MF: 3 Slot: 4 Chan.: 4

Table C.2 True table of analog selector

as0 as1 as2	Analog Selector Output
000	s1
001	s2
010	s3
011	s4
100	s5
101	s6
110	s7
111	s8

Table C.3 Pinout description for correlated readout demo chip

PAD #	PAD NAME	PAD DESCRIPTION	INPUT / OUTPUT
1	CI1	Output of Correlated CTIA #1	(O) SIGNAL OUTPUT
2	Vdet	Detector Bias	(I) DC BIAS
3	Vd(s)	Detector Bias Switch Control	(I) 0V or +5V DC
4	PHrst	Reset of Integration Capacitor	(I) +5V PULSE
5	Vout	Output Without Signal Processing	(O) SIGNAL OUTPUT
6	PH2	Correlated Switch 1	(I) +5V PULSE
7	PH1	Correlated Switch 2	(I) +5V PULSE
8	Vss(D)	Digital Vss	GND
9	C-a0	Column Decoder Input 0	(I) +5V PULSE
10	ENA	Column Decoder Enable	(I) 0V or +5V DC
11	C-a1	Column Decoder Input 1	(I) +5V PULSE
12	Ca2	Column Decoder Input 2	(I) +5V PULSE
13	C-a3	Column Decoder Input 3	(I) +5V PULSE
14	Vss(D)	Digital Vss	GND
15	Vdd(D)	Digital Vdd	(I) +5V DC POWER
16	Vdd(D)	Digital Vdd	(I) +5V DC POWER
17	R-a3	Row Decoder Input 3	(I) +5V PULSE
18	R-a2	Row Decoder Input 2	(I) +5V PULSE
19	R-a1	Row Decoder Input 1	(I) +5V PULSE
20	Rena	Row Decoder Enable	(I) 0V or +5V DC
21	R-a0	Row Decoder Input 0	(I) +5V PULSE
22	Vss(A)	Analog Vss	GND
23	Vref	OPAM Reference Voltage (V+)	(I) DC BIAS
24	Vbias	OPAM Bias Voltage	(I) DC BIAS
25	Vss(A)	Analog Vss	GND
26	VM21	Voltage Mode Output #2-1	(O) SIGNAL OUTPUT
27	VM22	Voltage Mode Output #2-2	(O) SIGNAL OUTPUT
28	VM11	Voltage Mode Output #1-1	(O) SIGNAL OUTPUT
29	VM12	Voltage Mode Output #1-2	(O) SIGNAL OUTPUT
30	DP1	Twin CTIA Output #1-1	(O) SIGNAL OUTPUT
31	DP2	Twin CTIA Output #1-1	(O) SIGNAL OUTPUT
32	Vdd(A)	Analog Vdd	(I) +5VDC POWER
33	Vdd(A)	Analog Vdd	(I) +5VDC POWER
34	as0	Processing Selection Input 0	(I) 0V or +5V DC
35	as-ena	Processing Selection Input 0	(I) 0V or +5V DC
36	as1	Processing Selection Input 0	(I) 0V or +5V DC
37	as2	Processing Selection Input 0	(I) 0V or +5V DC
38	DI1	Differential Integration Output #1	(O) SIGNAL OUTPUT
39	DI2	Differential Integration Output #2	(O) SIGNAL OUTPUT
40	CI2	Correlated CTIA Output #2	(O) SIGNAL OUTPUT

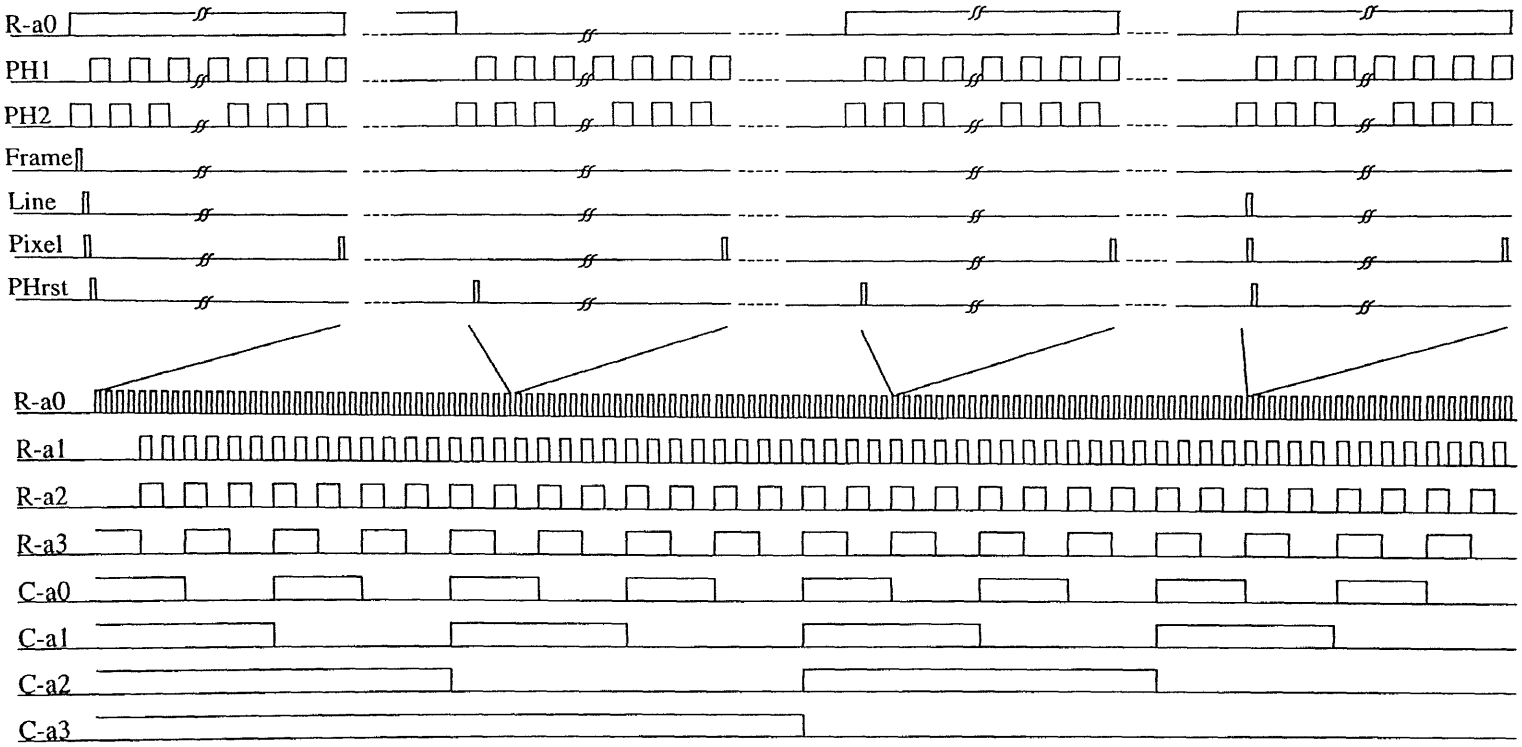

Figure C.1 Timing sequence for the correlated demo chip test.

Table C.4 Measurement results for frequency response testing

Period (μs)	Frequency (Hz)	Output Voltage (V)	Unified Value
10000	100	2.503	0.001
6000	167	2.594	0.045
4000	250	2.504	0.002
2200	455	2.607	0.051
2184	458	2.710	0.100
2168	461	2.801	0.143
2152	465	2.944	0.211
2136	468	3.125	0.297
2120	471	3.270	0.366
2104	475	3.274	0.368
2096	477	3.335	0.397
2088	479	3.434	0.444
2080	481	3.552	0.500
2072	483	3.621	0.533
2064	484	3.657	0.550
2056	486	3.695	0.568
2048	488	3.737	0.588
2040	490	3.756	0.597
2032	492	3.789	0.613
2024	494	3.802	0.619
2016	496	3.808	0.622
2008	498	3.840	0.637
2000	500	3.840	0.637
1992	502	3.829	0.632
1984	504	3.804	0.620
1976	506	3.785	0.611
1968	508	3.739	0.589
1960	510	3.699	0.570
1952	512	3.623	0.534
1944	514	3.617	0.531
1936	516	3.552	0.500
1928	519	3.482	0.467
1920	521	3.436	0.445
1912	523	3.440	0.401
1904	525	3.249	0.356
1888	530	3.133	0.301
1872	534	3.944	0.211
1856	539	2.780	0.133
1840	543	2.639	0.066
1824	548	2.542	0.020
667	1500	2.922	0.201
400	2500	2.750	0.119

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