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Dual material gate field effect transistor (DMG-FET)

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ABSTRACT

DUAL MATERIAL GATE FIELD EFFECT TRANSISTOR (DMG-FET)

by

Wei Long

Improving performance and suppressing short channel effects are two of the most important issues in present field effect transistors development. Hence, high performance and long channel like behaviors are essential requirements for short channel FETs. This dissertation focuses on new ways to achieve these significant goals. A new field effect transistor — dual material gate FET (DMG-FET) — is presented for the first time. The unique feature of the DMG-FET is its gate which consists of two laterally contacting gate materials with different work functions. This novel gate structure takes advantage of material work function difference in such a way that charge carriers are accelerated more rapidly in the channel and the channel potential near the source is screened from the drain bias after saturation. Using HFET as a vehicle, it is shown that the drive current and transconductance in DMG-FET are therefore substantially enhanced as compared to conventional FET. Moreover, it is observed that the short channel effects such as channel length modulation, DIBL and hot-carrier effect are significantly suppressed. Numerical simulations are employed to investigate the new device structure and related phenomenon. A simple and practical DMG-HFET fabrication process has been developed. The proposed DMG-HFET is thus realized for the first time. Experimental results exhibit improved characteristics as the simulation results predicted.

DUAL MATERIAL GATE FIELD EFFECT TRANSISTOR (DMG-FET)

by
Wei Long

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To the Memory of
My Parents

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CHAPTER 1

INTRODUCTION

1.1 Motivation

High performance high speed field effect transistors (FET), including MOSFET (metal-oxide-semiconductor FET), MESFET (metal-semiconductor FET), and HFET (heterostructure FET), have been playing increasingly important roles in high performance, high speed and high density IC applications, both analog and digital. High figure of merit values, such as high transconductance and drain impedance, are required. During the past decade, excellent high speed and performance have been achieved (see for example [1]) through improved design, the use of higher quality material, and the shink of the device structure. However, two major problems persist, namely, short channel effects and gate transport inefficiency.

The predominant feature of the detrimental short channel effects is high drain conductance, which also prevents the pinch off and leads to a shift in threshold voltage, and therefore V_T dependence on drain voltage [2], [3]. The phenomenon has been previously described in several cases of FETs (see for example [4]).

It has been demonstrated that the dual gate (DG) FET structure is an effective means to overcome the short channel effects [5], [6]. The DG-FET can be treated as a cascade connection of two FETs as long as the separation between the two gates is large compared to the channel thickness. But the evaluation of the dependence of its performance on DC bias and on its technological parameters is still extremely complicated due to an additional freedom of variables. Hence, it has become important that the dual gate analytical model be available for fully utilizing the benefits of the DG

structure, since the devices would have to be designed based on the analytic understanding of the device.

Gate transport efficiency is related to the average electron transport velocity traveling through the channel, which is related to the electric field distribution along the channel. In a field effect transistor, electrons enter into the channel with a low initial velocity, gradually accelerating towards the drain. As numerous numerical simulations of FETs indicate, the maximum electron drift velocity is reached near the drain [7]. The electrons move very fast in the region near the drain but relatively slow in the region near the source. Hence, the speed of the device is affected by a relatively slow electron drift velocity in the channel near the source region.

In 1989, M. Shur [8] theoretically suggested a split gate (SG) FET structure to enhance the gate transport efficiency. This device consists two closely separated gates with the gate closer to the drain having a positive voltage offset with respect to the gate near the source. Therefore, the electric field along the channel becomes more uniform and the electrons near the source are accelerated more rapidly. As a consequence, the average electron velocity in the channel is increased. However, the attempt to realize the SG-FET [9] has not been satisfactory up till now. The challenge is not only related to technological difficulties, but, above all, also to the inherent fringing capacitance between the two gates which rises significantly as separation of the two gates become close to or smaller than the channel depth as the device requires. This is detrimental to the device high speed performance. Thus, other ways have been looked for to take full advantage of the high efficiency electron transport without the inherent capacitance effect.

This thesis focuses on issues related to the reduction of short channel effects and the improvement of gate transport efficiency via dual gate or dual gate related approach.

Suppressing short channel effects hinges on an in-depth understanding of dual gate effects involved. Hence, the first part of this thesis attempts to present a new and simple analytic dual gate model by considering one of the most important parameters in calculating dual gate characteristics — the common node potential at the mid point between the two channels, fundamental treatment of which has been lacking in dual gate modeling.

Enhancing dual gate transport efficiency mandates a scaling in gate separation to less than channel thickness. As a consequence, parasitic gate to gate fringing capacitance [10] becomes dominant or comparable to intrinsic capacitance. This is extremely harmful to device's high frequency performance. Thus, a new approach to device structure design is needed. To this end, the split gate effect and the concept developed in the first part of this thesis for dual gate HFET are extended to a new device structure — a dual material gate (DMG) HFET. We select the HFET as a vehicle to explore the concept of DMG, which is presented in the main part of this thesis as a generic device structure, valid for all kinds of FETs, including MOSFET, MESFET, and HFET.

If we use two different materials with different work functions for the two gates in a DG-HFET, and merge them into one single gate by connecting them laterally, we obtain a DMG-HFET. The advantage of DMG is that both short channel effects and gate transport efficiency can be improved considerably. In the main part of this thesis, the simulation, structure design, processing realization, and measured characteristics of the DMG-HFET are presented in detail.

1.2 Scope and Organization

Introduction of a new device requires four steps: present approach overview, now approach analytic analysis, numerical simulations and practical realization. The existing approaches provide basis for new device. The physics based analytic models can give an overall knowledge and insight of device behavior and predict its dynamic characteristics dependence on its technological parameters and bias conditions. Numerical simulations serve the purpose of providing detailed data to illustrate complex device phenomena. Thus, with the help of these two approaches, one can predict the characteristics, and therefore selectively target technology optimizations. This leads to much improved effectiveness of experimental approaches with a large number of technological parameters.

The scope of this thesis is based on the following systematic methodology for our new device construction. The first step involves analytical modeling and calculation of dual gate HFETs. Secondly, in order to develop our new device structure, dual gate and split gate effects are investigated using numerical simulations. Then, the dual material gate structure is presented and compared with other related device structures. Afterwards, the proposed DMG structure is simulated and studied extensively. Finally, the optimized device structure supported by simulations is fabricated and tested.

In chapter 2, an overview of the state-of-the-art HFET is presented together with the design and optimization of the single gate HFET structures. The approaches employed in this thesis to develop new device structure are also discussed.

As we mentioned, the objective of this thesis is to develop a novel high performance DMG-HFET, which is virtually an extension the dual gate structure. Since analytic analysis has been lacking for DG-HFETs, it is carried out in first few chapters of

the thesis. In this part, Chapter 3 provides the background of a DC model and the calculation of DC I-V characteristics. The mechanism developed in Chapter 3 is then employed in Chapter 4 to calculate the key small signal characteristics. A systematic analysis needed for understanding of the origin of dual gate effect and for further device design and optimizations is also made.

Chapter 5 is concerned with the more detailed numerical simulation and study. Based on the theoretic approach, the novel device structure--dual material gate (DMG) FET--is proposed and its new features are outlined using HFET as the vehicle. Chapter 6 deals with the design, optimization and characteristic simulation of the resulting new DMG-HFET.

Finally, in Chapter 7, the DMG-HFET processing procedure is presented. Our goal is to realize the device which improves both short channel effects and gate transport efficiency. The fabricated DMG-HFETs are characterized under a wide range of bias conditions. As expected, the new device does exhibit greatly improved transport efficiency and significantly suppresses short channel effects, as our simulation results predicted.

Chapter 8 summarizes the conclusions of our research.

CHAPTER 2

BACKGROUND INFORMATIONS

2.1 Introduction

We have used HFET as a vehicle for the presentation of a new device structure as mentioned in preceding chapter. The HFET is a nature extension of the modulation-doping concept. By applying an external voltage across the heterojunction interface, one can modulate the 2DEG density, and thus its conductivity. Due to the high electron mobility, this novel device is the fastest three-terminal semiconductor device in the world and is very promising in ultra-high-speed/high-frequency applications. Today, there are tens of millions of HFETs in operation around world.

In this chapter, an overview of the state-of-the-art HFET is presented together with the design and optimization of the single gate HFET structures. The approaches employed in this thesis to develop new device structure are also discussed.

2.2 Development of HFETs

A breakthrough in HFET technology occurred when it was demonstrated that high quality, dislocation-free gallium indium arsenide (GaInAs) can be grown "pseudomorphically " on a GaAs substrate without misfit dislocations as long as its thickness is less than a certain critical thickness[11],[12],[13].This approach results in HFET structures with higher conduction band discontinuity and, consequently, higher 2DEG sheet density and modulation efficiency. As a result, the fT of state-of-the-art HFET's improved substantially, from 110 Ghz in 1987[14] to over 150 Ghz[15].

During this period, a significant amount of research and development also took place in the AlInAs/GaInAs material system, grown on an InP substrate[16],[17]. The conduction band discontinuity between AlInAs and GaInAs is considerably higher than other material systems, which results in a significantly higher 2DEG sheet density and modulation efficiency. This improvement yielded an approximately 33% increase in fT for state-of-the-art HFETs, from 150 to over 200GHz in 1988[18].

These dramatic improvements are also a result of significant advances in the fabrication of HFETs. The gate length of state-of-the-art HFETs has been steadily reduced, from 0.33um in 1984[19] to .05um in 1992[14]. At these short gate lengths, the effects of parasitic resistances become more pronounced and often mask the intrinsic device performance. As a result, a number of " mushroom- " or T-gate, and self-aligned gate process have been developed to reduce gate and parasitic source resistances, while still maintaining a small gate " footprint " [14],[20].

In addition, a great deal of work has been devoted to suppress the short channel effects of the HFETs. Several effective approaches, such as double-recessed structure[21], undoped surface cap structure[22], lightly doped drain structure[23], and low conductance drain[24], have been demonstrated. Significant improvements in short channel effect behaviors have been achieved.

2.3 Principles of Operation

The basic principles of operation of HFET can be described by a one dimensional(1-D) charge control model in the direction perpendicular to the heterojunction interface, which was developed by Delagebeaudeuf *et al* [25]. It was assumed that, for $0 < Ns < Nso$.

$$qNs==Cs(Vg-Vth) \qquad (2.1)$$

where Ns is the 2DEG sheet density, q the electrostatic charge, Cs the 2DG capacitance per unit area, Vg the applied gate voltage, and Vth the threshold voltage.

Despite its simplified assumptions, the charge control approximation correctly predicts the linear dependence of Ns on Vg. The real behavior, however, rapidly deviates from a simple linear relationship when Ns versus Vg curve approaches its upper bounds (Nso). This nonlinear charge control characteristic is associated with the onset of parasitic charge modulation in the wide-band gap material. The gate potential modulates the 2EDG electrons and their parent donors simultaneously, resulting in a nonconstant capacitance. This mechanism is responsible for the premature saturation of Ns in a modulation-doped structure and leads to degradation in device performance.

The modulation efficiency is a useful concept in the design and analysis of FET structures[26],[27]. Loosely speaking, it indicates how efficiently an FET modulates the total channel charge (Qtot) in order to produce an incremental change in drain current (Ids):

$$\text{efficiency} = \eta \propto \text{delta(Ids)/delta(Qtot)} \qquad (2.2)$$

Since Qtot is made up of various charge components, each with an unequal contribution to Ids, one must examine the rate of change of each of these components separately.

In a HFET structure, the only charge component that contributes to Ids is that of the 2DEG(Ns); the other " parasitic " components, such as donor bound electrons and low velocity electrons that reside in the wide-gap material, contribute essentially nothing to Ids. We now examine the simplest case in which the modulation of charge is assumed to be uniform over the entire length of the gate. We assume that all electrons in the 2DEG

travel at their saturated velocity (Vsat) over the entire length of the gate while those residing in the wide-gap material --- bound and free --- are stationary. Thus, the rate of charge of Ids with respect to Qtot is given by

$$\Delta Ids/\Delta Qtot = \Delta (q\ Vsat\ Ns)/\ \Delta(Qtot)$$

$$= Vsat\ \Delta\ (q\ Ns)/\ \Delta(Qtot) \qquad (2.3)$$

Comparing (2.2) and (2.3), one can define the modulation efficiency, η, as the ratio of the rate of change of the "useful" charge over that of the total charge, i.e.,

$$\eta = \frac{q\Delta Ns / \Delta Vg}{\Delta Qtot / \Delta Vg} = \frac{q\Delta Ns / \Delta Vg}{C_{tot}} \qquad (2.4)$$

Since $\Delta Qtot > q\Delta Ns$, $0 < \eta < 1$. An η of 1.0 represents the most efficient state of operation in which only the 2DEG sheet charge is being modulated by the gate voltage.

The current gain cutoff frequency (f_T) of a HFET, which is the most useful figure of merit for assessing device speed, is thus given by

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{q\, v_{sat} (\Delta Ns / \Delta Vg)}{2\pi L_g Ctot} \qquad (2.5)$$

where g_m is the device transconductance, Cgs is the total gate capacitance, and L_g is gate length.

Substitute (2.4) into (2.5), one obtains

$$f_T = \frac{v_{sat}}{2\pi L_g} \eta \qquad (2.6)$$

Thus the excess charge modulation reduces the f_T by a factor equal to η. η assumes the gate bias dependence of f_T as well as the differences among various types of FET's of similar gate length and saturation velocity.

Since the distribution of 2DEG electrons(Ns) and electron velocity are nonuniform along the gate, the modulation of charge is not as efficient as the ideal case that all electrons in the 2DEG travel at their saturation velocity (Vsat) over the entire length of the gate. Thus in order to support the same amount of current, the gate has to modulate more charges, particularly near the source end of the gate where the electron velocity is lowest. As a result, the modulation efficiency along the gate is always less than unity; and its magnitude depends on Ns, as well as the difference in Ns at the source and drain ends of the gate or the velocity distribution along the gate.

It is clear from the above discussion that one can establish the following relationship:

$$gm = Cs\ Vsat\ \eta \tag{2.7}$$

The maximum transconductance is achieved by improve η to reach the value of unity. Thus for a given gate length, and gate to channel thickness, the intrinsic transconductance of a HFET depends solely on the modulation efficiency.

This formulation has offered new insights on HFET's principles of operation. It was therefore found that smaller conduction band discontinuity(ΔEc) material system modulates more parasitic charge components, causing more severe reduction in HFET overall modulation efficiency.

2.4. Dynamic Performance of Short Channel HFET

2.4.1 Parasitic Effects

Since the speed of an FET is traditionally limited by the electron transit time, the most obvious approach to improve this speed has always been a reduction in gate length.

Unfortunately, as the gate length approach the 0.1μm regime, this strategy is no longer effective. At such a short gate length, the electron transit time is comparable to, or even smaller than, other parasitic delays in the device. Consequently, as the gate length is reduced, a simultaneous effort must be made to proportionally reduce the various parasitic delays as well. Among those, the parasitic capacitance charging time (gate pad, gate fringe, etc.), the source resistance, and drain delay (due to the extension of the drain depletion region), are the dominant delays and must be further reduced[29],[15].

Here, we describe the parasitic effects using a small signal model that takes into account the charging time associated with the gate pad (t_{pad}) and gate fringe (t_{fringe}) capacitances, as well as an additional parasitic delay due to the extension of the drain depletion region beyond the gate edge (t_{drain})[30]:

$$t_T = t_{pad} + t_{fringe} + t_{drain} + t_i = \frac{1}{2\pi f_T} \tag{2.8}$$

where t_T and t_i are the total and intrinsic delays, respectively. For simplicity, we left various terms, such as the output conductance (g_{ds}), and feedback capacitance (C_{gd}), and drain resistances (R_d), for later consideration.

For a field effect transistor with a pad capacitance C_{pad}, extrinsic transconductance g_m, and gate width, t_{pad} is approximately given by

$$t_{pad} = \frac{C_{pad}}{g_m} \tag{2.9}$$

where C_{pad} is typically 10 fF per 50×50-μm bonding pad. Although often ignored, this parasitic charging time has been found to account for a significant portion of the total

delay in ultra-short gate length FET's. For instance, a t_{pad} of 0.33 ps is estimated for a 30 μm wide device with g_m = 1000 mS/mm and C_{pad} = 10fF, which is as much as 60% of the intrinsic delay of a 0.1μm gate length AlGaAs/GaInAs MODFET[15].

Similarly, the gate fringe capacitance charging time is given by

$$t_{fringe} = \frac{C_{fringe}}{g_{mo}} \tag{2.10}$$

where g_{mo} is the intrinsic g_m and is approximately related to the extrinsic g_m and source resistance Rs by the relationship:

$$g_m = \frac{g_{mo}}{1 + g_{mo} \cdot R_S} \tag{2.11}$$

Thus the presence of R_S affects only the gate pad, but not gate fringe, capacitance charge time. This fringe capacitance is typically 0.18 pF/mm for HFETs.

The drain delay (t_{drain}) due to the extension of the drain depletion region is a difficult parameter to be obtained with high accuracy. For state-of-the-art MODFET's, t_{drain} introduces an additional 0.1-0.2 ps delay at low drain bias voltages [14].

From (2.3), the intrinsic delay at a particular bias condition is given by

$$t_i = \frac{C_{gs}}{g_{mo}} = \frac{L_g}{v_{sat} \cdot \eta} \tag{2.12}$$

where η is the modulation efficiency. Typically, t_i is equal approximately 0.4-0.6 ps for 0.1 μm gate length HFETs.

2.4.2 The Effects of Feedback Capacitance and Drain Conductance

In above discussions, we have taken into account the effects of the parasitic elements in addition to the major parameters, namely C_{gs} and g_m. Similarly, as the gate length continues to decrease, the effects of the feedback capacitance C_{gd} and drain conductance g_{ds} become more and more important. When these term are included, it can be shown that (2.4) must be modified as follows[31]:

$$t_T = \frac{C_{pad}}{g_m} + \frac{C_{gs} + C_{fringe} + C_{gd}}{g_{mo}} \cdot [1 + g_{ds}(R_s + R_d)] + C_{gd}(R_s + R_d) \qquad (2.13)$$

Therefore, in order to avoid excessive delays associated with g_{ds} and C_{gd}, one must ensure the following:

$$g_{ds}(R_s + R_d) \ll 1 \qquad (2.14)$$

and

$$\frac{g_{mo}}{1 + (C_{gs} + C_{fringe}) / C_{gd}} (R_s + R_d) \ll 1 \qquad (2.15)$$

Since g_{mo} must be increased with reduced gate length, one must proportionally reduce g_{ds} and C_{gd} in addition to the reduction of parasitic resistances, Rs and Rd, in order to minimize the effects associated with them.

It has been demonstrated that both g_{ds} and C_{gd} are strong functions of drain bias and drain recessed width[32]. This is due to the extension of drift region as a space charge layer by drain bias. Thus, the g_{ds} and C_{gd} could be reduced largely by increasing the recess width and drain bias. For high performance short channel HFETs a

highly doped cap layer is necessary to reduce the parasitic resistances. Therefore a recessed device configuration is employed. However, the performance of the device depends strongly on the shape of the recess configuration. A narrow recess leads to a low g_{ds} and high C_{gd}, whereas a wide recess introduces a current limiter, especially at the source. Therefore an asymmetric recess configuration is needed. A wider recess at the drain side can be used to reduce feedback and improve breakdown. A narrow recess at the source side leads to a low parasitic source resistance.

2.4.3 f_{max}, an Important Figure of Merit of RF HFETs

In above discussions, we concentrated on f_T, which is certainly an important figure-of-merit, especially in terms of digital performance. But with regard to RF performance, f_{max} is probably better indicator of high frequency performance. From reference [31], f_{max} can be expressed below:

$$f_{max} = \frac{f_T}{\sqrt{4\frac{g_{ds}}{g_{mo}}\left(g_{mo}R_g + \frac{R_s + R_d}{1/g_{mo} + R_s}\right) + \frac{4}{5}\frac{C_{gd}}{C_{gs}}\left(1 + \frac{2.5C_{gd}}{C_{gs}}\right)(1+g_m R_s)^2}} \qquad (2.16)$$

Equation (2.11) demonstrates that f_{max} takes more into account the losses associated with gate resistance, R_g, output conductance, g_{ds}, and gate drain feedback capacitance C_{gd}. Moreover, the ratios $\frac{g_m}{g_{ds}}$ and $\frac{C_{gs}}{C_{gd}}$ gain more influence. It should be noted that a device that is optimized for high f_{max} is not usually operated at optimized f_T. Therefore, it is not practicable to have a single device working simultaneously at highest

$f_{\max}$ and f_T. Instead many approaches are devoted to considerably improving $\frac{g_m}{g_{ds}}$, $\frac{C_{gs}}{C_{gd}}$, and small signal gain of ultra-short gate-length HFETs while not significantly degrade f_T.

2.4.4 Other Short Channel Effect Related Issues

Performance of short channel FETs is a strong function of device aspect ratio (the ratio between the gate length and effect gate-to-channel separation). Many key parameters, such as g_m, g_{ds}, $\frac{g_m}{g_{ds}}$ and $\frac{C_{gs}}{C_{gd}}$, degrades due to the reduction in aspect ratio. Thus, as the gate length of an FET is reduced, one must also proportionally reduce its vertical dimensions in order to maintain a reasonably high aspect ratio and thereby acceptable short channel effects. This geometrical parameter is a very important factor in controlling the field effect action of a transistor, and should be maintained above five[30].

For a given gate length, one can often increase the device transconductance and suppress short channel effects by reducing the gate-to-channel separation or increase the aspect ratio. This will also result in high speed or lower parasitic delays, which is proportional to the parasitic capacitance divided by transconductance.

2.5 The State-of-the-art Approaches of Short Channel HFETs

Significant improvement has been achieved in the area of short channel HFETs. Numerous device structures and excellent performance (e.g. $f_{\max}$, f_T, breakdown and

gain) have been reported in the literatures. However, due to complicity and often controversy behaviors, it is difficulty to merit all the parameters in a single device. Thus different approaches are often aimed to optimize one or some of the key parameters for specific applications. In this section, we discuss approaches of the state-of-the-art HFETs and the physics behind these approaches.

2.5.1 Self-aligned Gate and Ohmic Contact

In the presence of parasitic effects, the extrinsic f_T of a short gate length HFET is no longer inversely proportional to its gate length. In order to improve the speed of ultra-short gate length HFETs, self aligned gate scheme was used to allow the source and drain contacts to be " self-aligned " to the gate[33]. In this technology, additional ohmic contacts are evaporated in a self aligned process using the T-gate structure as mask. The corresponding self-aligned gate HFETs exhibited a factor-of-2 reduction in delays associated with g_{ds} and C_{gd}, due to their extremely low Rs and Rd. This is expected by (2.13) and (2.14). Moreover, for a 0.1μm gate length devices reported in [34], ~70% reduction in the Rs and Rd resulted in an increase in extrinsic transconductance approximately 22%, from 900 to 1100 mS/mm, and that in extrinsic f_T approximately 15%, from 200 to 230 GHz. With further optimization, the state-of-the-art self-aligned HFET with extrinsic transconductance of 1580 mS/mm and extrinsic f_T of 340 Ghz have been achieved for a 0.05 μm pseudomorphic HFET[35].

Another very attractive self-aligned gate structure is the lightly doped drain (LDD) structure[23]. The fundamental concept of this approach is the decrease of

maximum electric field along the channel. It shows low parasitic resistance, low drain conductance and high breakdown voltage. In addition, since the breakdown voltage is related to the strong electric field at the drain side of the gate, asymmetric LDD structures, such as lightly doped deep drain structure and long lightly doped drain[23], have therefore been proposed to further increase the drain breakdown voltage while the small source resistance.

2.5.2 Double-recessed Technique

HFETs with short gate length suffer from a high drain conductance, g_{ds}, low voltage gain $\frac{g_m}{g_{ds}}$ and low breakdown voltage, which consequently degrade the $f_{\max}$ and other performance. For many applications especially RF power, it is desired to have high breakdown voltage. Three advantages of high breakdown voltage are known: (1) higher breakdown has been attributed to longer life times[36]; (2) higher breakdown allows higher drain operating voltage which translates to a higher output power density as long as the power gain is sustained. (3) Higher drain operating voltage usually leads to lower g_{ds} and C_{gd}, and consequently higher voltage gain and $\frac{C_{gs}}{C_{gd}}$ ratio. Thus it is desirable to develop a HFET that has a breakdown voltage appropriate for the intended drain operation voltage.

An effective method for suppressing short channel effects and increasing the breakdown voltage is to use a double-recessed gate process. We know a wide recess width allows the spreading of the space charge while a narrow recess leads to small

source resistance. Therefore, the double stepped recess with gate close to the source combines the advantages of narrow recess (high transconductance and drain current) and wide recess (high breakdown voltage, low output conductance and low feedback capacitance). These leads to high RF performances.

An important issue is associated with distance, L_{gd}, between the gate metal edge and the N+ cap layer on the drain side of the device. In short gate-length HFETs, L_{gd} can have a profound effect on both the DC current-voltage characteristics and RF gain of device due to the extension of drift region. Increase L_{gd} benefit FET performance by reducing the output conductance and the gate to drain feedback capacitance[21]. It was shown that longer L_{gd} HFETs have simultaneously improved $\frac{C_{gs}}{C_{gd}}$, $\frac{g_m}{g_{ds}}$ and g_m in extremely short gate-length HFETs. Excellent $f_{\max}$ and gain have been achieved while not seriously degrading the f_T using double recess and longer L_{gd} [21].

2.5.3 V-shaped Spike Gate FETs

Both low-voltage and high efficiency operations are major concerns for the power applications. The narrowed voltage swings is due to the presence of the knee voltage of FETs which is originated from the on-resistance. This ends up with decreasing the available output power as well as the drain efficiency. In order to reduce the on-resistance, shrinking the channel length is most effective, however, as mentioned earlier, shortening the channel causes higher drain conductance that reduces the power gain and thereby the power added efficiency(PAE).

Recently, Tsuyoshi *et al* [22] reported very short channel HFETs using a V-shaped spike gate structure, which was first proposed by Kohn[37], in order to reduce the on-resistance. It was shown that this V-shaped structure can suppress the increase of drain conductance, because the depletion widening from the fringe of the V-shaped gate alleviates the electric field between the gate and drain. A lowest on-resistance ever reported by using the unique gate structure has been achieved. The attained on-resistance was less than a half of that without V-shaped spike. The implemented device achieved the PAE of 70% with 31.5 dBm output power at drain bias of 1.5V for the first time[22].

2.5.4 Dual Gate FETs

The advantage of dual gate structure comes from the added functionalities obtained by integrating two independent FET's in a compact manner. Compared to the single gate FET, a dual gate FET of the same gate length provides the same input impedance with higher output impedance, higher breakdown voltage, higher power gain, and much reduced feedback capacitance. This is mainly due to the second gate which increases the effective gate length and the distance between first gate edge and the drain end, therefore, also increases the aspect ratio, which suppresses short channel effects. However, the penalty of the improvements is also due to the increasing of the total effective gate length. This produces higher gate capacitance and lower transconductance, and consequently, lower f_T. Thus, a trade-off is required to optimize dual gate FETs.

2.6 Primary Goals of This Research

In the view of the trend of improving FET performance, device structure based on asymmetric design have become very attractive. Several new approaches, such as asymmetrical double-recessed structure[21], asymmetrical lightly doped drain structure[23], low conductance drain[24], and asymmetrical channel doping FETs[38],[39], have been demonstrated to be very effective in suppressing short channel effect, increasing the breakdown voltage and/or enhancing transconductance. In this work, we propose a new type of FET structure, the dual material gate field effect transistor (DMGFET), which is presented to suppress short channel effects and enhance transconductance simultaneously. The special feature of this new structure approach is that the improvements are due to the modification of electric field along the channel. We will show that this structure can considerably reduce drain conductance and improve transconductance. Like other device structures, this device has its inherited demerits besides the merits. Although the DMGFET exhibits lower g_{ds}, Cdg and higher g_m, its Cgs tends to be higher. Thus, a proper treatment of these parameters will require a trade-off. Another related issues is the manufacturing. Here we have limited ourselves to the ideal structural effect. Therefore more issues related to manufacturing are not addressed. Hence further works are still needed to obtain more stable/repeatable processing methods and, especially, to control the two gate contacts which are functions of many experimental parameters.

2.7 Scope and Methodology Used in This New Structure Development

In this work, we employ analytical modeling, device simulation and experimental data for the new structure study. Analytical model provides good physical insight. Device numerical simulation is a good tool for different structure comparison or trend prediction. The experimental approach is thus guided by simulation and analytical models.

Although the proposed DMGFET is a single gate FET, it has a structure like dual gate FET. We therefore expect that it has the benefits of both single and dual gate structures. In order to take full advantage of the dual gate effects, we first study the principles of operation of the dual gate HFET: Chapter 3 will outline the dual gate intrinsic I-V characteristics for the simplest case using simple analytical approach. To understand dual gate small signal behavior, Chapter 4 will discuss its key small signal parameters. In Chapter 3 and 4, we will simulated and studied dual gate InAlAs/InGaAs HFET, since this device is an ideal test vehicle for dual gate effects discussed in the chapters and we previously studied experimental dual gate HFET behaviors using this material system[40].

The rest chapters will be devoted to the new device structure, DMGFET. We will emphasize the pseudomorphic InGaP/InGaAs HFET since this device is most suitable for stable and simple device fabrications. The device structure and parameters employed in this study are primary come from the real material structure we used for experimental processing, which was provided by Bell Labs, Lucent Technologies.

A 2-D device simulator, PISCES, is used as a numerical tool to investigate the presented new device structure and other related device structures. It should be noted that PISCES is not a well developed tool for HFETs simulations, since some of the models it

used are far under/over-estimation of the real HFET behavior. Thus this simulator is used to serve as a tool to predict the trend of device behavior under different structures. In order to make the best comparisons, we will usually fix the channel doping Nso, gate-to-channel thickness and other vertical device parameters unchanged for devices simulated. The detail of this parameters used are presented in the Appendix A.

2.8 Summary

We have presented an overview on the state-of-the-art single gate HFET and the trends in improve single gate HFET performances. It was demonstrated that increase modulation efficiency and reduce parasitic and short channel effects are extremely important in achieving ultra-high-performance short channel HFETs.

We anticipate that the DMGFET will demonstrate enhanced overall electron velocity along the channel and therefore increased modulation efficiency. In addition, the short channel effects could be suppressed by this novel structure. Therefore, this new device can be a promising candidate for the applications such as low noise FET(needs high gm and low gds, Rs, etc), power amplifiers (high gm/gd ratio, low gds, Rs, Cdg, etc.), and digital integrated circuits(high modulation efficiency, low parasitic, etc.).

CHAPTER 3

ANALYTIC MODEL FOR DG-HFET DC CHARACTERISTICS

3.1 Introduction

Our development of analytical dual gate (DG) model starts with a closed form analytic single gate model proposed by Khondker et al [41], which has been successfully used for the prediction of single gate HFET behavior, and then proceeds through a set of simplifying assumptions to arrive at a novel expressions for the common node potential between the two gates that determines the operating status under each gate. For single gate, the DC I-V behavior, which is described in term of the two possible operating regions, is simply determined by given external biases. Whereas for dual gate, it is determined by specifying the common node potential in addition to the external bias conditions. Hence, to characterize the operation of dual gate analytically, we can not simply plug in the given external bias values into single gate equations, rather we have to solve for the common node potential under the given biases before the single gate analytic equations can be used. This points out that the major work needed for the dual gate model is to figure out external bias dependence of the common node potential.

Consider the DG-HFET to be composed of two single gates in cascade, its common gate potential can be obtained by determination of the intersection of two HFET I-V curves. Due to the complicated expression of HFET I-V behavior, we have to resort to non-analytic method which involves a numerical procedure. However, if we assume that the non-linearity in the whole linear operating region is weak, and that after both gates are in saturation, most of the excessive drain-source biasing voltage V_{ds} is dropped under the second gate near the drain, then the common node potential or the

intersection point can be calculated simply through analytic equations. Hence, we postulate that under those simplifying assumptions, the common node potential is governed by the analytic expressions thus derived, which forms the cornerstone of our dual gate analytic model.

In this chapter, we present the above-mentioned analytic methodology for calculating the DG-HFET I-V characteristics from the simplified analytic equations. A detailed derivation and discussion are presented in this chapter, which is organized into three main sections.

The first part, Section 3.2, is devoted to the derivation and simplification of the single gate HFET analytic model, which was originally presented by Khondker et al [41]. The Sub-Section 3.2.1 deals with the setting up of the I-V expressions based on charge control principles, while 3.2.2 presents an important simplification to the I-V expressions which permits us to calculate simple closed form expressions for DC characteristics.

In the beginning of Section 3.3, we discuss the approximations and outline the derivation of dual gate common node potential equations from single gate equations. The section concludes with a closed form expression for common node potential, which has external bias conditions as parameters. It is important to understand the dependence of common node potential on external biasing, since it determines how external biasing influences the operating status of the two HFETs, and therefore, the performance of the DG-HFET. This forms the subject of discussion in Sub-Section 3.3.2.

Finally Section 3.4 discusses the analytic methodology that allows one to calculate the DG-HFET I-V characteristics from a knowledge of device physical structure and bias parameters. Calculation and discussion of the key small signal parameters of DG-HFET forms the subject of the next chapter in which we first derive the closed form

expressions for those parameters, and then employ the machinery developed in this chapter to calculate DG-FET's behavior and discuss the dual gate effects.

3.2 Analytic Single Gate Modeling

The closed form analytical model for calculating the I-V characteristics and the small signal parameters of HFETs can be developed through a properly selected velocity - electric field (v_d-E) empirical expression. Khondker et al [41] used such an approach to give simple analytic expressions for single gate HFET I-V characteristics and the small signal parameters. In this section, the method we use to develop our dual gate HFET analytic model is in essence similar to Khondker et al.'s method.

Theoretical work[42] has been very critical of the use of a v_d-E curve in short channel device modeling. The recent literatures include a number of papers that deal with the current - voltage characteristics (I-V) of HFETs [43]–[47]. In these analytical models, several empirical relationships of the electron drift velocity-electric field ($v_d - E$) dependence have been used to achieve a fit to the experimental I-V data [44], [45], [46], [47]. In this thesis, we use the approximation used by Khondker et al [41] and illustrated in Fig.3.1:

$$v_d = \frac{v_s E}{\sqrt{E^2 + {E_c}^2}} \tag{3.1}$$

where v_d is the electron steady-state drift velocity, v_s the saturation velocity, E the electric field, and $E_c = v_s / \mu_o$, with μ_o as the low field mobility. It is instructive to notice that although the relation in (3.1) does not account explicitly for transient velocity overshoot, the phenomenon is partially implied in the assumption that the electron

velocity remains close to its peak value for channel field beyond E_c [42]. Furthermore it was shown that this type of velocity field relation produces the same current and transconductance as those resulting from the use of a hydrodynamic transport model which allows velocity overshooting[42]. It should be noted that in GaAs the equilibrium electron velocity goes down after reaching the maximum due to k-space transfer[49]. Therefore, equation (3.1) is approximately used in the interest of using an analytically solvable expression. It is probably fair to say that this is a weak link in this modeling.

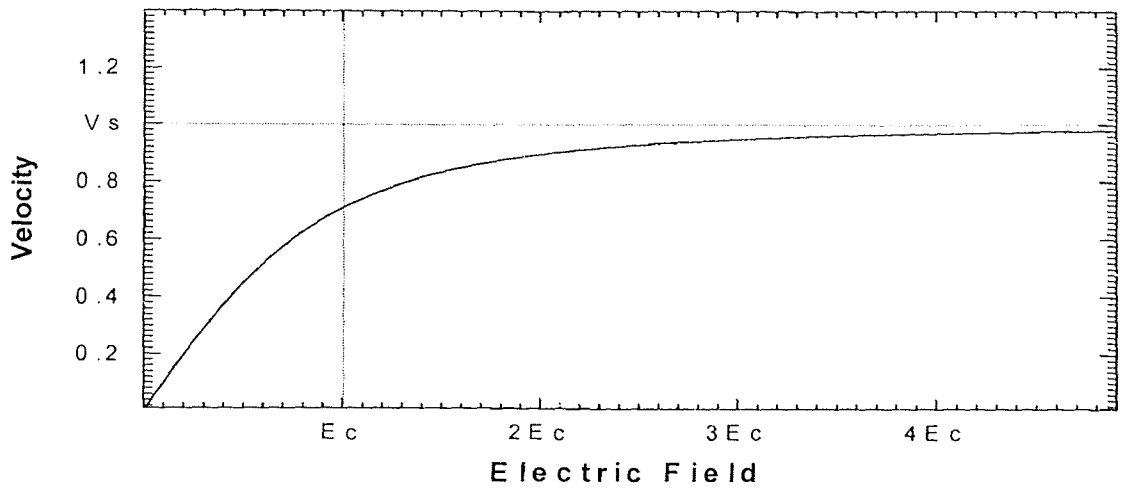


Fig. 3.1 The relationships of $(v_d - E)$ dependence defined by equation (3.1).

The charge control model for device analysis has been used extensively [50],[51],[53], due to its apparent simplicity. In the derivation, the electron density in the channel of the HFET shown in Fig.3.2 is assumed to be governed by the following basic charge control equation:

$$n_s(x) = \frac{\varepsilon_2}{q(d_i + \Delta d)}(V_{gs} - V(x) - V_{to})$$

$$= \frac{\varepsilon 2}{qd}(V_{gs} - V(x) - V_{to}) \tag{3.2}$$

where n_s is the channel electron area density, ε_2 is the permittivity of InAlAs, d_i is the thickness of the InAlAs layer, Δd is the moment distance of the electrons from the hetero-interface [45], V_{gs} and $V(x)$ are the applied gate voltage and the channel potential at any point x, respectively, and V_{to} is the threshold voltage of the device. this equation is valid for $0 \leq n_s \leq n_{s0}$, where n_{s0} is the maximum 2DEG sheet density. However, the linear $n_s(V_{gs})$ approximation of (3.2) under estimates n_s close to pinchoff, which predicts a lower subthreshold current than measured[45], [52], [53]. For n_s near n_{s0}, the above model ignors the fact that there is a gradual saturation of the 2DEG concentration as the gate voltage increases[54]. It therefore predict only a maximum transcoductance instead of a peak, which is experimentally observed(e.g., [55]).

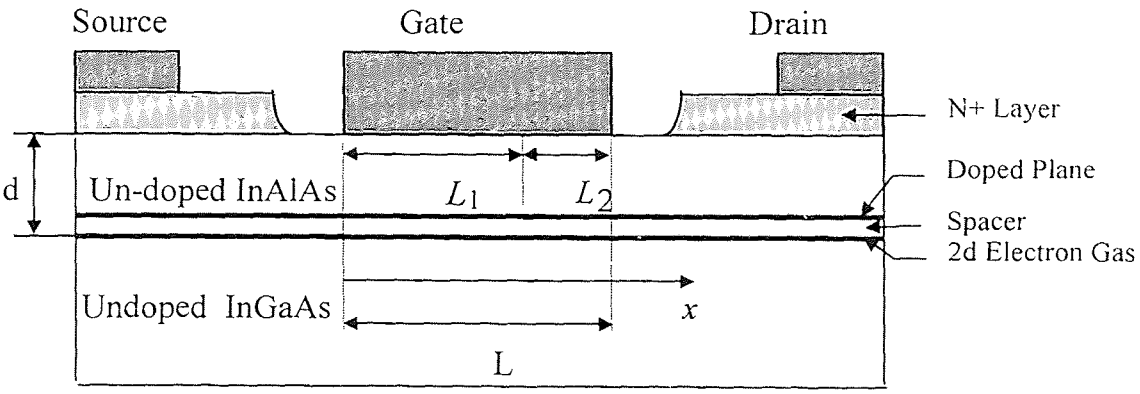


Fig. 3.2 A Cross-sectional Schematic Diagram of a Single Gate HFET Structure.

The simplest analytical HFET I-V models are those utilize the linear charge control approximation, equation (3.1), and integratable velocity-field models [52], [53]. The current in the channel of a HFET is given by $I_c = q\, n_s(x) W v_d(x)$, where W is the gate width. Substituting (3.1) and (3.2) in the expression for I_c yields

$$I_c = G_0[V_{gs} - V(x) - V_{t0}]\frac{E}{\sqrt{E^2 + E_c^2}} \tag{3.3}$$

where $G_o = \varepsilon_2 W v_s / d$ and $E_c = v_s / \mu_0$. Note that I_c is constant across the channel length.

After integrating (3.3) from x = 0 to x = L, the gate length, and rearranging, we have

$$I_c[D_2(t_L) - D_2(t_0)] = -\frac{v_s L G_0}{\mu_0} \tag{3.4}$$

where

$$t_0 = \frac{I_c}{G_0(V_{gs} - V_{t0} - I_c R_s)} \tag{3.5}$$

$$t_L = \frac{I_c}{G_0(V_{gs} - V_{t0} - V_{ds} - I_c R_d)} \tag{3.6}$$

and

$$D_2(z) = \int_z^1 dt \frac{\sqrt{1-t^2}}{t^3}, \qquad 0 < z < 1 \tag{3.7}$$

which upon integration yields

$$D_2(z) = \frac{\sqrt{1-z^2}}{2z^2} - \frac{1}{2}\ln\frac{1+\sqrt{1-z^2}}{z}, \quad 0 < z < 1 \tag{3.8}$$

Which is an analytical expression and where z is a dummy variable which may not need to define.

The linear region I-V characteristics of HFETs can be easily calculated using (3.4). For drain current greater than minimum saturation current, a technique similar to that proposed by Grebene and Ghandi [56] for MESFET and used by Chang and Fetterman [41] is followed. Near saturation the gradual channel approximation (GCA) becomes invalid since the longitudinal component of the electric field is no longer negligible. Therefore, one has to solve a two-dimensional Poisson equation in a region where the GCA break down. Hence, for saturation region, the channel of length L is divided into two zones. In zone L_1 the GCA is valid, whereas in zone L_2 a two-dimensional Poisson equation must be solved. The extent of the first region L_1 is calculated with the help of (3.4), which can be rewritten, considering that saturation has taken place, i.e., $D_2(t_L)$=0 and t_L = 1, we get

$$L_1 = \frac{\mu_0 I_c}{v_s G_0} D_2(t_{0s}) \tag{3.9}$$

In the second region, the longitudinal component of the electric field is not negligible. The field and potential distributions within these boundaries can be obtained by solving the two-dimensional Poisson's equation. The second region is assumed to be completely depleted. The analytic solution is based on the method develped by Chang and Day [57], and the assumptions and boundary conditions are similar to those used in [46]. They are: 1) there is continuity of potential, 2) there is discontinuity of the transverse field at the heterointerface due to 2DEG, and 3) the space charge layer ends at the gate edge. From the solution we obtain the following expression for the depletion region length along the channel:

$$L_2 = \frac{2d}{\pi} Sinh^{-1}\lambda \tag{3.10}$$

where

$$\lambda = \frac{\pi}{2d\,E_0}(V_{ds} - V_{gs} - V_{t0} + I_c(1/G_0 - R_d)) \tag{3.11}$$

where $E_0 \approx 7E_c$, is the field at which the electron drift velocity equals $0.99\,v_s$. Using (3.10) and (3.11), the length of the channel, which is the summation of L_1 and L_2, can now be written as

$$L = L_1 + L_2 = \frac{\mu_0 I_c}{v_s G_0} D_2(t_{0s}) + \frac{2d}{\pi} Sinh^{-1}\lambda \tag{3.12}$$

which yields the current-voltage characteristics beyond saturation. It should be noted here that, in order to be analytically solvable, the above derivations neglect the effects of dipole domain and drain depletion region extension. This will yield rather small values of drain conductance and drain to gate feedback capacitance as compared to those experimentally found for practical devices with comparable dimensions [58],[59],[60],[61],[62].

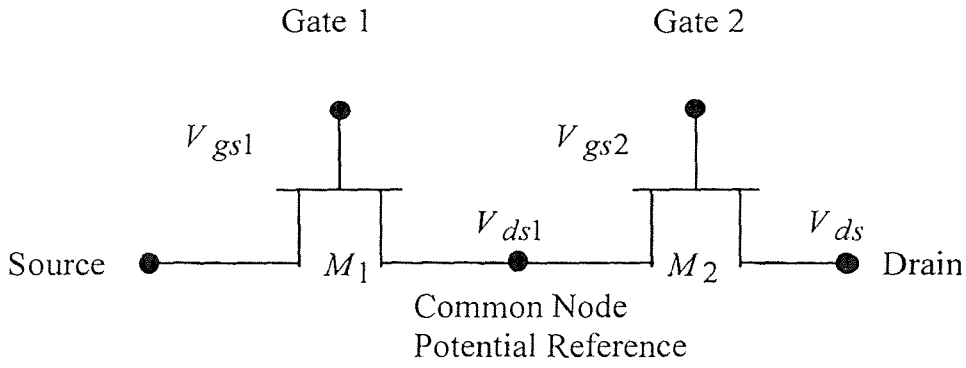


Fig. 3.3 Configuration of dual gate HFET.

3.3 The Common Node Voltage Model of Dual Gate HFETs

An analytical description of the dual-gate HFET can be constructed through the series connection of the channels of two single-gate devices as indicated in Fig. 3.3. When analytical behavior of these two gates in cascade is characterized for dual gate devices, the usual analytical approach loses much of its efficiency and insight, and usually requires the use of numerical programs to solve for the common node voltage V_{ds1} between the two gates. Under these circumstances, where a detailed and accurate V_{ds1} model is desired, particularly when the microwave small signal parameters is of interest, closed form common node V_{ds1} models are of crucial importance and are the key to the problems. These closed form V_{ds1} expressions can be used to conveniently determine not only the terminal I-V characteristics, but also the main small signal equivalent circuit parameters which are needed to represent the device microwave characteristics. Moreover, these models provide a good deal of insight into the correct operation regions of the two channels for proper utilization of the dual gate HFET.

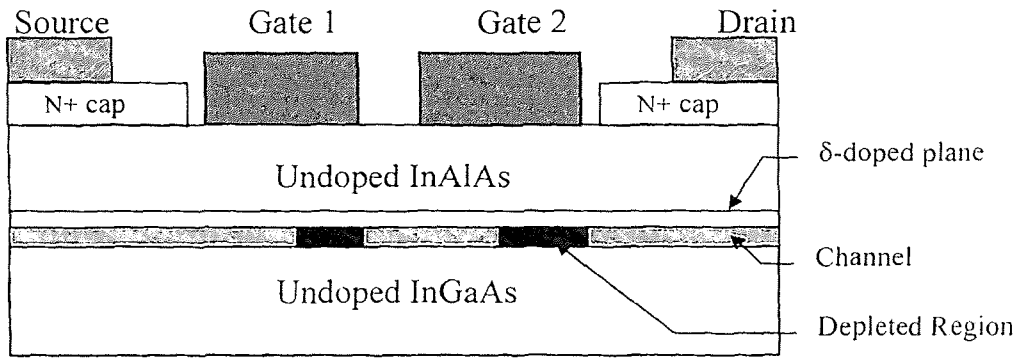


Fig. 3.4 A cross section schematic diagram of the dual gate HFET structure showing depleted regions below each gate when both gates are biased into saturation.

3.3.1 The Analytic Model

The structure of a typical DG-HFET is shown in Fig. 3.4. The device is assumed to be uniform in gate width direction with an overall width of W for both gates. To analyze this structure using analytical approach, the I-V expressions of single channel described in section 3.2 are used to derive the common node voltage expressions. With the two equivalent single gates, it is assumed all the physical and structure parameters are same except the gate length and threshold voltage. In a real device, the status of the surface of the recessed region is complicate and usually depleted due to interface states. To simplify the analytical approach, such a surface, where the surface potential should be changed accordingly, is not taken into account in this study and the potential at free InAlAs surface is assumed to be floating without surface states effects. Furthermore, for simplification purposes, we assume:

- In linear operation region, non linearity is weak.
- When one of the gate is in saturation, the excessive voltage above saturation is dropped in that gate.
- In case both gate are in saturation region, the potential drop of V_{gs} under each gate is similar.

Following the formal derivation for the V_{ds1} under different operation regions. We may express the V_{ds1} as function of external bias conditions. However, unlike the conventional single gate case, the expressions are more complicate and need much effort to derive due to the added external variable. Moreover, instead of conventional two operating regions, the dual gate FET has four possible combinations of operation regions: (1) both gates in linear region; (2) gate 1 (near source) in linear but gate 2 in saturation;

(3) gate 1 in saturation whereas gate 2 in linear; (4) both gates in saturation region. By equating the terminal characteristics of the two single gate as shown in Fig. 3.3 and solving for the common gate potential V_{ds1} at the four possible combinations of operating status, and by appropriate logical reasoning, we finally have figured out the V_{ds1} expressions under all possible external bias conditions, that are list below:

Case 1: $$(V_{gs1}-V_{t1}) \le (1-K_1)(V_{gs2}-V_{t2}) \tag{3.13}$$

Condition 1.1:

When

$$V_{ds} \le \frac{(K_1+K_2-K_1K_2)}{(1-K_1)}(V_{gs1}-V_{t1}), \tag{3.14}$$

both channels are operating in linear region, and

$$V_{ds1} = \frac{K_1}{(K_1+K_2-K_1K_2)} V_{ds} \tag{3.15}$$

Here, K_1 and K_2 are defined as

$$K_1 = \frac{G_0(R_{s1}+R_{d1})}{1+(R_{s1}+R_{d1}+R_{s2})G_0} \tag{3.16}$$

$$K_2 = \frac{G_0(R_{s2}+R_{d2})}{1+R_{s1}G_0} \tag{3.17}$$

Condition 1.2:

When

$$\frac{(K_1+K_2-K_1K_2)}{(1-K_1)}(V_{gs1}-V_{t1}) \le V_{ds} \le (V_{gs2}-V_{t2}) - (1-K_2)(V_{gs1}-V_{t1}) \tag{3.18}$$

the second channel operates in linear region, but the first channel works in saturation region, and

$$V_{ds1} = V_{ds} - K_2(V_{gs1}-V_{t1}) \tag{3.19}$$

Condition 1.3:

When

$$V_{ds} \geq (V_{gs2} - V_{t2}) - (1 - K_2)(V_{gs1} - V_{t1}) \tag{3.20}$$

both channels are placed in saturation region, and

$$V_{ds1} = (V_{gs2} - V_{t2}) - (V_{gs1} - V_{t1}) \tag{3.21}$$

Case 2: $$(V_{gs1} - V_{t1}) \geq (1 - K_1)(V_{gs2} - V_{t2}) \tag{3.22}$$

Condition 2.1:

When

$$V_{ds} \leq (K_1 + K_2 - K_1 K_2)(V_{gs2} - V_{t2}) \tag{3.23}$$

again both channels work in linear region, and we have

$$V_{ds1} = \frac{K_1}{(K_1 + K_2 - K_1 K_2)} V_{ds} \tag{3.24}$$

Condition 2.2:

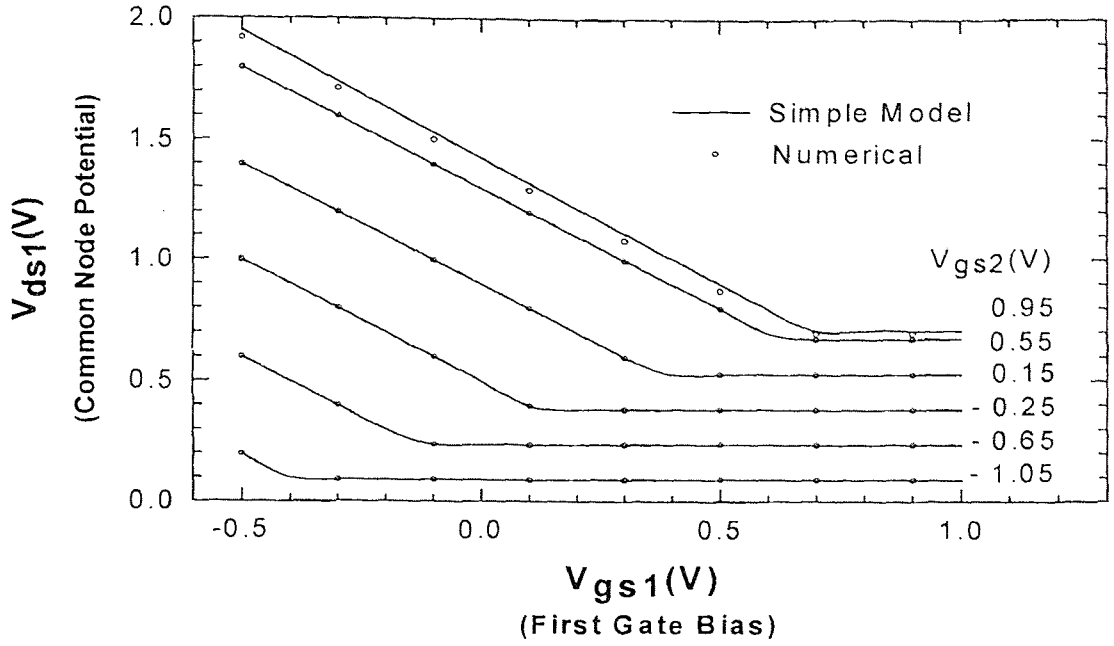
When

$$V_{ds} \geq (K_1 + K_2 - K_1 K_2)(V_{gs2} - V_{t2}) \tag{3.25}$$

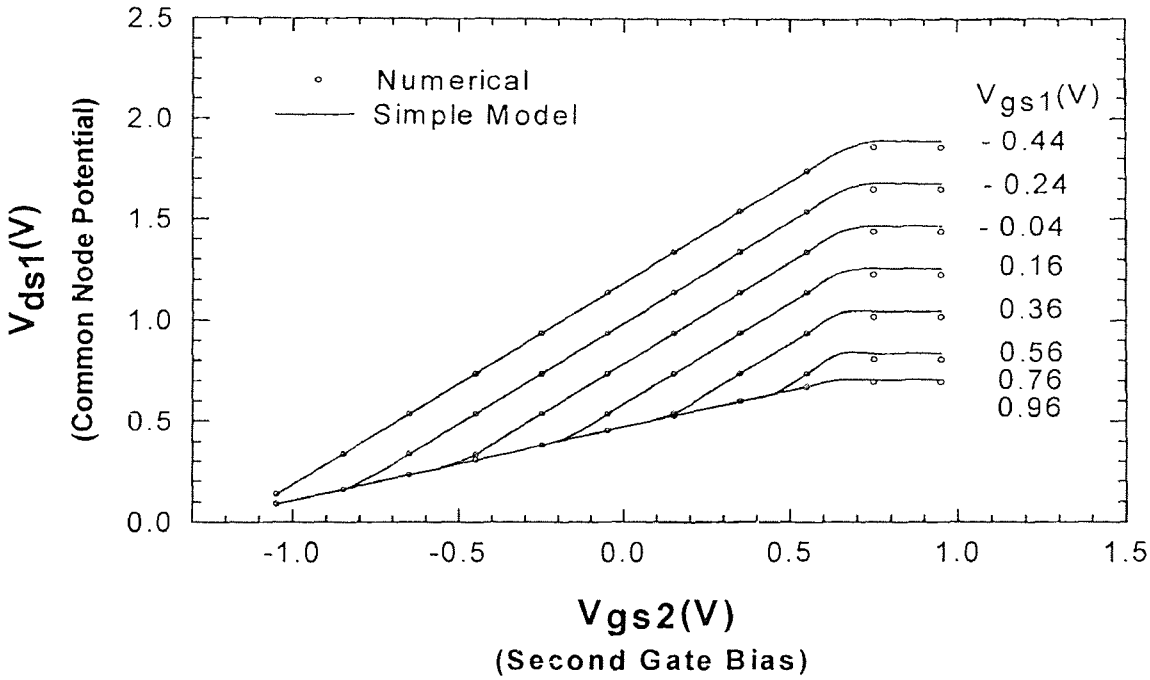
the first channel is placed in linear region, but the second channel is operated in saturation region, and thus we have

$$V_{ds1} = K_1 (V_{gs2} - V_{t2}) \tag{3.26}$$

As shown in the above expressions, the dual gate bias conditions can be divided into two special cases, that are $(V_{gs1} - V_{t1}) \leq (1 - K_1)(V_{gs2} - V_{t2})$ and $(V_{gs1} - V_{t1}) \geq (1 - K_1)(V_{gs2} - V_{t2})$. If the drain voltage increases, in both cases the channel current goes saturation from linear region and within these there exist all the four possible combination of bias regimes for dual gate FETs.



(a)



(b)

Fig. 3.5 The dependence of DGFET V_{ds1} upon V_{gs1} (a) and V_{gs2} (b) for several values of V_{gs2} and V_{gs1}, respectively, at V_{ds}=2V using the simple model presented here and the plots generated by exact semi-numerical method.

The resulting system of equations, (13)-(26), gives a set of closed form equations in the bias variables of $\{V_{ds}, V_{gs1}, V_{gs2}\}$. From these common node voltage expressions, one can easily determine the bias at internal node and thus the operational regimes under each gate. In Fig.3.5(a) and (b), we compare the V_{ds1} characteristics generated by using equations (13)-(26) with the plots obtained by semi-numerical method. The values of the parameters used in these calculations are shown in Table 3.1. The values of parameters used in both calculations are the same. The semi-numerical method uses single gate equations described in section 3.2 and solves for the intersection point under each bias condition using numerical method. Our simple model is in good agreement with the more complicated numerical results. Therefore, this simple analytic model allows the static and dynamic characteristics of dual gate HFET to be deduced with much reduced efforts. By using our model, it is possible improve our knowledge of device behavior, to calculate the elements of equivalent circuits and to optimize device performances with greatly improved effectiveness.

Table 3.1
Assumed and calculated structure and physical parameters
for each gate of the dual gate HFETs

L = 0.2 μm	W = 25 μm	d_i = 220 Å
d = 300 Å	$v_s = 1.2 \times 10^7 cm^2/s$	$\mu_0 = 4500\ cm^2/V \cdot s$
V_{to} = - 0.54 V	R_s = 15 Ω	R_d = 25 Ω
$N_s = 6 \times 10^{12} cm^{-2}$	$\varepsilon_2 = 12.1\ \varepsilon_o$	

3.3.2 Discussions

With the aid of the above common node voltage expressions, the mechanism of the operation of DGHFET can be described as follows. For the first case, where $(V_{gs1}-V_{t1}) \le (1-K_1)(V_{gs2}-V_{t2})$, low drain bias voltages drive both channels, referred to as M_1 and M_2, into linear region. The drain bias is then distributed between two linear resistors, and the common node voltage is thus mainly proportional to the drain bias. As the drain bias V_{ds} increases, the first channel M_1 turns saturated first and the first channel absorbs most of the drain bias. Therefore, the common node voltage and thus the device operation are also well controlled by the first gate bias. As M_1 saturates, the drain voltage of M_1 (or common node voltage) reaches a maximum value, and further increases in drain voltage V_{ds} will not change the voltage bias across the M_1. In other words, the first channel is screened from drain voltage variations. This eventually saturates the second channel M_2, with the common node voltage adjusting itself to allow both channels in saturation. It should be noted here that this is the only situation in which the two channels can both be biased into saturation region.

For the second case, where $(V_{gs1}-V_{t1}) \ge (1-K_1)(V_{gs2}-V_{t2})$, the low drain bias voltages again keep both M_1 and M_2 in linear region. The subsequent increase in V_{ds}, however, can only saturate M_2. Therefore, there is no way in this case to bias both channels into saturation simultaneously to produce two high field regions along the two channels. This is because in this situation the resulting current flow through M_1 is insufficient to cause a voltage drop across it large enough to induce pinch off. This behaves like a single gate with a channel resistance in series with its source, which degrades total transconductance. The corresponding common node voltage is thus

effectively controlled by the channel current or the bias of the second gate, whereas the first gate functions like a passive device.

3.4 Dual Gate I-V Characteristics

With the aid of the common node equations, (3.13)-(3.26), one can calculate dual gate I-V characteristics via single gate method. In Khondker's single gate method, the evaluation of D2(z) clearly does not require any numerical technique. However, one has to calculate the I-V characteristics via numerical techniques. The following method can be used instead of the numerical procedure at the expense of only a few percent loss of accuracy. Khondker suggested an empirical function which approximates the relationship between D2(z) and z:

$$D_2(z) \approx \left(\frac{1-z}{z}\right)^{3/2} \tag{3.27}$$

This equation slightly underestimates the velocity of electrons for $E \le E_c$. However, this approximation can be used to achieve a much better computational simplicity. Therefore, the following method can be used to calculate dual gate theoretical I-V curves instead of any numerical procedure. Rewriting (3.4) using (3.27), we have

$$V_{gs1} = V_{t1} + I_{csat} R_{s1} + \left[1 + \left(\frac{v_s L G_0}{\mu_0 I_{csat}}\right)^{2/3}\right] \frac{I_{csat}}{G_0} \tag{3.28}$$

for the first channel. Thus, for a given value of V_{gs1}, one can calculate the critical saturation current I_{csat} for the first gate. The magnitude of the common node voltage for a given value of channel current is given by

$$V_{ds1}=(V_{gs1}-V_{t1})+I_c R_d-[1+((\frac{1-t_0}{t_0})^{3/2}-\frac{v_s L G_0}{\mu_0 I_c})^{2/3}]\frac{I_c}{G_0} \qquad (3.29)$$

where $0 < I_c < I_{csat}$. Note that $I_c = I_{csat}$ when $t_L = 1$. For $I_c > I_{csat}$, (3.12) can be rewritten as

$$V_{ds1}=(V_{gs1}-V_{t1})-I_c(1/G_0-R_d)+\frac{2d E_0}{\pi}\sinh(\frac{\pi}{2d}[L-\frac{I_c}{G_0 E_0}(\frac{1-t_0}{t_0})^{3/2}]) \qquad (3.30)$$

The theoretical dual gate I-V curves can be calculated in the following manner. For a given set of values for $\{V_{gs1}, V_{ds}\}$ or $\{V_{gs1}, V_{gs2}\}$, one can first compute the value of I_{csat}. And for a given drain current, less than and greater than I_{csat}, the common node voltage V_{ds1} is then calculated using (3.29) and (3.30), respectively. Finally, using equations (3.13)-(3.26), either the gate two voltage V_{gs2} or the drain bias V_{ds} can be determined. The theoretical DG-HFET I-V curves calculated using (3.13)-(3.30) are compared with our experimental results. In Fig. 3.6, we present the calculated I-V characteristics at V_{gs2} biased at zero volt. For comparison, experimental I-V curves is also presented in the figure for a dual gate HFET with same structure parameters as the simulated device described in Fig. 3.4 and Table 3.1. Our theoretical plots are in good agreement with the experimental data. We mention here that the approximate equations overestimate the current in the transition to saturation and less well predict the current in the saturation region. This could arise due to the surface potential caused by surface states in the recessed region and extention of the drift region at gate edge[59],[60],[61],[62],[63], which we have not incorporated in the derivation of the simplified analytic equations.

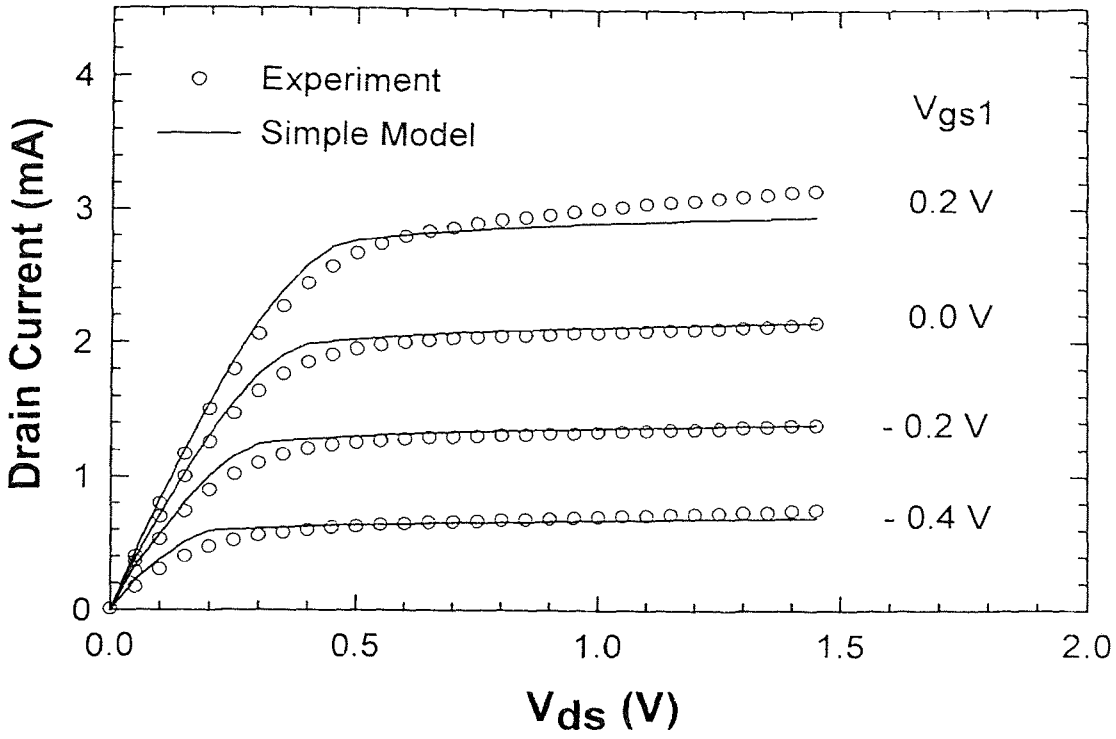


Fig. 3.6 DGHFET I-V characteristics of the first gate at $V_{gs2} = 0$V for a 0.2μm dual gate HFET. The solid lines are calculated results and circled markers are our experimental data.

3.5 Summary

In this chapter, we have presented an analytic common node potential model to provide the methodology of calculation of dual gate I-V characteristics. In the next Chapter, we will derive analytic expressions of device small signal parameters and make use of the methodology outlined in this chapter to calculate and investigate the small signal characteristics and dual gate effects.

We summarize here the dual gate I-V calculation methodology presented in this Chapter. Starting with device structural and physical parameters, the common node potential is calculated over the external bias ranges required according to equations given

in (3.13)-(3.26). For a given values of V_{gs1} the I_{csat} value is first calculated using equation (3.28). And for a given set of values for $\{V_{gs1}, V_{ds}\}$ or $\{V_{gs1}, V_{gs2}\}$, if drain current is less than I_{csat}, as in linear region, then the common node voltage V_{ds1} is given by equation (3.29), otherwise, as in the saturation region, the V_{ds1} is given by equation (3.30). Finally, using the calculated results from equations (3.13)-(3.26), either the gate two voltage V_{gs2} or the drain bias V_{ds} is determined.

It should be noted that the calculation methodology for dual gate HFET I-V characteristics presented in this chapter is for normal dual gate structure with gate to gate separation larger than the channel depth, which validates our analytical calculation.

CHAPTER 4

ANALYTICAL DUAL GATE HFET SMALL SIGNAL CHARACTERISTICS

4.1 Introduction

The design, process and characterization of DG-HFET with high performance dual gate HFET has gained considerable interest in recent years, particularly for RF application such as Mixers[64] and high efficiency power amplifiers[65]. To address the issue of device small signal characteristics, several dual gate key small signal parameters are being explored that would help achieve improved device performance and obtain better insight into device physics. These parameters include transconductance, drain conductance, gate-source capacitance and gate drain capacitance that dominate device behavior. Proper understanding of those device parameters requires correct prediction of how external biases affect the parameters, particularly since small changes in some biases can significantly alter those parameters. It is recognized that the characteristics of a dual gate HFET, and hence the behavior of small signal parameters, are different and much more complicated than its single gate counterpart. However, what has been lacking is analytical characterization and first order analytic modeling of dual gate small signal parameters.

In light of the above concerns, we present in this chapter a first order analytic calculations of dual gate HFET small signal parameters. The objectives are two fold: (1) to formulate closed form models for dual gate HFET small signal parameters that can be readily implemented analytically, and (2) to develop an analytic physics-based model which is an essential requirement for predictive device design and development.

The organization of this chapter is as follows. Section 4.2 is devoted to the single gate small signal parameters equations. An important aspect of analytic dual gate small signal modeling is the formulation of the corresponding single gate parameters in various operating regimes. Once the single gate parameters have been formulated, we then employ the methodology developed in the previous chapter to calculate respective parameters for dual gate HFET.

In section 4.3, we discuss the equivalent circuit approach and identify the key dual gate small signal parameters. Two possible dual gate configurations are investigated analytically.

In section 4.4, we demonstrate the dual gate small signal characteristics by comparing them with single gate results. The unique behavior of dual gate HFET are shown to be explainable through our simple analytic models. In direct support of in-depth understanding of dual gate effects on device performance, Section 4.4.1 through 4.4.4 are devoted to the four key parameters, transconductance, drain conductance, gate-source capacitance and gate drain capacitance, respectively. Moreover, in section 4.5, we discuss the results presented in section 4.4 and therefore the dual gate effects. Moreover, we give practical information on exploiting dual gate effects to the full potential. Finally in section 4.6, we summarize the work described in this chapter and the major conclusions.

4.2 Single Gate Small Signal Parameters

Small signal parameters are obtained analytically with the help of DC expressions presented in Chap. 3. Since we shall only be concerned with modeling the major parameters, four key parameters that affect intrinsic device performance are explored here.

4.2.1 The Transconductance and the Drain Conductance

Neglecting the non-intrinsic effects or in other words treating the device as a ideal intrinsic device, the tranconductance of the device in the linear (g_{ml}) and the saturation regions (g_{ms}) can be readily obtained by differentiating the corresponding linear and saturation current equations derived in section 3.2 with respect to V_{gs}, respectively. This approach yields the intrinsic transconductance,

$$g_{ml} = \frac{(\frac{\sqrt{1-t_o^2}\,t_l}{t_o} - \sqrt{1-t_l^2})\,I_c}{\frac{\sqrt{1-t_o^2}\,t_l(V_{gs}-V_{to})}{t_o} - \sqrt{1-t_l^2}(V_{gs}-V_{to}-V_{ds}) - \frac{v_s t_l L}{\mu}} \tag{4.1}$$

and

$$g_{ms} = \frac{I_c}{(V_{gs}-V_{to}) - \frac{I_c D_2(t_o)\,t_o}{G_o\sqrt{1-t_o^2}}} \tag{4.2}$$

where the symbols are specified in section 3.2 of Chapter 3.

Using the definition of drain conductance, that is, differentiating the corresponding current equations as given in section 3.2 with respect to V_{ds} in the linear and saturation regions, respectively, we obtain analytic drain conductance expressions for g_{dl} and g_{ds} as shown below:

$$g_{dl} = \frac{\sqrt{1-t_l^2}\,I_c}{t_l(\frac{\sqrt{1-t_l^2}(V_{gs}-V_{to}-V_{ds})}{t_l} - \frac{\sqrt{1-t_o^2}(V_{gs}-V_{to})}{t_o} - \frac{v_s L}{\mu_n})} \tag{4.3}$$

and

$$g_{ds} = G_o / (R_d G_o - 1 + 7(\frac{3}{2}\frac{(V_{gs} - V_{to}) G_o (1-t_o)^{1/2}}{I_c t_o^{1/2}} +$$

$$-\frac{(1-t_o)^{1/2}}{t_o^{1/2}}) \cosh(\frac{\pi(L - \frac{I_c \mu_n (1-t_o)^{1/2}}{v_s G_o t_o^{1/2}})}{2d})) \quad (4.4)$$

4.2.2 The Gate Capacitance and Drain to Gate Feedback Capacitance

For the calculation of the gate capacitance, the integrated stored charge in the 2-DEG channel is approximated and differentiated with respect to V_{gs}, and the resulting capacitance in the linear (C_{gsl}) and saturation regions (C_{gss}) can be written as,

$$C_{gsl} = g_{ml}(\frac{2L(D_3(t_o) - D_3(t_l))}{v_s(D_2(t_o) - D_2(t_l))} + \frac{\mu_n}{v_s^2}(\frac{(V_{gs} - V_{to} - V_{ds})\sqrt{1-t_l^2}}{t_l^2}$$

$$+\frac{I_c\sqrt{1-t_l^2}}{g_{ml} t_l^2} - \frac{(V_{gs} - V_{to})\sqrt{1-t_o^2}}{t_o^2} + \frac{I_c\sqrt{1-t_o^2}}{g_{ml} t_o^2})) \quad (4.5)$$

and

$$C_{gss} = \frac{g_{ms}\mu_n I_c D_2(t_o)(\frac{2D_3(t_o)}{D_2(t_o)} - \frac{1}{t_o})}{v_s^2 G_o} + \frac{g_{ms}}{v_s}(L - \frac{2\mu_n I_c D_2(t_o)}{v_s G_o})$$

$$+\frac{\mu_n\sqrt{1-t_o^2}(g_{ms}(V_{gs} - V_{to}) - I_c)}{v_s^2 t_o} \quad (4.6)$$

where

$$D_3(z) = \frac{(1-z^2)^{3/2}}{sz^3} \quad (4.7)$$

The drain to gate feedback capacitance arises primarily due to the gate to drain separation. For calculation of the drain to gate feedback capacitance, we calculate

channel charge with respect to V_{ds}, under the gate to source short circuit condition. Thus, we have in the linear (C_{dgl}) and saturation regions (C_{dgs}) that

$$C_{dgl} = g_{dl}\left(\frac{2L(D_3(t_o) - D_3(t_l))}{v_s(D_2(t_o) - D_2(t_l))} + \frac{\mu_n}{v_s^2}\left(\frac{(V_{gs} - V_{to} - V_{ds})\sqrt{1 - t_l^2}}{t_l^2}\right.\right.$$

$$\left.\left. + \frac{I_c\sqrt{1 - t_l^2}}{g_{dl}t_l^2} - \frac{(V_{gs} - V_{to})\sqrt{1 - t_o^2}}{t_o^2}\right)\right) \tag{4.8}$$

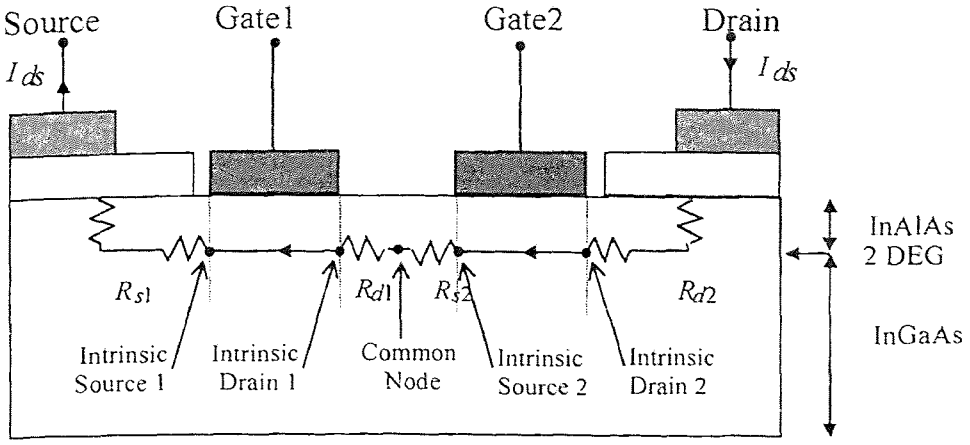
and

$$C_{dgs} = g_{ds}\left(\frac{\mu_n I_c D_3(t_o)}{v_s^2 G_o} + \frac{1}{v_s}\left(L - \frac{2\mu_n I_c D_2(t_o)}{v_s G_o}\right)\right.$$

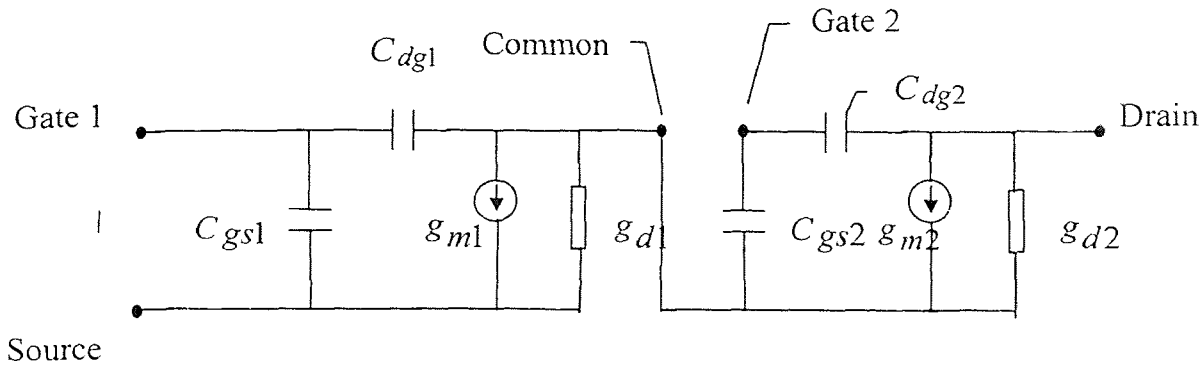
$$\left. + \frac{\mu_n\sqrt{1 - t_o^2}(V_{gs} - V_{to})}{v_s^2}\left(\frac{1}{t_o} - \frac{1}{t_o^2}\right)\right) \tag{4.9}$$

4.3 Dual Gate HFET Small Signal Equivalent Circuit

Fig. 4.1(a) illustrates the intrinsic HFET, the parasitic elements, and defines the simplification that will be used in the analysis. R_{s1}, R_{s2}, R_{d1} and R_{d2} are the parasitic resistances, assumed to be linear, which are included in our model equations as a first order approximation. This can be seem explicitly from the model parameters such as t_0 and t_l which are shown in equation (3.5) and (3.6), respectively. The fundamental performance of the intrinsic device can be understood in terms of the simplified small signal equivalent circuit shown in Fig.4.1(b). We focus on intrinsic device whereas the parasitic regions as shown in Fig. 4.1 (a) are modeled with linear resistance attached to the core intrinsic model.



(a)



(b)

Fig. 4.1. (a) Geometry of the dual gate HFET structure considered . The intrinsic HFETs and the parasitic resistance are shown. (b) Small signal equivalent circuit of Dual Gate HFET.

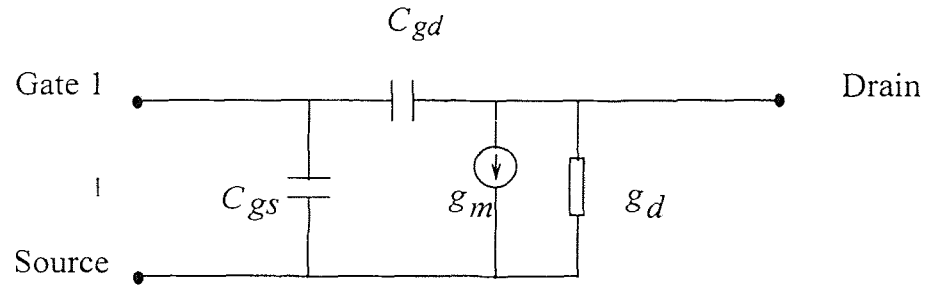


Fig. 4.2 Dual Gate HFET Equivalent Circuit with V_{gs2} Biased at Certain Value.

Therefore, we have neglected the parasitic-resistance blow-up effect at high drain current, which has been modeled by D. R. Greenberg and J. A. del Alamo [66]. This effect is of importance in HFETs optimized for high power and employing a sizeable gate-drain gap. We also ignore other performance-degrading effects, such as gate leakage current[67], parasitic MESFET formation[68], or electron real space transfer[67]. While these can be minimized by clever MBE structures[55] and optimized design.

Fig. 4.1(b) is based on the association of two intrinsic equivalent single gate FETs in cascade configuration. Since in most applications the input signal is applied to one of the two gates, the equivalent circuit can be simplified as shown in figure 4.2. The parameters in Fig. 4.2 can be expressed in terms of the parameters in Fig. 4.1(b) for two possible bias configurations as listed below:

(i) Fix the second gate potential V_{gs2} and use the first gate as the control gate.

$$g_m = g_{m1}\left(\frac{g_{d2}+g_{m2}}{g_{d1}+g_{d2}+g_{m2}}\right) \tag{4.10}$$

$$g_d = g_{d1}\left(\frac{g_{d2}}{g_{d1}+g_{d2}+g_{m2}}\right) \tag{4.11}$$

$$C_{gs} = C_{gs1} + C_{dg1}\left(\frac{g_{d1}+g_{d2}+g_{m1}+g_{m2}}{g_{d1}+g_{d2}+g_{m2}}\right) \tag{4.12}$$

$$C_{dg} = C_{dg1}\left(\frac{g_{d2}}{g_{d1}+g_{d2}+g_{m2}}\right) \tag{4.13}$$

(ii) Fix the first gate potential V_{gs1} and use the second gate as the control gate.

$$g_m = g_{m2}\left(\frac{g_{d1}}{g_{d1}+g_{d2}+g_{m2}}\right) \tag{4.14}$$

$$g_d = g_{d2}\left(\frac{g_{d1}}{g_{d1}+g_{d2}+g_{m2}}\right) \tag{4.15}$$

$$C_{gs} = C_{gs2} + C_{dg2}\left(\frac{g_{d1}+g_{d2}}{g_{d1}+g_{d2}+g_{m2}}\right) \tag{4.16}$$

$$C_{dg} = C_{dg2} + C_{gs2}\left(\frac{g_{d2}}{g_{d1}+g_{d2}+g_{m2}}\right) \tag{4.17}$$

From the above exertions, one can readily find that configurations (ii) has enhanced gate to drain feedback capacitance whereas in configurations (i) the feedback capacitance decreases significantly. Using the simple analytical method developed in last chapter and employing equations presented above, we calculate the transconductances behavior of the two configurations. The values of the parameters used in these calculations are the same as shown in Table 3.1 except for the values of parasitic resistances. We assume that $R_{s1} = 15\Omega$, $R_{s2} = 10\Omega$, $R_{d1} = 20\Omega$ and $R_{d2} = 25\Omega$. The corresponding results are plotted in Fig.4.3 and Fig. 4.4 which show the variation of the transconductance g_m with V_{gs1} and V_{gs2} respectively. Curves in two figures look similar in shape, but the maximum g_m values are significantly different. The first configuration demonstrates a much greater maximum transconductance than that of the second one. This is explainable, since in first configuration the second gate provides series drain resistance to the control gate which has minor influence on the transconductance, whereas in the second configuration the first device adds series source resistance to the active gate and it greatly reduces its transconductance. The above phenomenon is consistent with experimental observations [41]. This is the main reason why the first configuration in stead of the second one is preferred for applications.

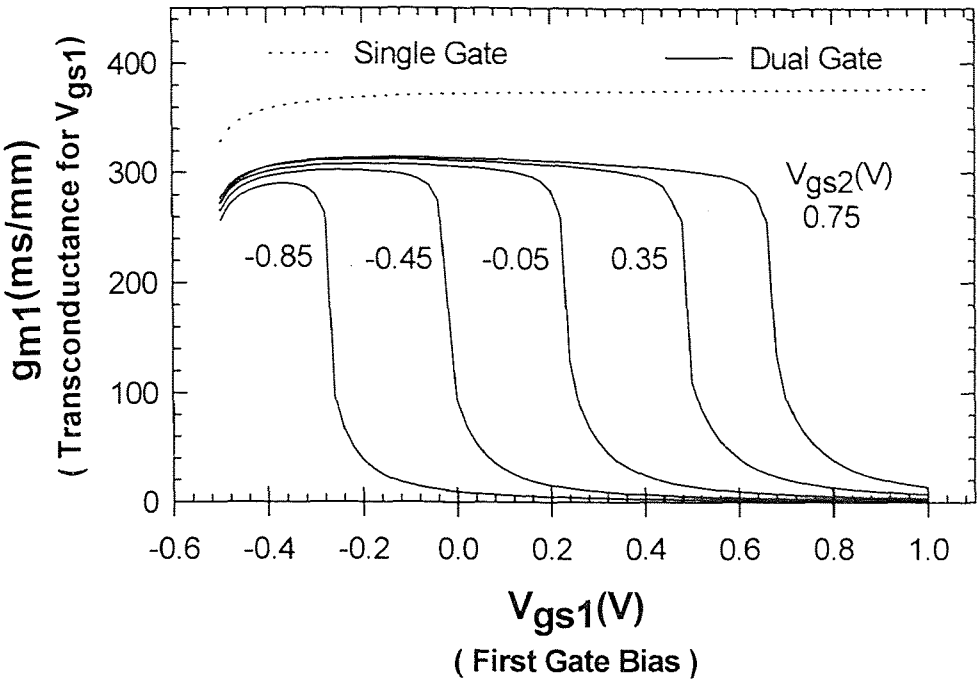


Fig. 4.3 Gate voltage dependence of the transconductance for the first equivalent gate with several V_{gs2} bias at V_{ds} =1.5 V. The dotted line represents single gate results.

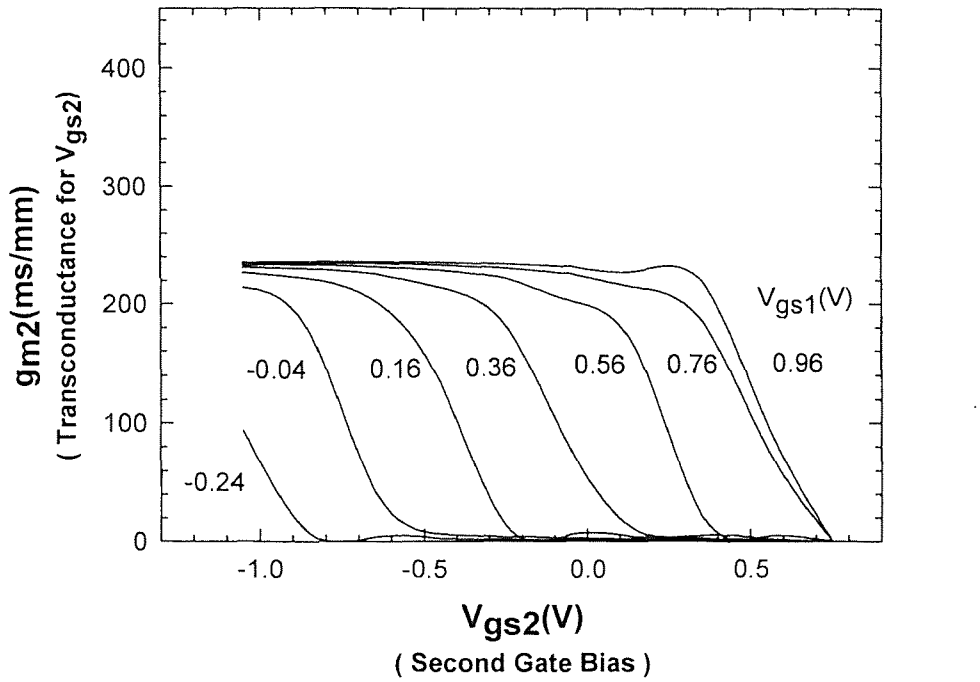


Fig. 4.4 Gate voltage dependence of the transconductance for the second equivalent gate at V_{ds} = 1.5 V, with several V_{gs1} bias.

According to the obvious advantages of the first arrangement, details of the small signal model described below will be limited in this configuration.

4.4 Dual Gate Small Signal Parameters in the Current Saturation Region

The four parameters that dominate device performance are transconductance, drain conductance, gate to source capacitance and gate to drain capacitance. Since none of previous works provide detailed pictures for current saturation operation, our objective in performing dual gate calculation of key parameters is to arrive at the understanding of all the four parameters. The device parameters used in the calculation below are same as those used for Fig.4.3 and Fig. 4.4, which are list in Table 3.1 except the parasitic resistances as illustrated in Fig. 4.1(a). We assume that $R_{s1} = 15\Omega$, $R_{s2} = 10\Omega$, $R_{d1} = 20\Omega$ and $R_{d2} = 25\Omega$. The drain bias is fixed at 1.5 V to ensure the saturation of drain current.

4.4.1 The Transconductance

By using the analytical equations described above, the small signal equivalent transconductances can be readily calculated. As shown in Fig. 4.3, which depicts the behavior of intrinsic HFETs, the magnitude of single gate g_m sharply increases with the gate voltage near the threshold and attains a nearly steady value at higher gate voltages. This two regime behaviors have been explored in detail elsewhere[69], establishing mobility-limited transport in the regime of g_m rise and velocity-saturation limited transport in the plateau regime. In this study, we neglect the some effects like nonlinear charge control and the mobility dependence on the gate bias. In practical HFETs, g_m

rises linearly at low gate voltages, reaching its peak value and then decreases with the increase of gate voltage. The peak value of g_m observed in practical devices coincides with the near steady value calculated analytically. As can be seen from Fig. 4.3, the envelope of the g_m curves corresponds to the g_m versus V_{gs1} curve of single gate HFET. g_m of the dual gate HFET which is always lower than that of its single gate counterpart increases as the bias of the second gate becomes more positive. This effect can be understood via our common node potential model. With the increase of the first gate bias V_{gs1} so that the condition $(V_{gs1} - V_{t1}) \geq (1 - K_1)(V_{gs2} - V_{t2})$ holds, the first gate (of the active device) is driven into linear regime no matter what V_{ds} is, and the equivalent transconductance drops sharply to linear regime value which is nearly zero.

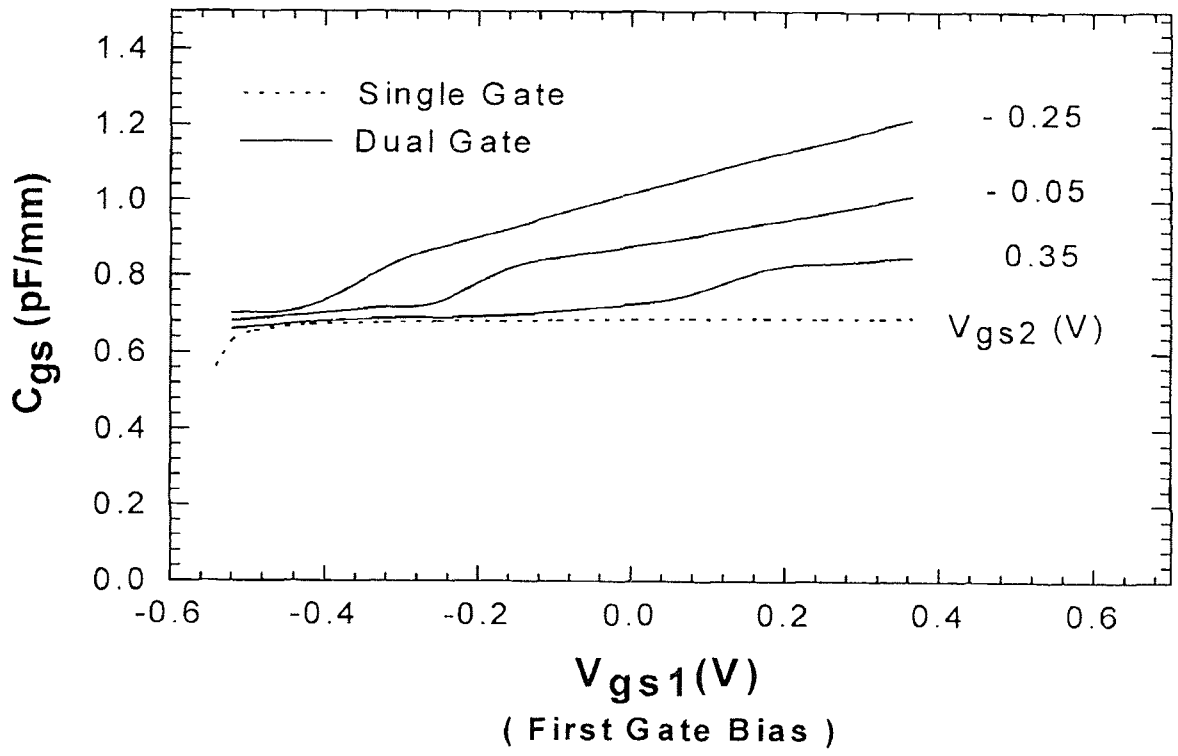


Fig. 4.5 Gate voltage dependence of the C_{gs} for several values of V_{gs2} and SGFET.

4.4.2. The Gate Capacitance

The integrated stored charge Q_{ch} in the 2-DEG channel is approximated and differentiated with respect to V_{gs1}. The corresponding analytical equations are calculated and results are depicted in Fig. 4.5. For the single gate device, its C_{gs}-V_{gs} curve looks like its corresponding g_m-V_{gs} curve with a sharp increase at the threshold voltage. For the dual gate case, the gate capacitance monolithically increases with the first gate bias, while decreases with the second gate potential. These observations, which clearly result from the change of operating regimes under the two gates, demonstrate that the gate capacitance is highly related to the bias of the two gates. Under the bias condition of $(V_{gs1} - V_{t1}) \geq (1 - K_1)(V_{gs2} - V_{t2})$, the first gate is always kept in linear regime. Due to very large gate capacitance in the linear regime, this results in higher gate capacitance at higher V_{gs1} and lower V_{gs2}.

4.4.3. The Output Conductance

Calculations of the equations of output conductance have yielded rather small values when compared to those experimentally found for practical devices with the comparable dimensions[70]. This is could partly due to the variation of spreading of Δ d, the 2-DEG moment distance, on the electric field. It has been suggested that for practical devices higher output conductance arises due to the de-confinement caused by the channel high electric field [71]. In other words, due to the high electric field in the carrier velocity saturation region of the channel, some carriers are injected into the buffer layer causing an additional drain current. In presence of deep level traps in the buffer layer, the drain current usually shows the so called "kink effect" due to the field ionization of traps.

However, at microwave frequencies the output conductance in the current saturation region has been found to be lower than its value predicted by the corresponding slope of the I-V characteristics in presence of the "kink effect"[72]. With or without the "kink effect" the output conductance in practical HFETs are found to be much higher than that can be predicted analytically. However, no analytical model has yet been proposed to incorporate these effects. Here we propose an alternate approach, first determine the single gate g_d at saturation regime using comparable experimental data, and then calculate the dual gate g_d characteristics using derived equations.

As depicted in Fig. 4.6, all g_d curves for the dual gate case are lower than that for the single gate case. In other words, the short channel effect has been greatly reduced by the use of dual gate configuration. This arises from the screen mechanism, or the modification of the resistivity distribution along the two channels by the second gate. In the case we consider here, the saturation condition for the second gate is kept true. Therefore, the second gate absorbs considerable part of drain bias and the influence of drain voltage on the resistance under the first gate is thus weakened. As the second gate becomes more saturated, the field distribution along the two channels is such that a very small increase in the drain current requires a large increase in the drain voltage. This means that the drain current practically saturates and the output conductance becomes smaller. This feature makes it possible to use dual gate FET to overcome the short channel effects.

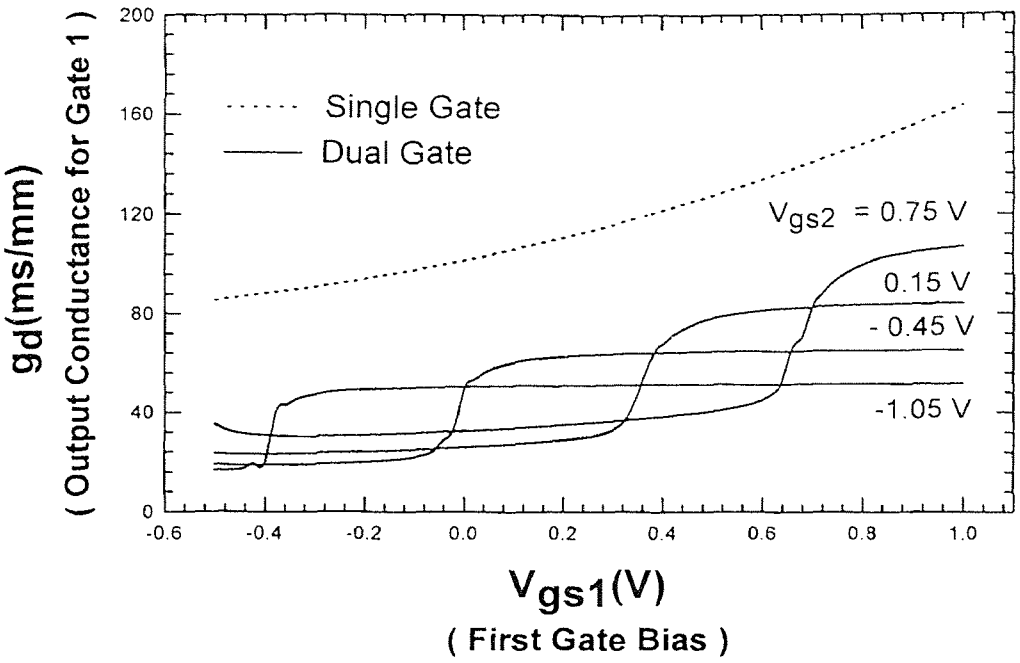


Fig. 4.6. Variations with V_{gs1} of the output conductance for the first gate of DGFET.

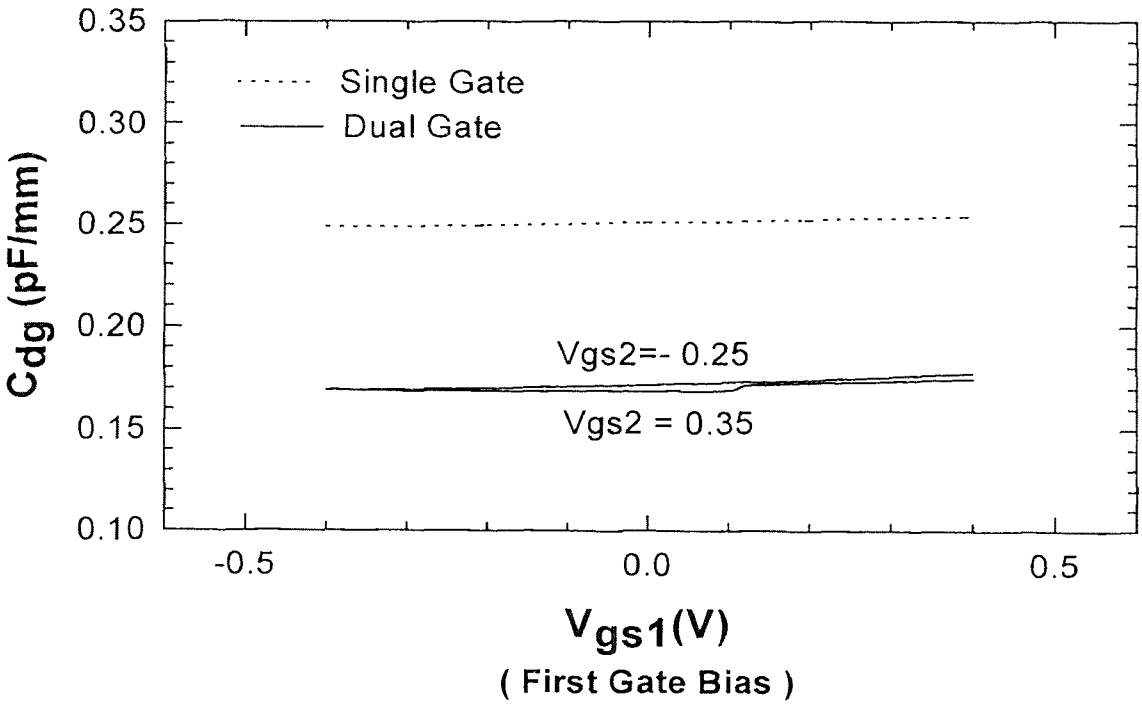


Fig. 4.7 Variations with V_{gs1} of the feedback capacitance with V_{gs2} biased at -0.25V and -0.35V. The dotted line represents single gate.

4.4.4 The Feed Back Capacitance

A clear advantage of the dual gate is observed in its influence on feed back capacitance C_{dg}. In Fig. 4.7, the feedback capacitance is significantly reduced for the dual gate case in comparison to the single gate device. This reflects the screen effect of the second gate. Even though the C_{dg1} can be large in these circumstances, a large variation in V_{ds} can only produce very small percentage change in V_{dg1}, the first gate drain bias, and thus result in small perturbation in Q_{dg}. Which leads to much decreased C_{dg} for the dual gate device.

4.5 Results and Discussions

In the previous few sections we have presented a simplified analytical model that describes the dc and small-signal characteristics of DG-HFETs. In the course of illustrating the bias dependence of the I-V and key small signal parameters, we have explained the dual gate characteristics and its comparison with that of the single gate. Our model based results have demonstrated that the dual gate configuration has dramatically improved the output conductance and feedback capacitance behavior at the expense of a relatively small decrease in transconductance and some increase in gate capacitance in contrast to its single gate counterparts. This leads to much enhanced g_m / g_d and C_{gs} / C_{dg} ratios for DG-HFET which are two key factors that determine the RF maximum power gain.

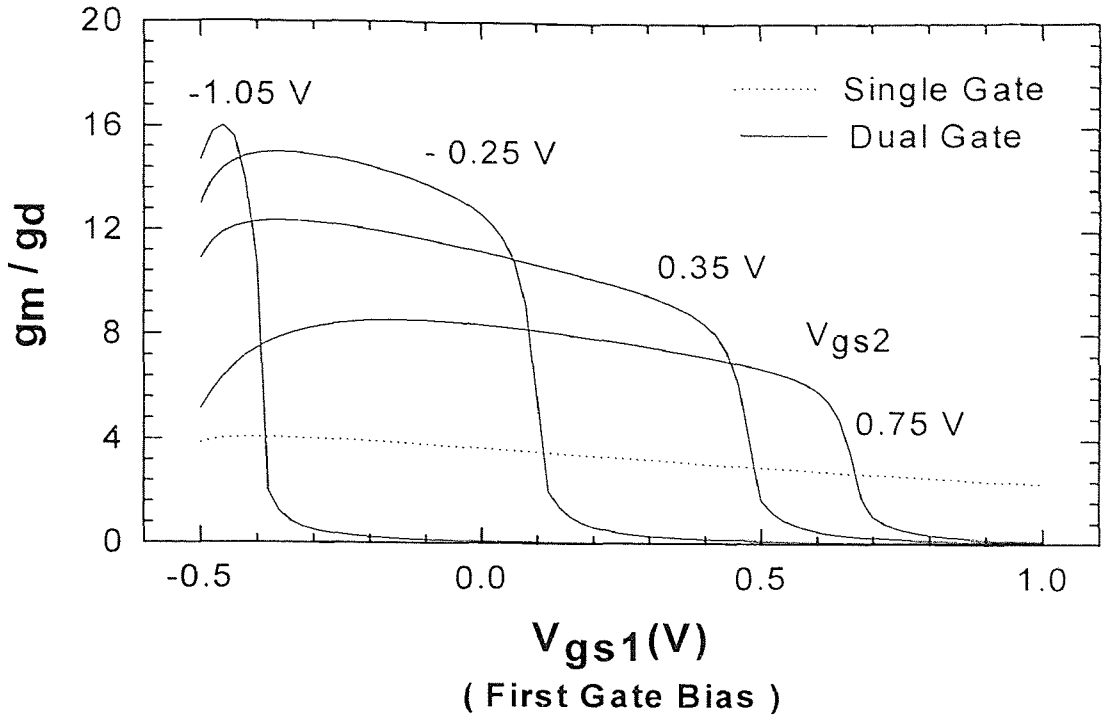


Fig. 4.8 g_m / g_d ratio as a function of control gate voltage V_{gs1} at V_{ds}=2V in DGFET(solid curves) and SGFET(dotted curve).

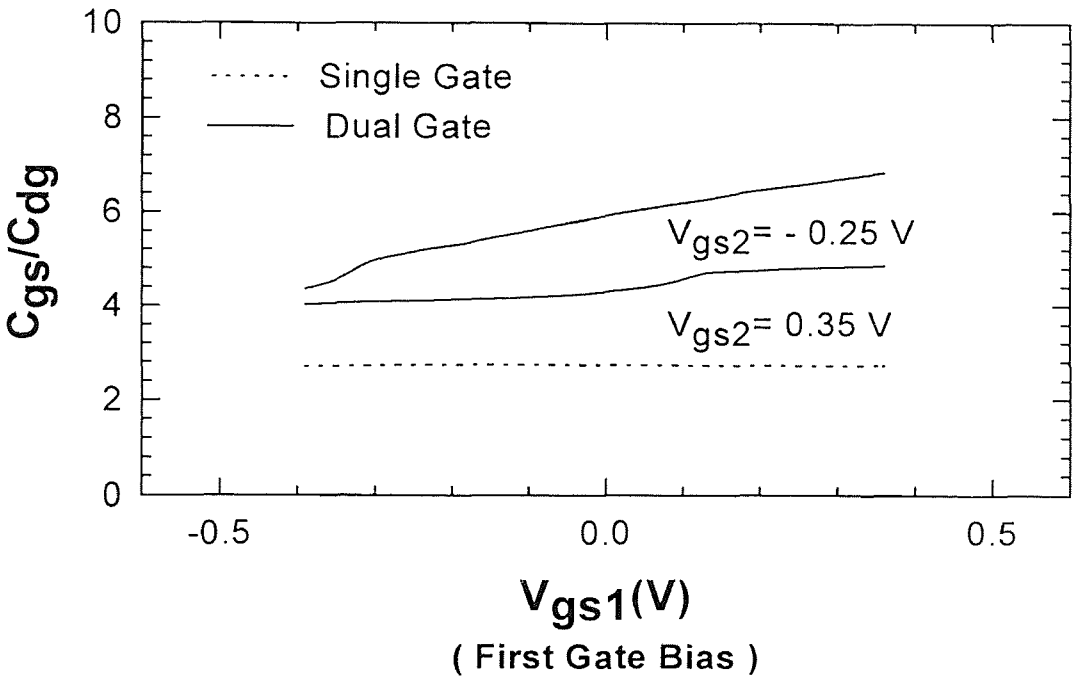


Fig. 4.9. C_{gs} / C_{dg} ratio as a function of control gate voltage V_{gs1} at V_{ds}=2V in DGFET(solid curves) and SGFET(dotted curve)

The data of the dependence of g_m / g_d and C_{gs} / C_{dg} on the gate bias voltage are presented in Fig. 4.8 and Fig. 4.9, respectively. They provide a clear picture as to why the external bias so profoundly affects the device performance. Since the parameter g_m / g_d has an maximum value and C_{gs} / C_{dg} increases with V_{gs1} but decreases with V_{gs2}, one would expect the best performance occurs for an optimum set of device bias voltages.

We can learn from our model based results presented in Fig. 4.3 to Fig. 4.9 that, in order to take the best advantage of dual gate devices, its two gates must be biased into saturation regime simultaneously (or double saturation). To realize this, according to our common node potential model, the following bias condition $(V_{gs1} - V_{t1}) \leq (1 - K_1)(V_{gs2} - V_{t2})$ and $V_{ds} \geq (V_{gs2} - V_{t2}) - (1 - K_2)(V_{gs1} - V_{t1})$ must be held true. Actually we find that these two conditions somehow conflict with each other. The maximum V_{gs2} applicable is clamped by V_{ds}, whereas the maximum V_{gs1} is determined by V_{gs2}. Hence, we need to select Vds large enough to provide required bias margin for V_{gs2}. After that we can choose V_{gs2} using the above two conditions for a required V_{gs1} value.

Our analytical model points out several aspects of the selection of device parameters to realize the double saturation conditions.

- Once V_{ds} condition or equation (3.13) is satisfied, smaller V_{t2} or larger V_{t1} are required to widen V_{gs2} and V_{gs1} bias margins.
- Since K1 and K2 are dominated by parasitic resistances, reducing these resistances will make the double saturation requirements easier to be satisfied.

- Gate lengths of the two gates have minor influence on the bias condition required.
- In double saturation, the drain bias of the first gate follow the variations of $V_{gs2} - V_{gs1}$. It is not a function of the total drain bias.

Furthermore, some hints to improve dual gate HFET performance or take full advantage of the dual gate configuration can be derived with our simple common node potential model. They include:

- Make the threshold voltage of the first gate more positive than that of the second, or, make the threshold voltage of the second gate more negative than that of the first..
- Minimize parasitic resistances.
- Increase breakdown voltage so that the device can work at higher drain voltages.
- Use V_{gs2} as high as possible, whereas use V_{gs1} as small as it can be.

4.6 Summary

In this chapter we provide closed form equations for the key current, transconductance/conductance and capacitance parameters as functions of the two gate and drain bias voltages. It is believed that the analytical results presented in this chapter, concerning the small signal characteristics of dual gate HFET, and the optimization of external bias voltages and device structural and physical parameters will provide the basis for effective experimental approaches on the improvement of dual gate HFETs and

construction of new device taking advantage of the dual gate effects. It should be noted that, even though our model is for HFET, similar results can be deduced for other dual gate FETs.

CHAPTER 5

A NEW DEVICE STRUCTURE: DUAL MATERIAL GATE HFET

5.1 Introduction

Considering the structure of more general dual gate HFETs than those we have studied in the previous chapters, at least three different device structures in which the device are expected to exhibit different behavior have been identified. They are two gates in cascade, split gate, and two gates in contact. For two gates in cascade which we discussed before, the separation is only important when considering the parasitic resistance between the gates. For a split gate with a separation gap so small that it is less than that channel thickness, the gate separation is especially important in determination of the device behavior. Moreover, the device performance is limited by how close the two gates can be made. The two gates in contact is the ultimate limit of the split gate approach. However, in that ultimate case we can not bias two gates independently as in cases of split or dual gate HFETs.

There are two kinds of effects when two gates are placed close together: screening effect and velocity enhancement effect. Screening effect is the effect that the second gate, which is near drain, absorbs most of the excessive drain bias when both gates are in saturation region, making the first gate or control gate insensitive to the drain bias in the saturation region and therefore ensuring low drain conductance for the first gate. This effect occurs for all the two gate structure as long as the two gates can be controlled differently. In contrast, velocity enhancement effect is valid only in case the two gates are extremely close, since it is based on the fact that electrons continuously accelerate

without cooling down during travel through the inter-gate region, and enter the second gate with high speed. The average electron velocity increases due to its higher value at the second gate.

In the case of two extremely close gates or the case of a split gate, the relationship between the two gates has changed in contrast to the case of two widely separated gates. In a split gate, the separation of gates is sufficiently small that the electron almost loses no energy when passing through the region between the gates. Thus, in the split gate case, the average electron velocity increases significantly and gate transconductance improves appropriately as the gate separation decreases. However, as the separation decreases, the parasitic fringing capacitance between the two gates also increases. The resulting device has a much higher parasitic capacitance, which degrades its high speed performance. In the discussion that follows, we shall be concerned exclusively with aspects of avoiding gate to gate capacitance but taking the full advantage of screen and velocity enhancement effects of dual and split gate FETs by introducing new device structures.

Simple but effective approaches to achieve screen and velocity enhancement in the channel are using single gate structure but change the threshold voltage along the channel. Shur[8] has suggested a FET consisting of two threshold voltages in the channel to improve the channel electric field distribution. Many related new device structures, such as low conductive drain(LCD) HFET[73] and double recessed asymmetric HFET[74],[75], have been demonstrated to be effective in improve device performance. In this thesis, we propose another single gate device structure to effectively improve device performance.

It is well known that among the FET structural and physical parameters that determine its channel threshold voltage, one is the work function of the gate material. The

principal feature of the work function is that it is inherent to the material but invariant to changes in the channel structural parameters. This indicates that two gates in contact with different threshold voltages can be achieved by simply using two gate materials with different work functions. This leads to a new device structure — dual material gate (DMG) field effect transistor where the gate consists of two laterally contacting materials with different work functions. By keeping two threshold voltage zones, higher near the source than near the drain, the DMG-FET retains the screening and speed enhancement effects of the dual/split gate structures, while intrinsically eliminating the fringing gate to gate parasitic capacitance of the dual/split gate FETs and simplifying the gate control to only a single bias.

In this chapter we present the physical principles that will help understanding of the new DMG structure, which can be used to all types of FETs, including MOSFET, MESFET, and HFET. We use HFET as a vehicle to explore the potential advantages of the DMG structure. The new DMG-HFET device have the improved characteristics of the dual gate and split gate HFETs, since the general form and operation of the DMG-HFET is similar to the dual gate and split gate HFETs. We consider the DMG-HFET as a result of shrinking the separation of two cascade gates to zero. The new structure has been numerically simulated using PISCES, a 2-D device simulator, which provides an insight into the physical behaviors of DMG-FETs. Details of the PISCES simulations are presented in Appendix A, which describes major issues concerning PISCES, including theoretical background, physical models, material parameters, and example of our simulation. In this chapter, several device structures will be simulated. In fact, as mentioned in Appendix A, all these simulations use same physical parameters shown in the appendix except some structure parameter changes.

The organization of this chapter is as follows. First, in Section 5.2, the general dual gate HFET simulation and the screening mechanisms are described in Section 5.3, the velocity enhancement effect is discussed for the split gate HFET. The new dual material gate HFET is introduced in Section 5.4, in which the basic DMG-HFET device structure is considered and its physical principles are presented. In Section 5.5 we present comparisons of the DMG-HFET with other related device structures. Finally, in Section 5.6, we summarize the concept of dual material gate HFET and other related physical concepts.

5.2 Screening Effect in Dual Gate FET

We have performed a DC PISCES simulation for the dual gate HFET(DG-HFET), the structure of which is as shown in Figure 5.1, similar in material structure as described in Appedix A. The gate regions of the channel are named control-zone (under gate 1) and screen-zone (under gate 2), which will be justified further on. The device considered and simulated here has a planar structure. The gate contacts are formed in a recessed manner. The effect surface potential in the recessed region is simplified in the numerical simulation by specifying high density of deep level impurities at the surface. Detail of this treatment in the simulation is presented in Appendix A. In practice, the effect of surface depletion may behave differently and influences the device performance other way[63]. As can be seen from Fig. 5.1, we have selected another heterostructure system, InGaP/InGaAs material system. This is mainly due to the simpler gate recess process control of the InGaP/InGaAs material system. The highly material selective etching of GaAs against InGaP[76] can provide a technological advantage concerning ending

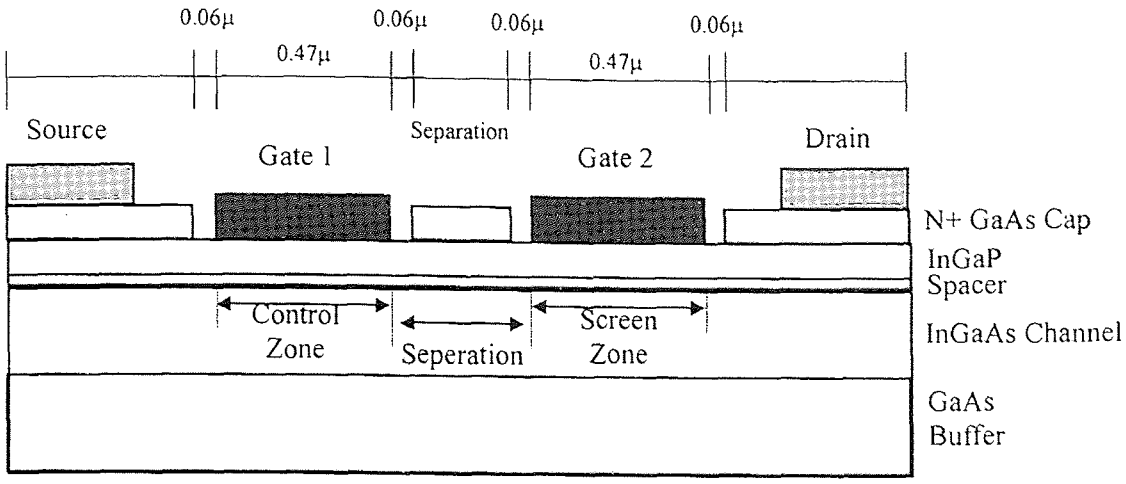


Fig. 5.1 Typical Schematic Cross Section of Dual Gate HFET
$V_{t2} > V_{gs1} - V_{t1}$.

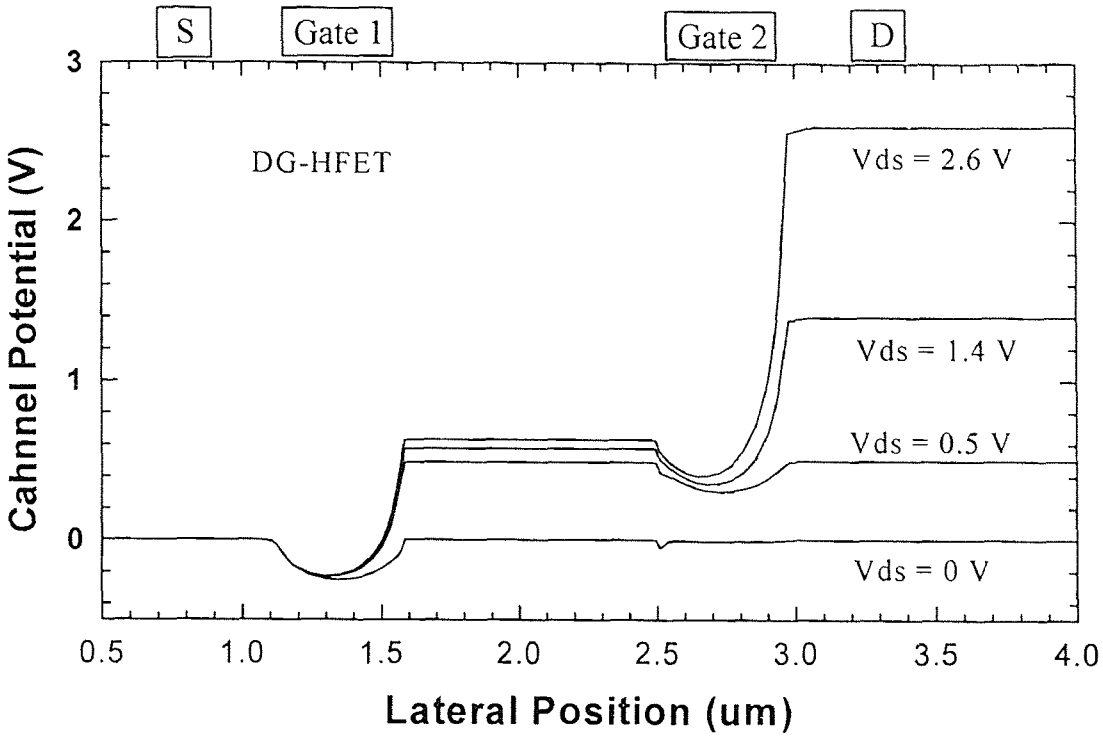


Fig. 5.2 Profile of potential variation along the channel for dual gate HFET with gate to gate separation of 1μm (Gate length of both gates are 0.47 μm). Vgs = - 0.6V.

point control. Another advantage of this material system is that the high valence band offset of InGaP/InGaAs heterointerface acts as a hole barrier and reduces hole-induced gate leakage current. HFETs with InGaP barrier layers have been reported with improved characteristics[77],[78],[79].

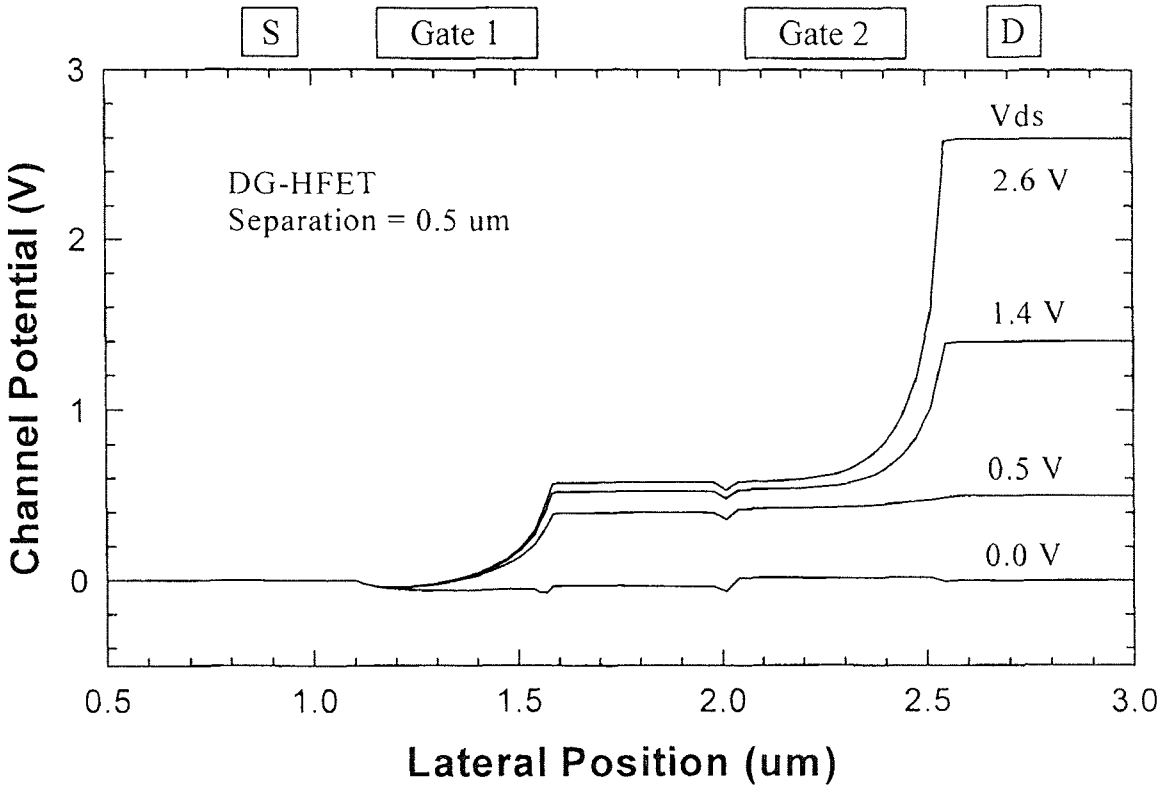
As described in details in Chapter 3, in order to bias the two channel zones into saturation simultaneously, the screen-gate driving voltage V_{gs2} - V_{t2} must be greater than that of the control-gate V_{gs1} - V_{t1} in such a way that at low V_{ds} the screen-zone is less resistive than the control-zone. The device is then simulated with $V_{gs2} = V_{gs1}$ but $V_{t1} = V_{t2} + 0.3$ V to keep a conservative condition of V_{gs2}.

By studying the potential variations along the channel for several V_{ds} as shown in Fig. 5.2, it is possible to have a better understanding of the respective role of two gates in the control of the channel current. Below 0.5 V drain voltage, i.e., before the current saturation, the drain to source potential is entirely absorbed in the region of the channel with small electron density that is to say under the control gate. The potential barrier that controls the electron injection is gradually lowered under the influence of V_{ds} and the current increases. In this drain voltage region, the screen gate has no influence on the device operating. Beyond 0.5 V drain bias, the additional drain voltage is not absorbed under the control gate but under the second gate. In other words, the first gate region is screened from drain potential variations. The electron injection is then well commanded by the control gate and the current saturates. This justifies the name of control gate (gate near the source) and screen gate (gate near the drain) used in this chapter.

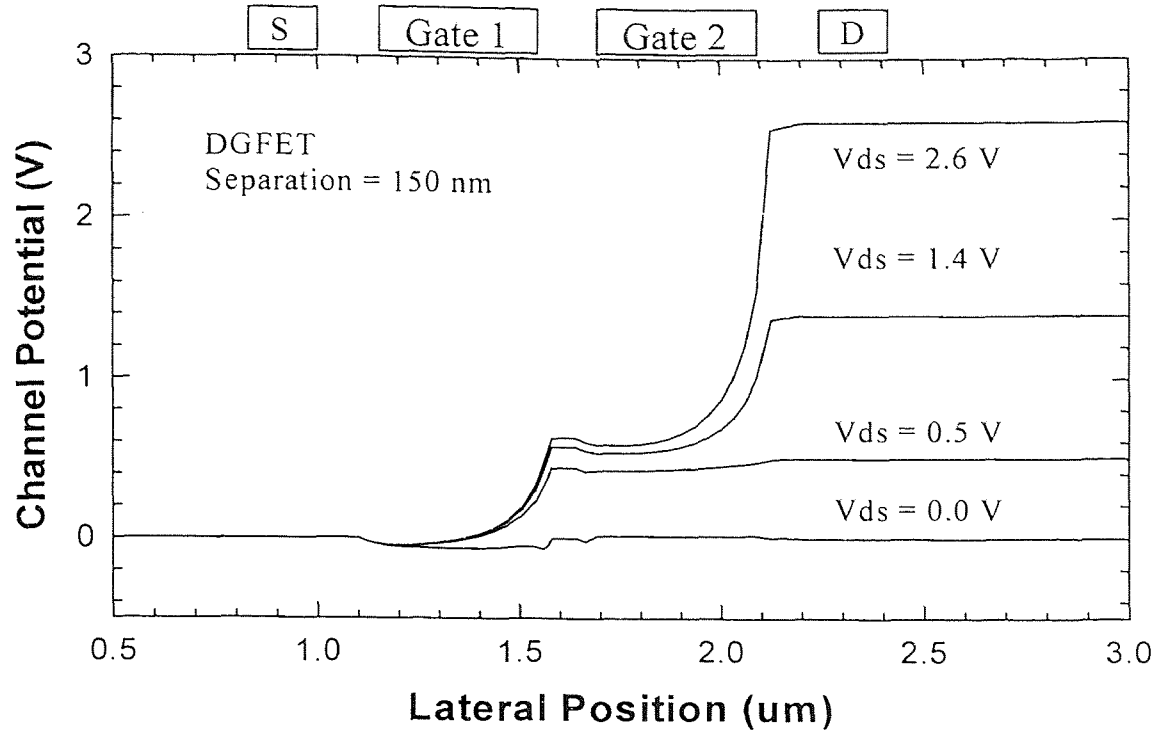
The screening mechanism can be described as follows. At low V_{ds} the longitudinal electric field builds only in the more resistive zone of channel, i.e., in the

control zone. If V_{ds} is high enough, a high field domain built up and grows just behind the control gate. Therefore, further increasing of drain bias will only change the field distribution along the screen zone. The screen zone then becomes more resistive than the control zone and absorbs the additional drain potential.

As we demonstrated in previous chapters, short channel effects can be effectively suppressed by introducing a second gate between the control gate and the drain. At lower control gate voltages the second gate allows to screen the potential barrier at the entrance of the active zone from drain voltage variations. As a consequence, V_{ds} has only a very small influence on drain current after saturation and the output conductance of the device is very small. Thus noticeable improvement in device short channel effects can be



(a)



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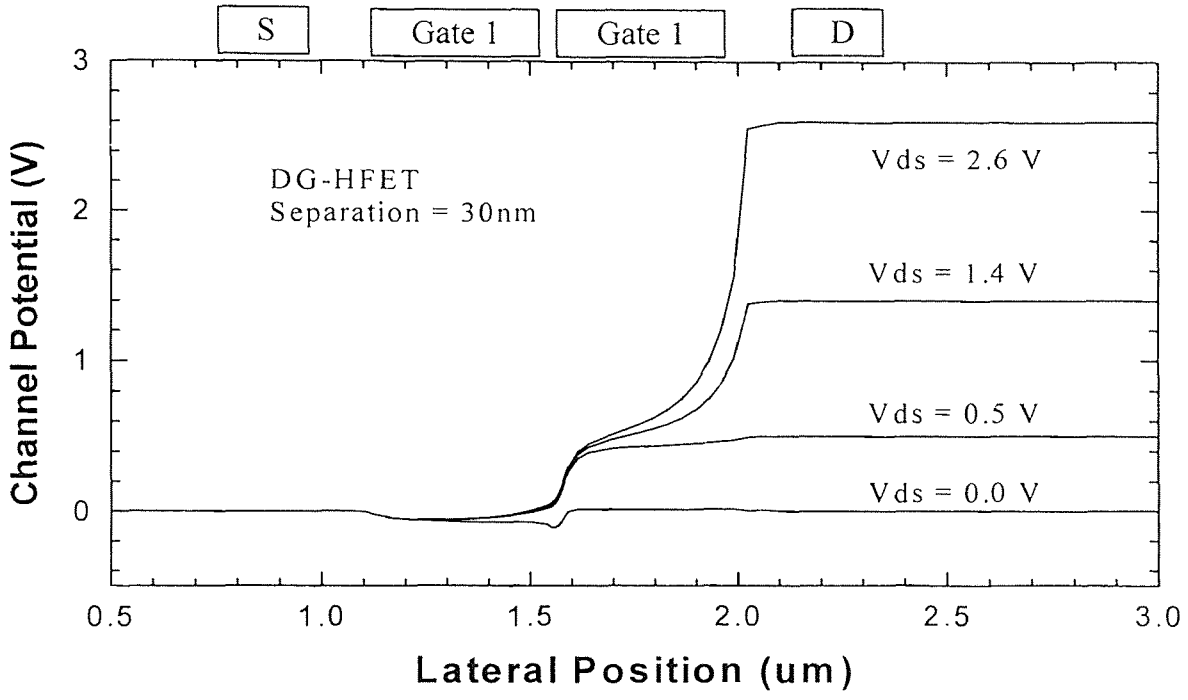


(c)

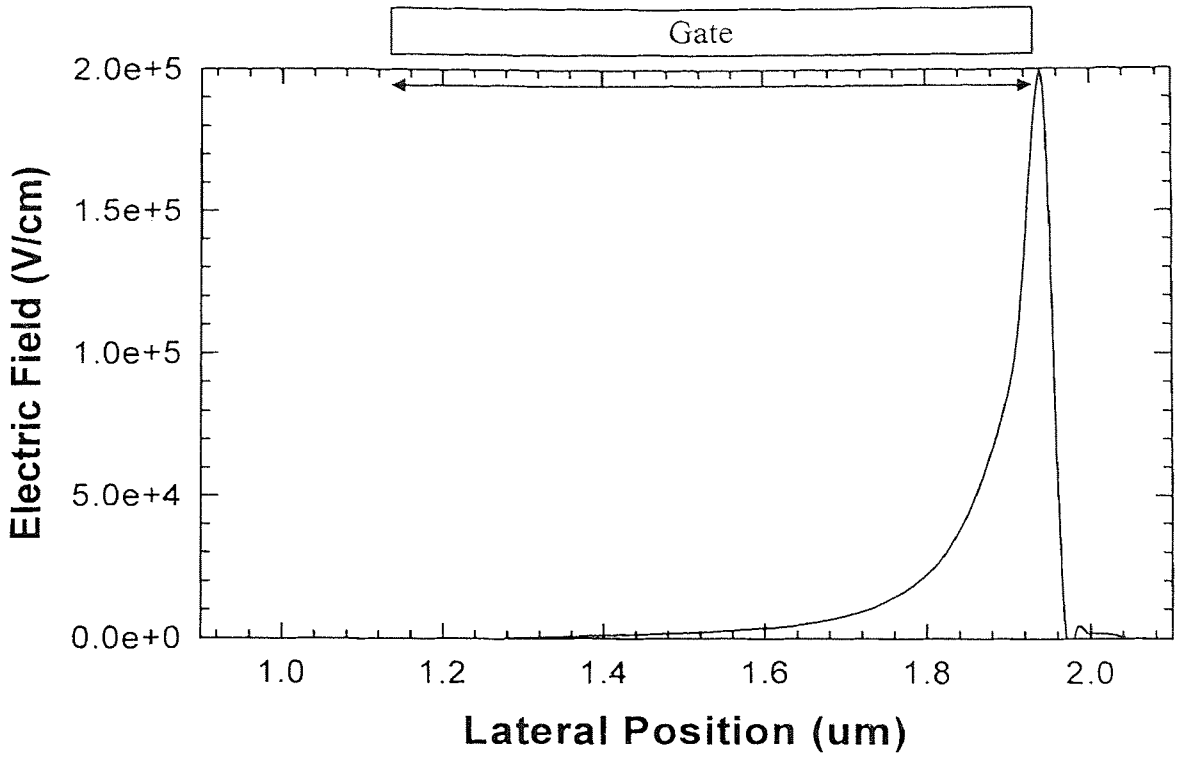
Fig. 5.3 Spatial variation of channel potential for various values of gate separations. Screening effect is retained true for all the gate separations studied. Vgs = - 0.4V.

achieved by this screening effect. It should be noted that this improvement is under same aspect ratio which is gate length divided channel depth. As we know, increasing aspect ratio is a very important way of suppressing short channel effects. Keep long channel aspect ratio and shrink the channel length is a main method of device scaling down. In practice, since reduce the channel depth also increase the gate capacitance which will reduce device speed, a treat off is required to balance the performances between short channel effects and speed. Thus, screening effect, suppressing short channel effects at fixed aspect ratio or channel depth, will benefit the device overall performance.

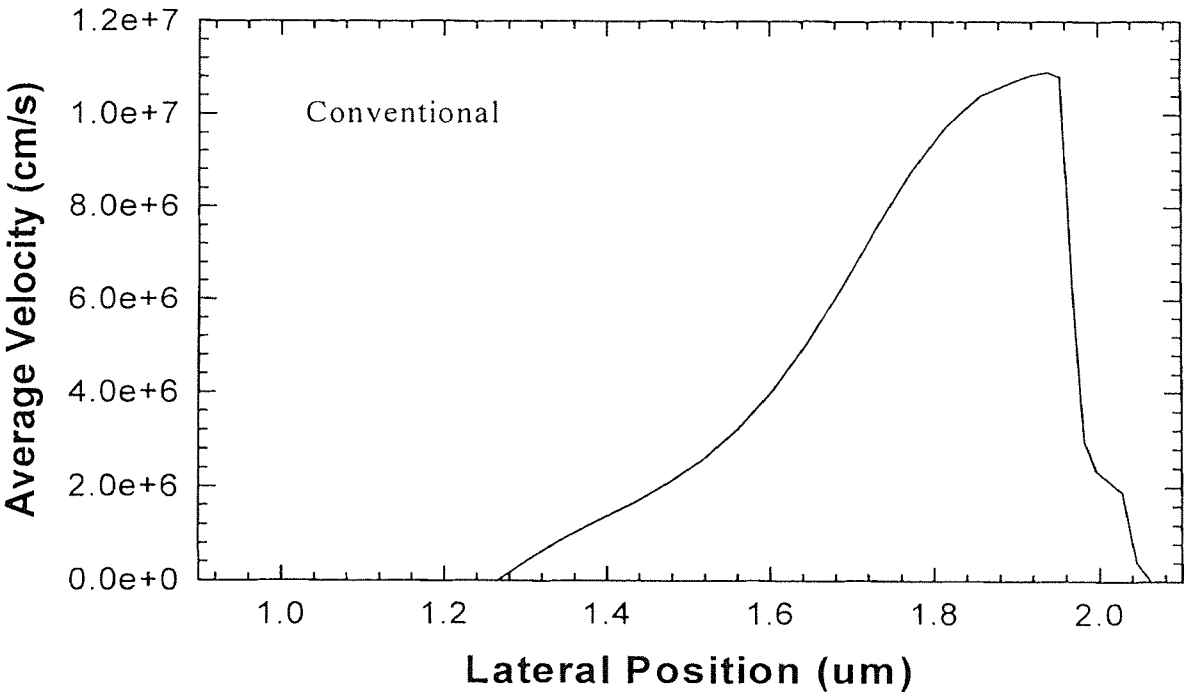
Fig. 5.3 represents the potential profiles along the channel for various gate to gate separations. (a) is a split gate HFET with a gate separation of 0.5 μm. (b) has a separation of 0.15 μm, while (c) has the two gates in contact. It is found that as long as the threshold voltages V_{t1} and V_{t2} of the two gates are kept unchanged, the screening effect remains basically the same for the 3 cases. This important result will be used in the construction of our new DMG-HFETs.

5.3 Velocity Enhancement Effect in Split Gate HFET

Under certain conditions, in the FET with an extremely short channel, electrons move ballistically from source to drain[80],[81],[82], i.e. they reach the drain without collisions with phonons and impurities, which are the causes for them to reach an equilibrium or saturate velocity. The ballistic transport of electrons may boost their velocity far beyond the values expected for a long channel FET. Even in a FET with somewhat longer channels, owing to the so-called "overshoot" effect, the electrons may still reach a velocity greater than the saturate velocity[83]. The overshoot effect is most prominent for FETs using GaAs and other III-V materials, in which the high speed or hot electrons may



(a)



(b)

Fig. 5.4 Profile of electric field and electron velocity along the channel for conventional HFET with a gate length of 0.8 μm. Vgs = - 0.4V, Vds = 1.2 V.

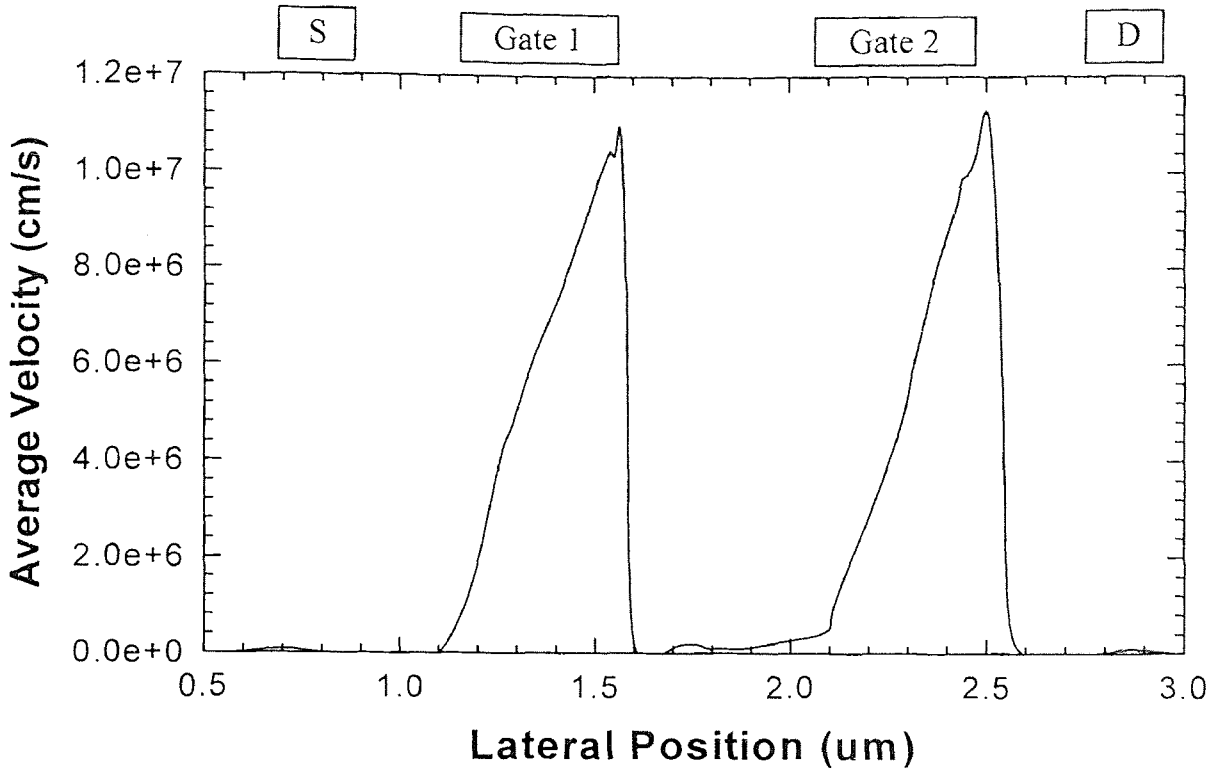


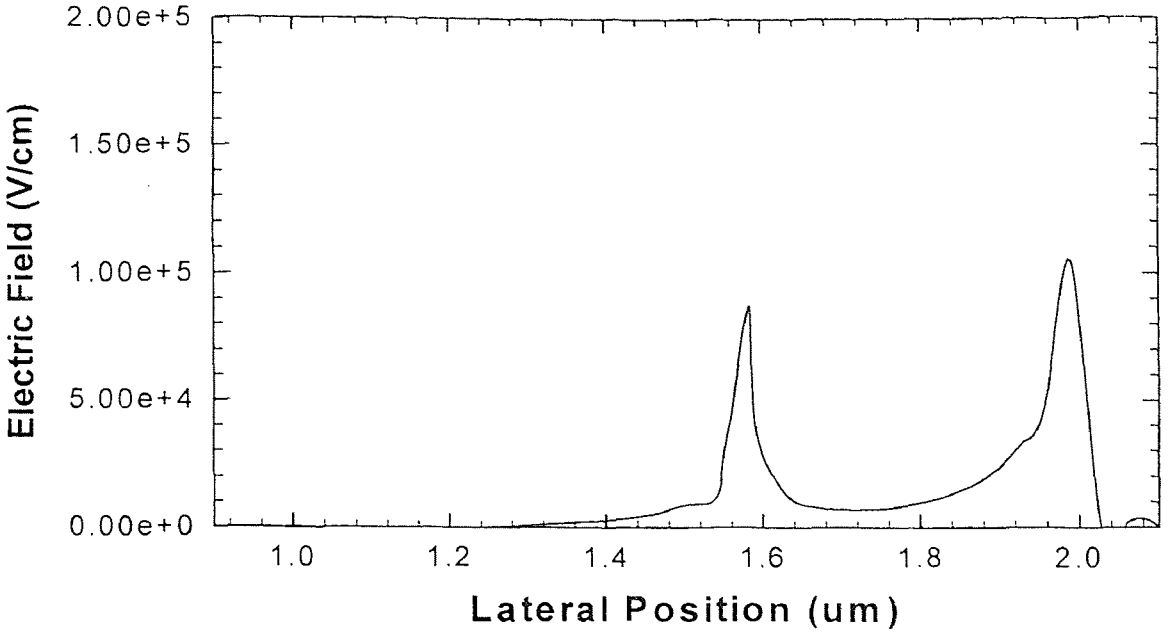
Fig. 5.5 The electron average velocity profile of a conventional DG-HFET with a large gate separation of 0.5 μm. Vgs1 = - 0.4V, Vgs2 = - 0.3V, Vds = 1.5 V.

loose their kinetic energy when scattered from Γ valley into X valley, which has a larger effective electron mass than Γ valley. It should be noted that PISCES has the capabilities to simulate the carrier and lattice temperatures in heterostructures. Hence, various non-stationary phenomena such as hot carrier effects and velocity overshoot can be analyzed using this program[84].

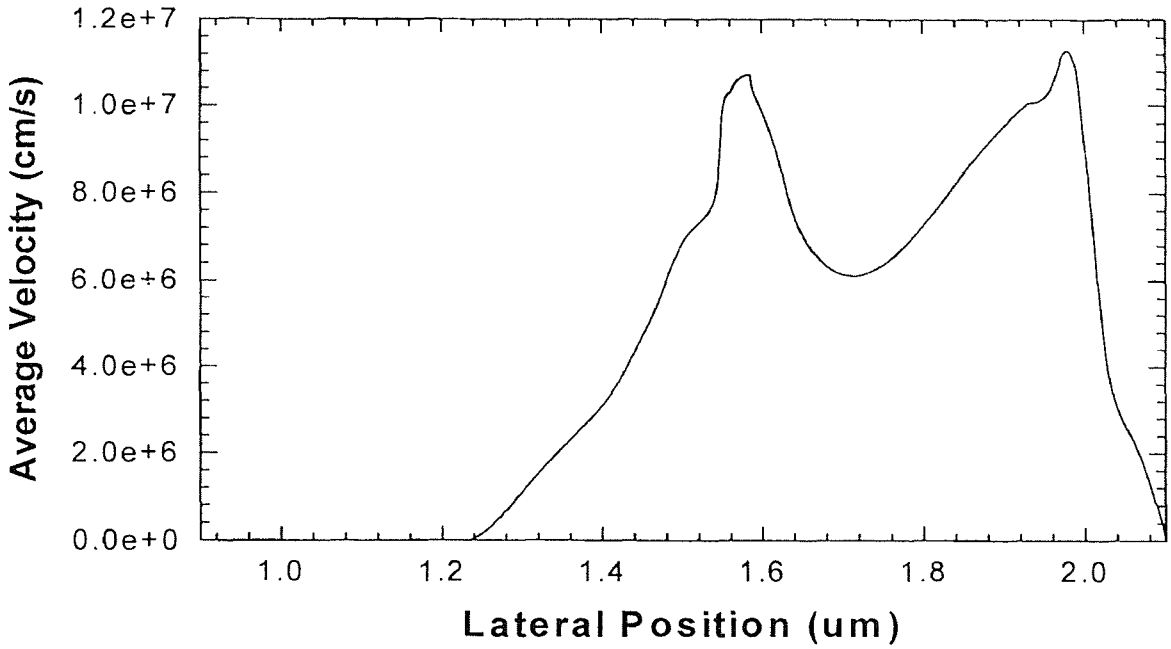
In a field effect transistor, electrons enter into the channel with a low initial velocity, gradually accelerating towards the drain. As numerous numerical simulation results(see, for example, [85]) and our numerical simulation of Fig. 5.4 indicate, the maximum electron drift velocity is reached near the drain. The electrons move fast in the region near the drain but relatively slow in the region near the source where they are

more likely to experience collisions. The device speed is determined by the overall transit time under the gate and, hence, the speed is heavily affected by a relatively slow electron drift velocity in the channel near the source region.

M. Shur proposed an idea to fully utilize the benefits of the ballistic and overshoot transport which is to change the electric field or electric potential distribution along the channel in such a way that electrons are accelerated more rapidly, leading to an enhanced average electron velocity in the channel[8]. This cannot be achieved by a conventional dual gate HFET, as shown in Fig. 5.5, since the electrons are cooled down in the fairly large intergate region. The average velocity enhancement, however, can be achieved by using a dual gate HFET with extremely small gate to gate separation, as shown in Fig. 5.6. The two high electric field distributions under the two gates overlap in the extremely short inter-gate region and, hence, electrons are rapidly accelerated under the gate that is closer to the source, move with high velocity through the gap region without significantly cooling down and travel into the high field drain region, resulting an enhanced overall electron average velocity. This fundamental difference between a conventional dual gate HFET and a DG-HFET with extremely small gate separation leads to the need for a different name of split gate, or SG-HFET for the latter. Note that in a velocity enhancement DG-HFET or SG-HFET, for the electrons not to cool down in the inter-gate region, the separation between the gates should be smaller than or in the order of the effective channel depth, d_{eff}, as shown. It should also noted that the high field drift region extention behind gate 2 is limited here by the self aligned N+ cap layer, which is 60nm away from the gate edge to reduce the series resistance. This length is approximately corresponding to the drift region length generated by 2.5 V of the drain



(a)



(b)

Fig. 5.6 The electric field (a) and average velocity (b) profiles along the channel of DG-HFET with extremely small gate separation (30 nm). Electric fields in the two gate regions overlap resulting velocity enhancement. Vgs1 = - 0.4V, Vgs2 = - 0.3 V, Vds = 1.5V.

bias[86]. Therefore, further increasing of Vds might negatively influence feedback capacitance and drain conductance due to the limited gate to drain separation[87].

In short, the electron transport in DG-HFETs can be made considerably faster by utilizing lateral field overlap between the gates. This can be achieved by making the gates separation extremely small. However, beside the technological difficulty in realization, this approach brings in addition fringing capacitance between the gates which will be detrimental to device performance.

5.4 The Introduction of Dual Material Gate FET

The characteristics of dual gate HFET have been investigated extensively in chapter 2 and 3. In the earlier sections of this chapter, the screening effect of the DG-HFET has been further analyzed for the purpose of better understanding and more insight into the physical origins of the effects. It was shown that the split gate HFET, or the DG-HFET with an extremely small gate separation, has higher overall electron velocity and shorter transit time than a conventional DG-HFET. On the other hand, the SG-HFET introduces a detrimental parasitic gate to source capacitance, hindering its high speed performance.

In order to take full advantage of both screening and velocity enhancement effects while avoiding the detrimental parasitic capacitance, a new approach to device design is necessary. Here, we propose the concept of dual material gate (DMG) structure which consists of two laterally contacting gate materials with different work functions. This structure exploits the high average electron velocity of the split gate HFET and the short channel suppressing screening of the dual gate HFET. The idea is to change the threshold voltage along the channel with the material work function difference in such a way that work function near the source is higher that that near the drain. Although the two metal or

metal like gate materials contact each other and have a common gate potential, the threshold voltage under gate material zone near the source is higher, since the threshold voltage is a function of its gate material work function.

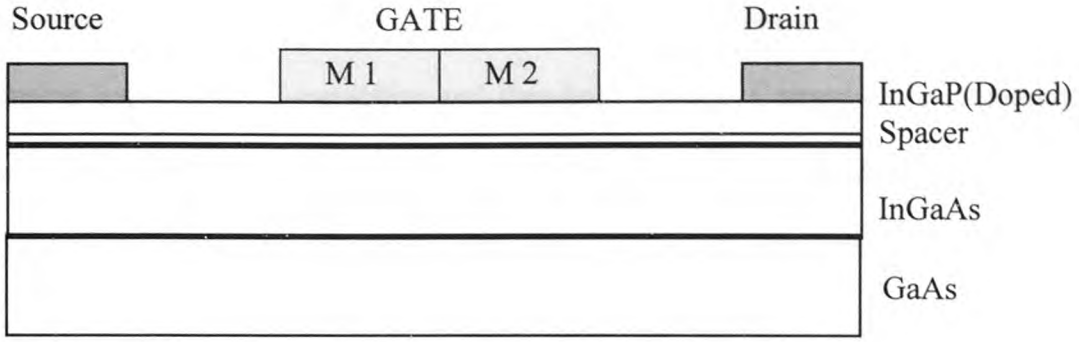


Fig. 5.7 Dual Material Gate HFET(DMHFET) structure consisting of gate using two lateral contacting materials with work function of M1 larger than that of M2.

Fig. 5.7 shows the proposed DMG-HFET structure. By choosing a material with higher work function near the source, we make the threshold voltage of this section of the channel more positive, thus introducing a threshold discontinuity and increasing the electric field near the source. This will lead to a more rapid acceleration of electrons near the source, as well as the screening of drain voltage to supress the short channel effect.

Similar to the case of Dual Gate HFET in section 2, the first gate material near the source play the role of channel current control, whereas the second material near the drain serves as screen zone. The difference here is that the second channel under total second material zone now can be depleted completely as an extension of the depletion region of the first channel.

For a given gate voltage, when changing the drain bias, the first channel will be pinched off first limiting the drain current, while the second channel still work in the

linear regime due to the more negative threshold voltage. The further drain bias will be mainly dropped in the second channel and pinch off the second channel. Because of the more negative threshold voltage, the second channel will not limit the channel current. We note that this not only retain the current drive capability of the first channel, but also will not waste the drive capability of the second channel. This can be understood by the relationship between drive capability and threshold voltage. Current drive increased by simply reducing the threshold voltage has boundary condition. The threshold voltage is optimized by the practical application and is usually fixed at certain value. In the case of DMG-FET, as we will show in section 6.2, the overall threshold voltage is determined

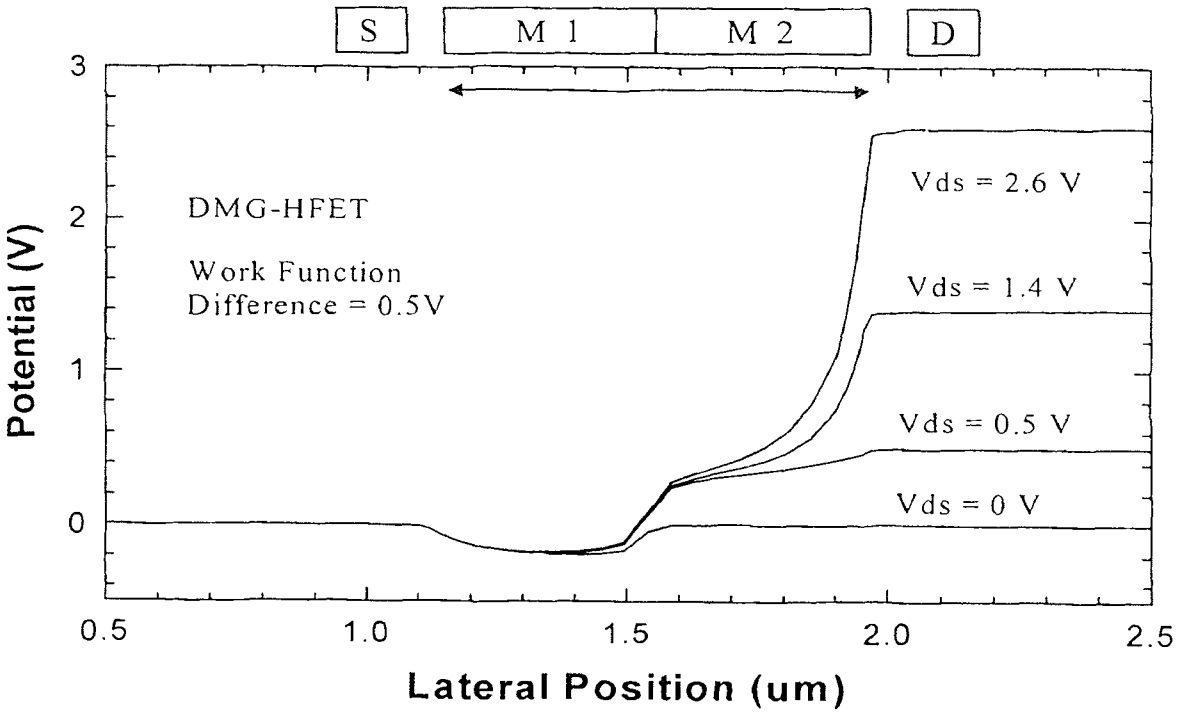


Fig. 5.8 The channel potential profile for dual material gate HFET with gate length of 0.8 μm. The applied gate voltage is -0.6 V. Strong screening effect is demonstrated. The two material work function difference ΔW is assumed to be 0.5V with W1 > W2 or Vt1 > Vt2.

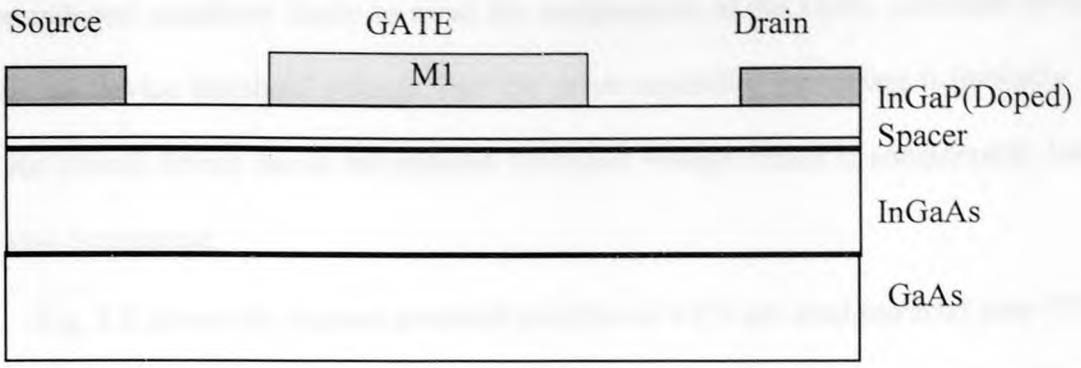


Fig. 5.9 Schematic cross section of conventional single material gate HFET.

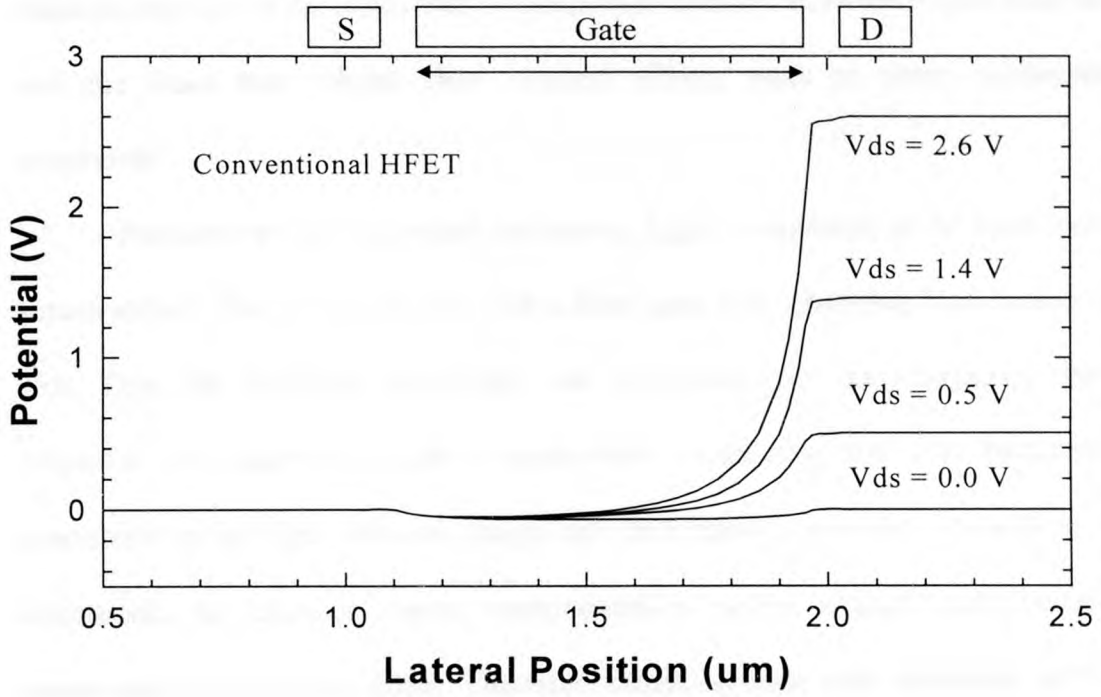


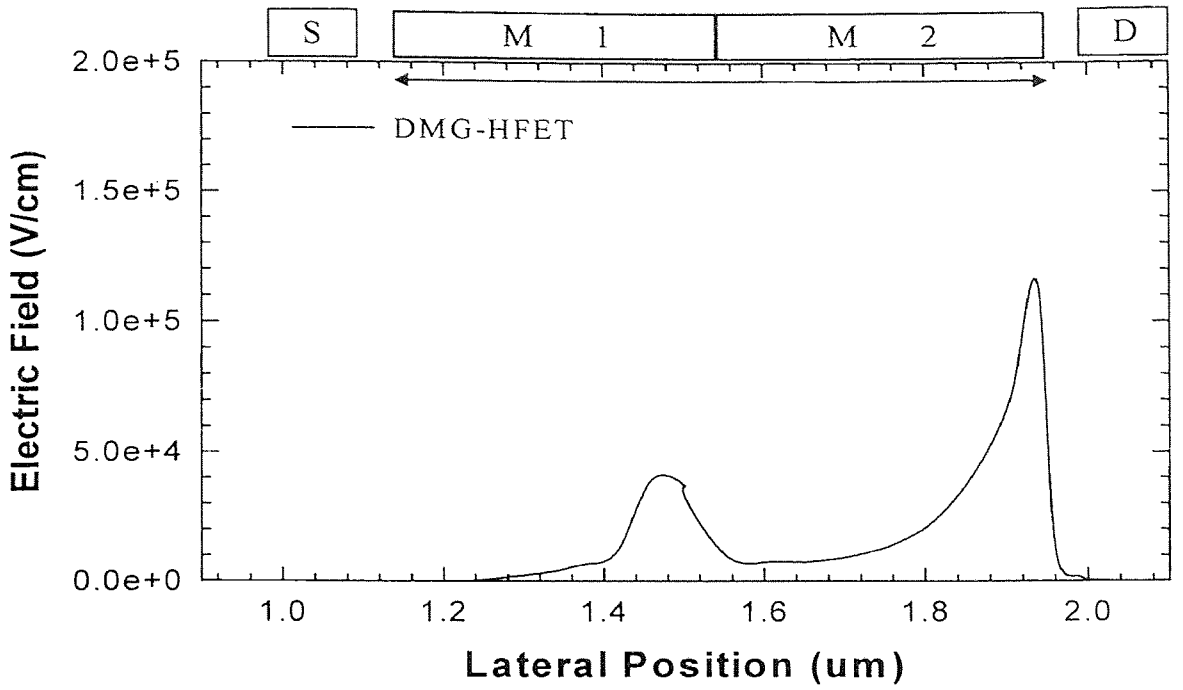
Fig. 5.10 The channel potential profiles of conventional HFET with different drain biases. The gate length is 0.8 μm; gate bias is -0.6 V. There is no screening effect in this situation. The M1 gate material of DMG-HFET is used here for the gate.

by the more positive material or first channel. Thus the threshold of the second channel can be reduced somehow freely to meet the requirement of the DMG structure without influencing device threshold voltage. But this drive capability increasing is basically not good for overall device due to the reduced threshold voltage which is considerably lower than what is required.

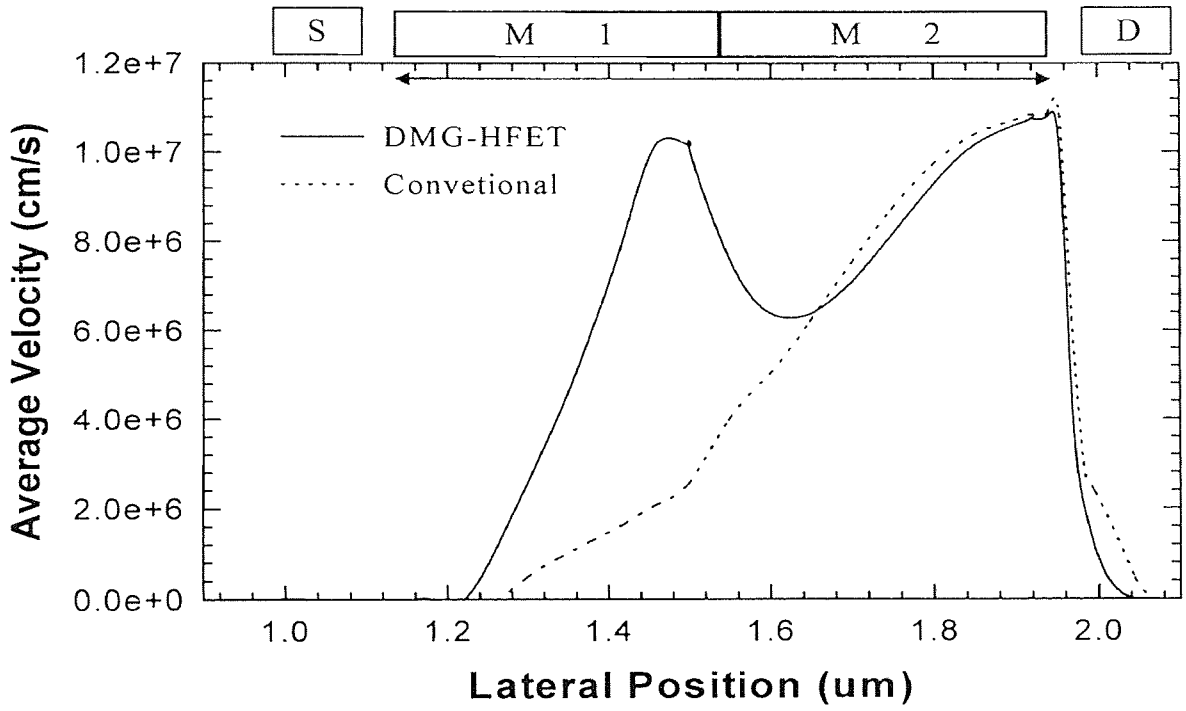
Fig. 5.8 shows the channel potential profiles of a 0.8 μm dual material gate HFET with gate bias at - 0.5 V. It shows a very good screening characteristics, similar to conventional dual gate HFETs (Fig. 5.2). When the drain is biased above 0.5 V, unlike the conventional single material gate case shown in Fig. 5.9 and Fig. 5.10 without screening effect, the further drain bias causes the changes only in the region under gate material near the drain. Drain bias is effectively screened from the region near the source and the drain bias related short channel effects, such as drain conductance, are suppressed.

Furthermore, an important parameter, Cgd, is expected to be improved by this screen effect. This is because that, for a fixed gate bias, changing Vgd is also changing Vds. Thus, the feedback capacitance can be obtained by the change of charge with respect to Vds, under the ac gate to source short circuit condition. Two main components contribute to the Cgd: channel charge and drift region extension. According to above discussion, the channel charge contribution(or current change) will be effectively suppressed by the screen effect. Therefore, assuming same drift extension for the DMG-HFET and SMG-HFET, the DMG-HFET is expected to have better Cgd behavior.

The electric field and average electron velocity profiles of DMG-HFET is shown in Fig. 5.11(a) and Fig. 5.11(b), respectively. There is still high electric field distributed in inter-gate region due to the screening effect, which will give rise to the further



(a)



(b)

Fig. 5.11 Electric field (a) and average electron velocity (b) profile of dual material gate HFET. In (b), the velocity profile of conventional single material gate HFET is also show for comparison.

acceleration of traveling electrons in this region. In Fig. 5.11(b), the velocity profile of conventional single material gate HFET is also shown as a comparison. The curves clearly indicate that velocity of DMG-HFET has another peak around the two gate material interface and the average velocity of DMG-HFET is always higher than those of the corresponding conventional single material gate HFET. Thus DMG-HFETs are expected to exhibit considerably higher speed over convention HFETs.

Due to the limited scope of this thesis, our study is concentrated on normal HFET with channel length around 0.8μm and aspect ratio about 30. We believe that similar results can be obtained when shrinking the channel length and keeping the same aspect ratio. For deep submicron devices, however, such as 0.1μm, it is difficult to reduce the channel thickness to the value (32Å) accordingly due to the tunneling. Thus the aspect ratio needs to be decreased for short channel device, and this make short channel effect more severe when shrink the channel length. DMG structure opens a new way to suppress short channel by introducing screening effect. It is expected that this improvement will be more pronounced for small aspect ratio or deep submicron devices as long as other effects were not dominating.

5.5 Comparison of Dual Material Gate HFET with Other Related Device Structures

In the view of the trend of improving FET saturation behavior, Device structures based on asymmatric design have become very attractive, because of its ability to modify channel electric field distribution. In order to suppress short channel effects and inprove breakdown, several promising asymmatric structures are proposed. These include Asymmetrical Lightly Doped Drain(A-LDD) MESFET[88], Asymmetrical Double

Recessed (LDR) MESFET[89], Low Conductive Drain (LCD) HEMT[90], Lightly Doped Deep Drain MESFET[91] and Floating Gates MESFET[92]. These structures successfully increase breakdown voltage and improve output conductance and feedback capacitance behaviors. But in these structure, the transconductance and source resistance are either unchanged as compared to conventional structure or are degraded by the parasitic resistance in the case of LDD[88],[93]. The DMG structure add another member to these asymmetical FETs. A remarkable feature of the DMG structure is its ability to enhance device transconductance and drain current in addition to overcoming short channel effects.

Another solution to enhance device transconductance and drain current is to realize FET with non-uniform channel doping[94],[95](Fig. 5.12). By doping more impurities near the drain than that near the source, the threshold voltage is gradually decreased from the source to the drain. Such a device can be made using tilt angle ion implantation in the region closer the source. Since the electric field under the gate closer to the source is larger, the transport properties of electrons in the channel or transconductor of the device are improved due to the average electron velocity improvement as shown in Fig. 5.13. The short channel effects, however, have not been noticeably changed due to the lack of screening effect as described for DMG-HFETs. This is clearly seen from Fig. 5.14. The numeric simulations demonstrate that in normal asymmetric channel HFETs, there is no screening effect for short channel suppressing.

Further theoritical investigating indicates that this asymmetrical channel doping structure can induce screening effect by discontinuously doping the channel supporting layer (Ns). Since $\Delta Vt \propto \Delta Ns$, threshold voltage therefore changes abruptly as the Ns

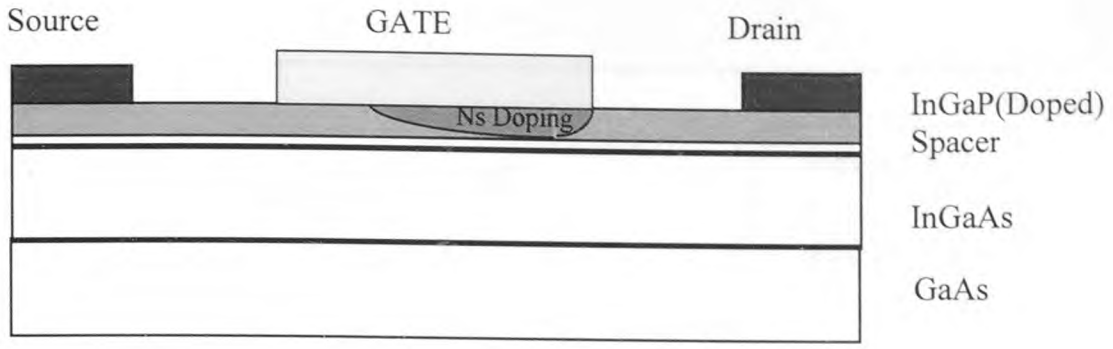


Fig. 5. 12 Schematic cross section of asymmetric channel HFET. More n-type doping is introduced in the region near drain making drain side threshold voltage less positive.

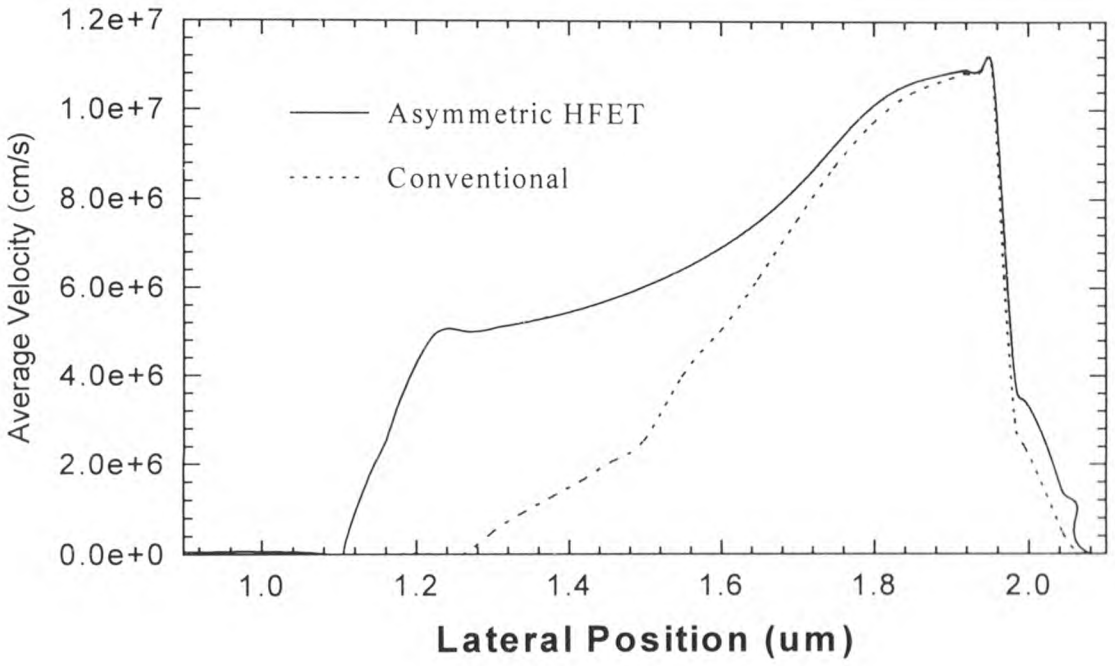


Fig. 5.13. Channel electron average velocity profile of asymmetric HEFT. Velocity enhancement is achieved by asymmetric threshold voltage distribution. Asymmetric structure is assumed to have same structure except Ns doping which is linearly increased from source to the drain.

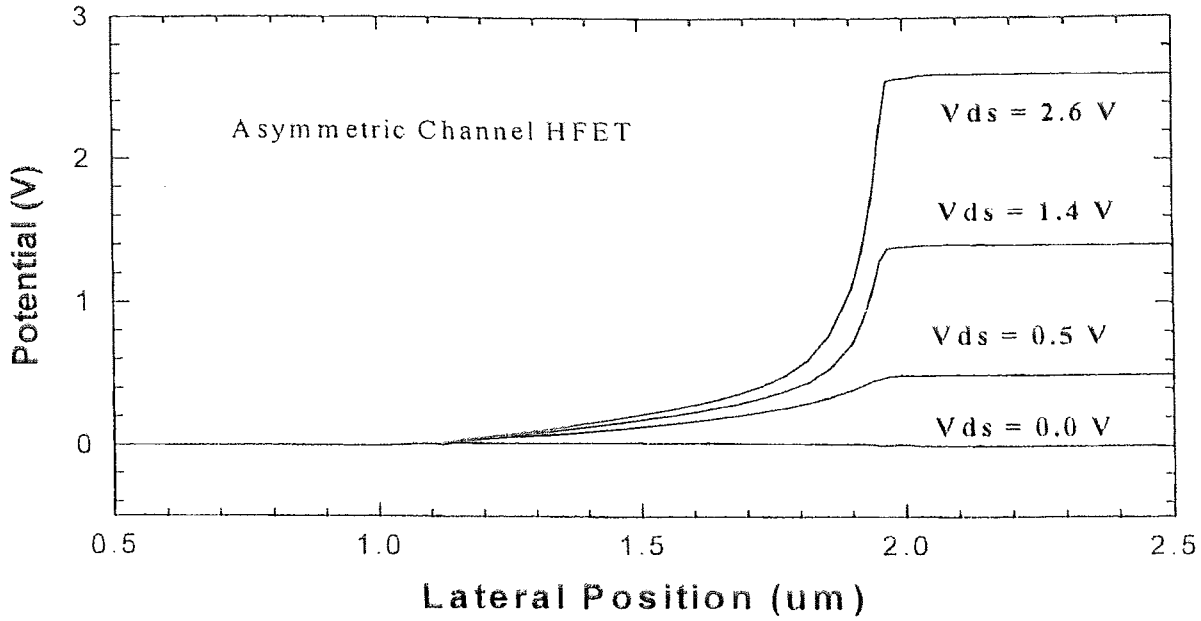


Fig. 5.14 Channel potential profiles of normal asymmetric HEFT. There is no evidence of screening effect. Asymmetric structure is assumed to have same structure except Ns doping which is linearly increased from source to the drain.

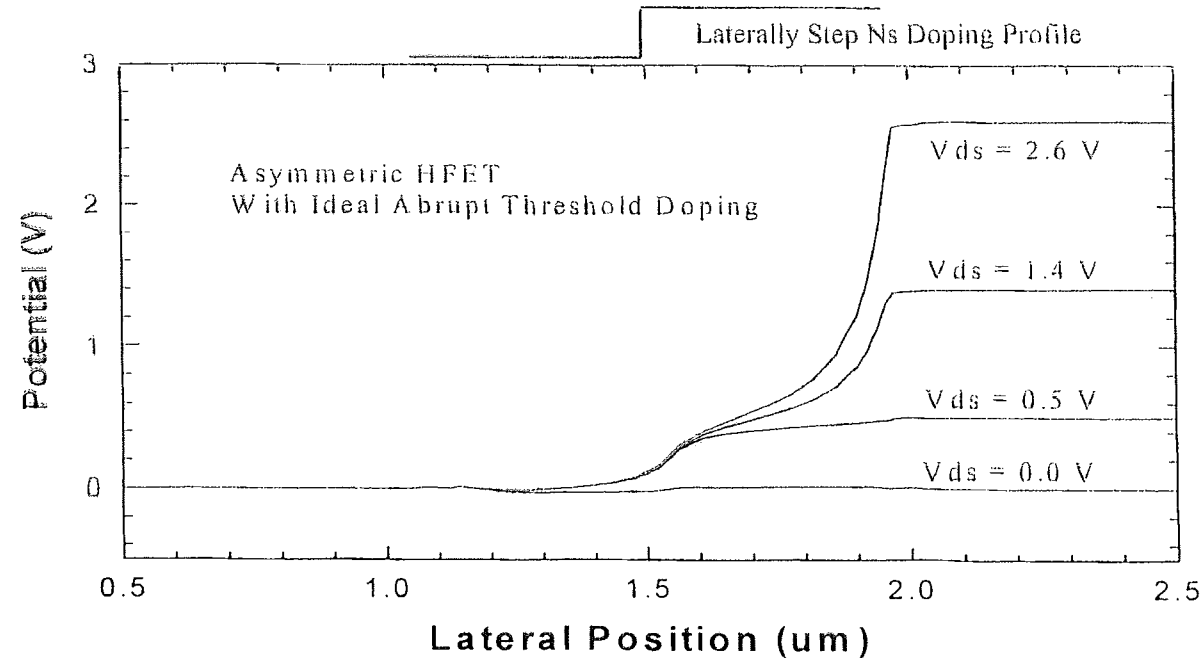


Fig. 5.15 The channel potential profiles of Asymmetric HEFT with ideal step Ns doping profile along the channel. Excellent screening effect shows up only at this theoretical situation.

changes discontinuously along the channel. The simulation result is demonstrated in Fig. 5.15. Screening effect is clearly shown. But this excellent screening behavior is extremely difficult and practically impossible to be realized due to the lateral redistribution during the doping activation. Thus, DMG-HFETs are essentially superior over this asymmetric channel HFETs and are more attractive device structure for both short channel suppressing and device performance improvement.

It should be noted here that both theoretical simulation and logic reasoning point out that the screening effect is due to the step change of threshold voltage along the channel. As numerous numerical simulations of conventional HFET clearly indicate (see, for example Fig. 5.4), electric field always peaks near the drain. This can be easily understood by the fact that a stepping change of threshold voltage exists in the end of channel near the drain. Therefore, we speculate that the high field region near drain can be effectively "compensated" by the field distribution inside channel when there is a step like change in threshold inside the channel.

This conclusion is important in evaluating new device structures like dual recess gate HFETs as shown in Fig. 5.16. Due to the gradual etching of wet etching feature, we predict that the performance of this device structure is inferior to our DMHFET, because of the obvious lack of screening effect.

We should point out that it is required in DMG-HFET to introduce a downward stepping change of threshold voltage instead of upward change, as it varies from source to the drain. In other words, if source side of the gate material has smaller work function, the screening effect will disappear and device performance will be somehow like a conventional HFET. Fig. 5.17 shows the channel potential profiles of DMHFET with larger work function in source side instead. Both screening and velocity

enhancement effects are missing in this situation and the related behavior of the device will not be improved in this structure.

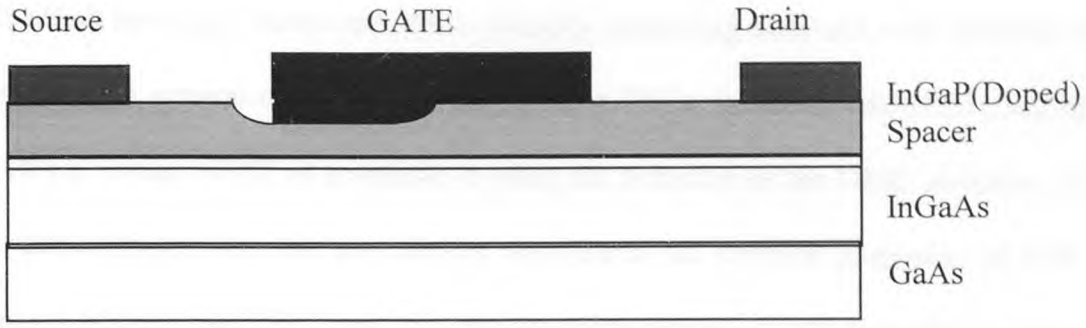


Fig. 5.16 Another DMHFET related asymmetric HFET structure using dual recess wet etching technology. Different threshold is realized via different channel depths.

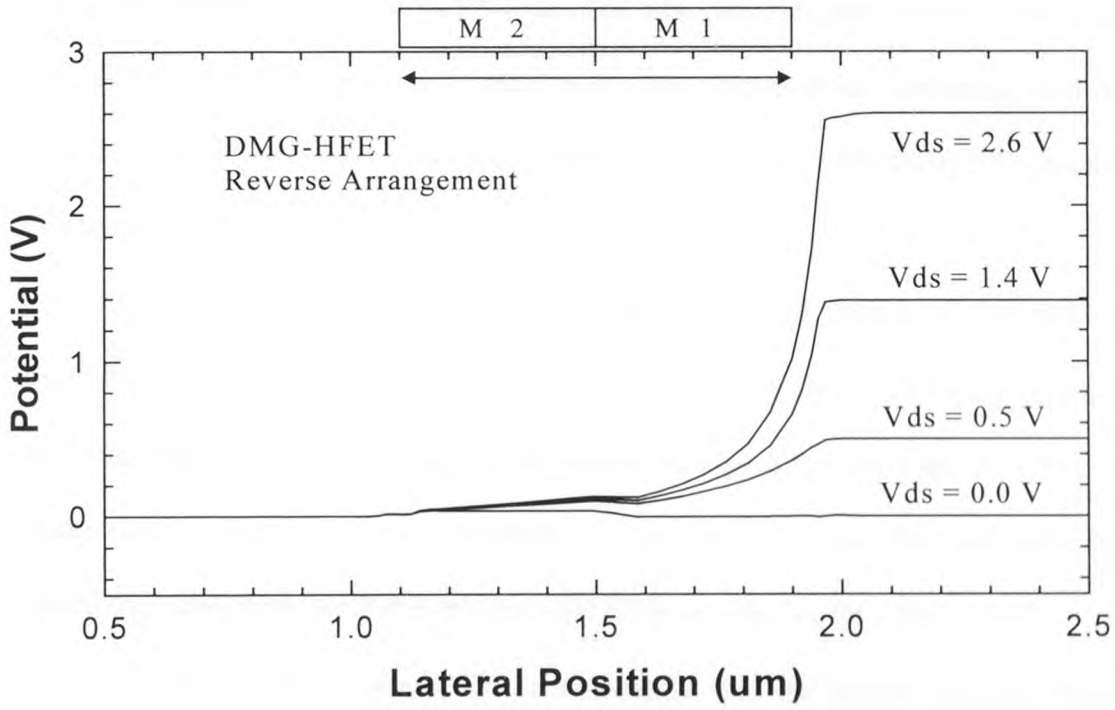


Fig. 5.17 Channel potential distribution of dual material gate HFET when inverse the gate structure to make threshold voltage near source smaller than that near the drain ($V_{t1} < V_{t2}$). There are not screening effect and velocity enhancement effect.

5.6 Summary

In this chapter, a novel device structure of dual material gate (DMG) FET is proposed and its related physical concepts studied via numerical simulation. The concept of DMG-FET, which has a gate composed of two laterally contacting materials with different work functions, is a general one, valid for all types of FETs, including MOSFET, MESFET, and HFET. Using HFET as a vehicle to study the behavior of the DMG structure, It has been demonstrated that this new device reproduces the superior properties of both the screening of dual gate HFET and the velocity enhancement of split gate HFET. This new device structure has been compared with other related device structures, and it is demonstrated that the proposed DMG-HFET has clear advantages over the other structures. It could be a preferred structure for high speed performance and short channel effect suppressing. As to our knowledge, this dual material gate HEFT is the first single gate device structure presented until now that shows both screening and velocity enhancement effect. The concepts related to this new DMG-HFET structure are summarized as follows.

It is concluded that the step like abrupt downward change of threshold voltage inside the channel from source to drain creates an electric field profile that warrants both the screening of the drain voltage in the saturation region and the overall carrier velocity enhancement. Since the gate potential is uniform, the detrimental parasitic gate capacitance associated with the split gate HFET is avoided in the DMG-HFET.

In conclusion, we would like to emphasize that the results obtained from a 0.8 micron DMG-HFET are expected to be valid for other FETs with other gate lengths.

CHAPTER 6

DMG-FET DESIGN AND ITS SIMULATED CHARACTERISTICS

6.1 Introduction

Designing single gate FET with high performance needs to optimize the key parameters, such as threshold voltage, channel length and channel thickness, and select best gate material. The threshold voltage is usally determined by application specification and is required to be adjusted to a certain value. Sufficiently short channel length and thin thickness are cretical in realizing high transconductance and high drive current. However, scaling down the channel length to submicron range leads to less effective carrier confinement in the channel and more severe short channel effect. Similarly, shrinking the channel thickness increases gate capacitance and faces some technological difficulties. Therefore, design and optimizing FET normally involves understanding the key device parameters and a trade-off among these parameters.

In the case of designing dual material gate (DMG) FET, more parameters are involved due to the more complicate structure. These include another gate material and its length. We therefore need to study effects related to these additional parameters.

First, we must choose two conducting materials for the DMG with different work functions, and therefore different threshold voltages, for the control zone and screen zone, respectively. The screening effect, which is related to the threshold voltage difference or the stepping change of the threshold, has been affected. In a conventional single material gate (SMG) HFETs, the gate material work function determines the threshold voltage range that can be realized, while in a DMG-FET, work functions have also become

significant factors, which determine the screening effect and related short channel effects in addition to the threshold voltage.

In addition to the selection of materials, it is also essential to select L_{m1} and L_{m2}, the lengths of the control zone and screen zone of the gate, respectively. For velocity saturation FETs, electrons are accelerated through the control zone L_{m1} from 0 to saturation velocity, and due to high field, velocity saturation, and velocity overshoot, they may continuously travel with almost this velocity through the screen zone L_{m2} until reaching at the drain. By adjusting L_{m1} and L_{m2}, we may optimize the most important device parameters, such as transconductance g_m and drive current I_{on}.

As discussed in the previous chapters, the concept of DMG-FET is evolved from the consideration of screening effect of the dual gate (DG) FET and velocity enhancement of the split gate (SG) FET. While in some aspects, the DMG-FET has similar behaviors as the DG-FET and SG-FET, however, certain fundamental differences do exist, since the nature of electron transport mechanism is different when the total length of the channel is considered. It is expected that the DMG-FET has its unique characteristics, different from any other device structures.

In this chapter, several unique design considerations for DMG-FET are presented which are based on numerical simulation results. These special design considerations of DMG-FET are theoretical and intrinsic in nature. Complete simulated characteristics for DMG-FETs based on the new design are also presented, and it is shown to be superior to conventional device structures.

The organization of this chapter is as follows. In Section 6.2, the threshold voltage of DMGFET is studied, in Section 6.3, the selection of gate material or work function

difference is discussed, and in section 6.4, the impacts of different length of the two gate materials are evaluated through 2D numerical simulations. In Section 6.5 the simulation of the high performance of DMG-FET is proposed, whereas in Section 6.6 is presented a systematic simulation of the device characteristics related to the short channel effects. An interest issue is discussed in section 6.7 in which an 1μm gate DMG-HFET is compared with a 0.5μm gate SMG-HFET. All the characteristics of DMG-FETs are compared with those of conventional SMG-FETs. Conclusions are drawn in Section 6.8.

6.2 Design Consideration 1: The Threshold Voltage of DMG-FET

It is well know that in conventional single material gate (SMG) FET, its threshold voltage is a simple linear function of the work function of the gate material. This means that keeping other parameters identical, different gate materials will result in corresponding threshold voltage shift. In DMG-FET, two gate materials are involved, therefore, its threshold voltage may behaves differently and further study is needed to clarify its special features.

The simulated threshold behavior or I_{ds}- V_{gs} curve for DMG-HFET is plotted in Fig.6.1, together with that for conventional SMG-HFET with same gate length(0.8μm). Except for the difference in gate composition, both the DMG-HFET and SMG-HFET have the same structure and geometry. The gate material of the SMG-HFET is the larger work function one of the two gate materials in the DMG-HFET for the purpose of comparison. As expected, they show almost the same threshold voltages when we do the extrapolation to extract the corresponding values from the plots. This verifies that the

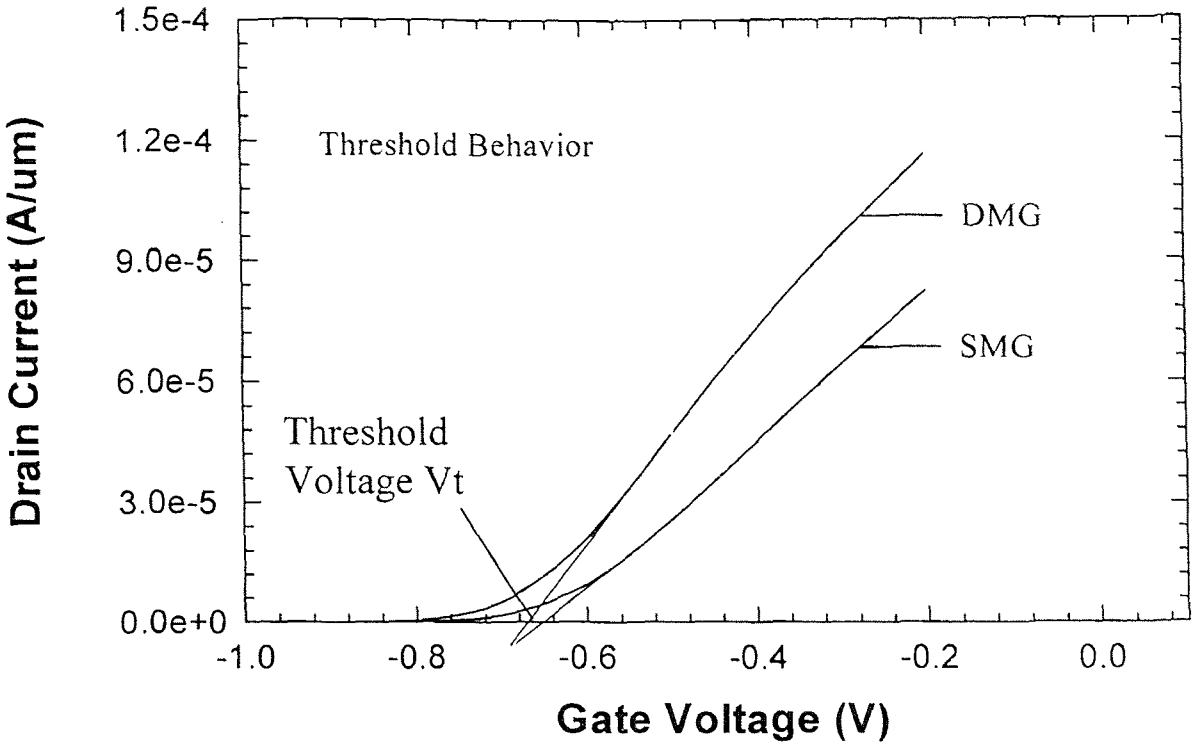


Fig. 6.1 The threshold behaviors of dual material gate HFET (DMG-HFET) and conventional SMG-HFET. Very close values (-0.67V for DMG and -0.65V for SMG)of threshold voltages have been extrapolated.

material with larger work function in the DMG-HFET dominates the threshold behavior. The physical interpretation of this interesting feature is that the maximum electron barrier height in the channel is introduced by the material with larger work function. Clearly, drain current is determined by the maximum electron barrier height along the channel, i.e. the potential minimum in the channel or the saddlepoint in the bulk region between the source and drain. Therefore, the device threshold virtually does not depend on the material with smaller work function. This fact is very useful in predicting the actual value of threshold voltage in a DMG-HFET from the device parameters.

6.3 Design Consideration 2: The Role of Work Function Difference of the Two Gate Materials

The work function of a conducting material is the energy difference between the vacuum level and its Fermi level. For ideal conventional single material gate FET(SMG-FET), its threshold voltage linearly depends on the work function of the gate material. For DMG-HFET, its threshold voltage is determined by the larger work function of the two gate materials and is no longer uniform along the channel. Thus, there is a threshold voltage offset along the channel material in DMG-HFET which is caused for by the laterally change of gate materials. Actually, this threshold offset is accounted for by the work function difference of the two gate materials.

We note that the relation between the gate material work function and the threshold voltage is complicated, involving many factors. For MESFET and HFET, the threshold is a linear function of Schottky barrier height ϕ_{bn} which is given by [48]

$$\phi_{bn} = B + S(W - \chi) \tag{6.1}$$

where B is a constant determined by other device and material parameters, S is Schottky constant which is a strong function of semiconductor surface states, oxides, foreign impurities, and other unstable candidates that have some uncertainties and are related to practical processing procedures. W is work function and χ is the electron affinity. Typically, S is close to 1 for large bandgap semiconductor, and reduces with the bandgap. Therefore, the threshold voltage offset ΔV_t can be written as

$$\Delta V_t = S(W_1 - W_2) \tag{6.2}$$

which is proportional to the work function difference.

For MOSFET, the effect of work function difference is to cause a direct voltage shift in the threshold voltage, and the threshold voltage offset is simply given by

$$\Delta V_t = W_1 - W_2 \tag{6.3}$$

There are virtually unlimited number of choices of gate materials or work function difference. Moreover, the material can be metal or non-metal. As we know, the material work function also depends strongly on the composition as well as on the doping level (for example the doping of polysilicon). For gate materials used in semiconductor device, most work function differences are in the 0 to 2V range and have typical values around 0.1V to 0.6V (for example the differences between Cr and Au, Al and Pt, etc.). In III-V material, the final Schottky barrier is also a strong function of the quality of the interfacial layer and may have a value much less than that predicted by work function.

Fig. 6.2 and Fig. 6.3 show the channel potential profiles for work function difference values of 0.36V and 0.63V, respectively. The two device have same first gate material (M1), gate length(0.8μm), and device structures except the second gate material. Thus the two device have the same V_t = -0.6V, but different work function difference due to the difference in second gate materials. The bias conditions are such that V_{gs} is fixed at - 0.4V and V_{ds} is changed parametrically. Very good screening behaviors are clearly observed in both situations.

Fig. 6.4 shows the comparison of channel electric field distributions for the two cases. The screening behavior improves with larger work function difference. The lower electric field peak near the drain reflects a relatively greater portion of overall electric field being screened. This will obviously improve device behavior against the hot carrier effect which depends on the maximum electric field in the channel. Moreover, as

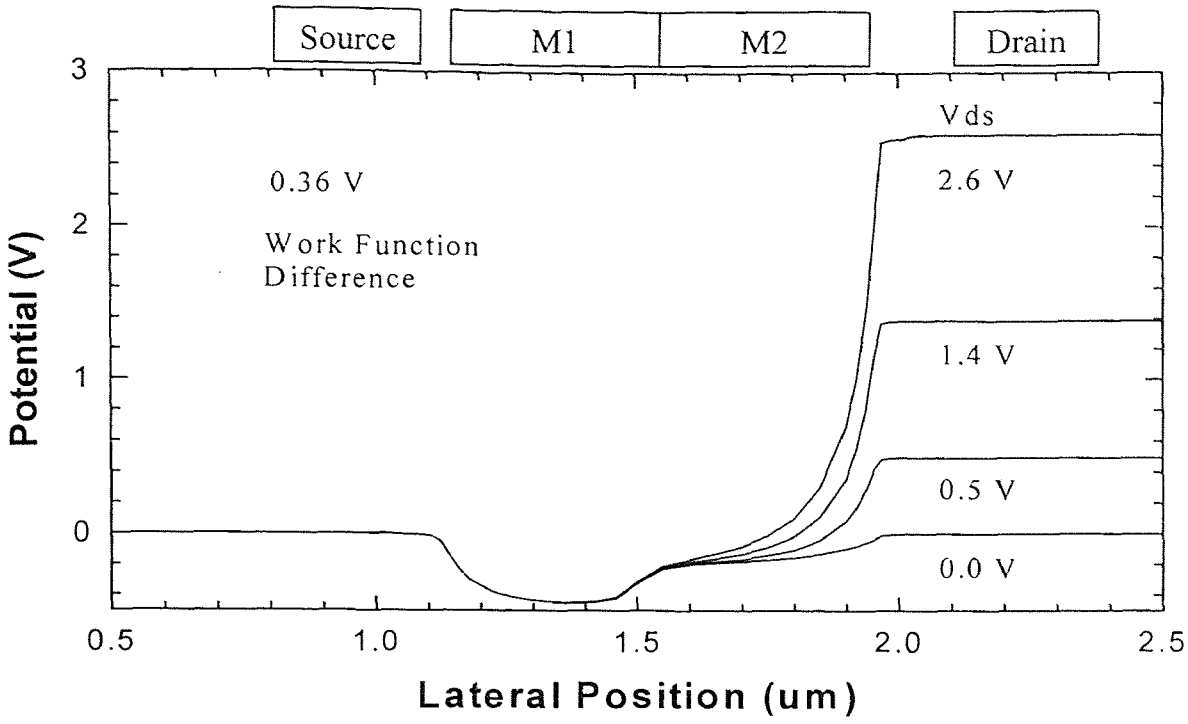


Fig. 6.2 Channel potential profiles of DMG-HFET with work function difference of 0.36 V .

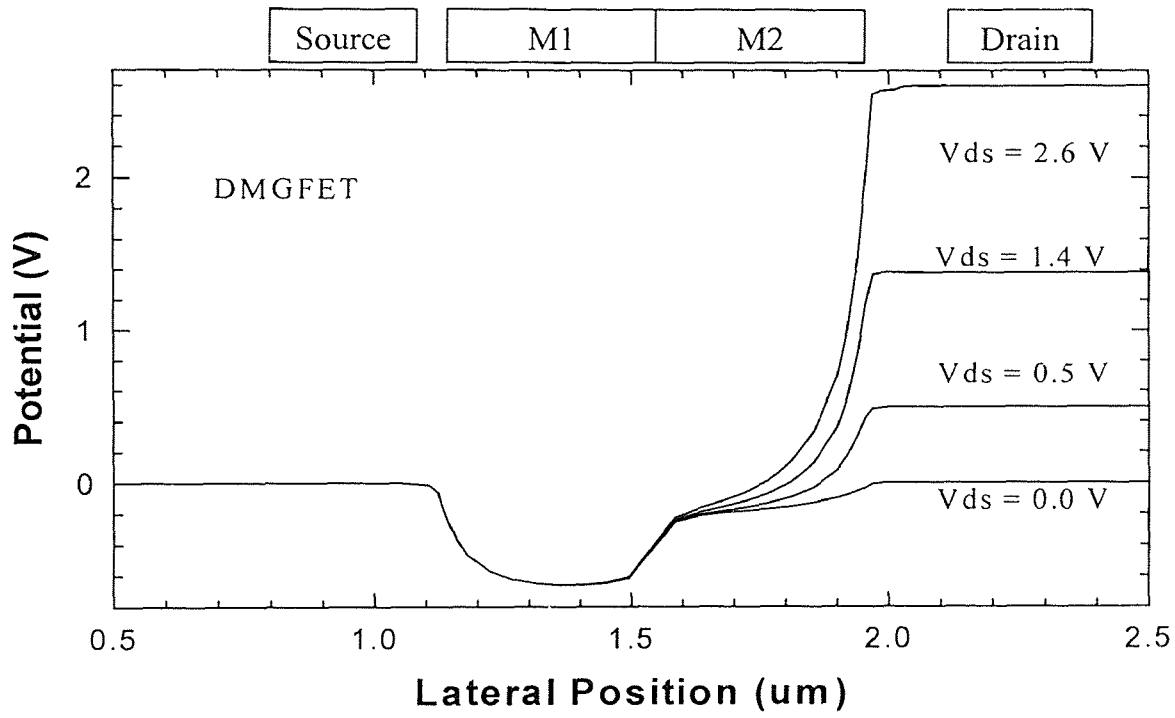


Fig. 6.3 Channel potential profiles of DMG-HFET with work function difference of 0.63 V.

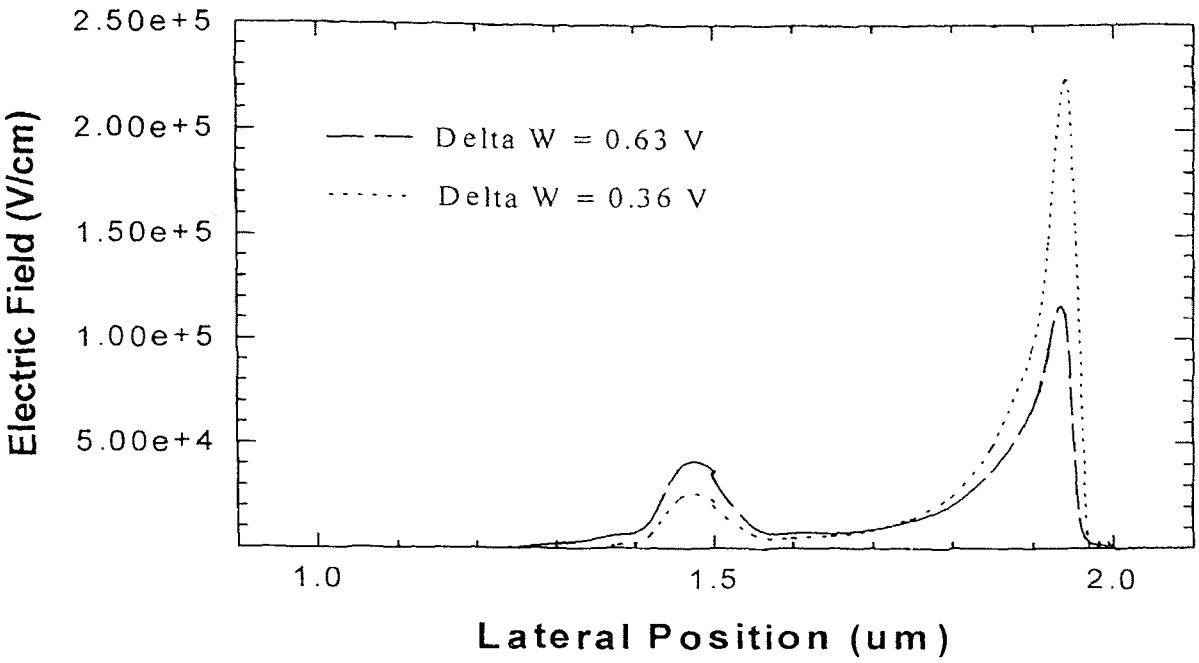


Fig. 6.4 Channel electric field distributions for two typical work function differences ΔW of 0.36V and 0.63V, respectively. The external biases are same.

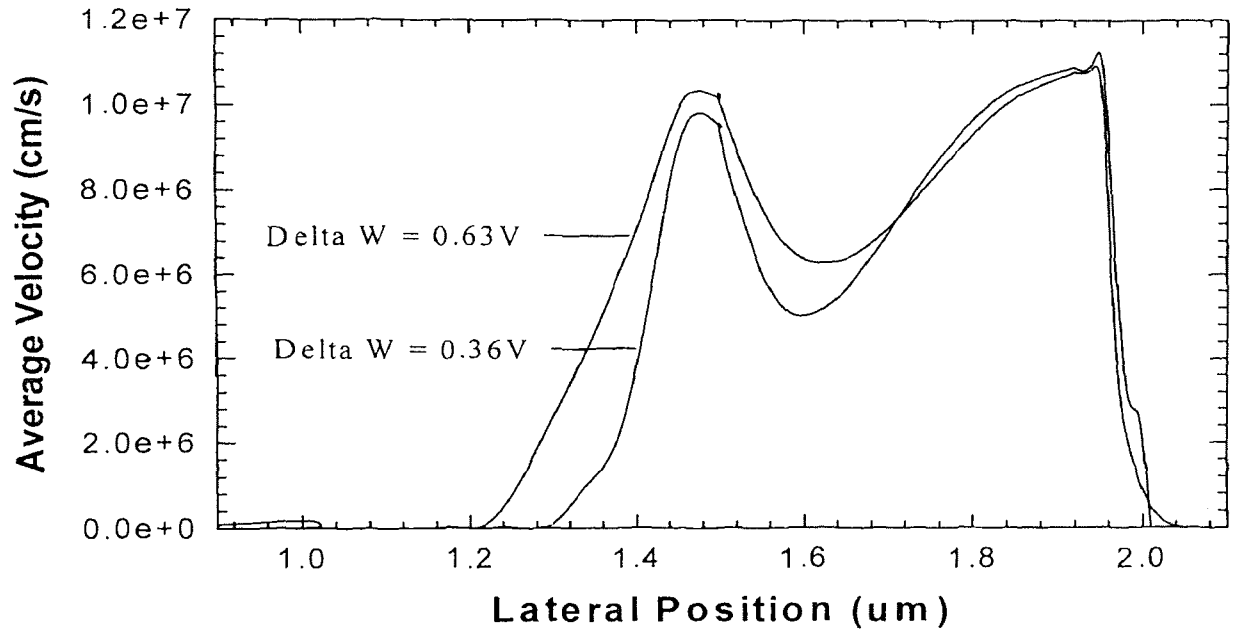


Fig. 6.5 Channel average electron velocity profiles of DMGFET for different work function differences under same biases.

seen in Fig.6.5, due to the greater acceleration field distributed near the source, more velocity enhancement is achieved in device with larger work function difference resulting in higher drain current. Thus, increasing work function difference will improve device performance and overcome short channel effects.

6.4 Design Consideration 3: The Role of Lengths of the Two Gate Materials in DMG-FET

Figure 6.6 is a schematic illustration of the gate structural components of The DMG-HFET, namely: (i) the control gate material with length of L_{m1}, (ii) the screen gate material with length of L_{m2}.

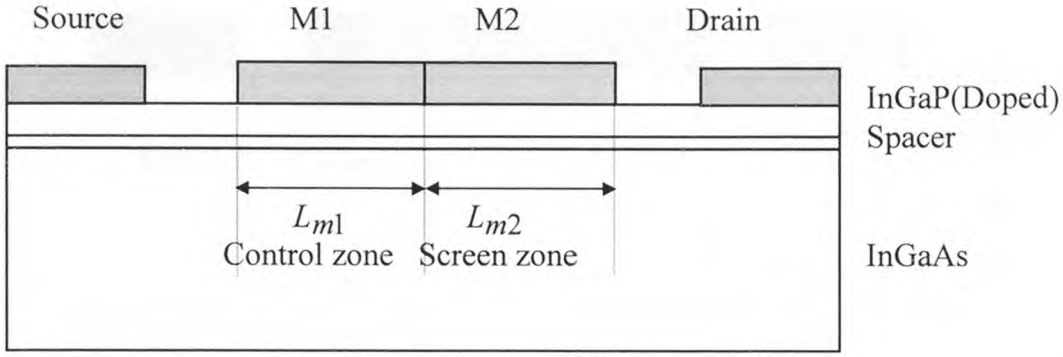


Fig. 6.6 Schematic cross-section of a dual material gate HFET. The two components of the gate region are shown. Other device and structural parameters besides gate length are same as described in Appendix A.

To assess the roles of L_{m1} and L_{m2} on device I-V characteristics, 2-D device simulation of several realistic DMG-HFET was performed using PISCES [84] which was essentially the Poisson and continuity equation solver(see Appendix A). In Fig. 6.7 - 6.9, the channel potential profiles obtained from PISCES simulations is shown for different

L_{m1} and L_{m2} values. For all the 3 cases, $_t$ = -0.6V, $_{gs}$ = 0V, and the source to gate and gate to drain distance unchanged. Fig.6.7 is a DMG-HFET with L_{m1}=L_{m2}= 0.4μm, Fig.6.8 with L_{m2} increased by 0.2μm, and Fig.6.9 with L_{m1} increased by 0.2μm. From Fig.6.10 and Fig.6.11, which show the channel electron velocity profiles corresponding to different L_{m1} and L_{m2} values, it is seen that electrons accelerate within the L_{m1} region, reach saturation velocity near the metallurgical interface between the two materials, and travel with high speed through L_{m2} region due to the high field in this region. From charge control point of view, the linear region is right within region L_{m1} and there is a relatively shallow saturation at the end of L_{m1}. As a consequence, an important

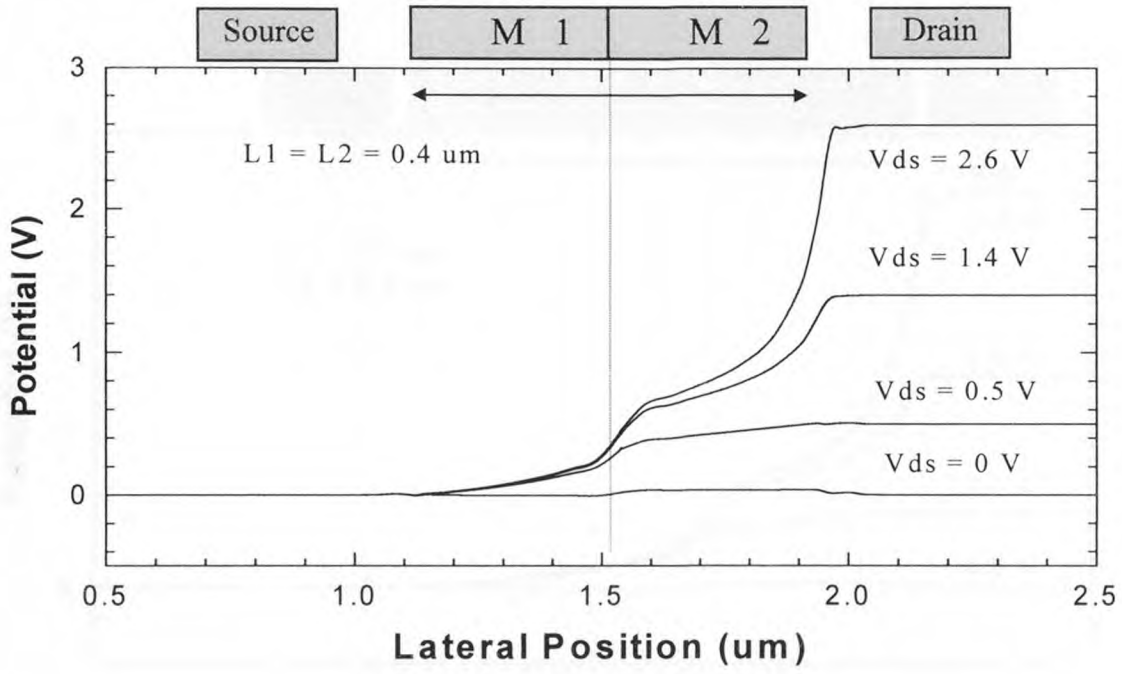


Fig. 6.7 Channel potential profile of DMG-HFET with equal lengths of L_{m1} and L_{m2}. The gate bias is 0V.

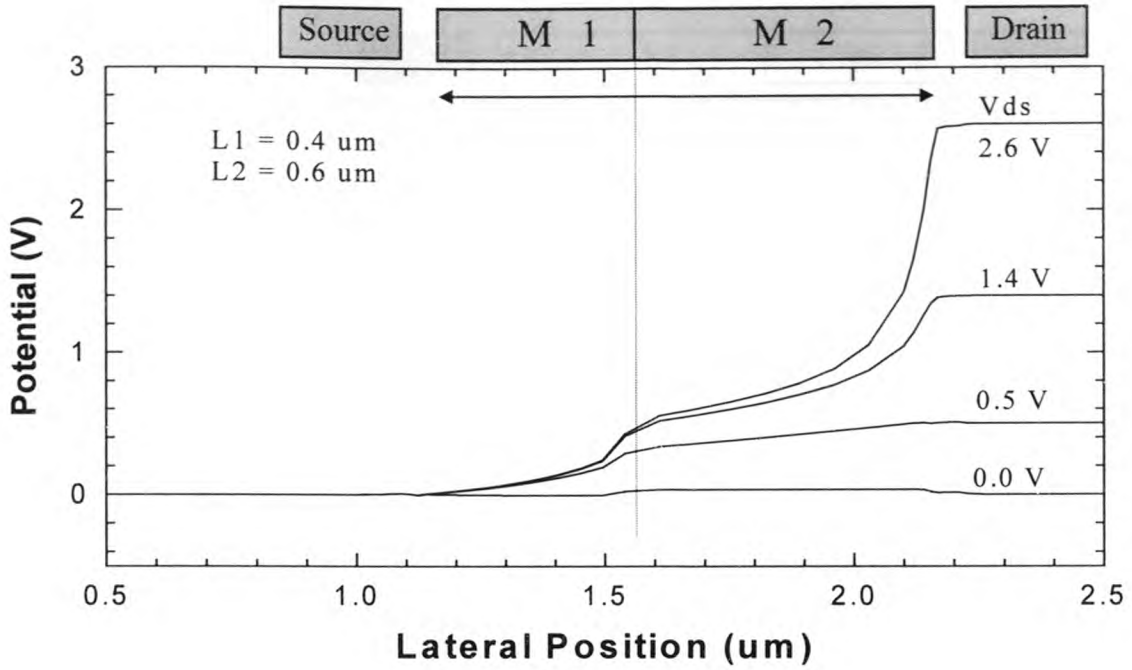


Fig. 6.8 The channel potential profiles of DMG-HFET with longer L_{m2}. The gate bias is 0.0V.

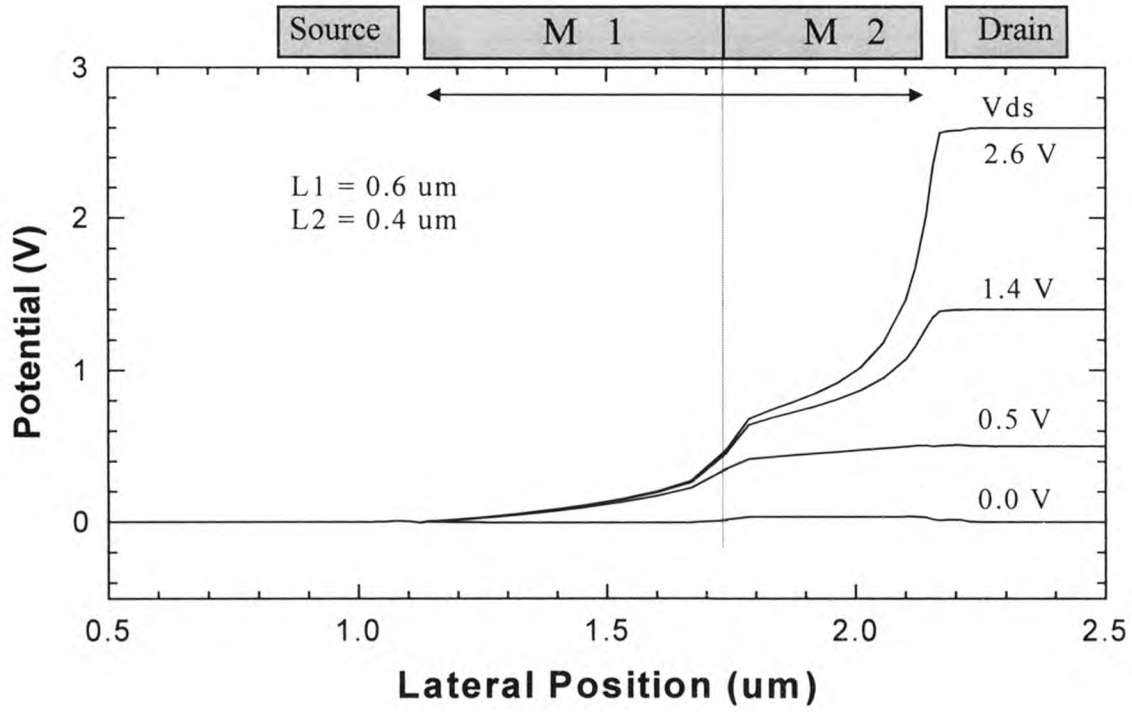


Fig. 6.9 The channel potential profiles of DMG-HFET with longer L_{m1}. The gate bias is 0.0V.

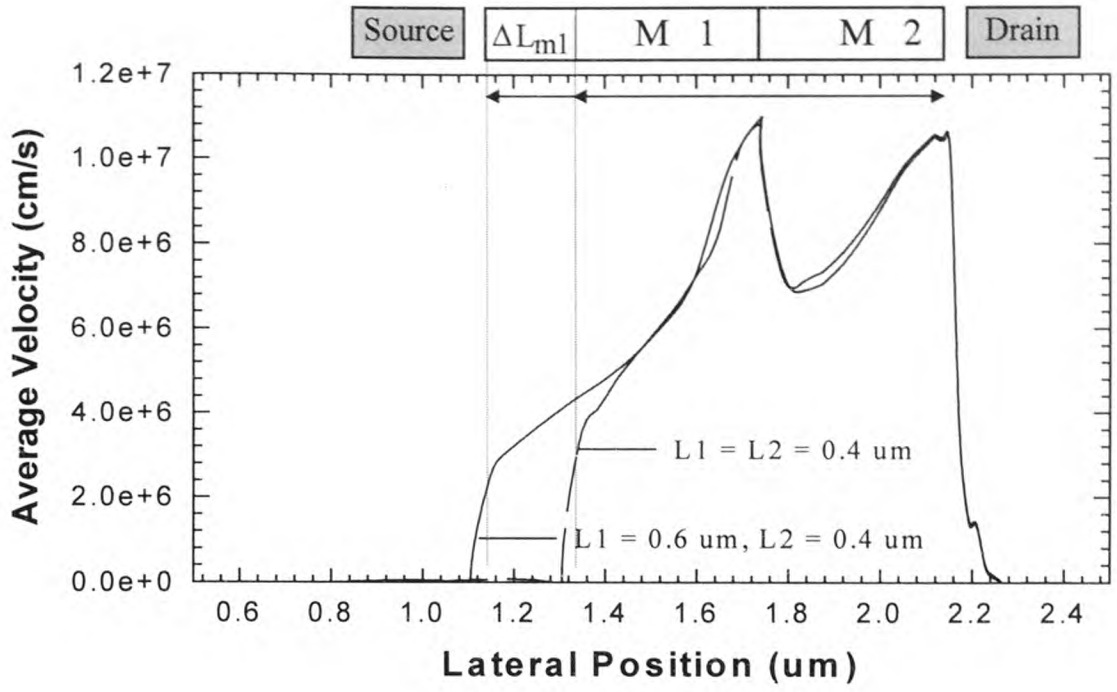


Fig. 6.10 The channel velocity profile changes with the L_{m1} variation for DMG-HFET.

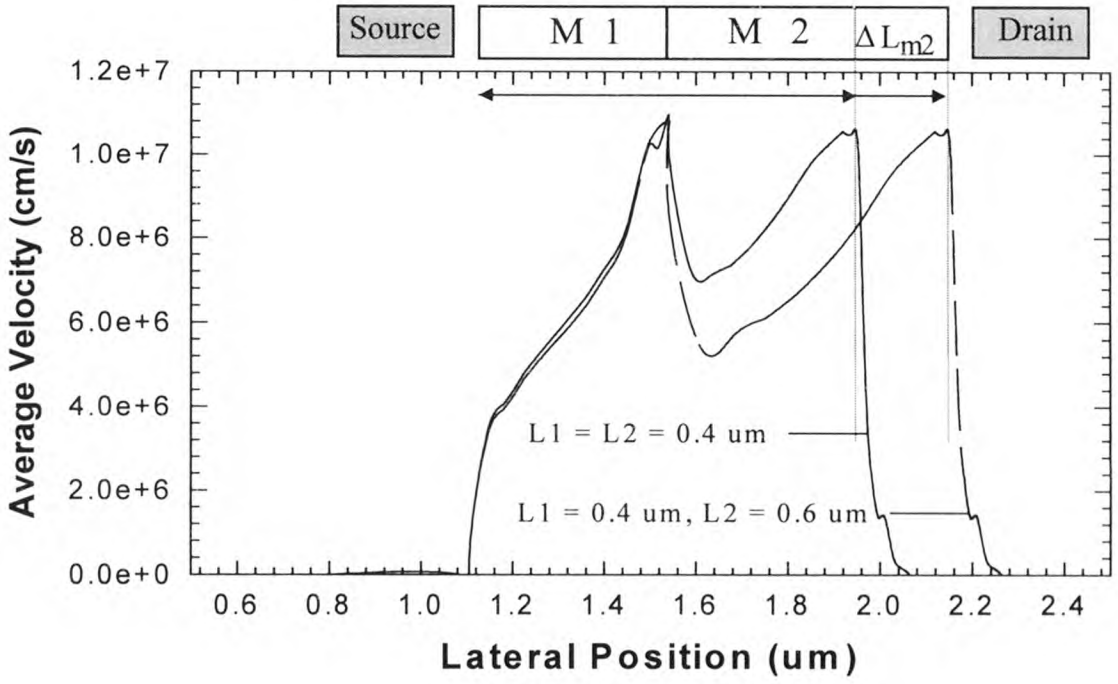


Fig. 6.11 The channel velocity profile changes with the L_{m2} variation in DMG-HFET.

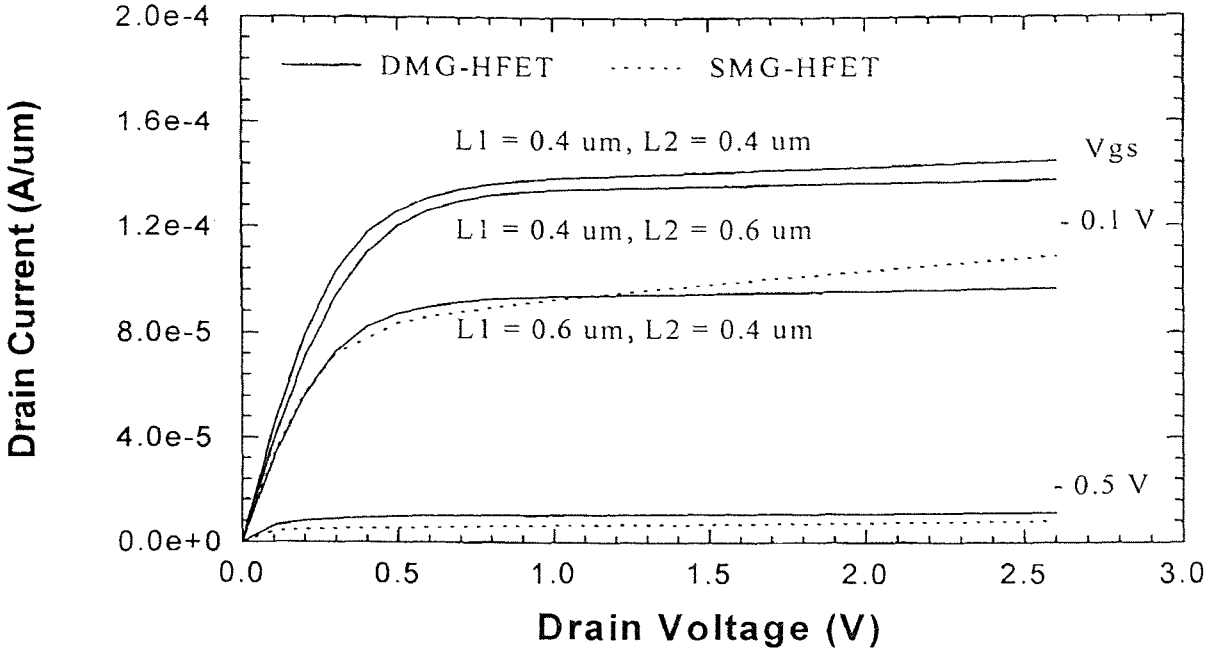


Fig. 6.12 The I-V characteristics of various L_{m1} and L_{m2} values of DMGFET. Conventional SMGFET's curves are also included for comparison.

characteristic for the HFETs' performance, I_{on}, which is defined as I_{ds} under conditions of maximum bias at both the gate and drain electrodes, will increase as the L_{m1} getting smaller.

To get an indication of the drain current for various L_{m1} and L_{m2} values, 2D PISCES simulations are performed for different device structure and sizes. Fig. 5.12 is a plot of I-V curves at V_{gs} = 0 V and -0.4V of DMG-HFET with different L_{m1} and L_{m2} values. 50 % and higher I_{on} increase can be achieved by reducing L_{m1}. This significant driving current increase is due to the fact that the length of charge control linear region is reduced and thus the channel potential changes increase by the scaling down of L_{m1}. From conventional charge control theory of electron transport in semiconductors [88], the current in the linear region of the device is given by:

$$I_{ds} = \frac{W}{L} \mu C_o (V_{gs} - V_t - \frac{V_{dsat}}{2}) V_{dsat} \qquad (6.4)$$

where W is the channel width, L the length of linear region or effective channel length, μ the electron mobility, C_o the channel capacitance, and V_{dsat} is the total bias of the linear region. For a given device structure, due to all the same parameters except the length of linear region L, I_{ds} is simply inversely proportional to L, and hence increases as L or L_{m1} shrinks.

It should be noted that reduction in linear region length L has a greater impact on driving current I_{on} than reduction in saturation region length which is proportional to L_{m2}. Since both are reduced in improved device technology, the result is a significant increase in channel driving current I_{on} which is a key characteristic in modern device technology.

Another important issue is the impact of L_{m1} and L_{m2} on the gate transconductance. This can be seen in Fig. 6.12 that, due to the similar threshold voltages, the drain current or transcondutance increases considerably with the decrease of the controlling length of L_{m1}. L_{m2} has similar impact on transconductance, but less significantly.

We should note here that since L_{m1} is the control zone, the reduction in L_{m1} will reduce the carrier confinement of the channel and lead to more short channel effect. Thus, a balance of drain current and improvement of short channel effects is required.

In short, significant change in current can occur due to the variation of L_{m1} and L_{m2}. Therefore, it would be useful to be able to predict the impacts of these parameter on characteristics of the DMG-FET prior to its fabrication especially deep submicron FETs.

6.5 High Drain Current in DMG-FET

In order to illustrate advantages of the DMG-FET, we simulate I-V characteristics of various FETs including both DMG-HFET and SMG-HFET using PISCES. We assume that all those device have the same structure, doping and geometry(detail in Appendix. A) except the gate structure and composition. For conventional SMG-HFET, the gate is consist of simply one material which is the material of the DMG-HFET near the source. For those DMG-HFETs, the two gate materials and total gate length are fixed, but each device has its own specific sizes of L_{m1} and L_{m2} as we defined in section 6.4.

Fig.6.13 shows the drain I-V characteristics of two devices that one is a 0.8 μm DMG-HFET with gate work function difference of 0.36V and the other is a 0.8 μm SMG-HFET with the same gate material as that near the source in the DMG-HFET. The threshold voltage of both devices was about - 0.6 V. The measured saturation current of DMG-HFET is 27% larger than that of the conventional SMG-HFET device at the gate voltage of - 0.1V. Moreover, at least two other advantages of DMG-HFET over its SMG-HFET counterpart have been seen from the figure: 1) higher transcoductance and 2) lower drain conductance. Noteworthy is that, although it is shown that dual gate FET has also the advantage of low drain conductance, it generally do not reveal high driving current or transconductance due to lack of velocity enhancement effect. Such performance gain is only expected through the use of extremely closed dual gate FET or split gate FET.

To understand the impact of the L_{m1}/L_{m2} or L_{m1}/L ratio on DMG-HFET performance for a fixed gate length L, we have simulated the I-V characteristics of a series of DMG-HFETs with different L_{m1}/L ratio.

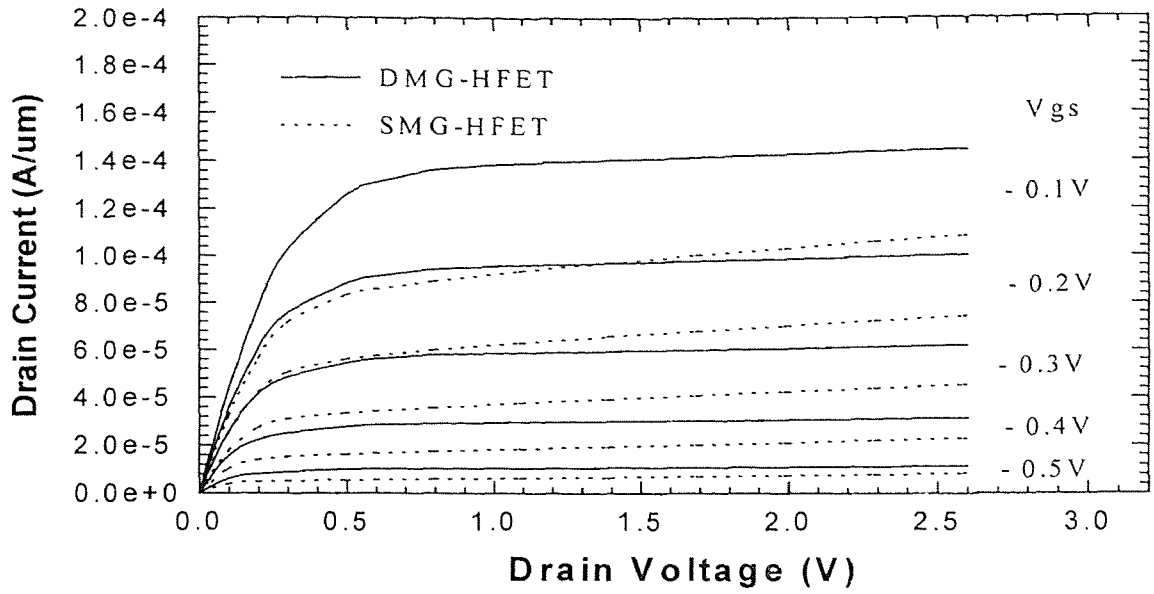


Fig. 6.13 The I-V characteristics of DMG-HFET with $L_{m1} = L_{m2} = 0.4$ μm and SMG-HFET with gate length of 0.8 μm.

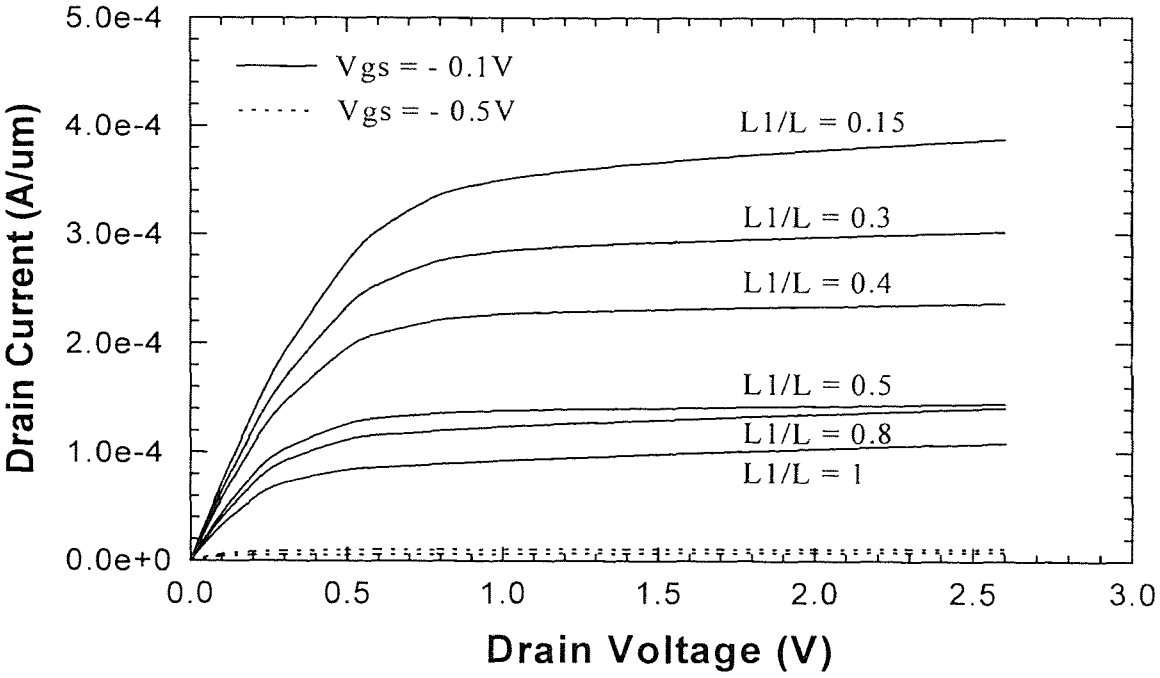


Fig. 6.14 The drain current variation with the change of gate sizes L_{m1} or L_{m2}, where $L_{m1} + L_{m2} = L$ fixed at 0.8 μm. Two gate voltage are used and the threshold voltages are almost same in all the situations.

Fig.6.14 shows the I-V curves of DMG-HFET with different L_{m1}/L ratio or location of the interface of the two gate materials. With V_t=-0.6V, the gate voltages are selected to be -0.1 V and -0.5 V, respectively. It is seen in Fig.6.14 that drain current dramatically increases with the shrinking of the L_{m1} or with the interface of the two gate materials moving closer to the source. This is explainable from our simulation results in section 6.3. Reducing L_{m1} is shortening the electron initial acceleration distance, or the linear region length, which will result in higher drain current and shorter transit time. Although it is considered that the L_{m2} is accordingly increased in those cases, since L_{m2} is high velocity region and has much less impact on drain current than L_{m1}, its drawback in rising total transit time is in contrast with the merits of the decreasing of L_{m1} as mentioned above.

A high drive current I_{on} of the DMG-FET can be achieved by optimizing the position of the gate material interface or L_{m1}/L. I_{on} will be augmented by an amount that depends on the length of L_{m1}. By shrinking the length of L_{m1}, the device can be designed to yield a very large I_{on}, limited highly by the maximum electron velocity. The effect of shrinking L_{m1} can be thought of as being similar in some ways to that of scaling down of gate length of short channel FETs, but the additional L_{m2} of DMG-FET provides superior property of short channel effects suppressing and some possible new ways of gate length control. Reversely, by increasing the length of L_{m1}, the drain current will reduce and eventually reach single gate value when $L_{m1} = L$ or $L_{m1}/L = 1$ as shown in Fig.6.14.

As a final note, we should recognize that in Fig.6.14 all the devices have almost same threshold voltages, therefore, the drain current is proportional to the corresponding

transconductance and similar trend and phenomena also occur to transcoductance. In other words, the reduction of L_{m1} also yields higher transconductance.

6.6 Suppressed Short Channel Effects in DMG-FET

The exciting feature of DMG-FET, due to its screening effect as we mentioned in the previous chapter, is its ability to effectively suppressing short channel effects, such as channel length modulation, drain induced barrier lowering (DIBL) and hot carrier damage. To demonstrate the effects, single gate FET counterpart with same physical and structural parameters except gate structure is employed. The detail of them is shown in the example of Appendix A.

We note that the degree of short channel effects discussed below is also a strong function of device aspect ratio. Thus different FETs have different onset of short channel effects. The devices simulated in this section have the same channel length of 0.8μm and aspect ratio of about 30 which have normal HFET values. It also shoud be noted that the PISCES simulator we used is not perfect for HFETs especially for deep submicron and small aspect ratio HFETs, but neverthless predicts trends of the device performance when the geometrical and physical parameters are varied.

6.6.1 Channel Length Modulation

For the conventional single gate FET, as the channel length is reduced, its departure from long-channel behavior is manifested by the drain current increasing with drain bias. This departure, one of the short channel effects, arises as the result of channel length modulation due to the drain bias. For a given FET, with the channel length reduction, the shift of the depleted region width after pinch off now becomes comparable to the channel

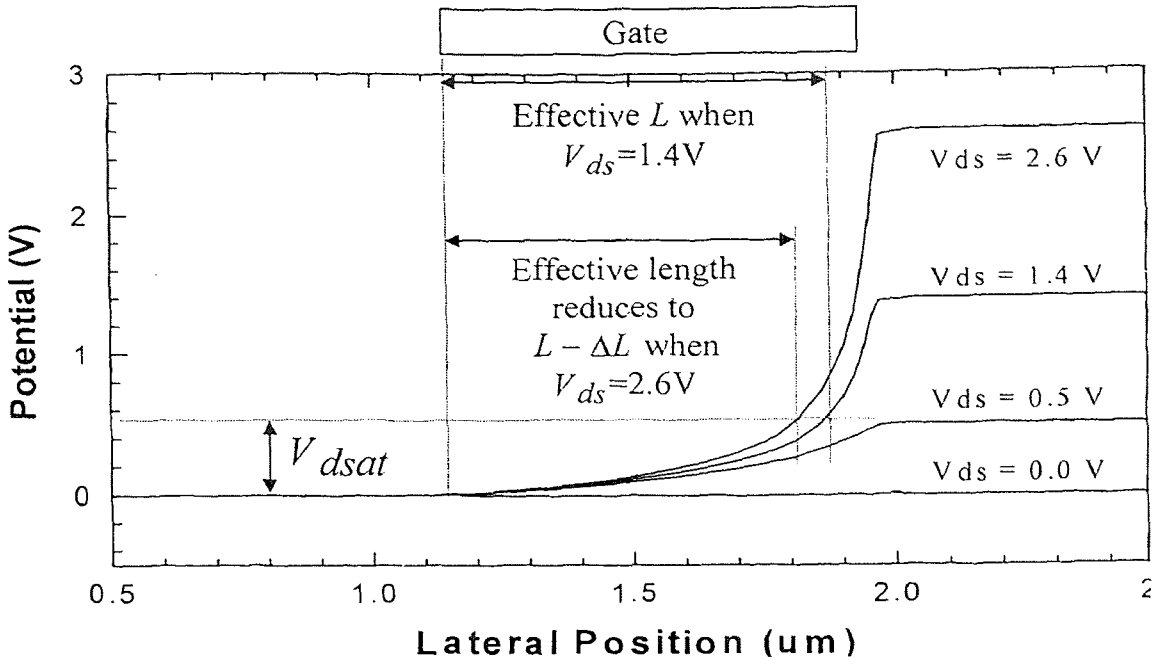


Fig. 6.15 Channel potential distribution of SMG-HFET. The effective linear region length L is seen continuously decreases with the drain bias increase.

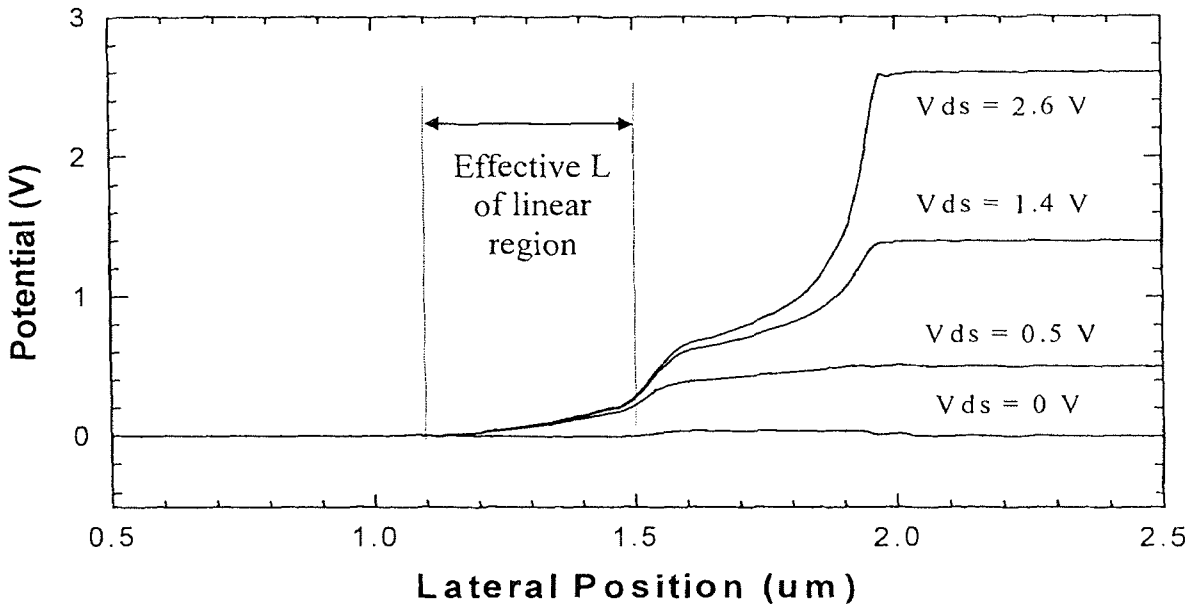


Fig. 6.16 Channel potential distribution of DMG-HFET. The effective linear region length L is seen nearly remain unchanged with the drain bias over 0.5V.

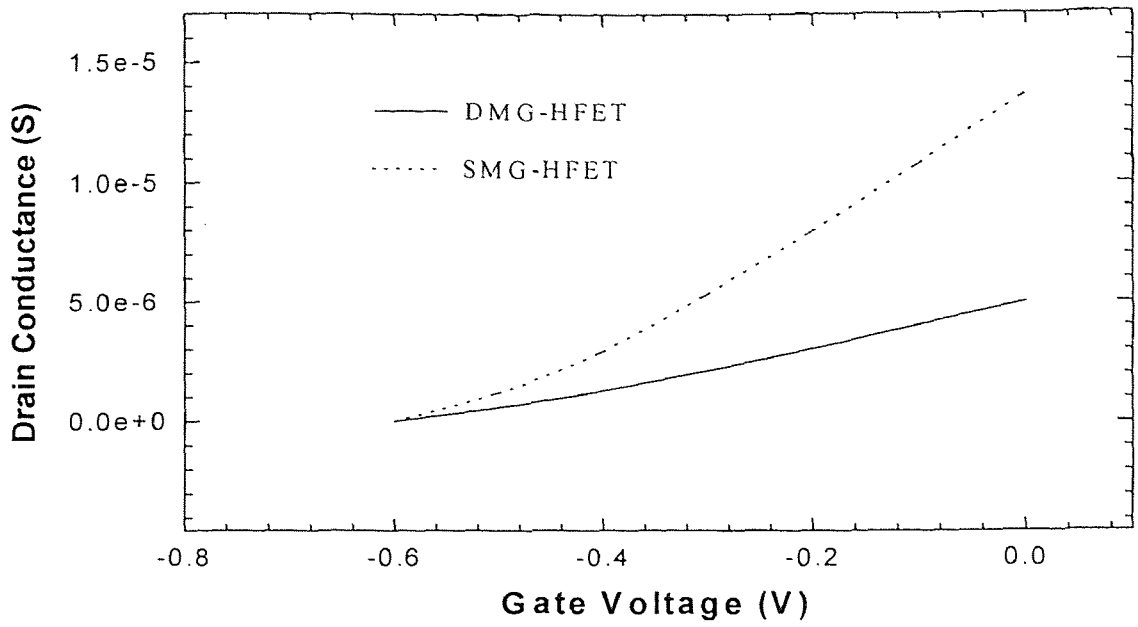


Fig. 6.17 The drain conductance behaviors of both DMG-HFET and SMG-HFET.

length L. In order to simplify the analysis of this effect, first order drain current equation is only used for the purpose of analysis. The length L in this equation for I_{ds} now depends on the shift of depletion region ΔL due to the change of V_{ds}. It can be seen from the 2D PISCES numerical result in Fig.6.15 that the depletion region is extended toward the source by large drain bias. Thus the length of L now must be substituted by $L - \Delta L$ in the analysis current equation (6.4) which is rewritten below as a convenience:

$$I_{ds} = \frac{W}{L} \mu C_o (V_{gs} - V_t - \frac{V_{dsat}}{2}) V_{dsat} \qquad (6.4)$$

Since the saturation drain voltage V_{dsat} is independent of the drain bias, this channel length modulation results in the rise of drain current after saturation in I-V curve, or the increase of drain conductance.

For the DMG-FET, however, the effect of drain bias on channel length modulation is effectively eliminated, because the linear region potential distribution is

screened from drain bias after saturation. As Fig.5.16 illustrates, the high field or depletion region near the drain no longer expands further to the linear region. For a given DMG-FET, the linear region is virtually independent to the saturation region drain voltage, leading to a decrease of drain conductance. Fig.6.17 shows a comparison of drain conductance behaviors of DMG-FET and SMG-FET. The improvement of drain conductance for DMG-FET is apparent.

6.6.2 Drain Induced Barrier Lowering

In the long channel FETs, we assume that in its subthreshold operation the entire V_{ds} is dropped across the drain depletion region. Thus, the channel potential in the rest of the channel region is essentially independent of V_{ds} and depends only on the gate bias. This also implies channel potential minimum $\varphi_{\min}$ is independent of V_{ds}. However, this assumption breaks down in the case of short channel FET. As the channel is reduced to be less than 2 μm, especially in submicron, deep submicron region, the $\varphi_{\min}$ or the potential energy barrier lowers considerably.

This drain induced barrier lowering (DIBL) can be empirically characterized by measuring and plotting a set of log I_{ds} versus V_{gs} curves with increasing values V_{ds} as the parameter. A quantitative estimate of DIBL can be extracted from the shift in gate voltage ΔV_{gs} at a fixed drain current as the drain voltage is changed. The shift in V_{gs} is normally expressed in normalized form as $\Delta V_{gs} / \Delta V_{ds}$. As shown in Fig.6.18, the value of $\Delta V_{gs} / \Delta V_{ds}$ for DMG-HFET is ~26 mV/V. $\Delta V_{gs} / \Delta V_{ds}$ for conventional SMG-HFET is extracted from the curves in Fig.6.19 and has a much higher value of ~75mV/V, exhibiting a more severe DIBL effect.

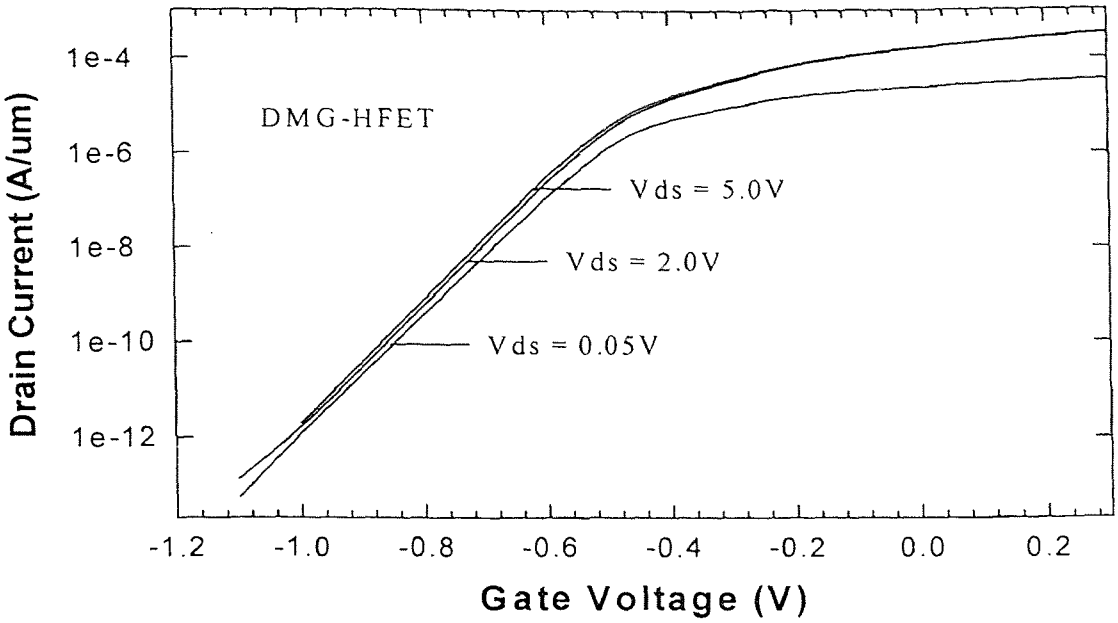


Fig. 6.18 Plot of log I_{ds} versus V_{gs} for DMG-HFET operated below threshold, with V_{ds} as the parameter. The value of $\Delta V_{gs} / \Delta V_{ds}$ for a fixed value of I_{ds} (e.g., 1×10^{-7} A/μm) is used to characterize the DIBL.

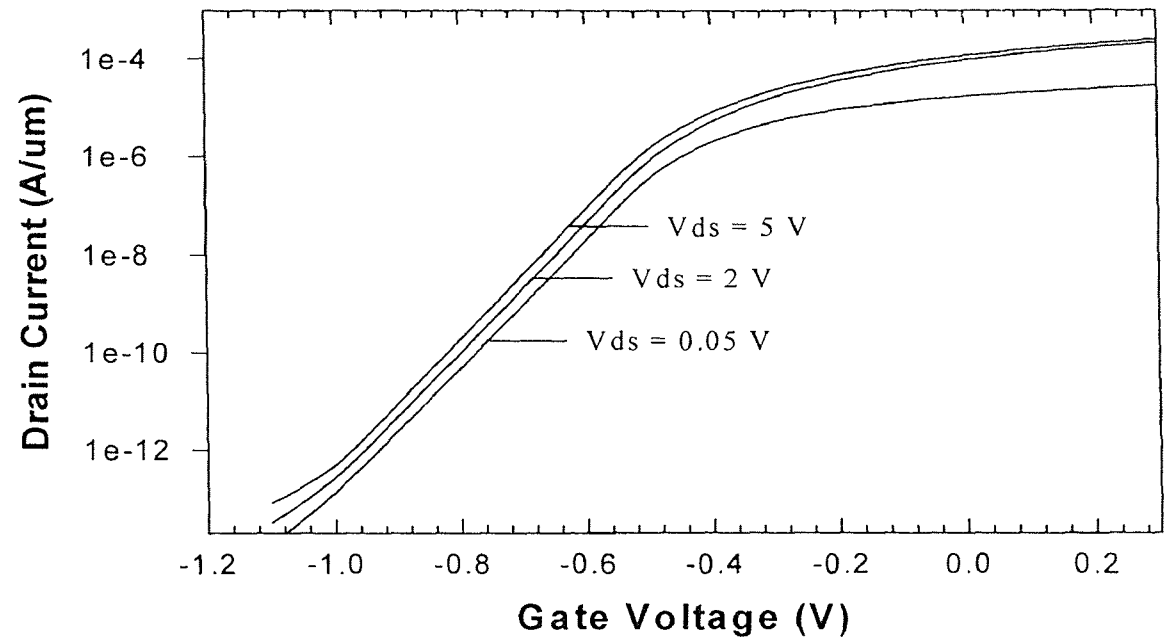


Fig. 6.19 Plot of log I_{ds} versus V_{gs} for conventional SMG-HFET operated below threshold, with V_{ds} as the parameter. $\Delta V_{gs} / \Delta V_{ds}$ value is also used.

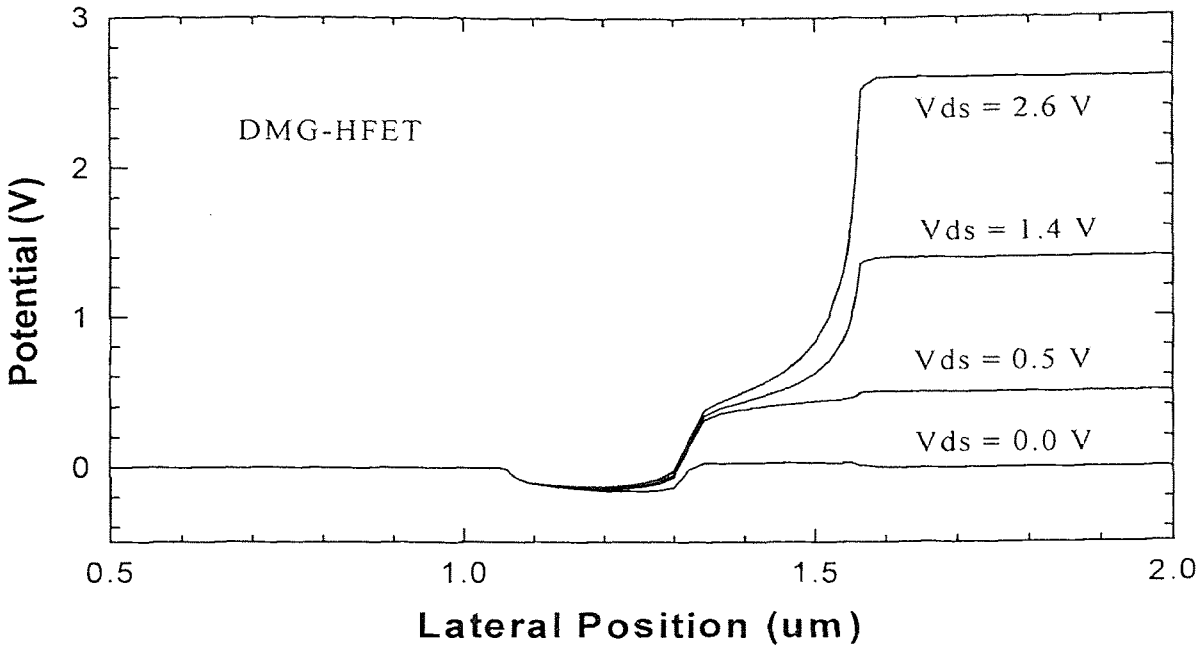


Fig. 6.20 The calculated channel potential of DMG-HFET for different drain biases.

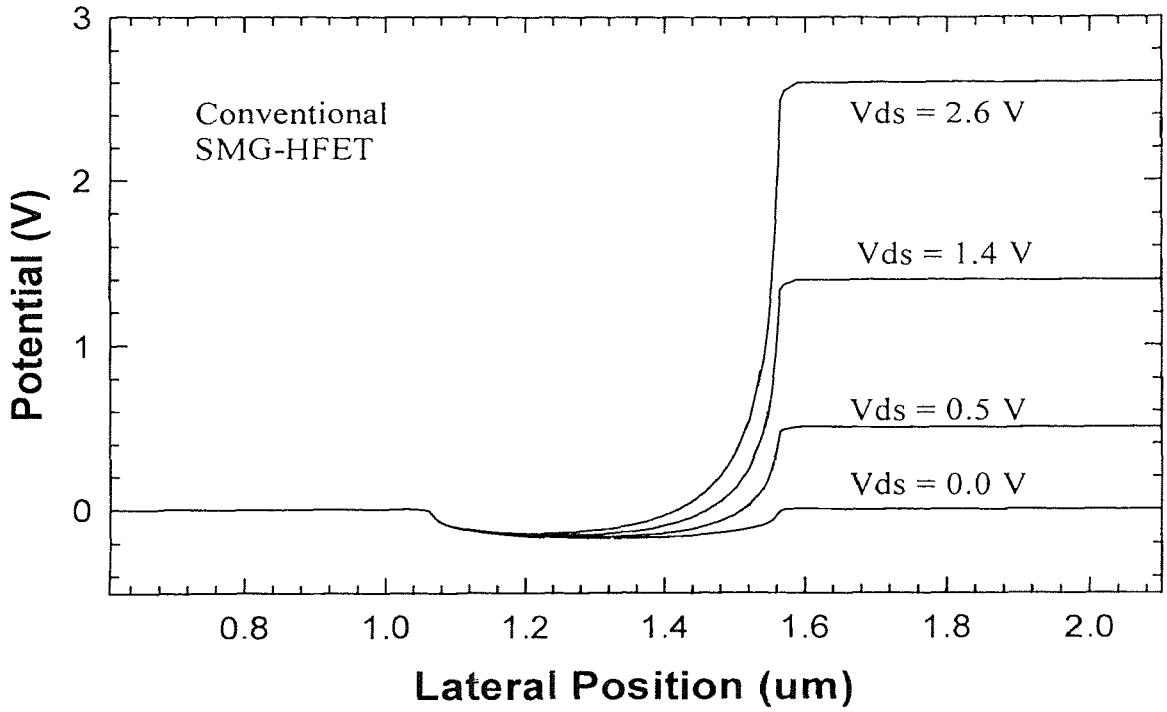


Fig. 6.21 The calculated channel potential of SMG-HFET for different drain biases.

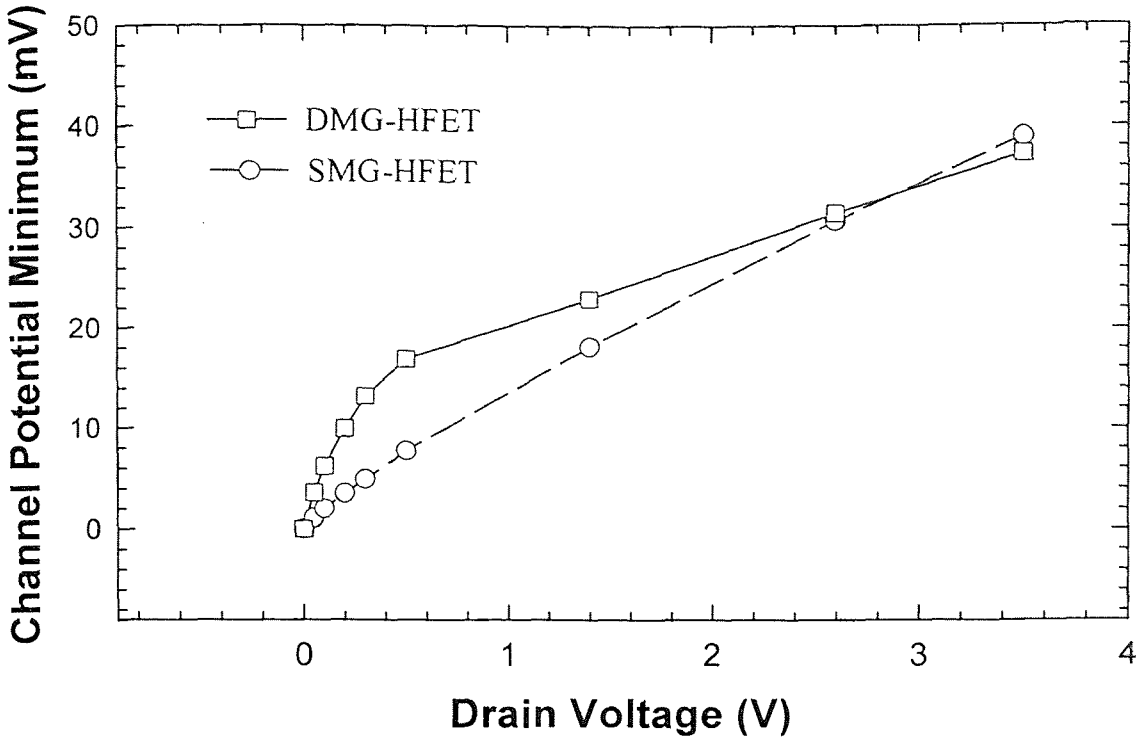


Fig. 6.22 Variation of channel potential minimum $\varphi_{\min}$ or potential energy barrier height versus V_{ds} for DMG-FET and SMG-FET with same channel length.

The results in Fig.6.18 and Fig.6.19 are accomplished by using a 2-D device simulator, PISCES. Such an entirely numerical approach, however, does not offer quantitative insight into the phenomenon of DIBL, nor does it provide detailed information on trends in the device behavior as the terminal voltages are varied. Therefore, a popular, hybrid approach that first employs a numerical method to calculate channel potential and then uses this solution in an analytical expression of I_{ds} to understand the device physics has been implemented.

The analytical equation for I_{ds} in subthreshold regime can be expressed as:

$$I_{ds} = A \exp\left[\frac{q}{kT}(\varphi_{\min} - V_s)\right]\left\{1 - \exp\left(\frac{-qV_{ds}}{kT}\right)\right\} \qquad (6.2)$$

where A is a constant related to the device structure and material parameters and V_S is the source potential. When $V_{ds} \geq 0.1$ V (the operating condition of practical interest), Equation (6.2) reduces to the following expression:

$$I_{ds} = A \exp\left[\frac{q}{kT}(\varphi_{\min} - V_S)\right] \tag{6.3}$$

Thus the variation of I_{ds} or DIBL increases exponentially with the change of $\varphi_{\min}$.

In Fig.6.20 and Fig.6.21, we examine potentials along the channel for V_{ds} stepped from 0 V to 2.6 V for DMG-HFET and SMG-HFET, respectively. The corresponding behaviors of the channel potential minimum $\varphi_{\min}$ are extracted and plotted in Fig.6.22. We note that, for conventional SMG-FETs, $\varphi_{\min}$ simply rises linearly with V_{ds}, but for DMG-FET, $\varphi_{\min}$ initially rises rapidly and then increases slowly as $\varphi_{\min}$ is increased. This indicates that the $\varphi_{\min}$ behavior for DMG-FET is actually due to some other phenomenon. In conventional SMG-FET, the continuous rising of $\varphi_{\min}$ can be explained as the continuous extension of depletion region due to V_{ds}. In DMG-FET, however, the rapid increase of $\varphi_{\min}$ at very low V_{ds} is due to the set-up of the potential distribution in the control zone near the source, afterwards, further drain bias is dropped in the screen zone or under gate material near the drain and the change of $\varphi_{\min}$ is slowed down due to the screening effect as show in Fig.6.20. Comparing the behavior of the rise of $\varphi_{\min}$ of a DMG-FET with that of a SMG-FET as shown in Fig.6.22, the $\Delta\varphi_{\min} / \Delta V_{ds}$ value or $\Delta V_{gs} / \Delta V_{ds}$ value ($\varphi_{\min} \propto V_{gs}$), or so called DIBL rate, of DMG-FET is only 60 % of that of conventional SMG-FET in the saturation regime.

6.6.3 Hot Carrier Effects

The hot carrier effect is caused by the high electric field in the channel. As the drain bias is increased to saturation regime, electric field increases rapidly at the region near the drain. When the maximum field is increased further, carrier multiplication near the drain occurs, leading to substrate current and parasitic bipolar transistor action. High fields also cause hot carrier injection into the gate region, leading to threshold voltage shift and transconductance degradation. Because the high electric field near the drain complicate device operation and degrade device performance, the maximum electric field should be minimized.

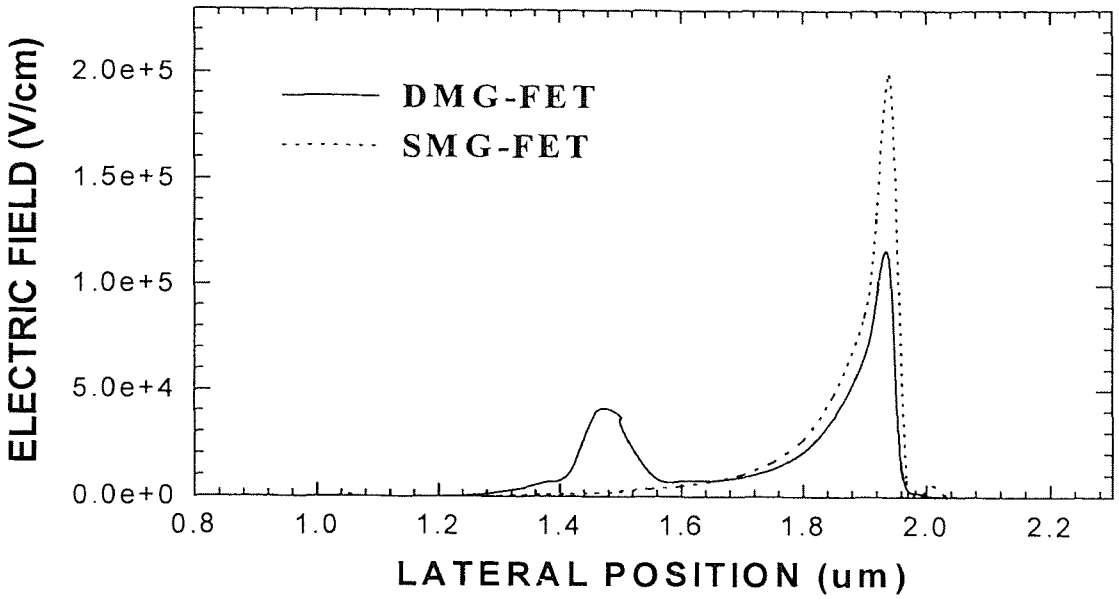


Fig. 6.23 The longitudinal channel electric field behavior of DMG-HFET and SMG-HFET in saturation. (V_{gs} = -0.4 V and V_{ds} = 1.4 V).

The longitudinal channel fields for both DMG-FET and SMG-FET as calculated from PISCES simulation are plotted in Fig.6.23. The numerical simulations predict that

in both cases, electric fields exhibit a near exponential dependent rise towards the drain, in addition, for DMG-FET, however, another relatively low electric field peak exists near the interface of the two gate materials, causing a dramatic reduction in maximum electric field near the drain. Because hot carrier effects are extremely sensitive to the magnitude of the maximum channel field, it can be concluded that the DMG-FET can effectively suppress the hot carrier effects. Consequently, highly reliable behaviors of the DMG-FET are predicted.

6.7 Comparison Between a 1 μm (0.5 μm + 0.5 μm) gate DMG-FET and a 0.5 μm gate SMG-FET

The advantages of DMG-FET structure comes from the added functionalities obtained by integrating the two laterally contacting gate materials. As we have demonstrated in previous discussions, compared to the conventional (single material gate) SMG-FET, a DMG-FET of the same total gate length provides the higher driving current, higher transconductance, lower drain conductance and much reduced short channel effects.

It is well know that in a conventional SMG-FET shrinking the gate length can also enhance the performance of the device. Therefore, it is of particular interest to compare a half micron SMG-FET with a one micron DMG-FET which is composed of two half micron gate materials.

Fig.6.24 shows the drain I-V characteristics of a 0.5 μm gate SMG-HFET and a 1 μm (0.5 μm + 0.5 μm) gate DMG-HFET. For the DMG-HFET, it shows very good saturation characteristics, but for the SMG-HFET, very high output conductance caused by severe short channel effects is observed. The dependences of transconductance for both DMG-HFET and SMG-HFET with drain biased at 1.5 V are shown in Fig.6.25. The

two transconductamces are comparable, with the DMG having values slightly lower than those of the SMG.

As predicted, the DMG-HFET yields significantly lower drain conductance, as shown in Fig. 6.26, by effectively eliminating the short channel effect such as channel modulation effect. Substantial reduction in drain conductance is seen in the figure as compared with the 0.5 μm gate SMG-HFET. It should be noted that both DMG and SMG structure simulated have the same channel depth. The 0.5 μm gate SMG-HFET, therefore, has lower aspect ratio than practical device. That is why higher than normal output conductance for SMG has been obtained here.

The DMG structure introduces an even more significant improvement in suppressing the drain induced barrier lowering (DIBL). This is illustrated in Fig.6.27. The DIBL rate or $\Delta \varphi_{\min} / \Delta V_{ds}$ as low as 0.75 mV/V has been extracted for the DMG-FET

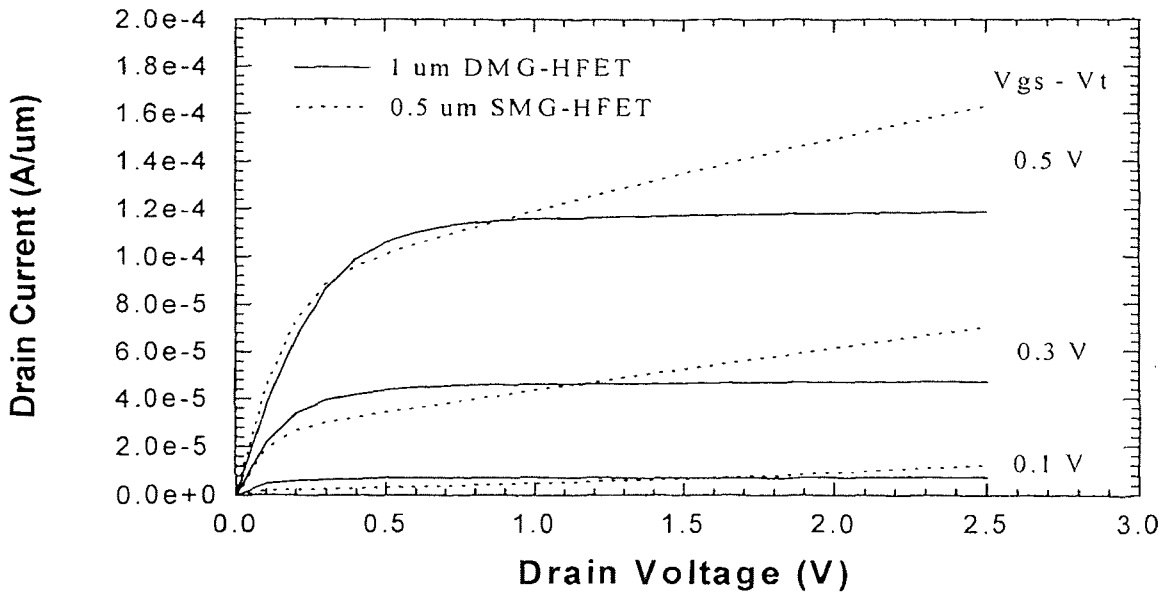


Fig. 6.24 I-V characteristics of a 0.5 μm gate SMG-HFET and a 1 μm (0.5 μm + 0.5 μm) gate DMG-HFET.

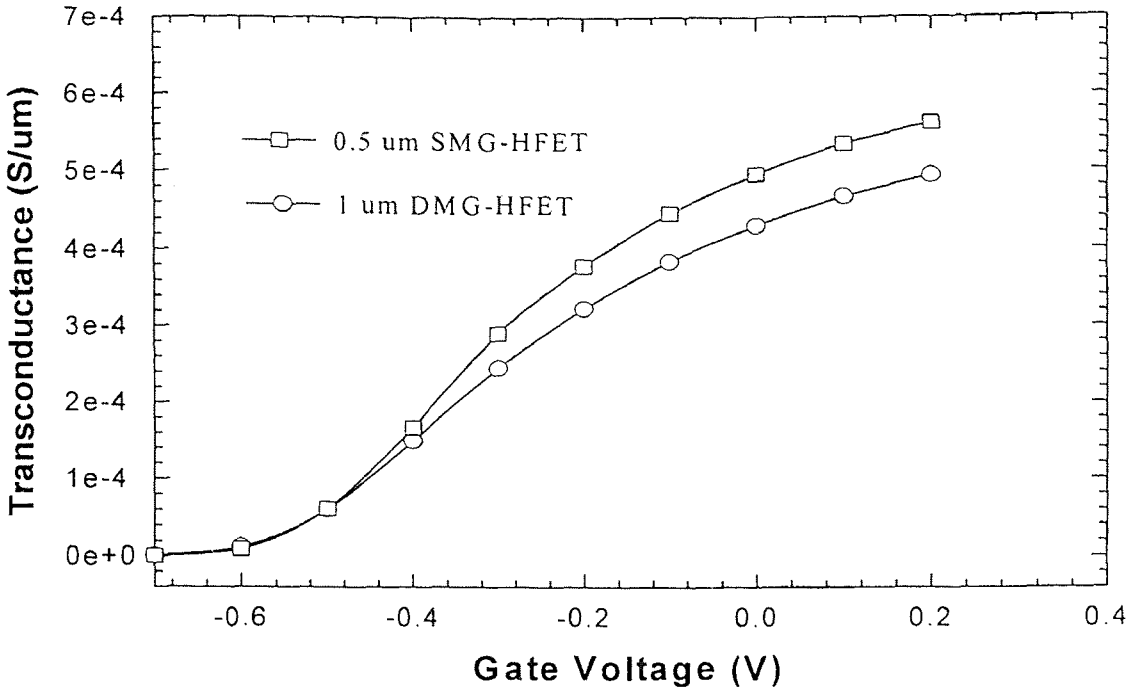


Fig. 6.25 The transconductance behaviors of the 0.5 μm gate SMG-HFET and 1 μm (0.5 μm + 0.5 μm) gate DMG-HFET.

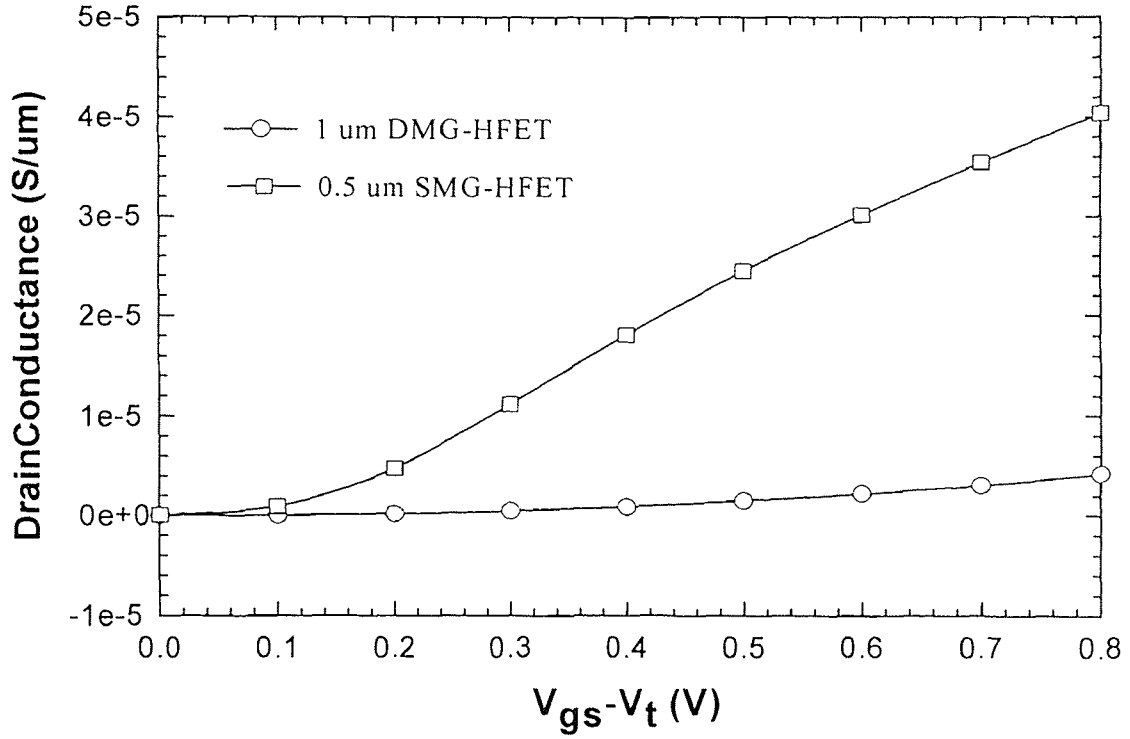


Fig. 6.26 Drain conductance behaviors of the two HFETs.

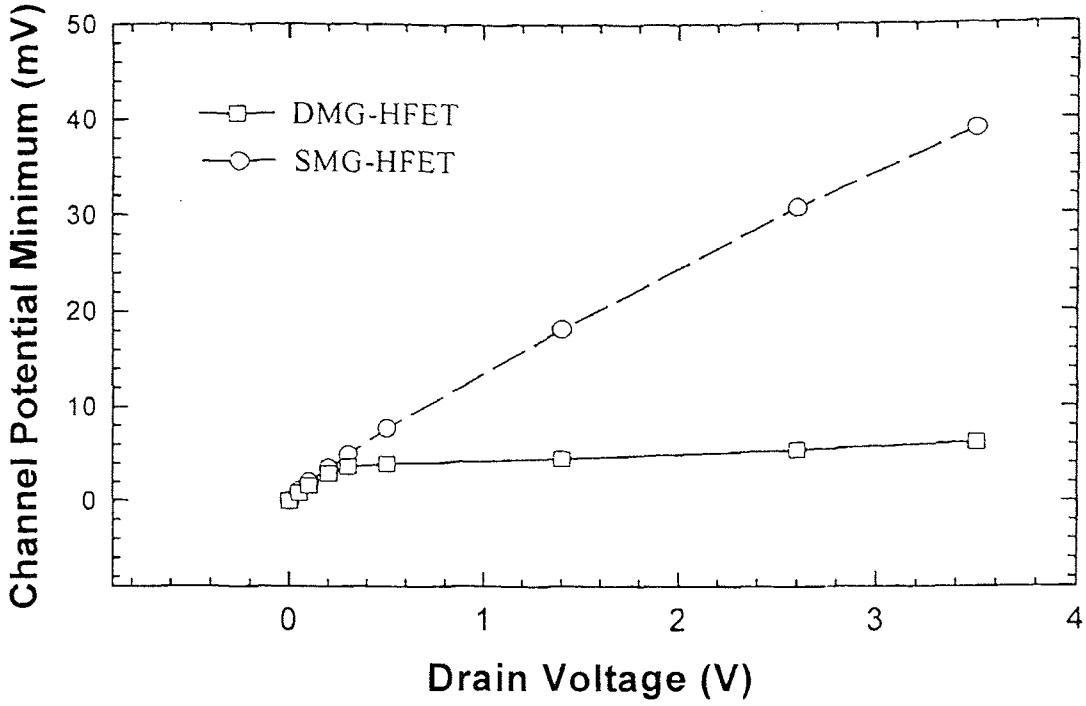


Fig. 6.27 Comparison of the channel potential minimum versus drain bias between a 0.5 μm gate SMG-HFET and a 1 μm (0.5 μm + 0.5 μm) gate DMG-HFET.

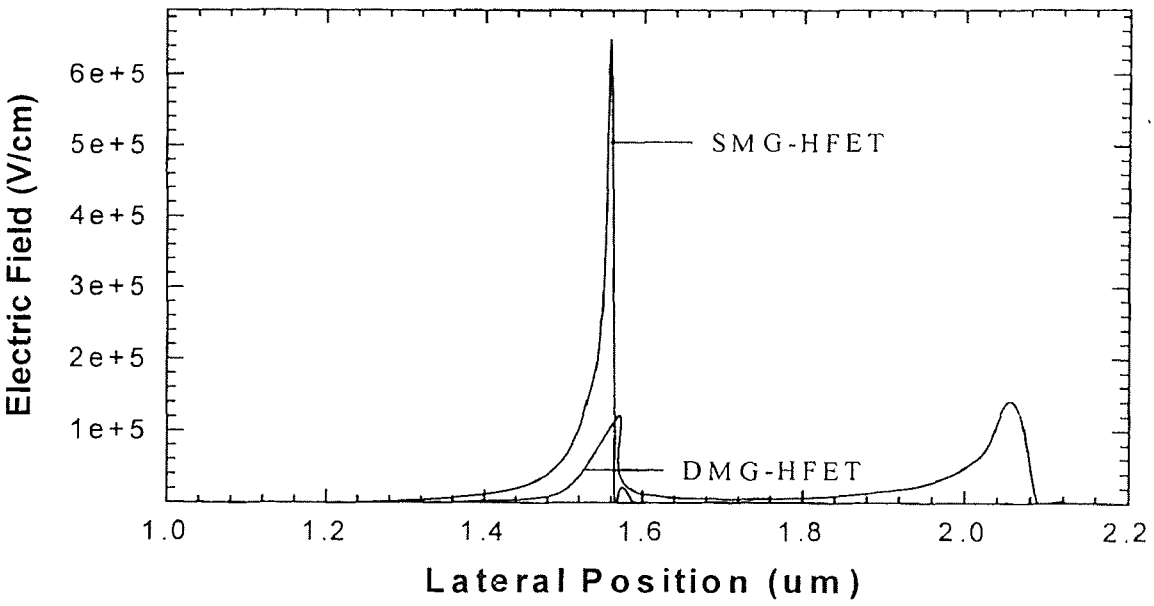


Fig. 6.28 Longitudinal channel electric field distributions for a 0.5 μm gate SMG-HFET and a 1 μm (0.5 μm + 0.5 μm) gate DMG-HFET.

in the saturation region, comparing to the value of 10.45 mV/V obtained for the SMG-FET, which indicates that the DIBL rate of the DMG-FET is over 13 times better than that of the SMG-FET.

The DMG-FET has another important advantage in suppressing hot carrier effects. The channel longitudinal electric fields are calculated and depicted in Fig.5.28 for both the 0.5 μm gate SMG-HFET and 1 μm (0.5 μm + 0.5 μm) gate DMG-HFET. Maximum channel electric fields of 6.5×10^5 V/cm for SMG-FET and 1.4×10^5 V/cm for DMG-FET can be extracted from the curves. Over 78 % reduction in maximum electric field has been achieved for DMG-HFET as compared to the SMG-HFET counterpart.

In short, the 1 μm (0.5 μm + 0.5 μm) gate DMG-HFET has nearly same drive current as compared to 0.5 μm gate SMG-HFET, but exhibits significantly suppressed short channel effects. 1 μm (0.5 μm + 0.5 μm) gate DMG-HFET is thus superior over the 0.5 μm gate SMG-HFET counterpart.

6.8 Summary

Using PISCES 2ET 2-D numerical device simulations, it was shown in this chapter that the two gate materials in DMG-FET have played different roles. The length and work function of the first portion of the gate, which is near the source, are the dominant parameters to determine the channel current and device threshold voltage, whereas the work function difference and length of the second portion of the gate determine to what degree the short channel effects can be suppressed.

A systematic simulations and analysis of the characteristics and effects of DMG-FET were presented in detail in this chapter, which emphasized the physical in-sight of

the following major issues for better understanding and design of the novel device structure:

- Threshold Voltage
- Length of two gate materials
- Work function difference
- Saturation current I_{on} and transconductance
- Drain conductance
- Drain Induced Barrier Lowering
- Hot carrier effect

Excellent I-V characteristics and suppressed short channel effects were demonstrated.

CHAPTER 7

DMG-HFET FABRICATION AND EXPERIMENTAL RESULTS

7.1 Introduction

Real fabrication is the critical step in the procedure of developing novel device structures. The effectiveness of the experimental approach of the new semiconductor device structure is intimately related to the degree in which we understand its physical origin. In the previous chapters, with the help of various numerical device simulations, extensive efforts have been devoted to the physical in-sight of the device. In this chapter we are concerned primarily with the experimental issues. The concepts and principles developed in previous chapters are adopted in directing the experimental efforts.

Because the proposed structure needs only modifications in the gate or channel, which all the FETs have in common, the new device structure is virtually good for all the family of the field effect transistors. Therefore, we can use any member of the general FETs as a vehicle to demonstrate the properties of the novel structure. To this end, Heterostructure Field Effect Transistors (HFETs) have been employed as a vehicle throughout the thesis.

In this chapter, we investigate the experimental DMG-FET using pseudomophic InGaP/InGaAs HFET as a vehicle. In order to realize the proposed DMG structure, a simple and realistic method for forming a gate with two laterally contacting metals is required. For the short channel region (1 μm or less), however, it becomes difficult to form the DMG structure by two levels of conventional lithography, which requires less than 10 % of the gate length align error. Such technology causes further complication of the fabrication process. In this work, using tilt angle evaporation and lift-off technology,

we have developed a simple and practical fabrication method to form the DMG structure with two laterally contacting gate metals. Moreover, for the purpose of comparison, conventional single material (SMG) HFET are processed along with the experimental DMG-HFETs. They have the same structure except the gate metalization and they are fabricated on the same wafer using the same lithography and processing steps except the gate metal evaporations. After successive fabrication, the characteristics of the two kinds of device structures are measured, analyzed, compared and discussed.

The organization of this chapter is as follows. Section 7.2 describes detailed HFET fabrication procedures and section 7.3 is devoted especially to the process technology of the formation of the laterally contacting dual metal gate. The fabricated devices are tested and the results are presented in section 6.4. The final section 6.5 summarizes the experimental approach.

7.2 HFET Fabrication Process

The starting material, shown in Fig.7.1, is the MBE-grown pseudomorphic InGaP/InGaAs heterostructure, which is the only HFET material available to us and is supplied by the high speed electronics department of the Bell Labs, Lucent technologies. This material system has its special advantages. InGaP does not form DX-centers[96] and is less liable to oxidation than AlGaAs. The high valence band offset of the InGaP/InGaAs heterointerface acts as a hole barrier and reduces hole-induced gate leakage current. Furthermore the highly material selective etching of GaAs against InGaP [76] can provide a technological advantage concerning yield and homogenity.

The material layer structure on the GaAs substrate consists of a 500 nm GaAs buffer layer, a 25 nm InGaAs channel, a 2 nm GaAs spacer, a 2 nm InGaP spacer, a 5 nm

N^+ InGaP supply layer, a 25 nm undoped InGaP Schottky contacting layer, and finally a 60 nm highly doped GaAs cap layer.

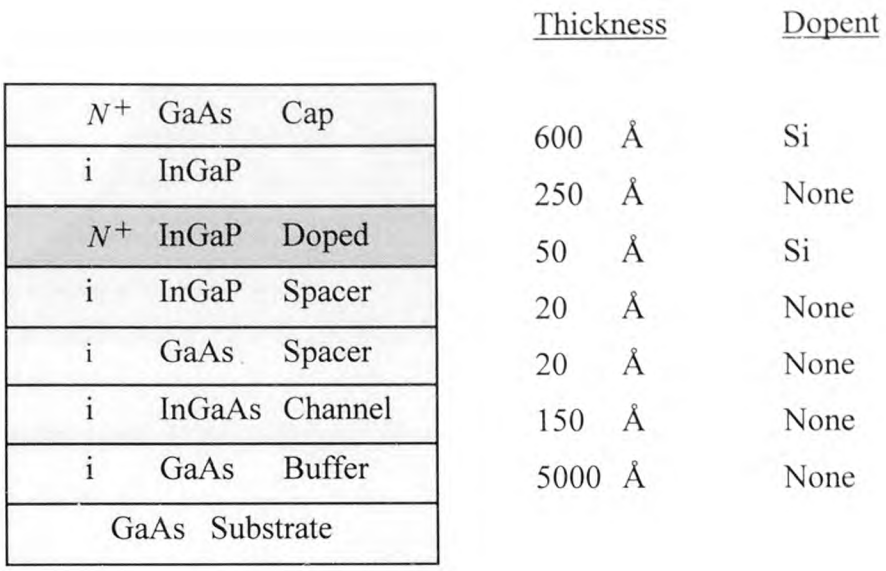


Fig. 7.1 Schematic structure of the starting MBE grown psudomophic heterojunction materials.

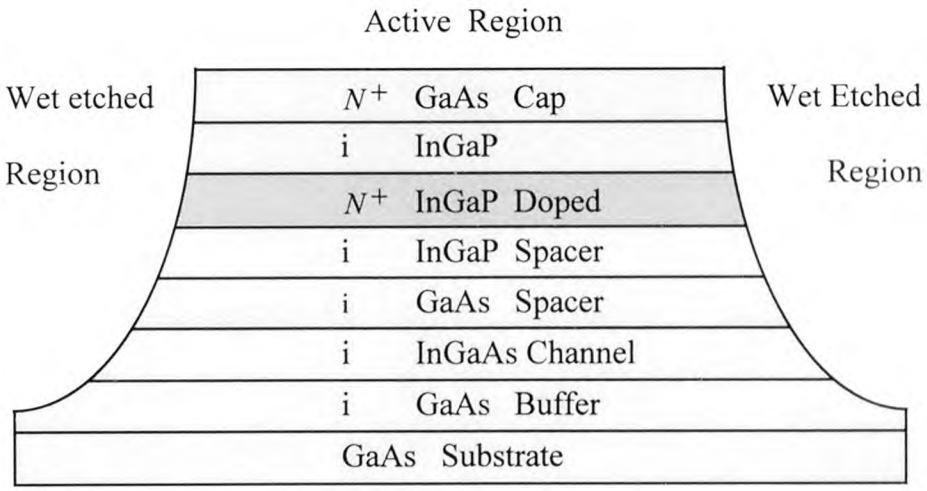


Fig. 7.2 Process cross section of the active region after the mesa etching to form the isolation between active regions.

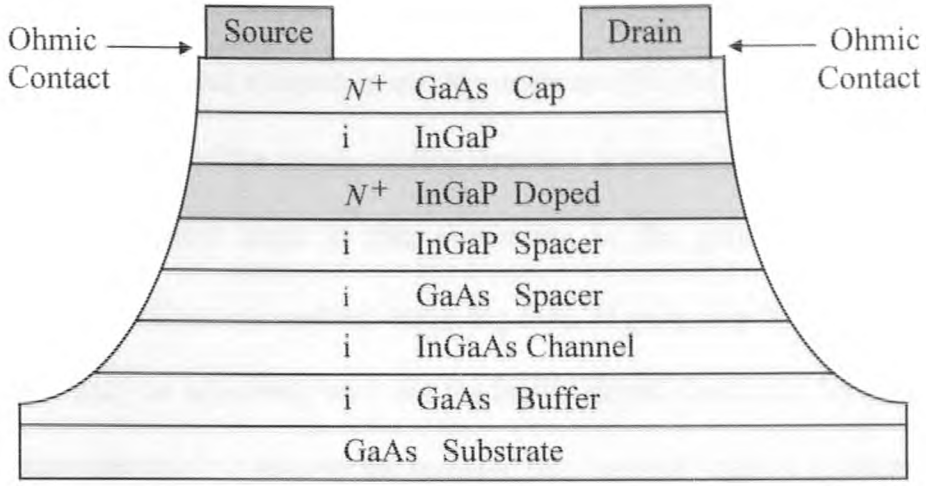


Fig. 7.3 Process cross section after the formation Source/Drain ohmic contact.

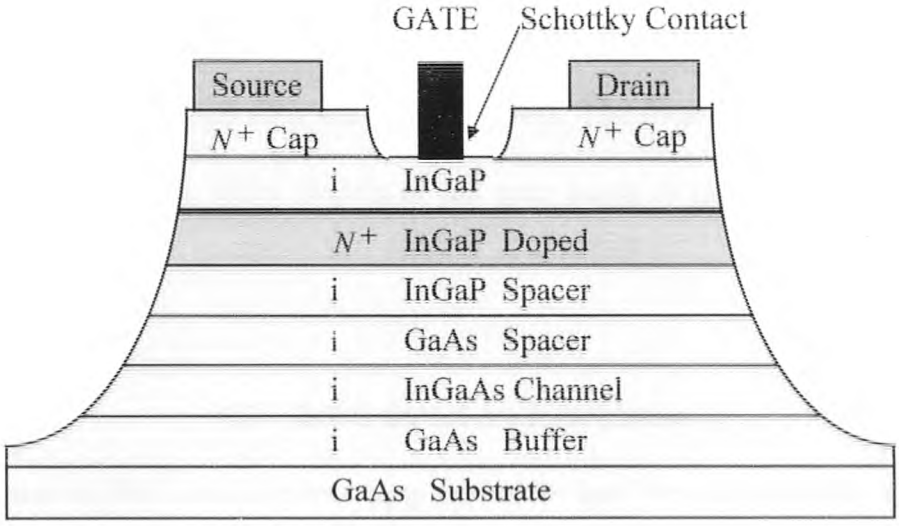


Fig. 7.4 Process cross section after the gate metallization. A typical HFET is fabricated.

Our major device processing sequence and process conditions are depicted in Fig.7.2 - Fig 7.4. After careful chemical cleaning, the wafer was patterned by lithography and recessed by isotropic wet chemical etching to form isolation between the active

regions as illustrated in Fig.7.2. The drain/source metal stacking structure consists of Au/Ge/Ni and Au. After ohmic contact evaporation with a total thickness of ~250 nm, the wafer was rapidly thermal alloyed in an N_2 ambient (385℃, 10 sec.) and tested for satisfied ohmic behavior. The corresponding structure is shown in Fig.7.3.

The most critical steps in this processing is the gate definition by optical lithography and wet chemical etching using $H_2SO_4:H_2O_2:H_2O = 2:2:50$ by volume (25 ℃, ~ 40 sec.) to selectively etch out the highly doped GaAs cap layer, followed by oxygen plasma treatment to remove the possible thin layer of organic contaminant on the gate region and then by short time etch-dip in light NH_4OH solution (~10 sec.) to etch out the native oxides. The subsequent gate material evaporation at room temperature incorporates the metal atoms effectively in the InGaP to form good Schottky contact. The 1 μm gate is formed after the step of lift-off. The final structure of the HFET is demonstrated in Fig.7.4. More details of the gate angle evaporation are described in section 7.3.

7.3 DMG Structure Fabrication

The conventional SMG-HFET processing procedure has been described in the previous section. The new DMG structure, however, requires additional processing step or steps in order to laterally form two well controlled contacting gate materials. A straightforward method of fabricating the DMG is using two steps of separate lithography to form the two gate material. Consequently, extremely precise lithography alignment is required especially for short channel FETs, which is extremely demanding and not practicable.

We propose another way to fabricate the DMG structure. As shown in Fig.7.5, tilt angle evaporation is utilized to process the DMG in a single gate pattern. This method,

which was used back in 1975[67], has the merits of simple, one lithography only and easy control of the corresponding lengths. The care must take to minimize the problem caused by the small amount of metal evaporated into the side wall which may result in some difficulties in lift-off.

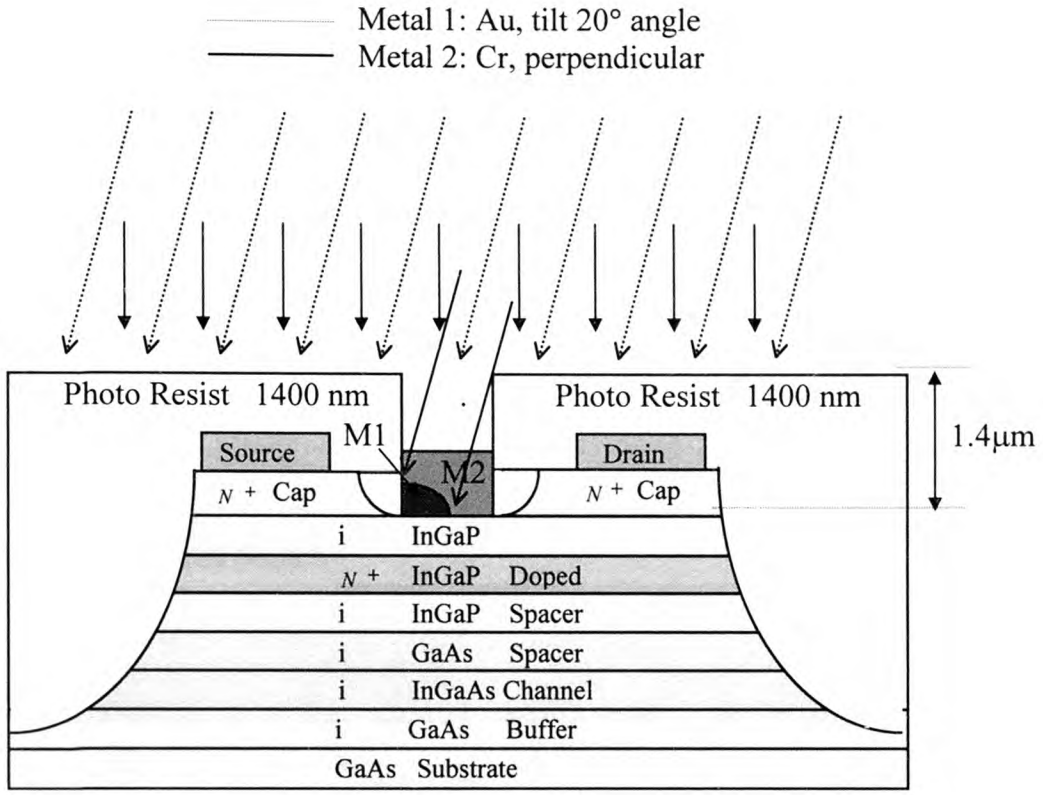


Fig. 7.5 Schematic diagram of the DMG structure fabrication process. The large work function metal is Au and the small work function metal is Cr.

After gate lithography, one of the gate metal, say, metal 1, is first thermally evaporated on part of the patterned gate region using photoresist as the shadow. The relation of the tilt angle, θ, the photoresist thickness, d, and the gate length, L_{m2}, is

$$Tan\theta = \frac{L_{m2}}{d} \qquad (7.1)$$

The subsequent second metal is therefore deposited just beside and on top of the first gate

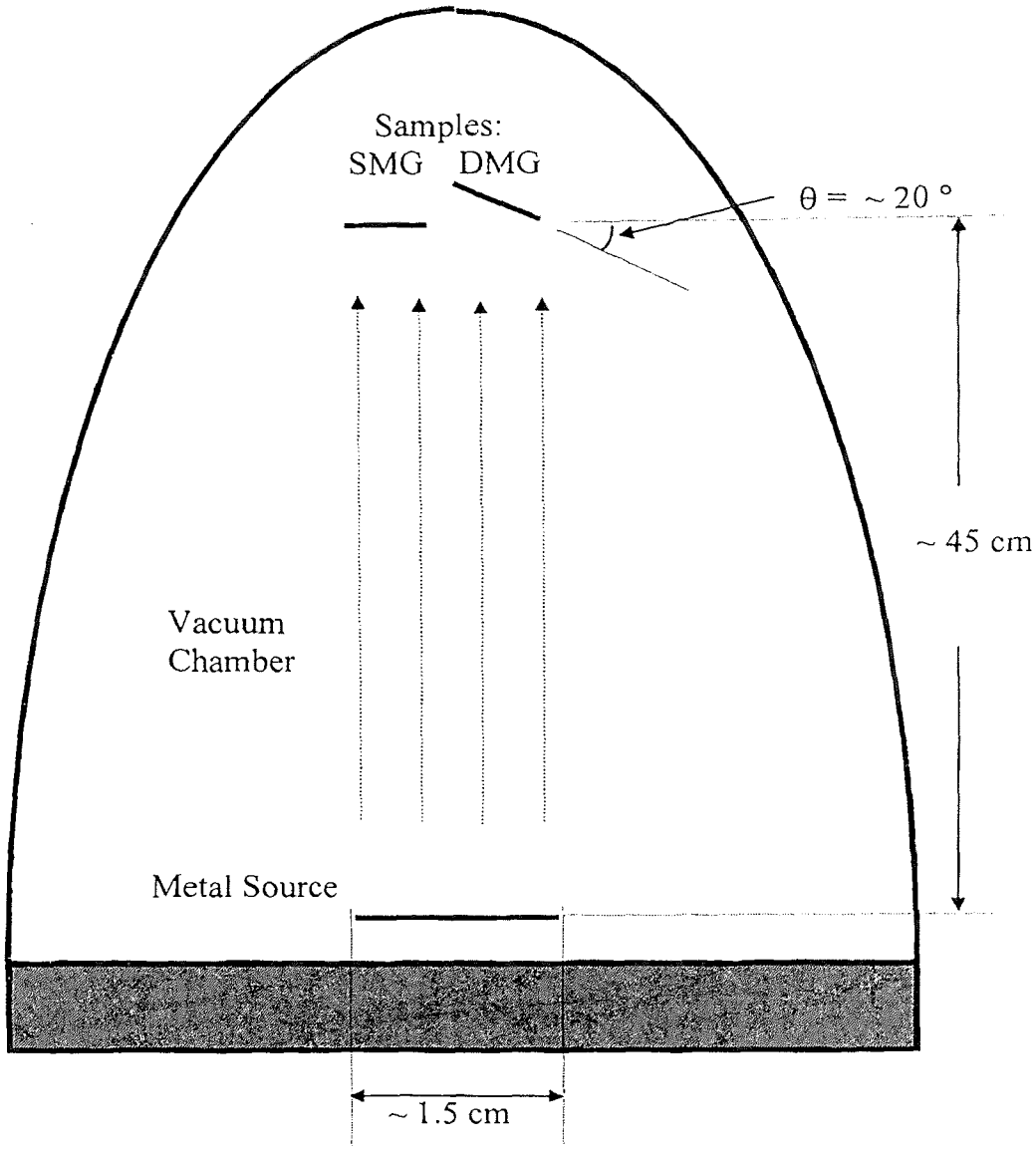


Fig. 7.6 Simplified schematic diagram of the evaporation method used to fabricate both SMG and DMG in the same vacuum system.

metal. A schematic diagram of the key features of tilt angle evaporation process are shown in Fig.7.6. By placing the sample wafer face down in a pre-designed angle with respect to the source, we can easily control the length of each gate metal. The total gate length is well defined by the lithography.

For the purpose of real comparison of the different gate structures between the DMG and SMG, we processed the DMG-HFET in the same wafer with the SMG-HFET. In other words, there was no difference between the DMG-HFETs and SMG-HFETs prior to the very beginning of the gate evaporation. The wafer was cut in two right before putting into the vacuum system. One of the pieces was placed perpendicularly face to the evaporation source to generate the SMG structure, whereas the other piece for DMG structure was placed with an angle of 20° to the direction of the evaporation source, which is schematically shown in Fig.7.6. Therefore, samples of the two kind of devices were first evaporated together, afterwards, the sample of DMG-HFETs was processed with an additional metal evaporation. The final fabricated HFETs have been examined using SEM. The typical gate lengths of 1 μm for both SMG-HFET and DMG-HFET have been measured and the lengths of the two gate metal for DMG-HFET are nearly equal and have a typical value of 0.5 μm as we predicted. Note that the tilt angle evaporation method does not require a separate lithography level, therefore, the lithography capable of processing 1μm gate can be used to fabricate 0.5μm + 0.5μm DMG. This is the reason why we compare the characteristics of a 0.5μm + 0.5μm DMG with a 1μm SMG-HFET.

7.4 Device Performance

As a vehicle for experimentally demonstrating the superb DMG-FET performance, we have fabricated both DMG-HFET and SMG-HFET using the technology described in section 7.2 and 7.3. Both the gate of SMG-HFET and the first gate material of DMG-HFET are Au. The second gate material of DMG-HFET is Cr which has lower work function. We have realized 1 μm total gate length for both the SMG- and DMG-HFETs.

7.4.1 I-V Characteristics

Typical current-voltage characteristics of DMG- and SMG-HFETs with the same gate width of 25 μm are shown in Fig.7.7. Both devices show good linear characteristics. However, as predicted by numerical simulation, the DMG-HFET exhibits a much higher drive current and clearly better saturation behavior than the SMG-HFET over all the bias conditions tested. The performance enhancement are apparently attributed to the more efficient electron transport or the electron velocity enhancement in the channel and the significant reduction in channel length modulation effect of DMG-HFET, which supports the concepts and simulation results we have explored in detail in previous chapters.

It is important to point out that angle evaporation and recess etch shape might generate different series resistance for the two compared device, which may cause transconductance and drain current difference. It can be seen from Fig. 7.7 that the compared DMG and SMG HFET have very consistent linear behaviors, which are related to series resistance. This indicate that two device have quite comparable series resistances. Therefore, the contribution of parasitic resistance difference should not be the reason of the characteristic difference we have obtained. It is noticed that the drive currents of the two device are low as compared to the values published for 1μm HFETs. We believe this is because that the devices is not well optimized especially the channel depth which seems large.

7.4.2 The Transconductance

The DMG-HFET sample also shows higher transconductance as shown in Fig.7.8. Up to 50 % improvement is observed for the DMG-HFET biased at V_{ds} = 2 V. This drain-source bias is large enough to place the devices into saturation mode of operation for the

gate voltage range we studied. The threshold voltage of the compared DMG-HFET and SMG-HFET is - 0.6V. If we substitute the gate metal of SMG-HFET with the same metal as the lower work function one in DMG-HFET, or use Cr as the gate instead, the threshold voltage of the fabricated SMG-HFET becomes -0.9V. From these values, we estimate the threshold voltage difference under the two gate metals is ~0.3 V which is lower than the work function difference and consistent with Bardeen's theory we quoted in section 5.3. This is probably because that other factors like surface states also play roles on the threshold voltage difference we can attain. Unfortunately, the measured Schottky barrier heights for Au and Cr on InGaP are not available to our knowledge. Instead, Au and Cr with barrier height about 1.3 and 1.06 were measured on GaP[99], respectively. From this reference, our experimental results seem reasonable.

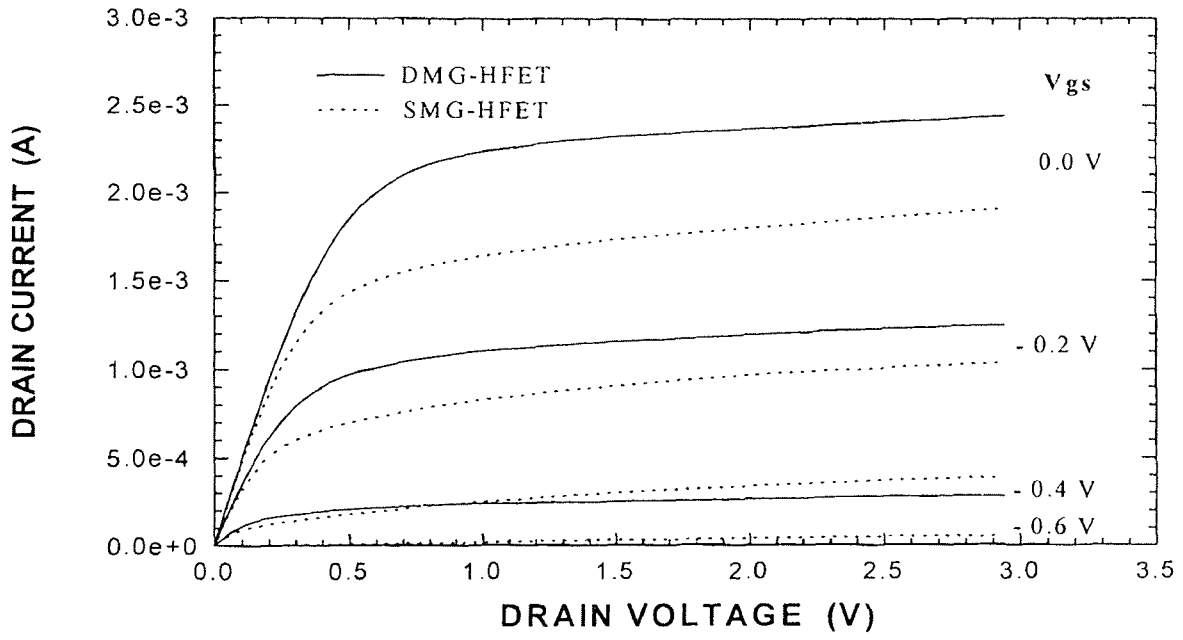


Fig. 7.7 Measured output characteristics of DMG-HFET (solid line) and SMG-HFET (dashed line).

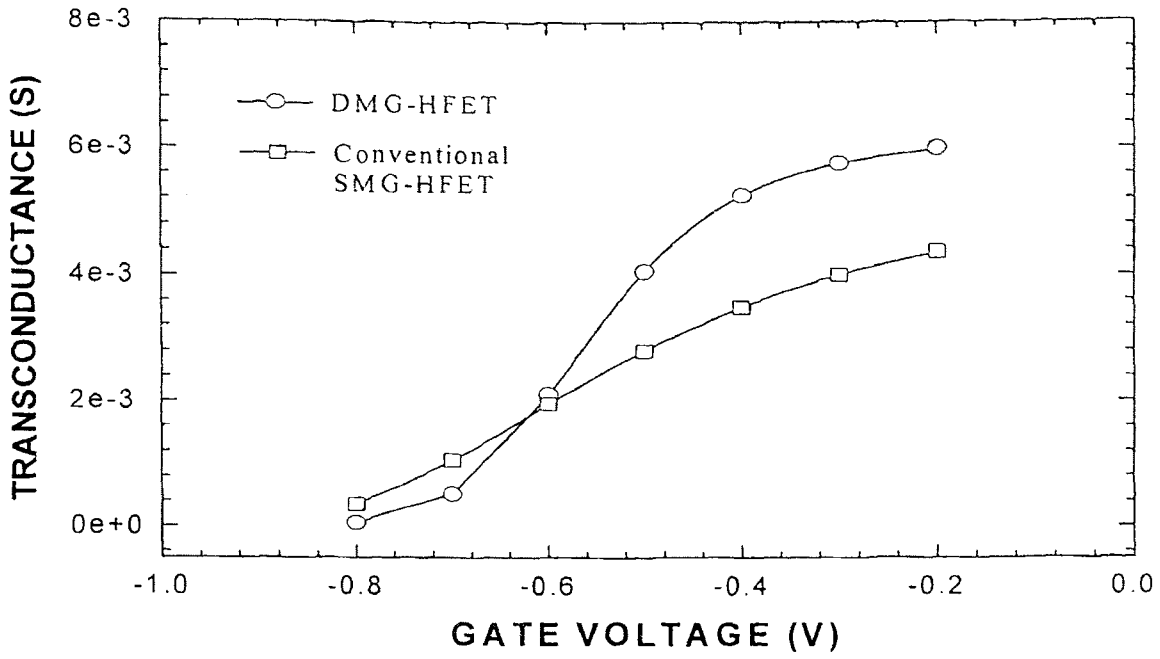


Fig. 7.8 Measured transconductance as a function of gate voltage for DMG-HFET and SMG-HFET.

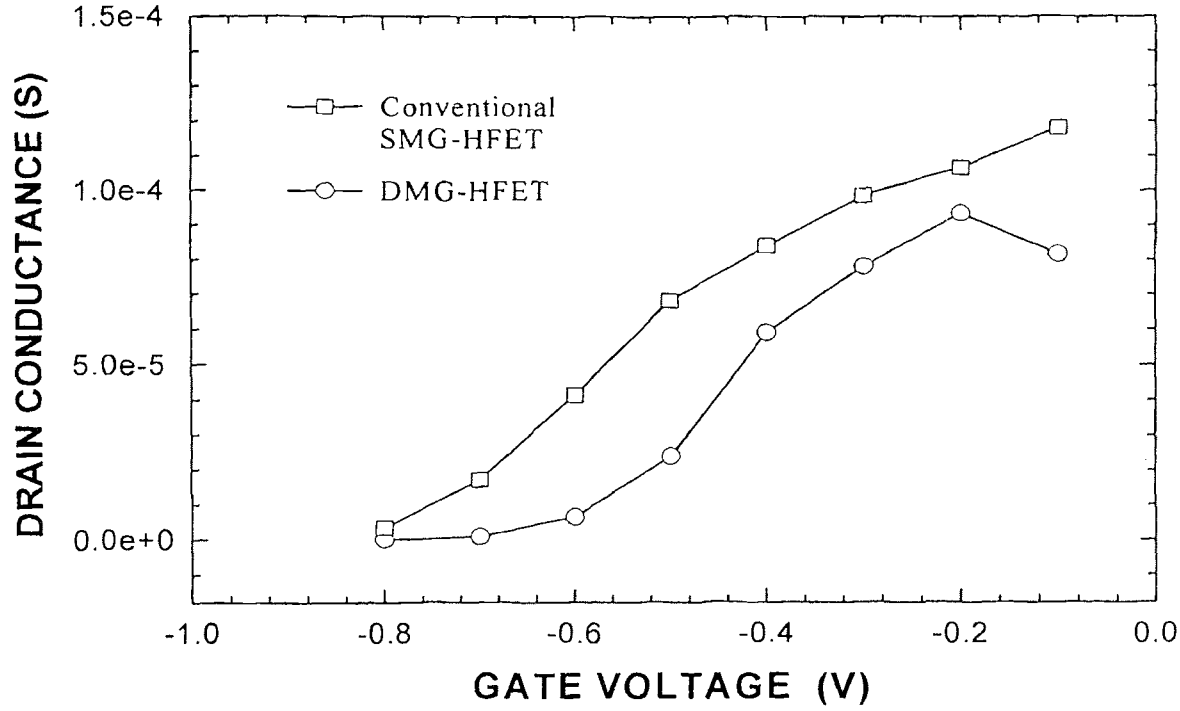


Fig. 7.9 Measured drain conductance versus gate voltage for DMG-HFET and conventional SMG-HFET.

Moreover, we find in the experimental results that for $V_{gs} < V_t$, the transconductance of DMG-HFET becomes smaller than that of SMG-HFET and decreases more rapidly when bias is down to the deep subthreshold region. This indicates that the decline of transconductance is due to the devices entering the subthreshold regime. We note that in regime below threshold, lower transconductance is an advantage instead of a drawback, because it stands for smaller subthreshold swing or faster current fall off.

7.4.3 The Drain Conductance

Fig.7.9 shows the behavior of drain conductance for typical DMG- and SMG-HFET biased at V_{ds} = 2 V. It is seen from the figure that the drain conductance of the DMG-HFET is always larger than that of the SMG-HFET. This suggests that in saturation regime after the channel has been pinched off near the drain, the channel charge depletion region in DMG-HFET almost does not extend and the effective gate length is almost kept unchanged with the increase of V_{ds}, indicating that the improvement in drain conductance is actually due to the screening effect. We note that in Fig.7.9, up to 100 % improvements in drain conductance are achieved by the DMG structure. The drain conductance deduction for the DMG-HFET is found to be more pronounced for lower gate voltage around the threshold.

7.4.4 Subthreshold Behaviors

The subthreshold characteristics for DMG-HFET and SMG-HFET are shown in Fig. 7.10 and Fig.7.11, respectively. Similar and excellent subthreshold slope or swing

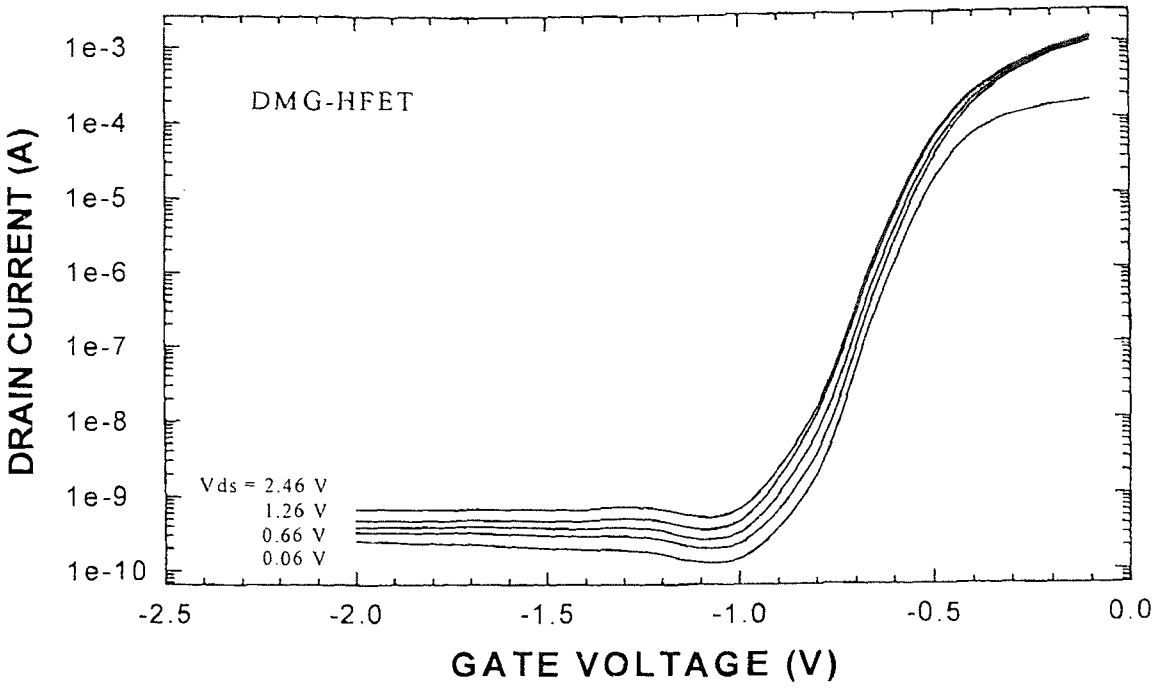


Fig. 7.10 Measured subthreshold characteristics of DMG-HFET at various V_{ds}.

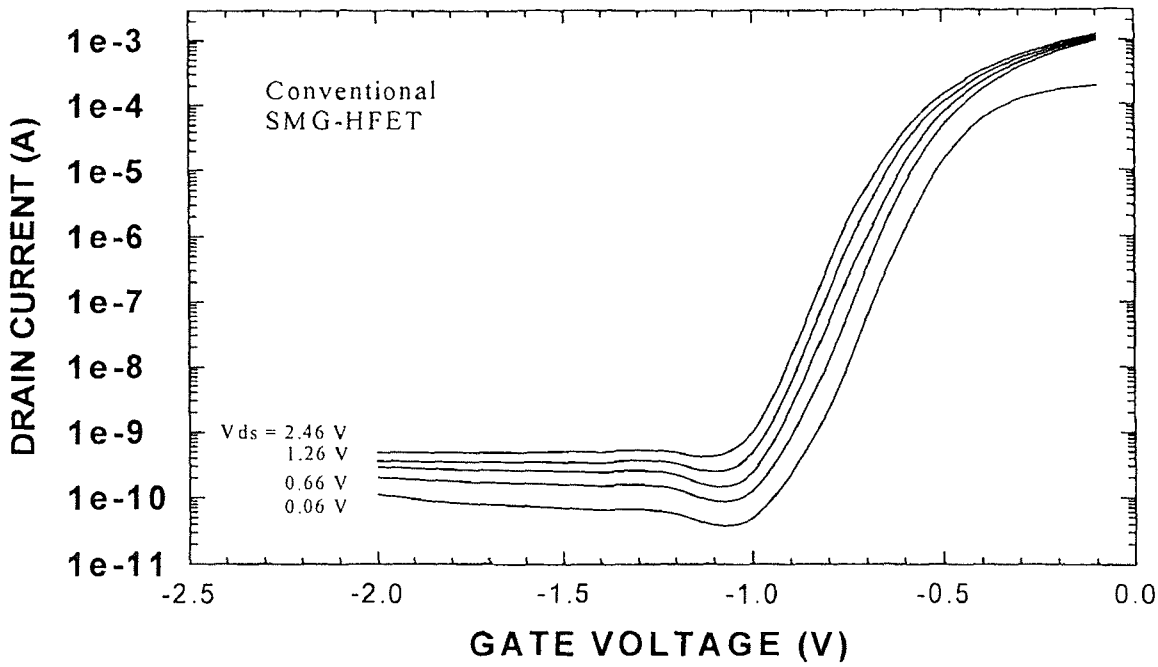


Fig. 7.11 Measured subthreshold characteristics of SMG-HFET at various V_{ds}.

($S = \frac{\Delta V_{gs}}{\Delta \log(I_{ds})}$) of only ~ 75 mV/decade is observed for both DMG-HFET and SMG-HFET. This may be due to the same vertical structure for the two devices we fabricated. The V_{ds} induced gate voltage shift ($\left.\frac{\Delta V_{gs}}{\Delta V_{ds}}\right|_{I_{ds}}$), neverthlessly, is found to be reduced to 23 mV/V for DMG-HFET in comparison to 50 mV/V for SMG-HFET. The considerable lower value of gate voltage shift for DMG-HFET compared to SMG-HFET sample corroborates that minimum channel potential of the former device undergoes much less variation during the change of V_{ds}, especially at relatively large V_{ds}. This directly indicates that DMG-HFET suppresses the drain induced barrier lowering (DIBL) extensively. This is due solely to the screening effect of DMG-FET according to our simulation results presented in previous chapters.

7.5 Summary

In this chapter, we have experimentally demonstrated significant performance improvement of DMG-FET over a wide bias conditions. Using InGaP/InGaAs HFETs as a vehicle, we have fabricated DMG-HFET using a tilt angle evaporation technique for the formation of the novel gate with two contacting metals. The tested results of the fabricated devices prove that the novel DMG structure can provide a wide range of benefits to the FET performance both above threshold and in the subthreshold regime.

From the measured characteristics, it can be seen that both drive current and transcoductance of DMG-HFETs significantly exceed that of conventional ones owing to the velocity enhancement. Also the use of two gate materials to introduce threshold voltage abrupt change in the channel leads to longer channel behavior in these short

channel DMG-HFETs we fabricated, resulting in greatly suppressing in short channel effects in terms of low drain conductance and small gate voltage shift in subthreshold, which suggests that the screening effect is responsible for the superb improvement. Therefore, the DMG-FET is very promising in many future applications, where high performance FET with deep submicron gate is required.

Further improvement can be expected by choosing different set of gate materials, optimizing the length ratio and device parameters. We believe that the advantage of DMG structure will be more pronounced if we use MOSFET instead of HFET as a demonstrating vehicle, because, as equation (6.2) and (6.3) indicated, for same work function difference, MOSFET will have more threshold voltage difference due to the non-Schottky contact of the gate.

CHAPTER 8

CONCLUSION

8.1 Summary

In summary, we have presented a new type of device — the dual material gate field effect transistor (DMG-FET) — for the first time and thereafter investigated this novel device extensively through theoretical and experimental approaches. Our investigation and study of DMG-FETs were motivated by the fact that it can take full advantage of dual gate FET and split gate FET while avoid their inherent disadvantages. We studied two most important issues — drive current and short channel effects — that have become the major concerns in recent years due to the continued scaling of FETs to deep submicron dimensions and the need for high performance. The objective of this research was to develop a new high performance FET structure, and the approach taken to achieve this was to start with related device of dual gate FETs, and then proceed to our new device structure. The major findings and results of this research are summarized below.

8.1.1 Analytical Study of Dual Gate FETs

1. An analytical dual gate FET model useful for device performance evaluation and physics study was derived. It included a complete set of device I-V equations and established a basis for DMG-FETs.
2. It was demonstrated that DG-FET could significantly suppress short channel effects but at a price of reduction in drive current and transconductance, as compared to conventional FETs.

8.1.2 Numerical Simulation of DMG-FET

1. The channel potential or electric field, coupled with the electron velocity, were combined to analyze the DMG-FET using PISCES 2ET, a 2D device simulator. The mechanisms of the new device operation was identified.
2. By making use of the work function difference between two gate materials, the DMG structure simultaneously induces two key effects: velocity enhancement effect and drain voltage screening effect. Velocity enhancement can increase device speed, drive current and transconductance. Screening effect can effectively suppress the short channel effects.
3. The DMG structure greatly improves the characteristics of FETs by substantially increasing transconductance, decreasing drain conductance and suppressing DIBL and hot carrier damage.
4. Two critical parameters limit the performance of DMG-FET: lengths of each gate material and the work function difference. We verified by numerical simulation that benefit was more pronounced by using shorter first gate material and larger threshold voltage offset or work function difference between the two gate materials.
5. Simulation results shown that one micron DMG-FET outperformed half micron conventional SMG-FET. Significant improvements in short channel effects were obtained.
6. The most important concept derived from our study is that the origin of screening effect is due to an introduction of step change of threshold voltage in the channel. Gradual change of threshold voltage can not induce

screening effect or introduce the mechanism of short channel effects suppression.

7. It should be noted that the DMG structure is expected to be applicable to all kinds of FETs. Excellent results were achieved using the HFET as a vehicle. Similar results are achievable with the use of other type of field effect transistors. Even better results are expected for the MOSFET due to the direct effect on threshold voltage offset from the two gate material's work function difference.

8.1.3 Experimental Realization of DMG-FET and Its Results

1. Tilt angle evaporation was applied to the fabrication of the critical dual material gate. DMG-HFET was thus fabricated for the first time. SMG-HFET were fabricated in the same process but without the tilt angle evaporation for comparison.
2. Experimental results showed significantly enhanced device performance and considerable reduction in short channel effects for DMG-HFET as predicted by simulation. This also clearly the validity and effectiveness of our theoretical approach.
3. Finally, it can be said that DMG-FET is very promising for the future, high speed, high performance, deep submicron FETs. It opens a new way to the improvement of the wide used FETs and it may be important to scaling down of FETs further into sub-quarter micron dimensions.

APPENDIX A

NUMERICAL 2D DEVICE SIMULATOR — PISCES AND THE SIMULATION DETAILS

PISCES is used for two-dimensional semiconductor device simulation. It takes as input the device geometric structure, including electrode specification, and doping/composition profile, and outputs the device I-V and C-V characteristics in addition to the internal distribution of electrostatic potential and electron and hole concentrations. There are many new features available in the new version of PISCES used, predominately, the capabilities to simulate the carrier and lattice temperatures and heterostructures in compound semiconductors. Hence, various non-stationary phenomena such as hot carrier effects and velocity overshoot can be analyzed using this program. Most of the material parameters have been calibrated and thoroughly surveyed with the help of industry[84].

1. Carrier Transport Model

PISCES uses a dual energy transport(for carrier temperatures and lattice thermal diffusion) model in semiconductors, which is developed based on the moment approach to solving Boltzmann Transport Equation(BTE). It uses six state variables to describe the status of a semiconductor device. These six variables are: electrostatic potential, Ψ, carrier concentrations, n and p, carrier temperatures T_n and T_p, and lattice temperature, T_L, and they are functions of space and time. All other device characteristics such as I-V characteristics and circuit model parameters can be calculated from the knowledge of the distribution of these basic variables, To determine the distribution of these variables

under applied bias, six independent equations are required together with proper boundary conditions. It is well established that with the drift-diffusion carrier transport model, Shockley semiconductor equations, i.e., Poisson's equation and carrier continuity equations, govern the distribution of Ψ, n, and p. The carrier concentrations can also be replaced, equivalently, by their respective quasi-Fermi levels, φ_n and φ_p, in classical distribution (either Boltzmann or Fermi-Dirac) functions. With the temperatures for both carriers and lattice introduced as independent variables, three more equations are needed and they can be derived from the energy balance principle. These include two kinetic energy balance equations for carriers and one thermal diffusion equation for the lattice.

2. Material Properties for Heterostructures

As mentioned in section 1, PISCES has introduced a set of expressions for carrier transport in heterostructures. In order to perform the simulation, essential material parameters must be known. The various material properties needed for the PISCES device simulation and their dependance on the composition are described below.

2.1 Material Parameters for Device Simulation

Material parameters in compound semiconductors depend strongly on the composition as well as (to a less degree) on the doping level. PISCES first identifies which material properties(parameters) are mostly concerned in the device simulation and then presents the composition dependence in terms of mole fraction. Beside, the lattice temperature effect on some parameters is also provided.

The minimum set of material parameters which have to be known in order to proceed the PISCES device simulation include:

1. Electron affinity, χ, and conduction band edge offset due to the composition change.
2. Energy bandgap, E_g.
3. Effective masses for electrons and holes, m_n^* and m_p^*, from which the effective densities of states for the conduction and valence bands, N_C and N_V, can be derived.
4. Dielectric constants.
5. Electron and hole mobilities, μ_n and μ_p, and their dependence on composition, doping density, electric field, and temperature.
6. Minority carrier lifetime and corresponding coefficients for various recombination mechanisms.
7. Coefficients for the impact ionization.
8. Saturation velocity, v_{sat}, which is used as a parameter in certain field-dependent mobility models.

2.2 Interpolation Scheme for Composition Dependence

The parameters for ternary materials are determined using the linear interpolation scheme from those of the constituent binary materials. But often this simple scheme is not accurate enough and the quadratic term, which is available for some materials from

experimental data, is therefore included. The material parameters for quaternaries is determined from those of ternaries using the following interpolation scheme.

$$Q(x,y)=\frac{1}{x(1-x)+y(1-y)}\cdot\{x(1-x)[(1-y)T_{Ga_xIn_{1-x}P}+yT_{Ga_xIn_{1-x}As}]+$$

$$y(1-y)(1-x)[(1-x)T_{Ga_xIn_{1-x}P}+xT_{GaAs_yP_{1-y}}]\} \qquad \text{(A.1)}$$

where $Ga_xIn_{1-x}As_yP_{1-y}$ is used as an example for quaternary material.

2.3 Parameters for Base Materials

Currently PISCES can handle four material systems: Ge_xSi_{1-x}, $Al_xGa_{1-x}As$, $Al_xIn_{1-x}As$, and $Ga_xIn_{1-x}As_yP_{1-y}$. Those compound materials can be derived from four types of base materials: Si, GaAs, InAs, and InP. A partial list of their respective material parameters are given in the following.

Table A.1

	Si	GaAs	InAs	InP	Units
E_g	1.08	1.424	0.359	1.347	eV
α	4.73	5.405	3.35	1.4205	eV
β	636	204	248	136	K
ε_o	11.8	13.1	14.55	12.4	
χ	4.17	4.07	4.9	4.4	eV
m_n^*	1.08	0.067	0.023	0.08	m_o
m_{lh}^*	0.16	0.074	0.024	0.089	m_o
m_{hh}^*	0.49	0.62	0.41	0.85	m_o
N_C	2.8×10^{19}	4.42×10^{17}	8.72×10^{16}	5.66×10^{17}	cm^{-3}
N_V	1.04×10^{19}	8.47×10^{18}	6.66×10^{18}	2.03×10^{19}	cm^{-3}
μ_n	1500	8500	22600	4500	$cm^2/V\cdot s$
μ_p	450	400	250	150	$cm^2/V\cdot s$
v_{sat}		1.5×10^7	1.0×10^7	2.5×10^7	cm/s

3. Mobility Models

Carrier mobility is one of the most important parameters in the carrier transport model. In PISCES, the mobility is, for most case, modeled as the function of the total doping density, N, lattice temperature, T_L, surface/interface scattering mechanisms which are generally modeled using the dependence on the transverse electric field to the surface/interface, and the electric field along the current path(longitudinal field). When the device size is in the submicron regime, however, the local, longitudinal field dependence may not be accurate enough and non-local effects, which is mainly characterized by the carrier temperature dependence, have to be taken into consideration. The following expression describes in a general way the carrier mobility dependence on various factors:

$$\mu(N,T_L,E_\perp,E_{II}) = f(\mu_o(N,T_L,E_\perp),E_{II}/T_c) \qquad \text{(A.2)}$$

where E_{II} and $E_\perp$ are the longitudinal and transverse components of the electric field with respect to the current direction, , which depends on N, T_L and $E_\perp$, is called the low field mobility because when $E_{II} \rightarrow 0$, $\mu \rightarrow \mu_o$, T_c is the carrier temperature with the subscript c representing either n or p for electrons and holes, respectively, and the symbol E_{II}/T_c indicates the dependency is either on E_{II} or on T_c but not on both.

3.1 Low Field Mobility Models

Without considering the transverse field dependence, the low field mobility can be written as μ_o(N, T_L). There are several such models available in PISCES.

Constant Mobility Model This mobility is the function of material only and does not dependent on the doping density. The values for four group of semiconductor materials are listed in table A.2:

Table A.2 Constant Mobility Used in PISCES

	$\mu_n(cm^2V^{-1}S^{-1})$	$\mu_p(cm^2V^{-1}S^{-1})$
$Silicon / Ge_xSi_{1-x}$	1500	450
$GaAs / Al_xGa_{1-x}As$	8500	400
$InAs / Al_xIn_{1-x}As$	22600	250
$InP / Ga_xIn_{1-x}As_yP_{1-y}$	4500	150

Arora's Empirical Mobility Model An empirical mobility model based on the fitting to the measurement data for silicon at different lattice temperature has originally been proposed by Arora and *et al.* [60] and is extended to apply to GaAs and related materials by Yu[61] based on the available measured data. The model has a general form of the following:

$$\mu_o(N,T_L) = \mu_{\min} + \frac{\mu_{dlt}}{1+(N/N_O)^{\alpha}} \qquad (A.3)$$

where parameters $\mu_{\min}$, μ_{dlt}, N_o, and α are all functions of T_L in the form of $aT_L{}^b$ where both a and b are constants. The parameter values for GaAs are list in Table A.3.

Table A.3

	$\mu_{\min}$	μ_{dlt}	$N_o(cm^{-3})$	α
Electrons	$2136T_L^{-0.7475}$	$6331T_L^{-2.687}$	$7.345\times10^{16}T_L^{3.535}$	$0.6273T_L^{-0.1441}$
Holes	$21.48T_L^{-1.124}$	$331.2T_L^{-2.366}$	$5.136\times10^{17}T_L^{3.690}$	0.8057

3.2 Mobility Dependency on Longitudinal Field

When the electric field along the current flow(called longitudinal field) becomes large, the carrier mobility is reduced. This reduction is on the top of the reduction due to the transverse field which usually happens only at the semiconductor and insulator interface. The longitudinal field reduction of the mobility can be modeled either as the function of the local field if the field intensity is not very large or the spatial change of either the field or the doping concentration is not very rapid, or as the function of the carrier temperature if the energy relaxation process lags apparently behind that of the momentum relaxation, a phenomenon termed as the non-local effect. In PISCES, two models for III-V are provided. One exhibits the behavior of the negative differential mobility when the field exceeds a critical value and is the accurate model for electrons in the bulk GaAs and related materials. The other has a saturation velocity and is suitable for the channel mobility modeling.

Bulk Mobility Model For electrons in the bulk GaAs and related materials due to the existence of several valleys with different effective mass in the conduction band structure, the drift velocity reaches a peak as the electric field is increased to a critical value and then the velocity decreases as the field further increases. This phenomenon, if viewed from the mobility modeling point of view, amounts to a negative differential mobility (defined as $dv/dE_{//}$). To model this field dependence for electrons in GaAs and related materials, a model proposed first by Thim[63] is used in PISCES as follows:

$$\mu(N,T_L,E_{//}) = \frac{\mu_o(N,T_L) + \frac{v_{sat}}{E}\left(\frac{E_{//}}{E_o}\right)^4}{1+\left(\frac{E_{//}}{E_o}\right)^4} \qquad \text{(A.4)}$$

where E_o is the critical field and has a default value of 4kV/cm, and $v_{sat} = 1.13 \times 10^7 - 1.2 \times 10^4 T_L$. It can be shown that when E > E_o, equation (A.3) leads to a negative differential mobility (NDM).

Channel Mobility Model One problem related to the above formulation is that when applied to the simulation of GaAs and related material FETs, the drain output characteristics (current vs. voltage) may exhibit an unrealistic zig-zag behavior. One possible reason is that the correct mobility model in the bulk may not be suitable to the carriers in the channel. In the program, PISCES provide another mobility model for electrons in GaAs and related materials, in which the carrier velocity approaches the saturation velocity with increased field monotonically in a manner of the hyperbolic tangent function. The model formulation is as follows[64] and does not exhibit NDM behavior.

$$\mu(N, T_L, E_{//}) = \frac{v_{sat}}{E_{//}} \tanh\left(\frac{\mu_o(N, T_L) E_{//}}{v_{sat}}\right) \qquad \text{(A.5)}$$

4. Simulation Example

A typical simulation example of our simulation is presented here to demonstrate the main features of PISCES and to describe the detail of the our numerical simulation. The simulated device is the pseudomophic InGaP/InGaAs HFET, as shown in Fig. A.1, which is a typical device structure we used as a demonstrating vehicle. All the PISCES simulation parameters or input files in this thesis are virtually kept same as described in this example except very few differences specified in the main text, which ensures that

the corresponding variation of simulation results are only due to the variations of appropriate parameter or structure.

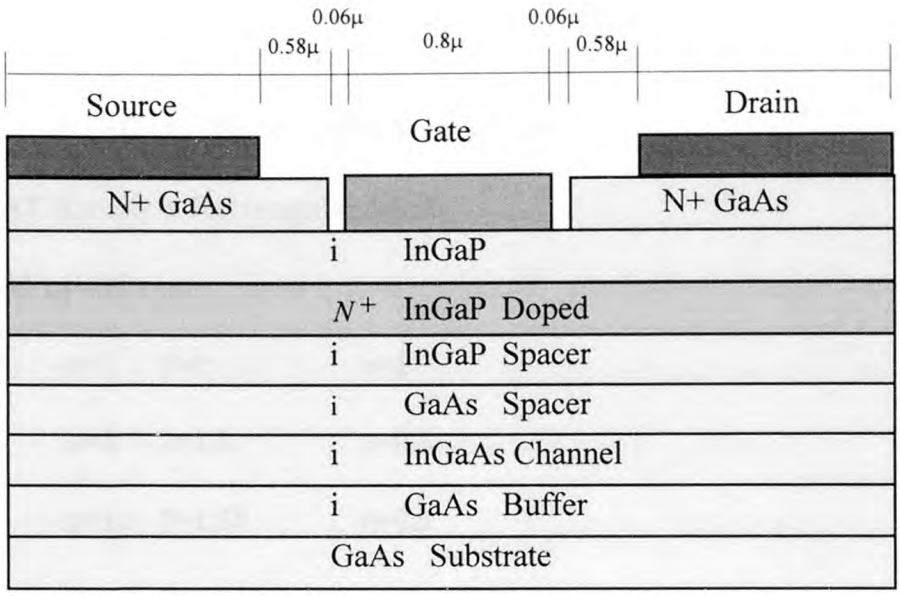


Fig. A.1 Simulated device structure.

As shown in Fig. A.1, This n-channel p-HFET is constructed in a rectangular region with source/drain regions formed in a N+ GaAs cap layer and the gate contact formed on top of undoped wide-bandgap InGaP layer. The layer structure consists of a 250Å undoped InGaP barrier layer followed by a 50 Å N+ doped InGaP layer, a 20 Å undoped InGaP supply layer, a 20 Å undoped GaAs spacer, a 150 Å undoped InGaAs channel layer, and a 5000 Å GaAs buffer. The GaAs buffer/substrate layer considered is limited to 5000 Å in order to save computational time. Because in PISCES ternary compound InGaP is represented by setting y=0 in quaternary $Ga_x In_{1-x} As_y P_{1-y}$, in the input deck which follows "GaInAsP" is used instead of "GaInAs". The gate contact is formed in a recessed manner. But in order to maintain the planarity of the structure, an

oxide is filled in the recessed region. The structure is described in the following input file. An important issue is the treatment of recessed surface, which is modeled by specifying the high density of deep level impurities at the recessed surface.

```
TITLE  InGaP/InGaAs based p-HFET structure
COMMENT Specify a Rectangular Mesh
mesh nx=55 ny=35 rect
x.mesh      n=1    l=0          r=1
x.mesh      n=6    l=1.0        r=0.8
x.mesh      n=10   l=1.58       r=0.9
X.MESH      N=15   L=1.64              R=1
X.mesh             n=37  l=2.44       r=1
x.mesh      n=42   l=2.50       r=1
x.mesh      n=46   l=3.08       r=1.1
x.mesh      n=51   l=4.0        r=1.2
$
y.mesh      n=1    l=0.0        r=1
y.mesh      n=4    l=0.06       r=1
y.mesh      n=12   l=0.085             r=0.8
y.mesh      n=14   l=0.09       r=1
y.mesh      n=16   l=0.092             r=1
y.mesh      n=18   l=0.094             r=1
y.mesh      n=25   l=0.109             r=1
```

```
y.mesh        n=35  l=0.609                r=1.5
$
$ Region and material specifications
region  num=1  ix.l=10  ix.h=42  iy.l=1   iy.h=4   insulator
region  num=2  ix.l=1   ix.h=10  iy.l=1   iy.h=4   algaas   xmole=0
region  num=3  ix.l=42  ix.h=51  iy.l=1   iy.h=4   algaas   xmole=0
region  num=4  ix.l=1   ix.h=51  iy.l=4   iy.h=12  gainasp  xmole=.51  ymole=0
region  num=5  ix.l=1   ix.h=51  iy.l=12  iy.h=14  gainasp  xmole=.51  ymole=0
region  num=6  ix.l=1   ix.h=51  iy.l=14  iy.h=16  algaas   xmole=0
region  num=7  ix.l=1   ix.h=51  iy.l=16  iy.h=18  gainasp  xmole=.51  ymole=0
region  num=8  ix.l=1   ix.h=51  iy.l=18  iy.h=25  gainasp  xmole=.47  ymole=1.0
region  num=9  ix.l=1   ix.h=51  iy.l=25  iy.h=35  algaas   xmole=0
$
$Electrodes: 1 Source, 2 Gate, and 3 Drain
$
elec  num=1   ix.l=1     ix.h=6     iy.l=1   iy.h=1
elec  num=2   ix.l=15    ix.h=37    iy.l=4   iy.h=4
elec  num=3   ix.l=46    ix.h=51    iy.l=1   iy.h=1
$
$Doping specification
$
doping  region=2  unif  conc=1e19  n.type
doping  region=3  unif  conc=1e19  n.type
```

```
doping  region=5  unif  conc=6e18  n.type
$
$ Interface trapping for the pinning of Fermi-level
$
deepimp unif  x.l=1.60 x.h=1.64 y.t=0.06  y.b=0.061 accep conc=1e19  eion=0.7
deepimp unif  x.l=2.44 x.h=2.48 y.t=0.06  y.b=0.061 accep conc=1e19  eion=0.7
$
contact  num=2 workf=4.8  surf.rec
models  temp=300  conmob  consrh  fldmob  auger  incompl
$
$ Solving Poisson's equation only for the equilibrium solution
$
symb  newton  carriers=0
method  itlimit=50  biaspart
$
solve    init
$
$ Switch to full set of semiconductor equations
$
symb   newton carr=2
$ Re-solve at the equvlibrium and save solution
$
solve outfile=hfet.ini
```

```
log   ivfil=modfet.iv
$
$ Apply the negative gate voltage and sweep Vd upto 4.0
solve  v2=-0.8   v3=0.0   vstep=0.2   nstep=4   elect=3   proj
solve  v3=1.3   proj
solve  v3=1.6   proj
solve  v3=2   vstep=1.0   nstep=2   elect=3   proj
$
plot.1d   x.axis=v3   y.axis=i3
$
end
```

Fig. A.2 PISCES input file for the simulation of InGaP/InGaAs HFET.

As shown in Fig. A.2, a non uniform mesh is used with a minimum mesh size of 10 Å in the y direction and 120 Å in the x direction (along the channel). The Poisson's equation, continuity equation and energy equations are solved by Newton method. Newton projection scheme is also adopted to project the next solution based on the current solution when the applied bias is changed.

REFERENCES

1. U. K. Mishra, A. S. Brown, and S. E. Rosenbaum, " DC and RF performance of 0.1 μm gate length $Al_{0.48}As/Ga_{0.47}In_{0.53}As$ pseudomorphic HEMT, " *IEDM Technique Digest*, San Francisco, CA, p. 180, 1988.

2. Y. Awano, M. Kosngi, K. Kosemura, T. Mimura, and M. Abe, *IEEE Trans. Electron Devices*, vol. 36, p. 2260, 1989.

3. K. Nummila, A. A. Ketterson, S. Caracci, J. Kolodzey, and I. Adesida, *Electron Letters*, vol. 27, p. 1519, 1991.

4. L. D. Nguyen, A. S. Brown, M. A. Thompson, and L. M. Jelloian, " 50nm self aligned gate pseudomorphic AlInAs/GaInAs high electron mobility transistors, " *IEEE Trans. Electron Devices*, vol. 39, p. 2007, 1992.

5. T. Furntsuka, M. Ogawa, and N. Kawamura, " GaAs dual gate MESFET's, " *IEEE Trans. Electron Devices*, vol. 25, p. 580, 1978.

6. Y. K. Chen, G. W. Wang, D. C. Raduleson, and L. F. Eastman, " Comparison of microwave performance between single gate and dual gate MODFET's, " *IEEE Electron Device Letters*, vol. 9, p. 59, 1988.

7. A. Cappy, B. Carres, R. Fanquembergues, G. Salmer, and E. Constant, *IEEE Trans. Electron Devices*, vol. 27, p. 2158, 1980.

8. M. Shur, " Split-gate field effect transistor, " *Applied Physics Letters*, vol. 54, p. 162, 1989.

9. K. Ismail, K. Y. Lee, D. P. Kern, and J. M. Hong, " Novel properties of a 0.1 μm long split-gate MODFET, " *IEEE Electron Device Letters*, vol. 11, p. 469, 1990.

10. M. Fukaishi, M. Tokushima, S. Wada, N. Matsuno, and H. Hida, " External gate fringing capacitance model for optimizing a Y-shaped, recess-etched gate FET structure, " *International Symposium on Compound Semiconductors*, San Diego, CA, p. 18, 1994.

11. A. Ketterson, W. T. Masselink, J. S. Gedymin, J. Klem, W. Kopp, H. Moorkoc and K. R. Gleason, " Characterization of InGaAs/AlGaAs pseudomorphic modulation-doped field effect transistor, " *IEEE Trans. Electron Devices*, vol. 33, p. 564, 1986.

12. T. Henderson, M. I. Aksun, C. K. Peng, H. Morkoc, P. C. Chao, P. M. Smith, and L. F. Lester, " Microwave performance of a quarter-micrometer gate low-noise P-MODFET, " *IEEE Electron Device Letters*, vol. 7, p. 649, 1986

13. J. H. van der merwe, " Crystal interfaces. Part II. Finite overgrowth, " *J. Applied Physics*, vol. 34, p. 264, 1963.

14. A. N. Lepore, M. Levy, R. Tiberio, P. Tasker, H. Lee, E. Wolf, L. Eastman, and E. Kohn, " 0.1um gate length MODFETs with unity current gain cut-off frequency above 110GHz, " *Electron Letters*, vol. 24, p. 364-366, 1988.

15. L. D. Nguyen, P. J. Tasker, D. C. Radulescu, and L. F. Eastman, " Characterization of ultra-high speed pseudomorphic AlGaAs/InGaAs(on GaAs) MODFET's, " *IEEE Trans. Electron Devices*, vol. 36, p. 2243, 1989.

16. C. K. Peng, M. I. Aksun, and K. R. Gleason, " Microwave performance of InAlAs/GaAs/ImP MODFET's, " *IEEE Electron Device Letters*, vol. 8, p. 24, 1987

17. A. S. Brown, U. K. Mishra, J. A. Henige, and M. Delaney, " The impact of epitaxial layer design and qulity on GaInAs/AlInAs high electron mobility transistor performance, " *J. Vac. Sci. Tech.*, vol. B6, p.2, 1988.

18. U. K. Mishra, A. S. Brown, and S. E. Rosenbaum, " DC and RF performance of 0.1um gate length AlInAs-GaInAs P-HEMT's, " *IEDM Tech. Dig.*, p. 180, 1988.

19. L. H. Camnitz, P. J. Tasker, H. Lee, D. van der Merwe, and L. Eastman, " Microwave characterization of very high transconductance MODFET, " *IEDM Tech. Dig.*, p. 360, 1984.

20. P. C. Chao, P. M. Smith, S. C. Palmateer, and J. Hwang, " Electron beam fabrication of GaAs low noise MESFETs using a new tri-layer resist technique, " *IEEE Trans. Electron Devices*, vol. 32, p. 1042, 1985.

21. L. F. Lester, P. M. Smith, and E. D. Wolf, " 0.15um double recess P-HEMT with Fmax of 380GHz, " *IEDM Tech. Dig.*, p. 172, 1988.

22. T. Tanaka, H. Furukawa, and D. Ueda, " Low voltage operation GaAs Spike-gate power FET with high power added efficiency, " *IEEE Trans. Electron Devices*, vol. 44, p. 354, 1997.

23. M. Hirose, K. Matsuzawa, M. Mihara, T. Nitta, A. Kameyama, and N. Uchitomi, " A lightly doped deep drain GaAs MESFET structure for linear amplifiers of personal handy-phone systems, " *IEEE Trans. Electron Devices*, vol.43, p. 2062, 1996.

24. Y. pao, and J. S. Harris, " Low conductive drain (LCD) design of InAlAs/InGaAs/InP HEMT's, " *IEEE Electron Device Letters*, vol. 13, p. 535, 1992.

25. D. Delagebeaudeuf, N. T. Linh, " Metal-(n) AlGaAs-GaAs two-dimensional electron gas FET, " *IEEE Trans. Electron Devices*, vol.29, p. 955, 1982.

26. M. C. Foisy, P. J. Tasker, B. Hughes, and L. F. Eastman, " The role of inefficient charge modulation in limiting the current gain cutoff frequency of the MODFET, " *IEEE Trans. Electron Devices*, vol.35, p. 871, 1988.

27. M. C. Foisy, *Ph.D. Dissertation,* Dept. of Electric Engineering, Cornell University, Ithaca, NY, 1989.

28. L. H. Camnitz, *Ph.D. Dissertation,* Dept. of Electric Engineering, Cornell University, Ithaca, NY, 1985.

29. N. R. Moll, M. R. Hueschen, and A. Fischer-Colbrie, " Pulsed doped AlGaAs/InGaAs P-MODFET's, " *IEEE Trans. Electron Devices*, vol.35, p. 878, 1988.

30. L. D. Nguyen and P. J. Tasker, " Scaling issues of ultra-high-speed HEMTs, " *SPIE High-speed Electronics and Device Scaling*, vol.1288, p. 251, 1990.

31. P. J. Tasker and B. Hughes, " Importance of source and drain resistance to the maximum fT of microwave MODFET's, " *IEEE Electron Device Letters*, vol. 10, p. 213, 1989.

32. S. Strahle, B. Henie, L. Lee, H. Kunzel, J. Dickmann, and E. Kohn, " Microwave performance of InP-based HEMTs for Low-voltage application, " *Microwave and Optical Technology Letters,* vol. 11, p. 131, 1996.

33. U. K. Mishra, A. S. Brown, L. M. Jelloian, and S. E. Rosenbaum, " Novel high performance self-aligned 0.1um long T-gate AlInAs GaInAs HEMT's, " *IEDM Tech. Dig.*, p. 101, 1989.

34. L. D. Nguyen, L. M. Jelloian, M. Thompson, and M. Jelloian, " 50nm self-aligned-gate P-AlInAs/GaInAs HEMT, " *IEDM Tech. Dig.*, p. 172, 1990.

35. L. D. Nguyen, A. S. Brown, M. Thompson, and M. Lui, " Fabrication of a 80-nm self-aligned T-gate AlInAs/GaInAs HEMT, " *IEEE Trans. Electron Devices*, vol.39, p. 2007, 1992.

36. P. M. Smith, " A high power, high efficiency millimeter-wave P-HEMT, " *1991 IEEE MTT-S Dig.*, p. 717, 1991.

37. E. Kohn, " V-shaped-gate GaAs MESFET for improved high frequency performance, " *Electronics Letters*, vol. 11, p. 160, 1975.

38. A. Hiroki, S. Odanaka, and A. Hori, " A high performance 0.1um MOSFET with asymmetric channel profile, " *IEDM Tech. Dig.*, p. 439, 1995.

39. A. F. Evason, J. R. A. Cleaver, and H. Ahmed, " Fabrication and performance of GaAs MESFETs with graded channel doping using focused ion-beam implantation, " *IEEE Electron Device Letters*, vol. 9, p. 281, 1988.

40. L. Lee, W. Long, S. Strahle, E. Kohn, et al., " Dual Gate HFET with Closed Spaced Electrodes on InP, " *15th Biennial IEEE Cornell Conference on Advanced Concepts High Speed The Semiconductor Devices and Circuits*, Ithaca, New York, p. VIII-3, 1995.

41. A. N. Khondker and A. F. M. Anwar, " Approximate analytic current-voltage calculations for MODFET's, " *IEEE Trans. Electron Devices*, vol. 37, p. 314, 1990.

42. D. Widiger, K. Hess, and J. J. Coleman, " Two-dimensional numerical analysis of high electron mobility transistor, " *IEEE Electron Device Letters*, vol. 5, p. 266, 1984.

43. K. Park and K. D. Kwack, " A model for the current-voltage characteristics of MODFET's, " *IEEE Trans. Electron Devices*, vol. 33, p. 673, 1986.

44. P. Rablin, S. C. Kang, and H. Morkoc, " Analytical solution of the velocity saturated MOSFET/MODFET wave equation and its application to the prediction of the microwave characteristics of MODFET's, " *IEEE Trans. Electron Devices*, vol. 37, p. 1068-1622, 1990.

45. T. J. Drummond, H. Morkoc, K. Lee, and M. S. Shur, " Model for modulation-doped field effect transistors, " *IEEE Electron Device Letters*, vol. 3, 1982.

46. C. S. Chang and H. R. Fetterman, " An analytical model for high-electron mobility transistors, " *Solid -State Electronics*, vol. 30,p. 485, 1987.

47. C. Z. Cil and S. tansal, " A new model for modulation-doped FET's, " *IEEE Electron Device Letters*, vol. 6, p. 434, 1985.

48. K. K. Chin, *Ph.D. Dissertation*, Department of Physics, Stanford University, Stanford, CA, 1986.

49. J. Pozela and A. Reklaitis, " Electron transport properties in GaAs at high electric fields, " *Solid-State Electron.*, vol. 23, p. 927,1980.

50. E. B. Johnson and A. Rose, " Simple general analysis of amplifier devices with emitter, control, and collector functions, " *Proc. Inst. on Radio Engineers*, vol. 47, p. 407, 1959.

51. M. B. Das and M. L. Roszak, " Design calculations for submicron gate length AlGaAs/GaAs modulation-doped FET structures using carrier saturation velocity/charge control model, " *Solid State Electronics*, vol. 28, p. 997, 1985.

52. D. Delagebeaudeuf and N. T. Linh, " Metal-(n)AlGaAs-GaAs two dimensional electron gas FET, " *IEEE Trans. Electron Devices*, vol. 29, p. 955, 1982.

53. K. Lee, M. S. Shur, T. Drummond, and H. Morkoc, " Current-voltage and capacitance-voltage characteristics of modulation-doped field effect transistors, " *IEEE Trans. Electron Devices*, vol. 30, p. 207, 1983.

54. B. Vinter, " Subbands and charge control in a two-dimensional electron gas field-effect transistor, " *Applied Physics Letters*, vol. 44, p. 307, 1984.

55. M. Hueschen, N. Moll, E. Gowen, and J. Miller, " Pulse doped MODFET's, " *IEDM Technique Digest*, p. 348, 1984.

56. A. B. Grebene and S. K. Ghandi, " General theory for pinched operation of the junction-gate FET, " *Solid-States Electron.*, vol. 12, p. 573, 1969.

57. C. S. Chang and D. Y. S. Day, " Analytic theory for current-voltage charateristics and field distibution of GaAs MESFET's " *IEEE Trans. Electron Devices*, vol. 36, p. 269, 1989.

58. J. Chen, M. Thurairaj, and M. B. Das, " Optimization of gate to drain separation in submicron gate length modulation doped FET's for maximum power gain performance, " *IEEE Trans. Electron Devices*, vol. 41, p. 465, 1994.

59. E. Kohn, " A semi-empirical comparison of key dynamic properties of GaAs and InP based HFET structures, " *17th Int. Sympos. on GaAs and Related Compounds*, InP Conference Series 112, p. 411, 1990.

60. E. Kohn, A. Lepore, H. Lee, M. Levy, " Performance evaluation of GaAs based MODFET's, " *1989 IEEE Cornell Conference on Advanced Concepts in High Speed Semiconductor Device and circuits*, Cornell Univ., NY, p. 91, 1989.

61. J. Dickmann, H. Dämbkes, H. Nickel, R. Schlapp, R. Rösch, K. Ploog and Y. H. Zang, " Influence of a surface layer on dc- and rf-performance of InAlAs/InGaAs HFETs, " *3rd International Conference on InP and Related Materials*, Cardiff, UK, p. 29, 1991.

62. E. kohn and J. Dickmann, " Carrier confinement and overshoot velocities in GaAs and InP based HEMTs, " *IEE-Colloqium on mm-wave Transistors and Circuits*, Leeds, p. 27, 1990.

63. Y. Pao, C Nishimoto, M Riaziat, R. Majidi-Ahy, N. G. Bechtel, J. S. Harris, " Impact of surface layer on InAlAs/InGaAs/InP HEMTs, " *IEEE Electron Device Letters*, vol. 11, p. 312, 1990.

64. S. C. Cripps and O. Nielson, " A dual gate MESFET X-band mixer, " *Proceding of Europe Microwave Conference*, p.125,1977.

65. T. Tanimoto, S. Tanaka, I. Ohbu, H. Matsumoto and T. Nakamura, " Dual gate FETs for ultra high efficiency HPA, " *IEDM Technique Digest*, p. 34, 1995.

66. D. R. Greenberg and J. A. del Alamo, " Velocity saturation in the extrinsic device: a fundamental limit in HFET's, " *IEEE Trans. Electron Devices*, vol. 41, p.1334, 1994.

67. S. R. Bahl, W. J. Azzam and J. A. del Alamo, " Strained-insulator In $In_x Al_{1-x} As / N^+ - In_{.53} Ga_{.47} As$ Heterostructure field-effect transistors, " *IEEE Trans. Electron Devices*, vol. 38, p.1986, 1991.

68. K. Hirakawa, H. Sakaki, and J. Yoshino, " Concentration of electrons in selectively doped GaAlAs/GaAs heterojunctions and its dependence on spacer-layer thickness and gate electric field, " *Appl. Phys. Lett.*, vol. 45, p.253, 1984.

69. D. R. Greenberg and J. A. del Alamo, " The impact of electron transport regimes on the linearity of GaAs/N+ InGaAs HFET's, " *Solid State Electronics*, vol. 36, p.53, 1993.

70. L. Lee, W. Long, S. Strahle, E. Kohn, et al., " Dual Gate HFET with Closed Spaced Electrodes on InP, " *15th Biennial IEEE Cornell Conference on Advanced Concepts High Speed The Semiconductor Devices and Circuits*, Ithaca, New York, p. VIII-3, 1995.

71. Y. C. Pao and J. S. Harris, " Physical origin of the high output conductance in $In_{.52} Al_{.48} As / In_{.53} Ga_{.47} As / InP$ HEMTs, " *Proc. 3rd Int. Conf. on InP and Related Materials*, p. 344, 1991.

72. J. B. Kuang, P. J. Tasker, G. W. Wang, Y. K. Chen, L. F. Eastman, O. A. Aina, H. Hier, and A. Fathimulla, " Kink effect in submicrometer-gate MBE-grown InAlAs-InGaAs-InAlAs heterojunction MESFET's, " *IEEE Electron Device Letters*, vol. 9, p. 630, 1988.

73. Y. Pao, J. S. Harris, " Low-conductance drain (LCD) design of InAlAs/InGaAs/InP HFET's, " *IEEE Electron Device Letters*, vol. 13, p. 535, 1992.

74. C. Gaquiere, B. Bonte, D. Theron, P. Arsene-Henri and T. Pacou, " Breakdown analysis of an asymmetrical double recessed power MESFET's " *IEEE Trans. Electron Devices*, vol. 42, p.209, 1994.

75. L. F. Lester, P. M. Smith, P. Ho, P. C. Chao, R. C. Tiberio, K. H. G. Duh, and E. D. Wolf, " .15 μm gate length double recess psudomorphic HEMT with Fmax of 350 Ghz, " *IEDM Technique Digest*, San Francisco, CA, p. 172, 1988.

76. J. R. Lothian, J. M. Kou, s. J. Pearton, and F. Ren, " Wet and Dry etching of InGaP, " *Material Research Soc. Symp. Proceedings*, vol. 240, p. 307, 1992.

77. M. Razeghi, F. Ommes, Ph. Maurel, Y. Chan, and D. Pavlidis, " GaInP/GaInAs lattice-matched and strained two dimensional electron gas field effect transistor, " *Semiconductor sci. Technology*, p103, 1991.

78. M. Takikawa and K. Joshin, " Pseudomorphic n-InGaP/InGaAs/GaAs high electron mobility transistor for low-noise amplifiers, " *IEEE Electron Device Letters*, vol. 14, p. 406, 1993.

79. D. Geiger, E. Mittermeier, J. Dickmann, C. Geng, R. Winterhof, F. Scholz, and E. Kohn, " InGaP/InGaAs HFET with high current density and high cut off frequencies, " *IEEE Electron Device Letters*, vol. 16, p. 259, 1995.

80. M. Shur and L. F. Eastman, *IEEE Trans. Electron Devices*, vol. 26, p.1677, 1979.

81. M. Heiblum, M. I. Nathan, D. C. Thomas, and C. M. Knoedler, *Physics Review Letters*, vol. 55, p. 2200, 1985.

82. A. F. Levi, J. R. Hayes, P. M. Platzman, and W. Wiegmann, *Physics Review Letters*, vol. 55, p. 2071, 1985.

83. J. G. Ruch, *IEEE Trans. Electron Devices*, vol. 19, p.652, 1972.

84. Z. Yu, D. Chen, L. So, and R. W. Dutton, " PISCES-2ET — Two Dimensional Device Simulation for Silicon and Heterostructures, " *Technical Report*, Stanford University, Stanford, CA, 1994.

85. A. Cappy, B. Carnes, R. Fauquembergues, G. Slamer, and E. Constant, *IEEE Trans. Electron Devices*, vol. 27, p.2158, 1980.

86. S. Strahle, B. Henle, L. Lee, H, Kunzel, J. Dickmann and E. Kohn, " Microwave performance of InP-based HEMTs for low voltage application, " *Microwave and Optical Technology Letters*, vol. 11, p. 131, 1996.

87. E. Kohn, S. Strahle, D. Geiger, and U. Erbent, " High field drift domain in GaAs and InP based heterostructure field effect transistors, " *Proc. IEEE Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, Ithaca, NY, 1993.

88. M. Yanagihara, Y. Ota, K. Nishii, O. Ishikawa and A. Tamura, " Highly efficient GaAs power MESFETs with n+-asymmetrical LDD structure, " *Electronics Letters*, vol. 28, p. 686, 1992.

89. C. Gaquiere, B. Bonte, D. Theron, P. Arsene-Henri, and T. Pacou, " Breakdown analysis of an asymmetrical double recessed power MESFET's, " *IEEE Trans. Electron Devices*, vol. 42, p.309, 1995.

90. Y. Pao and J. S. Harris, " Low conductance drain (LCD) design of InAlAs/InGaAs/InP HEMT's, " *IEEE Electron Device Letters*, vol. 13, p. 535, 1992.

91. M. Hirose, K. Matsuzawa, M. Mihara, T. Nitta, A. Kameyama, and N. Uchitomi, " A lightly doped deep drain GaAs MESFET structure for linear amplifiers of personal handy-phone systems, " *IEEE Trans. Electron Devices*, vol. 43, p.2062, 1996.

92. M. Levinson, P. G. Rossoni, S. Butler, and B. M. Ditchek, " Floating gates for avalanche suppression in MESFET's, " *IEEE Electron Device Letters*, vol. 13, p. 61, 1992.

93. K. Steiner, and N. Toyoda, " Mobility Profiles in submicron WNx-BPLDD -GaAs MESFETs, " *Japanese Journal of Applied Physics*, vol. 29, p. 489, 1990.

94. A. Hiroki, S. Odanaka, and A. Hori, " A high performance 0.1μm MOSFET with asymmetric channel profile, " *IEDM Technique Digest*, p. 439-442, 1995.

95. A. F. Evason, J. R. A. Cleaver, and H. Ahmed, " Fabrication and performance of GaAs MESFET's with graded channel doping using focused ion beam implantation, " *IEEE Electron Device Letters*, vol. 9, p. 281, 1988.

96. Y. J. Chan and D. Pavlidis, " Trap studies in GaInP/GaAs and AlGaAs/GaAs HFET's by means of low frequency noise and transconductance dispersion characterization, " *IEEE Trans. Electron Devices*, vol. 41, p.637, 1994.

97. R. H. Dean and R. J. Matarese, " Submicrometer self-aligned dual gate GaAs FET, " *IEEE Trans. Electron Devices*, vol. 22, p.358, 1975.

98. S. M. Sze, *Physics of Semiconductor Devices*, John Wiley & Sons, NYC, NY, 1981.