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Programmable latching probe microstructures for wafer testing applications

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ABSTRACT

PROGRAMMABLE LATCHING PROBE MICROSTRUCTURE FOR WAFER TESTING APPLICATIONS

by
Salmina Taifa Sadeq

The objective of this thesis is to design a programmable wafer testing array on a single chip based on micro electromechanical systems (MEMS) and VLSI. The wafer-scale integration in this thesis is a programmable array of test probes that are used for engineering test of VLSI and ULSI silicon integrated circuits at the wafer level. This consists of two subsystems (1) the VLSI address circuits used for addressing and controlling the MEMS on the chip and (2) the latching probe MEMS microstructure array that actuates into position for testing VLSI wafers. Each of the subsystems have been designed, analyzed and simulated separately. These structures were then integrated into a demonstration 4x4 array forming a programmable probe card. A 3-micrometer critical dimension is used for both the VLSI CMOS and the MEMS physical design layouts. The fabrication technique for the MEMS microstructure is detailed. A standard 12-mask CMOS technology is used for the fabrication of the address circuits.

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by
Salmina Taifa Sadeq

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PROGRAMMABLE LATCHING PROBE MICROSTRUCTURES FOR FOR WAFER TESTING APPLICATIONS

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This thesis is dedicated to my dear parents,
my husband and my daughter Sabriya

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CHAPTER 1

INTRODUCTION

Testing of the wafer functionality, during and after the chip has been fabricated, is an important part of silicon device manufacturing and technology. Over the years, many wafer testing systems have been developed that are either controlled manually or by computers. These systems fall into either of two categories. First, some systems include electric wires that act as probes into the wafer being tested [1-3]. Input signals are then applied to the probes, and the output signals from other probes are read out with discrete circuits. Most of the time, these test machines are large, expensive, and are not readily adapted to testing wide variety of chips and input/output pin configurations. Second, in other probe systems the probes are fabricated using micro-machined technology, but the addressing circuits are outside the tester chip [3]. In the later case, the system consumes more power since more power is supplied to the discrete transistor circuits. Also, the fabrication is expensive since the tester and the address circuits are fabricated separately.

The key idea explored in this thesis is whether one wafer can be used to test the functionality of another wafer. The testing wafer has probes that are programmable by addressing circuits fabricated using the same technology as that of the wafer to be tested. In addition, the control or addressing circuit is fabricated in the same chip as the tester probes. This results in a system which is comparatively less expensive to fabricate and consumes less power. In this thesis, a novel design of a wafer test probe head is proposed and demonstrated through an extensive set of numerical simulations. This wafer testing

system is based on an integrated circuit that uses CMOS and MEMS technology within a single chip which would be dramatically less expensive than their traditional counterparts [1-3]. This chip will carry both the control circuits as well as the testing probes. The wafer to be tested will be placed over the integrated probe array. The probes are mounted on MEMS structures where each includes a bimorph cantilever. The addressing circuits that control these cantilevers are designed using CMOS logic. The control circuit will heat the bimorph cantilevers to position them such that the probes mounted on the cantilever come in contact with the wafer under test (WUT).

The thesis is arranged in the following manner. Chapter 2 briefly describes the traditional wafer probe systems from a historical perspective, and also summarizes the Marcus-Carr patent which forms the basis of the new probe chip to be designed and analyzed in this thesis. Chapter 3 describes the novel system in detail. Chapter 4 describes the various components of the MEMS structures and includes a detailed description of its operation. In this chapter, not only the physical layout of this structure is discussed, but also a comprehensive calculation pertaining to heat, power dissipation, deflection of probe structure, and stress is included. Also included is a feasible fabrication technique for the MEMS structure, since the fabrication process is not as standardized as the CMOS technology. Chapter 5 describes the CMOS addressing circuit in detail. The simulations of the circuit components using PSPICE are demonstrated and the corresponding physical layout using L-EDIT is illustrated and discussed. Chapter 6 describes the integration of the CMOS and MEMS systems described in Chapters 4 and 5. Finally, in chapter 7, summarization of the thesis and discussion of further extension of this work for practical systems are included.

CHAPTER 2

BACKGROUND

2.1 Summary of Existing Wafer Probe Systems

In chapter 1, it was mentioned that the existing wafer probe equipments are either wire-grid based systems or systems based on VLSI circuits. Currently, the VLSI test systems have essentially replaced the more bulky and expensive wire-grid based test equipments. A number of companies now manufacture such VLSI test systems. One such leading company in this field is 'Advantest' [3].

The VLSI test systems manufactured by Advantest are primarily used in the testing of microprocessors and logic LSI devices. Advantest produces a large array of test structures. For example Advantest T6671B VLSI test system implements functions such as image processing in a system-on-a-chip form. Its test speed is 125MHz (I/O test rate) , 200MHz (data rate, clock rate). It employs 512 I/O pins and the overall timing accuracy is +/-500ps. An improvement over T6671B is T6681. This equipment is a high-performance system for new generation LSI devices such as those designed with a 0.25μm rule. It is used for testing RISC or CISC processors, data communication devices and high speed devices for use in multimedia applications. It has a test speed of 200/400MHz, 1024 I/O pins and a timing accuracy of +/-300ps. The T6682 VLSI test system is the newest member of the family of high performance logic and mixed signal test systems. This technology uses a new multi-pin architecture that provides each tester channel with a choice of three different DUT interface options – standard single wire I/O, Fly-By I/O and a separate (split) input and output per tester channel. The testing speed

varies from 250MHz to 1GHz with a high speed clock. The number of I/O pins is up to 1024. This equipment also supports audio and video frequency mixed signal and high speed clock options.

A sampling of these test systems highlight both the importance as well as the sophistication of these test structures. However, these structures also highlight the key limitation of the existing test structures. First, these test systems, with rigid input-output pin structure, and fixed spacing and depth of the probing pins are meant to test certain classes of chips having similar I/O pin structure. Second, the current system can only probe packages chips and are generally inflexible. This lack of versatility, which in turn increases cost, is the key objection to such systems.

The system to be explored in this thesis addresses the key limitations of the test structure and adds remarkable versatility of probing technology by replacing the rigid I/O probe pins with MEMS based microstructures. While there can be many different implementations of this concept, the architecture based on the Marcus-Carr patent [4] was selected as a prototype to explore this concept.

2.2 The Bimorph Structure Proposed by Marcus and Carr [4, 5]

The Marcus-Carr patent outlines a design of a wafer test system that is comprised of a microprobe structure to replace the rigid I/O probe pins in the traditional VLSI test equipment. This microprobe is made up of a base, a microcantilever extending in a plane from the base and a probe tip projecting from the microcantilever out of the plane. It is used for testing silicon wafers by bringing the probe tip in contact with the wafer under test (WUT).

The working principle in this case in quite simple. The microcantilever is a bimorph structure of two layers of materials having different coefficients of thermal expansion. There is also an integrated heating element that supplies heat to the microcantilever. The probe tip is made of silicon. The radius of the tip can be controlled to atomic sharpness (less than 1 nm) if desired. It can also be a planar structure. The two layers of the microcantilever are made of aluminum and silicon dioxide and the heating element is made of a line or ribbon of conductive material such as polysilicon. This heating element is in contact with the aluminum layer and supplies heat thereby causing the probe tip to deflect into an arc and bring it in contact with the material or wafer under investigation. Figure 2.1 shows the cross-sectional view of the microprobe in the present invention.

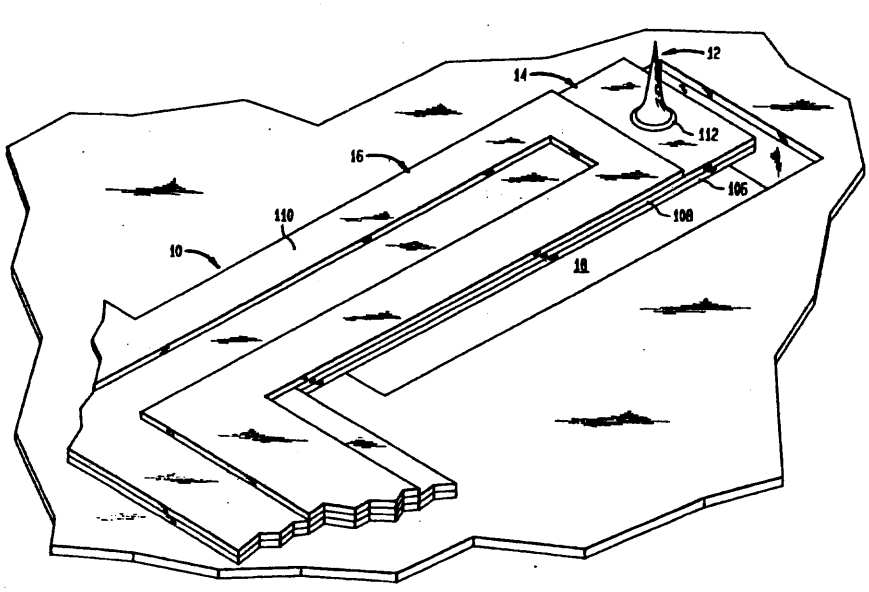
The microprobe is a monolithic structure (i.e. it is fashioned from a single piece of semiconductor) using the techniques of silicon chip processing. Typically the cantilever is 200 to 600 μm long, and about 20 to 30μm wide. The probe tip, which is made of silicon, is about 5μm long. The point of the probe tip is very sharp, typically 0.5nm. This allows it to penetrate the surface oxides for better connections. The air gap is about 10μm wide.

The bimorph structure of the cantilever consists of aluminum which is 1.5μm thick and a layer of silicon dioxide which is 1μm thick. The ribbon of conductive polysilicon that forms the heating elements is about 0.5μm thick.

Due to the difference of coefficients of thermal expansion of aluminum and silicon dioxide the cantilever which is 200μm long and 20μm wide will traverse an arc corresponding to a vertical distance of 10μm when 50mW power is applied to the heating

element. This power raises the temperature of the bimorph to 150 degrees Centigrade. Greater distances can be traversed if the cantilever is made longer. For example, a vertical distance of 50μm can be traversed if the length of the cantilever is increased to 500μm. In all these cases the direction of deflection is upwards. However, it is possible to reverse the direction of deflection with the probe tip pointing downward by reversing the layers of aluminum and silicon dioxide.

There can be many functional extension of the work done in the Marcus-Carr patent. One such extension of the invention is an array of individually addressable microprobes of this kind that are processed out of a silicon wafer and are connected by appropriate leads to the outside world to form a wafer probe card. While the Marcus-Carr patent emphasizes the concept of a flexible MEMS-based probe, one still needs to deal with the complete and specific layout architecture and electrical integrity to see if the basic concept could be converted into true a wafer probe system. This thesis explores in great details the concept presented in this patent. In this work, latching structures are used upon which probes are mounted. It utilizes CMOS row and column addressable circuits to address the programmable segments of the latching structures. The address circuits are also mounted in the same wafer. In short, it extends the basic concept presented into a true wafer probe system to see if the scaled-up version is feasible. The basic design of the patent has been modified to suit the purpose for this work.



U.S. Patent Dec. 12, 1995 Sheet 1 of 7 5,475,318

Figure 2.1 Bimorph cantilever proposed by Marcus-Carr patent.

In the above figure, the numbers 106 and 108 represent aluminum and silicon dioxide layers respectively. Number 110 is the polysilicon heater and 12 represents the probing pin. The air gap is represented by number 18.

CHAPTER 3

DESCRIPTION OF THE NEW SYSTEM

3.1 The System Architecture

This project utilizes cross row and column address circuits to program the position of a two dimensional array of microcantilever latching structures (see Figure 3.1). The row circuit consists of a shift register, a polysilicon resistor and a row driver. The column circuit consists of a shift register and a D/A converter. This configuration has application for semiconductor manufacturing test systems at the wafer processing level. The row and column circuits select one or more of the MEMS pixels in the array depending on the values shifted through them. A whole string of bits have to be loaded into the column circuits and one bit of data is shifted through the row circuits. Hence, the speeds of clock in the two address circuits are different. The clock rate in the column circuit is faster than the row circuit.

When one or more of the MEMS pixel is selected, current flows through it from the row address circuit. This current heats up the heaters in the pixel and raises the microprobe to touch the wafer being tested. The amount of current flowing depends on the value being loaded into the column address circuits. When all 0's are shifted into the column register, there is no current flow , and all the cantilevers remain in their equilibrium position. When all 1s are shifted, then there is maximum current flow causing maximum deflection of the cantilever beams. The intermediate values will allow current flow into the circuit too and will deflect the bimorph cantilever at varying heights making possible electrical contacts with wafer surface of non-planar topology.

3.2 Block Diagram of System Architecture

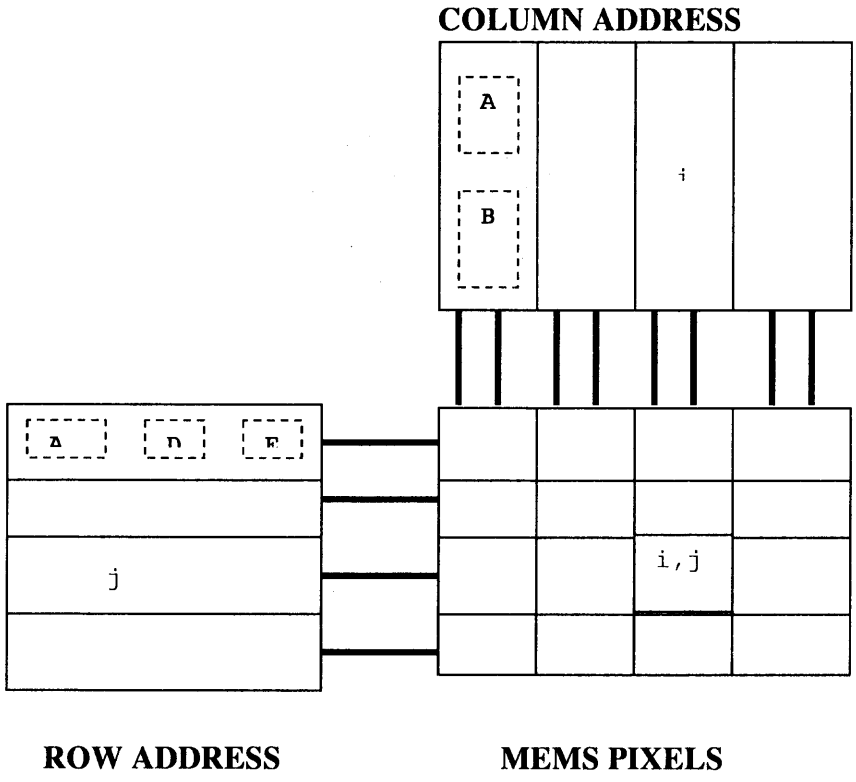


Figure 3.1 A 4x4 array of microcantilevers

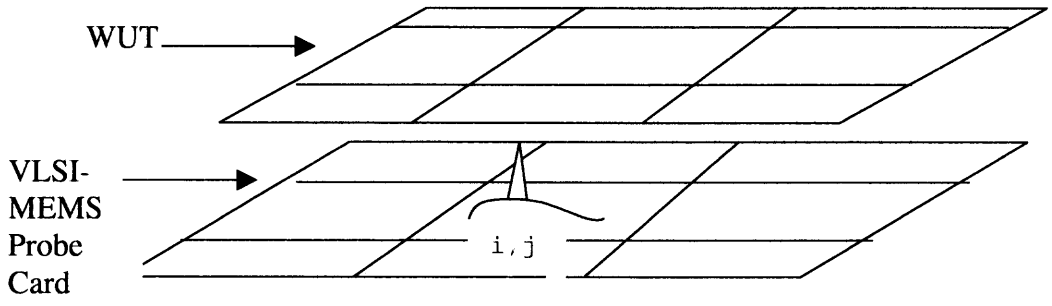


Figure 3.2 Illustration of wafer probing operation.

The column address circuit consists of a 3-bit shift register represented in Figure 3.1 as block **A** and a DAC, block **B**. The shift register is used to load the digital signal. This signal is sent to the DAC to be converted to analog current. This current will control the

current flowing from the row circuits that will heat the heaters in the microstructures. The DAC is the controller of current to the pixels. The row address circuit consists of a 1-bit shift register **A**, a polysilicon resistor **D** and a large PMOS transistor that acts as a row driver **E**. This row driver is necessary to supply the huge amount of current flowing through the pixels in the selected row. The shift register is the same one used in the column circuit, except only one of its bits is used in the row. The pixel itself includes the latching probe microstructure with the probe integrally mounted on a bimorph cantilever (see Figure 3.2). Current controlled by column address circuit flows from the row address circuit through the selected row of pixels. In Figure 3.1 a pixel represented by the ith column and jth row is selected and its testing operation is illustrated in Figure 3.2. The next chapters describe the microstructure and the address circuits in details.

3.3 Overall Design Strategy and Considerations

The main component in this thesis work is the design of the latching probe microstructure that is the wafer tester itself. First of all, the configuration of this design was chosen, and then the materials used for the design were decided upon depending on the material properties. In Chapter 4, ANSYS simulation was performed to compute the amount of heat required to deflect the probes to the desired height of 60μm. Then the current needed to produce this heat was calculated. In Chapter 5, the addressing circuits that would produce this current were then designed. The D/A converter in the column address circuit is the controller of current in the microstructure. The row driver in the row address circuit is the supplier of the current to heat the cantilever actuation structures.

CHAPTER 4

DESIGN AND SIMULATION OF MEMS LATCHING PROBE MICROSTRUCTURES

In the previous chapter the design strategy for this work was outlined. In this chapter, the design and operation of the latching probe microstructures referred to as 'pixels' in Figure 3.1 will be discussed. Detailed simulation results are presented, and a feasible comprehensive fabrication sequence is discussed.

4.1 Brief Description of Latching Probe Microstructure

The microstructure consists of a SiO_2 cantilever that is attached to a pedestal on one end. The other end is free to deflect. (See Figure 4.1). The microprobe is situated in the center of the cantilever. There are two aluminum heaters one on top and one on the bottom side of the cantilever. The heater next to the pedestal is located on the bottom side and the other one is on the top side. As a result of this arrangement when both heaters are heated, the cantilever deflects into an arc shape with the probe tip on the peak of the arc. The substrate has grooves cut into it so that with complete deflection, the free end of the cantilever latches into one of the grooves. Hence, the name latching probe microstructure. Once the cantilever is latched into a position, any change in ambient temperature of the heaters or the switching off of the power supply will not change the position of the probe. This helps to reduce power consumption as well as take accurate readings throughout the probe. The probe can only be unlatched with a temperature in excess of 100 degrees Centigrade.

4.1.1 Description of Components

As described in the previous section the components of the microstructure are the following: the pedestal, the SiO_2 cantilever, two aluminum heaters and the probe tip. The dimension of the microstructure is 300μm by 210μm. The dimension of the SiO_2 cantilever is 300μmX210μmX2μm. The two heaters on either side of the probe have serpentine structure. Each is made of approximately 300 squares of aluminum that has a thickness of 100nm. This results in a resistance of 100Ω. (See Figure 4.1). Heater A is situated below the SiO_2 cantilever and heater B is situated at the top of the cantilever. (See Figure 4.2). As shown in Figure 4.2, the base of the probe tip has a layer of aluminum that is about 1.5μm thick. The tip of the probe is made of gold and is square in shape. The thickness of the gold tip is 2μm. . The base of the probe has a dimension of 70μm x 70μm and the tip is 25μm x 25μm. Finally the cantilever is attached to a SiO_2 pedestal that is about 80μmX210μmX2μm.

The fabrication technique and masks to fabricate this microstructure is outlined in section 4.4 of this chapter. In the next section, the principle of operation of the microstructure is outlined.

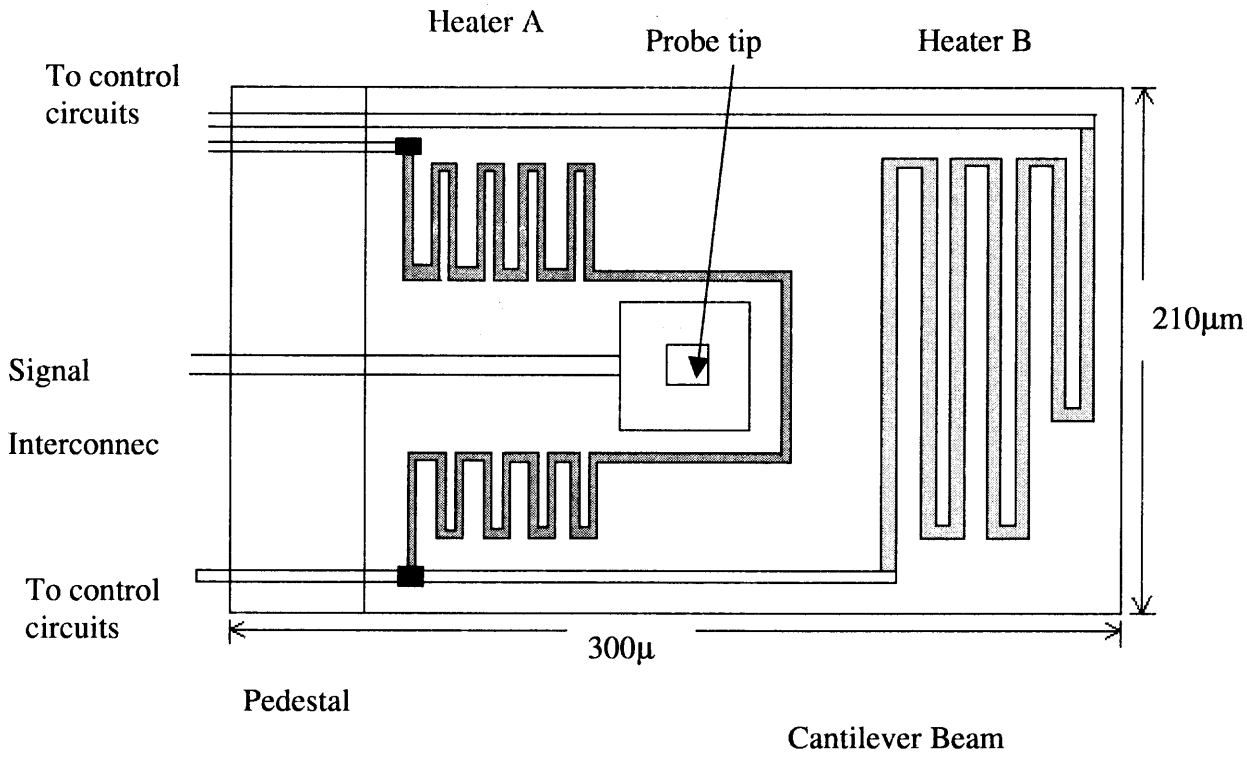


Figure 4.1 Top view of the microstructure

4.1.2 Operation of the Microstructures

Each of the heaters are connected to a row address circuit through an NMOS transistor switch which is controlled by the column address circuit. (See Figure 4.1). Current flows from the row address circuit into the aluminum heaters. The column address circuit controls this amount of current through the NMOS switch and with a load resistance 50kΩ.

The detailed operation of the addressing circuits will be described in the next chapter. As the current flows into the heater, the heater heats up the cantilever beam.

Since it is a bimorph structure as shown in Figure 4.2, heater A will deflect one half of the cantilever upwards and heater B will deflect the other half downwards thus forming an arc. On deflection, the free end of the beam latches itself on one of the grooves cut in the substrate. The wafer under test (WUT) is then brought in contact with the probe tip. Figure 4.3 illustrates graphically the latching process of the cantilever. In order to unlatch the cantilever, both heaters are activated first and then heater B is switched off . Refer to Figure 4.4 for the steps required to unlatch the cantilever from the grooves. This will first bend the cantilever slightly and then straighten the B portion of the cantilever This will release the cantilever from the latched position. Before beginning the unlatching sequence, the WUT is removed from the probe tip contact. Then as both the heaters are off, the cantilever will come to the unstressed level position.

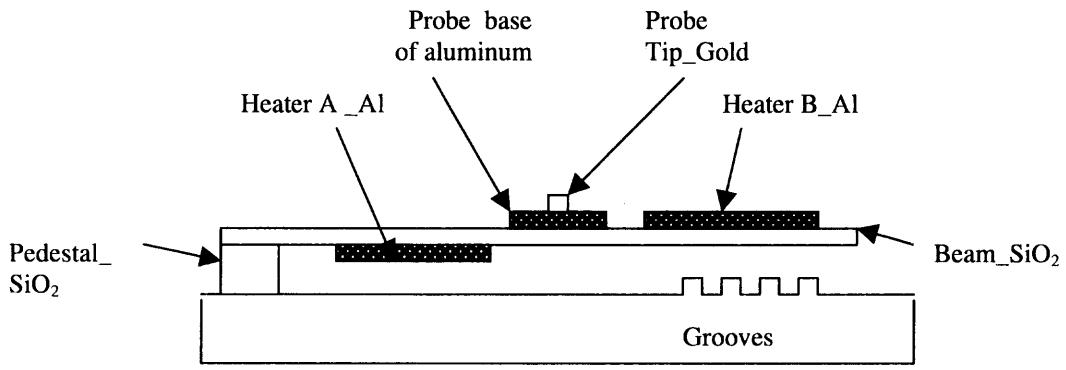


Figure 4.2 Side View of the microstructure

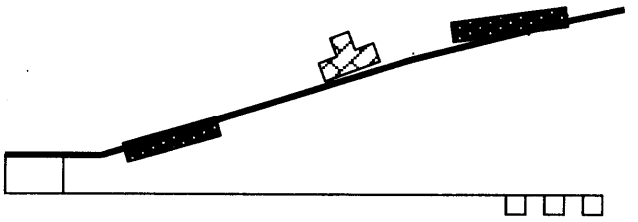
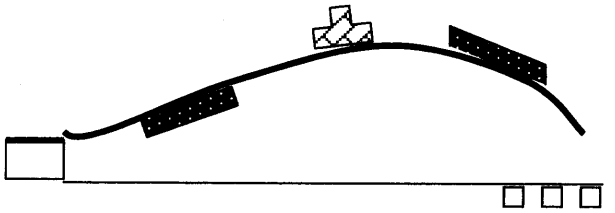
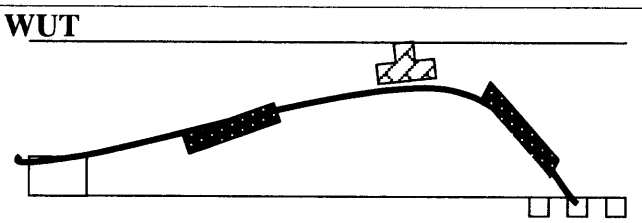
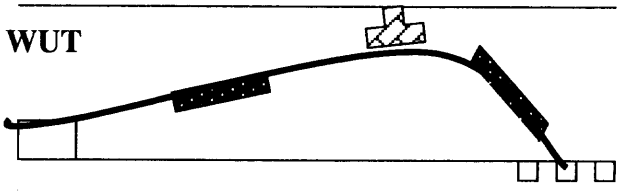
Heater A	Heater B	Side view of cantilever beam
OFF	OFF	
ON	OFF	
ON	ON	
OFF	ON	
OFF	OFF	

Figure 4.3 Programming sequence of latching position for WUT contact

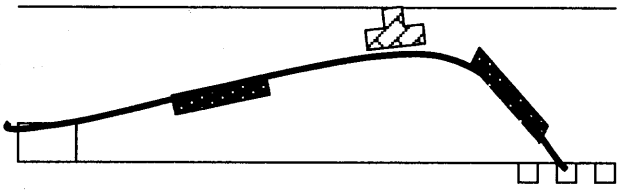
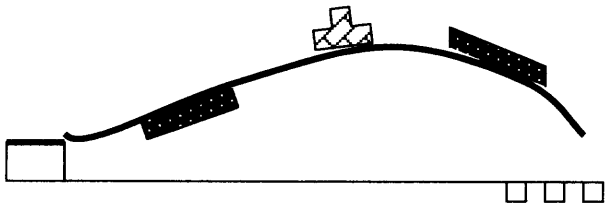
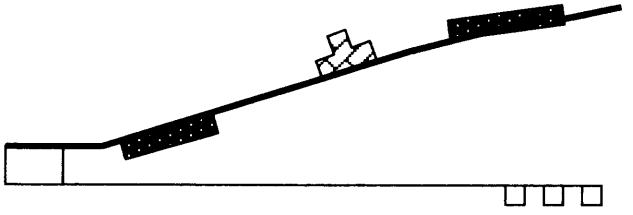
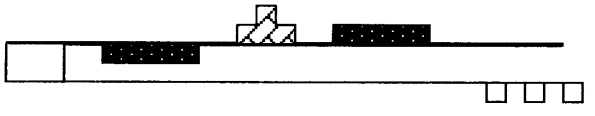
Heater A	Heater B	Side View of cantilever beam
OFF	OFF	
ON	ON	
ON	OFF	
OFF	OFF	

Figure 4.4 Programming sequence of unlatching for release at the WUT contact

4.2 Theory and Numerical Analysis of Microprobe Structure

While the previous section gives an overview of the operation, it is important to consider the process more quantitatively. In this section, first an analysis of the theory of bending is provided and then a numerical analysis based on ANSYS [6] simulation is done to quantitatively establish the theory.

4.2.1 Theory of the Bending of the Bi-metal Cantilever [7,8]

The theoretical analysis is based on calculation of longitudinal stress acting over the cross-section as well as the magnitude and distribution of the shearing and normal stresses along the interface. Figure 4.5 shows the components of the bimetal strip.

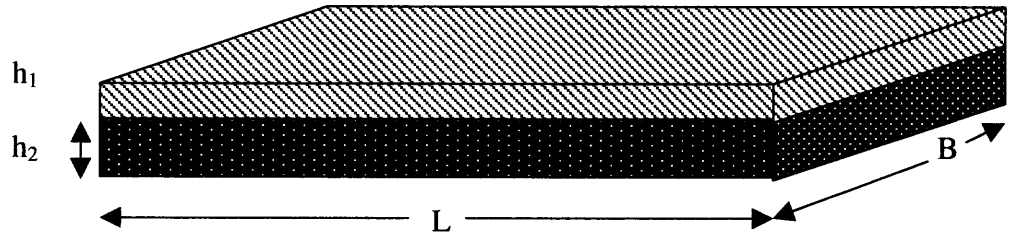


Figure 4.5 The bimetal strip for theoretical analysis

h_1 and h_2 are two thickness of SiO_2 and aluminum, respectively, L is the length and B is the width of strip.

We assume that the bimetal strip is heated by a temperature ΔT. The left end is fixed, whereas the right end is free to deflect. The thermal coefficient of expansion of upper component is $\alpha 1$ and that of lower component is $\alpha 2$. The longitudinal displacement

of the lower extreme fiber of the component number 1, $U_1(x)$ and of the upper extreme fiber of component number 2, $U_2(x)$ are given by:

$$U_2(x) = \alpha_2 \Delta t\, x - \frac{1-\nu_{21}^2}{E_2 h_2 b}\int_0^x Q(\xi)d\xi + \kappa_{21} q(x) + \frac{h_2}{2}\int_0^x d\xi \frac{1}{\rho(\xi)} \tag{4.1}$$

$$U_1(x) = \alpha_1 \Delta t\, x - \frac{1-\nu_1^2}{E_1 h_1 b}\int_0^x Q(\xi)d\xi + \kappa_1 q(x) + \frac{h_1}{2}\int_0^x d\xi \frac{1}{\rho(\xi)} \tag{4.2}$$

where E_1, E_2 are Young's modulus of elasticity, ν1, ν2 are Poisson's ratio.

$$\kappa_2 = \frac{2(1+\nu_2)h_2}{3E_2 b} \tag{4.3}$$

$$\kappa_1 = \frac{2(1+\nu_1)h_1}{3E_1 b} \tag{4.4}$$

are the coefficients of interfacial compliance. Here ρ(x) is the radius of curvature, Q(x) is the shearing force per unit plate length, given by

$$Q(x) = \int_{-l}^{x} q(\xi)d\xi \tag{4.5}$$

and *q(x)* Is the force at the X cross-section and *L* is half the plate's length. The first terms in Equation 4.1 and Equation 4.2 are the unrestricted thermal expansions of the stripes. The second terms are due to the forces Q(x), and the third term account for actual non-

uniform distribution of forces Q(x). The last term is due to bending. Since the displacement of the upper and lower stripes, U1(x) and U2(x), must be the same, and therefore Equation 4.1 and Equation 4.2 must be equated:

$$U_1(x) = U_2(x) \tag{4.6}$$

$$\kappa q(x) - \left(\frac{1-\nu_1^2}{E_1 h_1} + \frac{1-\nu_2^2}{E_2 h_2}\right) \int_0^x Q(\xi) d\xi + \frac{bh}{2} \int \frac{d\xi}{\rho(\xi)} = b\Delta\alpha\Lambda t \; x \tag{4.7}$$

where h=h1+h2 and $\Delta\alpha = \alpha_1 + \alpha_2$.

$$\begin{aligned} \kappa &= b(\kappa_1 + \kappa_2) \\ &= 2\frac{(1+\nu_1)}{3E_1} h_1 + 2\frac{(1+\nu_2)}{3E_2} h_2 \end{aligned} \tag{4.8}$$

Moreover, at equilibrium the net bending moments must be balanced by the shear force.

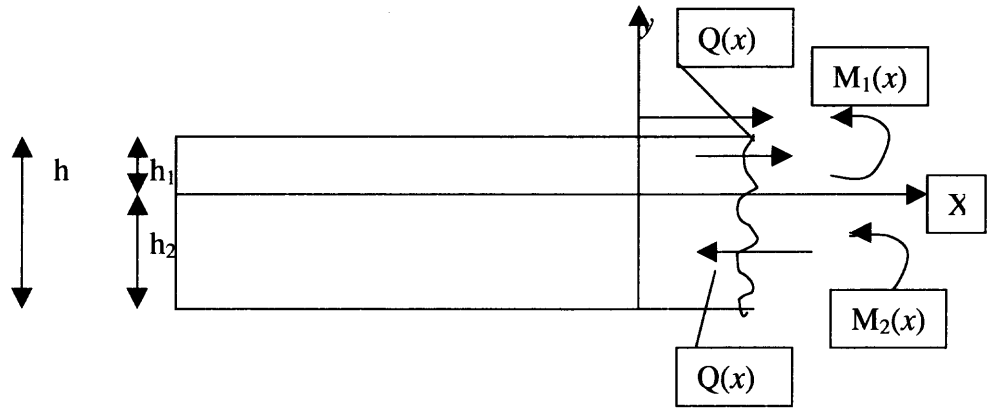


Figure 4.6 Forces and moments acting on the bimetal strip

The equation of equilibrium for the portion of the plate is as follows.

$$M_1(x)+M_2(x)-\frac{h}{2}Q(x)=0 \tag{4.9}$$

where $M_1(x)$, $M(x)$ are the bending moments of the strips and D1, D2 are flexural rigidities. It can be shown that

$$M_1(x)=\frac{bD_1}{\rho(x)} \quad , \quad M_2(x)=\frac{bD_2}{\rho(x)} \tag{4.10}$$

$$D_1=\frac{E_1h_1^3}{12(1-\nu_1^2)} \quad , \quad D_2=\frac{E_2h_2^3}{12(1-\nu_2^2)} \tag{4.11}$$

From equations 4.9 and 4.10 we get

$$\frac{1}{\rho(x)}=\frac{h}{2bD}Q(x) \quad , \quad D=D_1+D_2 \tag{4.12}$$

This is substituted in equation 4.7. After further manipulations it was found that

$$Q(x)=\frac{-b\Delta\alpha\Delta t}{\lambda}\chi(x) \tag{4.13}$$

where for large value of κl, we have

$$\begin{aligned}\chi(x)&=1-\frac{Cosh(\kappa x)}{Cosh(\kappa l)}\\&=1-e^{-\kappa(l-x)}\end{aligned} \tag{4.14}$$

and

$$\lambda=\frac{1}{12}\left(\frac{h_1^2}{D_1}+\frac{h_2^2}{D_2}+\frac{3h^2}{D}\right)$$

Hence equation 4.12 can be rewritten as

$$\frac{1}{\rho(x)} = \frac{-h\Delta\alpha\,\Delta t}{2\lambda D}\chi(x) \tag{4.15}$$

and the bending moments

$$M_1(x) = \frac{-bh\Delta\alpha\Delta t}{2\lambda D} D_1\chi(x) \tag{4.16}$$

$$M_2(x) = \frac{-bh\Delta\alpha\Delta t}{2\lambda D} D_2\chi(x) \tag{4.17}$$

The deflection function $v(x)$ can be found using the following equation:

$$\frac{d^2v}{dx^2} = \frac{-1}{\rho(x)} = \frac{h\Delta\alpha\Delta t}{2\lambda D}\chi(x) \tag{4.18}$$

After integrating this formula twice, an expression for maximum deflection is got

$$v_{\max} = \frac{hl^2\Delta\alpha\Delta t}{4\lambda D} \tag{4.19}$$

This expression shows that the displacement should vary linearly with temperature, quadratically with half the length of the plate. Later, this expression will be used to verify the detailed numerical simulation based on finite element analysis of the coupled elasto-thermal system by ANSYS software package. An alternative derivation of theoretical bending was performed based on a more recent publication [16]. The resulting expression turned out to support equation 4.19. Refer to Appendix C.

4.2.2 A Brief Description of the ANSYS Simulation for Bending Calculation

ANSYS is the software that is used here to simulate the MEMS structures [6]. It is used for thermal, electrical, mechanical, electro-mechanical and many other types of coupled-field analyses. The analysis is done by solving stress, heat, electrical and mechanical equations. The software is interactive and can be used for any combinations of analysis. The method that ANSYS uses for doing the simulation is called finite element method. It breaks down the material under test into finite number of elements of a shape and size chosen by the user and applies stress or heat. Then it meshes the elements together and solves the equations to give the outcome. The finer the size of the mesh, the more accurate the results of the simulation are since more number of algebraic equations has been used to represent the partial differential equations resulting from thermo-mechanical systems. This software is very versatile. It is able to analyze any geometric shape of any material. It can also be used to analyze multi-morph structures made of different materials stacked on top of each other, and therefore ideally suited for our purpose.

For our purpose, ANSYS has been used to simulate the bi-morph cantilever beam to see how much temperature difference is needed to get a deflection of about 60 to 80μm, which is the system specification. Shell 91, a 16-layer structural shell was chosen for the simulation. For the thermal-stress analysis the thickness of aluminum and SiO_2 layers was given. The material properties like the Young's modulus of elasticity, the thermal coefficients of expansion and Poisson's ratio for the two materials were also provided as inputs to the preprocessor. The schematic of the cantilever beam was then drawn. It was then broken into finite elements, tethered on one end and meshed. The temperature was then applied uniformly and the post processor was prompted to show the

resulting figure. These results were then tabulated and plotted for completeness. The simulation was carried for two cantilever beams of 100μm and 300μm long.

4.2.3 Results and Discussion of ANSYS Simulation

The results from the ANSYS simulation are tabulated below. Two cantilever beams of different lengths were simulated to accurately observe the relationship between the temperature and deflection with length.

Table showing deflection vs. temperature for 100μm long beam from ANSYS simulation.

Table 4.1 Temperature vs deflection of 100μm beam

TEMP. DIFF (ΔT)	DEFLECTION (μm)
0	0
200	15
400	30

Table showing deflection vs. temperature for 300μm long beam from ANSYS simulation.

Table 4.2 Temperature vs deflection of 300μm beam

TEMP. DIFF(ΔT)	DEFLECTION (μm)
0	0
150	60
200	80

Tables 4.1 and 4.2 show that the deflection is linearly proportional to the change in temperature. This fact is illustrated better in the following plot as expected from our theoretical analysis.

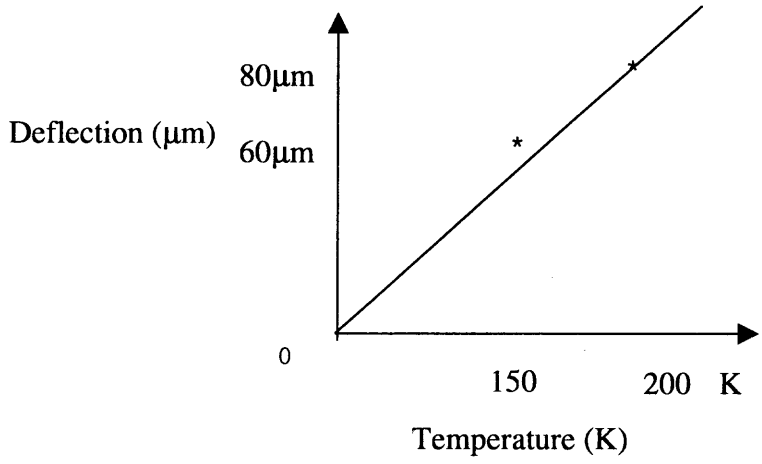


Figure 4.7 Illustration of linear relationship between temperature difference and deflection of 300μm long cantilever

Based on the simulation, it was concluded that for a deflection of 80μm, a cantilever beam of 300μm, and width of 210μm requires a temperature difference of approximately 200 K. Here it should be noted that the deflection calculations are limited to the linear range only.

4.2.4 Comparison between ANSYS and Simple Analytical Theory

In this section, a comparison of the results of deflection obtained by ANSYS and the calculated value of deflection using the analytical expression in equation 4.19 are done. This will validate the ANSYS simulation in a general manner.

Table 4.3 Parameters and their values in theoretical calculation of deflection height

Parameters	**Symbol**	**Value**	**Units**
Length of beam	l	$300x10^{-6}$	m
Thickness of SiO_2	h_1	$2x10^{-6}$	m
Thickness of Al	h_2	$100x10^{-9}$	m
Temperature difference	ΔT	200	K
Difference in thermal exp.	$\Delta\alpha$	$22.6x10^{-6}$	K^{-1}
Poisson's ratio of SiO2	ν_1	0.27	-
Poisson's ratio of Al	ν_2	0.27	-
Young's modulus of SiO_2	E_1	$0.74x10^{11}$	N/m^2
Young's modulus of Al	E_2	$0.69x10^{11}$	N/m^2
Constant	λ	$1.6x10^{-4}$	m^3/N
Flexural rigidity of SiO_2	D_1	$5.32x10^{-8}$	N/m
Flexural rigidity of Al	D_2	$6.2x10^{-12}$	N/m

Using the above values and Equation 4.19 the maximum deflection found for a 300μm beam was approximately 25μm. Although the deflection is significantly underestimated by this formula compared to the numerical simulation, however, both the functional dependence expected from the analytical theory (see Equation 4.19) that (a) the deflection is proportional to the temperature difference and (b) that the deflection is proportional to the square of the length are clearly demonstrated in from numbers in

tables 4.1 and 4.2, respectively. It was therefore concluded that although the simple theory is not quantitatively accurate it does capture accurate underlying physics of the problem correctly. An alternative calculation based on a more recent publication [16] is included in Appendix C.

4.3 Physical Layout

ANSYS simulation shows that a 300μm long cantilever will bend to give a deflection height of 60 to 80μm when heated by a temperature difference of 200 °K. Hence the layout of the microstructure was then proceeded with.

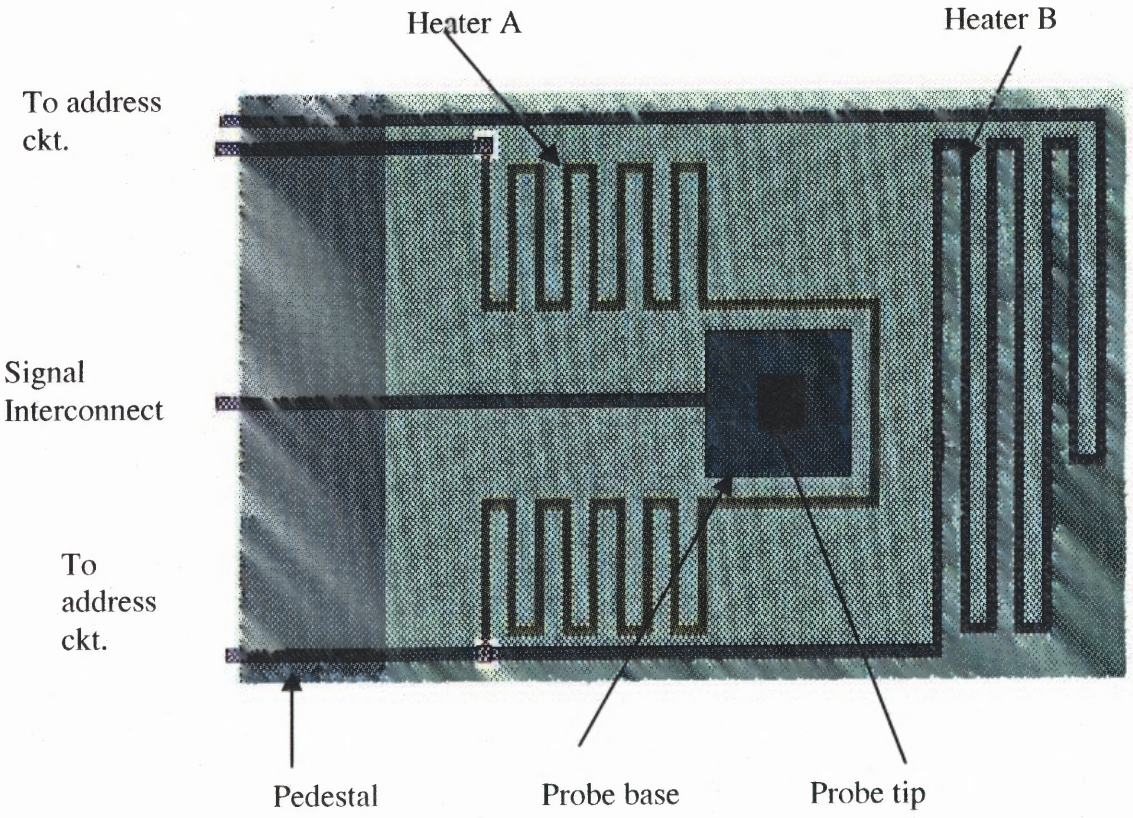


Figure 4.8 Layout of microstructure from L-EDIT

Figure 4.8 clearly shows the layout of the microstructure in LEDIT [9]. The heaters A and B are connected to the row and the column address circuits. The signal from the probe goes out of the pixel and connects to the bonding pad. The dimension of the structure is 300 μm x 210 μm as mentioned earlier. The different layers used in the layout of the microstructures are shown in Chapter 6.

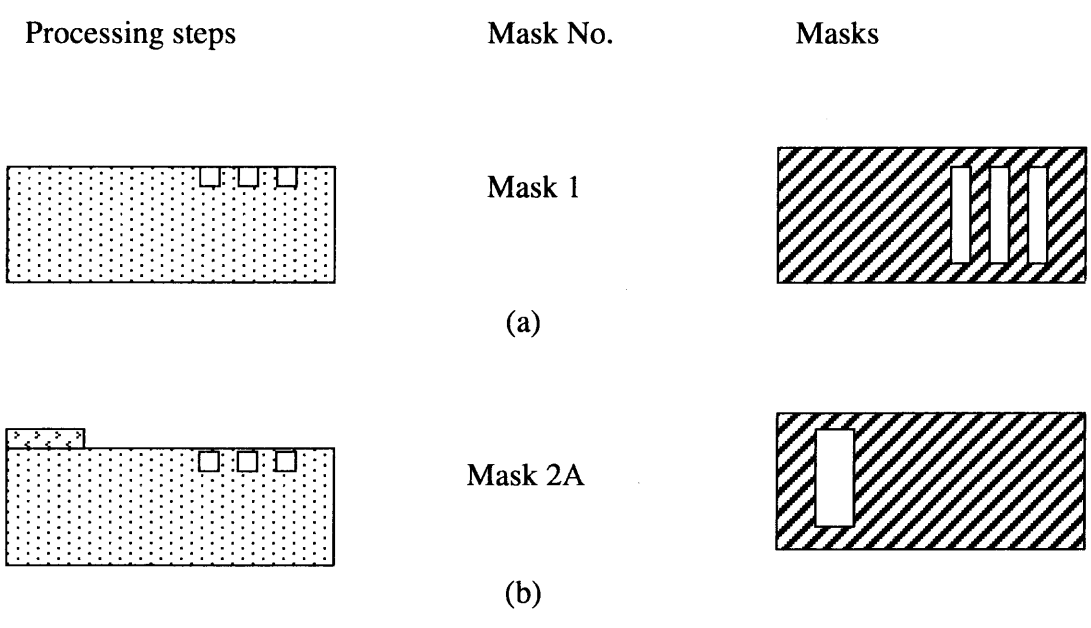
4.4 Fabrication Technique

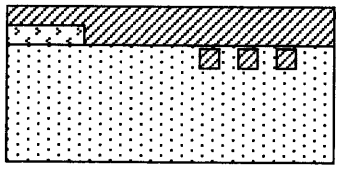
The previous section shows the desired layout of the microstructure. In this section, a feasible processing technique for the fabrication of MEMS pixels [10] is outlined. The layout of MEMS pixels in L-EDIT shows that there are nine layers of materials used. The number of masks required in this processing is eight. The starting material consists of single crystal Si substrate. This substrate is patterned and etched to form the latching grooves. The grooves are 2μm deep and are etched by SF_6 reactive ion etching (RIE). Refer to Figure 4.9a. After patterning the substrate, SiO_2 is formed by dry oxidation in a pure oxygen ambient. Then this layer is patterned with negative photoresist mask and etched with CF_4 RIE to create the pedestal of the cantilever beam (Figure 4.9b). On top of the SiO_2 layer, polyimide is deposited by spin-on technique. This will give, a planar surface for further processing steps and eventually act as sacrificial layer to be etched away at the end of the processing. The polyimide is planarized to the same level as the pedestal. This is done by sputtering (Figure 4.9c). The same mask can be used to pattern the pedestal and the polyimide sacrificial layer with a positive photoresist. This will save the expense of creating a separate mask for this layer. Next the aluminum layer is

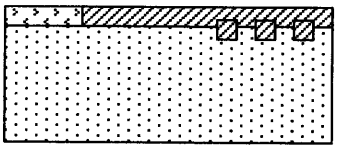
deposited by sputtering. In L-EDIT, this is METAL 3. The metal is patterned with heater-A mask, and etched (Figure 4.9d). The etching is done by Cl^+ RIE. The thickness of aluminum layer is 100 nm. On top of the Al layer, another layer of SiO_2 by PECVD technique is deposited (Figure 4.9e). This is done so that the deposition can occur at lower temperature below the melting point of aluminum. This would be 2μm thick, and would eventually form the cantilever beam. On top of this SiO_2 layer, another aluminum layer is deposited to form HEATER B after patterning and etching (Figure 4.9f). The next step is to pattern the SiO_2 cantilever beam. Then photoresist is deposited, and patterned to expose the area where the probe tip will be formed. The probe has four layers of metal stacked on top of each other. It is fabricated using two masks (Figure 4.9g). The first mask is for the base of the probe and the second mask is for the tip. The base is made up of aluminum deposited by sputtering, to a thickness of 1.5μm. The second mask for the tip has a small opening. This mask is used to deposit the gold tip which has a thickness of 2μm and is etched in a wet chemical ambient. The final step of processing is to create the air gap for the free deflection of the cantilever beam (Figure 4.9h). This is done by removing the polyimide sacrificial layer. This removal is done by cutting four access holes in the cantilever and isotropic O^+ plasma etching the polyimide layer. The access holes are created at the beginning of the process and the pattern in the mask for these holes can be used as alligners during the processing steps as well. There is also a mask for the via connecting the heater A to the wires of the address circuits. The following table (Table 4.4) lists the masks in sequence and Figure 4.9 shows the processing steps sequentially.

Table 4.4 List of masks in the fabrication of the microstructure

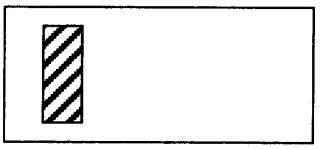
Mask Level	Processing Steps
1	Create grooves using RIE in silicon substrate
2A	Oxidize a SiO2 substrate and pattern for pedestal
2B	Spin-on polyimide and planarization
3	Aluminum sputter deposition and patterning into heater A
4	Via cut between heater A and heater B
5	Aluminum sputter deposition and patterning into heater B
6	Patterning the SiO_2 cantilever beam
7	Aluminum sputtered to form the base of probe.
8	Gold sputtered or electro deposited to form the probe tip.







Mask 2B



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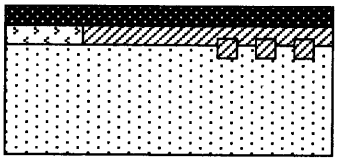
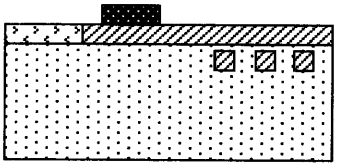
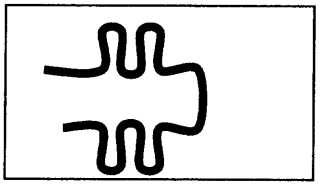




Mask 3



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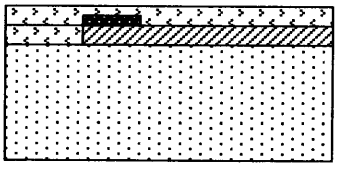

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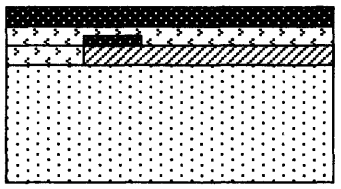

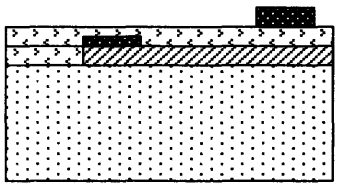

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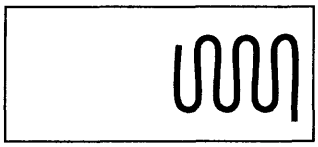

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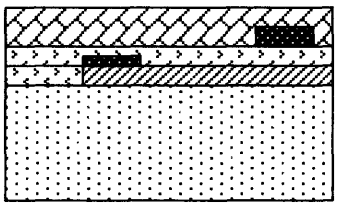

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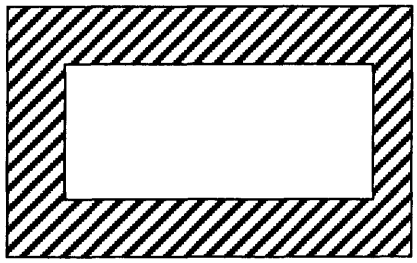
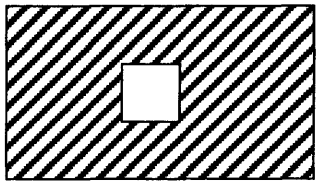
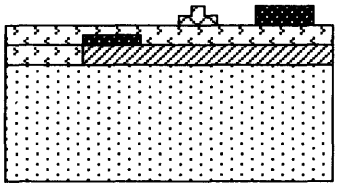
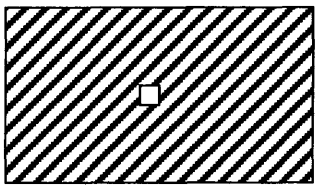


Mask 6





Mask 7



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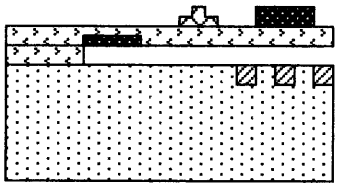


(h)

Figure 4.9 Graphical illustration of fabrication steps and masks required

4.5 Numerical Analysis

We know how much heat is required for the bending of our bimorph cantilever. The question is how much current is needed? This section explores the various calculations necessary to find the amount of this current.

4.5.1 Calculation of Cooling through Power Dissipation

The cooling rate of the cantilever beam is determined by three factors. These three are actually the powers dissipated through the microstructure. This power is equivalent to sum of the convection and radiation power dissipated by the beam [11, 12] and the conduction power dissipated by the aluminum wire over the support pedestal and the SiO_2 pedestal itself. Figure 4.10 shows how the remaining electrical power is converted to heat or thermal power which in turn is converted to mechanical power that will bend the cantilever. By ANSYS simulation in section 4.3 it was found that a temperature change in the heater from 300 °K to 500 °K gave a deflection height of about 60μm.

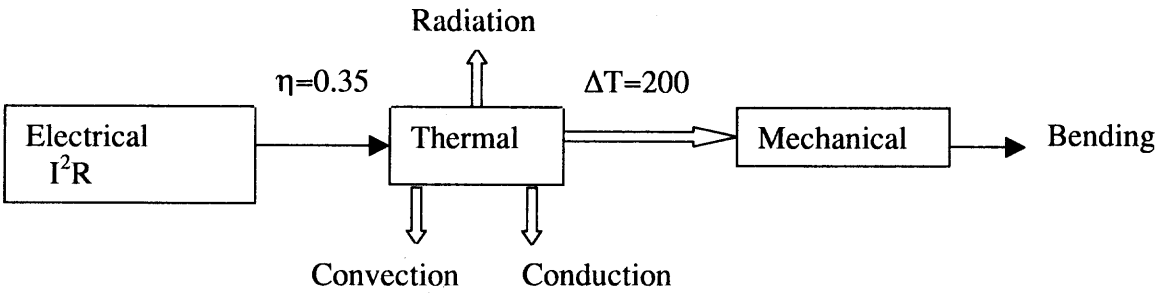


Figure 4.10 Block diagram of energy conversion in the system

The convection power is given by

$$P_{conv} = \kappa A \Delta T \tag{4.20}$$

where κ is coefficient of convection in SiO_2 and its value is 1.7E-9 J/(s.μm^2.K)

A is the area of the beam which is 300μmX210μm = 63000μm^2

ΔT = 200.

Using equation 4.20 it was found that the convection power P_{conv} = 21.42mW.

The Radiation power is given by Stefan-Boltzmann law

$$P_{rad} = \sigma A\, e(T^4 - T_0^4) \tag{4.21}$$

Where σ = 5.6696E-8 W/m^2.K^4

e = emissivity of SiO_2, assume 0.7

T = 500 °K

T_0 = 300 °K

Using equation 4.21 it was found that the radiation power P_{rad} = 0.136 mW for each surface.

Hence for two surfaces, P_{rad} is 0.27 mW.

There is also some power being dissipated by conduction through the support portion of the cantilever beam. This is through the aluminum wires on top of the pedestal and also through the SiO_2 pedestal. These are calculated as follows:

$$P_{Al} = A_{Al}\,\sigma_{Al}\,\Delta T \,/\, L_{Al} \tag{4.22}$$

Where A_{Al} is cross-sectional area of wire = 0.1μm x 6μm

σ_{Al} is Thermal conductivity of aluminum = $240 Wm^{-1}K^{-1}$

L_{Al} is the length of wire over the pedestal = 80μm

ΔT is the temperature difference = 200 °K

Using equation 4.22 it was found that P_{Al} = 0.36 mW for each wire. There are three wires over the pedestal excluding the signal line (See Figure 4.8). Hence the conduction power through the aluminum wires is 1.08 mW. Similarly, the conduction power through the SiO_2 pedestal is calculated.

$$P_{SiO_2} = A_{SiO_2}\,\sigma_{SiO_2}\,\Delta T \,/\, L_{SiO_2}$$

Where A_{SiO2} = 210μm x 2μm

$\sigma_{SiO2} = 1.5 Wm^{-1}K^{-1}$

L_{SiO2} = 80μm

Using the above values it is found that P_{SiO2} = 3.1mW. Hence the total conduction power is calculated to be

$P_{cond} = 3\,P_{Al} + P_{SiO2}$ = 1.08 + 3.1 = 4.2mW.

The total power dissipated in the form of heat is also the total power required for actuation of the cantilever to 200 °K in air. This is equivalent to:

$$P_{air} = P_{conv} + P_{cond} + P_{rad} = 25.9\ mW. \quad (4.23)$$

It can also be noted that the total power required for actuation of the cantilever to 200 K in vacuum is:

$$P_{vac} = P_{cond} + P_{rad} = 4.47\ mW \quad (4.24)$$

The amount of input power left after the total dissipation in the form of conduction, convection and radiation is finally converted to mechanical energy that results in the bending of the cantilever. *If it is assumed that the efficiency of the overall system is 35%, then the input power to the system is found to be approximately 40mW.*

4.5.2 Calculation of the Thermal Time Constant of the Cantilever

The thermal time constant in our system is equivalent to the RC time constant in an electrical system [12]. It is basically the time required for the cantilever to completely cool down. It is very crucial to know the thermal time constant τ because this will tell us the time after which the microstructure can be reconfigured for a new set of tests. In this section the approximate value of τ is calculated. The following parameters and their values will be used in subsequent calculations:

C_{Al} = specific heat capacity of aluminum = 100 JK^{-1} Kg^{-1}

C_{SiO2} = specific heat capacity of SiO_2 = 750 JK^{-1} Kg^{-1}

ρ_{Al} = density of aluminum = 2700 Kg m^{-1}

ρ_{SiO2} = density of SiO_2 = 2500 Kg m^{-1}

$V_{Al\_pedestal}$ = volume of the three aluminum wires on pedestal

= No. of wires x length of wire over pedestal x width of wire x thickness

= 3 x 80μm x 6μm x 0.1μm = 4.8×10^{-17} m^3

$V_{SiO2\_pedestal}$ = volume of SiO_2 pedestal

= length of pedestal x width of pedestal x thickness

= 80μm x 210μm x 2μm = 3.36×10^{-14} m^3

V_{Al_beam} = volume of the two aluminum heaters on the cantilever beam

= No. of heaters x length of a heater x width of a heater x thickness

= 2 x 1500μm x 5μm x 0.1μm = 1.5×10^{-15} m^3

V_{SiO2_beam} = volume of the SiO_2 cantilever beam

= length of beam x width of beam x thickness

= 300μm x 210μm x 2μm = 1.26×10^{-13} m^3

The time constant τ is given by the following formula :

$$\tau = \frac{\Delta E}{G_{thermal} \Delta T} \tag{4.24}$$

$$= \frac{\sum C \rho V \, \Delta T}{P_{thermal}} = \frac{\sum C \rho V \Delta T}{P_{cond} + P_{conv} + P_{rad}} \tag{4.25}$$

$$= \frac{\Delta T \left[\begin{array}{l} C_{Al} \rho_{Al} V_{Al\_pedestal} + C_{SiO_2} \rho_{SiO_2} V_{SiO_2\_pedestal} \\ \quad + C_{Al} \rho_{Al} V_{Al\_beam} + C_{SiO_2} \rho_{SiO_2} V_{SiO_2\_beam} \end{array} \right]}{P_{cond} + P_{conv} + P_{rad}} \tag{4.26}$$

$$\tau = \frac{200\left[1.3x10^{-11} + 6.3x10^{-8} + 4.05x10^{-10} + 2.36x10^{-7}\right]}{26x10^{-3}}$$

$$= \frac{5.988x10^{-5}}{26x10^{-3}}$$

$$= 2.3m \text{ sec}$$

Hence $\tau = 2.3$ *msec in air.*

In vacuum,

$$\tau = \frac{5.988x10^{-5}}{P_{cond} + P_{rad}} = \frac{5.988x10^{-5}}{4.47x10^{-3}} = 13.3\, m\,\text{sec}$$

In the above equations, $G_{thermal}$ is the total thermal conductivity and $P_{thermal}$ is the total thermal power in the system. The conduction, convection and radiation power for the above calculation was taken from section 4.5.1. The thermal time constant for actuation to 200 °K in air is found to be 2.3 m sec and that in vacuum is 13.3 m sec.

4.5.3 Calculation of Current and Resistance of the Heater

The DAC is indirectly the supplier of current in the circuit since it controls the amount of current that will flow in the circuit from the row driver. According to our design, the maximum length of our heater will be approximately 350 squares of aluminum. Aluminum was chosen as the material of the heater because of its convenience and high coefficient of expansion. The resistivity of aluminum $\rho(Al) = 27\ x10^{-2}\ \Omega$/square . The resistance of each heater is $350x27x10^{-2}=94.5\ \Omega$. A resistance of 100 ohms for design

and simulation purposes is used. From Sec.4.5.1, it is known that the required input power is 40 mW, and the resistance R=100 ohms, *the current to be delivered to the microstructure by the DAC should be* $I = \sqrt{(P/R)} = 20\ mA$ *to cause a* $\Delta T=200\ ^{\circ}K$. This is based on using aluminum of thickness 100nm for the heaters.

4.6 Summary and Conclusion

In this Chapter, the MEMS cantilever based on ANSYS simulation has been designed. The results were verified by using a simple theoretical analysis. Also a feasible sequence of fabrication, based on standard MEMS processing techniques is discussed. Also, based on simple energy flow, the power requirement of the heater assuming 35% efficiency is found to be 40mW and the corresponding current in each heater is about 20mA. In the next chapter the addressing circuits that will deliver the cantilever the required power and current found in this Chapter, are designed.

CHAPTER 5

DESIGN AND SIMULATION OF CMOS ADDRESSING CIRCUITS

In this chapter, the components of the row and column address circuits as shown in the block diagram of Figure 3.1 in details, will be designed. The design and physical layout using LEDIT is illustrated. Finally the combining of the components into the row and column address circuits are shown.

5.1 The Shift Register

5.1.1 Circuit Schematic and Analysis

The shift register circuit is used in both the row and column address circuits. The design chosen for this shift register is a two-phase non-overlapping clocked design [13]. The design was done such that 3-bits of data could be shifted simultaneously in the column addressing circuits at every clock cycle. In other words, each column consists of three shift registers. The row, however, shifts only one bit at each clock cycle, and hence only one of the shift registers in the addressing circuits are utilized.

Figure 5.1 shows the schematic of a 1-bit shift register. This circuit is cascaded to form the 3-bit shift register required in this thesis. CMOS logic was used to design this circuit. The Sin bit shown in the figure is the input and Sout is the output, which would be the input for the next bit. The 'D' bit carries the same information as the Sout, but it takes the information into the DAC in the column circuit and to the gate of the row driver in the row circuit. The SSR1 bit acts as an enable. In our case, it is always high.

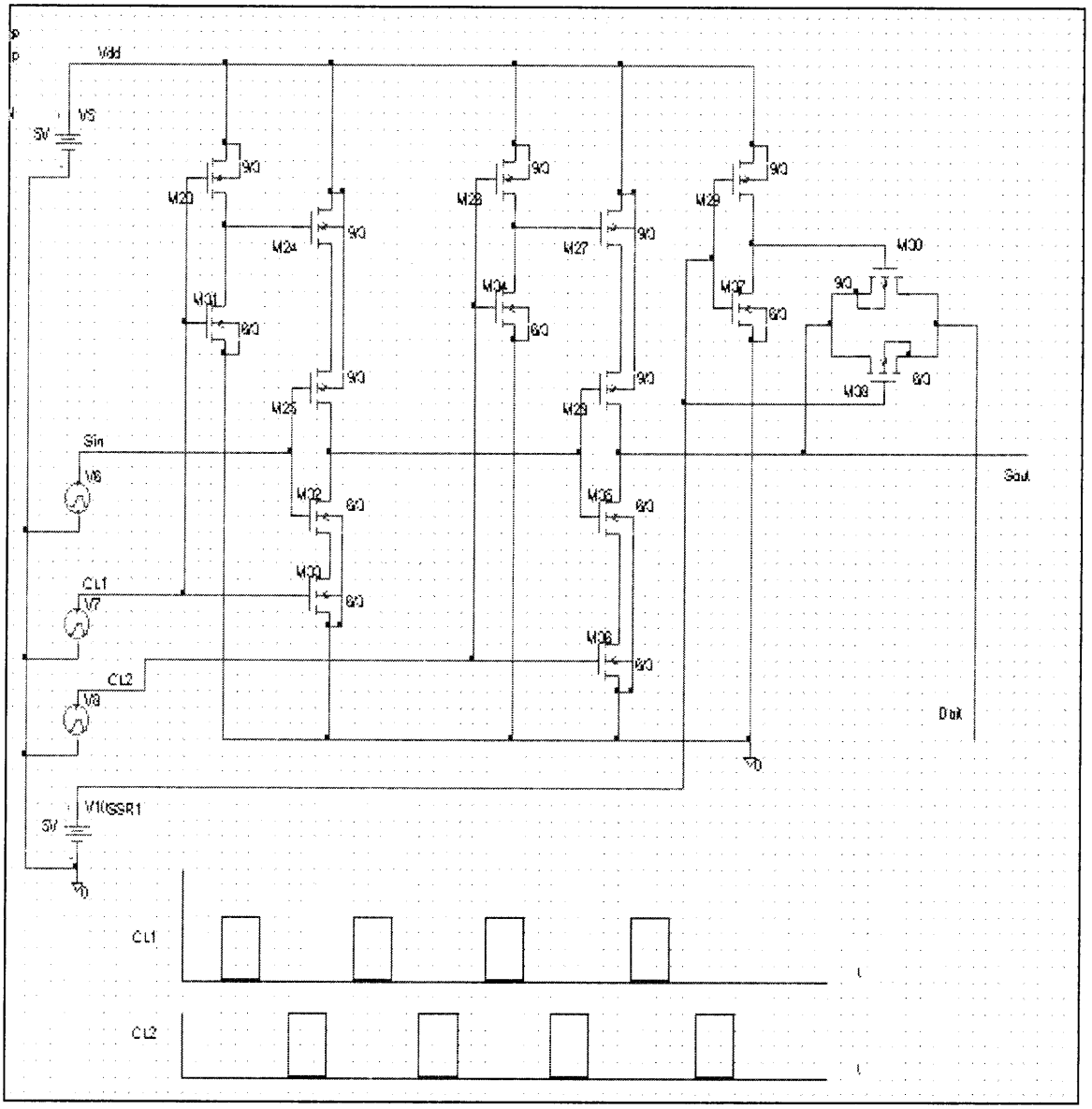


Figure 5.1 Schematic of a Shift register cell from PSPICE (Corresponding to block A of Figure 3.1).

5.1.2 Simulation Using PSPICE

Figure 5.2 shows the simulation of the one bit shift register illustrated in Figure 5.1. The simulation was done using the software PSPICE [14, 15].

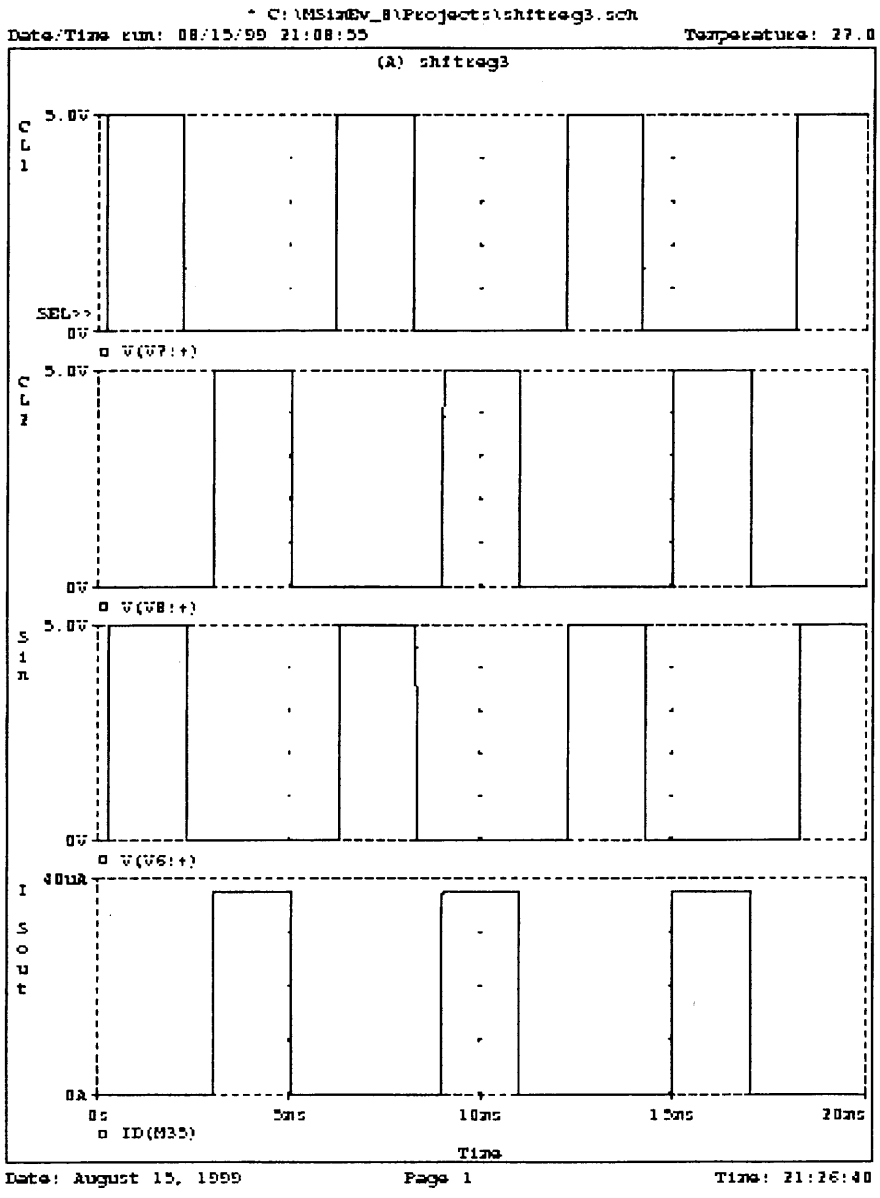


Figure 5.2 Simulation of the shift register cell using PSPICE.

5.1.3 Physical Layout of Shift Register

Since the electrical integrity of the circuits is demonstrated, now the layout of the circuit is considered. All physical layouts of the CMOS circuits are done using p-well 3μm technology [16]. Figure 4.3 shows the layout of the 3-bit shift register. The layout was done using the software LEDIT from Tanner research Inc. [9, 16]. In this design, the first bit was laid out shown in the Figure as A and flipped to form the 2_{nd} bit of the shift register, represented by B in the Figure 4.3. This was done to avoid one ground bus. By implementing this technique, a common ground bus can be shared by two bits of the same shift register. After the two bits, the two clock lines were laid out and then the 3^{rd} bit represented by C in the figure was laid out. The bits marked as D0, D1 and D2 are the shifted bits that will form the inputs to the DAC in the column circuit. Only D0 is taken in the row circuit. Appendix A describes the design rules used in this and all other subsequent layouts. The different layers used in LEDIT are also outlined. The number of mask levels used for the fabrication of the CMOS circuits is twelve. The layers used in LEDIT to layout all the CMOS circuits are shown in Chapter 6.

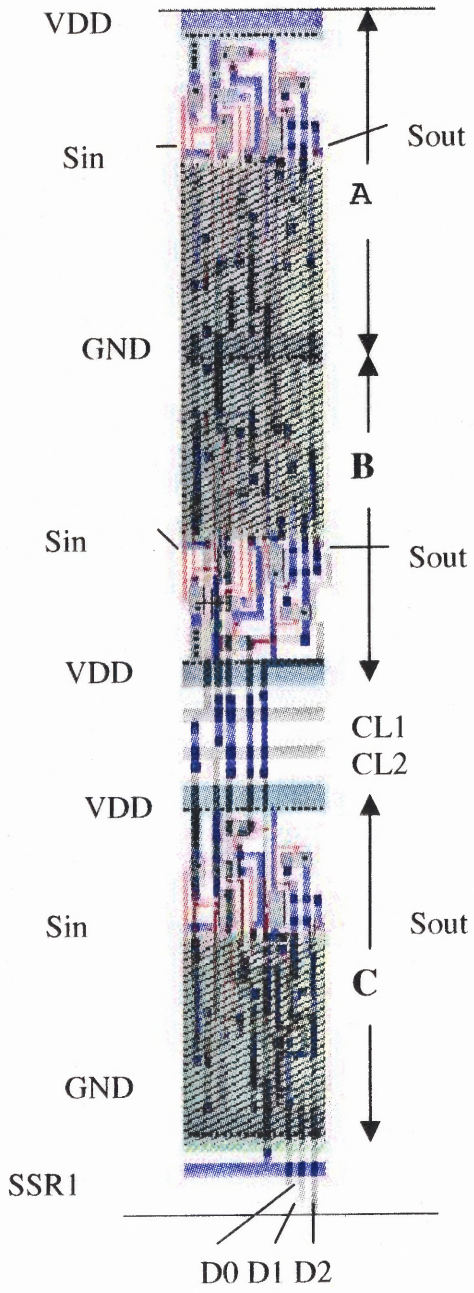


Figure 5.3 Physical layout of the 3-bit shift register in L-EDIT

5.2 Digital to Analog Converter

5.2.1 Circuit Schematic and Analysis

The digital to analog converter is used only in the column addressing circuit (See Figure 3.1, block B). It is a 3-bit DAC. The inputs to this DAC are the 3-bits being shifted in the shift register (Figure 5.3). The DAC converts these bits into a specific output current value. Hence the shift register along with the DAC controls the amount of current flowing into the MEMS pixel and in turn controls the amount of bending of the cantilevers. Figure 5.4 shows the schematic of the DAC done in PSPICE.

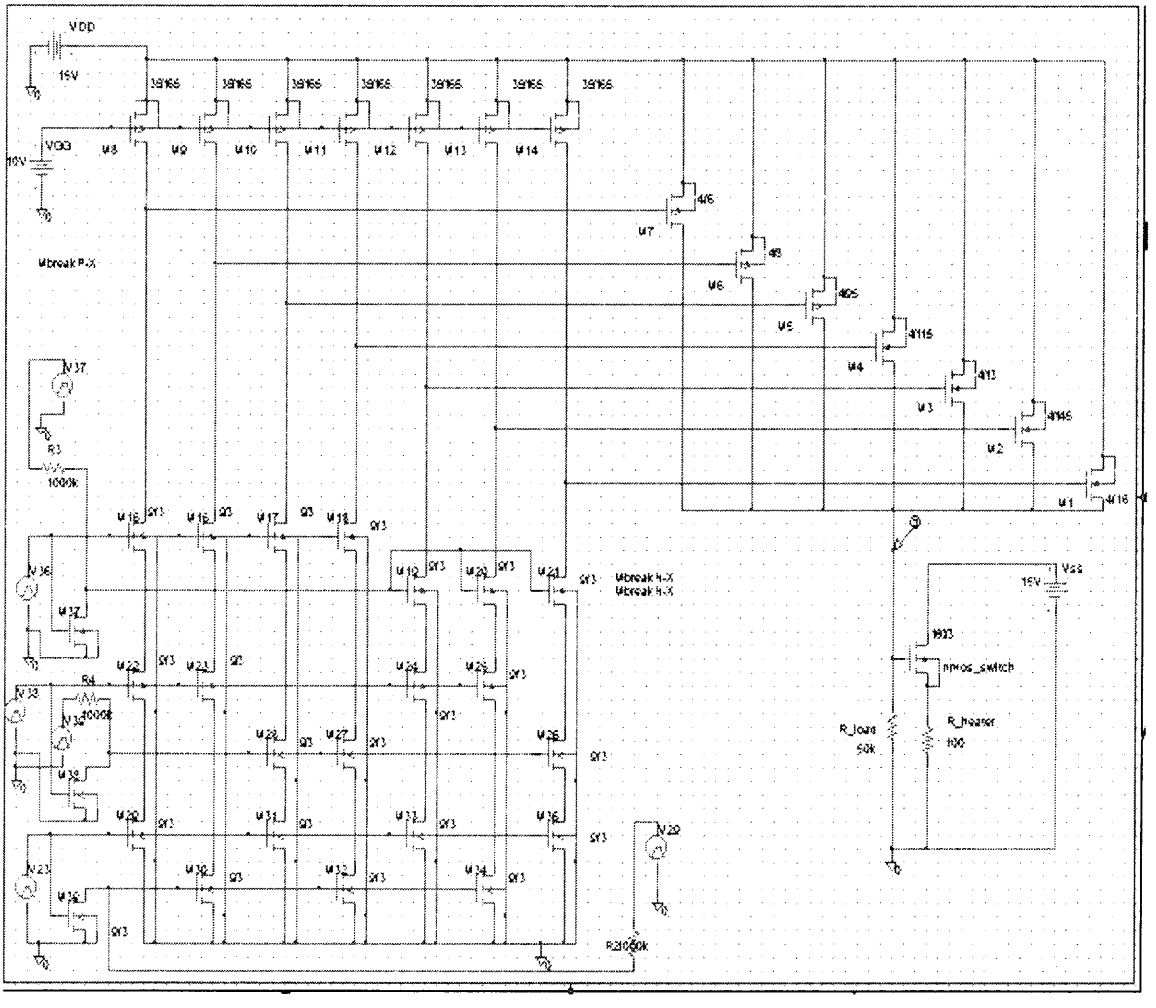


Figure 5.4 Schematic of DAC circuit in PSPICE

The design of DAC consists of 41 transistors. 17 of them are PMOS and the rest are NMOS. There are three voltage sources in the circuit namely, VDD, VGG, and Vss. (See figure 5.4). The sources A, B, and C are the outputs of the shift register D0, D1 and D2. VDD, VGG, and VSS are 15V, 10V, and 15V respectively. The size of the transistors were chosen according to the required performance of the circuit. The transistor M1 has the largest length and M7 has the shortest length. M7 will be turned on when the input to the circuit is 111. This will allow maximum current to flow into the pixel. In Figure 5.4 there are two resistances. The resistance R5 represents the resistance of one of the heaters in the pixel and its value is 100Ω. The resistance R1 is the load resistance of 50k that was placed in the circuit to get a full swing of the voltage at the output circuit. The W/L ratio of the NMOS switch transistor is 160/3. When this switch is ON, the current flows from the VSS source in the row address circuit through the switch and into the heater.

5.2.2 Simulation Using PSPICE

The following two plots, Figures 5.5 and 5.6 were obtained by simulating the DAC circuit with PSPICE. It can be seen that the maximum current in the circuit is 30mA which clearly fulfills the requirement of this design.

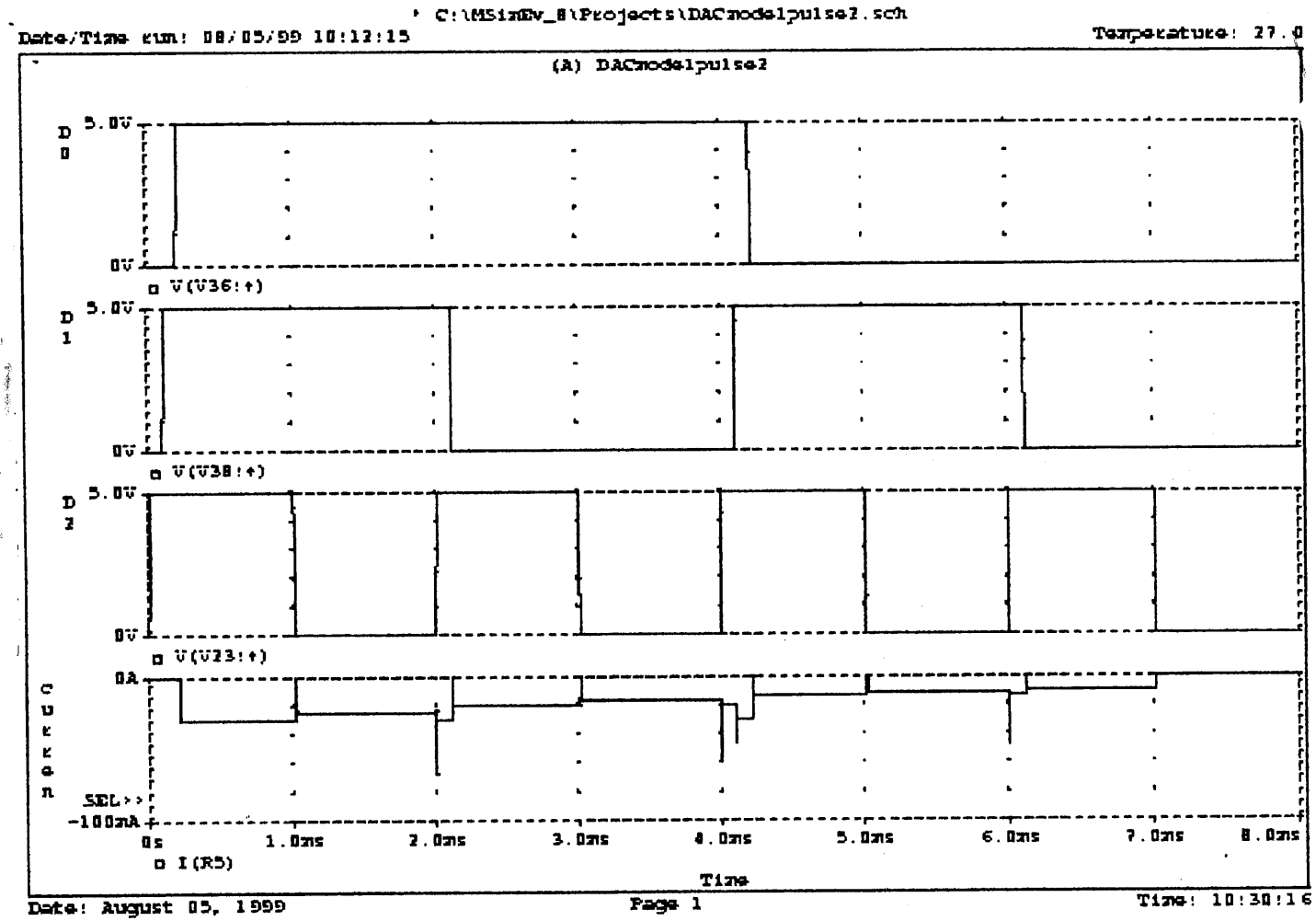


Figure 5.5 Simulation of DAC in PSPICE

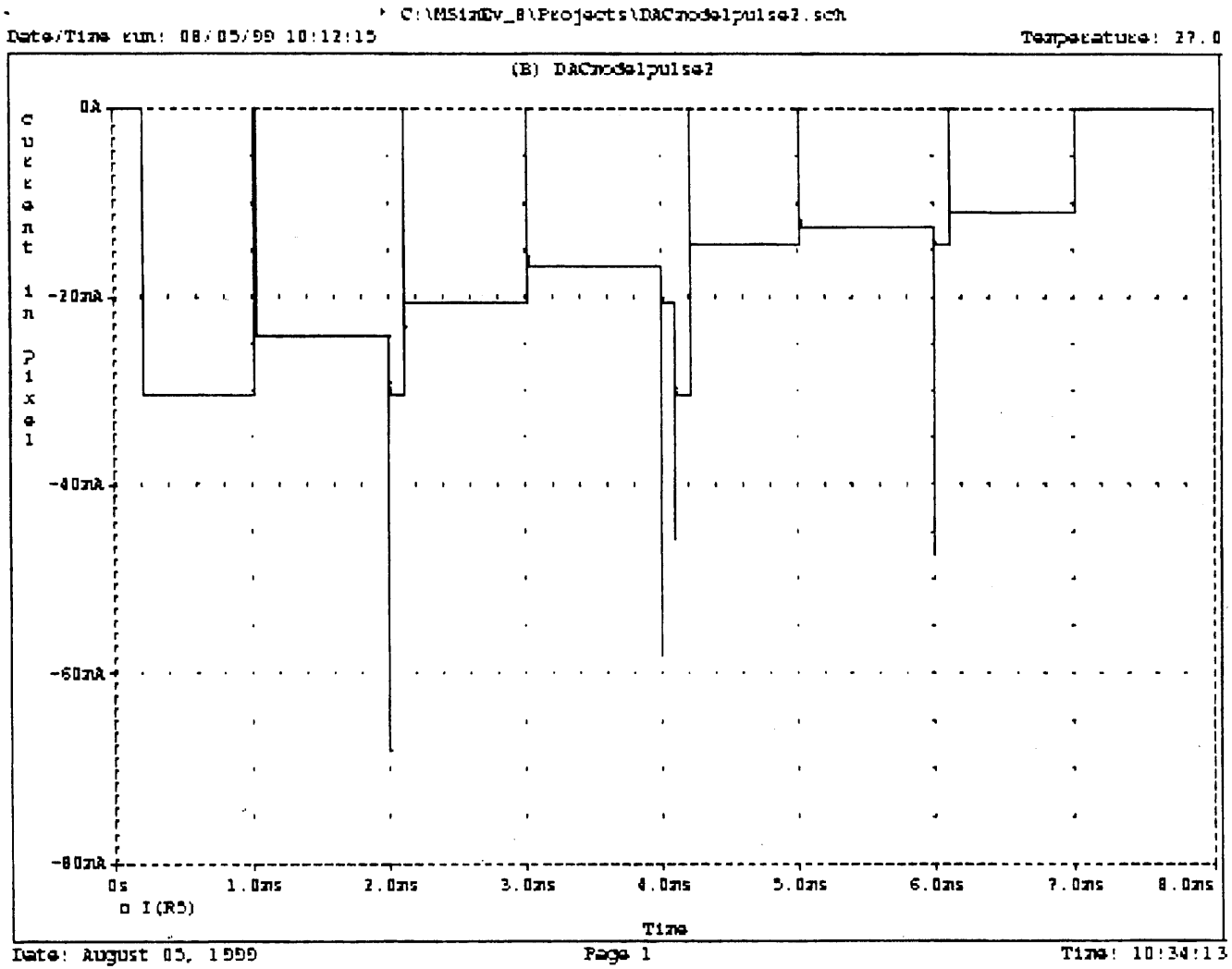


Figure 5.6 Current in the DAC circuit

5.2.3 Physical Layout of the Digital to Analog Converter

Figure 5.7 shows the physical layout of two digital to analog converter (DAC) circuits in L-Edit. This segment of the circuit marked as **A** represents one DAC circuit. The other DAC circuit is a flipped version of **A**. The PMOS transistors M1 through M7 are also shown in Figure 5.7. The line marked as **I** carries the analog current of the DAC. The current flows from the **Vss** bus which is the part of the row driver described in the next section.

The reason for designing two DAC is that two column address circuits for each pixel are needed. This is because each of the **I** outputs are connected to each of the heater in a single pixel through an NMOS switch. Once again, these separate heaters allow for greater flexibility in terms of deflection of the cantilever beam.

The layout of the NMOS switch and the load resistance are not shown in Fig. 5.7. They will be shown in Chapter 6 in the final layer. The switch is just and NMOS transistor with a W/L ratio of 160/3. The resistance was laid out with seventeen squares of p-well. P-well was chosen because of its high resistivity of 3000 ohms/square.

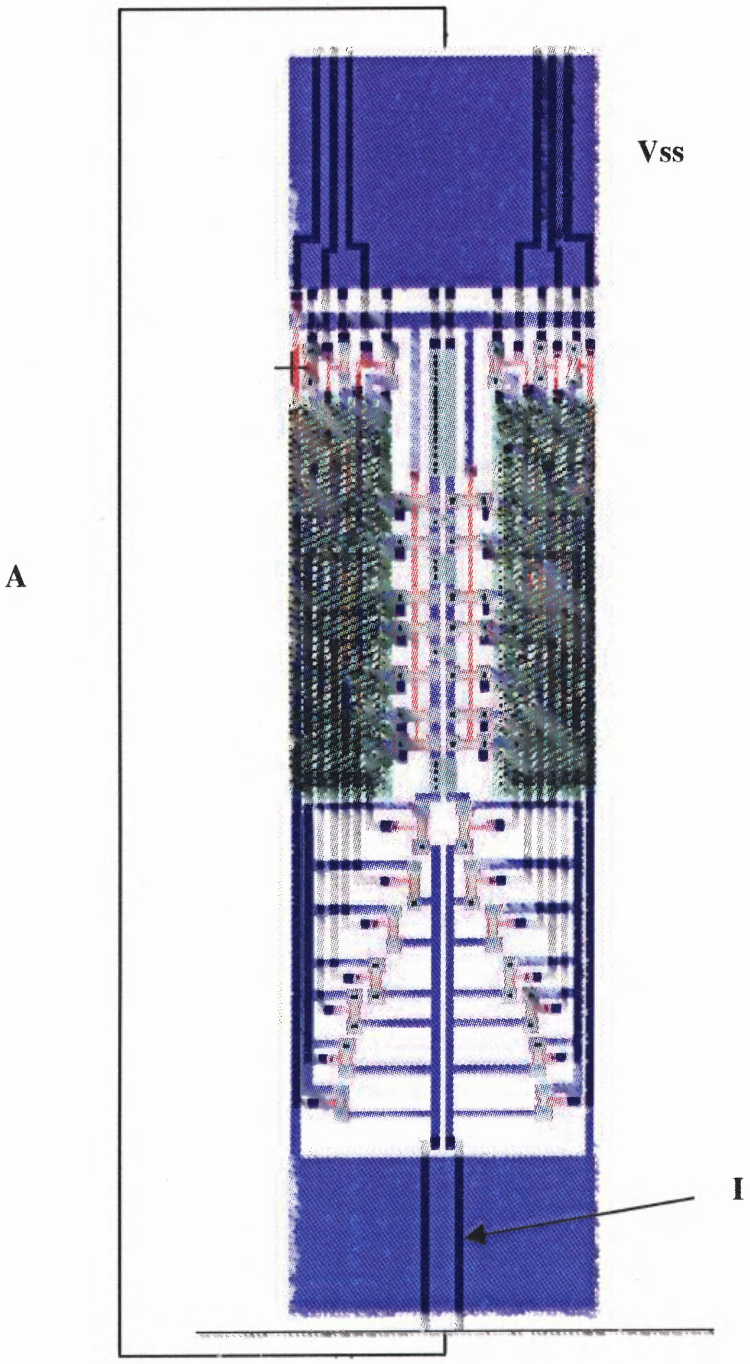


Figure 5.7 Layout of the two DAC circuits in L-EDIT. One is the mirror image of the other.

5.3 Row Driver and Poly Resistor

5.3.1 Description of Circuit

The row driver is a large PMOS transistor placed in the row addressing circuit. This is to handle large amount of current that will flow through this transistor and into the heaters of the MEMS pixels. The current is large because it is the collection of all the current flowing through each of the MEMS pixels in that particular row. The switching on and off of the row driver is controlled by the shift register, which is connected to the gate of the row driver. The current from the pixels flow through the source connected to VSS bus which is 15V and out the drain which is connected to the drain of the NMOS switch. When there is a valid input into the column address circuit, the switch is closed and current flows into the heaters. The row resistor **R** is used as a pull-up resistor. It is made up of polysilicon. It is 900μm in length and 3μm wide. Figure 5.8 shows a simplified schematic of the circuit configuration. Detailed operation of the circuit is discussed in Sec. 5.4.

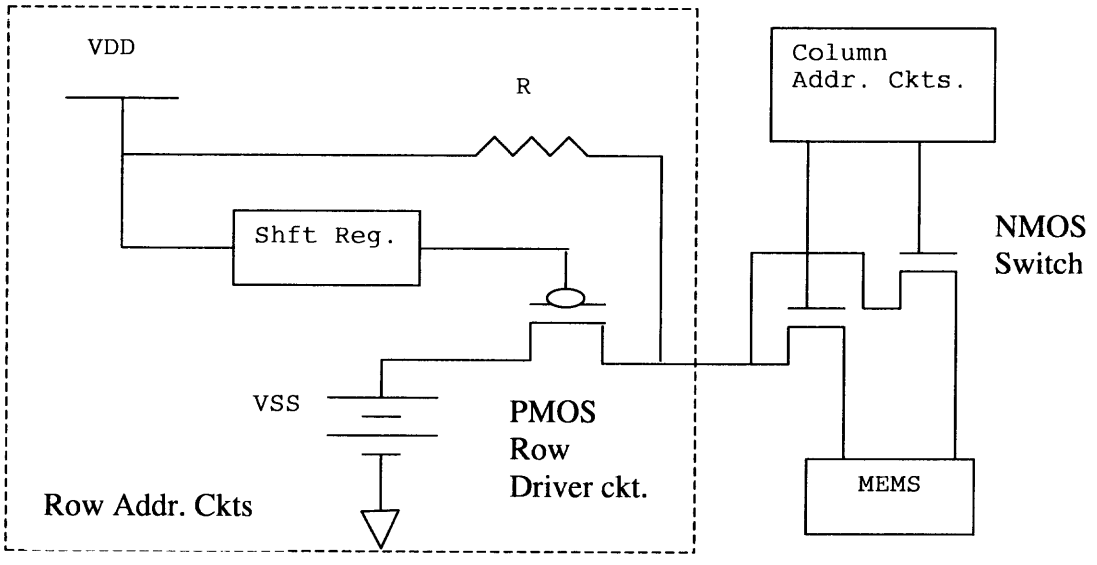


Figure 5.8 Schematic showing the arrangement of row address circuit

5.3.2 Physical Layout of the Row Driver

Figure 5.9 shows the layout of the row driver drawn using L-Edit. As shown in the Figure, the gate of the transistor is connected to the shift resister. This gate is a polysilicon serpentine structured gate. The drain is connected to the MEMS pixel at one end and to the polysilicon pull-up resistor on the other end. The source (the portion of the transistor outside the polysilicon gate) is connected to the Vss bus. If the pixel dimension were 100μm by 100μm, then the row driver circuits could link each other without any difficulty. The cutouts then mesh with each other perfectly. The W/L ratio of this transistor is 3/900. The reason for the large size of this transistor is that this transistor produces the current that will flow through the activated heaters of all the selected pixels in a row. So, if all the heaters in a single row are selected, the row driver will have to supply a total of 160mA of current since the two heaters in each pixel require a total of 40mA of maximum current.

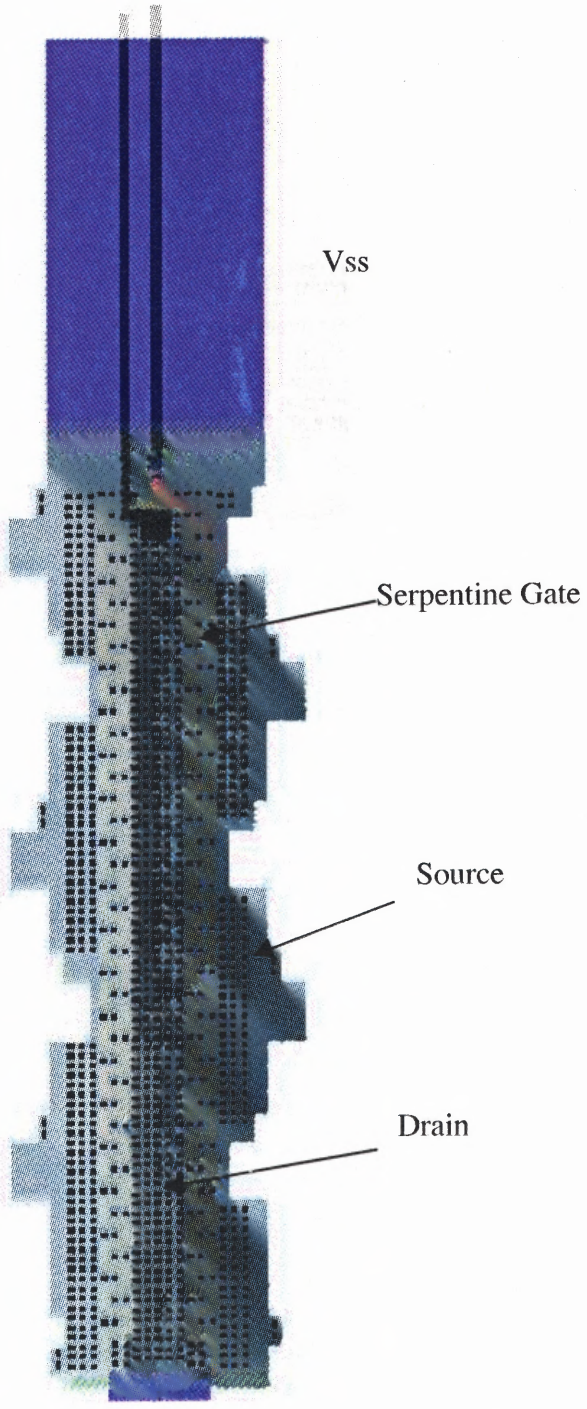


Figure 5.9 Layout of PMOS Row Driver transistor

5.4 Sub-circuit Driving Current in the Pixel

The sub-circuit described in this section can be viewed as a circuit combining the row and column address circuits. Part of it is connected to the DAC in the column address circuit and part of it to the row driver in the row address circuit. The simulation of this sub-circuit is done in PSPICE to see if the heaters in the pixel are getting enough power for the maximum deflection of the cantilever beam. As mentioned in Chapter 4, the required power is 40mW. The current flowing through the heaters in the pixel is being controlled by the DAC and is supplied by the Vss bus in the row circuit. Figure 5.10 shows the schematic of the sub-circuit simulated in PSPICE.

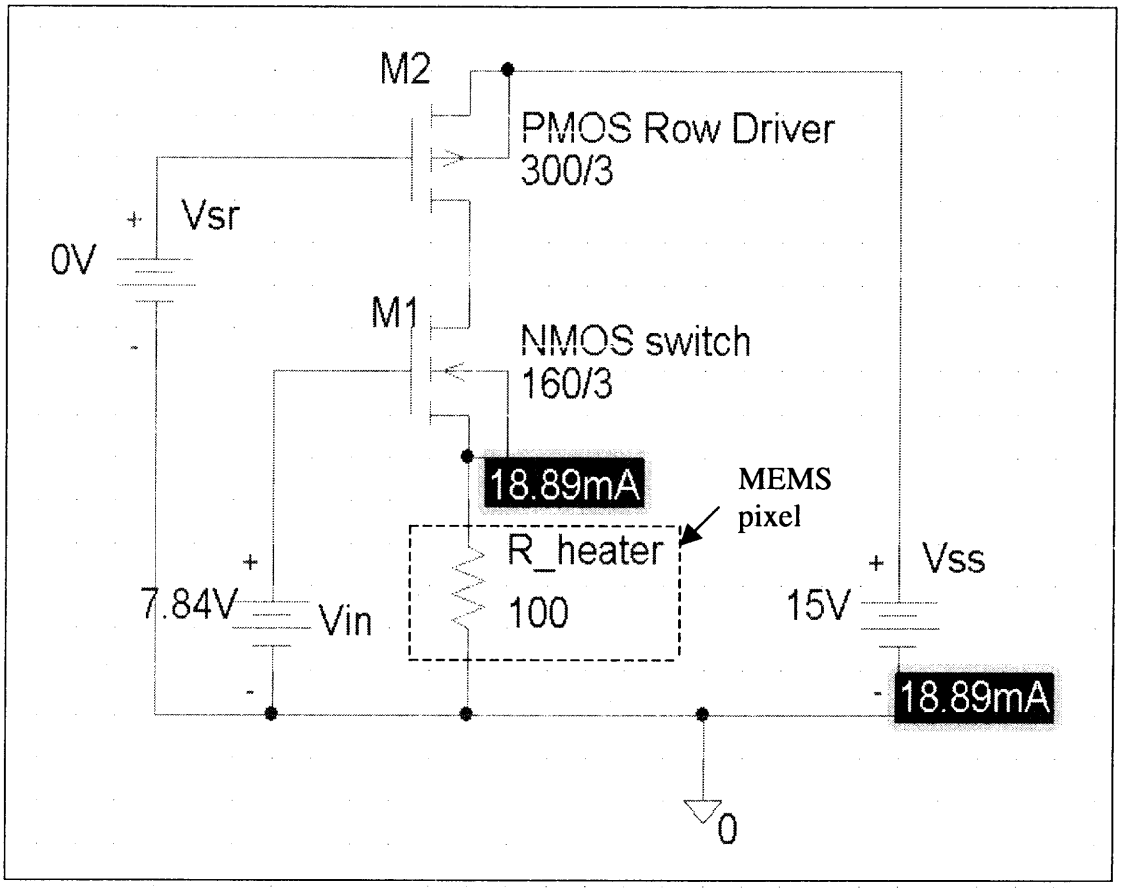


Figure 5.10 Schematic of sub-circuit supplying current in the pixel heaters

The circuit in Figure 5.10 was simulated with different Vin values and the corresponding current and power in the pixel was tabulated. Table 5.1 shows the results of the simulation. Here I_H represents the current in one of the heaters in the MEMS pixel and P_H represents the total input power in the pixel.

Table 5.1 Simulation Results of the sub-circuit

DAC Input	Vin (Volts)	I_H (mA)	P_H (mW)
000	5.25×10^{-6}	15.03×10^{-9}	2.25×10^{-14}
001	4.658	7.956	6.3
010	4.989	8.942	8.0
011	5.356	10.08	10.2
100	5.77	11.42	13.04
101	6.406	13.59	18.46
110	6.956	15.56	24.2
111	7.840	18.89	35.68

The Vin values are got by simulating the DAC circuit separately. During that simulation the load resistor of 50KΩ was included. Hence the values of Vin include the load resistor simulation. From the table it can be seen that the maximum current flowing through the heater is when the DAC input is 111 giving a maximum power of 36mW that meets our requirement of approximately 40mW adequately.

5.5 Combining Row and Column Address Circuits

The current components described in the previous section were combined to form the row and column address circuits. Figure 5.11 below shows a simplified schematic of the whole circuit including column and row addressing circuits. In the following sections Figure 5.11 will be referred to, to illustrate the operation of the circuit.

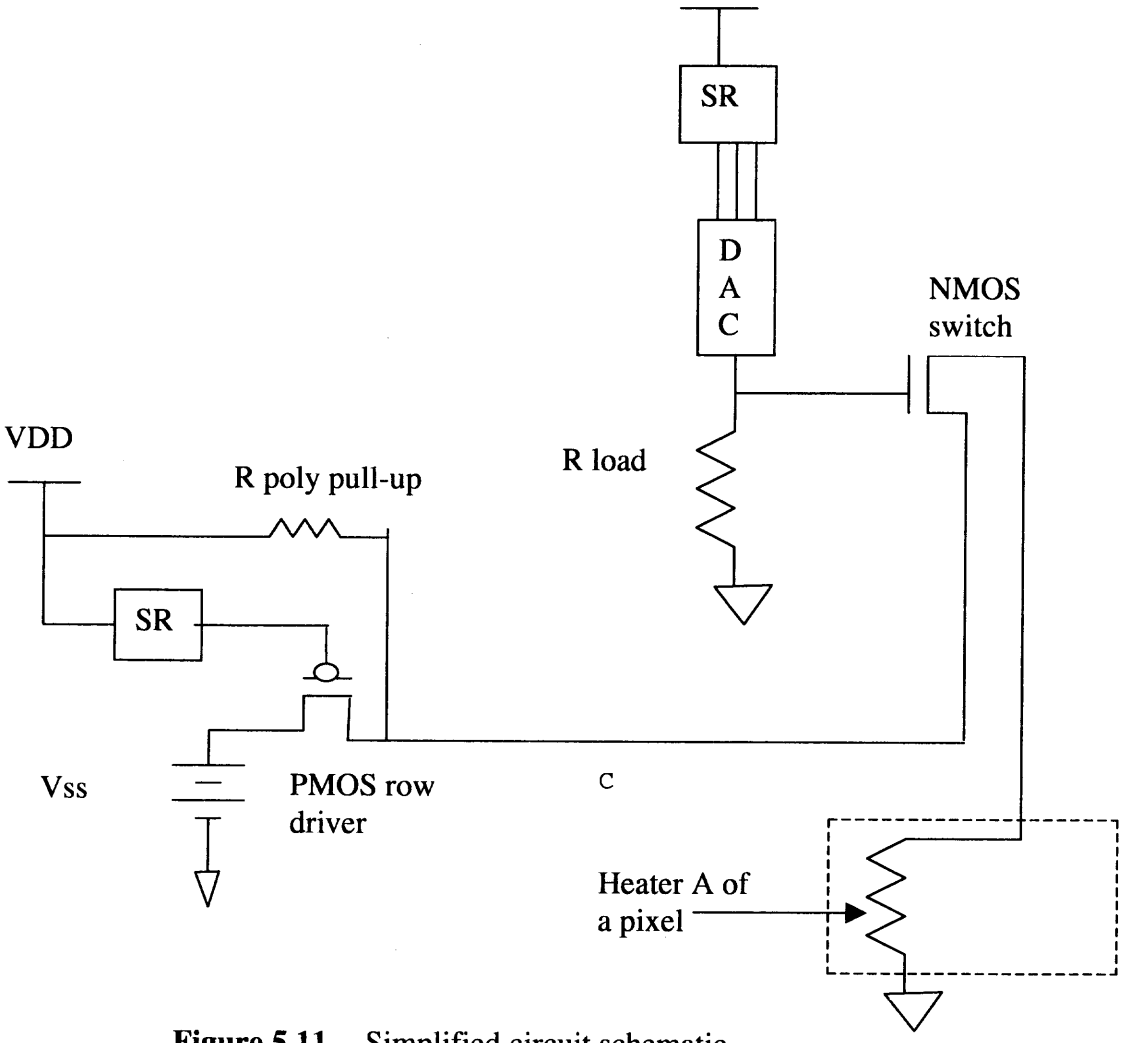


Figure 5.11 Simplified circuit schematic

5.5.1 Description of Row Address Circuit

The row address circuit consists of a one-bit shift register, the polysilicon resistor R and the row driver. The drain of the row driver PMOS transistor is connected to the resistor R and the drain of the NMOS switch, the source of which is connected to one of the heaters (A or B) in a microstructure. The gate of the row driver is connected to the shift register and the source is connected to the Vss bus, which is at 15V. Figure 5.11 shows the schematic of the arrangement.

When the SR in the row circuit has a value of 0, it switches on the PMOS row driver. Current will flow from the Vss bus to point C. The amount of this current is controlled by the input values to the shift register in the column address circuit. If the value is 000, the NMOS switch is open and no current will flow. If it is 111, the NMOS switch is closed and maximum current will flow through the heater. This current is of large amount as it flows through all the heaters in all the pixels in the selected row.

5.5.2 Description of Column Address Circuit

The column address circuit consists of a 3-bit shift register and the D/A converter. The data being shifted in the shift-register is the input to the DAC. This value determines the amount of current that will flow from the row address circuit into the MEMS pixel. As mentioned in the previous section, the maximum current that will flow is when the SR register output is 111. When the SR register output is 000, no current will flow. The range of the current change between 000 and 111 will not give maximum deflection to the cantilever in the pixel but will control the height of the probe point. This can be used for testing wafers during fabrication in non-planarized surface. For testing the final chip,

which is the goal of this project, only the two extreme values are required which are 000 and 111. The maximum required current through each pixel is found to be approximately 40mA. This current will deflect the cantilever by 60 to 80 μm as per system specification. The shift register values are shifted serially to consecutive columns. Depending on the SR programmed values in the row circuit, 0 or 1, a particular row of pixels is activated.

5.5.3 Physical Layouts of Combined Cells

The layout process using L-Edit was described in the previous sections. The separate circuit components were instanced, combined and connected to get the corresponding row and column address circuits. Figure 5.12 shows the row address circuits. The segment of the circuit marked **A** is the shift register, **B** is the polysilicon resistor, and **C** is the PMOS row driver transistor.

Figure 5.13 shows the column address circuit. The segment of the circuit labeled **A** is the shift register and that marked as **B** is the DAC. In this figure, note that two shift registers and the DAC are used to drive the two separate heaters in the pixels.

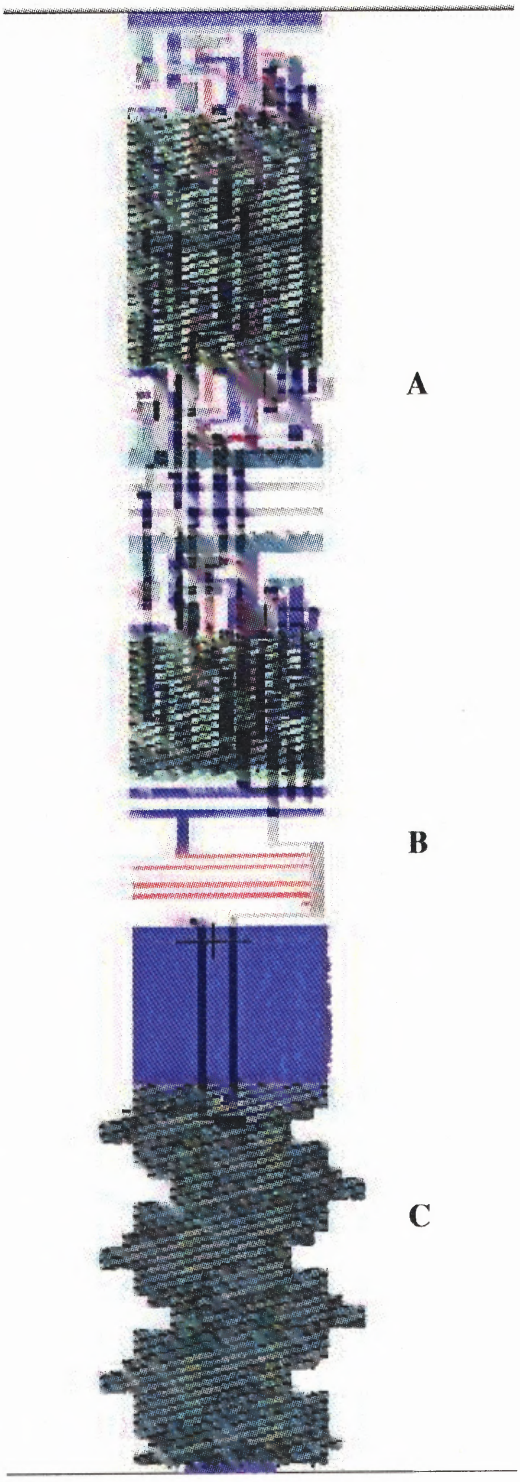


Figure 5.12 Layout of row address circuit

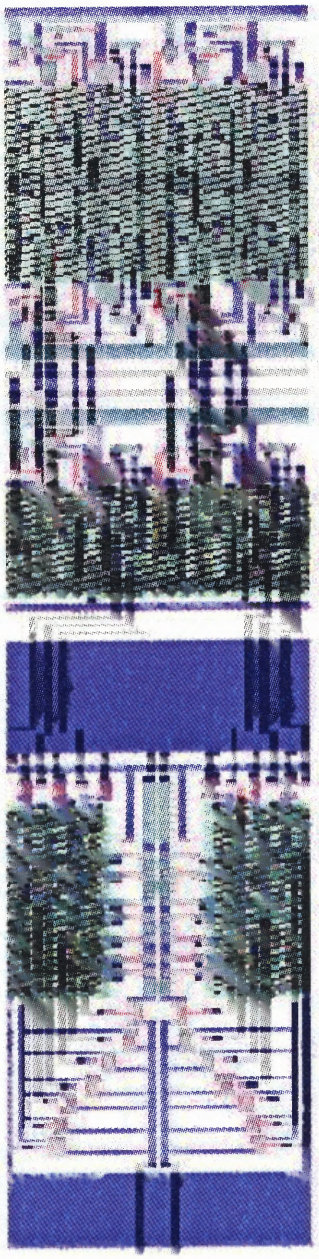


Figure 5.13 Layout of two column address circuits, one the mirror image of the other.

5.6 Summary and Conclusion

In this Chapter, the addressing circuits that are used for programming the MEMS pixel has been designed. PSPICE simulation was done on each of the circuit components to check their functionality separately. The D/A converter along with the NMOS switch, the load resistor, heater and the row driver was simulated using PSPICE as well. This showed the total amount of current flowing through the heaters to be meeting the requirement. The corresponding layouts of each of the components are also illustrated. In the next chapter, the addressing circuits and the MEMS pixel will be combined into a 4x4 array of probe card and the layout of the final chip will be shown.

CHAPTER 6

THE INTEGRATED CMOS AND MEMS CELL

In this chapter, the CMOS circuits are integrated with the MEMS pixels that were developed in Chapters 4 and 5, respectively. Since CMOS and MEMS circuits have their unique layout characteristics, the integration process is important for the overall success of the chip design. Before illustrating the integrated chip, all the successive mask levels used in the layout of the CMOS circuits and MEMS microstructure will be shown. From the CMOS circuits, as an example, the shift register circuit was chosen to show its layout layers separately and in composite.

6.1 Layout Masks for the CMOS Shift Register

In this section the separate layers of the CMOS shift register will be illustrated separately and in composite. Figure 6.1 shows the list of the layers used in LEDIT for the layout of the CMOS circuits. Figures 6.2a through 6.2k show the mask layers separately and 6.3 shows the circuit in composite.

Figure 6.1 List of Layers used in LEDIT to layout the CMOS circuits

Figure 6.2a P-well layer for CMOS shift register circuit

Figure 6.2b Active layer for CMOS shift register circuit

Figure 6.2c N channel field implant layer for CMOS shift register circuit

Figure 6.2d P channel field implant layer for CMOS shift register circuit

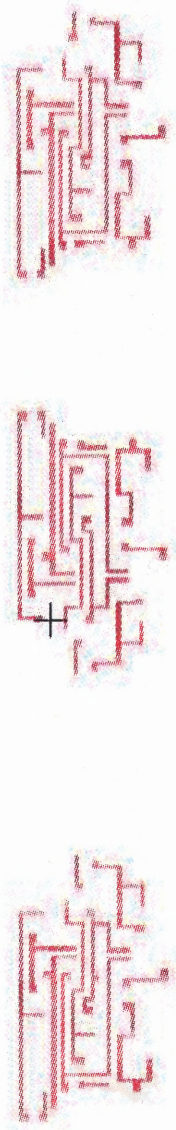


Figure 6.2e Polysilicon layer for CMOS shift register circuit

Figure 6.2f N+ source/drain layer for CMOS shift register

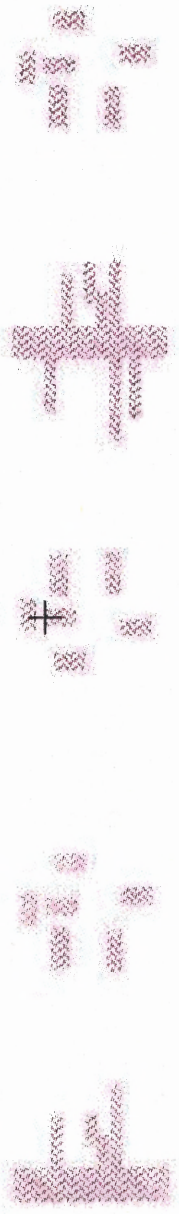


Figure 6.2g P+ source/drain layer for CMOS shift register

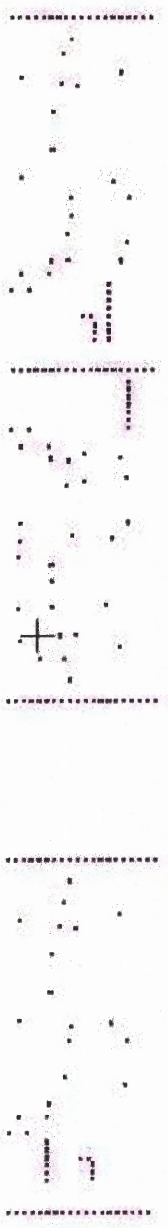


Figure 6.2h Contact layer for CMOS shift register circuit

Figure 6.2i Metal1 layer for CMOS shift register circuit

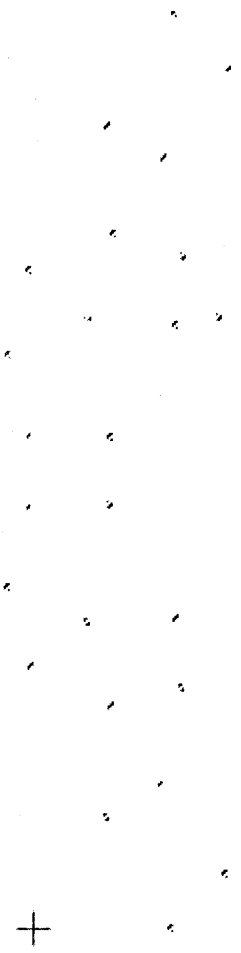


Figure 6.2j Via layer for CMOS shift register circuit

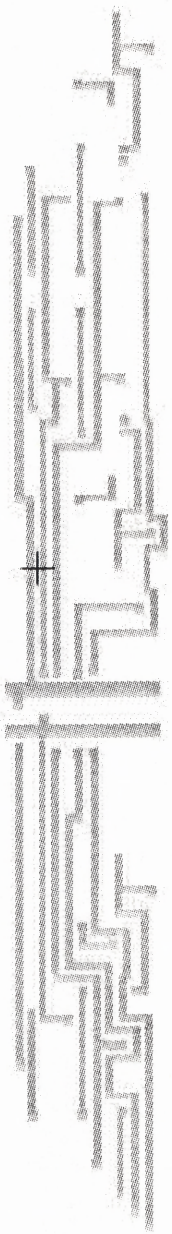


Figure 6.2k Metal2 layer for CMOS shift register circuit

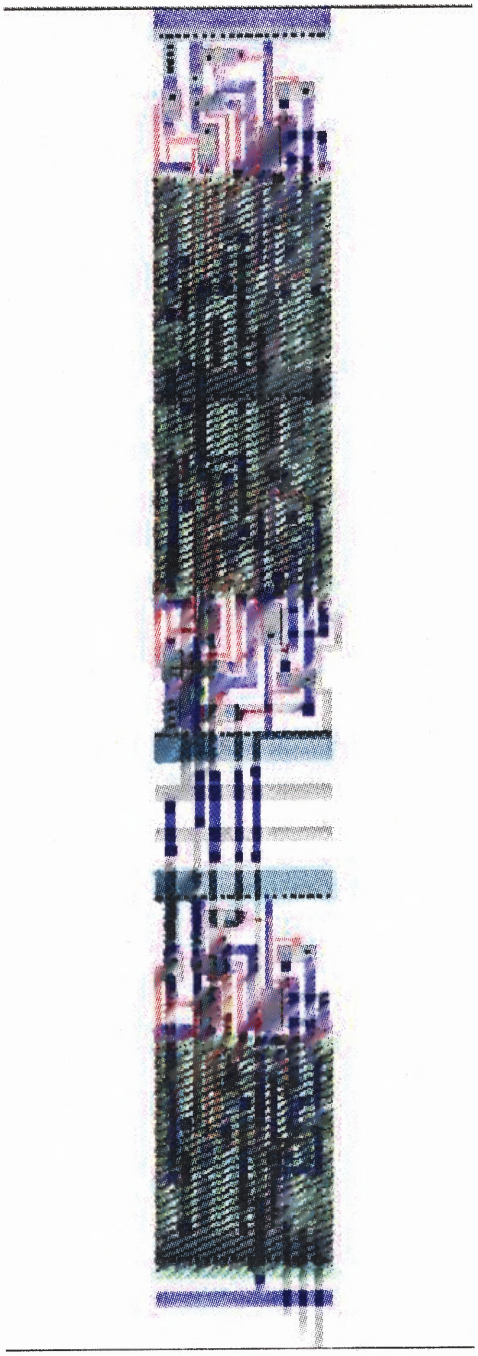


Figure 6.3 The composite CMOS shift register circuit

6.2 Layout Masks for the MEMS Structures

In this section, the layout mask layers of the MEMS structures are shown separately and in composite just as it was done for the CMOS shift register in the previous section. The MEMS structures needed a whole new set of layers as shown in Chapter 4.

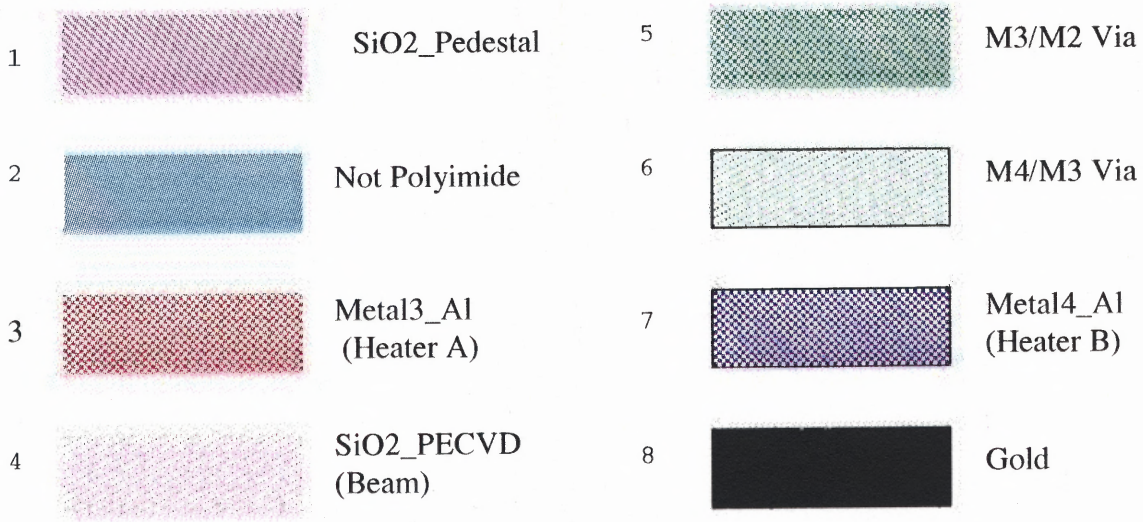


Figure 6.4 List of layers in LEDIT for the layout of the MEMS structures

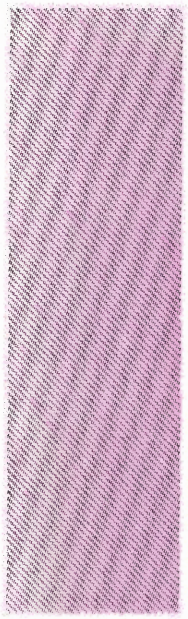


Figure 6.5a SiO_2_pedestal layer for the MEMS microstructures

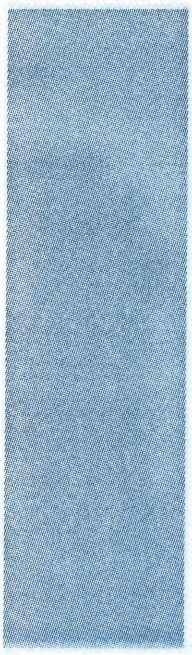


Figure 6.5b Polyimide layer for the MEMS microstructures

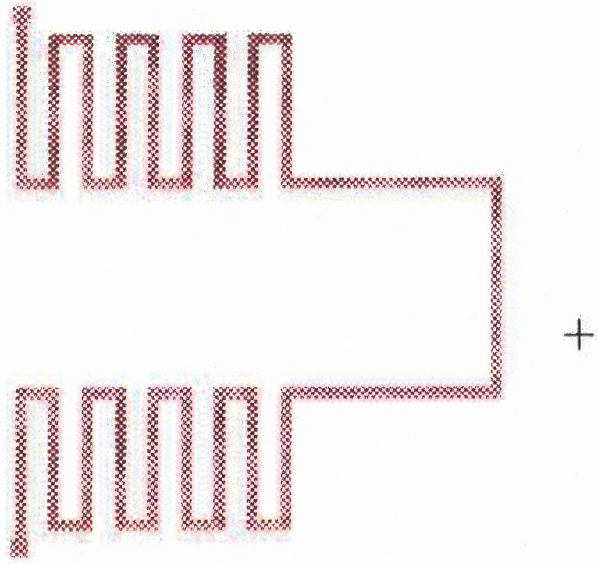


Figure 6.5c Metal3_Al layer for heater A of the MEMS microstructure

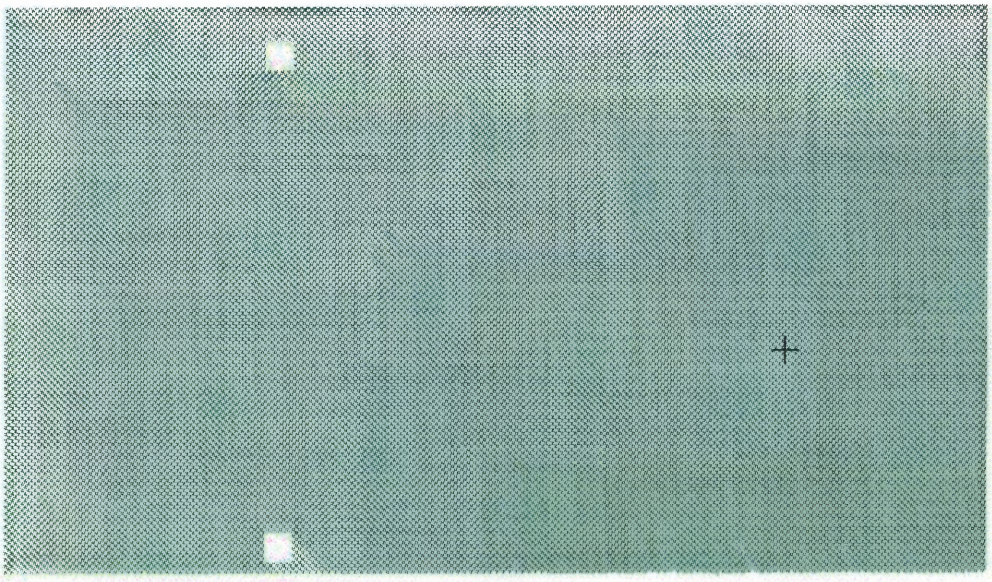


Figure 6.5d SiO_2_PECVD layer for the beam of the MEMS microstructure

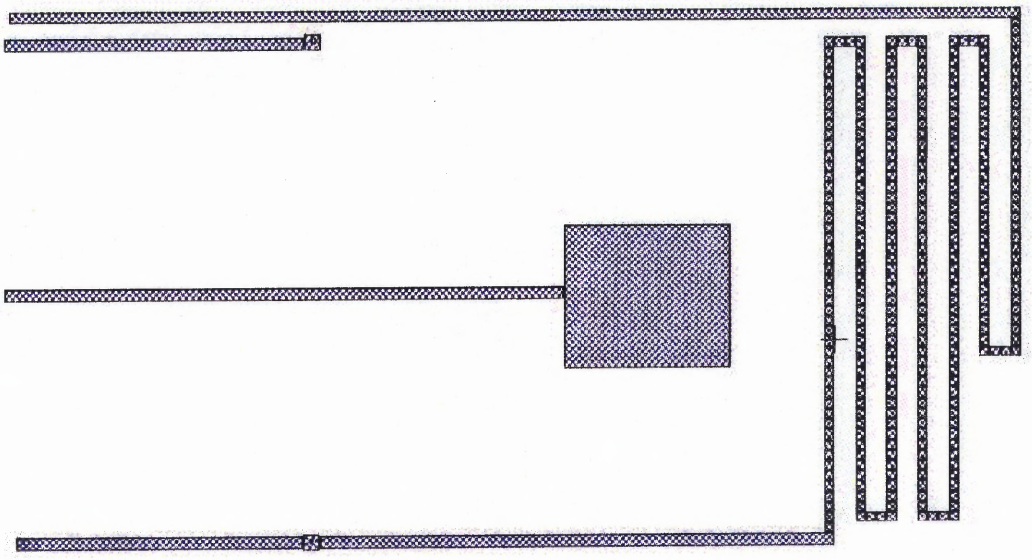


Figure 6.5e Metal4_Al layer for heater B of the MEMS microstructure

Figure 6.5f Gold layer for the probe tip of the MEMS microstructure

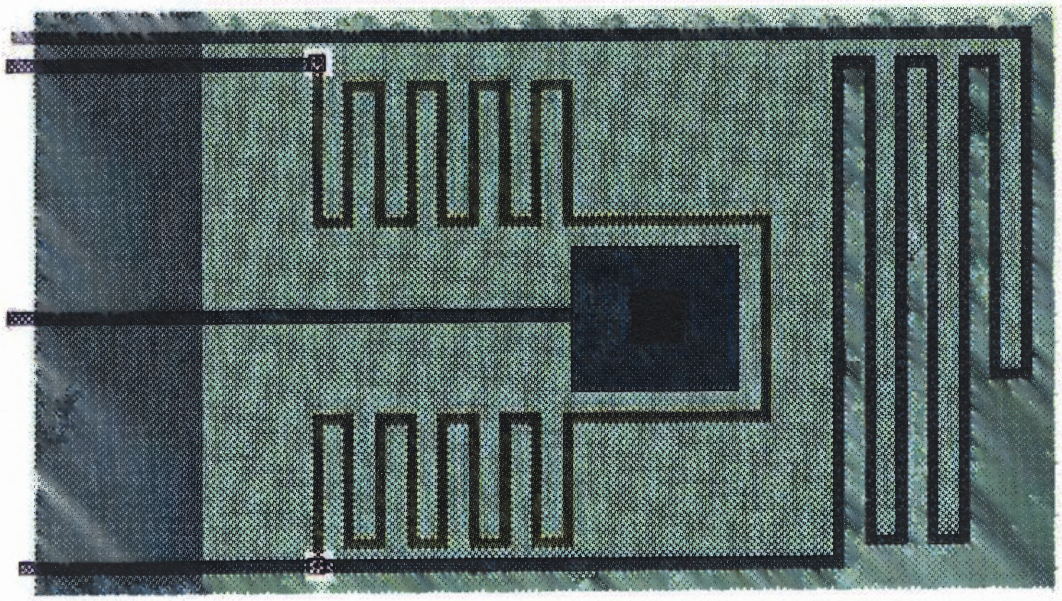


Figure 6.6 The composite MEMS microstructure

6.3 Integration of the CMOS and MEMS Designs

In this section, a series of figures that will show the integration of the CMOS control circuits and the MEMS microstructure are shown. The 4x4 array of the MEMS structures that will form the probe card is also shown. Finally, the whole chip with the bonding pads is shown.

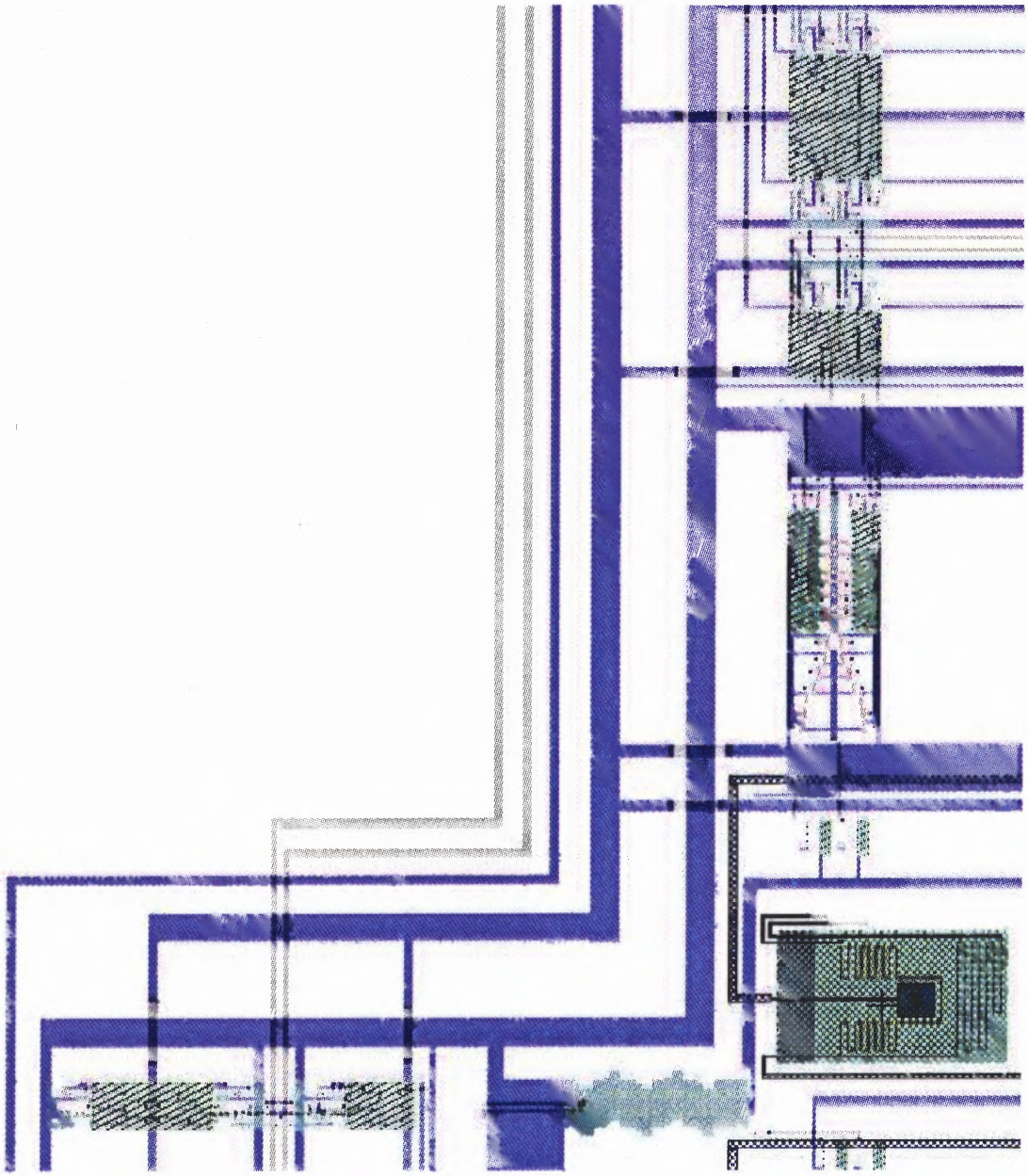


Figure 6.7a Layout of a single MEMS microstructure with its corresponding row and column address circuits

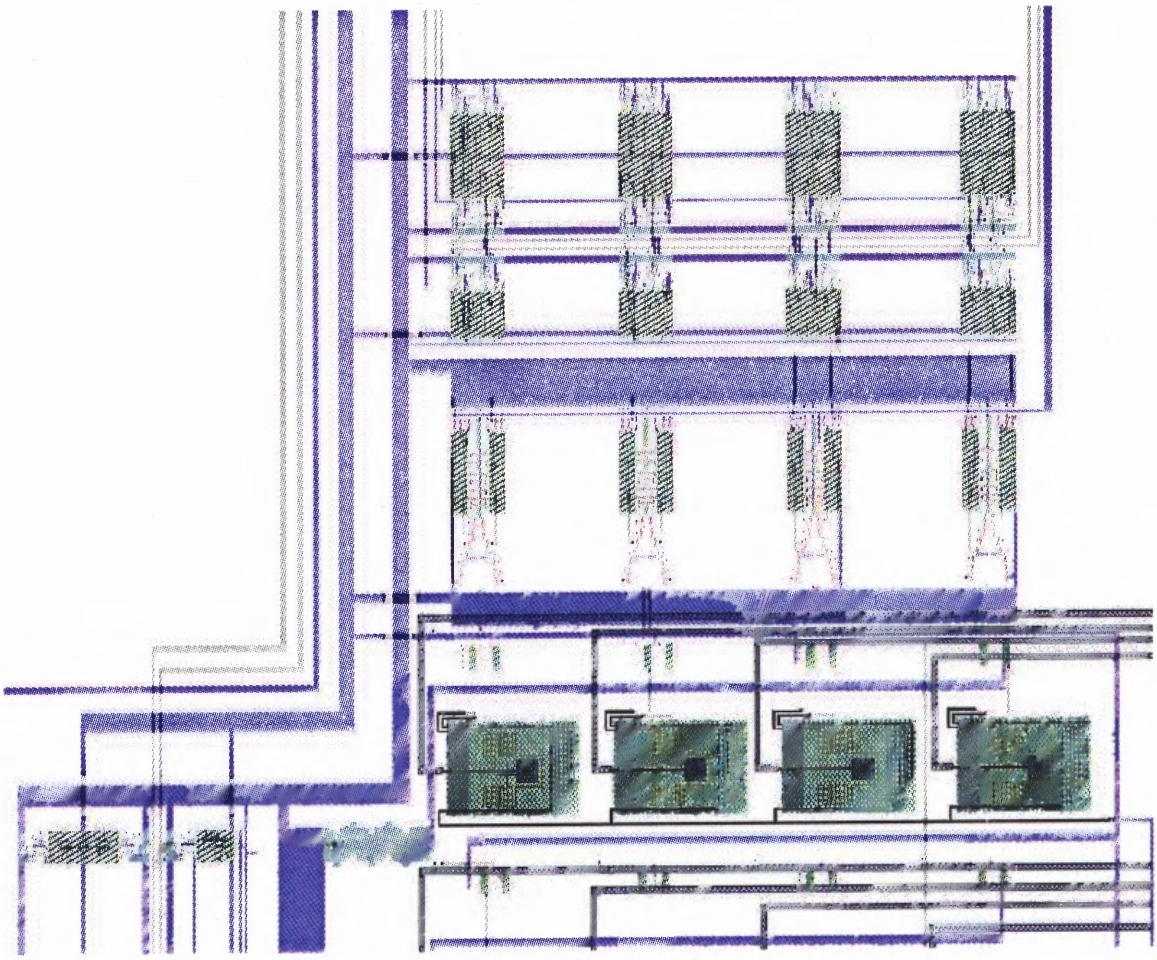


Figure 6.7b Layout showing a row of pixels

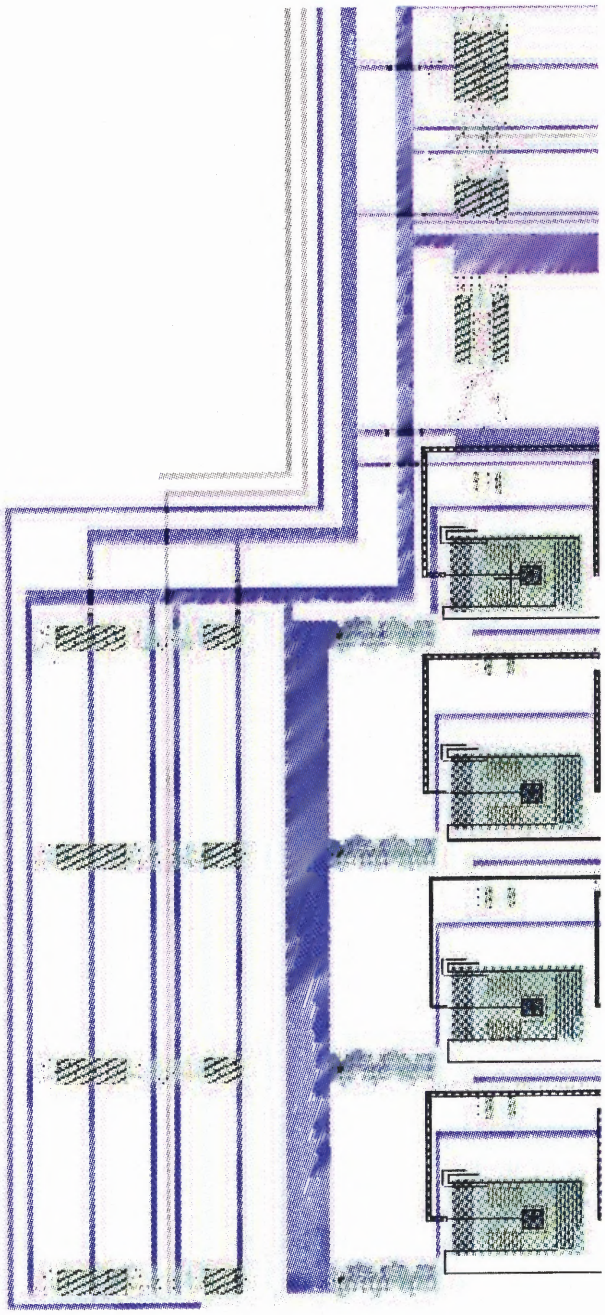


Figure 6.7c Layout showing a column of microstructures

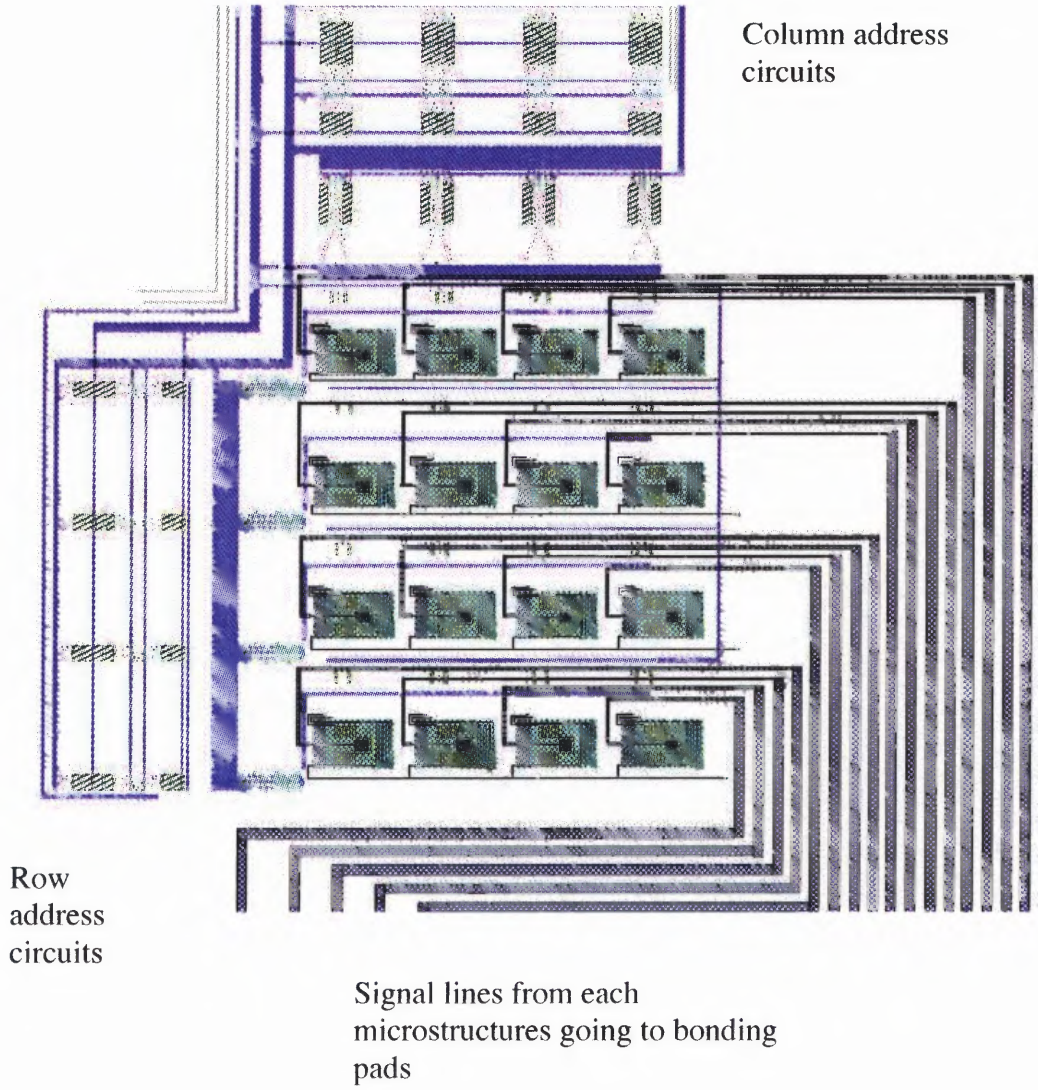
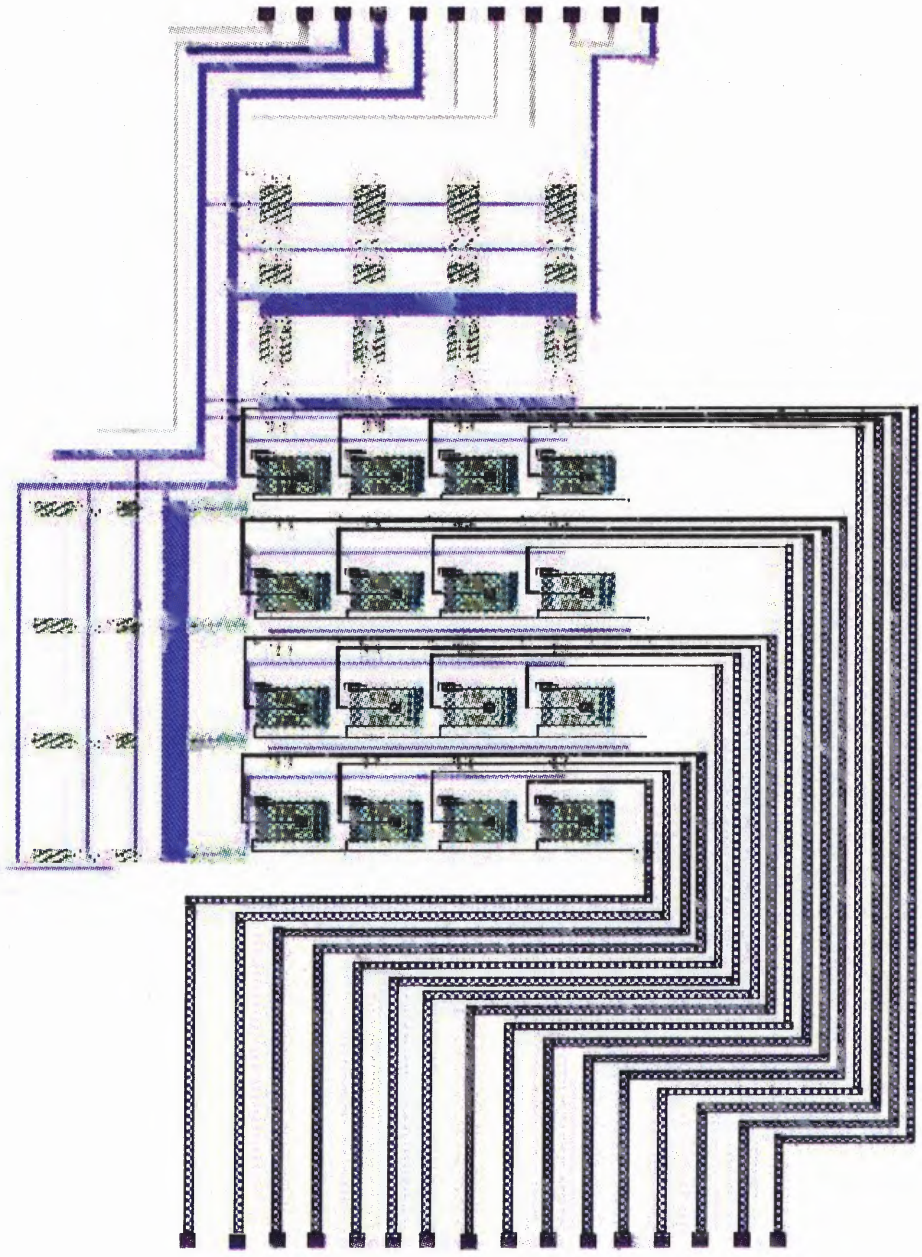


Figure 6.7d Layout of the 4x4 array of MEMS microstructures forming the probe card

Input bonding pads for the power supply and control signals



I/O bonding pads connected to the probe tips of each of the 16 microstructures

Figure 6.7e Layout of the whole chip

6.4 Summary and Conclusion

In this chapter, the addressing circuits described in Chapter 5 and the microstructures described in Chapter 4 were presented in integrated form to fulfill the design goal specified in Chapters 2 and 3 of this thesis. Each of the components of this design was thoroughly tested. Finally, the comprehensive PSPICE simulations show that the overall design will most likely function properly.

CHAPTER 7

SUMMARY AND CONCLUSIONS

A four by four latching probe microstructure has been designed. Each of the structures are controlled by two column and one row address circuits. The row and column address circuits were designed using 3-micron CMOS technology, and the micro-structures were designed using the MEMS technology. The CMOS circuit supplied the desired current to the microstructure so that the specified deflection could be achieved. The microstructure consists of bimorph cantilever with aluminum heaters mounted on SiO_2 deflection beam. On heating arches and latches on the substrate that has wedges cut into it. The probe-tip then touches the wafer under test and the test operation begins. The total chip area for the four by four probe card is approximately 1mm by 1mm.

This thesis demonstrates by detail design the feasibility of a MEMS-based probe head for testing wafers. The MEMS microstructures containing the probes and the CMOS programming circuits are fabricated on a single wafer. The CMOS circuits were simulated using PSPICE and the MEMS microstructures were simulated using ANSYS. The two could not be simulated together, and hence the clock speed of the overall system performance was difficult to ascertain. It was calculated that the switching time for each microstructure was about 2.3 msec. Hence it can be deduced that the reconfiguration time of the probe card to be approximately 10 msec which is quite fast.

The work done in this thesis can be extended in a number of ways. For example, it should be possible to easily scale the system to a 20x20 array or larger probe-cards. This larger array of probes would permit higher probe density and thus enable one to use this

chip in testing more complicated circuits. Another extension of the work could involve individual control of each microostructures. This can be done when the row and column address circuits are not coupled together, and if they have separate inputs. Combining all or some of the above features one can design a state of the art wafer testing system that has more flexibility in terms of the number of probes, ability to probe at different depths as well as of spacing of probes. These probe heads would cost far less that the traditional wafer probe heads since these are reconfigurable unlike the existing heads. That means that the same probe head can be programmed to test different circuits.

APPENDIX A

PSPICE SIMULATION AND NETLIST FILE

A.1. D/A Converter Netlist File.

```
* Schematics Netlist *


V_VGG          $N_0001 0 10V
M_M21          $N_0004 $N_0003 $N_0002 0 MbreakN-X
+ L=3u
+ W=9u
M_M19          $N_0006 $N_0003 $N_0005 0 MbreakN-X
+ L=3u
+ W=9u
M_M18          $N_0009 $N_0008 $N_0007 0 MbreakN-X
+ L=3u
+ W=9u
M_M17          $N_0011 $N_0008 $N_0010 0 MbreakN-X
+ L=3u
+ W=9u
M_M15          $N_0013 $N_0008 $N_0012 0 MbreakN-X
+ L=3u
+ W=9u
M_M22          $N_0012 $N_0015 $N_0014 0 MbreakN-X
+ L=3u
+ W=9u
M_M23          $N_0017 $N_0015 $N_0016 0 MbreakN-X
+ L=3u
+ W=9u
M_M24          $N_0005 $N_0015 $N_0018 0 MbreakN-X
+ L=3u
+ W=9u
M_M26          $N_0002 $N_0020 $N_0019 0 MbreakN-X
+ L=3u
+ W=9u
M_M35          $N_0019 $N_0021 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M33          $N_0018 $N_0021 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M27          $N_0007 $N_0020 $N_0022 0 MbreakN-X
+ L=3u
+ W=9u
M_M28          $N_0010 $N_0020 $N_0023 0 MbreakN-X
+ L=3u
+ W=9u
M_M29          $N_0014 $N_0021 0 0 MbreakN-X
+ L=3u
+ W=9u
```

```
M_M30          $N_0016 $N_0024 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M32          $N_0022 $N_0024 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M31          $N_0023 $N_0021 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M37          $N_0003 $N_0008 0 0 MbreakN-X
M_M39          $N_0024 $N_0021 0 0 MbreakN-X
M_M38          $N_0020 $N_0015 0 0 MbreakN-X
R_R3          $N_0025 $N_0003  1000k
R_R4          $N_0026 $N_0020  1000k
M_M16          $N_0027 $N_0008 $N_0017 0 MbreakN-X
+ L=3u
+ W=9u
V_VDD          $N_0028 0 15V
M_M1          $N_0029 $N_0004 $N_0028 $N_0028 MbreakP-X
+ L=16u
+ W=4u
M_M2          $N_0029 $N_0030 $N_0028 $N_0028 MbreakP-X
+ L=14.5u
+ W=4u
M_M3          $N_0029 $N_0006 $N_0028 $N_0028 MbreakP-X
+ L=13u
+ W=4u
M_M5          $N_0029 $N_0011 $N_0028 $N_0028 MbreakP-X
+ L=9.5u
+ W=4u
M_M6          $N_0029 $N_0027 $N_0028 $N_0028 MbreakP-X
+ L=8u
+ W=4u
M_M13          $N_0030 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M12          $N_0006 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M11          $N_0009 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M10          $N_0011 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M8          $N_0013 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M9          $N_0027 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M14          $N_0004 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M4          $N_0029 $N_0009 $N_0028 $N_0028 MbreakP-X
+ L=11.5u
+ W=4u
```

```
M_M7          $N_0029 $N_0013 $N_0028 $N_0028 MbreakP-X
+ L=6u
+ W=4u
R_R5          $N_0032 $N_0031  100
V_V28          $N_0031 0 15V
M_M41          $N_0032 $N_0029 0 0 MbreakN
+ L=3u
+ W=150u
R_R1          0 $N_0029  50k
M_M34          $N_0033 $N_0024 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M20          $N_0030 $N_0003 $N_0034 0 MbreakN-X
+ L=3u
+ W=9u
M_M25          $N_0034 $N_0015 $N_0033 0 MbreakN-X
+ L=3u
+ W=9u
V_V38          $N_0015 0
+PULSE 0.0 5v 0.1ms 10us 10us 2ms 4ms
V_V39          $N_0026 0
+PULSE 0 5v 2.1ms 10us 10us 2.0ms 4ms
R_R2          $N_0024 $N_0035  1000k
V_V37          $N_0025 0
+PULSE 0 5V 4.20ms 10us 10us 4ms 8ms
V_V36          $N_0008 0
+PULSE 0 5V 0.2ms 10us 10us 4ms 8ms
V_V23          $N_0021 0
+PULSE 0 5V 0 10us 10us 1ms 2ms
V_V29          $N_0035 0
+PULSE 0v 5v 1.02ms 10us 10us 1ms 2ms
```

D/A Converter Output File.

```
**** 08/25/99 19:13:09 ***** Win95 PSpice 8.0 (July 1997) ***** ID#
109713 ***

 * C:\MSimEv_8\Projects\DACmodelpulse2.sch


 ****     CIRCUIT DESCRIPTION


********************************************************************************
*******



* Schematics Version 8.0 - July 1997
* Wed Aug 25 19:01:57 1999
```

```
** Analysis setup **
.tran 1ms 8ms
.LIB "C:\MSimEv_8\Projects\DAC.lib"
.LIB "C:\MSimEv_8\Projects\DACmodelpulse.lib"


* From [SCHEMATICS NETLIST] section of msim.ini:
.lib nom.lib

.INC "DACmodelpulse2.net"

**** INCLUDING DACmodelpulse2.net ****
* Schematics Netlist *



V_VGG          $N_0001 0 10V
M_M21          $N_0004 $N_0003 $N_0002 0 MbreakN-X
+ L=3u
+ W=9u
M_M19          $N_0006 $N_0003 $N_0005 0 MbreakN-X
+ L=3u
+ W=9u
M_M18          $N_0009 $N_0008 $N_0007 0 MbreakN-X
+ L=3u
+ W=9u
M_M17          $N_0011 $N_0008 $N_0010 0 MbreakN-X
+ L=3u
+ W=9u
M_M15          $N_0013 $N_0008 $N_0012 0 MbreakN-X
+ L=3u
+ W=9u
M_M22          $N_0012 $N_0015 $N_0014 0 MbreakN-X
+ L=3u
+ W=9u
M_M23          $N_0017 $N_0015 $N_0016 0 MbreakN-X
+ L=3u
+ W=9u
M_M24          $N_0005 $N_0015 $N_0018 0 MbreakN-X
+ L=3u
+ W=9u
M_M26          $N_0002 $N_0020 $N_0019 0 MbreakN-X
+ L=3u
+ W=9u
M_M35          $N_0019 $N_0021 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M33          $N_0018 $N_0021 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M27          $N_0007 $N_0020 $N_0022 0 MbreakN-X
+ L=3u
+ W=9u
M_M28          $N_0010 $N_0020 $N_0023 0 MbreakN-X
+ L=3u
+ W=9u
```

```
M_M29          $N_0014 $N_0021 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M30          $N_0016 $N_0024 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M32          $N_0022 $N_0024 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M31          $N_0023 $N_0021 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M37          $N_0003 $N_0008 0 0 MbreakN-X
M_M39          $N_0024 $N_0021 0 0 MbreakN-X
M_M38          $N_0020 $N_0015 0 0 MbreakN-X
R_R3          $N_0025 $N_0003  1000k
R_R4          $N_0026 $N_0020  1000k
M_M16          $N_0027 $N_0008 $N_0017 0 MbreakN-X
+ L=3u
+ W=9u
V_VDD          $N_0028 0 15V
M_M1          $N_0029 $N_0004 $N_0028 $N_0028 MbreakP-X
+ L=16u
+ W=4u
M_M2          $N_0029 $N_0030 $N_0028 $N_0028 MbreakP-X
+ L=14.5u
+ W=4u
M_M3          $N_0029 $N_0006 $N_0028 $N_0028 MbreakP-X
+ L=13u
+ W=4u
M_M5          $N_0029 $N_0011 $N_0028 $N_0028 MbreakP-X
+ L=9.5u
+ W=4u
M_M6          $N_0029 $N_0027 $N_0028 $N_0028 MbreakP-X
+ L=8u
+ W=4u
M_M13          $N_0030 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M12          $N_0006 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M11          $N_0009 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M10          $N_0011 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M8          $N_0013 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M9          $N_0027 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
M_M14          $N_0004 $N_0001 $N_0028 $N_0028 MbreakP-X
+ L=16.5u
+ W=3.5u
```

```
M_M4          $N_0029 $N_0009 $N_0028 $N_0028 MbreakP-X
+ L=11.5u
+ W=4u
M_M7          $N_0029 $N_0013 $N_0028 $N_0028 MbreakP-X
+ L=6u
+ W=4u
R_R5          $N_0032 $N_0031  100
V_V28          $N_0031 0 15V
M_M41          $N_0032 $N_0029 0 0 MbreakN
+ L=3u
+ W=150u
R_R1          0 $N_0029  50k
M_M34          $N_0033 $N_0024 0 0 MbreakN-X
+ L=3u
+ W=9u
M_M20          $N_0030 $N_0003 $N_0034 0 MbreakN-X
+ L=3u
+ W=9u
M_M25          $N_0034 $N_0015 $N_0033 0 MbreakN-X
+ L=3u
+ W=9u
V_V38          $N_0015 0
+PULSE 0.0 5v 0.1ms 10us 10us 2ms 4ms
V_V39          $N_0026 0
+PULSE 0 5v 2.1ms 10us 10us 2.0ms 4ms
R_R2          $N_0024 $N_0035  1000k
V_V37          $N_0025 0
+PULSE 0 5V 4.20ms 10us 10us 4ms 8ms
V_V36          $N_0008 0
+PULSE 0 5V 0.2ms 10us 10us 4ms 8ms
V_V23          $N_0021 0
+PULSE 0 5V 0 10us 10us 1ms 2ms
V_V29          $N_0035 0
+PULSE 0v 5v 1.02ms 10us 10us 1ms 2ms

**** RESUMING DACmodelpulse2.cir ****
.INC "DACmodelpulse2.als"


**** INCLUDING DACmodelpulse2.als ****
* Schematics Aliases *

.ALIASES
V_VGG           VGG(+=$N_0001 -=0 )
M_M21           M21(d=$N_0004 g=$N_0003 s=$N_0002 b=0 )
M_M19           M19(d=$N_0006 g=$N_0003 s=$N_0005 b=0 )
M_M18           M18(d=$N_0009 g=$N_0008 s=$N_0007 b=0 )
M_M17           M17(d=$N_0011 g=$N_0008 s=$N_0010 b=0 )
M_M15           M15(d=$N_0013 g=$N_0008 s=$N_0012 b=0 )
M_M22           M22(d=$N_0012 g=$N_0015 s=$N_0014 b=0 )
M_M23           M23(d=$N_0017 g=$N_0015 s=$N_0016 b=0 )
M_M24           M24(d=$N_0005 g=$N_0015 s=$N_0018 b=0 )
M_M26           M26(d=$N_0002 g=$N_0020 s=$N_0019 b=0 )
M_M35           M35(d=$N_0019 g=$N_0021 s=0 b=0 )
M_M33           M33(d=$N_0018 g=$N_0021 s=0 b=0 )
M_M27           M27(d=$N_0007 g=$N_0020 s=$N_0022 b=0 )
```

```
M_M28           M28(d=$N_0010 g=$N_0020 s=$N_0023 b=0 )
M_M29           M29(d=$N_0014 g=$N_0021 s=0 b=0 )
M_M30           M30(d=$N_0016 g=$N_0024 s=0 b=0 )
M_M32           M32(d=$N_0022 g=$N_0024 s=0 b=0 )
M_M31           M31(d=$N_0023 g=$N_0021 s=0 b=0 )
M_M37           M37(d=$N_0003 g=$N_0008 s=0 b=0 )
M_M39           M39(d=$N_0024 g=$N_0021 s=0 b=0 )
M_M38           M38(d=$N_0020 g=$N_0015 s=0 b=0 )
R_R3            R3(1=$N_0025 2=$N_0003 )
R_R4            R4(1=$N_0026 2=$N_0020 )
M_M16           M16(d=$N_0027 g=$N_0008 s=$N_0017 b=0 )
V_VDD           VDD(+=$N_0028 -=0 )
M_M1            M1(d=$N_0029 g=$N_0004 s=$N_0028 b=$N_0028 )
M_M2            M2(d=$N_0029 g=$N_0030 s=$N_0028 b=$N_0028 )
M_M3            M3(d=$N_0029 g=$N_0006 s=$N_0028 b=$N_0028 )
M_M5            M5(d=$N_0029 g=$N_0011 s=$N_0028 b=$N_0028 )
M_M6            M6(d=$N_0029 g=$N_0027 s=$N_0028 b=$N_0028 )
M_M13           M13(d=$N_0030 g=$N_0001 s=$N_0028 b=$N_0028 )
M_M12           M12(d=$N_0006 g=$N_0001 s=$N_0028 b=$N_0028 )
M_M11           M11(d=$N_0009 g=$N_0001 s=$N_0028 b=$N_0028 )
M_M10           M10(d=$N_0011 g=$N_0001 s=$N_0028 b=$N_0028 )
M_M8            M8(d=$N_0013 g=$N_0001 s=$N_0028 b=$N_0028 )
M_M9            M9(d=$N_0027 g=$N_0001 s=$N_0028 b=$N_0028 )
M_M14           M14(d=$N_0004 g=$N_0001 s=$N_0028 b=$N_0028 )
M_M4            M4(d=$N_0029 g=$N_0009 s=$N_0028 b=$N_0028 )
M_M7            M7(d=$N_0029 g=$N_0013 s=$N_0028 b=$N_0028 )
R_R5            R5(1=$N_0032 2=$N_0031 )
V_V28           V28(+=$N_0031 -=0 )
M_M41           M41(d=$N_0032 g=$N_0029 s=0 b=0 )
R_R1            R1(1=0 2=$N_0029 )
M_M34           M34(d=$N_0033 g=$N_0024 s=0 b=0 )
M_M20           M20(d=$N_0030 g=$N_0003 s=$N_0034 b=0 )
M_M25           M25(d=$N_0034 g=$N_0015 s=$N_0033 b=0 )
V_V38           V38(+=$N_0015 -=0 )
V_V39           V39(+=$N_0026 -=0 )
R_R2            R2(1=$N_0024 2=$N_0035 )
V_V37           V37(+=$N_0025 -=0 )
V_V36           V36(+=$N_0008 -=0 )
V_V23           V23(+=$N_0021 -=0 )
V_V29           V29(+=$N_0035 -=0 )
.ENDALIASES


**** RESUMING DACmodelpulse2.cir ****
.probe


.END
```

**** 08/25/99 19:13:09 ***** Win95 PSpice 8.0 (July 1997) ***** ID# 109713 ***

* C:\MSimEv_8\Projects\DACmodelpulse2.sch

**** MOSFET MODEL PARAMETERS

****

	MbreakP-X PMOS	MbreakN-X NMOS	MbreakN NMOS
LEVEL	2	2	1
L	100.000000E-06	100.000000E-06	100.000000E-06
W	100.000000E-06	100.000000E-06	100.000000E-06
LD	531.000000E-09	310.000000E-09	
WD	1.030000E-06	1.177000E-06	
VTO	-.54	.438	0
KP	11.700000E-06	43.580000E-06	20.000000E-06
GAMMA	.856	.798	0
PHI	.6	.6	.6
RSH	65	33.6	
IS	10.000000E-15	10.000000E-15	10.000000E-15
JS	.0141	2.195000E-03	0
PB	.701	.95	.8
PBSW	.701	.95	.8
CJ	250.000000E-06	223.800000E-06	0
CJSW	388.000000E-12	348.600000E-12	0
MJ	.417	.5096	
MJSW	.2	.216	
FC	.95	.95	
CGSO	288.000000E-12	215.000000E-12	0
CGDO	288.000000E-12	215.000000E-12	0
CGBO	138.000000E-12	173.000000E-12	
TOX	48.000000E-09	48.400000E-09	0
XJ	700.000000E-09	300.000000E-09	0
UCRIT	8.000000E+06	7.847000E-06	
UEXP	.0754	.0719	
UTRA	.03	.224	
VMAX	40.000000E+03	47.830000E+03	
NEFF		1.787	
DELTA	1	1.053	
DIOMOD	1	1	1
VFB	0	0	0
U0	0	0	0
TEMP	0	0	0
VDD	0	0	0
XPART	0	0	0

```
**** 08/25/99 19:13:09 ***** Win95 PSpice 8.0 (July 1997) ***** ID#
109713 ***

 * C:\MSimEv_8\Projects\DACmodelpulse2.sch

 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

*********************************************************************
*******


 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE
VOLTAGE

($N_0001)   10.0000                  ($N_0002) 168.5E-21

($N_0003)-748.3E-24                  ($N_0004)   15.0000

($N_0005) 168.5E-21                  ($N_0006)   15.0000

($N_0007) 168.5E-21                  ($N_0008)    0.0000

($N_0009)   15.0000                  ($N_0010) 168.5E-21

($N_0011)   15.0000                  ($N_0012) 168.5E-21

($N_0013)   15.0000                  ($N_0014) 263.6E-21

($N_0015)    0.0000                  ($N_0016) 263.6E-21

($N_0017) 168.5E-21                  ($N_0018) 263.6E-21

($N_0019) 263.6E-21                  ($N_0020)-748.3E-24

($N_0021)    0.0000                  ($N_0022) 263.6E-21

($N_0023) 263.6E-21                  ($N_0024)-748.3E-24

($N_0025)    0.0000                  ($N_0026)    0.0000

($N_0027)   15.0000                  ($N_0028)   15.0000

($N_0029) 5.254E-06                  ($N_0030)   15.0000

($N_0031)   15.0000                  ($N_0032)   15.0000

($N_0033) 263.6E-21                  ($N_0034) 168.5E-21

($N_0035)    0.0000
```

```
VOLTAGE SOURCE CURRENTS
NAME          CURRENT

V_VGG          0.000E+00
V_VDD         -2.101E-10
V_V28         -1.502E-11
V_V38          0.000E+00
V_V39         -7.483E-28
V_V37         -7.483E-28
V_V36          0.000E+00
V_V23          0.000E+00
V_V29         -7.483E-28

TOTAL POWER DISSIPATION   3.38E-09  WATTS


      JOB CONCLUDED

      TOTAL JOB TIME            9.60
```

A.2. Shift Register Netlist File

```
* Schematics Netlist *


V_V5          $N_0001 0 5V
M_M23          $N_0003 $N_0002 $N_0001 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M31          $N_0003 $N_0002 0 0 MbreakN
+ L=3um
+ W=6um
M_M24          $N_0004 $N_0003 $N_0001 $N_0001 MbreakP
+ W=9um
M_M25          $N_0006 $N_0005 $N_0004 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M33          $N_0007 $N_0002 0 0 MbreakN
+ L=3um
+ W=6um
M_M32          $N_0006 $N_0005 $N_0007 0 MbreakN
+ L=3um
+ W=6um
M_M26          $N_0009 $N_0008 $N_0001 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M34          $N_0009 $N_0008 0 0 MbreakN
+ L=3um
+ W=6um
M_M27          $N_0010 $N_0009 $N_0001 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M28          $N_0011 $N_0006 $N_0010 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M35          $N_0011 $N_0006 $N_0012 0 MbreakN
+ L=3um
+ W=6um
M_M36          $N_0012 $N_0008 0 0 MbreakN
+ L=3um
+ W=6um
M_M29          $N_0014 $N_0013 $N_0001 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M37          $N_0014 $N_0013 0 0 MbreakN
+ L=3um
+ W=6um
M_M30          $N_0015 $N_0014 $N_0011 $N_0011 MbreakP
+ L=3um
+ W=9um
M_M38          $N_0011 $N_0013 $N_0015 $N_0015 MbreakN
+ L=3um
+ W=6um
V_V10          $N_0013 0 5V
```

```
V_V7          $N_0002 0
+PULSE 0v 5v .2ms 10us 10us 2ms 6ms
V_V8          $N_0008 0
+PULSE 0v 5v 3ms 10us 10us 2ms 6ms
V_V6          $N_0005 0
+PULSE 0v 5v .3ms 5us 5us 2ms 6ms
```

Shift Register Output File

```
**** 08/25/99 19:09:47 ***** Win95 PSpice 8.0 (July 1997) ***** ID#
109713 ***

 * C:\MSimEv_8\Projects\shftreg3.sch

 ****     CIRCUIT DESCRIPTION

*******************************************************************************
*******



* Schematics Version 8.0 - July 1997
* Mon Aug 23 12:09:26 1999



** Analysis setup **
.tran 1ms 20ms


* From [SCHEMATICS NETLIST] section of msim.ini:
.lib nom.lib

.INC "shftreg3.net"

**** INCLUDING shftreg3.net ****
* Schematics Netlist *



V_V5          $N_0001 0 5V
M_M23          $N_0003 $N_0002 $N_0001 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M31          $N_0003 $N_0002 0 0 MbreakN
+ L=3um
+ W=6um
M_M24          $N_0004 $N_0003 $N_0001 $N_0001 MbreakP
+ W=9um
M_M25          $N_0006 $N_0005 $N_0004 $N_0001 MbreakP
```

```
+ L=3um
+ W=9um
M_M33          $N_0007 $N_0002 0 0 MbreakN
+ L=3um
+ W=6um
M_M32          $N_0006 $N_0005 $N_0007 0 MbreakN
+ L=3um
+ W=6um
M_M26          $N_0009 $N_0008 $N_0001 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M34          $N_0009 $N_0008 0 0 MbreakN
+ L=3um
+ W=6um
M_M27          $N_0010 $N_0009 $N_0001 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M28          $N_0011 $N_0006 $N_0010 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M35          $N_0011 $N_0006 $N_0012 0 MbreakN
+ L=3um
+ W=6um
M_M36          $N_0012 $N_0008 0 0 MbreakN
+ L=3um
+ W=6um
M_M29          $N_0014 $N_0013 $N_0001 $N_0001 MbreakP
+ L=3um
+ W=9um
M_M37          $N_0014 $N_0013 0 0 MbreakN
+ L=3um
+ W=6um
M_M30          $N_0015 $N_0014 $N_0011 $N_0011 MbreakP
+ L=3um
+ W=9um
M_M38          $N_0011 $N_0013 $N_0015 $N_0015 MbreakN
+ L=3um
+ W=6um
V_V10          $N_0013 0 5V
V_V7          $N_0002 0
+PULSE 0v 5v .2ms 10us 10us 2ms 6ms
V_V8          $N_0008 0
+PULSE 0v 5v 3ms 10us 10us 2ms 6ms
V_V6          $N_0005 0
+PULSE 0v 5v .3ms 5us 5us 2ms 6ms

**** RESUMING shftreg3.cir ****
.INC "shftreg3.als"



**** INCLUDING shftreg3.als ****
* Schematics Aliases *

.ALIASES
V_V5            V5(+=$N_0001 -=0 )
M_M23           M23(d=$N_0003 g=$N_0002 s=$N_0001 b=$N_0001 )
```

```
M_M31           M31(d=$N_0003 g=$N_0002 s=0 b=0 )
M_M24           M24(d=$N_0004 g=$N_0003 s=$N_0001 b=$N_0001 )
M_M25           M25(d=$N_0006 g=$N_0005 s=$N_0004 b=$N_0001 )
M_M33           M33(d=$N_0007 g=$N_0002 s=0 b=0 )
M_M32           M32(d=$N_0006 g=$N_0005 s=$N_0007 b=0 )
M_M26           M26(d=$N_0009 g=$N_0008 s=$N_0001 b=$N_0001 )
M_M34           M34(d=$N_0009 g=$N_0008 s=0 b=0 )
M_M27           M27(d=$N_0010 g=$N_0009 s=$N_0001 b=$N_0001 )
M_M28           M28(d=$N_0011 g=$N_0006 s=$N_0010 b=$N_0001 )
M_M35           M35(d=$N_0011 g=$N_0006 s=$N_0012 b=0 )
M_M36           M36(d=$N_0012 g=$N_0008 s=0 b=0 )
M_M29           M29(d=$N_0014 g=$N_0013 s=$N_0001 b=$N_0001 )
M_M37           M37(d=$N_0014 g=$N_0013 s=0 b=0 )
M_M30           M30(d=$N_0015 g=$N_0014 s=$N_0011 b=$N_0011 )
M_M38           M38(d=$N_0011 g=$N_0013 s=$N_0015 b=$N_0015 )
V_V10           V10(+=$N_0013 -=0 )
V_V7            V7(+=$N_0002 -=0 )
V_V8            V8(+=$N_0008 -=0 )
V_V6            V6(+=$N_0005 -=0 )
.ENDALIASES


**** RESUMING shftreg3.cir ****
.probe


.END
```

**** 08/25/99 19:09:47 ***** Win95 PSpice 8.0 (July 1997) ***** ID# 109713 ***

 * C:\MSimEv_8\Projects\shftreg3.sch

 **** MOSFET MODEL PARAMETERS

****
****

	MbreakP PMOS	MbreakN NMOS
LEVEL	1	1
L	100.000000E-06	100.000000E-06
W	100.000000E-06	100.000000E-06
VTO	0	0
KP	20.000000E-06	20.000000E-06
GAMMA	0	0
PHI	.6	.6
IS	10.000000E-15	10.000000E-15
JS	0	0
PB	.8	.8
PBSW	.8	.8
CJ	0	0
CJSW	0	0
CGSO	0	0
CGDO	0	0
TOX	0	0
XJ	0	0
DIOMOD	1	1
VFB	0	0
U0	0	0
TEMP	0	0
VDD	0	0
XPART	0	0

```
**** 08/25/99 19:09:47 ***** Win95 PSpice 8.0 (July 1997) ***** ID#
109713 ***

 * C:\MSimEv_8\Projects\shftreg3.sch

 ****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

**********************************************************************
*******


 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE
VOLTAGE

($N_0001)    5.0000                   ($N_0002)    0.0000

($N_0003)    5.0000                   ($N_0004)    3.7550

($N_0005)    0.0000                   ($N_0006)    3.7550

($N_0007)-576.3E-09                   ($N_0008)    0.0000

($N_0009)    5.0000                   ($N_0010)    3.7553

($N_0011)    1.8724                   ($N_0012)    1.8724

($N_0013)    5.0000                   ($N_0014) 25.05E-09

($N_0015)    1.8724


    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_V5        -2.444E-11
    V_V10        0.000E+00
    V_V7         0.000E+00
    V_V8         0.000E+00
    V_V6         0.000E+00

    TOTAL POWER DISSIPATION   1.22E-10  WATTS


          JOB CONCLUDED

          TOTAL JOB TIME            2.47
```

APPENDIX B

ANSYS SIMULATION GRAPH

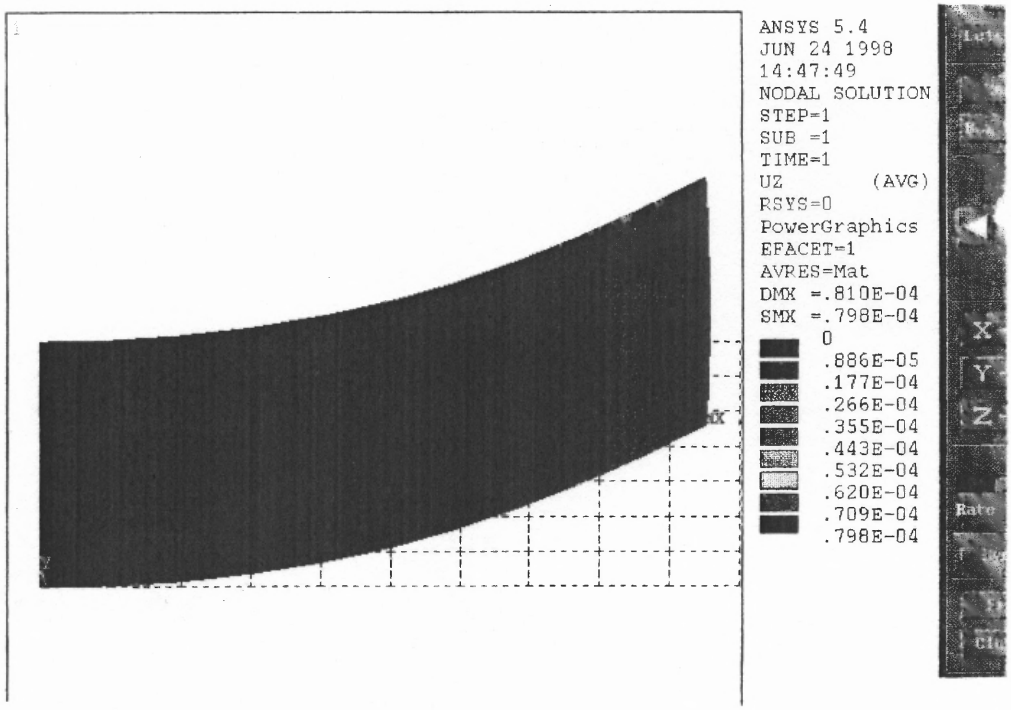


Figure B.1 ANSYS simulation of bimorph cantilever

The above ANSYS simulation was done for half the length of the cantilever. The portion of the cantilever with heater A was simulated. The result shows that the deflection height is 80μm. If the portion of the cantilever with heater B had been included, then half of the cantilever would bend in the opposite direction. Hence it can be concluded that for the simulation of the whole cantilever, the resulting deflection height in the center of the cantilever beam would approximately be 60μm.

APPENDIX C

ALTERNATIVE THEORY OF BENDING

In this section a comparison is done between the theory of bending described in section 4.2.1 of chapter 4 and a more recent publication [16] on the same topic. It is shown that for the design proposed in this thesis, the result obtained after further approximations, is the same in both the papers.

From the recent paper by Chu, Mehregany and Mullen [16], the maximum tip deflection d in a bimorph cantilever is given by the following equations:

$$K = \frac{6b_1b_2E_1E_2t_1t_2(t_1+t_2)(\alpha_2-\alpha_1)\Delta T}{(b_1E_1t_1^{\,2})^2+(b_2E_2t_2)^2+2b_1b_2E_1E_2t_1t_2(2t_1^{\,2}+3t_1t_2+2t_2^{\,2})} \qquad (1)$$

$$d = KL^2/2 \qquad (2)$$

where b_1, b_2 are width of the two layers

E_1, E_2 are Young's modulus of elasticity

t_1, t_2 are thickness of the two layers, $t_2 << t_1$

α_1, α_2 are thermal coefficients of expansion, $\alpha_2 > \alpha_1$

L is the length of the bimorph cantilever

ΔT is the temperature difference

In this thesis, for simplification, we have assumed $b_1 = b_2 = b$ and $E_1 = E_2$ approximately. By substituting the approximations in equation (1), it can be rewritten as

The following:

$$K = \frac{6t_1t_2(t_1+t_2)\Delta\alpha\,\Delta T}{t_1^{\,4}+t_2^{\,4}+t_1t_2(2t_1^{\,2}+3t_1t_2+2t_2^{\,2})} \tag{3}$$

In this thesis, t_2 represents aluminum heater and t_1 is SiO_2 beam. The thickness of aluminum is 0.1μm and that of SiO_2 is 2μm. Hence we can approximate $t_2 << t_1$. Rewriting equation 3 by neglecting t_2 from the summation:

$$K = \frac{6t_1^{\,2}t_2\Delta\alpha\,\Delta T}{t_1^{\,4}+2t_1^{\,3}t_2}$$

$$= \frac{6t_2\Delta\alpha\,\Delta T}{t_1^{\,2}} \tag{4}$$

Substituting equation 4 in equation 2, the maximum deflection is found to be:

$$d = \frac{3t_2\Delta\alpha\,\Delta TL^2}{t_1^{\,2}} \tag{5}$$

From the earlier paper of E. Suhir [7], the equation for maximum deflection of cantilever was derived in section 4.2.1. Rewriting the final equation 4.19,

$$v_{max} = \frac{hl^2\Delta\alpha\Delta t}{4\lambda D} \tag{6}$$

Where $h = t_1 + t_2$

$$D = D_1 + D_2 = \frac{E_1 t_1^{\,3}}{12(1-\nu_1^{\,2})} + \frac{E_2 t_2^{\,3}}{12(1-\nu_2^{\,2})} \tag{7}$$

Here ν_1 and ν_2 are Poisson's ratio of the two materials.

$$\lambda = \frac{1}{12}\left[\frac{t_1^{\,2}}{D_1} + \frac{t_2^{\,2}}{D_2} + \frac{3(t_1+t_2)^2}{D_1+D_2}\right] \tag{8}$$

Now, one can assume $E_1 = E_2 = E$ approximately and since $\nu_1^{\,2} = \nu_2^{\,2} << 1$, equation 7 can be rewritten as follows:

$$D = D_1 + D_2 = \frac{E}{12}(t_1^{\,3} + t_2^{\,3}) \tag{9}$$

Since it has been shown that $t_2 << t_1$, equation 9 can be further rewritten as:

$$D = D_1 + D_2 = \frac{E t_1^{\,3}}{12} \tag{10}$$

For the denominator of equation 6, the value of D is found to be:

$$\lambda D = \frac{t_1^{\,3}}{12 t_2} \tag{11}$$

Substituting equation 11 back in equation 6, we get

(12)

$$v_{max} = \frac{12t_2(t_1 + t_2)L^2\Delta\alpha\Delta T}{4t_1^3} = \frac{3\Delta\alpha\Delta T t_2 L^2}{t_1^2}$$

Comparing equations 5 and 7, it is shown that both publications come to the same conclusion for the approximations done in this thesis. Hence, even with the more recent paper, the theoretical calculation done in section 4.2.1 stands.

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