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Low-power transceiver design for mobile wireless chemical biological sensors

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ABSTRACT

LOW-POWER TRANSCEIVER DESIGN FOR MOBILE WIRELESS CHEMICAL AND BIOLOGICAL SENSORS

by
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The design of a smart integrated chemical sensor system that will enhance sensor performance and compatibility to Ad hoc network architecture remains a challenge. This work involves the design of a Transceiver for a mobile chemical sensor. The transceiver design integrates all building blocks on-chip, including a low-noise amplifier with an input-matching network, a Voltage Controlled Oscillator with injection locking, Gilbert cell mixers, and a Class E Power amplifier making it as a single-chip transceiver. This proposed low power 2GHz transceiver has been designed in TSMC 0.35μm CMOS process using Cadence electronic design automation tools. Post layout HSPICE simulation indicates that Design meets the separation of noise levels by 52dB and 42dB in transmitter and receiver respectively with power consumption of 56 mW and 38 mW in transmit and receive mode.

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by
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LOW-POWER TRANSCEIVER DESIGN FOR MOBILE WIRELESS CHEMICAL AND BIOLOGICAL SENSORS

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To my beloved Parents and Brother

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CHAPTER 1

INTRODUCTION

With the development of information society, sensors are getting more and more challenges. Detecting, monitoring and transmitting the data are becoming more and more complicated issues. There are many environments unsuitable to humans, therefore use of sensors is only solution. The threat of terrorism is also prompting innovative approaches. Therefore it is required to design and develop the technologies that are rapid and cost effective deployment of sensor based systems in an ad-hoc fashion, where the signal from the sensors can be monitored remotely using advanced wireless technologies. In order for this type of chemical sensors to be useful in wireless applications in an ad-hoc network, it is required to have transceiver circuit integrated in the device to communicate with the network system for considerable atmospheric changes.

The explosive growth of these kinds of wireless applications has resulted in an increasing demand for wireless transceivers with low cost, low power consumption and small form factors. Unfortunately, all these transceivers still require some special post-processing or some off-chip components, including off-chip or bondwire inductors, input matching network, filters and Voltage Controlled Oscillators (VCO), which inevitably increases the cost of the whole transceiver. The VLSI capabilities of CMOS make the technology particularly well-suited for very high levels of integration while increasing the functionality of a single-chip Transceiver.

In this Thesis a CMOS RF transceiver is designed for short-distance communication using Ad-hoc networks without any off-chip components. The transceiver integrates all required building blocks in a single chip, including a Injection Locked Voltage Controlled Oscillator, Mixers, Low Noise Amplifier and a class-E power amplifier with matching network.

Direct conversion architecture is chosen for the transmitter to reduce the components, to maximize the image rejection, and to minimize the chip area. Superheterodyne architecture is used in receiver to eliminate the image reject filters needed between the LNA and mixer. All building blocks are fully differential to minimize the substrate coupling and to maximize the linearity at a cost of larger power consumption.

The report is organized into six chapters. Literature survey, different architectures for transceiver and the architecture of the proposed transmitter are briefly discussed in Chapter 2. The circuit implementations using TSMC 0.35 μ SCMOS Technology of VCO, Mixer, Power Amplifier and LNA are described in Chapter 3.Chapter 4 presents layouts and experimental results of every component and transceiver. Finally, Chapter 5 summarizes the thesis work and presents the future work.

CHAPTER 2

TRANSCEIVER ARCHITECTURE OVERVIEW AND DESIGN

CMOS RF ICS at gigahertz range frequencies have made great sliders in recent years. The effort so far has been directed towards the applications like wireless LAN, DECT and cellular communications [1-3]. Different types of transceivers are implemented for these applications. Some are designed as a single chip ,other are designed by using external components. A fully integrated CMOS transceiver tuned to 2.4 GHz for Bluetooth applications is implemented in 0.35μ technology [4]. It includes all the receive and transmit building blocks, such as frequency synthesizer, voltage-controlled oscillator (VCO), power amplifier, and demodulator. The receiver uses a low-IF architecture for higher level of integration and lower power consumption. The direct-conversion transmitter delivers a GFSK modulated spectrum. The VCO consisting of a cross-coupled differential pair loaded by on-chip inductors. Transceiver consumes 46 mA in receive mode and 47 mA in transmitmode from a 2.7-V supply.For digital narrow band cordless applications, transceiver is implemented in 0.25μ technology [5]. The transmitter use open-loop FSK modulation and receiver use a single conversion image-reject architecture followed by an IF chain and demodulator that provides output data to baseband for further processing. But this transceiver use external channel filters to employ 10.7 MHz IF.A CMOS IC that implements the 802.3 Ethernet standards for 10- and 100-Mb/s data rates is described [6]. The circuit uses mixed-signal techniques to perform transmit pulse shaping, receive adaptive line equalization, baseline wander compensation, and timing recovery. The IC occupies 23 mm^2 in a 0.6μ single-poly CMOS process and dissipates

more power 850 mW from a 5-V supply.A transceiver in 0.18μ technology with 2.5Gb/s is implemented for optical communication [7]. The transceiver consists of receiver with photo-detector and n-well-p-substrate photo diode, and a transmitter with a laser diode driver and flip-chip package VCSEL laser diode. The circuit operates with 1.8V and consumes 19mW power. A 5GHz CMOS transceiver for IEEE 802.11a WLAN application is designed in 0.25μ technology [8]. Both transmitter and receiver employ dual conversion with 1GHz intermediate frequency. The transmitter and receiver used same synthesizer, which generates both 1GHz and 4GHz LO signals. The IC occupies large area 22mm^2 with 40mW power consumption from 2.7 V supply. A 0.25μ CMOS transceiver front end for GSM is implemented [9]. It needs few external passive components and consumes moderate power. A 900-MHz CMOS wireless transceiver [10] uses Single-conversion architecture with a high-IF of 70 MHz for the receiver and direct modulation architecture for the transmitter. This transceiver has been designed and fabricated with 0.5μm CMOS process. The IC also occupies larger area 8.1mm^2 and consumes more power (227mW).

There are a few transceivers in ad-hoc networks for wireless integrated sensors applications. In ad-hoc technology major problem is with battery, The RF front end consumes 30% - 40% of battery power. So these devices must be designed with mow power consumption to increase the life of battery. In this work we designed a low power transceiver (56dB in transmit mode and 36dB in receive mode) for 2 GHz frequency.

To design transceiver that is low power as well as low in manufacturing cost, CMOS scaling and improved circuit techniques help to achieve many evolutionary advances in architectural innovations.

2.1 Transmitter Architectures

Various transmitter architectures are described in [11- 15]. Issues such as image rejection and band selectivity are more relaxed in transmitter design, leaving the output amplifier design as the primary challenge. In the following section we will discuss various architectures currently used in transmitter design.

2.1.2 Direct Conversion Architecture

A simple direct conversion transmitter is sown in Figure 2.1. In this architecture the baseband signal is mixed with the Local oscillator output and result is bandpass filtered and applied to PA. A matching network is placed between the antenna and PA to allow maximum power transfer and filter out-of-band components that result from nonlinearities in amplifier. Direct conversion architecture suffers from an important draw back: disturbance of the local oscillator by PA output. As shown in Figure 2.2 this issue comes because the PA output is modulated waveform with high power and a spectrum centered around the VCO frequency. Thus the output of PA corrupts the oscillator spectrum. This corruption occurs through "injection pulling" or "injection locking", thereby the frequency of an oscillator tends to shifts towards the frequency of an external stimulus. As shown in Figure 2.3, if the frequency of the injected noise is close to the

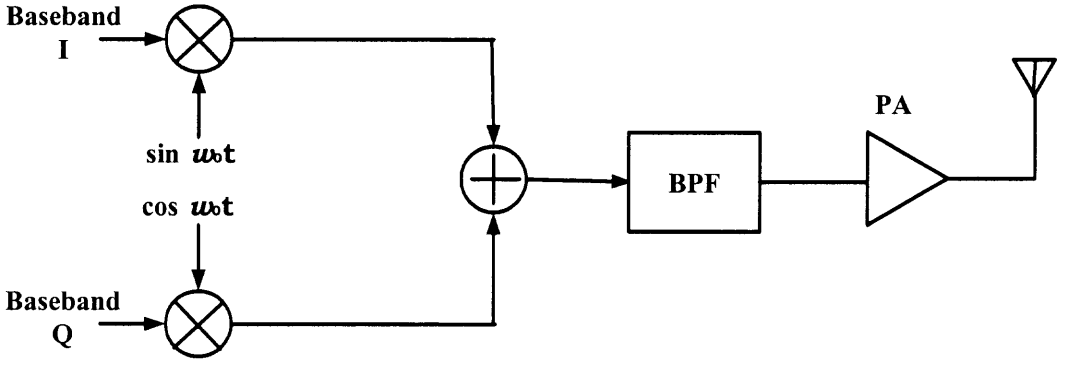

Figure 2.1 Direct conversion transmitter.

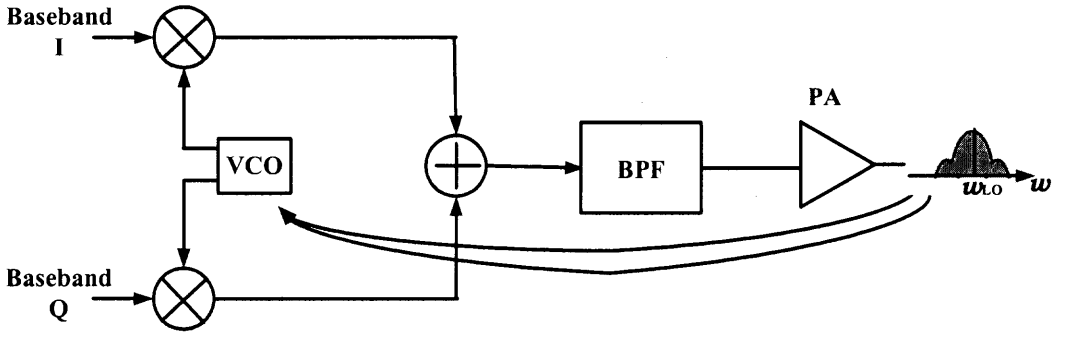

Figure 2.2 LO pulling by PA.

oscillator natural frequency, then the LO output is disturbed increasingly as the noise magnitude rises, eventually "locking" to the noise frequency. This phenomenon is alleviated if the PA output spectrum is sufficiently far from the oscillator frequency i.e. careful frequency planing avoids the pulling problem.

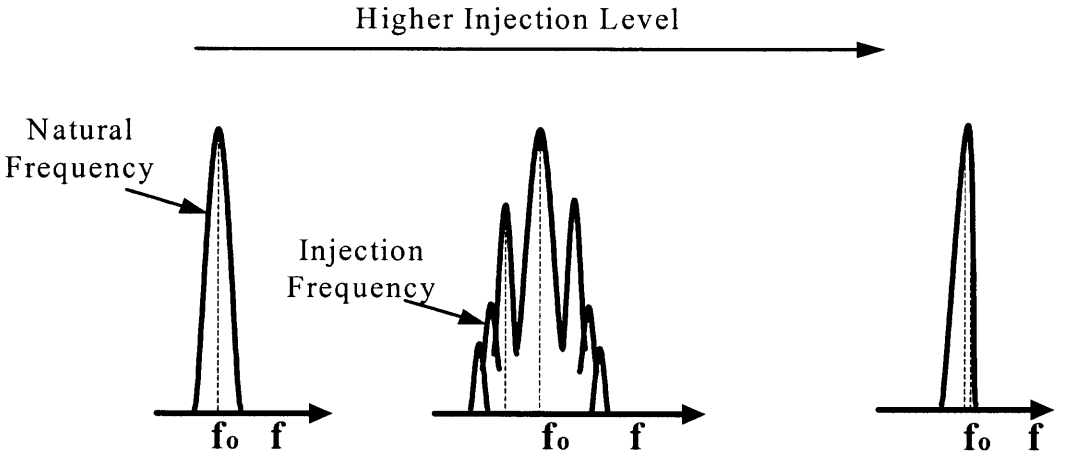

Figure 2.3 Injection pulling as the magnitude of the injected noise increase.

This Problem can also be avoided by "offsetting" the LO frequency i.e. by adding or subtracting the output frequency of another oscillator. Figure 2.4 shows an example where the output signals of VCO_1 and VCO_2 are mixed and the result is filtered that the carrier frequency,which is equal to $\omega_1+\omega_2$, far from either ω_1 or ω_2.

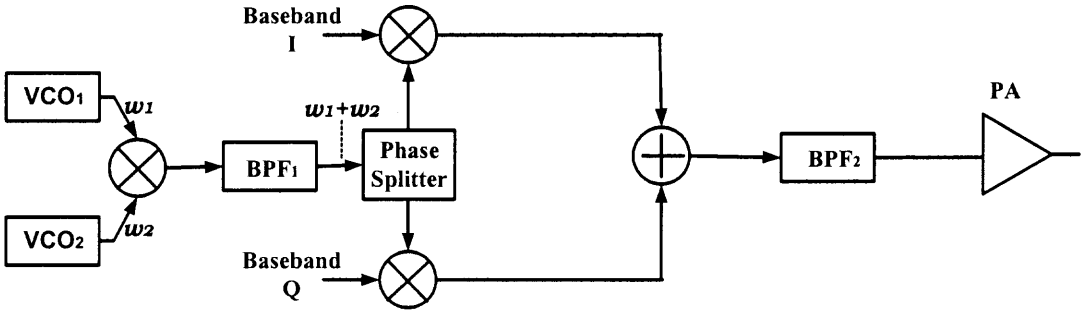

Figure 2.4 Direct-conversion transmitter with offset LO.

The selectivity of the first bandpass filter, BPF_1, in Figure 3.4 impacts the quality of the transmitted signal. Owing to nonlinearities in the offset mixer, many spurs of from $m\omega_1+n\omega_2$ appear at the input of BPF_1, If not adequately suppressed by the filter, such components degrades the quadrature generation of the carrier phases as well as create spurs in the unconverted signal.

2.1.1 Two-Step Transmitters

Another approach to circumventing the problem of LO pulling in transmitters is to upconvert the baseband signal in two (or more) steps so the PA output spectrum is far from the frequency of the VCOs. As shown in Figure 2.5, here the baseband Q and I signals undergo quadrature modulation at a lower frequency, ω1(called intermediate frequency (IF)), and the result is unconverted to $\omega_1+\omega_2$ by mixing and band-pass filtering. The first BPF suppresses the harmonics of the IF signal while the second removes the unwanted sideband centered around $\omega_1-\omega_2$ .An advantage of two-step upconversion over the direct approach is, the quadrature modulation is performed at lower frequencies.

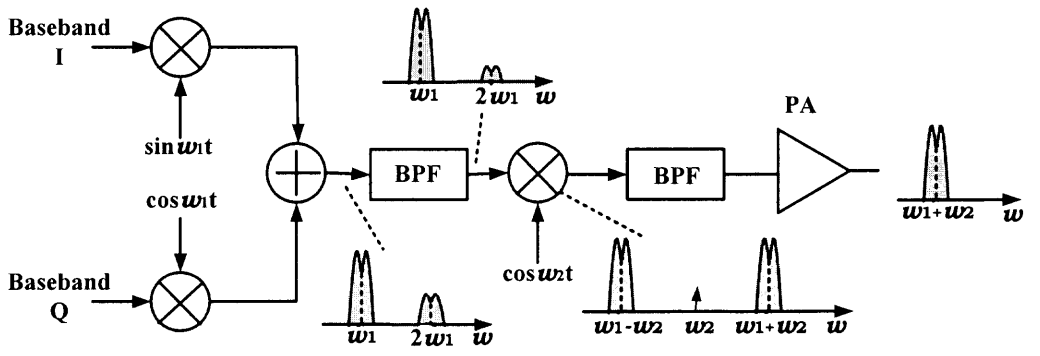

Figure 2.5 Two step transmitter.

The difficult in two-step transmitter is that the band pass filter following the second upconversion must reject the unwanted sideband by a large factor. This is because the simple upconversion mixing operation produces both wanted and unwanted sidebands with equal magnitudes.

2.2 Receiver Architecture

Complexity, cost, power dissipation and number of external components have been the primary criteria for selecting receiver architectures. There are several types of architectures implemented for different applications. [11-14,16]. Different receiver architectures are described below.

2.2.1 Homodyne Architectures

This type of architectures is also called "direct conversion" architecture. The homodyne receiver is the natural topology for down converting a signal from RF to base band. The idea is simple to mix the RF signal with a local oscillator (LO) output and low-pass filter. The result that the center of the band of interest is translated directly to zero frequency (Figure 2.6). Because of typically high noise, the mixer is usually preceded by an LNA.

In, phase and frequency modulation schemes, the RF signal is mixed with both the LO Output and its quadrature so as to provide phase information (Figure 2.7).

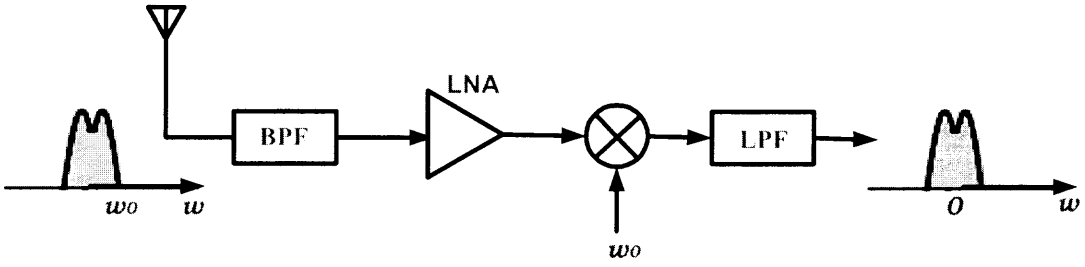

Figure 2.5 Homodyne architectures.

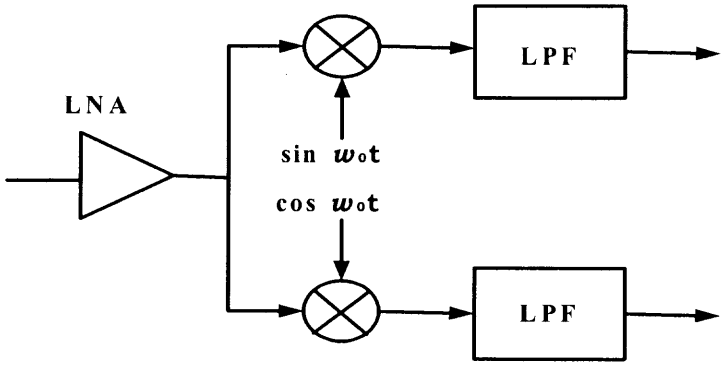

Figure 2.7 Homodyne receiver with quadrature downconversion.

The simplicity of the homodyne architecture makes it attractive for compact, efficient implementation of RF receiver. However several issues have impeded its widespread use. Description of these issues and their impact on the design of related ICs are briefly discussed.

2.2.1.2 DC Offsets. Since in homodyne receiver the down converted band extended to the vicinity of the zero frequency, extraneous offset voltage can corrupt the signal and, more importantly, saturate the following stages. To understand the origin and impact of

offsets, consider the more realistic circuit shown in Figure.2.8. Here, a low–pass filter, and a post–amplifier, follow the mixer. The isolation between the LO and RF ports of the

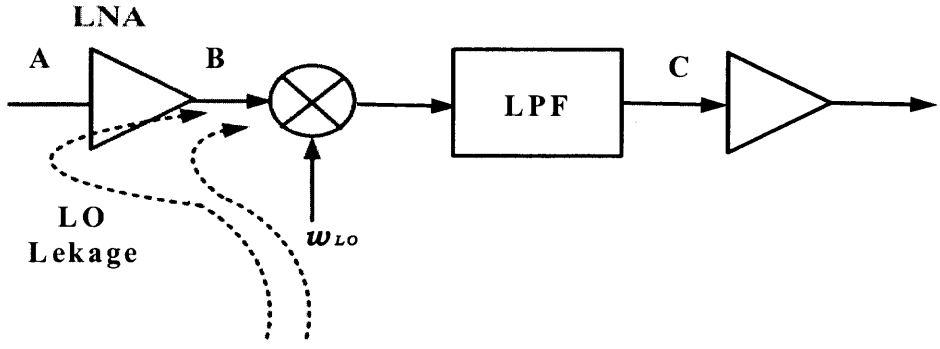

Figure 2.8 LO leakage input.

mixer is not perfect; due to capacitive coupling and, if LO signal is supplied externally, bond wire coupling, a finite amount of feedback through exists from the LO port to points A and B. this effect is called "LO leakage". This leakage signal appearing at the input of LNA is amplified and mixes with the LO signal, thus producing a dc component at a point C. this phenomenon is called "self mixing".

While high pass filter (i.e. AC coupling) may seem the solution here. But implementing such a filter in IC form is difficult, and more fundamental problem is its slow response, an important issue if the offset varies very quickly. For this reason, homodyne receivers required offset –cancellation techniques.

2.2.1.2 Even _order distortion. As depicted in Figure 2.9, if two strong interferes($x(t),x^2(t)$) close to the channel of interest experience a non-linearity is

$$y(t)= \alpha_1 x(t)+\alpha_2 x^2(t),$$

Then they are translated to a allow frequency before the mixing operation and result is passes through the mixer with finite attenuation. This is because, the mixer operation can

be viewed as x(t)(a+Acosωt),indicating that a fraction of x(t) appears at the output without frequency translation. an other issue is that the second harmonic of the input

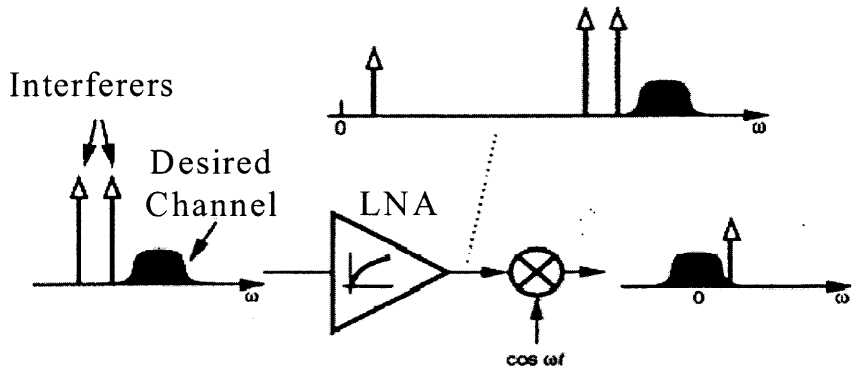

Figure 2.9 Effect second order distortions.

signal (due to square term in the above equation)is mixed with the second harmonic of the LO output, there by appearing in the base band and interfering with actual signal. For these reason this effect corrupt the base band signal.

Other issues like I-Q mismatching, Lo leakage and Flicker Noise also corrupts the base band signal.

2.2.2 Heterodyne Architecture

The issues mentioned above for the homodyne receiver have motivated the invention of other architectures. Most used is the heterodyne topology illustrated in Figure.2.10 in a simple form. Heterodyne receiver first downs convert the input to an "intermediate frequency". The resulting signal is band pass filtered, amplified, and down converted again. In the case of digital modulation, the last down convention generates both I and Q phases of the signal.

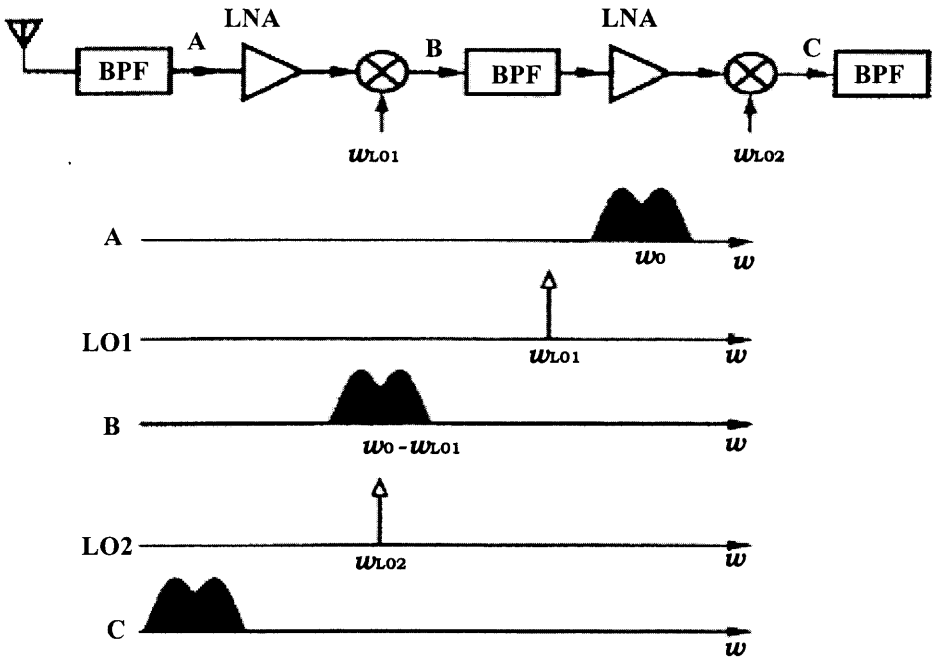

Figure 2.10 Heterodyne architecture.

The heterodyne architecture alleviates two of the homodyne reception issues by avoiding them at high frequencies or low signal levels. The effect of DC offsets of the first few stages is removed by band pass filtering, and that of the last stage is suppressed by the total gain in the preceding stages. Also Q and I mismatches occur at the lower frequencies and therefore it is easier to control and correct. As for the LO leakage, since ωLO1is out of the band of interest, it is suppressed by the front-end BPF and its radiation from the antenna is less objectionable.

The most important feature of heterodyne receiver is its selectivity i.e. the capability to process and select small signals in the presence of strong interference. The band pass filter is performed progressively at lower frequencies.

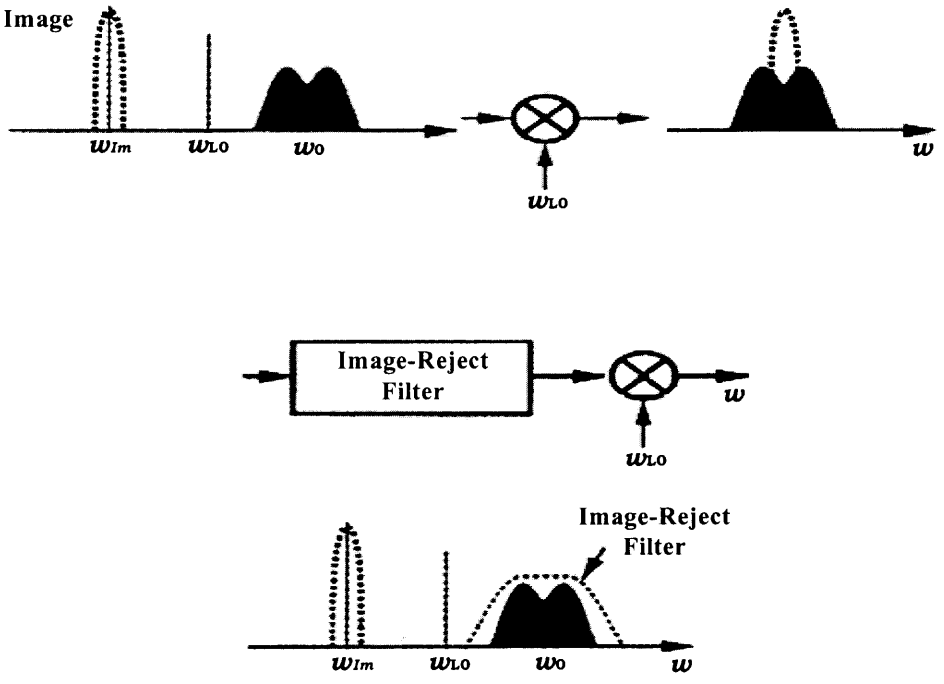

Figure 2.11 Problem of image and image rejection by filtering.

Despite of the above merits, heterodyning entails a number of drawbacks. The most important issue is the "image frequency" since a simple mixer does not preserve the polarity of the difference between its input frequencies, it translates the same frequency (Figure 2.11). Thus, the mixing operation must preceded by an image reject filter (Figure 2.11). This filter is designed to have relatively small loss in the desired band a large attenuation in the image band, two requirements that can be simultaneously met if 2ωIF is sufficiently large. A high IF leads to substantial rejection of the image whereas a low IF great suppression of nearby interferes. So the choice of selection of IF depends on trade-offs among three parameters: the amount of image noise, the spacing between the desired band and the image, and the loss of image filter.

2.2.3 Dual IF Topology

In simple heterodyne architecture, if the IF is high, the image can be suppressed but complete channel selection is difficult, and vise versa. To resolve this issue, the concept of heterodyne can be extended to multiple down conversions, each followed by filtering and amplification is illustrated in Figure 2.12

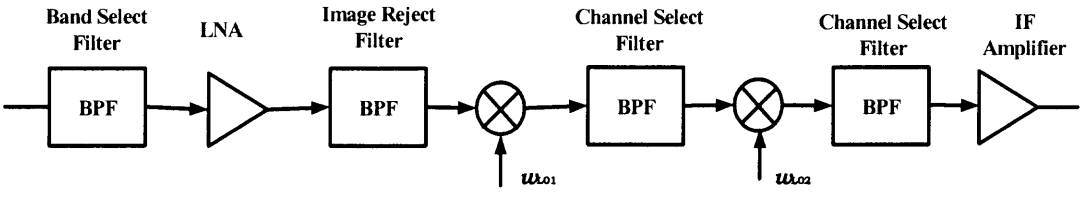

Figure 2.12 Dual IF topology.

2.2.4 Image –Reject Architectures

The issues related to the image-reject filter have motivated RF designers to seek other techniques of rejecting the image in the heterodyne receiver. One such technique Hartley architecture originating from a single sideband (SSB) modulator introduced by Hartley is

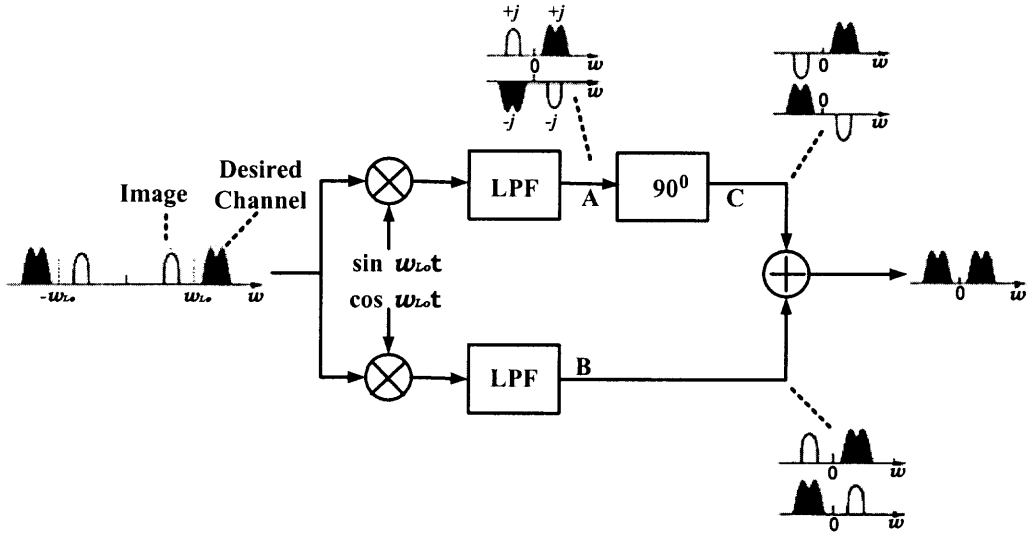

Figure 2.13 Image –Reject architectures.

shown in Figure 2.13. Hartley's circuits mixes the RF input with the quadrature output of the local oscillator, low pass filters the resulting signals, and shift one by 90^0 before adding them together.

The principle draw back of image –reject mixers id their sensitivity to mismatches. for example if phase difference between the LO quadrature phases deviates from 90^0 ,the cancellation are imperfect and some image noise corrupts the down converted signal.

2.2.5 Weaver Architecture

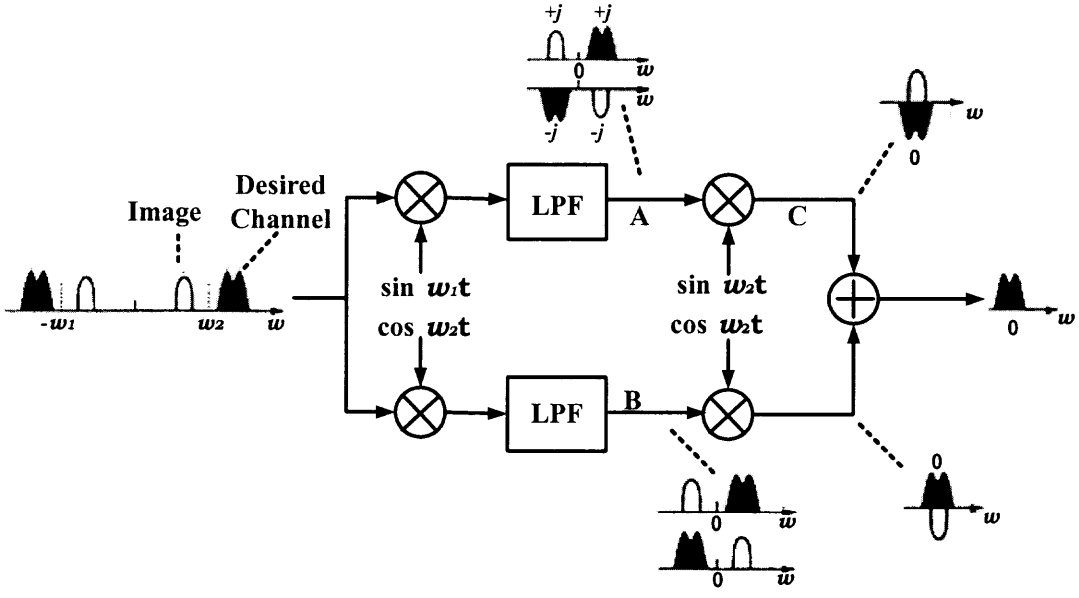

Figure 2.14 Weaver architecture.

As illustrated in Figure 2.14, this approach down converts signal in two steps. In the first step, the input is mixed with quardature phases of the first local oscillator and the result is low pass filtered, yielding the spectra at nodes A and B. In the second step, these signals are translated to zero frequency and added together, herby effecting image cancellation.

The important advantage of the waver architecture is that is does not require high-Q band pass filters. The waver method suffers from same draw back as the image reject mixers.

3.2 Proposed Architecture

The proposed transmitter architecture is shown in Figure 2.15. To achieve the highest level integration and to reduce cost and power consumption, the transmitter incorporates the direct conversion architecture. Similarly receiver incorporates the image reject architecture to eliminate the image reject filters needed between the LNA and mixer in the superheterodyne architecture. The differential circuit topology is employed throughout both the transmitter and receiver circuits to minimize the undesired coupling, especially the local oscillator leakage through the mixers to the antenna as it causes the dc offset to corrupt the desired signal.

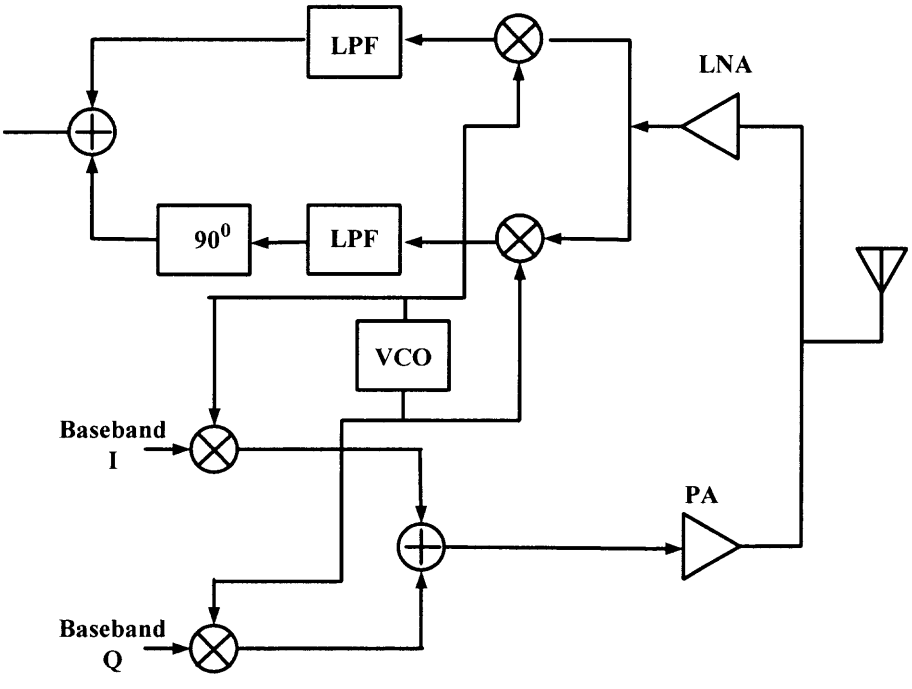

Figure 2.15 Proposed architecture of transceiver.

This transmitter IC comprises the Following key elements: a 1 GHz voltage controlled oscillator, two upconversion mixers and a power amplifier. The transmitter takes in baseband data, then after upconversion and power amplification, the output leading to the antenna to be propagated into air. 1 GHz fully differential VCO is at the core of transmitter architecture is a combination of two LC oscillators, which have both direct coupling and cross coupling connection to produce the inphase and quadrature phase components. This VCO is fundamental injection locked oscillator (ILO). The baseband signals(I-Q) of 1 GHz are directly upconverted in to RF by upconversion mixer driven by on chip fixed frequency 1GHz oscillator. The upconverted signals from the I-Q branches are then combined to produce the desired single-sideband while suppressing the unwanted image signals. Local oscillator harmonics are inherently canceled out due to the fully differential implementation of the VCO. Because of same frequency of both baseband and VCO signal, the upconversion mixer produces signals only at 2 GHz. Therefore no need of band pass filtering in this architecture. Finally signal is boosted by power amplifier, which equipped with signal driver before being propagated in to air by the 50Ω antenna.

As shown in the Figure 2.15, the receiver integrates the LNA, a set of mixers and an integrated quadrature VCO. Receiver gets the signal from the antenna and passed to LNA. LNA amplifies this weak signal from antenna. Set of mixers are followed by LNA, which are driven by quadrature LO signals from VCO. Mixer differential outputs are converted to single-ended operation with balun circuits.90^0 Phase shifter at mixer output is used to suppress the image signal before being further filtered and amplified by following stages. Similarly, baluns are used at other differential ports for measurements.

CHAPTER 3

DESIGN OF COMPONENTS FOR TRANSCEIVER

It is required to design various critical components for both transmitter and receiver. In this chapter all components (VCO, PA, Mixer and LNA) circuit diagram are designed.

3.1 Voltage Controlled Oscillator

In the spirit of single-chip integration of the transmitter, on-chip fixed-frequency voltage controlled oscillator is designed that do not require an external resonator as conventional oscillator topology deamands. The oscillator must exhibit low phase noise behavior, and produce a large swing to drive mixer directly without a RF buffer. Incidentally, these two requirements are in accord with each other, rather than in conflict.

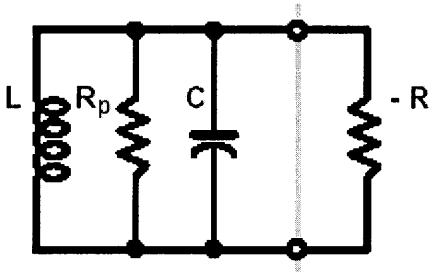

Figure 3.1 Oscillator core topology.

The classic oscillator topology in Figure 3.1 comprises a negative resistance block in parallel with an LC tuned circuit to compensate for the loss in the associated parasitic resistance. The negative resistance is often realized in bipolar implementations with a cross-coupled differential pair, and a single *LC* tuned circuit is connected to one end. In this implementation, the negative resistance is implemented by two cross-coupled

common-source FETs to enable a large voltage swing under the constraint of a 3.3 V supply. Inductor load can be replaced by a NMOS load with a voltage controlled resistor connected at its gate as shown in Figure 3.2. Clipping in the FET characteristics determines the amplitude of oscillation, and this in turn depends on the top-rail voltage.

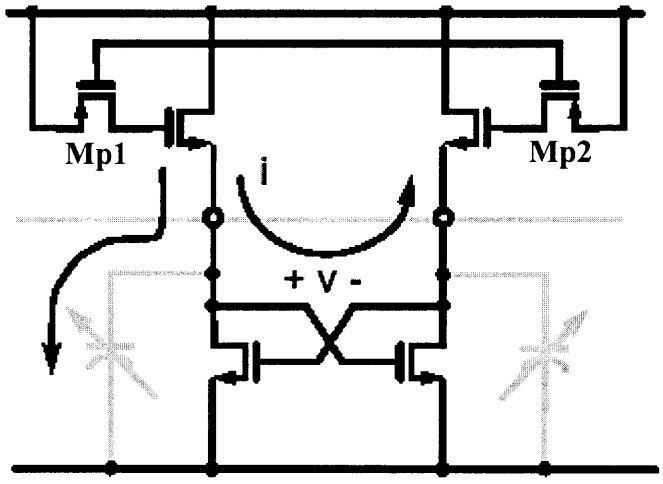

Figure 3.2 MOS implementation of oscillator core.

This variable resistor is implemented by using a PMOS (Mp1 and Mp2), and the resistance is varied by controlling the bias. The input impedance seen at the source of the simulated inductor load is complex, and at 1GHz it can be approximated by a real resistive part and a reactive part as illustrated in Figure 3.3; the real part can be thought of

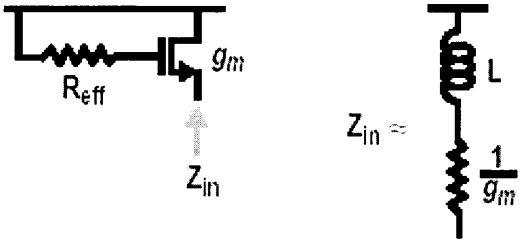

Figure 3.3 Input impedance of a simulated inductor load at 1GHz.

as the 'parasitic' resistance of the inductor. The derivation for the input impedance Z_{in} is as follows.

Using a small signal MOSFET model considering only the *gm* and C_{gs} for the ease of analysis, the input impedance looking into the source is

$$Z_{in} = (1 + S R_{eff} C_{gs}) / (g_m + S C_{gs}) = (j\omega Reff C_{gs} + 1)/(g_m + j\omega C_{gs})$$

At the operating frequency of 1GHz, $g_m >> \omega C_{gs}$ for a typical transistor. So Z_{in} can be approximated as

$$Z_{in} = (1 + j\omega R_{eff} C_{gs})/ g_m = (1/ g_m) + j\omega (R_{eff} C_{gs} / g_m) = Z_R + j\omega Z_L$$

where the equivalent inductance Z_L is directly proportional to the effective resistance of the PMOS, Reff, and is given by

$$L \approx R_{eff} C_{gs} / g_m = R_{eff} / \omega_T$$

where C_{gs} is the parasitic capacitance and *gm* is the current gain of the NMOS load.

By changing the resistance of the PMOS, the effective inductance can be varied, thus tuning the oscillation frequency. A useful balanced output is obtained from this oscillator with phases at 0° and 180°. The equivalent capacitance C in the oscillator of Figure 3.1 is the total capacitance at the drain of each FET, which is consisting of the NMOS load drain junction capacitance, the C_{gs} and effective C_{gd} of the opposite FET in the cross-coupled pair. The circuit will oscillate slightly above the resonant frequency of the inductor when the phase of the resonator is equal to -45°. The resonance frequency of the oscillator is

$$\omega o = \sqrt{(1/LC_{load})} = \sqrt{(g_m / R_{eff} C_{gs} C_{load})}$$

The Q of the simulated inductor is given by

$$Q = (\omega oL/r) = \omega o R_{eff} C_{gs} = \sqrt{(g_m R_{eff} C_{gs} / C_{load})}$$

3.1.1 Proposed Circuit Architecture

Instead of deriving quadrature phases from what is originally a single-phase oscillation with a phase-shift network, it is possible to use two identical oscillators together so they synchronize in quadrature. This entails a fundamental topology of coupling, shown in Figure 3.4 , which was first observed in vacuum-tube oscillators in 1934. Two identical oscillators, labeled A and B, are coupled together by FETs (M3, M4) of the same size as the main FETs (M1, M2), such that there is direct-coupling in one direction, and cross-coupling in the other. If the two oscillations synchronize in-phase, then the crosscoupled path from Oscillator B to A absorbs the negative-resistance current produced by M1A, M2A. So that Oscillator A ceases. The FETs in Oscillator A pull up both drain nodes to V_{dd}, and through the cross-coupled FETs , Oscillator A shuts off Oscillator B. The same process applies in reverse if the two oscillations are in 90° phase shift. Therefore, the oscillations only co-exist when they synchronize in quadrature. They then acquire the unique combination of 0° at M1A, 180° at M2A, 90° at M1B, and 270° at M2B.

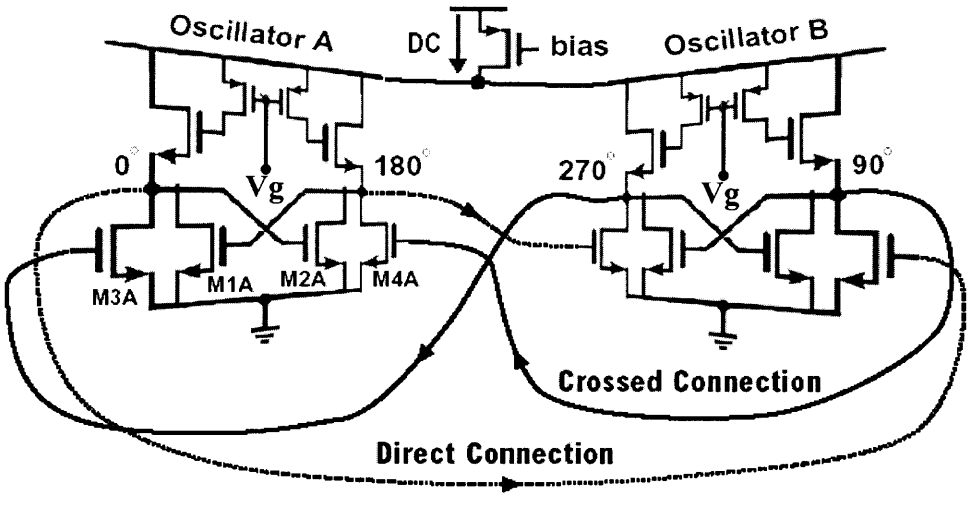

Figure 3.4 Oscillator synchronized in quadrature using simulated inductor load.

There are two ways to tune the frequency in Figure 3.4. Fine tuning is accomplished by varying the effective inductance presented at the load of the oscillator via Reff. Coarse tuning, on the other hand, relies on varying the oscillator load capacitance, and in particular, the junction capacitance of the FETs. Changing the bias of the PMOS resistor that connects to the top rail of both oscillators A and B will chage top rail voltage, and therefore indirectly control the junction capacitance. These tuning techniques where the frequency tuning is not controlled by varying a current source as it is typically done in ring oscillators, any phase noise due to frequency modulation is eliminated.

3.1.2 Injection Locking

In the design of transmitter main problem is interferences of the local oscillator by PA output. As shown in Figure 2.2 this is signifiacnt because the PA output waveform is modulated with high power and a spectrum centered around the VCO frequency. Thus the output of PA corrupts the oscillator spectrum. This problem is reduced by appropriate injection locking.

Injection locking [18] is a well known physical phenomenon, is achieved by impressing an oscillator with an external (incident) signal. Therefore that an oscillator's output frequency tracks the frequency of an injected signal within a limited bandwidth. This bandwidth, called the locking bandwidth, is dependent on the quality factor Q of the oscillator and on the magnitude of the injected signal. Once locked to the injected signal, the frequency drift of a free-running oscillator is eliminated. Injection locking allows well characterized VCO stabilization and frequency synchronization. ILO's are three types: first-harmonic, subharmonic and superharmonic ILO's. In first-harmonic ILO, the

oscillation frequency is the same as the fundamental frequency of the incident signal, while in a subharmonic ILO, the incident frequency is a subharmonic of the oscillation frequency. Likewise, in a superharmonic ILO, the incident frequency is a harmonic of the oscillation frequency. In our design fundamental injection locking is used.

3.2 Power Amplifier

In transmitters design, the integration of one of the essential components, the power amplifier (PA), is a difficult challenge. For applications requiring moderate-to-high output power, the PA contributes significantly to the total transmitter power consumption, making the PA efficiency crucial to the overall system performance. Realizing high-efficiency PA's in CMOS, however, is impeded by the technology's low breakdown voltage, low current drive, and lossy substrate. In addition, the efficiency achieved in traditional approaches (e.g., classes A, B, AB, and C), is often optimized merely at the maximum output power, which typically accounts for only a small portion of time in a transceiver's normal operation. Class D, E and S amplifiers utilize the active devices as a switch and hence the theoretical maximum efficiency is 100%, assuming that the device has zero switching time, zero on-resistance and infinite off-resistance. However, in reality, the turn-on resistance of the switch, and the loss in the on-chip inductors limit the efficiency. Class E switch amplifier is generally used for wireless applications.

Figure 3.5 shows a conceptual picture of a class-E power amplifier . In operation, the input signal V_{in} toggles the switch periodically with approximately 50% duty cycle. When the switch is on, a linearly increasing current is built up through the inductor.

When the switch is turned off, this current is steered into the capacitor, causing the voltage across the switch V_s to rise. The tuned network is designed such that in steady state, V_s returns to zero with a zero slope, immediately before the switch is turned on.

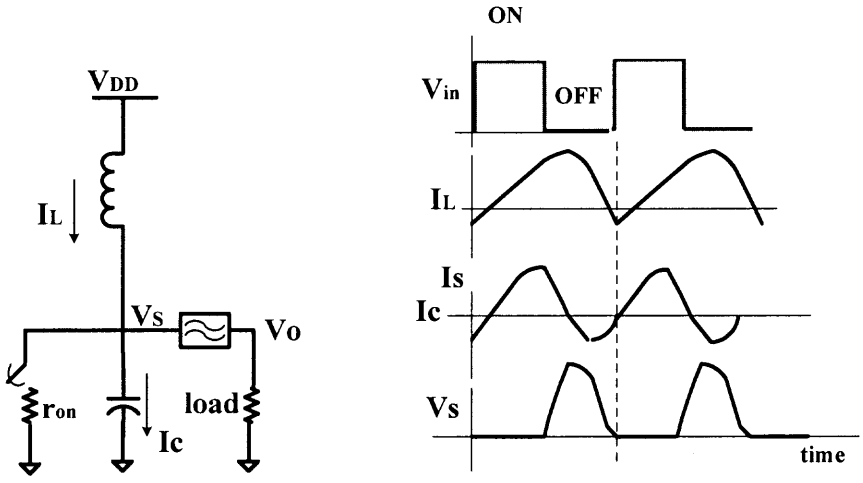

Figure 3.5 A simplified class-E PA and its steady-state operation.

The bandpass filter then selectively passes the fundamental component V_s to the load, creating a sinusoidal output that is synchronized in phase and frequency with the input.

By analyzing V_s and I_s (Figure 4.5.), the switch voltage and the switch current are never simultaneously nonzero. Since the instantaneous power dissipation of the switch is the product of these two quantities, the switch is ideally lossless, and all the power from the dc supply is delivered to the radio-frequency (RF) output. In addition, the capacitor is designed to be fully discharged before the switch is turned on. This property, commonly known as "soft switching," eliminates any $1/2CV^2$ discharging energy loss.

When the switch is turned on, current is not being drawn actively through the triode transistor. Instead, it is being forced through the transistor by the inductor. Since the IR drop across the transistor is normally very small compared with V_{DD}, the exact

value of the on-resistance r_{on} does not significantly affect the current circulation in the tuned load network. The voltage and the current waveforms, as well as the output power becomes insensitive to the detailed transistor characteristics.

Since the input provides only timing information in a class-E PA, the output power cannot be controlled through the input like what is normally done in a linear or weakly nonlinear amplifier. Instead, output power control can be realized effectively through a variable power supply, implemented, for example, by a dc–dc converter. Since V_{DD} is the only voltage reference in the switching circuit, every node voltage is proportional to V_{DD} , and every power term, including the output power, is proportional to V_{DD}^2 . This means that the output power is controllable through the supply voltage, which leads to the potential of maintaining a constant efficiency over a wide range of output power. This is illustrated in Figure 3.6, here we assume, without loss of generality, that the only loss is from the finite switch on-resistance r_{on}. Since both the loss and the output power scale with V_{DD}^2 (P_{OUT} , $P_{LOSS} \alpha V_{DD}^2$) , their ratio, and the overall efficiency, is virtually unaffected as the output power is adjusted through the variable supply.

$$\text{Efficiency} \quad \eta = P_{OUT} / (P_{OUT} + P_{LOSS}) = \text{Constant}$$

The single-ended circuit in Fig. discharges a large amount of current to ground, or the silicon substrate, once per cycle. This generates an unwanted substrate noise component at the same frequency as the desired signals, which is particularly undesirable in an integrated environment. Also the input driving requirement is a problem with single ended circuit.

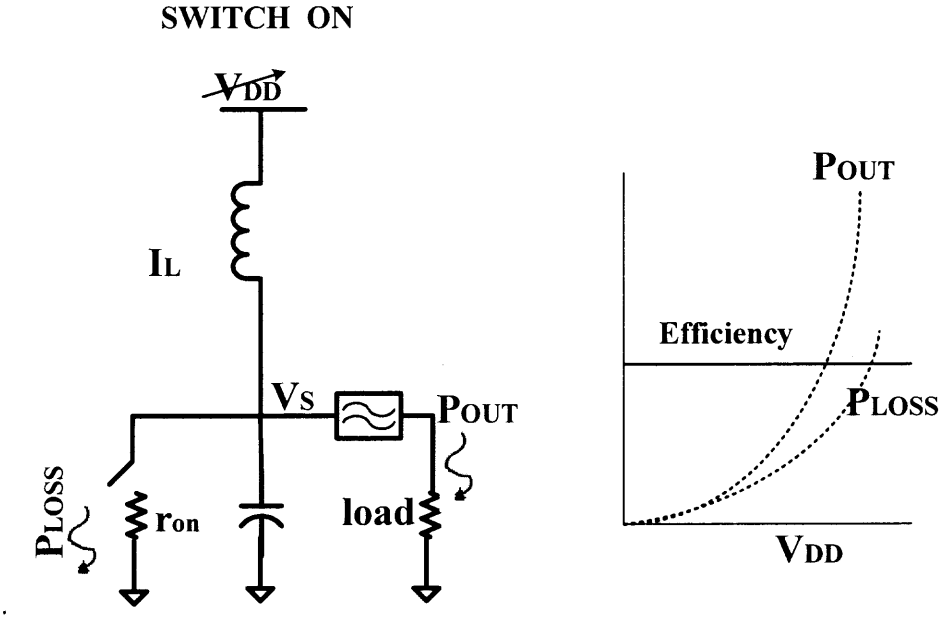

Figure 3.6 Constant efficiency over supply voltage.

3.2.1 Circuit Diagram

Figure 3.6 shows a two-stage CMOS class-E power amplifier designed to operate in the gigahertz frequencies. A fully differential configuration is used to alleviate the problem of substrate coupling. In a fully differential configuration, current is being discharged to ground twice per cycle. This expels the substrate noise component from the desired signal frequency to twice the signal frequency, resulting in a reduced interference. In addition, for the same supply voltage and output power, the current passing through each switch in a differential configuration is lower than its single-ended counterpart. This allows a smaller transistor to be used on each side without increasing the total switch loss. A differential configuration alone, however, might not provide sufficient relief to the transistor's input driving requirement, especially when large on/off driving signals are needed. To mitigate this problem, the technique of mode locking is used.

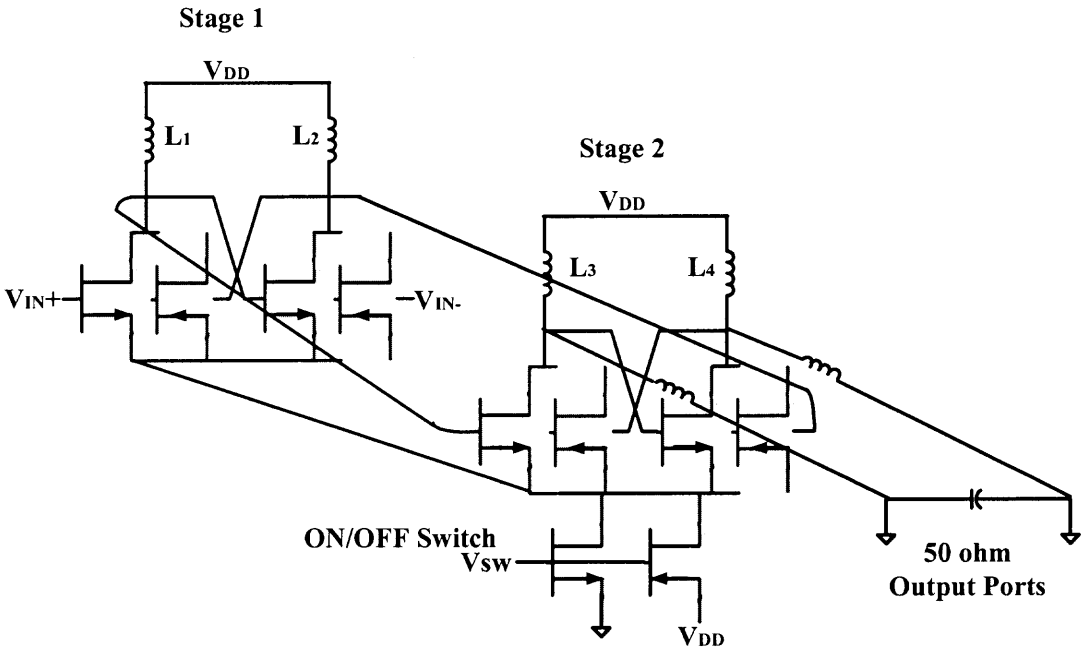

Figure 3.7 Schematic of the complete power amplifier.

3.2.2 Mode Locking

Mode locking refers to the condition in which an otherwise self-oscillating circuit is coupled and forced to run at the same frequency as input signal, resulting in a substantial

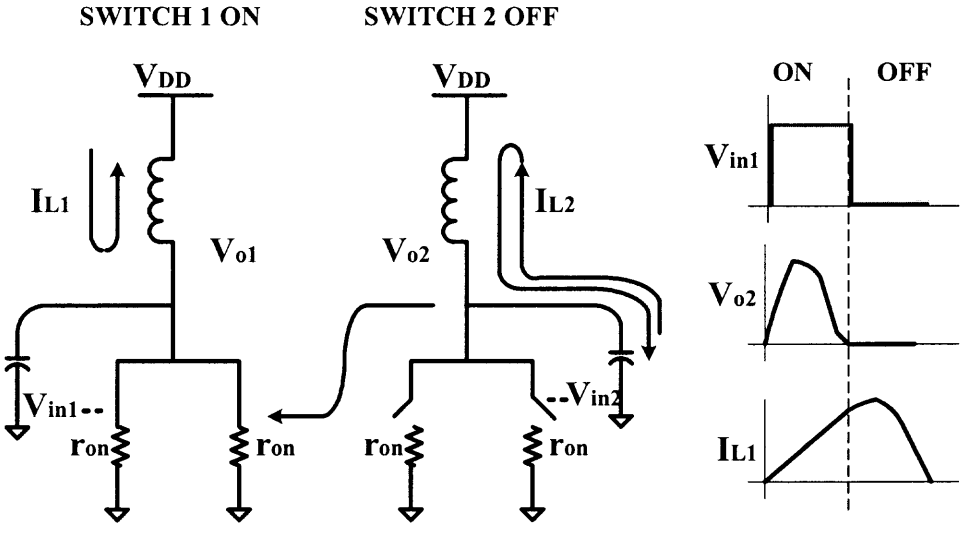

Figure 3.8 Illustration of the mode-locking concept.

reduction in the input driving requirement. This is realized in each stage of the amplifier by a pair of cross-coupled assisting devices, as shown in Figure 3.8. The two input voltages are out of phase, as are the two output voltages. The load impedance at the output nodes is designed such that and run in phase to control the composite switch. As far as each half circuit is concerned, the operation is similar to the single-ended version as shown in Figure 3.5, except for two features. First, the current originally circulating at each tuned load is now utilized to assist switching of the other half circuit. Second, the capacitance at each input can now be significantly reduced without increasing the overall composite switch on-resistance.

3.3 Mixer

In transceiver, mixers directly follow the VCO to convert the baseband signals into the desired RF band. While it is desirable to achieve high conversion gain and low intermodulation distortion in the output signal, there are also practical implementation considerations such as mismatches and un-balances in the circuits, which cause LO signal feedthrough.

In terms of conversion gain, mixers can be divided into two types, which are passive and active. The advantage of the passive mixers is better linearity, but the disadvantages are conversion loss, higher Noise Figure (NF) and larger LO power. In contrast to the passive mixers, the active mixers provide conversion gain, lower NF and demand smaller LO power. A smaller LO power requirement is very important in mixer design. There are several reasons. First, it is difficult to generate large LO power in low voltage and low power design. Second, larger LO power means larger LO-to-RF

feedthrough, which results in LO signal leaks through the antenna and becomes a strong interference to other RF systems. Third, reducing the required LO power also indicates that improve the LO-RF and LO-IF isolation.

Active mixers are again divided in to three types.

1. Single ended mixers (SEMs)

Principle: Mixer perform its function through its nonlinearity

No isolation between RF, LO, and IF.

2. Single-balanced mixers (SBMs)

Principle: Mixer directly implement a multiplication

Only isolates between LO and RF. IF is not isolated from RF, LO.

3 .Double-balanced mixers (DBMs)

Principle: Mixer directly implement a multiplication

The isolations available between LO, RF, and IF

3.3.1 Proposed Architecture of Mixer

The Gilbert cell mixer is a double balanced active mixer, chosen for transmitter because this mixer style provides reasonable conversion gain (IF power output with respect to the RF power input), good rejection at the RF and LO ports, and a differential IF output connection. The good rejection characteristics are achieved by cancellation of the undesired generated signal components by the out of phase driver components (RF and LO). The RF and LO signals must be fed 180^{o} out of phase to the mixer input ports.

In a Differential Pair, the small-signal gain of the circuit is function of the tail and the two transistor Differential pair provides a simple means of steering the tail current to one of two destinations. By combining these two properties, if a control voltage controls

the tail current of the Differential pair, then gain is a function of controlled voltage(LO voltage). This circuit can be called as Variable Gain Amplifier (VGA) as shown in Figure 3.9

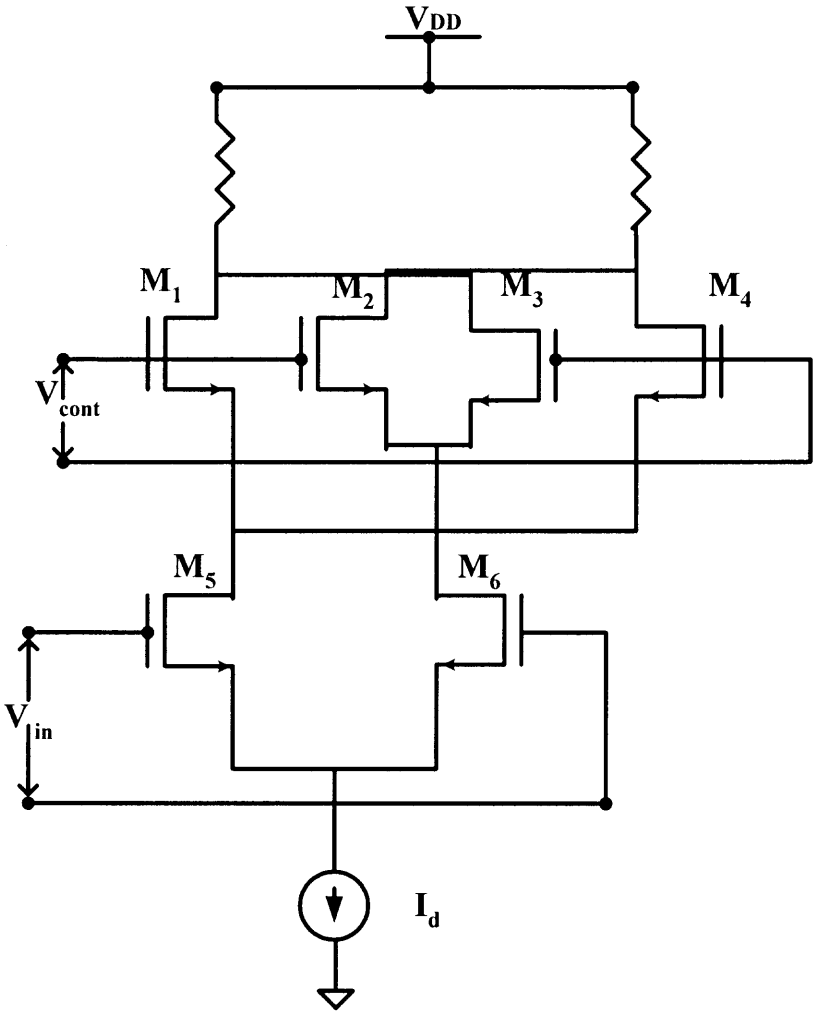

Figure 3.9 Gilbert cell mixer.

It is clear that the output voltage is the product of the input voltage (RF voltage) (V_{in}) and the gain (A_v). However, gain (A_v) is a function of control voltage (V_{cont}). Thus, the Output Voltage (V_{out}), can be expressed as follows

$$V_{out} = V_{in} * f(V_{cont})$$

For small values of V_{cont}, the Taylor's expansion of f (Vcont) is approximately equal to V_{cont}. Hence, the Output Voltage is the product of input voltage (V_{in}) and Control Voltage (V_{cont}).

$$V_{out} = (V_{in} * V_{cont})$$

The output can be approximated to the product by making both inputs into small signals. In the circuit (Figure 3.9) the control voltage controls the drain currents of the transistors M5 and M6, thus it controls the gain of the differential pair M5, M6. The output of the differential pair is function of the input voltage V_{in} and V_{cont}.

As a cascode structure, the Gilbert cell consumes greater voltage headroom than a simple differential pair does. This is because the two differential pairs M1-M2 and M3-M4 are "stacked" on top of the control differential pair. In order for the M5-M6 to be in saturation the difference of the common mode levels of the input and control voltage must be atleast $V_{GS1} - V_{TH5}$.

3.3.2 Design of the Mixer

The current in the current mirror is assumed to be equal to 1mA, and the drain voltage Vdd, is 3.3V. As there are four cascode stages the V_{ds} across current mirror is assigned as 0.3V, and across the transistors M5-M6 as 0.8V and across M1-M4 as 0.8V and across the resistors as 0.8V.

The W/L values of the transistors are obtained by using the following formula:

$$I_{ds} = K` W/L V_{ds}^2$$

3.4 Low Noise Amplifier

One of the key circuits in the RF front-end of mobile communications is Low-Noise Amplifier. The LNA amplifies a weak signal coming from an antenna. The amplified output from the LNA is then fed in to a mixer. In the design of low noise amplifiers, there are several common goals. These include minimizing the noise figure of the amplifier, providing gain with sufficient linearity and providing a stable 50Ω input impedance. The additional constraint of low power is imposed in portable systems.

3.4.1 LNA Architecture

With above goals in mind, requirement of providing stable input impedance is focused first. To provide input impedance, a number of circuit topologies as shown in Figure 3.10, were examined and their advantages and disadvantages are discussed below. The

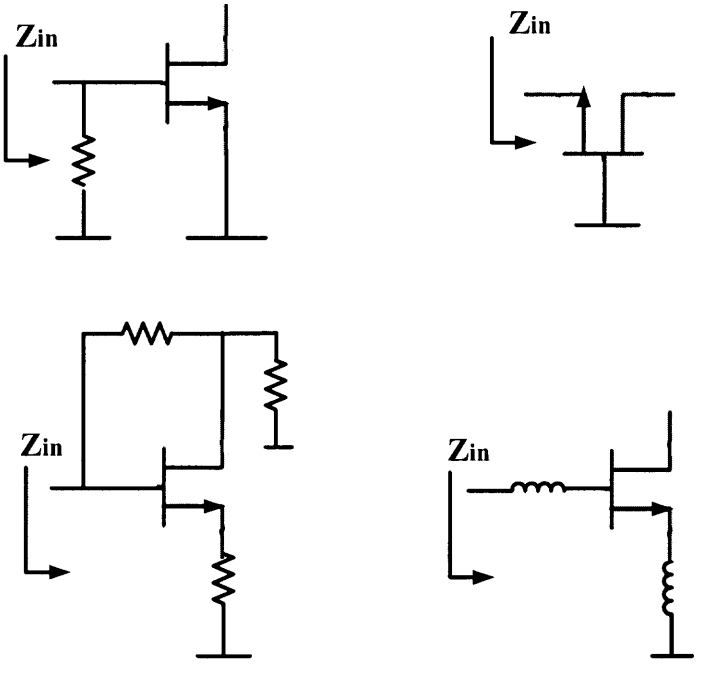

Figure 3.10 Common LNA architectures (a) Resistive termination (b) 1/ g_m termination (c) Shunt-series feedback (d) inductive degeneration.

input impedance of a MOSFET is inherently capacitive, so providing a good match to a 50Ω resistance without degrading noise performance would appear to be difficult. Simply putting a 50Ω resistor across the input terminals of a common source amplifier, as shown in Figure 3.10(a), adds thermal noise while attenuating the signal ahead of the transistor. This produces unacceptably high noise figures. Another method as shown in Figure 3.10(b) for realizing a resistive input impedance is to use a common-gate configuration since the resistance looking into the source terminal is 1/gm; a proper selection of device size and bias current can provide the desired 50Ω resistance. But the noise figure of this configuration would be high for high frequencies due to the gate current noise of the transistor. The third configuration (Figure 3.10(c)) uses a resistive shunt and series feedback to set the input and output impedances of the LNA. But this has high power dissipation compared to others with similar noise performance. The fourth architecture shown in Figure 3.10(d), employing an inductive source degeneration, is the best method. With such an inductance, a real term in the input impedance can be generated without the need of real resistances which degrade the noise performance. To simplify the analyses, if we consider a device model that includes only a transconductance and a gate-source capacitance, it can be seen that the input impedance of the circuit is

$$Z_{in} = sL_g + 1/(sC_{gs}) + g_{m1}(L_s/C_{gs})$$

$$= sL_g + 1/(sC_{gs}) + \omega_T L_s$$

where $\omega_T = g_{m1} / C_{gs}$

Hence, the input impedance is that of a series RLC network, with a resistive term that is directly proportional to the inductance value. At the series resonance of the input circuit, the impedance is purely real and proportional to L_s. By choosing Ls appropriately,

this real term can be made equal to 50Ω. The gate inductance L_g is then set by the resonance frequency once the L_s is chosen to satisfy the criterion of a 50Ω input impedance. The equivalent circuit for the input stage of the amplifier is shown in Figure 3.11.

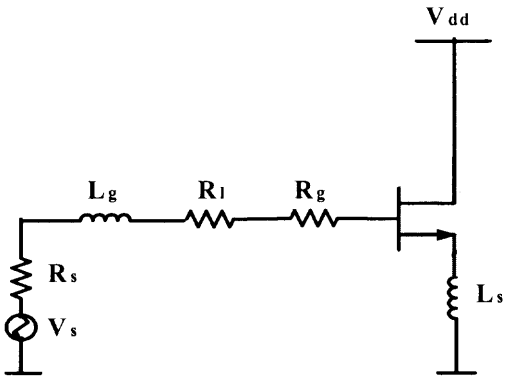

Figure 3.11 Equivalent circuit.

3.4.2 Noise Figure

The noise figure of the LNA can be computed by analyzing above equivalent circuit. Rl represents the series resistance of the inductor L_g, and R_g is the gate resistance of the NMOS device. Analysis based on this circuit neglects the contribution of subsequent stages to the amplifier noise figure. The overlap capacitance C_{gd} is neglected for simplicity.

The noise factor for an amplifier is defined as

F= Total output noise / Output noise due to the source

To evaluate the output noise, transconductance of the input stage need to be evaluated first. With the output current proportional to the voltage on C_{gs},

$$G_m = g_{m1} Q_{in}$$

$$= \omega_T / (\omega_0 R_s (1+ \omega_T (L_s/ R_s))$$

$$= \omega_T / (2\omega_0 C_{gs})$$

which is valid at the series resonance ω_0 , where Q_{in} is the effective Q of the amplifier input circuit. R_l and R_g have been neglected relative to the source resistance. As seen, the transconductance of this circuit at resonance is independent of g_{m1} (the device transconductance) as long as the resonant frequency is constant. If the width of the device is adjusted, the transconductance of the stage will remain the same as long as L_g is adjusted to maintain the fixed resonant frequency. If we reduce the size of transistor M_1 without changing any bias voltages, the device transconductance would also shrink by the same factor, and the inductances would have to increase (by the same factor) to maintain resonance. Since the ratio of inductance to capacitance increases, the Q of the input network must increase. The increase in Q cancels precisely the reduction in device transconductance, so that the overall transconductance of the circuit remains unchanged.

Using above Equation for the transconductance, the output noise power density due to the 50Ω source resistance and due to R_l, R_g and the channel current noise of the first MOS device is computed. Final simplified equation for the noise figure

$$F= 1+ (R_l / R_g) + (R_g / R_s) + \gamma g_m (\omega_0 / \omega_T)^2$$

This equation shows that we can improve the noise figure and reduce the power consumption simultaneously by reducing g_m and without modifying ω_T (although this is probably different from our first intuition). This can be achieved by scaling the width of the device while maintaining constant bias voltages. In this equation, the Flicker noise at this frequency is neglected with respect to the channel thermal noise.

As the amplifier is operated at series resonance of its input circuit, a reduction in g_m (and hence in C_{gs}) must be compensated by an increase in Lg. So, better noise performance and reduced power dissipation is obtained by increasing the Q of the input circuit resonance. However, at resonance of the RLC series tank, the voltage drop at the capacitance C_{gs} will be Q times input voltage V_{in}. This has a direct influence on the distortion. We also know that for the MOSFET in the common source configuration, the third order intermodulation coefficient is proportional to the square of the gate source voltage, and therefore the distortion is propotional to Q^2. Thus, there is a trade-of between the noise performance and the distortion, as reducing the size of the transistors to decrease the noise figure increases the level of distortion.

3.4.3 Circuit Design of LNA

The basic input circuitry has already been discussed, so to complete the design, it requires only the addition of bias and output circuitry.

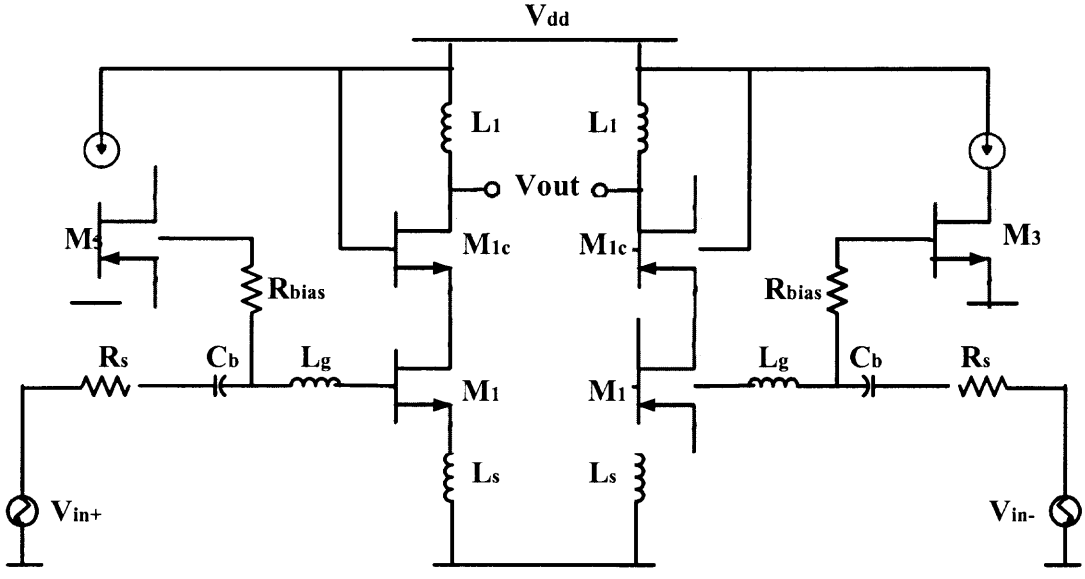

Figure 3.12 Schematic of the LNA.

As shown in Figure 3.12 differential LNA, the Cascoding transistor M_{1C} is used to reduce the interaction of the tuned output with the tuned input, and to reduce the efficient of M_1's Cgd. The total node capacitance at the drain of M_{1C} resonates with the inductance L_l, both to increase the gain at the centre frequency and simultaneously to provide an additional level of highly desirable bandpass filtering. The input and output resonances are set equal to each other. Transistor M_3 forms a current mirror with M_1, and its width is a small fraction of M_1's to minimize the power overhead of the bias circuitry. The current through M_3 is set by the constant g_m circuitry as shown in Figure 3.13,this provides constant gm for different temperatures, in other words, a current that is directly proportional to the temperature.

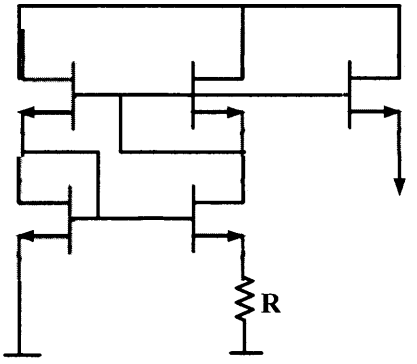

Figure 3.13 Current source for constant g_m biasing.

Large value of resistance R_{bias} is chosen so that its equivalent noise current is small enough to be ignored. To complete the biasing, a DC blocking capacitor C_B must be present to prevent upsetting the gate-to-source bias of M_1. The value of C_B is chosen to have a negligible reactance at the signal frequency. Differential configuration was used as the single ended architecture is sensitive to the parasitic ground inductance. As seen from the figure, the ground return of the signal source is supposed to be at the same

potential as the bottom of the source degenerating inductor. However, there is inevitably a difference in these potentials because there is always some nonzero impedance between these points. Since Ls is not a large inductance, small amounts of additional parasitic reactance between the grounds can have a large effect on amplifier performance. In the differential configuration, the incremental ground at the symmetrical point is exploited (i.e. the point at where the source degenerating inductances return to a virtual ground). Any parasitic resistance in series with the inductance is irrelevant. The real part of the input impedance is controlled by Ls and is unaffected by parasitics in the ground return path. Another important attribute to the differential connection is its ability to reject common-mode disturbances. To maximize common mode rejection at high frequencies, it is critically important for the layout to be absolutely as symmetrical as possible. Lastly, the linearity is improved in this configuration as the input voltage is divided between two devices.

CHAPTER 4

LAYOUTS AND SIMULATION RESULTS

The layout and the experimental results of all circuit components, the complete transmitter and receiver using TSMC 0.35μ technology, are presented in this chapter. All layouts are drawn to avoid the transmission line effects, to optimize the power dissipation and to optimize the area.

4.1 Layouts

Layout of Voltage Controlled Oscillator (VCO) is shown in the Figure 4.1.Layout is symmetrical, differential and it is designed to produce 1Ghz Frequency outputs with quadrature phases. Total 21 transistors are used in this layout with fixed length of 0.4μm and variable width of 10μm to 100μm.

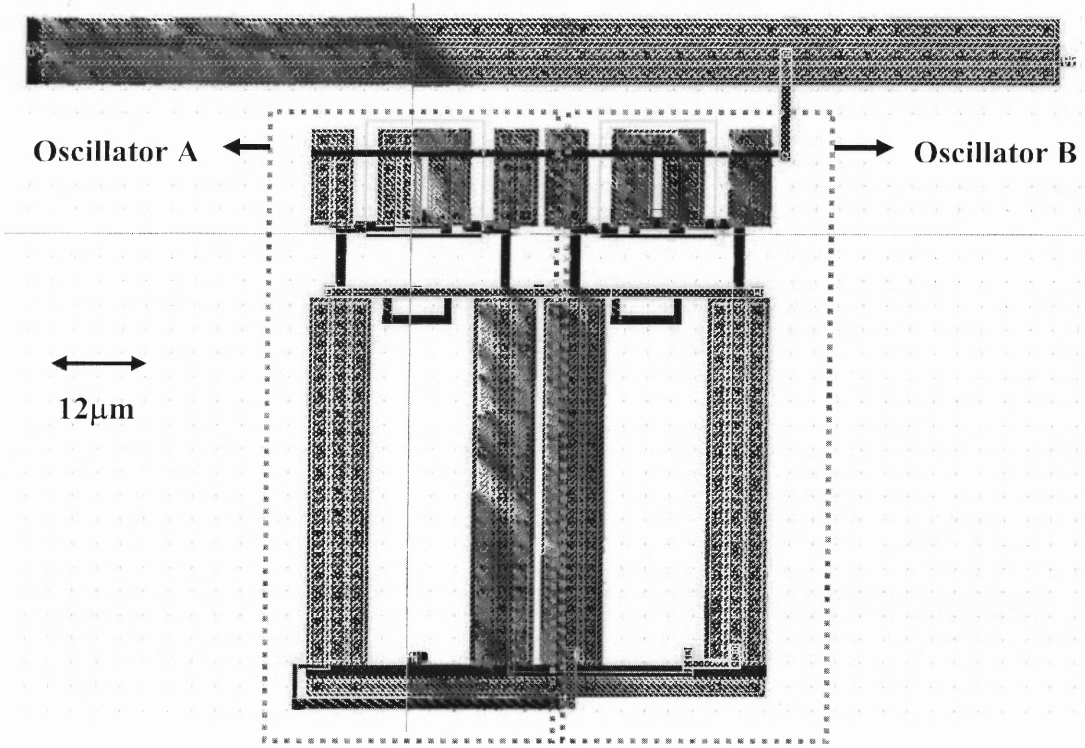

Figure 4.1 Layout of VCO.

Figure 4.2 shows the layout of the Power amplifier with mode technique. Differential configuration is used to avoid substrate coupling. six Inductors(Four 0.37nH and two 0.8nH) are used in this layout. Four 0.37nH inductors, with 5 turns,

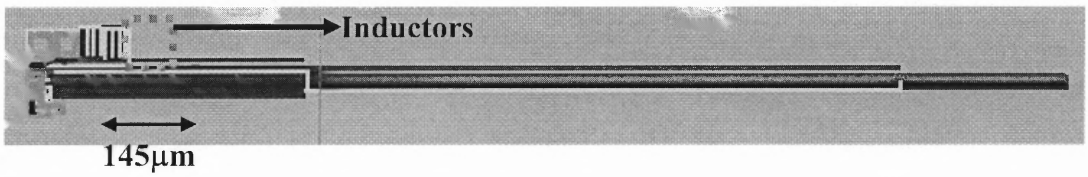

Figure 4.2 Power amplifier layout.

25μm length,1μm width and 1μm spacing are first simulated using ASITIC tool and imported into layout. Similarly two 0.8nH inductors, with 4 turns, 44μm length, 1μm width and 1μm spacing are simulated and imported. Metal M3 and M2 are used for all inductors.

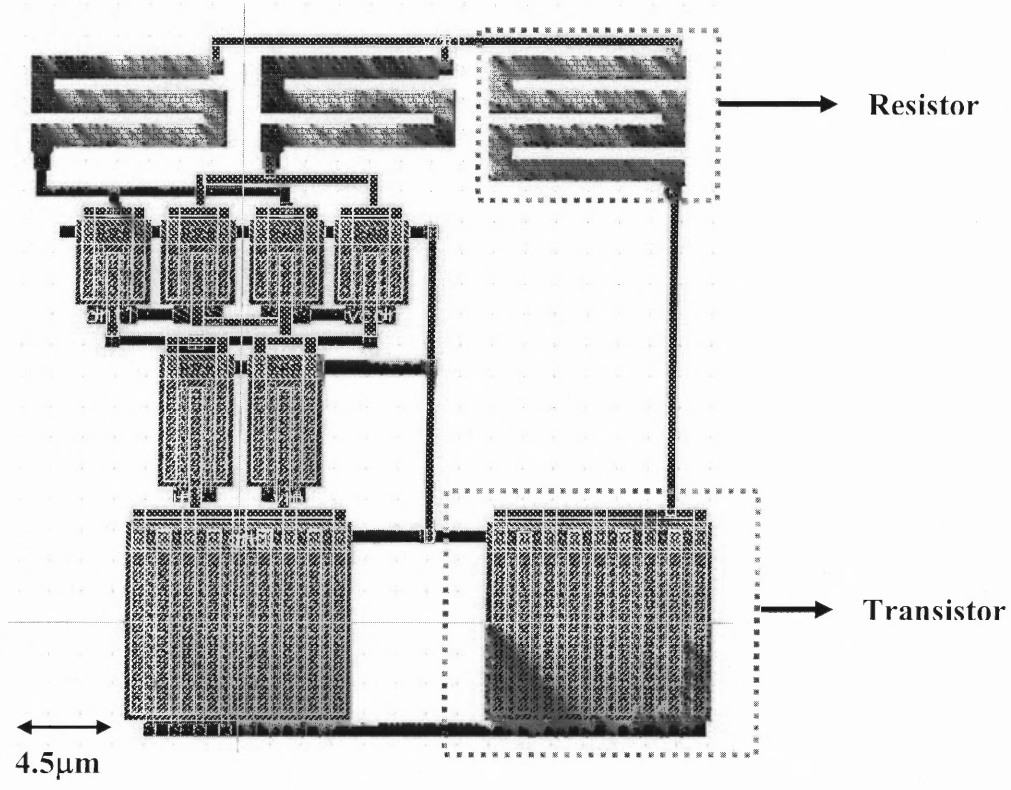

Figure 4.3 Layout of mixer circuit.

A Gilbert's cell is used to multiply the outputs. Its layout is shown in Figure 4.3 .it is double balanced mixer with 7 transistors with fixed length of 0.4μm and variable width of 6μm to 80μm. Second ploy is used for resistors. The total area of mixer is $45X44\mu m^2$.

Low Noise Amplifier (LNA) layout is shown in Figure 4.4. It is completely symmetrical to improve the matching between two differential ends. This layout also has six inductors, two capacitors and two resistors. The two capacitors are drawn using polysilicon. 5 Turns, 46μm length, 1μm width and 1μm space is used for two 0.26nH inductors. The 4.6nH inductors are designed with 12 turns, 57μm length, 1μm width and 1μm spacing. The other two 25nH inductors have 10 turns, 102μm length, 1μm width and 1μm spacing. All inductors are drawn and simulated in ASITIC and imported into final LNA layout. The circuit is designed for 2GHz frequency.

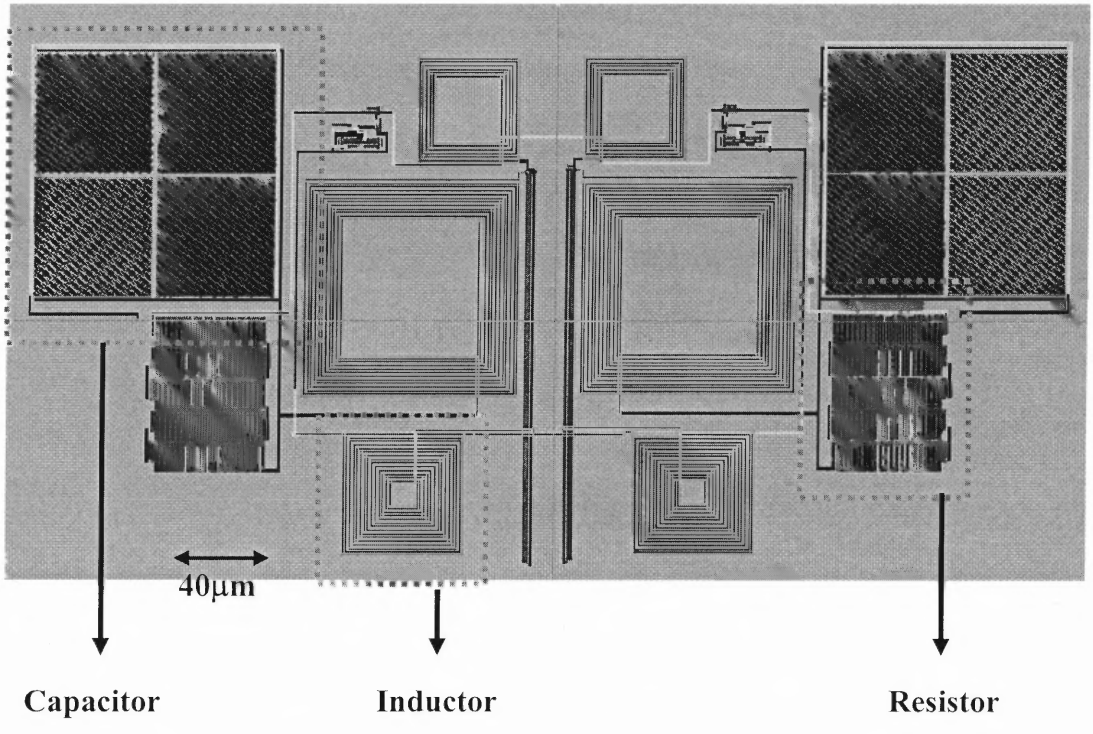

Figure 4.4 Low Noise amplifier layout.

To convert differential outputs to single ended outputs, balun circuit has been used. Its layout is shown in Figure 4.5.Total six transistors are used. The four resistors are drawn using second polysilicon.

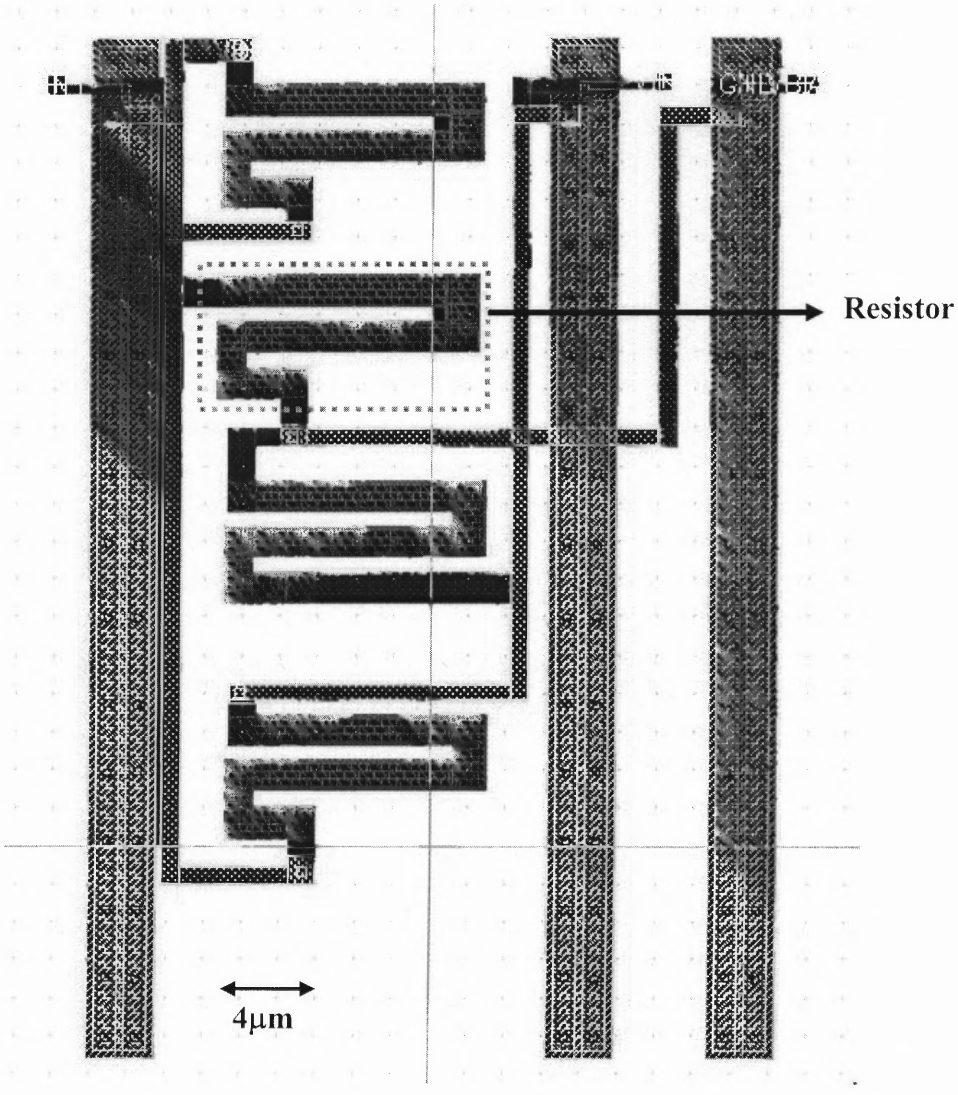

Figure 4.5 Balun circuit layout.

The layout of the whole transceiver is shown in Figure 4.6. The total core area is 4.7mm^2. The layout is extremely critical and carefully done to minimize the coupling among the building blocks.

In all blocks PA amplifier consumes more area. So it placed over top of the transceiver circuit. LNA is placed below left corner of PA.VCO layout is placed right side to PA. Mixers are put close to the outputs of VCO. Low pass filters are placed nearer to LNA. Similarly Phase shifter is placed to close to the mixer. The Input and Control signal to VCO are put at lower side of the chip. VDD and GND are put at upper side of the chip. Table 4.1 summarizes the chip area of each block and final transceiver.

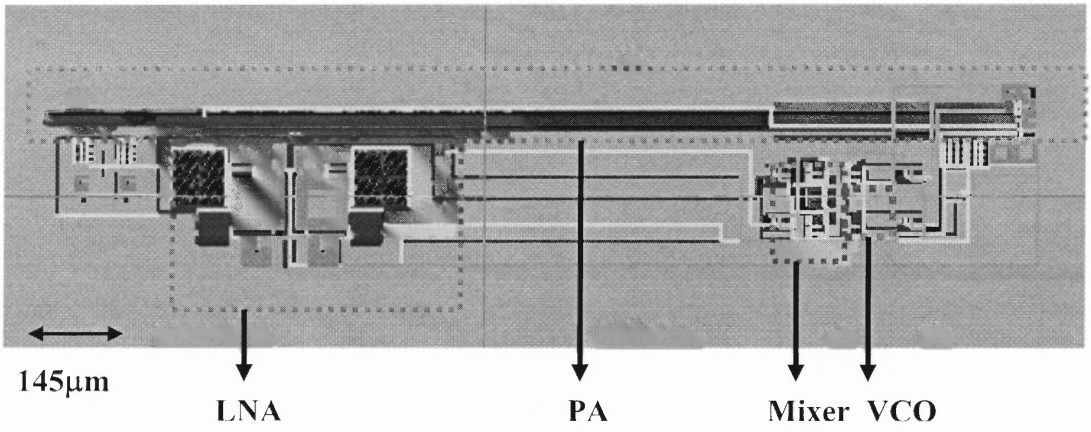

Figure 4.6 Transceiver layout.

Table 4.1 Chip Area of each component

Component	Area μm^2
VCO	58 X 87
PA	2020 X 181
Mixer	45 X 44
LNA	245 X 480
Balun	54 X 38
Total	2020 X 370

4.2 Experimental Results

4.2.1 Voltage Controlled Oscillator

The post layout transient response of Voltage Controlled Oscillator is shown in Figure 4.7 for dc input voltage. The shown 1GHZ output waveforms have phase

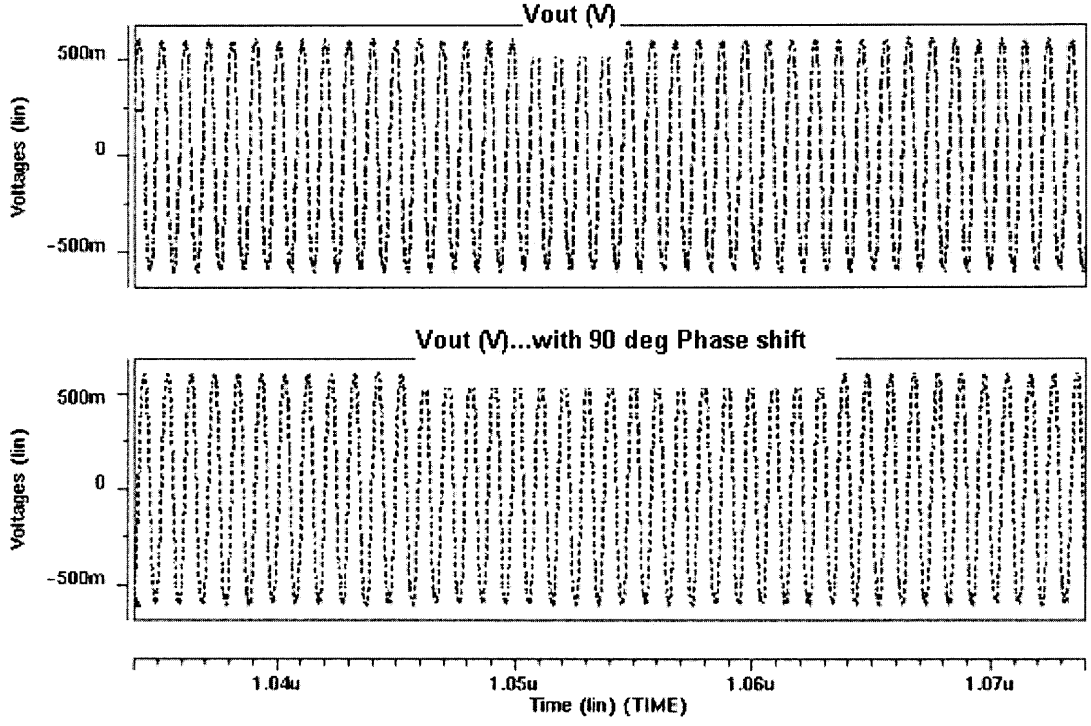

Figure 4.7 Post Layout quadrature outputs of VCO.

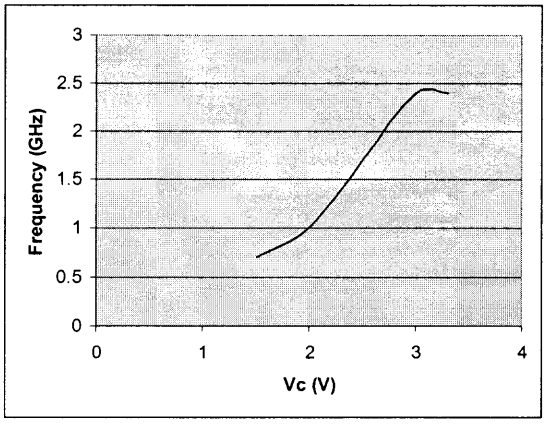

Figure 4.8 VCO characteristics.

difference of 90^0 each other. By changing dc input of VCO the frequency of these output curves changes. It can operate between 700MHz and 2.4 GHz frequencies as shown in Figure 4.8.

To investigate the noise behavior of the VCO Fast Fourier Analysis is done. The result output spectrum is shown in the Figure 4.9. The difference between fundamental (at 1GHz) and 3^{rd} order (at 3 GHz) components is 42dB at typical room temperature.

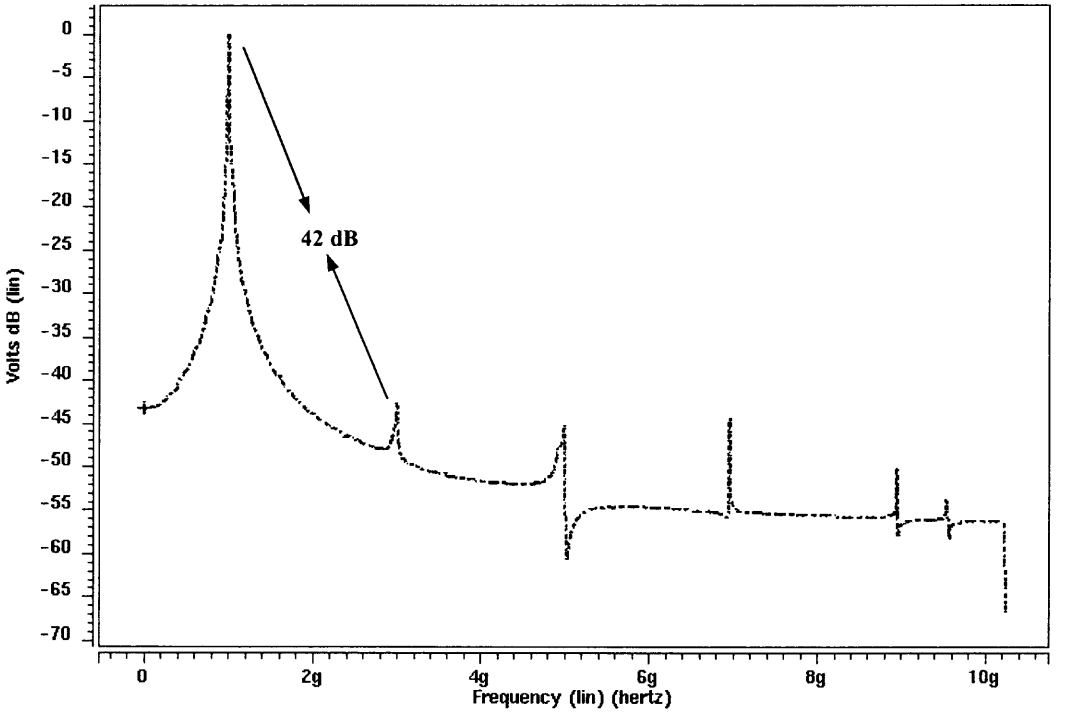

Figure 4.9 Output spectrum at room temperature.

The jitter analysis that corresponds to the drift in the center frequency was reviewed through the corresponding eye diagram, which is in below Figure 4.10. At room temperature, jitter in VCO is 28 psec. The VCO dissipates 8mW of power. The functional summary of VCO is outlined in Table 4.2.

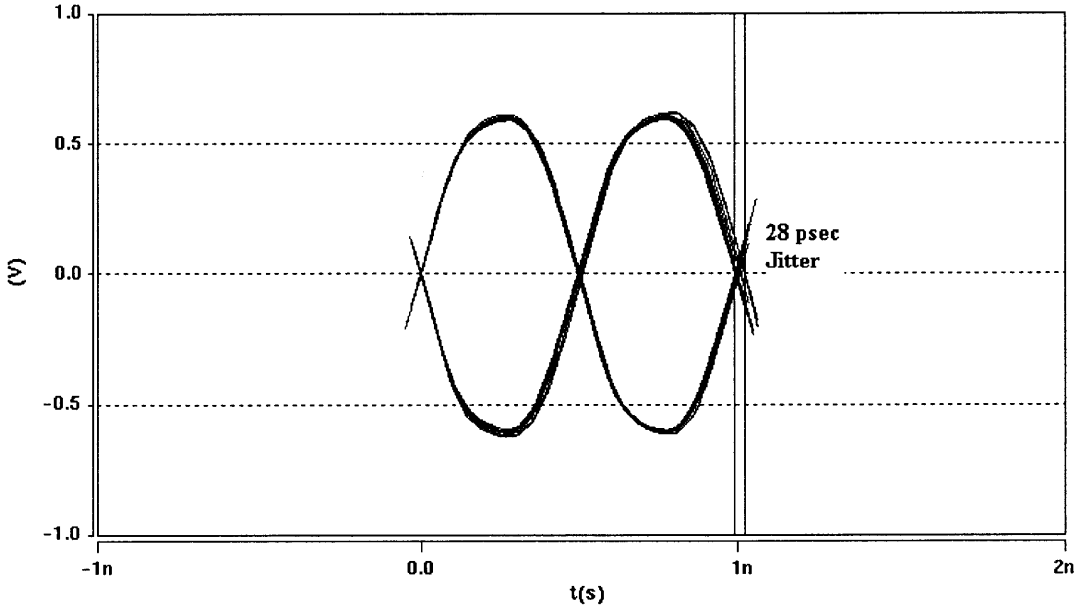

Figure 4.10 Corresponding eye diagram.

Table 4.2 VCO Results

Parameter	**Experimental Results**
Center Frequency	1GHz
Jitter	28Psec
Harmonic Separation	42dB
Power	8mW

4.2.2 Power Amplifier

Figure 4.11 shows a typical plot of the output power verses V_{DD}, measured at 2 GHz. the output power increases from 0.1 W to 2.1W monotonically as the supply voltage is swept from 0.5 V to 3.3 V and is approximately proportional to V_{DD}^2.

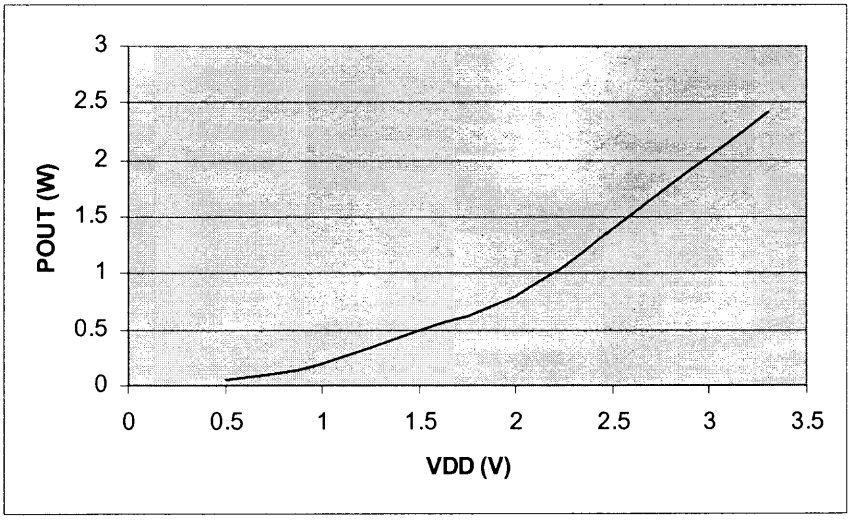

Figure 4.11 Output Power verses supply voltage.

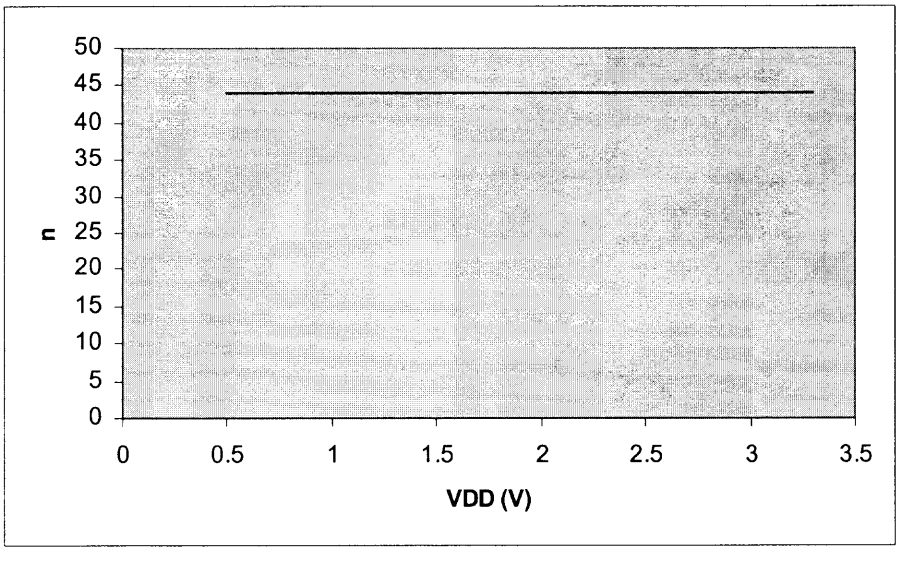

Figure 4.12 Efficiency verses supply voltage.

As expected from the switching nature of PA , the drain efficiency is constant over the supply voltage shown in Figure 4.12.Similarly Power Added Efficiency (PAE) is constant after some supply voltage is shown in Figure 4.13.

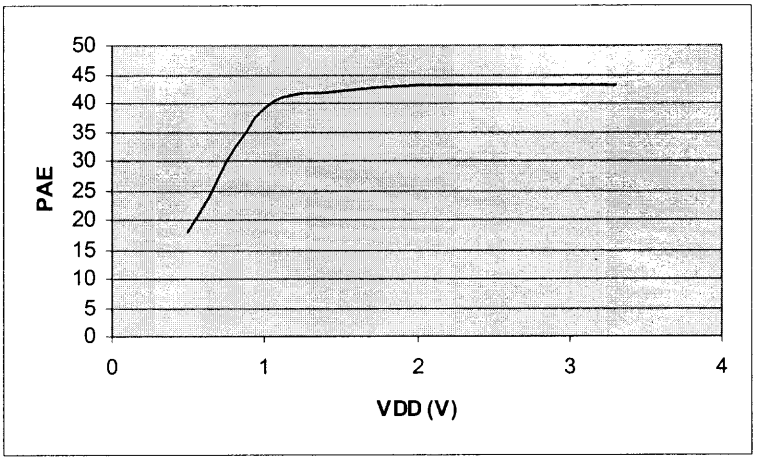

Figure 4.13 PAE verses supply voltage.

For sinusoidal and differential input of 2GHz , output waveforms are shown in Figure 4.14 .The output is also a 2 GHz, differential sinusoidal waveform. Table 4.3 shows the all obtained results of PA in tabular form.

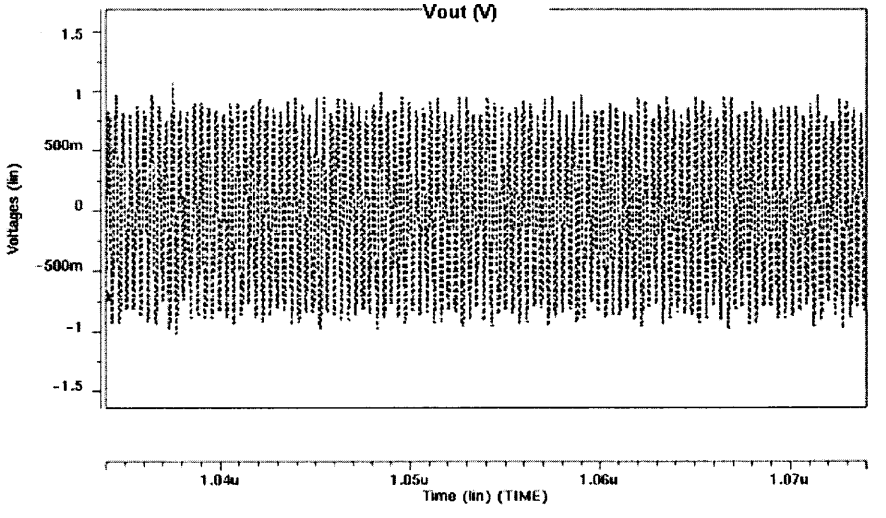

Figure 4.14 Post Layout transient response of PA.

Table 4.3 Power Amplifier Results

Parameter	**Experimental Results**
Center Frequency	2GHz
Efficiency	44%
Power Consumption	46mW

4.2.3 Mixer

The post layout transient response of the Gilbert's Cell is shown in Figure 4.15. The inputs to the Gilbert's cell are stimulated with a 1GHz signal with peak-to-peak amplitude of .2V. As shown in the Figure 4.15, the output is a 2 GHz, differential sinusoidal signal and with its minimum voltage at zero volts.

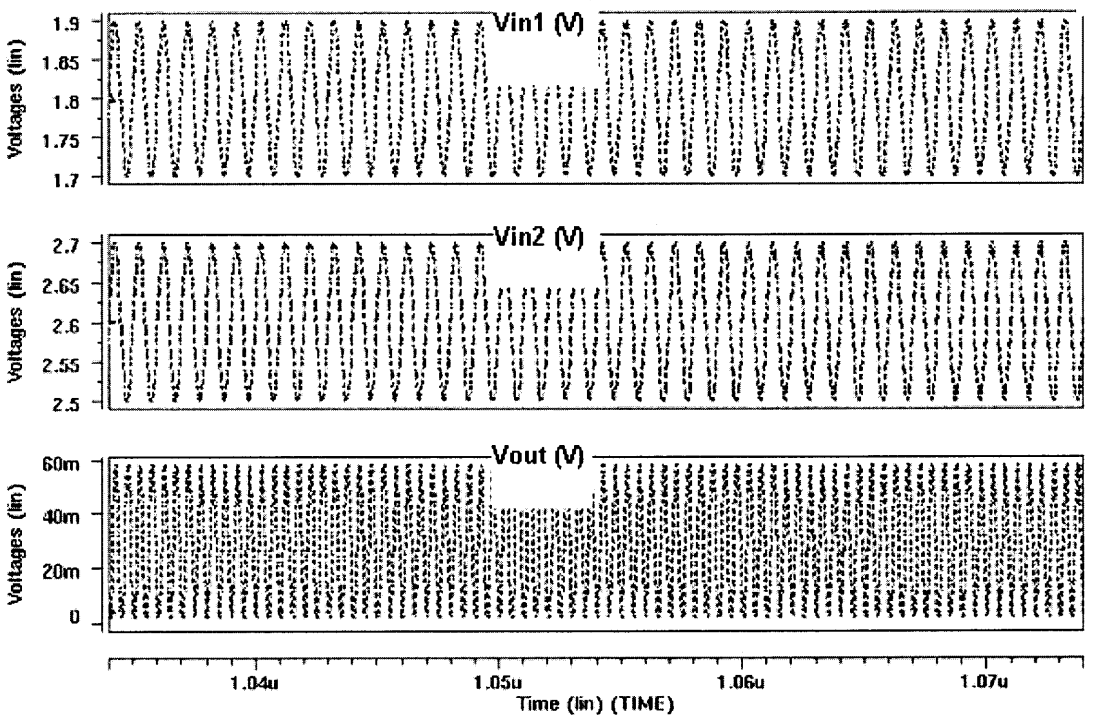

Figure 4.15 Post layout waveforms of mixer.

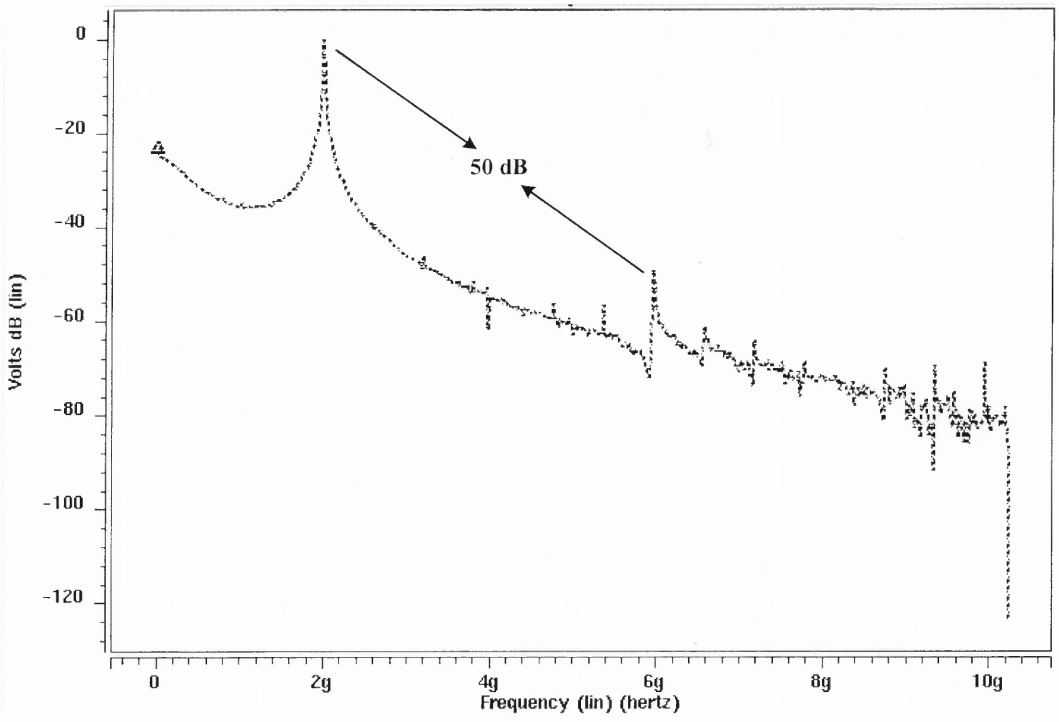

Figure 4.16 Mixer output spectrum.

The output spectrum of mixer to check noise behavior is shown in Figure 4.16.Fundamental and 3rd order components are separated by 52dB. The Noise Figure (The ratio of output noise to noise due to the input sources) is at 2GHz is low and it is

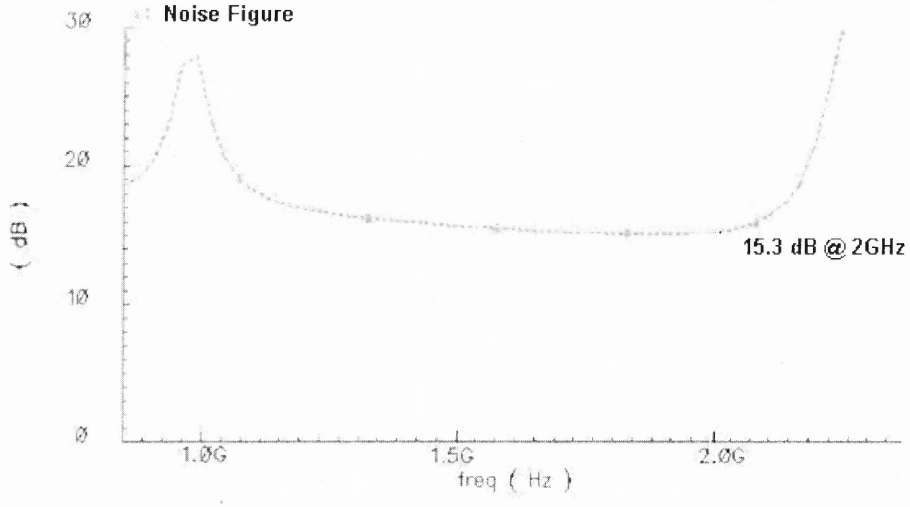

Figure 4.17 Noise figure of mixer.

15.3dB as shown in Figure 4.17.Similarly, mixer linearity is observed by measuring the input intercept point (IIP3) of 10.5dB and 1-dB compression point of 5.39dB as shown in Figure 4.18 and 4.19.All Mixer results are briefed in Table 4.4

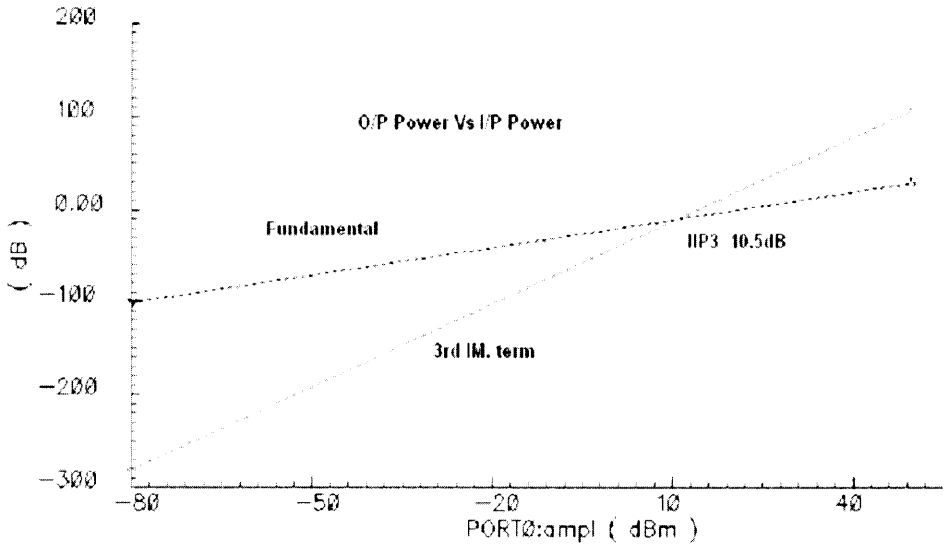

Figure 4.18 IIP3 of mixer.

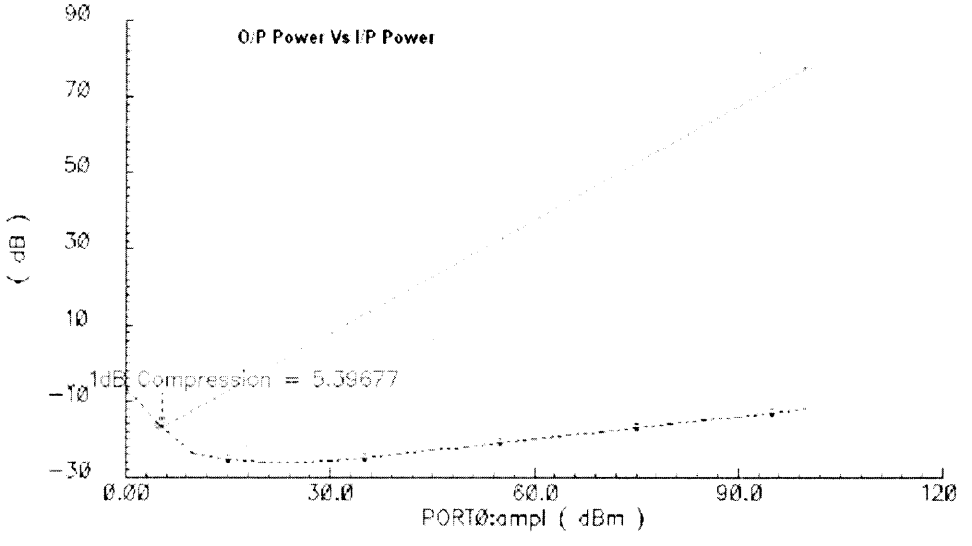

Figure 4.19 1-dB compression point.

Table 4.4 Mixer results

Parameter	**Experimental Results**
Noise Figure	15.3 dB
IIP3	10.5 dB
1-dB Compression Point	5.39dB
Power	6.4mW
Harmonic Separation	50 dB

4.2.4 Low Noise Amplifier

Post a layout transient response for LNA is shown in figure 4.20 for 2GHz differential input. The output is a differential waveform with 5V gain.

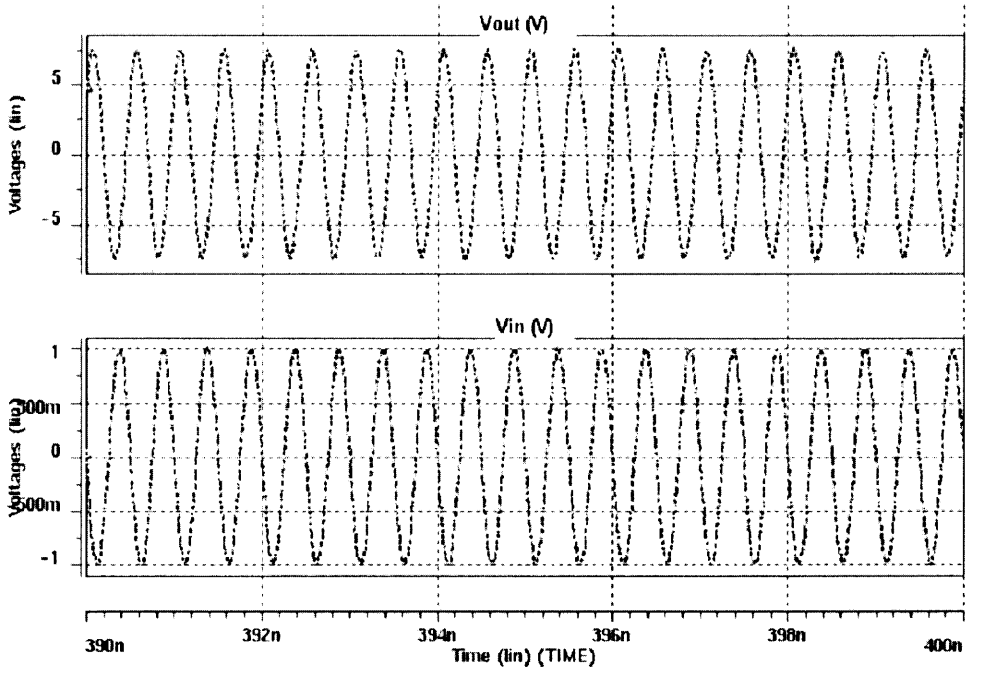

Figure 4.20 Post layout simulations of LNA.

The gain of LNA is measured to be 6 dB as shown in Figure 4.21. This value is depends on the output load. With the smaller capacitive load, the gain can be increased sufficiently. If add resistor to load at the output the gain drops. Figure 4.22 shows the noise results for LNA. At 2 GHz the value is 5.8dB. Final results of LNA are summarized in Table 4.5

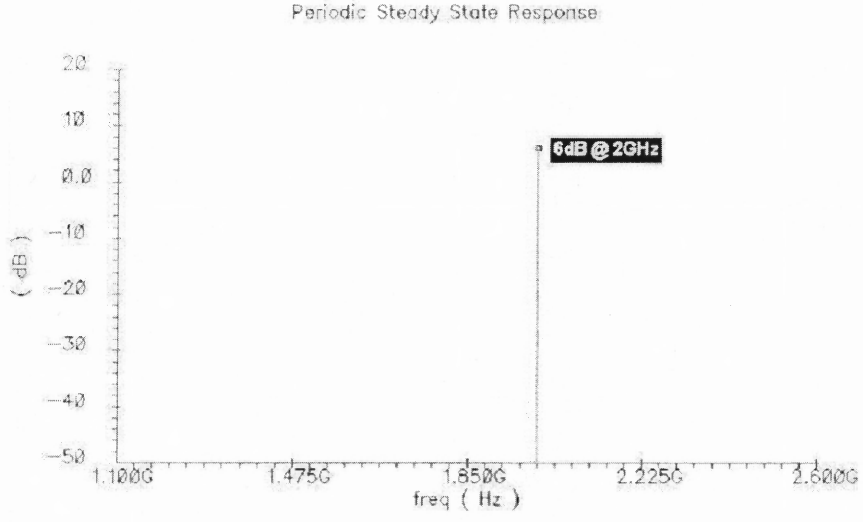

Figure 4.21 Gain of LNA.

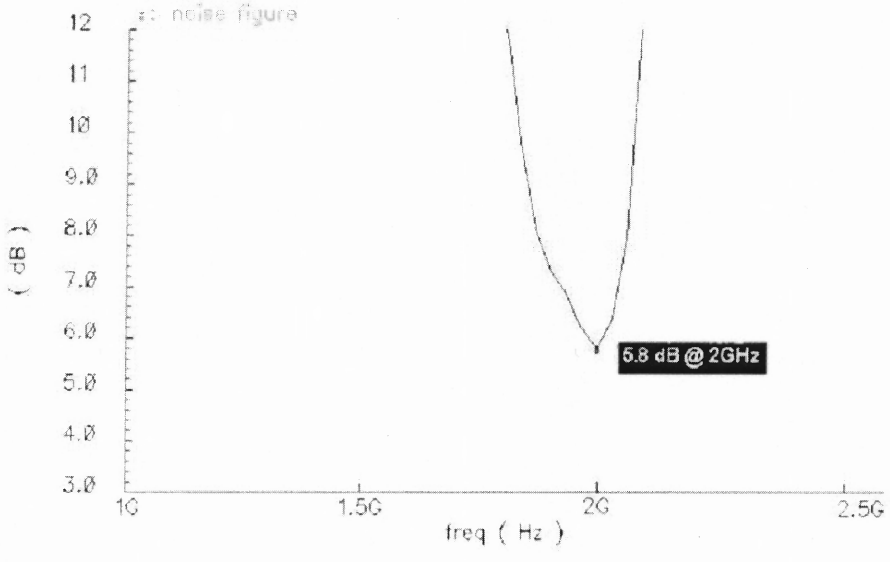

Figure 4.22 Noise figure of LNA.

Table 4.5 LNA Results

Parameter	**Experimental Results**
Center Frequency	2GHz
Noise Figure	5.8 dB
Gain	6 dB
Power	16.5mW

4.2.4 Transceiver Results

Final post layout transmitter output waveforms are shown in Figure 4.23 for sinusoidal 1GHz base band signals. The output is a 2GHz, differential signal is locked with fundamental component of VCO. Fundamental and 3rd order components are separated by 52dB is shown in the output spectrum of Figure 4.24.

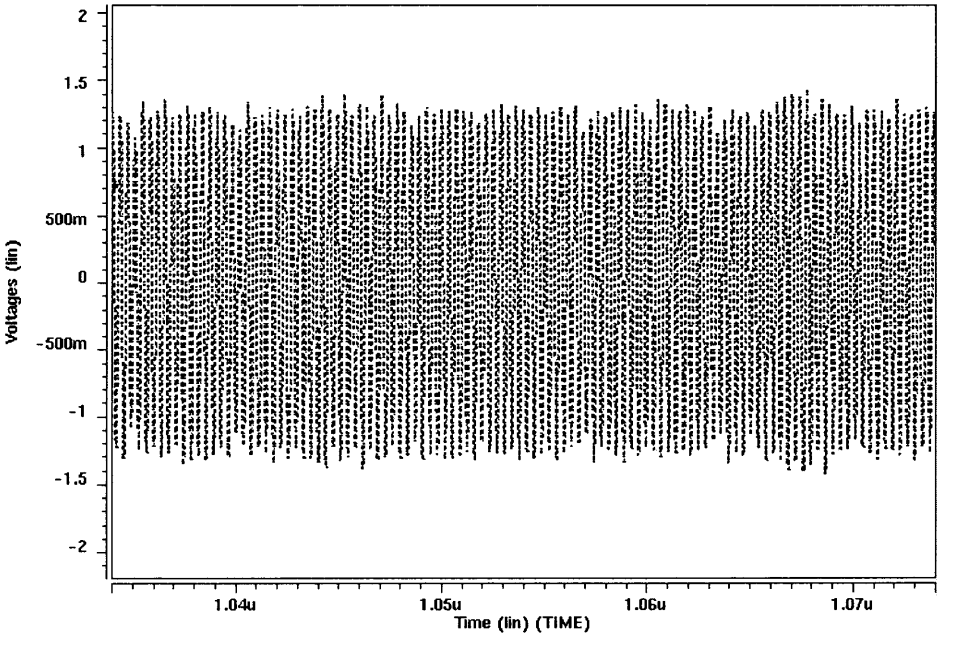

Figure 4.23 Post layout transient response of transmitter.

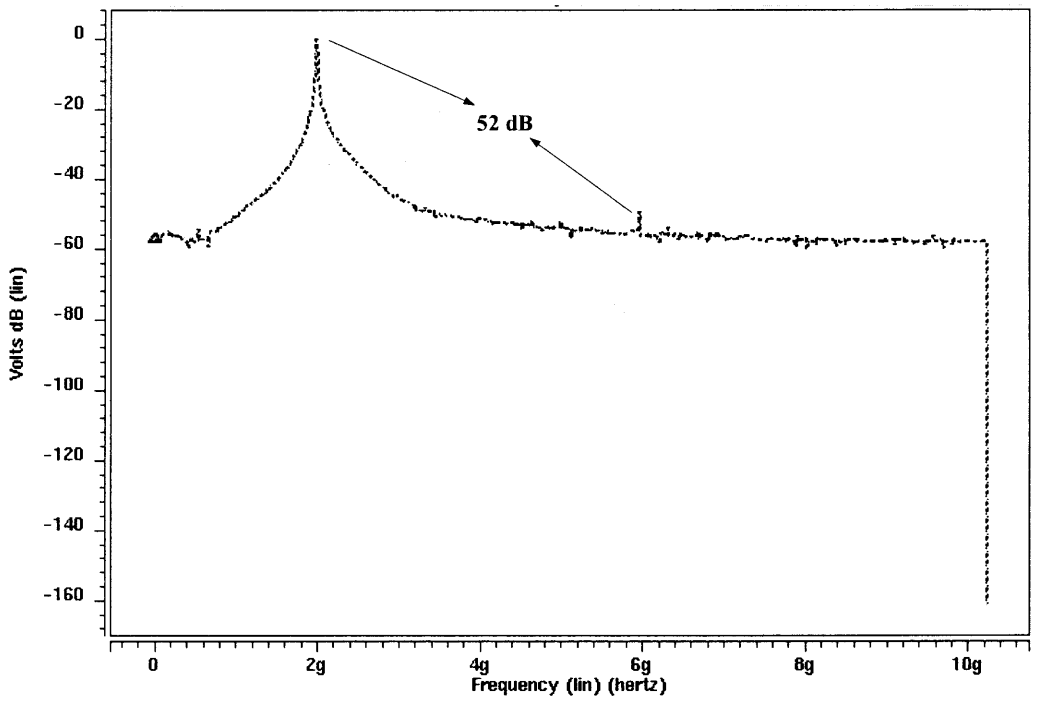

Figure 4.24 Output spectrum of transmitter.

Similarly for receiver Post layout transient response is shown in Figure 4.25.The whole overall receiver measures the 42dB difference between the desired and undesired components shown in Figure 4.26.

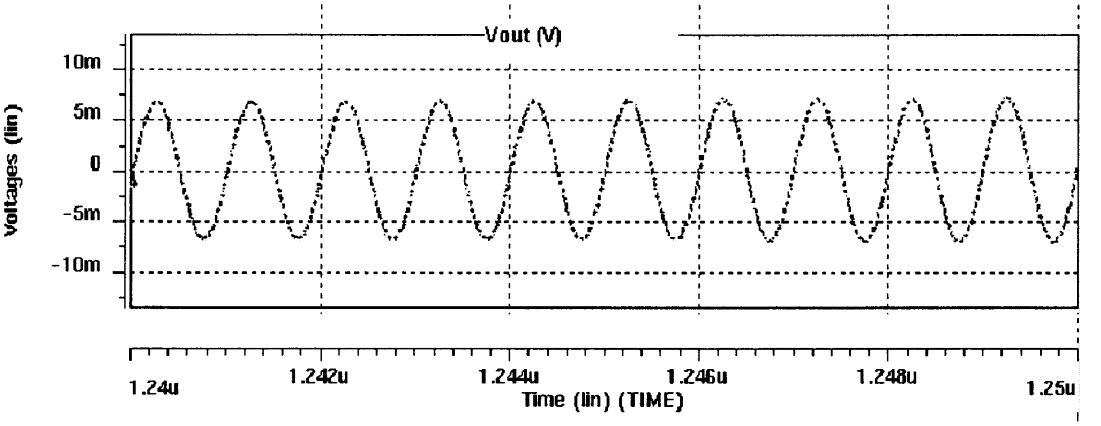

Figure 4.25 Post layout transient response of receiver.

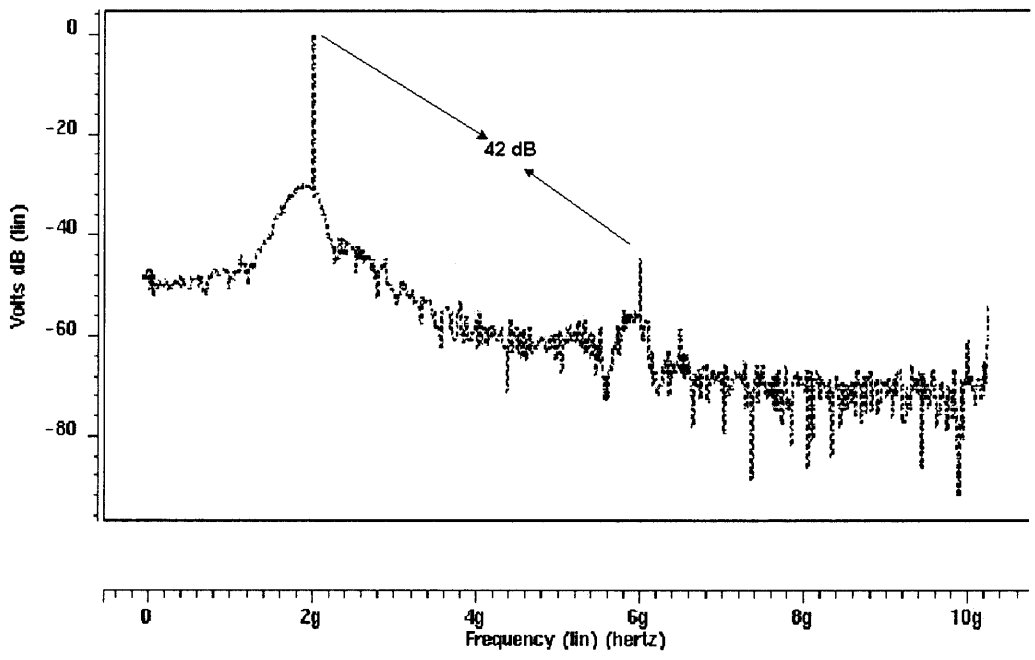

Figure 4.26 Output spectrum of receiver.

The simulation results of the transceiver are presented in this chapter. Designed in a standard TSMC 0.35μm CMOS process and without any off-chip component with 56 dB and 38 dB power consumption in transmit and receive mode.

CHAPTER 5

CONCLUSION AND FUTURE WORK

The proposed low power Transceiver designed in TSMC 0.35μm CMOS Technology, to transmit and receive the alert signals from Chemical and biological sensors implemented in Ad-hoc networks. This transceiver doesn't use any external components and still achieves a high noise rejection of 52 dB and 42 dB in transmitter and receiver respectively, and a small chip area of 4.65 mm^2. Because of the fully-differential topology and the high level of integration, power consumption is 56 mW and 38 mW in transmit and receive mode, is low. The Transceiver circuit can be used in wireless integrated network system architecture to build a robust sensor wireless network.

The Class E Power amplifier consumes 46 mW power out of total 56 mW power consumption in transmit mode. This is mainly because of bulky transistors. With more advanced technology in the future, the transistor size can be reduced. As a result, the power consumption can be limited.

APPENDIX A

MODEL LIBRARIES

The following model libraries used in Hspice simulations for TSMC 0.35μ technology are obtained from MOSIS.

T17C SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Aug 30/01

* LOT: T17C WAF: 9105

* Temperature_parameters=Default

.MODEL CMOSN **NMOS** (LEVEL = 49

+VERSION = 3.1 TNOM = 27 TOX = 7.9E-9

+XJ = 1E-7 NCH = 2.2E17 VTH0 = 0.5278

+K1 = 0.5643116 K2 = 0.0159544 K3 = 1E-3

+K3B = -6.5518637 W0 = 3.086035E-5 NLX = 1.449731E-7

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 3.683553 DVT1 = 0.7013954 DVT2 = -0.0874192

+U0 = 420.8098574 UA = -1.08294E-13 UB = 1.432196E-18

+UC = 2.880479E-11 VSAT = 1.720176E5 A0 = 1.1474866

+AGS = 0.1579867 B0 = 9.123275E-7 B1 = 5E-6

+KETA = 8.206723E-3 A1 = 0 A2 = 0.4130611

+RDSW = 678.3137662 PRWG = 0.0938188 PRWB = -0.1197785

+WR = 1 WINT = 6.937808E-8 LINT = 0

+XL = -2E-8 XW = 0 DWG = -1.424855E-9

+DWB = 6.560579E-9 VOFF = -0.0866003 NFACTOR = 1.1330513

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.7479226 ETAB = 0.0279069

+DSUB = 0.8150882 PCLM = 1.4340831 PDIBLC1 = 1.422419E-3

+PDIBLC2 = 4.95301E-3 PDIBLCB = 0.0708244 DROUT = 0.1051684

+PSCBE1 = 3.065424E8 PSCBE2 = 5.089459E-7 PVAG = 0

+DELTA = 0.01 RSH = 3.2 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 2.85E-10 CGSO = 2.85E-10 CGBO = 1E-12

+CJ = 1.044665E-3 PB = 0.7931568 MJ = 0.3234315

+CJSW = 2.974052E-10 PBSW = 0.6619191 MJSW = 0.1

+CJSWG = 1.82E-10 PBSWG = 0.6619191 MJSWG = 0.1

+CF = 0 PVTH0 = -0.0226202 PRDSW = -82.9299492

+PK2 = 2.121644E-3 WKETA = -7.492882E-3 LKETA = -0.0120587)

```
*
.MODEL CMOSP PMOS (                    LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 7.9E-9
+XJ     = 1E-7          NCH     = 8.52E16     VTH0    = -0.6396344
+K1     = 0.4500926     K2      = -0.0176532  K3      = 69.937281
+K3B    = -5            W0      = 5.905597E-6 NLX     = 2.412511E-7
+DVT0W  = 0             DVT1W   = 0           DVT2W   = 0
+DVT0   = 0.8215402     DVT1    = 0.3861919   DVT2    = -0.0538688
+U0     = 153.6980343   UA      = 1E-10       UB      = 1.838397E-18
+UC     = -2.19315E-11  VSAT    = 2E5         A0      = 0.8962302
+AGS    = 0.341277      B0      = 2.630117E-6 B1      = 5E-6
+KETA   = -5.843835E-3  A1      = 8.405968E-5 A2      = 0.3
+RDSW   = 3.151471E3    PRWG    = -0.1069483  PRWB    = 0.0311708
+WR     = 1             WINT    = 7.489645E-8 LINT    = 0
+XL     = -2E-8         XW      = 0           DWG     = -1.180966E-8
+DWB    = 9.724667E-9   VOFF    = -0.1125403  NFACTOR = 2
+CIT    = 0             CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB  = 0             ETA0    = 0.1045234   ETAB    = 0.0179808
+DSUB   = 0.7110116     PCLM    = 3.6021609   PDIBLC1 = 0.0113757
+PDIBLC2 = 3.570949E-3  PDIBLCB = 8.277369E-3 DROUT   = 0.0619081
+PSCBE1 = 8E10          PSCBE2  = 5.009841E-10 PVAG   = 2.4840484
+DELTA  = 0.01          RSH     = 2.5         MOBMOD  = 1
+PRT    = 0             UTE     = -1.5        KT1     = -0.11
```

```
+KT1L   = 0          KT2    = 0.022       UA1    = 4.31E-9
+UB1    = -7.61E-18  UC1    = -5.6E-11    AT     = 3.3E4
+WL     = 0          WLN    = 1           WW     = 0
+WWN    = 1          WWL    = 0           LL     = 0
+LLN    = 1          LW     = 0           LWN    = 1
+LWL    = 0          CAPMOD = 2           XPART  = 0.5
+CGDO   = 3.29E-10   CGSO   = 3.29E-10    CGBO   = 1E-12
+CJ     = 1.386917E-3 PB    = 0.99        MJ     = 0.5597842
+CJSW   = 4.008208E-10 PBSW  = 0.99        MJSW   = 0.3375785
+CJSWG  = 4.42E-11   PBSWG  = 0.99        MJSWG  = 0.3375785
+CF     = 0          PVTH0  = 5.38001E-3  PRDSW  = -70.0899484
+PK2    = 1.701039E-3 WKETA = -6.9905E-4  LKETA  = -4.949014E-3  )
*
```

APPENDIX B

COMPONENT NETLISTS OF TRANSCEIVER

The following component netlists of transceiver are used in Hspice simulations.

Low Noise Amplifier

R5 0 NET163 230.0

R4 0 NET165 230.0

R3 NET180 NET254 10E3

R2 NET177 NET211 10E3

R1 NET175 VIN2 50.0

R0 VIN1 NET173 50.0

C1 NET180 NET175 10E-12

C0 NET173 NET177 10E-12

L5 NET180 NET245 25E-9

L4 NET177 NET181 25E-9

L3 VDD VOUT2 4.6E-9

L2 VDD VOUT1 4.6E-9

L1 NET188 0 2.6E-9

L0 NET190 0 2.6E-9

C2 Vout1 0 1E-12

C3 Vout2 0 1E-12

M11 VDD NET195 NET195 NET195 CMOSN L=400E-9 W=6E-6

AD=+6.00000000E-12

+AS=+6.00000000E-12 PD=+1.40000000E-05 PS=+1.40000000E-05

NRD=+1.66666667E-01

+NRS=+1.66666667E-01 M=1.0

M12 NET195 NET197 NET163 NET163 CMOSN L=400E-9 W=6E-6

AD=+6.00000000E-12

+AS=+6.00000000E-12 PD=+1.40000000E-05 PS=+1.40000000E-05

NRD=+1.66666667E-01

+NRS=+1.66666667E-01 M=1.0

M10 NET197 NET197 0 0 CMOSN L=400E-9 W=6E-6 AD=+6.00000000E-12

+AS=+6.00000000E-12 PD=+1.40000000E-05 PS=+1.40000000E-05

NRD=+1.66666667E-01

+NRS=+1.66666667E-01 M=1.0

M9 VDD NET195 NET197 NET197 CMOSN L=400E-9 W=6E-6 AD=+6.00000000E-

12

+AS=+6.00000000E-12 PD=+1.40000000E-05 PS=+1.40000000E-05

NRD=+1.66666667E-01

+NRS=+1.66666667E-01 M=1.0

M15 NET254 NET254 0 0 CMOSN L=400E-9 W=5E-6 AD=+5.00000000E-12

+AS=+5.00000000E-12 PD=+1.20000000E-05 PS=+1.20000000E-05

NRD=+2.00000000E-01

+NRS=+2.00000000E-01 M=1.0

M14 NET211 NET211 0 0 CMOSN L=400E-9 W=5E-6 AD=+5.00000000E-12

+AS=+5.00000000E-12 PD=+1.20000000E-05 PS=+1.20000000E-05

NRD=+2.00000000E-01

+NRS=+2.00000000E-01 M=1.0

M7 NET229 NET231 NET165 NET165 CMOSN L=400E-9 W=6E-6

AD=+6.00000000E-12

+AS=+6.00000000E-12 PD=+1.40000000E-05 PS=+1.40000000E-05

NRD=+1.66666667E-01

+NRS=+1.66666667E-01 M=1.0

M8 VDD NET229 NET211 NET211 CMOSN L=400E-9 W=6E-6 AD=+8.00000000E-13

+AS=+8.00000000E-13 PD=+3.60000000E-06 PS=+3.60000000E-06

NRD=+1.25000000E+00

+NRS=+1.25000000E+00 M=1.0

M6 VDD NET229 NET229 NET229 CMOSN L=400E-9 W=6E-6 AD=+6.00000000E-12

+AS=+6.00000000E-12 PD=+1.40000000E-05 PS=+1.40000000E-05

NRD=+1.66666667E-01

+NRS=+1.66666667E-01 M=1.0

M4 VDD NET229 NET231 NET231 CMOSN L=400E-9 W=6E-6 AD=+6.00000000E-12

+AS=+6.00000000E-12 PD=+1.40000000E-05 PS=+1.40000000E-05

NRD=+1.66666667E-01

+NRS=+1.66666667E-01 M=1.0

M5 NET231 NET231 0 0 CMOSN L=400E-9 W=8E-6 AD=+6.00000000E-12

+AS=+6.00000000E-12 PD=+1.40000000E-05 PS=+1.40000000E-05

NRD=+1.66666667E-01

+NRS=+1.66666667E-01 M=1.0

M2 VOUT2 VDD NET243 NET243 CMOSN L=400E-9 W=180E-6

AD=+1.80000000E-10

+AS=+1.80000000E-10 PD=+3.62000000E-04 PS=+3.62000000E-04

NRD=+5.55555556E-03

+NRS=+5.55555556E-03 M=1.0

M0 VOUT1 VDD NET247 NET247 CMOSN L=400E-9 W=180E-6

AD=+1.80000000E-10

+AS=+1.80000000E-10 PD=+3.62000000E-04 PS=+3.62000000E-04

NRD=+5.55555556E-03

+NRS=+5.55555556E-03 M=1.0

M3 NET243 NET245 NET188 NET188 CMOSN L=400E-9 W=180E-6

AD=+1.80000000E-10

+AS=+1.80000000E-10 PD=+3.62000000E-04 PS=+3.62000000E-04

NRD=+5.55555556E-03

+NRS=+5.55555556E-03 M=1.0

M1 NET247 NET181 NET190 NET190 CMOSN L=400E-9 W=180E-6

AD=+1.80000000E-10

+AS=+1.80000000E-10 PD=+3.62000000E-04 PS=+3.62000000E-04

NRD=+5.55555556E-03

```
+NRS=+5.55555556E-03 M=1.0
M13 VDD NET195 NET254 NET254  CMOSN  L=400E-9 W=6E-6
AD=+6.00000000E-12
+AS=+6.00000000E-12 PD=+1.40000000E-05 PS=+1.40000000E-05
NRD=+1.66666667E-01
+NRS=+1.66666667E-01 M=1.0
vin1 vin1 0  sin(0 1 2e9 0 0 0)
vin2 vin2 0  sin(0 1 2e9 0 0 180)
VDD VDD 0  3.3
.Include CMOSN
.Include CMOSP
.OPTION NODE LIST POST
.Tran 10p 2500n
.OP
.Print V(Vout1,Vout2)
*.fft V(Vout1,Vout2)
.END
```

Gilbert Cell Mixer

```
r1 c 1 1600
r2 c 2 1600
m1 1 cont1 3 0 cmosn w=6u l=.35u pd = 8.7u ps = 12.7u as=6.3p ad=6.3p
m2 2 cont1 4 0 cmosn w=6u l=.35u pd = 12.7u ps =12.7u as=6.3p ad=6.3p
m3 1 cont2 4 0 cmosn w=6u l=.35u pd = 12.7u ps =12.7u as=6.3p ad=6.3p
```

```
m4 2 cont2 3 0 cmosn w=6u l=.35u pd = 12.7u ps =12.7u as=6.3p ad=6.3p

m5 3 in1 5 0 cmosn w=12u l=.35u pd = 24.7u ps =24.7u as=12.6p ad=12.6p

m6 4 in2 5 0 cmosn w=12u l=.35u pd = 24.7u ps =24.7u as=12.6p ad=12.6p

m7 5 6  0 0 cmosn w=80u l=.35u pd = 160.7u ps =160.7u as=84p ad=84p

m8 6 6 0 0 cmosn w=80u l=.35u pd = 160.7u ps =160.7u as=84p ad=84p

r3 c 6 2520

vcc c 0  3.3

vcont1 cont1 0 sin(2.6 0.1 0.8eg 0 0 0)

vcont2 cont2 0 sin(2.6 0.1 0.8eg 0 0 180)

vin1 in1 0  sin(1.8 0.1 1.6eg 0 0 0)

vin2 in2 0  sin(1.8 0.1 1.6eg 0 0 180)

.tran 10p 10n

.options node list post

.op

.print  v(2,1) vdb(2,1)

.include cmosn

.include cmosp

.end
```

Voltage Controlled Oscillator

```
M8 NET3 VC VDD VDD CMOSN  L=400E-9 W=100E-6

M13 NET060 NET039 NET3 vdd  CMOSP  L=400E-9 W=10E-6

M12 NET044 NET039 NET3 vdd  CMOSP  L=400E-9 W=10E-6

M17 NET047 NET048 NET3 vdd  CMOSP  L=400E-9 W=10E-6
```

```
M16 NET054 NET048 NET3 vdd  CMOSP  L=400E-9 W=10E-6

M11 NET3 NET044 NET25 0  CMOSN  L=400E-9 W=10E-6

M14 NET3 NET054 NET37 0  CMOSN  L=400E-9 W=10E-6

M15 NET3 NET047 NET21 0  CMOSN  L=400E-9 W=10E-6

M10 NET3 NET060 NET39 0  CMOSN  L=400E-9 W=10E-6

M7 NET21 NET39 0 0  CMOSN  L=400E-9 W=30E-6

M6 NET21 NET37 0 0  CMOSN  L=400E-9 W=30E-6

M5 NET37 NET21 0 0  CMOSN  L=400E-9 W=30E-6

M4 NET37 NET25 0 0  CMOSN  L=400E-9 W=30E-6

M3 NET25 NET21 0 0  CMOSN  L=400E-9 W=30E-6

M2 NET25 NET39 0 0  CMOSN  L=400E-9 W=30E-6

M1 NET39 NET25 0 0  CMOSN  L=400E-9 W=30E-6

M0 NET39 NET37 0 0  CMOSN  L=400E-9 W=30E-6

VDD VDD 0 3.3

Vc Vc 0  2.5

.Include CMOSN

.Include CMOSP

.OPTION NODE LIST POST

.Tran 10p 20n

*.fft v(net25,net39)

.Print v(net25,net39) v(net21,net37)

.ic v(net25) =0.95 v(net039) =0.1 v(net048)=0.1

.OP
```

.END

Power Amplifier

R1 NET9 0 50.0

R0 NET7 0 50.0

C0 NET9 0 5.1E-12

C1 NET7 0 5.1E-12

M9 0 VSW NET38 NET38 CMOSP L=400E-9 W=500E-6

M8 NET38 VSW VDD VDD CMOSN L=400E-9 W=31.58E-3

M7 NET25 NET34 NET38 NET38 CMOSN L=400E-9 W=3.6E-3

M6 NET25 NET24 NET38 NET38 CMOSN L=400E-9 W=4.8E-3

M4 NET24 NET39 NET38 NET38 CMOSN L=400E-9 W=3.6E-3

M5 NET24 NET25 NET38 NET38 CMOSN L=400E-9 W=4.8E-3

M3 NET34 VIN2 NET38 NET38 CMOSN L=400E-9 W=980E-6

M2 NET34 NET39 NET38 NET38 CMOSN L=400E-9 W=980E-6

M1 NET39 NET34 NET38 NET38 CMOSN L=400E-9 W=980E-6

M0 NET39 VIN1 NET38 NET38 CMOSN L=400E-9 W=980E-6

L5 NET25 NET9 0.8E-9

L4 NET24 NET7 0.8E-9

L3 VDD NET25 370E-12

L2 VDD NET24 370E-12

L1 VDD NET34 370E-12

L0 VDD NET39 370E-12

```
VDD VDD 0  3.3

Vin1 Vin1 0 sin(0 0.2 2e9 0 0 0)

Vin2 Vin2 0 sin(0 0.2 2e9 0 0 180)

Vsw Vsw 0 0.5

.include cmosp

.include cmosn

.tran 10p 10n

.Print v(net9,net7)

.option node list post

.TEMP    25.0000

.OP

.END
```

REFERENCES

1. J. C. Rudell, et al., "A 1.9-GHz wide-band IF double conversion CMOS receiver for Cordless Telephone Applications", *IEEE Journal of Solid-State Circuits*, Dec. 1997, pp. 2071-2088.

2. A. Abidi, et al., "The future of wireless transceiver", *Digest of Tech. Papers, ISSCC'97,* pp. 118-119.

3. M. S. J. Steyaert, J. Janssens, B. Muer de, M. Borremans, N. Itoh, "A 2-V CMOS cellular transceiver front-end", *IEEE Journal of Solid-State Circuits,* Dec. 2000, pp. 1895 – 1907.

4. Darabi H., Khorram S., Hung-Ming Chien, Meng-An Pan, Wu. S., Moloudi S., Leete J.C., Rael J.J., Syed M., Lee R.; Ibrahim B., Rofougaran M., Rofougaran A., "A2.4-GHz CMOS transceiver for bluetooth" *IEEE Journal of Solid-State Circuits,* vol. 36, Dec. 2001, pp. 2016 –2024.

5. Jerng A., Truong A., Wolday D., Unruh E., Landi E., Wong L., Fried R., Gibbons S., "Integrated CMOS transceivers using single-conversion standard IF or low IF RX for digital narrow band cordless systems", *Radio Frequency Integrated Circuits (RFIC) Symposium,* 2002, pp. 111 –114.

6. Everitt J., Parker J.F., Hurst P., Nack D., Rao Konda K., "A CMOS transceiver for 10-Mb/s and 100-Mb/s ethernet", *IEEE Journal of Solid-State Circuits*, vol. 33, Dec. 1998, pp. 2169 –2177.

7. Cheng TaChan, JenShang Hwang, Chen,"2.5Gb/s low-power CMOS optoelectronic transceiver for opticalcommunications", *Circuits and Systems, MWSCAS 2001, Proceedings of the 44th IEEE 2001 Midwest Symposium,* vol. 1, 2001, pp. 381 – 384.

8. Su D., Zargari M., Yue P., Rabii S., Weber D., Kaczynski B., Mehta S., Singh K., Mendis S., Wooley B., "A 5 GHz CMOS transceiver for IEEE 802.11a wireless LAN" *Solid-State Circuits Conference, Digest of Technical Papers, ISSCC, 2002 IEEE International,* vol. 1, 2002, pp 92 –449.

9. Piazza F., Orsatti P., Qiuting Huang, "A 0.25 μm CMOS transceiver front-end for GSM", *Custom Integrated Circuits Conference, Proceedings of the IEEE 1998,* May 1998, pp. 413 –416.

10. Chunbing G., "A Monolithic 900-MHz CMOS wireless transceiver", *Department of Electrical and Electronic Engineering,,* Southeast University, China, Aug. 2001.

11. Thomas H. Lee, "The design of CMOS radio-frequency integrated circuits", *Cambridge, 1998.*

12. B. Razavi, "Design of analog integrated circuits", *McGraw Hill, Boston, 2000.*

13. K. Martin, J. David, "Analog integrated circuit design", *John Wiley & Sons, New York,1997.*

14. B. Razavi, "RF microelectronics", *Prentice-Hall, 1998.*

15. B. Razavi, "RF transmitter architectures and circuits", *Custom Integrated Circuits, 1999.Proceedings of the IEEE 1999*, pp.197-204.

16. B. Razavi, "Architectures and circuits for RF CMOS receivers", *Custom Integrated Circuits, Proceeding of the IEEE 1998*, May *1998,* pp.393-400.

18. Hamid R. Rategh, Thomas H. Lee, "Superharmonic injection-locked frequency dividers", *IEEE Journal of Solid-State Circuits,* Vol.34, June 1999, pp. 813 –821.