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ABSTRACT

CHARACTERIZATION AND MAPPING OF CRYSTAL DEFECTS IN SILICON CARBIDE

by

Ejiro Emorhokpor

Silicon carbide (SiC) is a semiconductor with attractive properties, such as a wide bandgap (3. 26 eV), high dielectric strength, and high thermal conductivity that make it suitable for high power, high-speed electronic devices. A major roadblock to its wider application is the presence of defects, particularly micropipes and dislocations, in SiC wafers produced today and decreasing density of these defects is the most important challenge of the industry. The goal of this thesis was to design, build and test a system for detection and analysis of the defects in SiC wafers. The system is based on the reflection optical microscopy of the surface of wafers etched with Potassium Hydroxide (KOH). Etching in molten KOH at 450°C enhances the defects and allows distinguishing micropipes and dislocation in dark field or bright field microscopic images, depending on the semiconductor doping level. Computer image analysis of the microscopic images, which included threshold filtering, dilation, and erosion, resulted in creation of wafer maps of micropipes and dislocation defects. The process was automated and the duration for scanning wafers, 5 cm in diameter, and generating defect maps is typically four hours.

The ability to generate defect maps of SiC wafers will help to reveal the conditions under which micropipes are formed, and may ultimately lead to developing methods of their reduction. Since there is a well established theory that screw dislocations play a role in the generation of micropipes, the correlation between micropipes and dislocations maps will further help to confirm this hypothesis.

CHARACTERIZATION AND MAPPING OF CRYSTAL DEFECTS IN SILICON CARBIDE

by
Ejiro Emorhokpor

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Department of Electrical and Computer Engineering

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APPROVAL PAGE

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To my beloved family and friends, especially my parents.

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The system was setup at *II-IV Inc.*, a company that grows SiC crystals and fabricates wafers, where it helps in monitoring of the wafer quality and in controlling the processes of SiC crystal growth.

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CHAPTER 1

INTRODUCTION

Silicon carbide (SiC) use is becoming widespread due to its superior properties as a semiconductor material, i.e. high breakdown electric field, wide bandgap, high thermal conductivity and saturation drift velocity, which are necessary for developing high temperature and high frequency electronics.

Silicon carbide substrate is commonly used for the fabrication of epitaxial devices based on SiC and group III-nitrides. Its applications include light emitting diodes (LEDs), power switching devices, opto-electronic devices, high temperature devices, microwave transistors, laser diodes, metal-semiconductor field effect transistors (MESFETS), vertical metal-oxide-semiconductor (MOS) devices, etc.

The reason for SiC's slow acceptance is the relatively high defect density in the currently manufactured material. The defects most common in SiC are dislocations and micropipes. Dislocations exist in three forms: screw dislocations that propagate perpendicular to the <0001> plane, basal plane dislocations and threading edge dislocations. Micropipes are screw dislocation with Burger's vector of at least $2b_o$ in 6H-SiC and $3b_o$ in 4H-SiC where b_o is the Burger's vector of a unit screw dislocation that has a direction parallel to the c-axis (b_o = 15.19A). These defects exist in the popular polytypes of SiC (6H, 4H and 3C), and their reduction in SiC substrate is the topic of current extensive research and development.

Several techniques used to reveal defects in SiC include potassium hydroxide (KOH) etching, and optical microscopy, synchrotron white beam X-ray topography

(SWBXT), scanning electron microscopy (SEM), and atomic force microscopy (AFM). Some of these techniques have been studied as development tools for monitoring the density and distribution of defects in SiC.

To date, there is no industry standard on a system for mapping defects in SiC crystal. The SWBXT system is possibly the most precise technique of presenting defect density images based on an X-ray diffraction technique. But it is an expensive approach that may not be economical for consistently keeping track of defects in production wafers.

Since KOH etching of SiC is easy and cost effective, it is a widely used technique for revealing defects in SiC. Optical microscopy was used in conjunction with KOH etching to monitor the density and distribution of defects, from which defect maps of SiC samples were generated. This technique utilizes image analysis software that can discriminate between the various types of defect images. This process can be utilized for any semiconductor material that has visible defects on a scale down to 1μm (the resolution limit of optical microscopes).

This thesis reports a study on monitoring the distribution and density of SiC defects utilizing KOH etch technique and optical microscopy, and compares the effectiveness of other techniques currently utilized, such as SWBXT and optical transmission microscopy. Also reported is the study of SiC etch rate with molten KOH at 450°C and KOH vapor etching and their effects on the SiC crystalline material.

CHAPTER 2

SILICON CARBIDE

2.1 Brief History

Silicon carbide (SiC) first appeared in science in 1824 when Jöns Jacob Berzelius accidentally synthesized the compound in an effort to create diamond [1]. Then in 1891, Edward Goodrich Acheson began to mass-produce SiC for the abrasive industry. He thought the crystals he produced were a combination of carbon and aluminum and he patented the trademark named Carborundrum, after aluminum oxide, which had been named Corundum [2]. Although SiC had been formed through experimentation, it was not until 1893 that Henri Moissan discovered SiC in nature. He discovered small amounts of SiC in a meteorite in Arizona, USA [2]. The Mineralogy community named the natural crystal Moissanite in honor of the founder. The flourishing jewelry industry adopted this name for synthesized diamond material made from semi-insulating SiC [3].

In 1955, J. Lely developed the first sublimation process for growing SiC crystals, which were of better quality than those from Acheson's process. In 1978, Tairov and Tsvetkov developed the physical vapor transport (PVT) growth of SiC through sublimation. This were the first crystals grown that would be applicable to the semiconductor industry both in size and quantity. Then in 1987, the first seeded growth was developed and has since been a mainstay in the industry.

2.2 Crystal Structures

Silicon carbide has different crystal structures with the same chemical composition. This phenomenon is known as polymorphism. Polytypism, a special case of polymorphism, is a phenomenon whereby a compound occurs in different one-dimensional structural modifications. SiC has more than 200 polytypes each of which consist of stacking layers of identical structure and composition, with modifications observed only in their stacking sequences. The most common polytypes are 3C, 4H and 6H. Each polytype is named according to the Si-C units stacking sequence, which is known as Ramsdell notation. To name a polytype, first count the number of layers in one stacking direction, followed by the first letter of the crystal stacking structure: C – cubic, H – hexagonal, R – Rhombohedral. Hence, 3C-SiC has three Si-C layers stacked in a cubic structure before it repeats itself, and 6H-SiC has six Si-C layers stacked in a hexagonal structure before the pattern is repeated. Figure 2.1 shows schematic representations of the stacking sequences in common SiC polytypes. Table 2.1 indicates the known SiC polytypes.

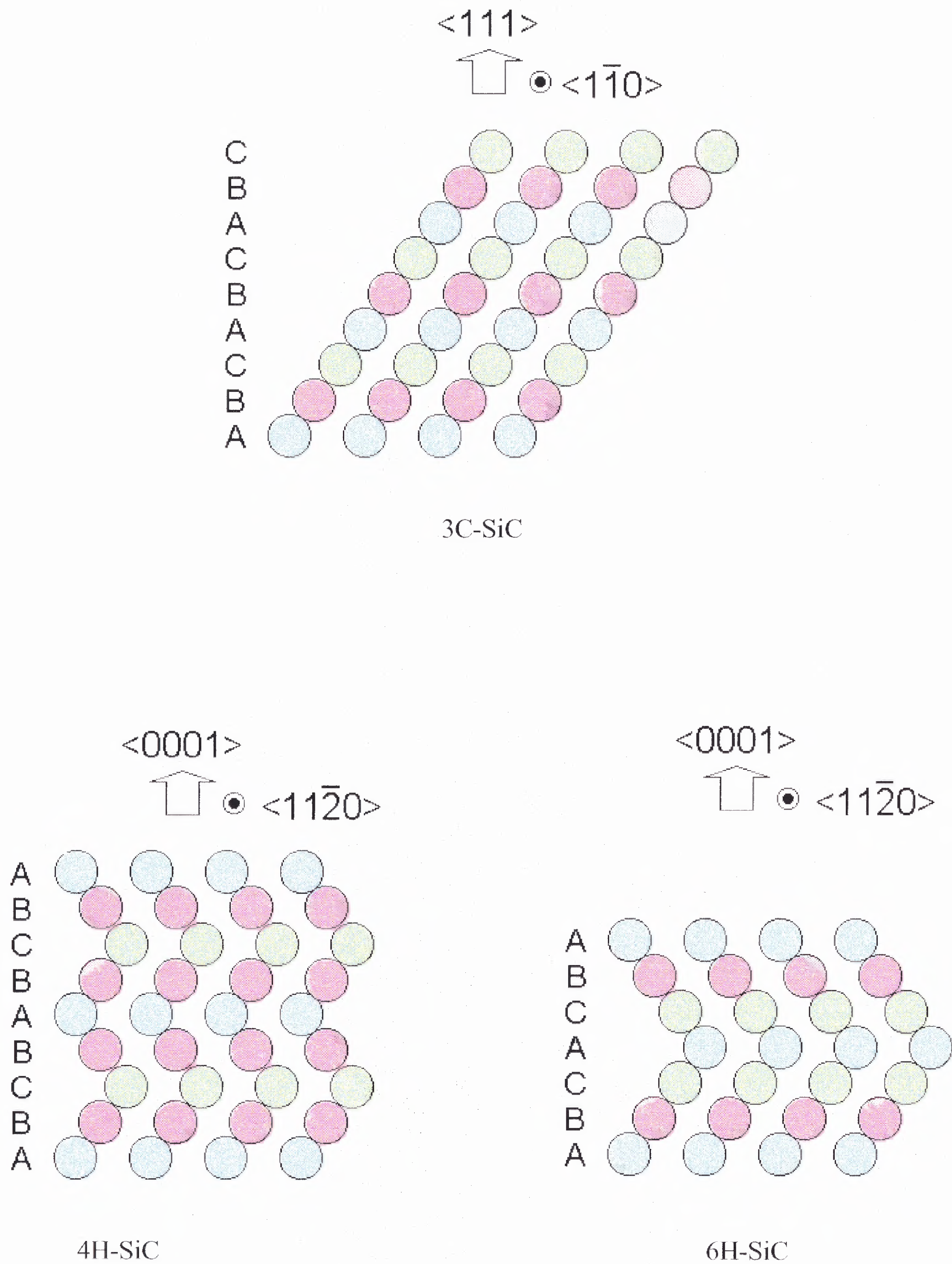

Figure 2.1 3-C, 4-H and 6-H Silicon carbide stacking sequence schematic.

Table 2.1 List of SiC Polytypes with Known Structures

Polytype	Structure (Zhdanov sequence)	Polytype	Structure (Zhdanov sequence)
2*H*	11	54*H*	$(33)_6323334$
3*C*	∞	57*H*	$(23)_93333$
4*H*	22	57*R*	$(33)_234$
6*H*	33	69*R* 1	$(33)_332$
8*H*	44	69*R* 2	33322334
10*H*	3322	75*R* 1	$(33)_334$
14*H*	$(22)_233$	75*R* 2	$(32)_3(23)_2$
15*R*	23	81*H*	$(33)_535(33)_634$
16*H* 1	$(33)_222$	84*R*	$(33)_3(32)_2$
16*H* 2	332332	87*R*	$(33)_432$
18*H*	$(22)_333$	90*R*	$(23)_43322$
19*H*	$(23)_322$	96*R*	$(33)_33434$
20*H*	$(22)_344$	99*R*	$(33)_43222$
21*H*	333534	105*R*	$(33)_532$
21*R*	34	111*R*	$(33)_534$
24*R*	35	120*R*	$(22)_523222333$
27*H*	$(33)_2(23)_3$	123*R*	$(33)_632$
27*R*	2223	141*R*	$(33)_732$
33*R*	3332	147*R*	$(3332)_432$
33*H* 1	$(33)_2353334$	159*R*	$(33)_832$
33*H* 2	$(33)_3(23)_3$	168*R*	$(23)_{10}33$
36*H* 1	$(33)_232(33)_234$	174*R*	$(33)_66(33)_54$
36*H* 2	$(33)_43234$	189*R*	$(34)_843$
39*H*	$(33)_232(33)_3(32)_2$	222*R*	$(33)_634(33)_434$
39*R*	3334	267*R*	$(23)_{17}22$
45*R*	232332	273*R*	$(23)_{17}33$
51*R* 1	$(33)_232$	303*R*	$(33)_{16}32$
51*R* 2	$(22)_323$	393*R*	$(33)_{21}32$

Source of data: International Union of Crystallography

2.3 Physical Properties of Silicon Carbide

The physical properties of silicon carbide make it a special material for manufacturing semiconductor devices that will function beyond the physical capabilities of most other semiconductor materials. Table 2.2 shows important physical properties of SiC, Gallium Ascenide (GaAs) and Silicon (Si) semiconductor materials.

Out of the many polytypes of SiC outlined in Table 2.1, 3C-, 4H- and 6H-SiC are the most interesting today for the manufacturing of devices.

Table 2.2 Semiconductor Physical Properties

Property	4H-SiC	6H-SiC	GaAs	Si
Band Gap Eg (ev)	Indirect 3.26 [(a)]	Indirect 3.03 [(a)]	Direct 1.43 [(b)]	Indirect 1.12 [(b)]
Thermal Conductivity (W/cm K @ 298K)	3.0 – 3.8 [(a)]	3.0 - 3.8 [(b)]	0.5 [(b)]	1.5[(b)]
Saturated Electron Drift Velocity (cm/sec @ E > 2 x 10^5 V/cm)	$2.0E^7$ [(b)]	$2.0E^7$ [(b)]	$1.0E^7$ [(b)]	$1.0E^7$ [(b)]
Breakdown Electric Field (V/cm, 100 V operation)	$2.2E^6$ [(b)]	$2.4E^6$ [(b)]	$3.0E^5$ [(b)]	$2.5E^5$ [(b)]
Electron Mobility (cm^2/V-s @ 298K, doping~ 10^{16} cm^{-3})	800	370	6000	1100
Hole Mobiliy (cm^2/V-s @ 298K, doping~ 10^{16} cm^{-3})	115	90	320	420
Dielectric Constant, ε	9.7	9.7	12.8	11.8

Sources of data: (a) Cree Research, Inc. [4]
(b) Choycke and Pensl. [5]

2.3.1 Band Gap

The band gap is the energy (E_g) separating the conducting and valence bands in solids. It represents the minimum energy needed to excite an electron in a semiconductor material from the valence to the conduction band, and it is equal to the energy of the photon that is emitted in a luminescent transition. SiC has an indirect band gap, which means the bottom of the conduction band does not occur at K=0, where the top of the valence band occurs. Since SiC has an energy gap $E_g > 2.5$ev, it is considered a wide band gap semiconductor. It is important to note the larger band gap for SiC than GaAs or Si, as can be seen from Table 2.2.

2.3.2 Thermal Conductivity

Thermal conductivity of is the measure of a semiconductor's ability to conduct heat. The higher a semiconductor's thermal conductivity, the better the material. From Table 1, SiC has a higher thermal conductivity than GaAs and Si, which means that heat flows through SiC more readily. At room temperature, SiC has a higher thermal conductivity than any other semiconductor [4]. This is an important property for advanced electronics capable of operation at approximately 600 °C.

2.3.3 Saturated Electron Drift Velocity

The high value of saturated electron drift velocity of SiC makes devices created using this substrate capable of operation at high RF and microwave frequencies.

2.3.4 Breakdown Electric Field

The electric field at which the semiconductor allows the flow of high current through electrons avalanche is known as the breakdown electric field. Diodes do not allow current to flow in the reverse direction until the breakdown electric field is attained. Thus, the breakdown electric field is an indication of how difficult it is to make a diode conduct with reverse polarity. The dieletric strength of SiC is eight times greater than that of GaAs, making SiC a more suitable substrate for manufacturing of high power devices than the GaAs or Si.

2.3.5 Electron Mobility

The electron mobility is a measure of electron scattering in semiconductor crystals. Higher mobility in a semiconductor is necessary for high-speed applications. The electron mobility is a ratio of the electron drift velocity and the electric field:

$$\mu_n = -\frac{v_d}{E} \tag{2.1}$$

Where μ_c is the electron mobility and it is negative because electrons move in the opposite direction with respect to the electric field, V_d is the drift velocity of carriers (in this case electrons), and E is the electric field acting on the electron.

2.3.6 Hole Mobility

The hole mobility is a measure of the hole scattering in SiC and any other semiconductor. The hole mobility is a ratio of the hole drift velocity and the electric field acting on it. The equation for the hole mobility is the same as for the electron mobility but the symbol

μ_c is changed to μ_p and it is positive because holes move in the same direction as the electric field.

$$\mu_p = \frac{v_d}{E} \tag{2.2}$$

2.3.7 Other Properties

Other properties of SiC and other semiconductor materials that are important in device applications include the carrier concentration (*n, p)* and resistivity (ρ). The current density (*J*) is the product of the electron charge (*q*), the carrier mobility (μ_c), the carrier concentration, and the electric field:

$$J_n = q\mu_n n(x)E_x \tag{2.3a}$$

$$J_p = q\mu_p p(x)E_x \tag{2.3b}$$

The ratio of the current density and the electric field is the conductivity (σ).

$$\sigma = qn\mu_c \tag{2.4}$$

The resistivity is the inverse of the conductivity:

$$\rho = \sigma^{-1} \tag{2.5}$$

The resistivity of a wafer indicates the carrier concentration in the wafer material. The greater the resistivity, the lower the majority carrier concentration. The technique most commonly used to measure the resistivity and carrier concentration of SiC is the Hall effect measurements.

Edwin Hall discovered this effect in 1879, when he observed a small transverse voltage that existed in a thin strip of conductor carrying current in a magnetic field. The Hall effect enables the measurement of various characteristics of a semiconductor

material that are very important in the material's applications. Hall effect can be described as follows:

An electron moves through a square strip of semiconductor material (e.g. SiC), in response to forces acting normal to its direction, and it also moves due to the internal electric field force (See Figure 2.2). A current *I* flows along the *x* axis in the presence of a magnetic field *B*, perpendicular in direction to *I*. Electrons subjected to the *B* and E_x field forces drift in an opposite direction to *I* towards the edge of the semiconductor material. Holes, on the other hand, flow in the same direction as *I* towards the opposite end of the semiconductor material. Since electrons and holes are separated to opposite ends of the semiconductor strip, there remains an excess charge across the width of the semiconductor (*d*). This charge results in the Hall voltage, which is the potential difference across the width of the semiconductor strip.

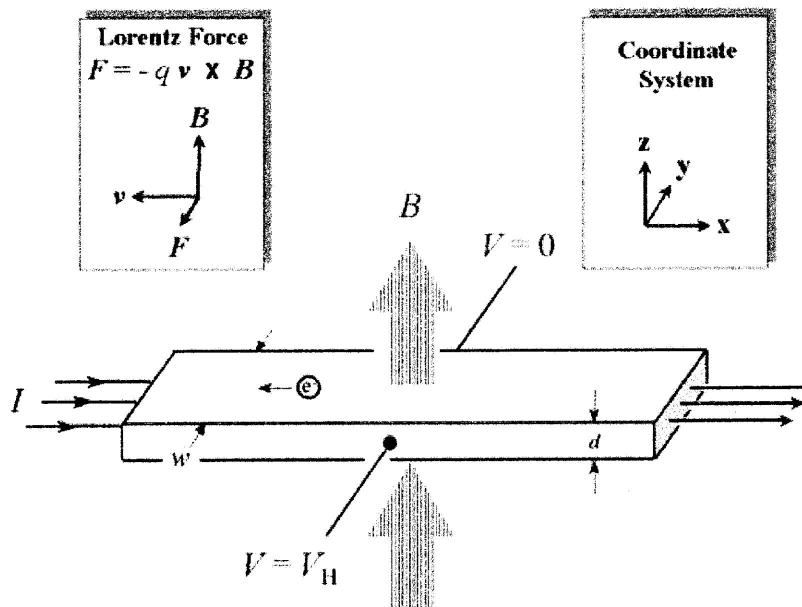

Figure 2.2. The Hall effect and Lorentz force.

For an n type semiconductor, the Hall voltage is:

$$V_H = \frac{IB}{qnd} \quad (2.6)$$

Where q is the electron charge ($1.6E^{-19}$ C), n is the electrom concentration and d is the semiconductor thickness. Thus, with known values of I, B, q and from the measured Hall voltage V_H, the carrier concentration can be calculated:

$$n = \frac{IB}{V_H qd} \quad (2.7)$$

To calculate the carrier mobility μ_c, one may apply the Van der Pauw technique to obtain the sheet resistivity R_s, and then μ_c is easily calculated:

$$\mu = \frac{V_H}{R_s IB} = \frac{1}{qndR_s} \quad (2.8)$$

and the bulk resistivity becomes:

$$\rho = R_s d \quad (2.9)$$

The Hall effect is useful for calculating the mobility, carrier concentration, material resistivity, and for dopant identification. The resistivity has been observed to depend on defects in SiC. This will be demonstrated in successive chapters in the thesis. The major drawback of the Hall effect measurement is that it is a destructive method of inspection, but it is a vital technique in the semiconductor industry.

2.4 Growth and Applications of SiC

The growth of SiC was only possible through the Acheson process for making abrasive substance from 1891 until the mid-1950's [6]. The principle behind the process was a reaction $SiO_2 + C \rightarrow SiC$. SiC became popular as an abrasive because it is the third hardest compound after diamond, and boron carbide. The Acheson process is still used today for producing SiC abrasives.

In 1955, J. Lely engineered a laboratory sublimation process for generating SiC crystals [7]. This method was an improvement on the pioneering Acheson process. The crystals produced through the Lely method were not suitable for the semiconductor industrial applications, because the formation of the scattered hexagonal crystals (Lely platelets) were non-uniform in size and location, but were, and still are, regarded as the highest purity SiC crystals [8]. In 1978, Tairov and Tsvetkov developed the Physical Vapor Transport (PVT) technique (sometimes called Modified Lely technique) of growing SiC. This technique was used to produce better SiC crystals that were applicable in the semiconductor industry. In 1987, the first growth with a seed was implemented using a modified Lely method [9]. In this technique, only one large crystal of single polytype was grown.

2.4.1 Physical Vapor Transport (PVT)

Physical vapor transport technique is the most popular technique now employed for the growth of SiC. The generation of single polytype, single crystalline, SiC was accomplished with the PVT technique. The PVT technique involves the sublimation of Si-C species transported due to a temperature gradient between the source (crushed SiC chunks grown through the Acheson method) and the area where SiC is deposited.

The Lely method and the Tsairov-Tvetskov are two variants of the PVT technique, with the latter being the preferred technique for growth of electronic grade SiC.

2.4.1.1 The Lely Technique. The Lely technique, developed in 1955, produced SiC with much better quality than the Acheson technique. In the Lely technique, a graphite cylinder and a larger diameter graphite crucible are used. SiC chunks produced through the Acheson method are placed between the graphite cylinder and the larger diameter graphite crucible. The crucible is closed with graphite lids and the setup is placed in an oven. The setup is baked at 2500° C in Argon atmosphere and 760-mmHg pressure [10]. SiC crystals (platelets) are deposited on the walls of the inner graphite cylinder. The outer graphite crucible is occupied by graphite layer after Si has sublimed to the inner graphite cylinder. The SiC crystals retrieved from the inner graphite cylinder are generally of a high quality, with low defect densities. The Lely technique is used to produce crystals of an average size of 5 mm x 8 mm [11]. This property of Lely grown SiC crystals, coupled with the fact that the polytypes cannot be controlled, the low yield from the process, and varying sizes of platelets, makes them inadequate for popular semiconductor applications.

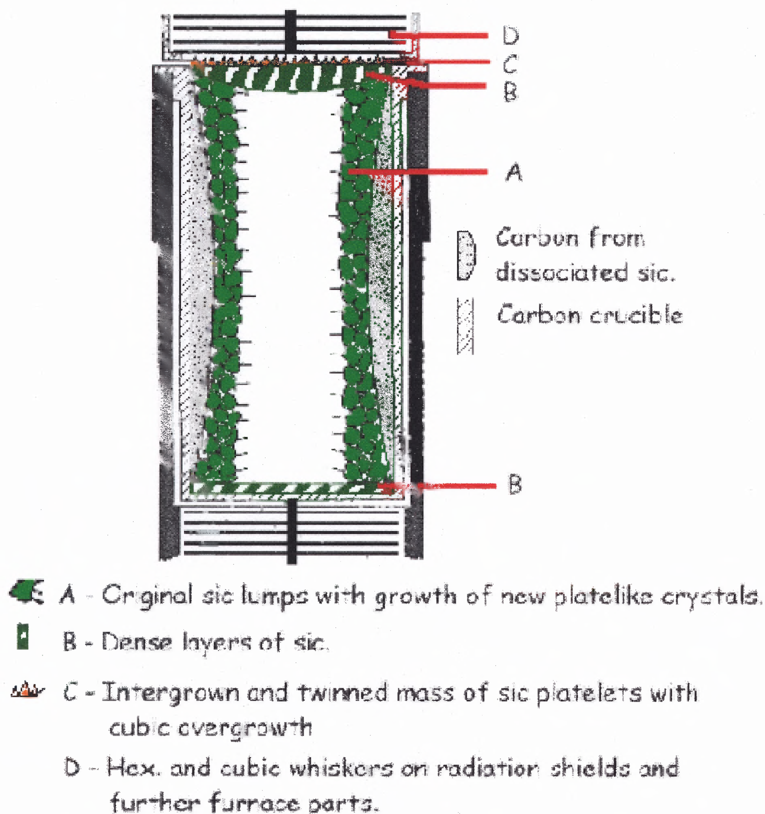

Figure 2.3 Cross Section of a Lely furnace (Knippenberg).

2.4.1.2 The Modified Lely Technique. Tairov and Tsvetkov modified the Lely process to overcome the shortcomings of the original Lely technique, which include, low yield, irregular sizes, and mixed polytype crystals. The modified technique employs the use of a SiC seed.

In the modified Lely technique, SiC chunks or powder (source material), are placed in a graphite crucible. The crucible is covered with a graphite lid with a SiC seed attached to the inside part of the lid. The crucible is placed in an insulating cylindrical housing made of graphite. The crucible is heated to a temperature above 2000° C, in an argon rich environment below atmospheric pressure. A temperature gradient of 20° C to

40° C is maintained between the seed and the source. The SiC source at the bottom of the crucible is at a hotter temperature than the seed. The source sublimes, with consisting of molecular species such as Si_2C, SiC_2, Si_2, and Si. Through thermal design of heat flow in the crucible, the seed is positioned so that the vapor is deposited on it, since it is the coldest region. A schematic of the modified Lely technique is shown in Figure 2.4.

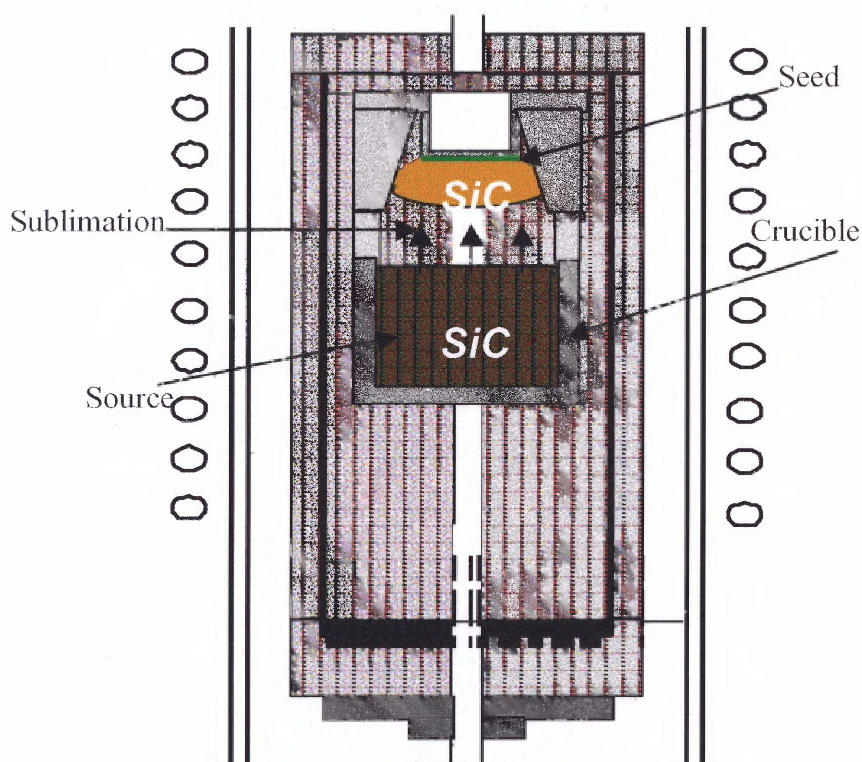

Figure 2.4. Schematic diagram of modified Lely chamber.

Many variables are considered when trying to achieve proper growth conditions. To grow a crystal at a fast rate, one can adjust the temperature, the temperature gradient, the pressure, and the distance between the source and the seed [36]. Growth of different polytypes can be achieved with the selection of seed orientation, and adequate temperature [13]. For example, it is known that 4H polytype is best grown on the C face (000-1) of the SiC crystal, whilst the 6H polytype is best grown on the Si face or the {0001} surface [10].

The growth rate is to a large extent also affected by the transport rate of different Si-C species from the seed to the source. C is transported to the seed by Si, as Si_2C, SiC_2, but Si vapor pressure sets the vapor limit of the total growth pressure [14].

One of the major problems encountered in the modified Lely process is the introduction of unwanted impurities such as Vanadium (V), aluminum (Al), sulphur (S), boron (B), nitrogen (N), and tungsten (W), which are all present in minute amounts in the crucible, from where they are transported into the boule. Some of these impurities alter the electrical characteristics of the crystal. Impurities can also be added intentionally (doping), to compensate and alter the characteristics of the crystal to achieve the desired properties.

The growth parameters must also be engineered so that the grown crystal is of single polytype. Mixed polytype in a crystal leads to domain problems, and ultimately, a poor crystalline quality. The seed used is another important variable for a good growth. The use of a poor seed leads to the growth of a poor crystal, which may be worse than the seed because defects may propagate and expand from the seed to crystal during the growth process. Localized eruption of polycrystalline growth as a result of local

evaporation of the seed leads to the propagation of defects in growth material, and is one of the major problems reducing SiC yield in the modified Lely process. Grain boundaries and other defects in a seed wafer are localized weak spots that easily vaporize or decompose at growth temperatures that result in eruptions. Another possible cause of major macro defects in crystals is due to the material with which the seed is secured to the lid of the crucible. Seed wafers are bonded to the lid of the crucible with a bonding agent strong enough to secure the seed in place at growth temperatures of 2000° C. When a seed is bonded to a crucible lid, there are often micro voids, or air pockets, were the bonding agent is not in physical contact with the seed and the graphite lid. During growth, such voids transfer heat through radiation, whilst properly bonded areas transfer heat through conduction. Thus, the temperature in these voids is higher in than other areas of the seed, leading to eruptions and thermal decomposition cavities.

Micropipes are the final product of the problems listed above is the creation of micropipes. Micropipe defects are a major problem for the production of electronic grade SiC crystals as most devices located around micropipes fail. Micropipes are screw dislocations with large Burgers vector [15]. They are essentially cylindrical pipes, 0.5 microns to 10 microns in diameter, that traverse along the length of the crystal. The delineation, qualification and quantification of micropipes will be treated extensively in the following chapters.

2.4.2 Doping

Doping of is the introduction of foreign impurities into the crystalline semiconductor material to alter the electronic properties of the semiconductor. Doping is principally used to achieve *n*-type or *p*-type properties in SiC and other semiconductors. For SiC to acquire *n*-type properties, donor impurities such nitrogen (N) is used. Nitrogen is a donor because it has more electrons than the atom it replaces [3]. Similarly, *p*-type doping leads to the introduction of holes. This is achieved by the introduction of acceptors, i.e. atoms with less electrons than those in the material. Aluminum (Al) and Boron (B) are acceptors in SiC because they have three available electrons, compared with four electrons of C and Si.

As an example of how the electronic properties of SiC are altered, consider SiC, which has two group IV elements with four valence electrons. It needs an atom with more than four valence electrons to make the material *n*-type. Nitrogen, which is group V element with one extra valence electron, is added. According to Burton, a donor state is created and nitrogen behaves like a donor in SiC. This state is the result of the additional charge on nitrogen N^+. The electron is attracted to the charge and "orbits" the donor atom like an electron in the hydrogen atom [3].

Dopants are introduced into SiC either through the normal sublimation growth process, through ion implantation, or through diffusion of impurities. Diffusion doping has been found to be undesirable for device fabrication and is not a method generally used for doping SiC. Doping through the growth process is utilized for N, B and Al doping. Nitrogen is introduced as a gas into the growth chamber during the growth process. Al can be added as part of the source material. Sometimes, other unwanted

impurities exist in high concentration in grown crystals. The source material and the graphite parts used in the growth process, may contain high quantities of impurity atoms, and often need to be purified before using them in the growth process.

Ion implantation is another alternative for introducing foreign impurities into the SiC crystal lattice. This technique is primarily used to create source and drain regions in field effect transistors. Al, N and B are common elements used in ion implantation. To implant these dopants, their atoms are fired at desired energy levels, depending on the distance at which the atoms need to be in the crystal. The material is annealed at a high temperature to activate the dopants. The problem with this technique is that at the high temperature used for annealing of SiC, Si preferentially evaporates and modifies the surface region. Several methods to impede the evaporation of Si from the material during annealing have been studied, amongst which the use of AlN cap that is stable up to ~1600° C is a possible solution [16].

2.4.3 Applications of Silicon Carbide

The physical properties of SiC make it an excellent substrate for the manufacture of device that will serve various industries such as the aircraft, automobile, power, spacecraft, communications and radar industries. Commercially available products based on SiC, include light emitting diodes (LEDs), power transistors, microwave transistors, RF switches and many others.

CHAPTER 3

SILICON CARBIDE DEFECT QUALIFICATION

3.1 Common Defects in Silicon Carbide

Silicon carbide is a material with impressive properties that will permit to manufacture devices that will function beyond current semiconductor device capabilities in terms of temperature. However, one of the major challenges in growing such a material is to eliminate the numerous defects seen in the material. Three types of dislocations exist in silicon carbide: threading screw dislocations, threading edge dislocations and basal plane dislocations [17]. Super screw dislocations are dislocations with Burgers vector of several tens of Angstroms. They are also known as micropipes, hollow tubes that run along the *c* axis of SiC crystals.

3.2 Micropipes: Super Screw Dislocations

Micropipes are hollow tube-shaped defects that are generally observed in several single crystalline materials, e.g. in CdI_2, PbI_2, ZnS, mica, hexagonal barium ferrites, GaN, and SiC [18]. It has been noticed that micropipes occur in material that exhibit polytypic characteristics. For these materials, the micropipes grow parallel to the polytype direction. There are several solid arguments that attempt to explain the formation of micropipes, but the limitations of existing imaging techniques make it difficult to provide structural demonstrations of micropipes. Most theories on micropipes are based on Frank's model of hollow core screw dislocation [19]. It is useful to understand this model when studying micropipes.

3.2.1 Observations of Micropipes

A possible explanation of the physical nature of hollow screw dislocation was given by Frank in the late 50's. Heindl noted that the strain field around a dislocation that has a Burgers vector greater than 1nm contains such high energy, that it is preferable to remove the crystalline material adjacent to the dislocation line, and to create an additional surface in the form of a hollow tube [18]. Frank deduced a mathematical model of the hollow core dislocation with the Burgers vector B and the hollow tube radius r_o (Frank radius) from total energy minimization by considering the dislocation caused strain energy E_{dis}, and the energy used to create the hollow tube around the dislocation E_{surf}.

$$\frac{d(E_{dis} + E_{surf})}{dr_o} = 0 \tag{3.1}$$

$$E_{dis} = \frac{\mu B^2}{4\pi} \cdot \ln \frac{r}{r_o} \tag{3.2}$$

$$E_{surf} = 2\pi r_o \gamma \tag{3.3}$$

where μ is the shear modulus and γ is the surface energy. Assuming a pure screw dislocation creating a micropipe we obtain the equilibrium radius of the stable micropipe as:

$$r_o = \frac{\mu B^2}{8\pi^2 \gamma} \tag{3.4}$$

3.2.2 Evaluation of Frank's Model

Several authors have verified the relationship between r_o and B^2 in Equation 3.4 using different measurement techniques. For example, Dudley et al. [23] used SWBXT to determine the Burgers vector of a dislocation, a scanning electron microscope used to determine the radii of micropipes. Dudley studied 6H-SiC samples and reported radii ranging from 50 to 2100 nm. Utilizing a shear modulus of 200 Gpa and applying Equation 3.4, a surface energy of 0.25 (± 0.05) Jm^{-2} was calculated for the inner surface of the micropipe.

Giocondi et al. [24] measured the radii of micropipes by atomic force microscopy (AFM) of 6H-SiC crystals. The radii of micropipes were determined by evaluation of a topographic profile across micropipes. The difference in height on both sides of micropipes was also evaluated, and the topographic analysis allowed the calculation of the screw component of the Burgers vector in the micropipe. Micropipe radii from 90 to 160 nm were used to obtain results similar to Equation 3.4 with the surface energy of 4 Jm^{-2} [20].

Heindl et al. also measured the micropipe radii in two 6H-SiC crystals using AFM. The radius of the micropipe was measured by summing up several line scans across the middle of the micropipe. The screw component of the dislocation in the micropipe was measured by summing up the heights of upwards and downwards steps of the accompanying growth spirals [18]. Micropipe radii between 25 to 6000 nm were found and in order to fit this data a kinetic extension by Cabrera and Levine [21] was added to Frank's theory. The respective analysis leads to a surface energy of 0.14 Jm^{-2},

and with the addition of an edge component of the Burger's vector in the micropipes, the surface energy becomes 0.79 Jm^{-2}.

The consensus by the three studies summarized above agree that micropipes in SiC are hollow core dislocations in accordance with Frank's model, and that a dislocation stabilizes the hollow shape of the micropipe. However, this does not seem to be the case with micropipes in GaN substrates as Liliental-Weber et al. [25] discussed having observed micropipes that do not contain a dislocation.

Additionally, there is a discrepancy amongst studies about the smallest hollow core Burgers vector. Heindl et al. observed hollow holes even around dislocations with an elementary Burgers vector, in 6H-SiC of 1.5 nm [18], whilst Dudley et al. found elementary dislocation not being hollow. The smallest hollow core dislocation had a Burgers vector of 3 nm or two unit cells [23]. Giocoindi observed that the smallest Burgers vector in a micropipe had to be four unit cells or 6 nm, in order to stabilize a hollow core dislocation. Liliental-Weber et al. reported micropipes in GaN without any Burgers vector. Obviously, the need to improve the measurement techniques for analyzing the formation of micropipes is necessary to understand the nature and origin of micropipes. It should also be mentioned that AFM measurements only represent the screw component of the dislocation in a micropipe, it disregards the edge component that might exist and will alter results.

3.2.3 Formation of Micropipes

There are two hypotheses that try to explain why micropipes form. One idea is of processes that lead to the existence of a screw dislocation with a large Burgers vector and a hollow core in accordance with Frank's theory. The second idea is the existence of

mechanisms that generate depressions in the growth surface that may attract dislocations to stabilize the formation of the hollow tube during growth [18].

Liliental-Webber et al. suggests that micropipes are generated in GaN as a result of depressions at the growth surface that are caused by crystalline inhomogeneities, which result in the formation of several crystalline facets. It is also suggested that due to their different crystalline orientations, the various crystalline facets grow at different rates. This non-uniform growth rate may lead to depressions in the growth surface that may lead to micropipes. These facets have been found at the end of micropipes in GaN [25].

Yang et al. made a different observation in SiC boules. The authors observed particles in the grown boules. They propose that these particles are pushed from the seed to the top of the boule during growth. This, they reason, should leave a hole tube behind.

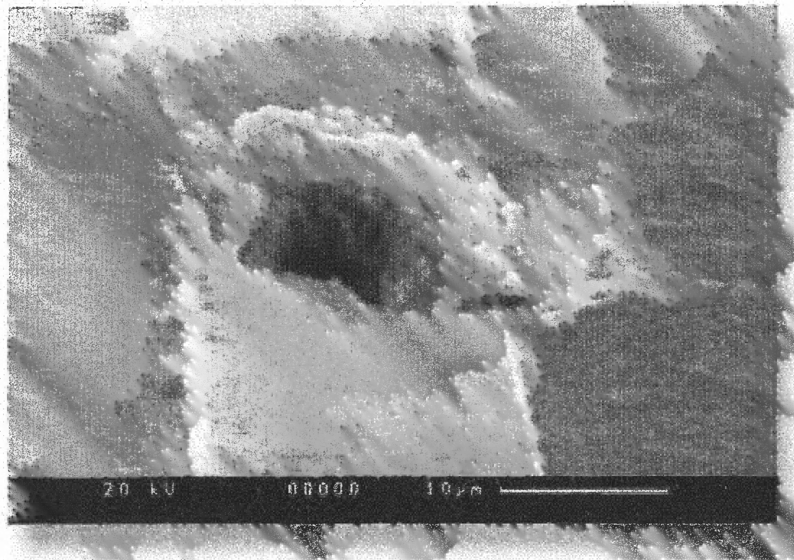

Figure 3.1 Scanning Electron Microscopy (SEM) image of micropipe from a silicon carbide crystal [26].

Baronnet and Turner et al. [27], [28] proposed similar mechanisms that generate dislocations with large Burgers vectors. Their work looked at synthetic mica and hexagonal barium ferrites, respectively, which had large screw dislocations with hollow cores. They observed that platelets grew laterally on the growth surface. Baronnet observed two platelets growing towards each other, eventually overgrew one another, likely forming a screw component. Turner reported a mechanism where the arms of a single platelet overlap. In the corner of the arms, a hollow core and a screw dislocation was found. It is important to note in both cases the screw component of the dislocation and hollow cores were formed simultaneously.

Giocondi et al. proposed a model for the formation of super-dislocation/micropipe that involve accumulation of unit screw dislocations due to a macro steps that grow around the heterogeneous material on the surface. During growth, these steps sweep up dislocations by shifting their emergence points in the growth direction. These macro steps stop at obstacles such as second phase inclusions, and restart as another complete macrostep, leaving behind a depression, which contains the collected screw dislocations.

All authors listed above agree that micropipes in SiC are hollow core that follow the theory developed by Frank, but there are differences in opinions and observations as to the process of the formation of superscrew dislocations. The Burgers vector can be of a mixed nature composed of a screw and edge components.

3.2.4 Dislocations

There are various types of dislocations that exist in SiC. Ha et al. investigated three types of dislocations in low-doped homoepitaxial layers by KOH etching, optical microscopy, synchrotron white beam X-ray topography (SWBXT), scanning electron microscopy (SEM), and atomic force microscopy (AFM). The dislocation types observed were threading screw, threading edge and basal plane dislocations. The dislocations were revealed by KOH etch of the sample crystals. After etching, the pits due to threading screw dislocations were found to be larger and deeper than those due tothreading edge and basal plane dislocations. Additionally, the size and depth difference became more pronounced with longer etch times.

The degree of perfection of a crystal depends on the dislocation density in that material. Dislocations act as recombination centers for electrons and holes, as traps for electrons, as leakage paths for current, and as lines of higher diffusion rates that worsen device characteristics [29]. A simple method of determining the crystal quality of SiC is through analysis of X-ray rocking curves. Rocking curves indicate the existence and degree of mis-orientation of grains and sub-grains within a small section of a wafer. Figure 3.1 shows rocking curve measurements of crystals grown by the Lely process and the modified Lely process. The rocking curve with the dotted line corresponds to a Lely platelet. Note that the curve has a single peak and a full width at half maximum (FWHM) of approximately 10 – 20 arc-seconds. This means that the crystal, or the measured area of the crystal, contains a single domain. This is typical for good quality Lely platelets, but not so common for samples grown by modified Lely seeded sublimation. The superimposed rocking curve with the solid line represents a crystal grown by seeded

sublimation and the modified Lely process. Notice the numerous peaks composed in a broad band. These peaks represent several low angle grain boundaries, or several mis-oriented domains that reflect the incident x-ray at specific angles (Bragg angles separated by the degree of misorientation). These grains have typical sizes from microns to millimeters. One can get a rough idea of the domain size by varying the X-ray probing beam size. It is proposed that an intricate network of densely packed defects form boundaries around the grains. KOH etched SiC wafers show a network of lines, which are the boundaries between domains or grains.

A single point x-ray rocking curve is representative of a very small area (typically 1mm x 7mm at its largest or 0.5mm x 0.5mm at its smallest) of the wafer. Wafer maps of multiple points can be developed with current x-ray software, and the results are more representative of the whole wafer. The width of X-ray rocking curves is broadened from the theoretical minimum set by temperature (vibration of atoms) by defects such as dislocations, voids, thermal decomposition cavities, dislocations at grain boundaries etc. The width is also widened due to misoriented grains, which also show up as multiple peaks. Thus, one of the most informative dislocation and misoriented grains maps are of the FWHM and the shift in omega (ω) across the wafer. Figure 3.2 shows a 49 point, 30mm x 30mm, FWHM map using a Philips XRD system.

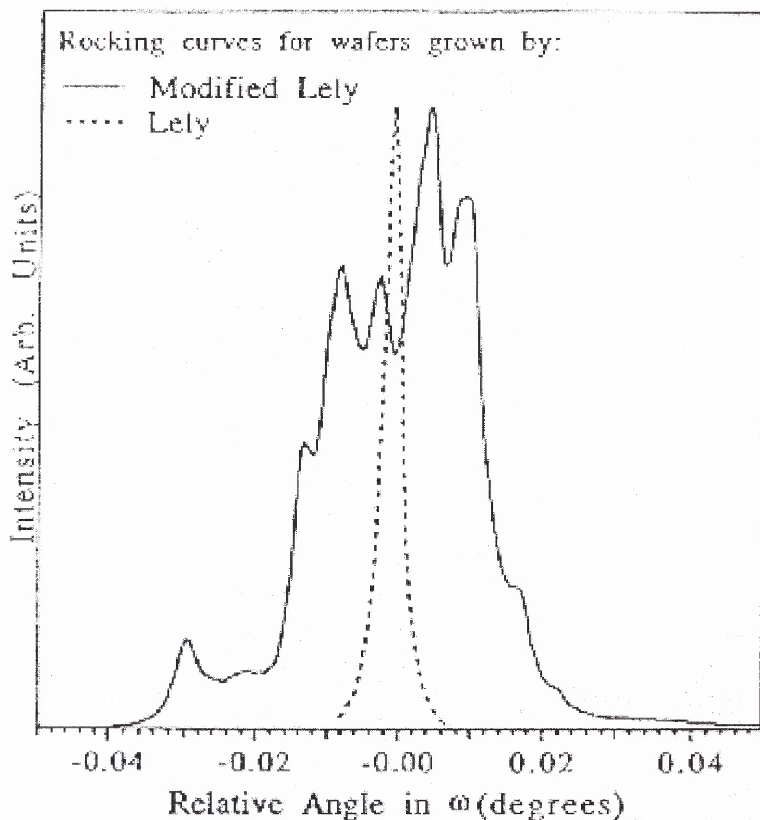

Figure 3.1 Comparison between Lely grown platelet (dotted line) and Modified Lely grown crystal (solid line). Lely grown platelets often have single peaks representative of a single domain crystal.

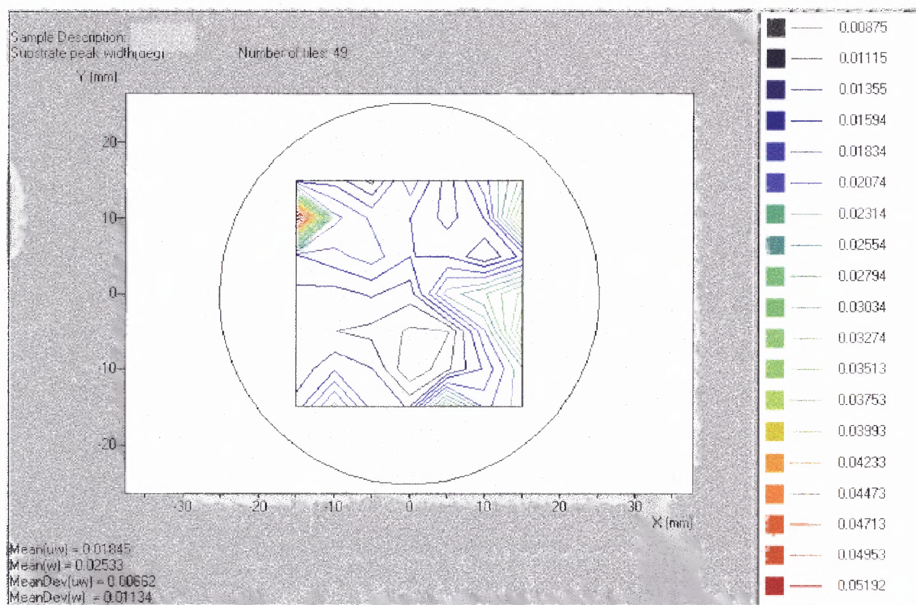

Figure 3.2 49 point, 30mm x 30mm, X-ray FWHM map of a 2 inch wafer (Average FWHM ~ 66.6 Arc-seconds).

The FWHM map shown in Figure 3.2 gives a quick observation on the quality of the crystal. From studies done with high purity Lely samples we know that a crystal area that has a single domain has an x-ray rocking with FWHM of less than10 arc-seconds. Rocking curves that have FWHMs greater than this range most likely have several peaks, thus several domains. For example, looking at Figure 3.2 we can immediately see that there is an area of extremely high purity crystalline structure to the bottom-left of the image. That section of the wafer has an average FWHM of approximately 30 arc-seconds. The scale to the right of the image gives a color-coded guide to the FWHM in degrees (1 degree = 3600 arc-seconds).

However, on the top-right of the image is a small area of very poor crystalline structure. The average FWHM in this area is 178 arc-seconds. This is an area with a high density of mis-oriented grains and low angle grain boundaries.

3.3 Destructive Methods of Revealing Micropipes and Other Defects

There are various techniques in practice today that are geared towards imaging and qualifying defects in SiC, especially micropipes. These techniques can be either destructive or non-destructive. Some examples of non-destructive methods of material characterization are discussed in Section 3.4.

Faust listed six basic etching processes, four of which apply to SiC.

(a) Chemical – The material surface is caused to undergo chemical change, with the condition that the reaction products leave the surface.

(b) Electrolytic – The flow of electric current is necessary to causes dissolution of the material in a suitable electrolyte (the products evaporate or are dissolved).

(c) Alloying – Molten materials can be used as etches because of their ability to dissolve solid materials.

(d) Cathodic Bombardment - The etched material is a cathode in glow discharge. The energy from the bombardment drives atoms from the surface of the material (e.g. plasma etching).

Out of the four techniques mentioned above, the method of interest is chemical etching with a molten salt. In order to etch a material such as SiC, it is necessary to form compounds with each of the elements (Si and C). Since SiC is chemically inert at low temperatures, etching has to be performed at high temperatures. Various etches have been used for SiC wafer defect delineation, including molten Potassium Hydroxide (KOH) etching, KOH vapor etching, hot phosphoric acid, and various other etchants that were primarily studied in the 1960s, including $Na_2B_4O_7$, Na_2O_2 and $NaF{:}Na_2SO_4$ [29]. The last three etchants gave problems of high temperature, high viscosity, severe chemical attack to the crucible and instability of the respective etchant. Hence, KOH eventually became the etchant of choice for etching of SiC.

Most of the earlier papers were on studies done using SiC crystals grown by the Acheson or Lely method. The crystals were not very well engineered such that parameters like polytype and carrier concentrations were not properly controlled. This has led to a limited source of reliable quantitative data on SiC etching characteristics, so that a fundamental knowledge of the chemical mechanism of etching in SiC is limited.

3.3.1 Potassium Hydroxide Etching of SiC Single Crystals

Potassium hydroxide etching of SiC wafers is an industry-wide practice that is popular because its ease of use. Etching in molten KOH reveals common defects in SiC, of which micropipes are the most important. It is important to achieve a smooth surface after etching as this allows easier qualification of defects. Gabor and Jenning [30] observed that during etching with NaF:Na_2SO_4, stirring the etchant by pumping of gas into the melt resulted in smooth etched wafer surfaces. Katsuno et al. [31] instead of pumping gas into the melt stirred the melt by rotating the sample holder and achieved an improved spatial variation of etching rate from (± 100%) to (± 12%). Katsuno et al. also reported that the protection of the backside (carbon face) of the sample is important to achieve accurate estimates of the Si face removal. A polished SiC wafer was used as a mask for the backside of the etched crystal. This was an important step to achieving the spatial variation that was reported. What is not addressed is results from etch runs that involve only one of the two variables mentioned above.

However, it is important to have a very high etch rate of defects compared to the surface etch rate to delineate them. Figure 4.1 shows etch rate versus time. The initial etch rate represents the removal of the work damage, and the later, more gradual etch rate represents the normal material removal. A general description of KOH etching is provided below.

The general procedure of KOH etching of SiC in a vertical anneal furnace (see Figure 3.3) is as follows. Nickel crucibles are used, as they are generally inert to molten KOH. Solid KOH pellets are heated above the melting point temperature (375°C). The SiC crystals are placed in holders made of nickel. A temperature range from 400°C to

550°C for the molten KOH is suitable for etching. Higher etching temperature will increase the removal of SiC [31]. The etch rate also depends on the degree of oxygen in the ambient around the system as well as the quantity of KOH used. The etch rates also depends on the depth of damage, polytype differences, variations in orientation,

Figure 3.3 Typical anneal furnace used for potassium hydroxide etching (KOH) of SiC.

doping level differences and variation in temperature. Some of these relationships have been investigated by other authors and their findings will be summarized later. Results obtained from the experiments performed on KOH etching in preparation of this thesis will also be presented.

The etch defects can be viewed utilizing an optical microscope with a 50X or higher magnification. Figure 3.4 shows an image of a section of a KOH etched SiC sample as seen with optical microscopy.

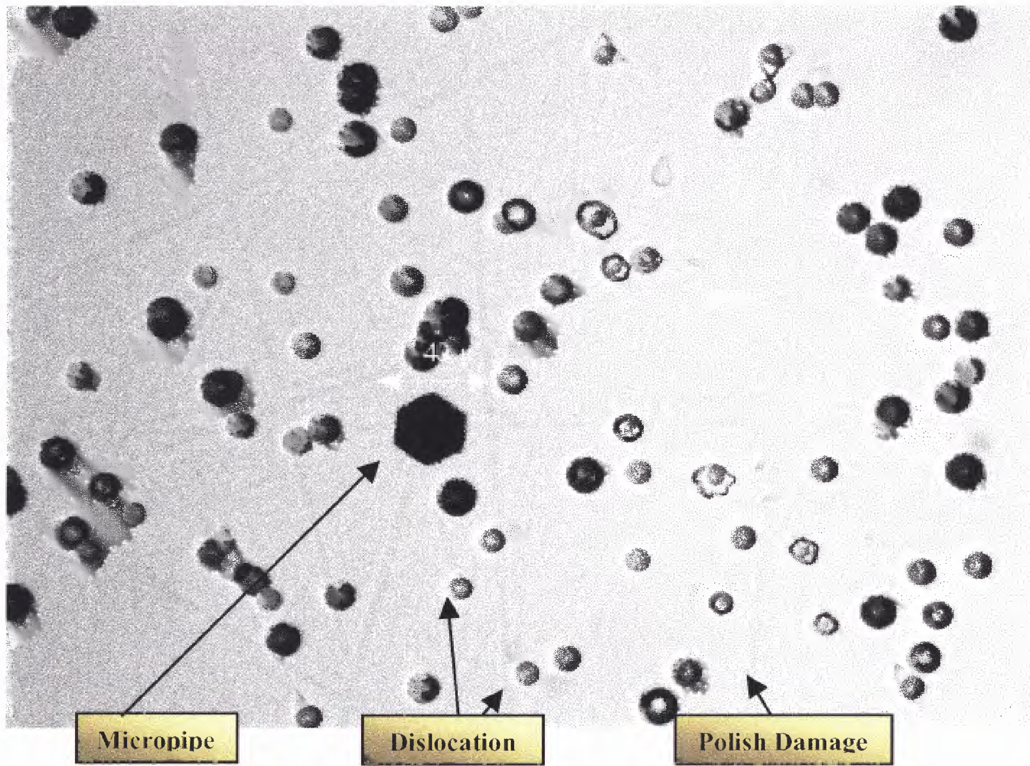

Figure 3.4 An optical microscopic image of an etched 4H silicon carbide wafer showing defects.

3.3.2 Potassium Hydroxide Vapor Etching of SiC Single Crystals

Although molten KOH etching is a common technique for the delineation of defects in SiC, various shortcomings of this technique have prompted scientists to investigate possible modifications to the technique. These shortcomings include the difficulty in etching defects on the (0001) C face of SiC, difficulty in separating different specific dislocations, dependency on doping levels, type of impurity, surface finish, sub-surface damage, and other material properties. Moreover, the delineation of defects on the (0001) C face of SiC will become very important for growth of 4H material, which is grown on the (0001) C face of the seed wafer. For this reason, the use of molten KOH vapor as an etchant is currently been investigated as a potential technique of delineating several SiC crystalline defects.

Bondokov et al. used this technique to etch 4H-SiC crystals that were sliced parallel to either {0001} or {1120} planes. The crystals used were n-type and had doping concentrations around 5E16 to 3E19 cm^{-3}. The etching experiment was performed under normal KOH etching procedure described earlier. A muffle furnace was utilized and the SiC wafer was suspended above the molten KOH. The temperature of the melt was set at 700°C to 1000°C. The 4H-SiC samples were etched for duration of a few minutes to 40 minutes at atmospheric pressure. The etching rate was determined by weight loss of the wafer, and by thickness measurements.

Figure 3.5 Typical muffle furnace used in vapor KOH etching of silicon carbide.

Several advantages observed by Bondokov et al. include the use of small quantities of KOH (10 cm^3), the lag time before etching is reduced because there is no

waiting period for the melt to stabilize at a desired temperature, and the reaction between KOH and SiC begins immediately after the specimen is exposed to vapor.

The activation energy (E_A) for the system was calculated using the material loss in the etching phase. The values for *c*- and *a*-face wafers were reported to be approximately 17 kcal/mol and ~20 kcal/mol respectively. The corresponding activation energy for molten KOH is18 kcal/mol. Microscopic observations showed the presence of etch pits on all planes analyzed. Reported etch rates (≥0.02mg/min.cm^2, which is equivalent to 0.5μm/min, for the sample with a surface area of 0.4 x 0.4 cm^2) for this process were observed at temperatures above 900°C. Lower temperatures led to delineation of sub-surface damage/scratches due to plastic deformation caused from wafer's fabrication and polish processes. Optimal conditions for delineation of dislocation were observed at 1000°C and an etch duration of five minutes.

Selective etching in molten KOH is a reaction-limited process, thus preferential etching occurs [32]. The etch rate variation in the Si and C faces is explained by the different surface energies on the respective faces. However, with KOH vapor, etching is limited by adsorption and desorption routes [33].

Bondokov et al. explain that KOH vapor is adsorbed into the SiC material due to Van der Waals forces. The easiest route into SiC material is in defective areas with more bonding sites exist and where reaction between KOH and SiC occurs. The reverse process (desorption) then occurs, whereby the reactive materials evaporate from the SiC surface. This explanation indicates why there are no differences observed in the etch rates on the Si-, C-, *p*-, and *a*- faces and the delineation of defects on all faces.

Recent attempts by this thesis author to duplicate the work reported by Bondokov on 6H-SiC with carrier concentration greater than 10^{17} cm^{3} confirms his results. However, similar experiments with compensated highly resistive 6H-SiC material, at a temperature of 700°C and duration of several hours showed only defects due to plastic deformation from the fabrication and polishing of the material. Further investigation of this finding is needed.

3.4 Non-destructive Methods of Qualifying Micropipes and Other Defects

Although characterization of SiC using etching in molten KOH is the most common technique in use, it is a costly one that leaves the wafer unusable afterwards. There are several imaging methods that are used to characterize micropipes without any processing of the polished samples. These techniques include SWBXT, AFM, SEM, TEM and transmission optical microscopy. Of these techniques, only SWBXT is capable of reliable detection of dislocations as well as micropipes on an un-etched sample. The SWBXT system and transmission microscopy will be described in the following pages.

3.4.1 Synchrotron White Beam X-ray Topography of SiC

Synchrotron white beam x-ray topography (SWBXT) is considered the most effective technique for characterization of micropipe, or pure super screw dislocation on the (0001) plane of SiC wafers. The technique has a high strain sensitivity and suitable spatial resolution [34]. Micropipe images typically appear as a dark circle surrounding a white core (see Figure 3.8). This image can be magnified to tens of microns to give a unique resolution of the micropipe image. SWBXT was principally employed to show "unambiguously and quantitatively that micropipes are pure screw dislocations" [38]. It

is typically employed to give a relatively precise density distribution of defects in SiC material.

Figure 3.7 shows the diffraction geometry of the SWBXT system from Huang et al. where **r** is the position vector, s_0 and s_g are the unit vector directions of the incident and the diffracted beams respectively, **n** is normal to the (0001) plane, θ_B is the Bragg angle and **b** is the Burgers vector with a c-spacing of polytype repeat pattern c = 15.18Å. The diffraction equation is shown below:

$$S_g(\mathbf{r}) = S_0 + 2 \sin \theta_B(\mathbf{r})\mathbf{n}(\mathbf{r}) \quad (3.5)$$

The local Bragg angle is given by the equation:

$$\theta_B = \pi/2 - \cos^{-1}[-S_0, \mathbf{n}(\mathbf{r})] \quad (3.6)$$

If one considers a single pure screw dislocation that is along the z direction, then the lattice displacement can be shown as:

$$u_z = \frac{b\varphi}{2\pi} \quad (3.7)$$

where b is the magnitude of the Burgers vector **b.** Differentiating u_z with respect to the cylindrical coordinates we derive the normal to the (0001) plane.

$$n_r = 0 \quad (3.8a)$$

$$n_{\varphi} = -\frac{b}{\sqrt{b^2 + 4\pi^2 r^2}} \tag{3.8b}$$

$$n_z = \frac{2\pi r}{\sqrt{b^2 + 4\pi^2 r^2}} \tag{3.8c}$$

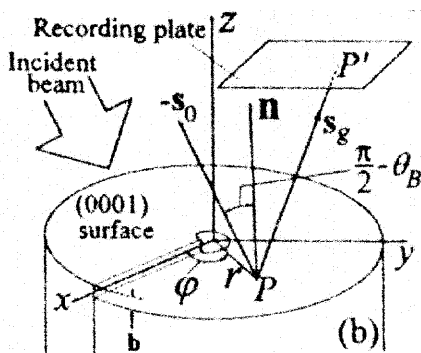

Figure 3.7 Schematic of synchrotron white beam X-ray topography system [34].

n_r, n_φ and n_z are the three components of **n** in the polar coordinate system [38]. With **n**, derived, the direction of the diffracted beam reflected from anywhere on the crystal surface can be calculated with Equation 3.6. This enables the correct representation of features from the surface to be represented on the recording plate. The sample's surface is divided up onto tiny squares in relation to diffraction intensity, and each square with a unique intensity level is projected onto the recording plate, and due t the sum of the intensities that each point on the recording plate receives dictates the contrast level for that spot.

3.4.2 Optical Transmission Microscopy

Optical transmission microscopy has a wide variety of applications. Additionally, it can be further enhanced with the use of polarized light. It is particularly suited for observing micropipes in un-etched SiC crystals, and can achieve field of view of 0.65mm x 0.65mm using a 100x objective [35].

Transmission optical microscopy has been used for some time as a method for observing and mapping micropipe density distribution in SiC wafers. It is very economical to setup a system for this type of characterization, and an advantage of this technique over KOH etching is that the unwanted destruction of SiC crystal is not necessary. However, since optical microscopy has a limit of resolution of 0.6μm due to the wavelength of visible light [38], micropipes with diameters less than 0.6μm may be difficult to observe using optical transmission microscopy except the object scatters enough light, or the light is polarized.

For this technique, the wafers have to be double side polished otherwise the backside scatters too much light. Elkington & Emorhokpor et al. reported a micropipe mapping technique by bonding a sapphire wafer unto a SiC wafer. The sapphire wafer is laser marked into squares of 0.5 cm x 0.5 cm, with the wafer position adjusted with an automated slide.

It was also demonstrated that observed patterns of micropipe density was found to be non-Poisson, not random, and were highly non-normal. This is caused primarily because of a clumping effect observed in micropipes. Figure 3.8 shows an optical microscope field view of a SiC wafer with micropipes similar to long tail shooting stars.

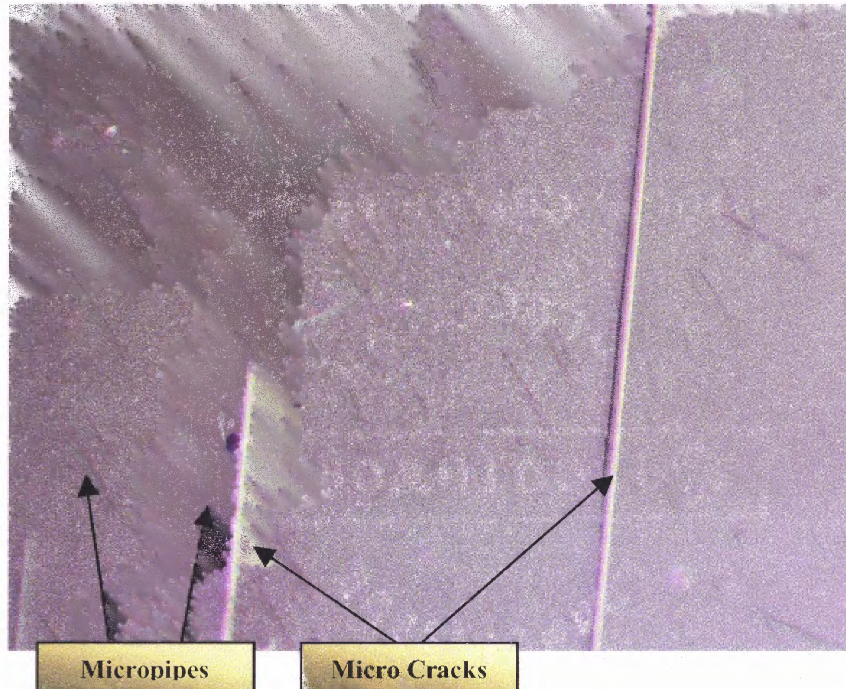

Figure 3.8 Optical transmission microscopy view field of a silicon carbide crystal.

3.4.3 Other Characterization Techniques

Several other techniques applied in the analysis of SiC crystalline defects include very high-resolution imaging systems such as atomic force microscopy (AFM), scanning electron microscopy (SEM), transmission electron microscopy (TEM), etc. These systems have been vital in understanding the physical profiles of nano- and micro-scale micropipes, and they have enables many studies into the possible formation of micropipes. Descriptions of these systems will not be considered in the thesis, mainly because these tools target high-resolution study (atomic scale) of defects, instead of the spatial distribution and mapping of defects across an entire wafers surface.

CHAPTER 4

POTASSIUM HYDROXIDE ETCHING OF SILICON CARBIDE

4.1 Materials and Methods

Silicon carbide crystals grown by the modified Lely process at *II-VI Incorporated* were utilized in these experiments. Several wafers were sliced and mechanically polished to a $1\mu m$ surface finish (roughness ~ 10 – 15 Å). Several as-sawn (unpolished) samples were also used (roughness ~ 1500 Å). The samples were all 6H-SiC; nitrogen doped with concentrations $1 \times 10^{-15} - 9 \times 10^{-18}$ cm $^{-3}$, and sliced on-axis (orientation ~ $0^o \pm 0.5^o$). All wafers were 2" in diameter, approximately 420 – $450\mu m$ thick, and were obtained from various boules. In addition, sapphire (Al_2O_3) wafers were also etched for comparison of how the two substrates react under similar conditions and for demonstrating the effects of surface finish on etch rates.

Etching has been carried out in a box furnace (for general description of etch procedure see Section 3.3.1). Solid KOH pellets were held in a nickel crucible, which was heated in the furnace. The temperature was maintained constant at 450°C, and was controlled with an accuracy of ± 5°C. The process was performed in air at atmosphere pressure. The wafers were suspended above the molten KOH for 5-minutes to avoid breaking the wafers upon immersion into the melt due to thermal shock. The process duration varied between 1 – 15 minutes after the molten KOH reached a steady state at the process temperature. The etch rate was calculated from the weight difference before

and after etching (balance with an accuracy of 0.1mg). The etch patterns were observed using a Leitz Ergolux microscope with an affixed CCD camera.

4.2 Results and Discussion

Figure 4.1 shows the measured dependence of etch rate of SiC on etching time. The samples used in these tests had as-sawn surfaces that have not been plastically deformed through a polish process. The etch rate is highest in the first minute (etch rate ~ 0.7 μm/min) and quickly decreases to about half the initial rate (etch rate ~ 0.36 μm/min) after 3minutes. After fifteen minutes the rate of etching has reduced to about 25% of the initial value (etch rate ~ 0.18 μm/min).

Katsuno et al. reported an etch rate for 6H-SiC of approximately 0.5 μm/min on the (0001) Si face, which is close to the initial etch rate shown in Figure 4.1, and represents the combined etch rate for both (0001) Si and (000-1) C face. The as-sawn SiC surface is very rough (Ra ~ 6 μm). The initial high etch rate in Figure 4.1 is due to preferential etching of the surface damage layer. The etch rate is dependent on the surface finish of the wafer as well as the quantity of defects. Figure 4.4 shows the instantaneous etch rate versus depth for as-sawn and double side polished SiC wafers. Note that the initial etch rate for the double side polished wafer is less than half of the as-sawn wafer. This is due to the reduced roughness on the wafers' (0001) Si and (000-1) C faces. The depth of material removal as it preferentially etches away defects is much smaller in the double side polished wafers compared to the as-sawn wafers. Figure 4.2 shows the depth of etch affected by the etch rate for the as-sawn 6H-SiC wafers. The etching process

achieved a 6 μm overall material removal in 15 minutes. The cumulative material removal versus the duration of etching is shown in Figure 4.3.

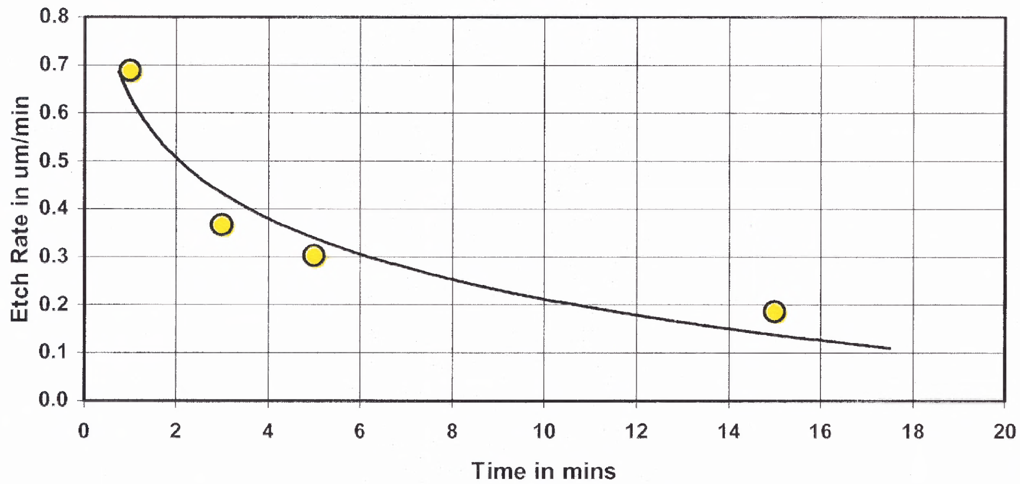

Figure 4.1 Time dependence of KOH etch rate. Solid line fit of logarithm function to the data ($y \sim 0.7 - log_{150}t$).

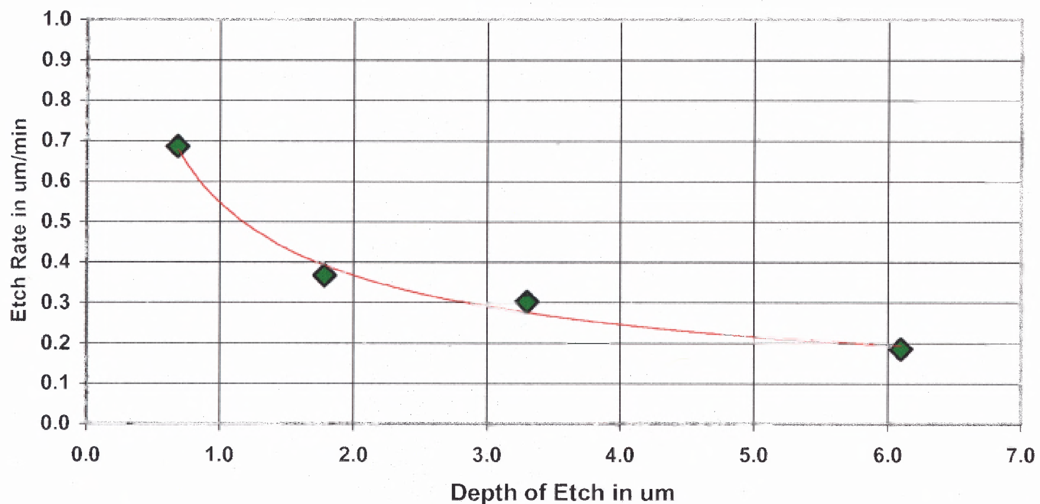

Figure 4.2 KOH etch rate versus depth of material removed. Solid line fit of logarithm function to the data ($y \sim 0.55\text{-}log_{131}x$).

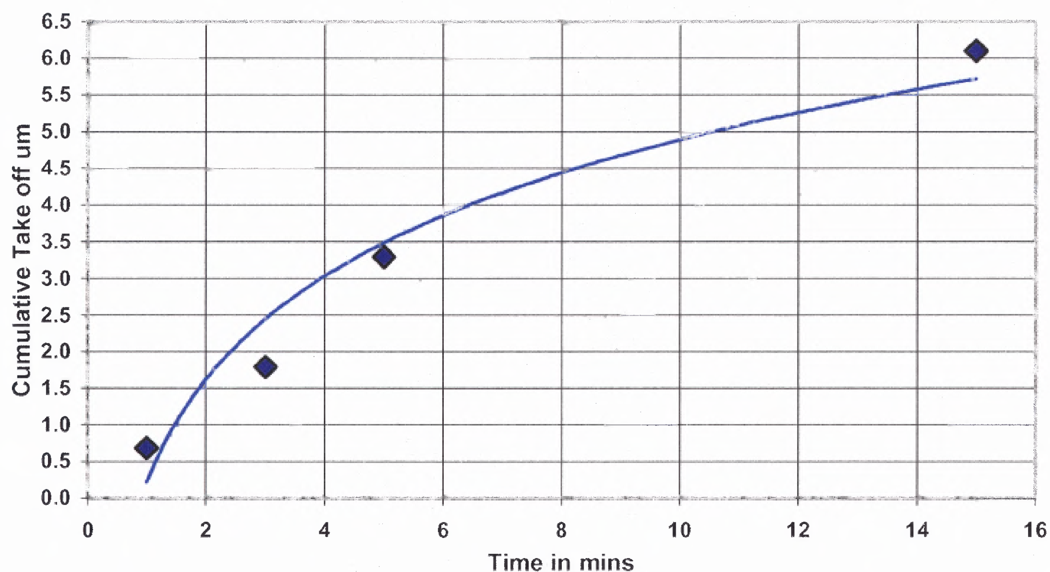

Figure 4.3 Time dependent cumulative material removal. Solid line fit of logarithm function to data ($y \sim log_{1.6}t$).

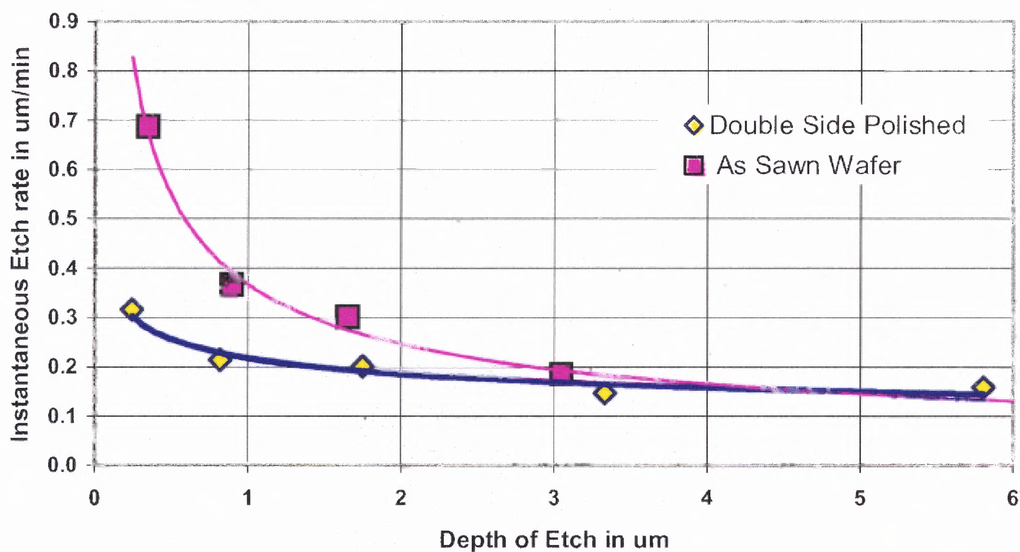

Figure 4.4 KOH etch rate versus depth of material removed for as-sawn and double side polished SiC wafers.

Figure 4.5 to 4.9 show optical microscopy images of etched heavily doped 6H-SiC samples after different etch intervals. It is interesting to note how the features of defects enlarge in time. If etched longer, these features will overlap, after which characterization of the material becomes difficult. Notice the relatively short etching duration it took to start revealing defects in this material. After 1-minute, defects already start to appear. In 3-minutes, there is a network of defects and scratches from the wafer processing. After 5-minutes, the defects start to enlarge in size. After 10-minutes, the defects become clearer, and the features of the polish induced scratches become clearer. After 15-minutes, the defect features are amplified and one can clearly see the different types of dislocations present.

Figure 4.10 to 4.12 show optical microscopy images of etched lightly doped, semi-insulating, 6H-SiC wafers at different intervals. When lightly doped semi-insulating material is etched, it takes a longer duration before defects are revealed, confirming that the etch rate and the delineation of defects is affected by the carrier concentration in the material. After 1-minute one cannot see any defects or scratches from mechanical polishing of the wafer. After 5-minutes an extensive scratch network caused from processing of the wafer can be seen. After 10-minutes one can see scratches but cannot observe any defects. Not until 10 minutes of etching do the defects start to appear.

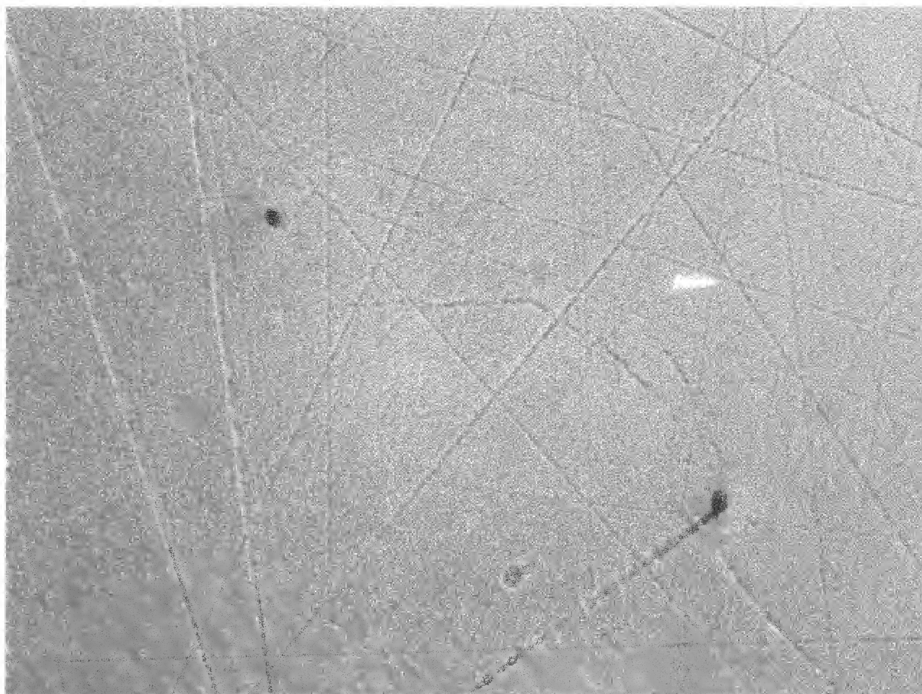

Figure 4.5 1-minute KOH etched wafer (6H-SiC, $N^+ > 10^{17} cm^{-3}$).

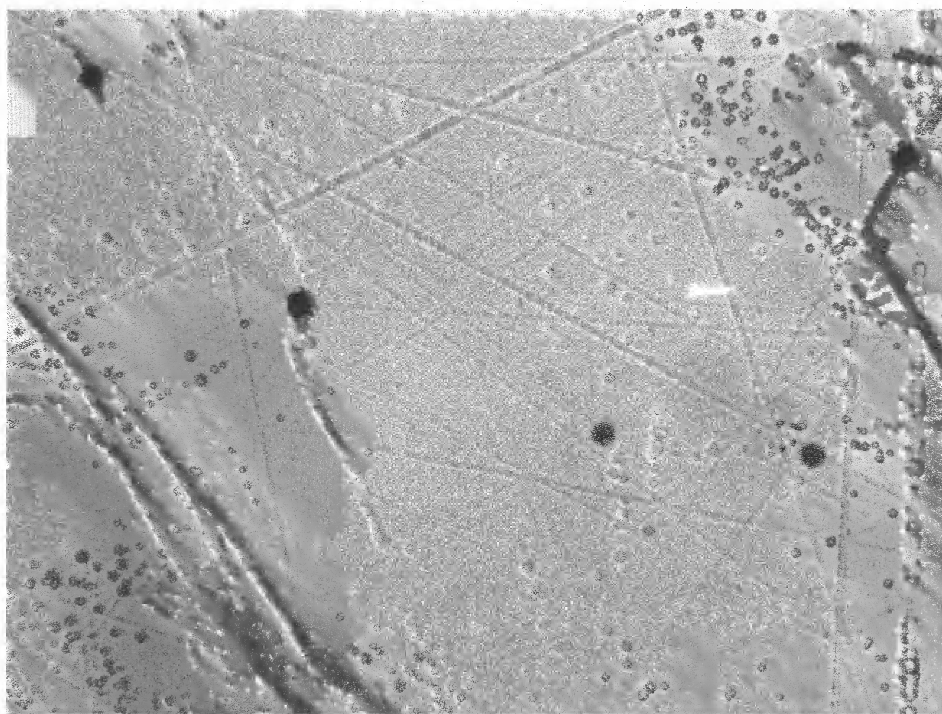

Figure 4.6 3-minutes KOH etched wafer (6H-SiC, $N^+ > 10^{17} cm^{-3}$).

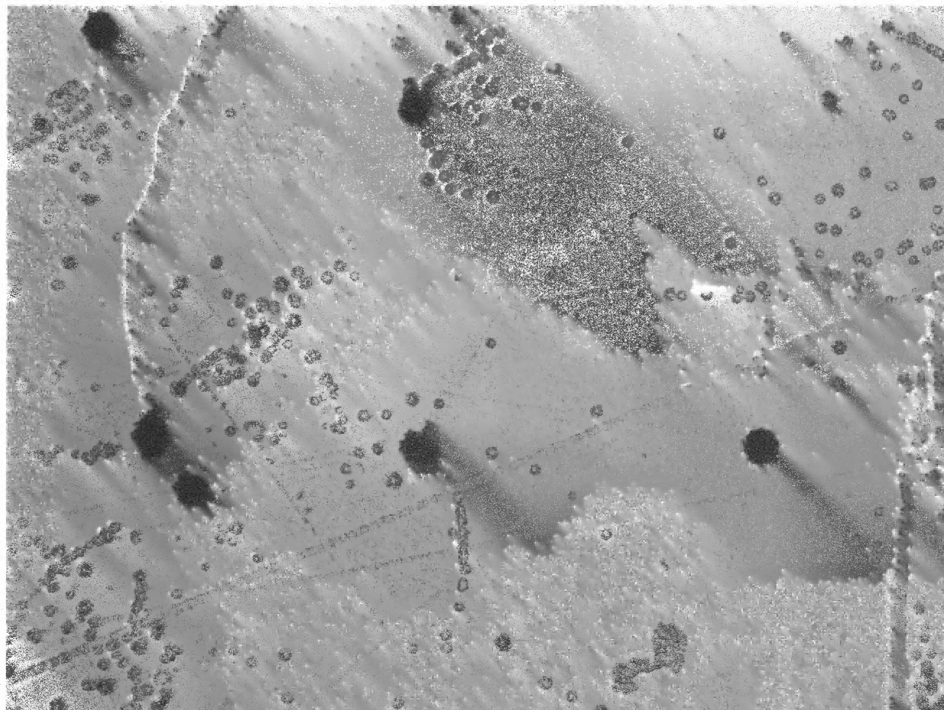

Figure 4.7 5-minutes KOH etched wafer (6H-SiC, $N^+ > 10^{17} cm^{-3}$).

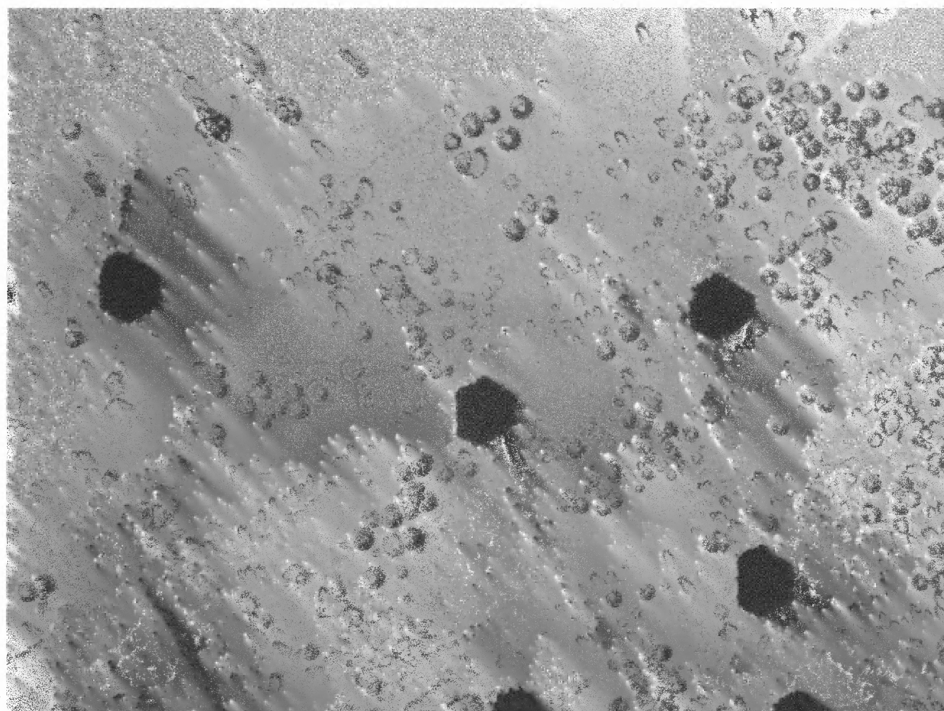

Figure 4.8 10-minutes KOH etched wafer (6H-SiC, $N^+ > 10^{17} cm^{-3}$).

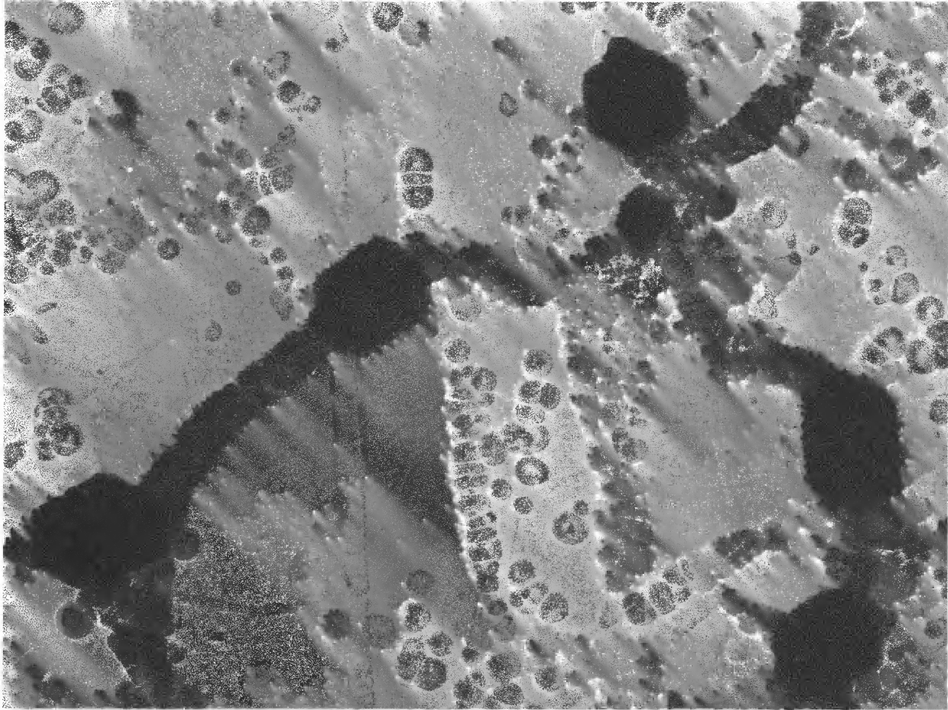

Figure 4.9 15 minutes KOH etched wafer (6H-SiC, $N^{+} > 10^{17} cm^{-3}$).

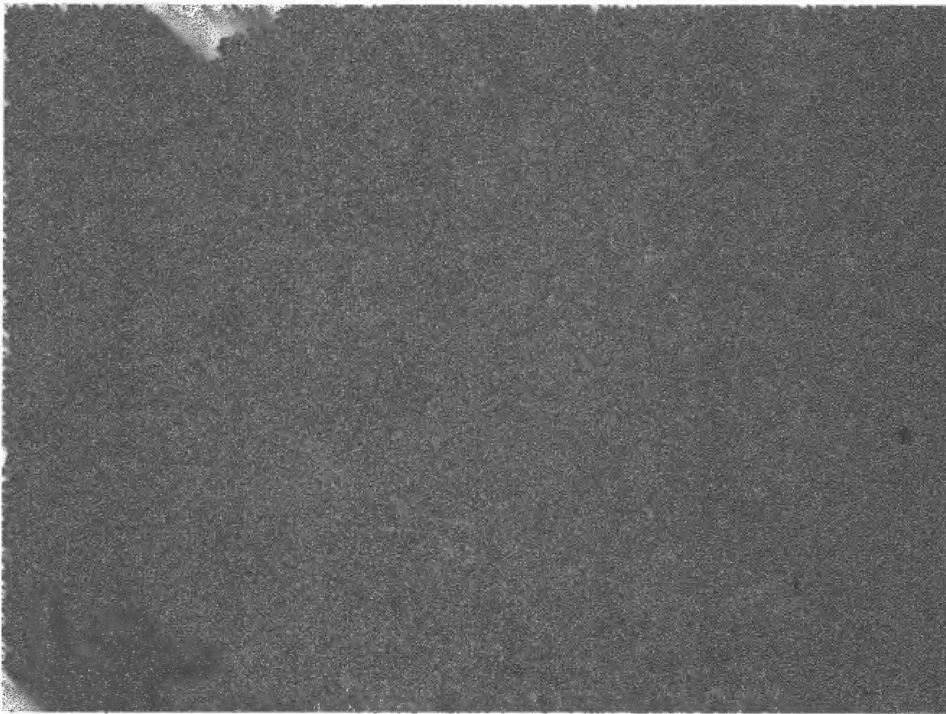

Figure 4.10 1-minute KOH etched wafer (6H-SiC, Semi-Insulating).

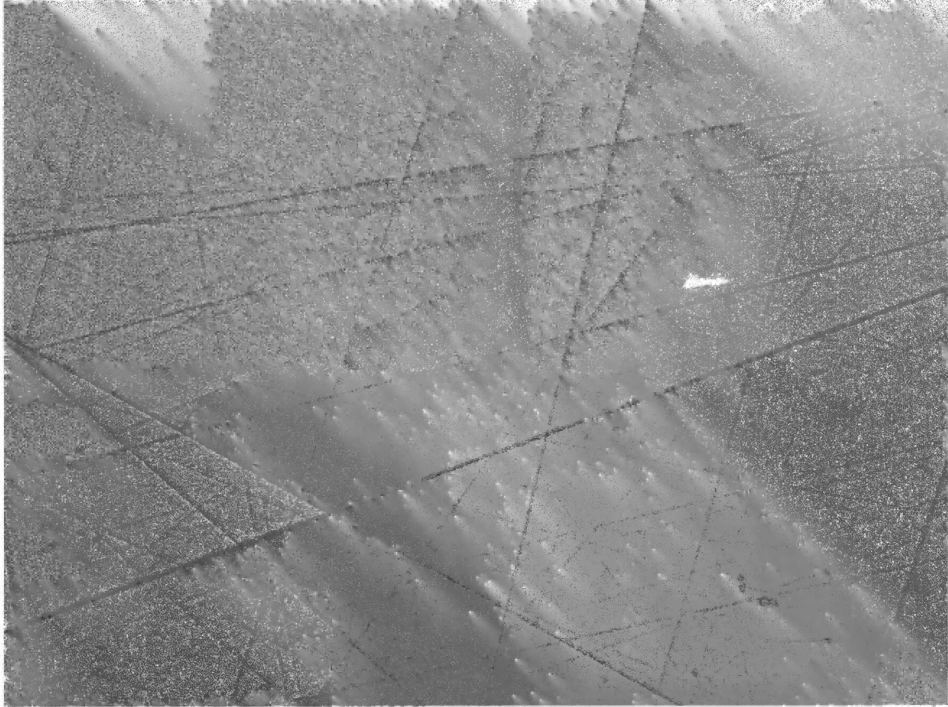

Figure 4.11 5-minutes KOH etched wafer (6H-SiC, Semi-Insulating).

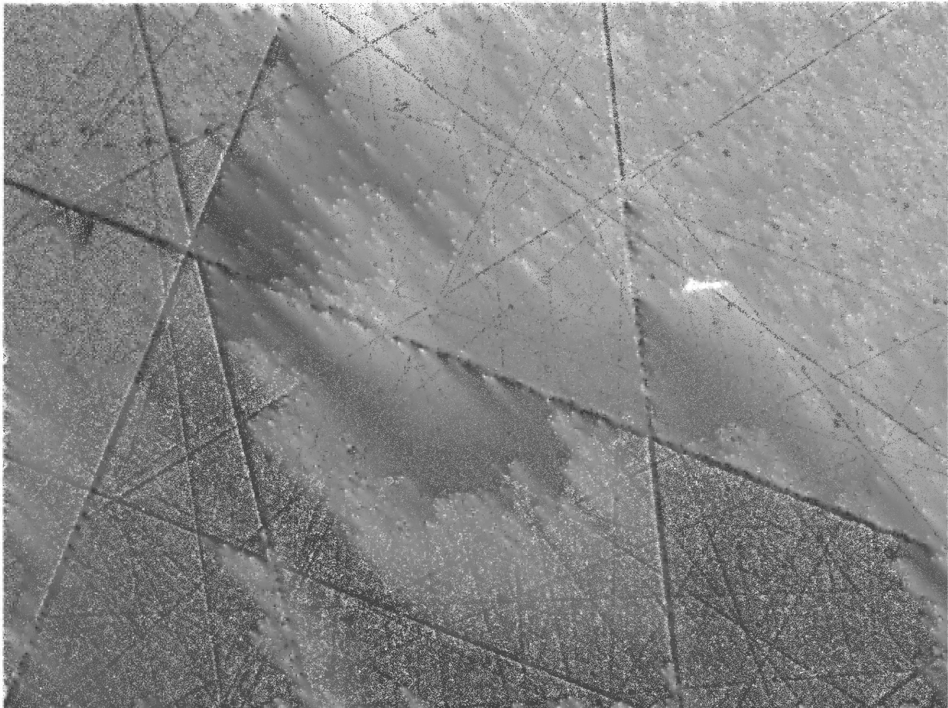

Figure 4.12 10-minutes KOH etched wafer (6H-SiC, Semi-Insulating).

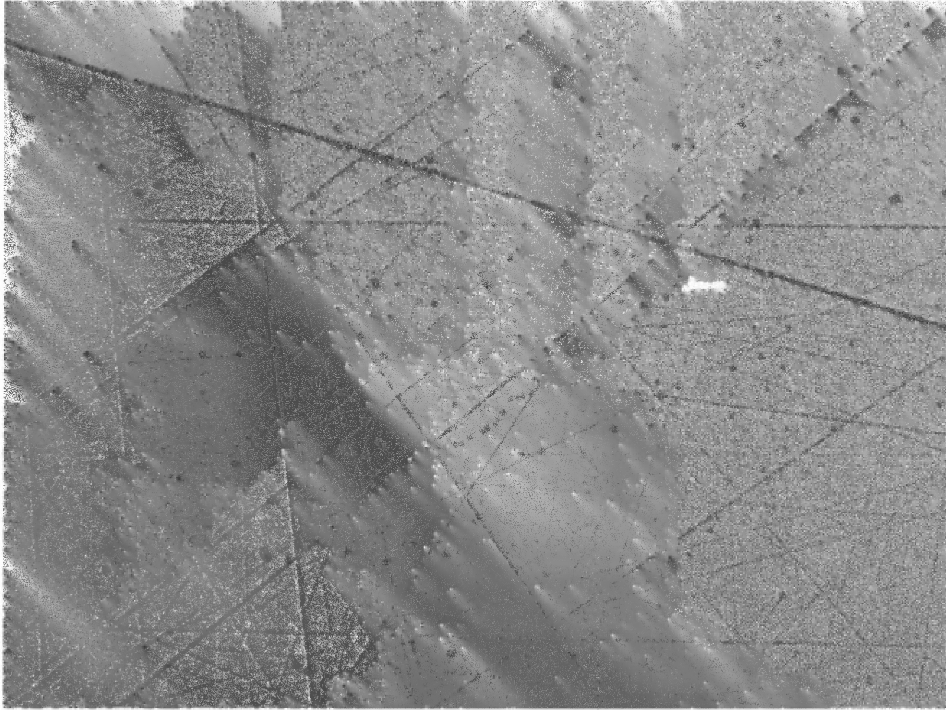

Figure 4.13 15-minutes KOH etched wafer (6H-SiC, Semi-Insulating).

A comparative KOH etch study was performed on silicon carbide and sapphire wafers. Figure 4.14 shows the time dependent etch rate of SiC, as-sawn sapphire, and lapped sapphire. Note that the etch rate of SiC and sapphire are different even for similar as-sawn surfaces on both materials. There is a slight difference between the etch rates of the as-sawn and lapped sapphire surfaces. The lap process leaves approximately 10 μm damage in the material, which is better than the damage of the as-sawn material. It is interesting to note that for SiC and sapphire curves, there is a point of inflection at around the same time. However, the etch rate of sapphire reduces significantly once the damage has been etched. The quasi-horizontal portion of the curves for the sapphire wafers show that the etch rate reduces significantly to several hundredths of microns per minute. The

same is not true for SiC as the etch rate remains at 2 μm/min. The difference in SiC and sapphire etch rates is equal in the duration of the experiment, however the SiC etch rate curve should approach that of sapphire etch after a long time.

Figure 4.15 shows the etch rate versus the depth of material removed. A set of double side polished sapphire wafers is included in the graph. The etch rates of the double side polished wafers are less than that of the as-sawn and lapped sapphire wafers. Also notice that the damage removal on double side is faster because there is less damage. Finally observe the SiC rates and material removal. Figure 4.14 and 4.15 show that in KOH, SiC etches faster and undergoes higher material removal than sapphire. However, the SiC wafers used in the experiment may have a high defect density that may lead to significantly faster etch rates.

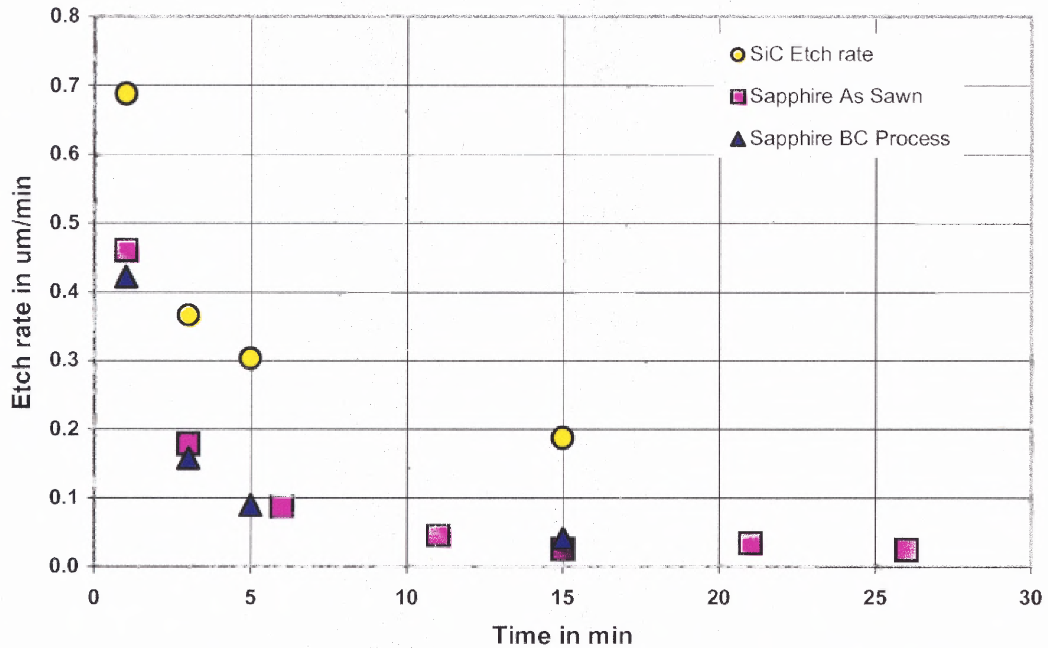

Figure 4.14 Time dependent KOH etch rate for SiC, as sawn Sapphire and Lapped Sapphire.

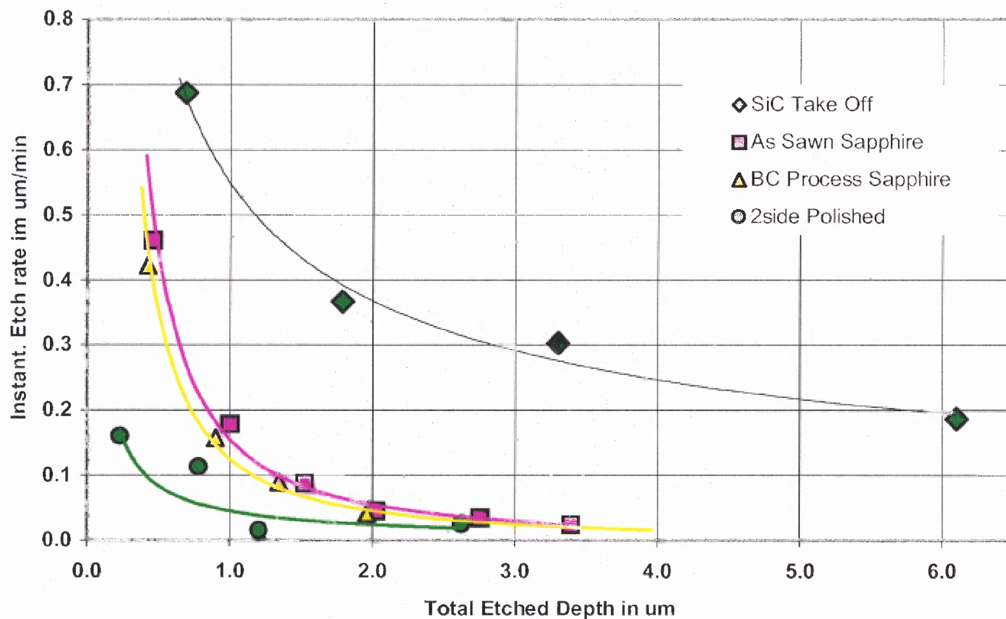

Figure 4.15 Etch rate versus depth of material removed for SiC, as sawn sapphire, lapped sapphire and double side polished sapphire.

CHAPTER 5

OPTICAL CHARACTERIZATION AND MAPPING OF DEFECTS IN SILICON CARBIDE

5.1 Materials and Methods

In order to detect, analyze and map the defects descried in Chapters 3 and 4, an automated optical microscopy system was designed. The automated mapping system consists of an optical reflection microscope with a laser auto focus system, a CCD camera with 1024 x 1024 pixel resolution, an automated stage with minimum step increments of 1nm, and a desktop computer. The CCD camera, as well as the automated stage controller is interfaced with the computer. A graphics/programming package called Image Pro Plus is used to interact with the stage controller and the CCD camera.

5.1.1 Leitz Ergolux Optical Microscope

The Leitz Ergolux optical microscope operates in bright and dark field modes. Bright field image is obtained by illuminating the object uniformly by incident light rays directed perpendicular to the sample surface. Light reflected back towards the objective is collected and focused into the eyepiece or camera to form a true color image at magnification up to 2000X. Surfaces that are perpendicular and reflective to the light rays appear bright. Objects, such as pits, scratches, and particles that scatter light, reflect less light back into the objective and appear dark.

In the dark field mode, the microscope works by enhancing contrast of subtle topographical features. An occluding disk is placed in the light path, disrupting the direct vertical illumination as well as the light reflected from the object. Peripheral rays are

reflected at oblique angles to the object plane. The result is bright reflectance only from ridges, pits, scratches, and particles. Reflective features that normally appear bright in bright field illumination are completely black in dark field illumination.

Closed core dislocation etch pits, scratches, cracks and surface particles will appear as black features in bright field and bright features in dark field. On the other hand, hollow core micropipes, do not reflect light back in both cases because the light stays trapped in the tunnel shaped hole. Therefore, micropipes will remain black features whether viewed in bright field or dark field mode.

However, if the sample has an off-axis orientation, there will be a small amount of light reflected from the hollow core, which makes micropipes appear like screw dislocations in dark field mode. A solution is to use a combination of imaging filters and higher magnification, which will enable considerable contrast between micropipes and dislocations.

5.1.2 Image Analysis Using ImagePro Plus 4.0

Image analysis software packages contain various applications that allow processing and analysis of images, which enable delineation and counting of interesting features. Mathematical morphology makes up a branch of image analysis that is useful for processing defect features. These methods are based on mathematical notations that utilize set operations. In this thesis several morphological operations are addressed with reference to binary images (black and white images), however they can also be used for gray-scale and RGB color images.

5.1.2.1 Thresholding. The delineation of elements of an image is a problem that can be solved by different parameters, such as the shape, the size and the intensity. The latter two techniques require a preliminary step that separates the objects of interest from the remaining image. The simplest way to achieve this separation is by utilizing the individual pixel values through thresholding. Figure 5.1 shows an image that has its features separated through intensity thresholding, and also the brightness histogram that is used to set the thresholding level. Through thresholding one can separate the defects from the background noise (see Figure 5.1 - b).

One simple way of thresholding is to select a range of brightness values in the original image, which selects the pixels within this range and assigns them as the foreground, whilst all other pixels are assigned as the background. If we have a binary image with the '1' and '0' representing the foreground and the background respectively then we can express the thresholding as $b(x, y) = (h(x, y) > T)$, where T is the threshold brightness value. For example Figure 5.1(a) shows a grey scale optical microscopy image of a SiC wafer. The image shows dislocations and micropipes, common defects seen in SiC. Additionally it shows line scratches that were as a result of mechanical polishing of the wafer. Notice that the scratches and the background are lighter in contrast than the defects. Since we are interested in observing defects, we can select a brightness level, which will assign any pixel with light intensity above the threshold level to the white background, and the remaining pixels to the foreground (Figure 5.1(b)). Figure 5.1(c) shows the brightness histogram where the threshold level is set for pixel designation to background or foreground.

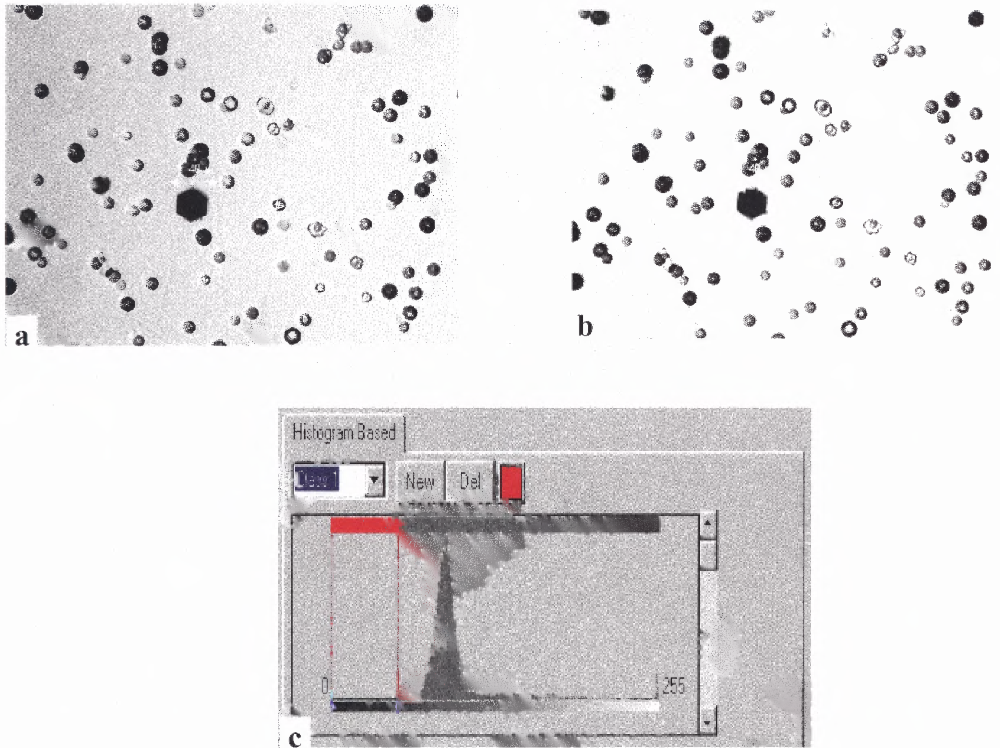

Figure 5.1 A grey scale image of a section of a SiC wafer **(a)** with its binary image produced by changing the threshold values used to select pixels **(b)** through its brightness histogram **(c)**.

5.1.2.2 Eroding. Other operations of image processing adding or removing neighboring pixels from the binary image according to certain rules that based on the pattern of neighboring pixels (Russ 460). Two basic operations commonly used in binary image processing are erosion (removing) and dilation (adding). These processes utilize a mask that is used to evaluate the actual image values. One of the pixels in the mask is a reference point, which is usually, but not always the center pixel of the mask. The reference point is placed at each pixel in the image. Image pixels around the reference point are changed (or not) depending on their evaluation by comparing with the pixels of the mask.

If one considers a pixel of the image to be *p*, *f* to be the image value at this pixel, and *M(p)* to be the value of the mask at *p*, then the general morphology expression is *f(p)=g(p, M(p))*, where *g* is some function of the image value at p and *M(p)*. The values of the functions are 0 or 1 for the binary case. The function *g* will be either *min* or *max*. Min function value is 0 when one or both values (of the image and the mask) are 0, and 1 when both values are 1. Max function is 1 when one or both of the values are 1 and 0 when both are 0.

The erosion operation can be expressed as *f(p)=min(p, M(p))*, an example of which is shown in Figure 5.2. The mask in this case is a square 3 x 3 pixel matrix with the center pixel being a reference point. The mask elements are pixels with values '0' or '1'. The mask is moved over the original image (left), and wherever a '0' appears within the mask, the value of the new image pixel at the reference point is set to zero. If all the image pixels overlapped by the mask have values of '1s' then the reference point in the new image is set to one (right).

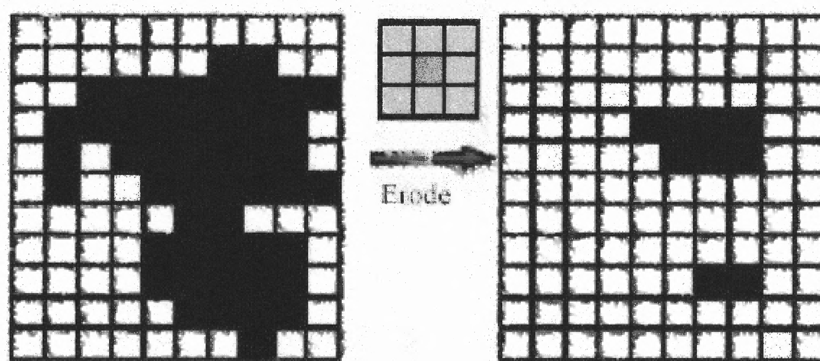

Figure 5.2 Image processing showing the erode operation. [39].

5.1.2.3 Dilating. The dilation operation is the opposite of the erosion process. The mathematical function representing this operation is $f(p)=max(p, M(p))$. The mask in Figure 5.3 is a square 3 x 3 pixel matrix with the center pixel as reference point. The mask is moved over the original image (left), and wherever a '1' appears within the mask, the value of the new image pixel at the reference point is set to one. If the mask element is full of '0s' then the reference point in the new image is set to zero (right).

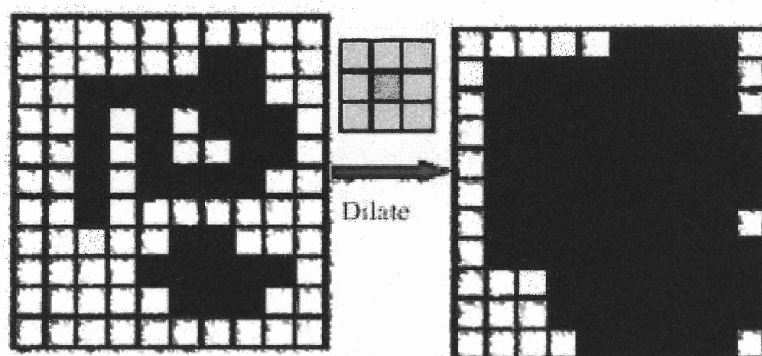

Figure 5.3 Image processing showing the dilate operation [39].

5.1.2.4 Opening and Closing. A combination of the eroding and dilating operations forms popular image processing techniques known as 'opening' and 'closing'. First eroding, then dilating, an image is known as opening, which refers to the ability of this combined operation to open up spaces between objects that are just touching. It is commonly used to remove pixel noise from binary images. The other combination of first dilating, then eroding, is known as closing, because of its ability to close up gaps, or breaks in features. Figure 5.4 shows the open and close operations performed on the two images. Observe how the open operation separates touching pixels and the closing operations joins together nearby pixels.

These operations are important when applying image analysis to microscopic images showing SiC defects. They enable the delineation of different defects like micropipes, basal plane dislocations, screw thread dislocations, and screw edge dislocations.

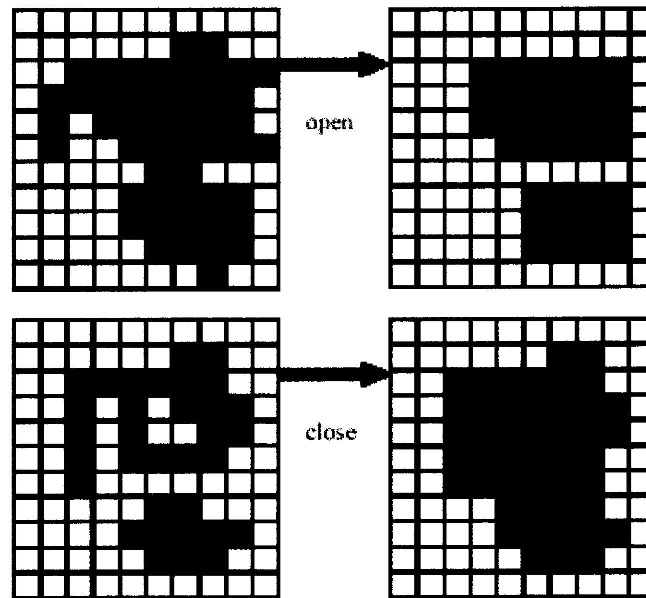

Figure 5.4 Image processing showing opening and closing operations [39].

5.1.3 Wafer Mapping Algorithm

The mapping algorithm was designed as shown in Figure 5.5. The algorithm assumes a wafer of any diameter with two flats ground in. An inner circle represents a boundary of the exclusion zone, which is typically 2mm (SEMI standard) from the wafer edge. The wafer is separated into tiny squares (tiles), which represent image frames that differ in size depending on the microscope lens magnification utilized. Each image frame is

indexed according to the frame position. The scan origin has an index (0,0) and is to the bottom right edge of the wafer as shown in Figure 5.5.

Figure 5.5 shows the schematic of the mapping system. The wafer is oriented on a fixture by its major and minor flats. This enables measurement repeatability as the wafer can be replaced to the same position. For wafers without flats, the orientation is difficult to maintain and slight misalignment will be inevitable. The user specifies the wafer diameter (x, y offset), and the scan diameter. Only tiles completely inside the scan area will be processed as image frames for defects scans. Tiles that lie outside the scan area will be ignored.

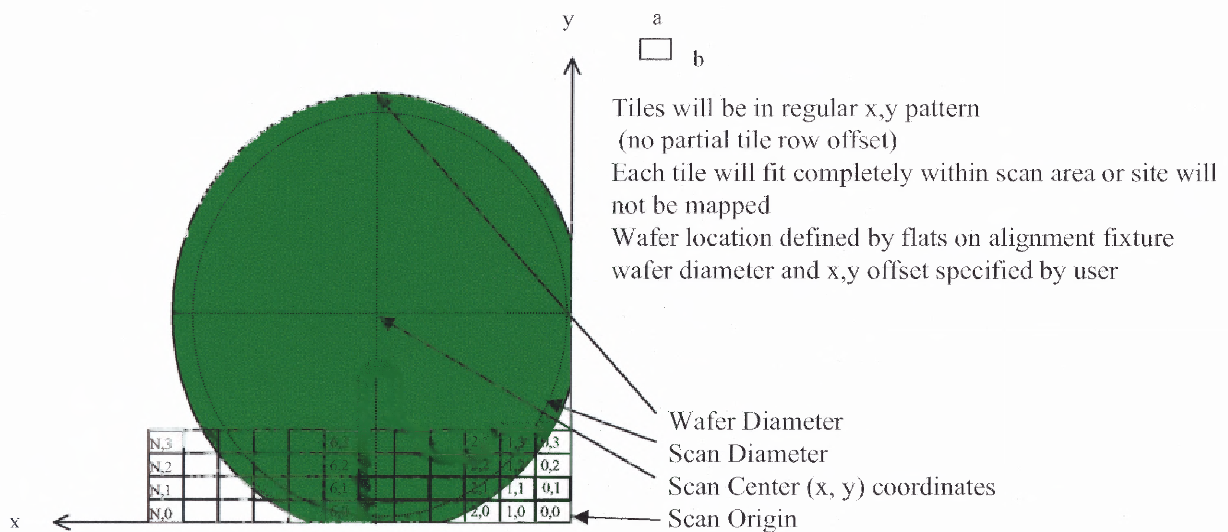

Figure 5.5 Schematic for wafer mapping program.

The automated stage moves first vertically in rows, then at the end of a row it moves horizontally by a column, and then moves in the opposite direction on the next row. Figure 5.6 shows the direction of movement of the automated stage.

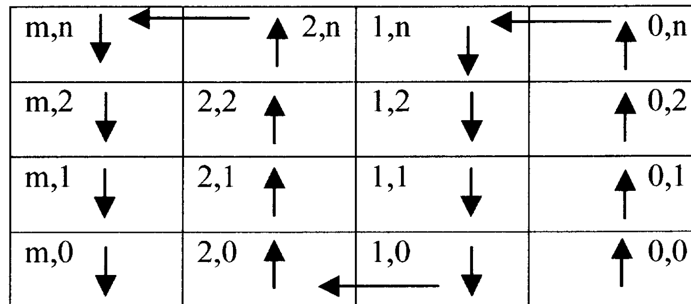

Figure 5.6 Automated stage scanning movement.

5.1.4 Image Analysis of Defects in Heavily Doped 6H-SiC

Etched wafers of various characteristics were studied to develop effective methods of defect image analysis. The fastest and easiest distinction of various defects was made utilizing the contrast (brightness level) of the etch features. Etched micropipe pits appear hexagonal independent of the wafer doping level, whereas dislocation pits are round in heavily doped N^+ SiC wafers, and are hexagonal in lightly doped SiC samples. As a result of their nature, micropipes do not reflect much light and appear to be darker than other defects.

In heavily doped N^+ samples, discrimination of dislocations and micropipes was easy to achieve. An image of a section of the wafer is acquired under bright field microscopic setting. The acquired image is eroded to eliminate or minimize background noise and, uninteresting defects. This enables tagging of only micropipe features. The threshold level is set constant across the wafer surface, and then the software is

programmed to count the features (micropipes). Figure 5.7 shows the result of a typical image analysis process for micropipes in a section of a heavily doped 6H-SiC wafer.

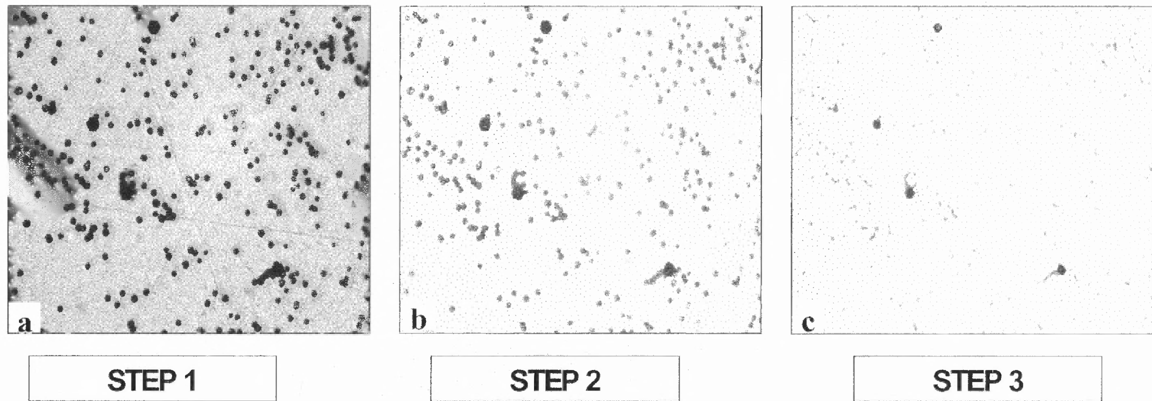

Figure 5.7 An image frame of a 4H-SiC wafer with 10X magnification **(a)** with the same image taken at a higher exposure **(b)** and the result of erosion on the image **(c)** leaving micropipes visible for counting.

The following are the steps for bright field image analysis of micropipes and dislocation, which is a technique used for heavily doped SiC wafers. The steps describe the images in Figures 5.7 to 5.9.

Step 1: Obtaining a bright field microscopy image with all features on the wafer's surface apparent. This image is not part of the process, but is important for revealing what the process eventually does. The digital camera was set at an exposure time of 32 milli-seconds. The exposure time are chosen as multiples of 8 milli-seconds because that is the shortest exposure time supported by the camera.

Step 2: This is the initial step of the analysis of an area on the wafer. The microscope is slightly defocused and set at a lower level to distinguish surface impurities like dirt from subsurface damage and defects. The digital camera takes the same picture as in Step 1,

but with a longer exposure time. This eliminates the scratches that usually appear on the surface, leaving only micropipes and screw dislocations.

Step 3: A filter is used to erode the image from the previous step. Notice that this filter eliminated round objects like screw dislocations, leaving only micropipes. If needed further erosion can be applied to the image to completely remove all background noise. If that is done then it will be necessary to dilate the image so as to enlarge the micropipes.

Step 4: With the threshold level previously set to discriminate the darkest objects (micropipes), a software tool counts the number of micropipes in the image from the previous steps. Figure 5.8 shows the image of the counted features. Notice that there is a total of four micropipes counted in the image.

Figure 5.8 Image used in Step 4 for counting micropipes with Image-Pro.

Analyzing screw dislocations is easy and faster than micropipes. It only requires only two steps:

Step1: Acquire a bright field microscopic image of the wafer. The image is the same as that shown in Figure 5.7 (a).

Step 2: With the threshold level previously set to discriminate micropipes and dislocations from the background and scratches, the defects are counted using the software tools. When analyzing a wafer for dislocations, there is no need to separate the dislocations from the micropipes. All defects (micropipes and screw dislocations) in the frame are counted. Since the number of micropipes in the frame is known from a separate count, the number of dislocations is calculated simply by subtracting the number of

micropipes from the total number of defects. The picture below shows the second step of the defect count.

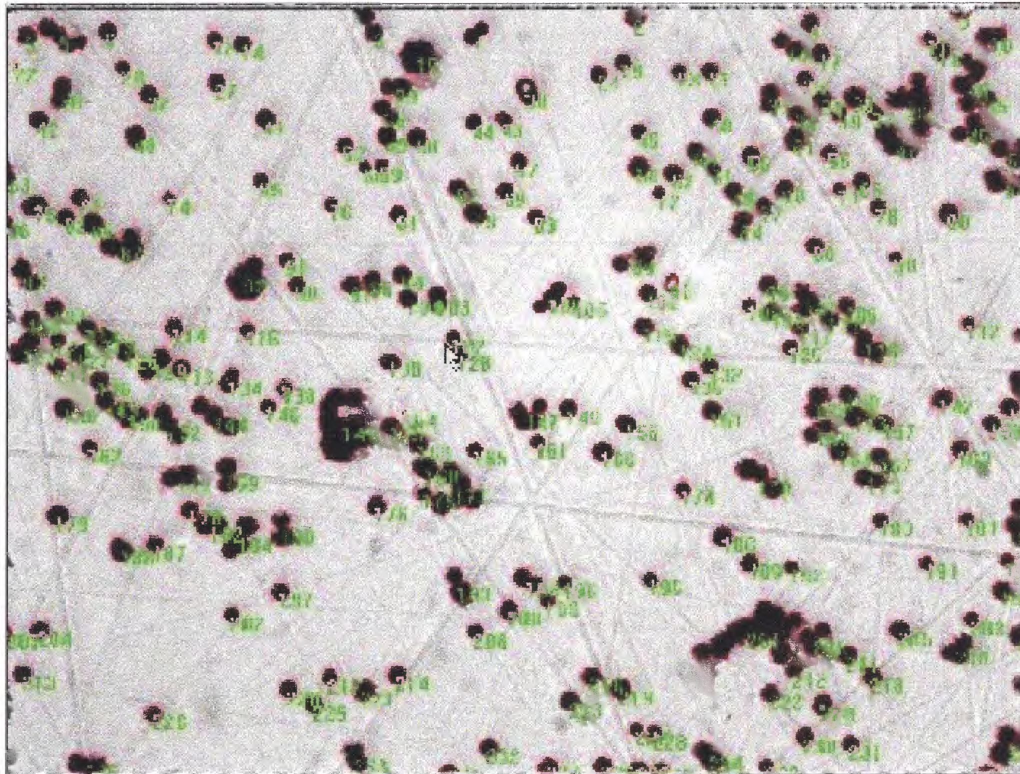

Figure 5.9 An image used for counting dislocations with Image Pro.

5.1.5 Image Analysis of Defects in Lightly Doped and Semi-Insulating 6H-SiC

For lightly doped and compensated N^+ SiC samples, dislocations and micropipes appear as hexagonal features, thus it is very difficult to differentiate them in bright field images. It is not easy to discriminate the micropipes from the dislocations by size because micropipes appear to be only slightly larger than dislocations. However, in dark field microscopic setting, these features are easily discriminated. Figure 5.10 shows a section of a lightly doped 6H-SiC wafer taken with bright and dark field microscopic settings. In the bright field image (Figure 5.10 (a)) all the defects appear to be the same with no

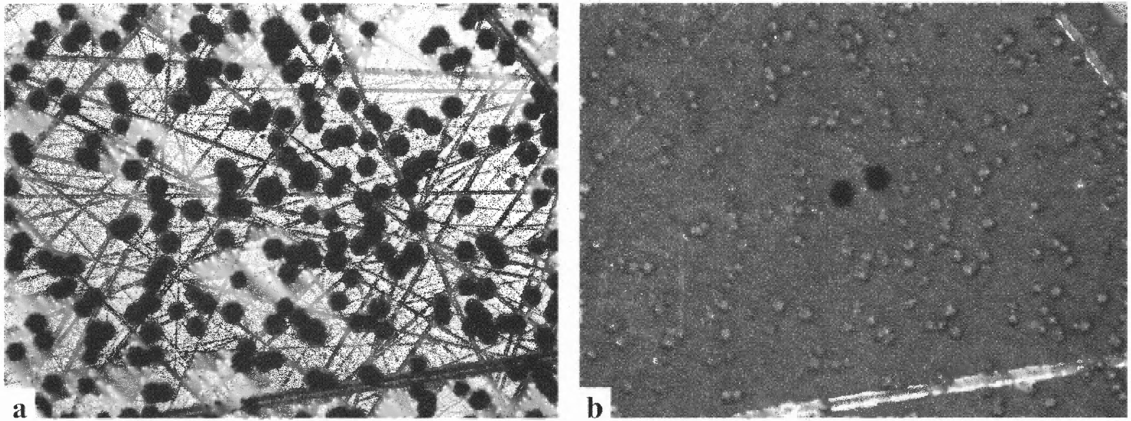

Figure 5.10 Bright field (a) and dark field (b) microscopic images of a section of a lightly doped 6H-SiC wafer.

distinct differences between them. It is very difficult to identify the micropipes from this image. However, in Figure 5.10 (b), which shows of the same wafer acquired under dark field microscopic settings, certain features stand out more that the others. If one considers the fundamentals of dark field microscopy it is understood that features that reflect light in oblique angle appear bright in dark field, and as dark bright field images. However, micropipes do not reflect a lot of light since they are essentially holes. As a result, micropipes will appear dark in both bright and dark field microscopic settings.

The process for counting defects in lightly doped and compensated SiC material is essentially similar to that of the heavily doped SiC described earlier. The only difference is the use of dark field in place of bright field microscopy. Figure 5.11 shows the typical image analysis process for micropipes in a section of lightly doped and compensated 6H-SiC wafers.

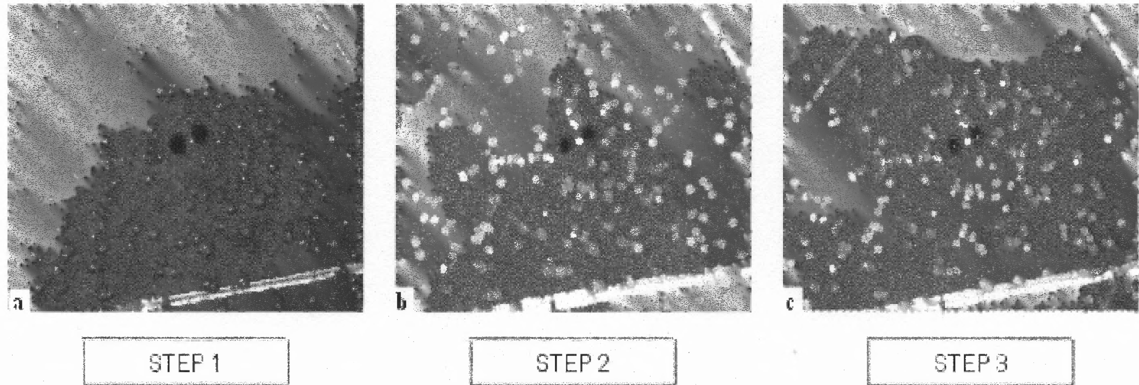

Figure 5.11 A dark field image a section of a 6H-SiC wafer **(a),** with the erosion of the same image **(b),** and the image for counting of visible micropipes **(c)**.

The following are the steps for dark field image analysis of micropipes and dislocations. This is a technique used for lightly doped and compensated SiC wafers where dislocation and micropipe feature are hexagonal. The steps are illustrated describe the images in Figure 5.11.

Step 1: Acquire a digital image of the wafer with the microscope set in the dark field mode.

Step 2: Erode the image so that bright features become blurred and dark features become prominent. Notice that dislocations are unrecognizable.

Step 3: Set the threshold level so that the darkest features (micropipes) are discriminated from the other features. Count the number of micropipes in the image from the previous steps. Figure 5.11 (c) shows the image with the counted features. Notice that there is a total of two micropipes counted in the image.

The dislocations in this case are brightly lit features in the background. Thus setting the threshold level at a different brightness level for brighter objects will allow counting of the dislocation.

5.1.6 Image Analysis of Defects in Off-Axis SiC Crystals

Materials that are oriented 3° or 8° off-axis present a challenge for characterizing the defects. The problem is that the shape of defects in off-axis material is slightly altered due to the angle at which the wafers are sliced. The greater the off-axis orientation, the greater the impact it will have on the defect shape.

The use of a combination of erosion and dilation of the image known as 'opening', resolves this problem. Figure 5.12 shows the application of this image analysis technique to a dark field microscopic image. The following steps describe the process:

Step 1: A dark field microscopic image is acquired. Figure 15.12 (a) shows a section of a semi-insulating 6H-SiC wafer.

Step 2: The image is eroded so that the brighter features of dislocations and cracks are blurred. Notice in Figure 15.12 (b) that the micropipes are reduced in size such that they are hardly recognizable. Image erosion also results in the separation of features that touch each other.

Step 3: The image is dilated (see Figure 15.12 (c)) to open up dark features such as micropipes and suppress bright ones. Notice that the bright features have been suppressed to the point where they are unrecognizable, and cannot be discriminated. On the other and, the micropipes are the only features that standout in the image.

Step 4: Thresholding the image so that the brightness level of the micropipes enhances their features to facilitate their counting.

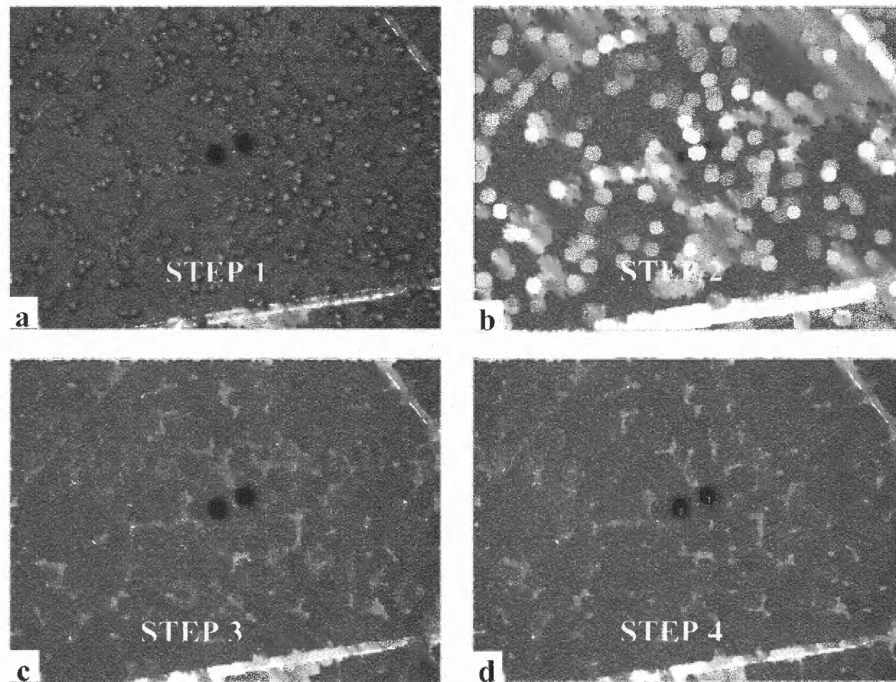

Figure 5.12 Image analysis process for off-axis oriented SiC material where the original image **(a)** is eroded **(b)** and dilated **(c)** after which the remaining micropipe features are counted **(d)**.

This process enables the accurate tagging and counting on off-axis oriented crystals as all other features are suppressed whilst the micropipes are enhanced.

5.1.7 Data Analysis

The data collected in the defect mapping of wafers include the (x, y) coordinate positions, the (x, and y) distances of each frame from the origin, and the dislocation and the micropipe count at each frame. During mapping, the image of a small section of the wafer is acquired, then it is analyzed for defects, and then the image is replaced by the

next frame's acquired image. To save storage space the acquired digital images are not saved.

The data are saved as text (.txt extension) or data (.dat extension) files to a database that is used to generate the final maps. Table 5.1 shows a small portion of the data collection generated from the mapping process of a heavily doped 6H-SiC wafer. Notice that the number of dislocations is much higher than the number of micropipes seen in the wafer.

Table 5.1 Data Collected for Defect Mapping of SiC Wafers

	A(X) X - Coordinate	B(Y) Y - Coordinate	C(Y) X - Distance (mm)	D(Y) Y - Distance (mm)	E(Y) # Dislocations	F(Y) # Micropipes
1	2	33	1.644	20.4996	119	0
2	2	34	1.644	21.1208	113	0
3	2	35	1.644	21.742	230	21
4	2	36	1.644	22.3632	194	6
5	2	37	1.644	22.9844	197	0
6	2	38	1.644	23.6056	223	1
7	2	39	1.644	24.2268	397	2
8	2	40	1.644	24.848	327	0
9	2	41	1.644	25.4692	316	0
10	3	47	2.466	29.1964	272	0
11	3	46	2.466	28.5752	283	0
12	3	45	2.466	27.954	246	0
13	3	44	2.466	27.3328	294	0
14	3	43	2.466	26.7116	297	0
15	3	42	2.466	26.0904	211	0
16	3	41	2.466	25.4692	285	0
17	3	40	2.466	24.848	182	0
18	3	39	2.466	24.2268	269	0
19	3	38	2.466	23.6056	141	0

Wafers are routinely scanned using 100X magnification. However the system is setup to map wafers using 50X, and 200X magnifications. These magnifications have shown to be appropriate for discriminating different elements in an image. Using a higher magnification would be inefficient, as it would take too much time to map a wafer. The quickest scans are achieved using the 50X magnification, however, this scale works best

when analyzing heavily doped SiC material where only micropipes and TDC's are hexagonal features that are easily tagged.

An image frame is 0.5 mm^2 of area when using the 100X magnification. A total of 3600 image frames are generated when mapping a 2-inch wafer with a 2mm exclusion area. Hence, approximately 89% of the whole wafer is mapped. Most of the additional 11% of the wafer that is not mapped belongs to the exclusion zone of the wafer. The maps are representative of majority of the surface area of the wafers, which will be used for devices.

It takes 3.5 to 4.5 hours to completely map a two-inch wafer using 100X magnification. The time depends on the type of analysis performed per image frame. If one considers that there are 3600 image frames analyzed per 2-inch wafer, then any additional analysis that is completed in 1-second per image frame will add 1-hour to the overall scanning time. By changing the magnification used one can change the speed at which the scan can be performed. It can be as short as 1-hour with a 50X magnification, or as long as 16-hours for a 200X magnification.

The data collected during mapping is binned into several rows. Table 5.2 shows the data set in Table 5.1 that has been separated into bins. The bins show the distance of the frames. The data are sorted depending of the number of micropipes held per image frame. The first column shows the x-distance for the frames. The second column shows the y-distance of image frames with no micropipes in them, the third column is for image frames with one micropipe and so on, until the seventh column, which is the y-distance for image frames that have more than five micropipes.

Table 5.2 Bins Showing the Distribution of Number of Micropipes per Frame

X-Axis (mm)	Zero	One	Two	Three	Four	Five	> Five
1.644	20.4996						
1.644	21.1208						
1.644							21.742
1.644							22.3632
1.644	22.9844						
1.644		23.6056					
1.644			24.2268				
1.644	24.848						
1.644	25.4692						
2.466	29.1964						
2.466	28.5752						
2.466	27.954						
2.466	27.3328						
2.466	26.7116						
2.466	26.0904						
2.466	25.4692						
2.466	24.848						
2.466	24.2268						
2.466	23.6056						
2.466	22.9844						
2.466	22.3632						
2.466							21.742

The binned data can be converted into spatial maps that are very accurate representations of the wafer from the data in Table 5.2. To generate a map, the first column is set as the x-axis and the remaining columns are set as y-axis. The result is a scatter map that represents each image frame's distance relative to the starting point of the scan (the origin).

Figure 5.13 is a micropipe density distribution map of the data shown in Table 5.2. Each square block represents an image frame that is 0.5 mm^2 in area. The x- and y-coordinates represent distance on the wafer. This allows one to better identify areas of very high defect densities on wafers. Notice that in this particular case the average micropipe density is $29cm^{-2}$, which is well below the expected average of $100cm^{-2}$.

Figure 5.14 shows the percentage of frames occupied by various numbers of micropipes. Most frames have no micropipes (91.3%), and a very small number of frames have one to five micropipes (8.7%). To calculate the density of micropipes per frame, divide the number of micropipes by the area of the frame. For example, a frame with one micropipe is has a density of 197 cm^{-2}.

Figure 5.15 shows a dislocation density distribution map. A separate set of bins has been created for dislocations because of their relatively large number in SiC. For the dislocation map, 23 bins were created. The bins range from 0 to 500 with intervals of 25. The average dislocation density is 2×10^4 cm^{-2}. Notice that the highest dislocation densities appear towards the edges of the wafer. When comparing these areas to regions of high micropipe density in Figure 5.15, one can observe a correlation of these areas with regions of high dislocation densities. Figure 5.16 shows the percentage of frames occupied by various quantities of dislocations in ranges. Most frames have between 100 and 125 dislocations, which have equivalent calculated densities between 2×10^4 and 2.5×10^4 cm^{-2}.

Micropipe Density Distribution Map
II-VI Wafer, 6H-SiC, N $^{+}$, Heavily Doped

MPD Per Frame
Zero
One
Two
Three
Four
Five
> Five

Average MPD ~ 29 cm $^{-2}$
Average DD ~ 2E4 ^{2}
Frame Area ~ 5E-3 cm ^{2}

Major Flat
Minor Flat
Distance (mm)
Distance (mm)

Figure 5.13 Micropipe density distribution map of a 6H-SiC, N^{+}, wafer grown at *II-VI Incorporated.* The average micropipe density (MPD) is 29cm^{-2} and the average dislocation density (DD) is 2 x 10^{4} cm^{-2}.

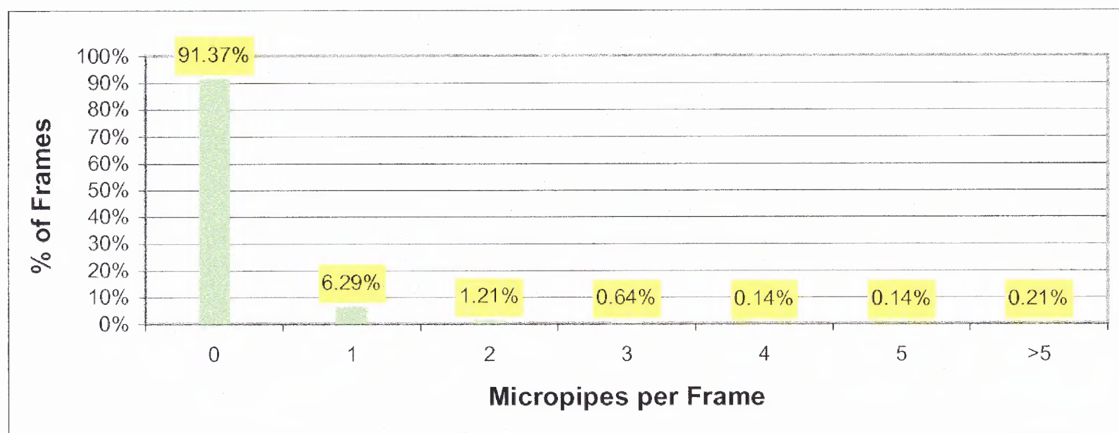

Figure 5.14 A graph showing the frequency of the number of micropipes per frame as a result of the map above.

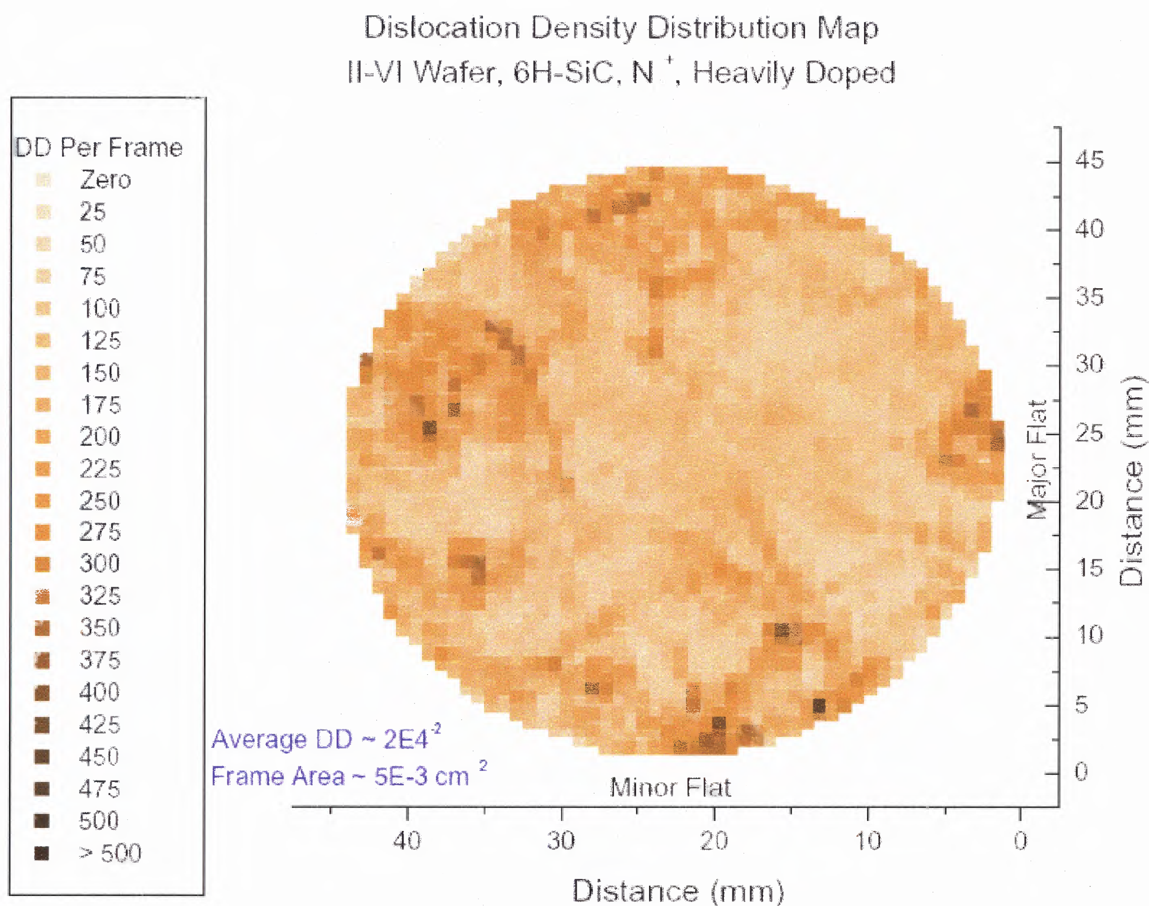

Figure 5.15 Dislocation density distribution map of a 6H-SiC, N^+, wafer grown at *II-VI Incorporated.* The average micropipe density (MPD) is $29 cm^{-2}$ and the average dislocation density (DD) is 2×10^4 cm^{-2}.

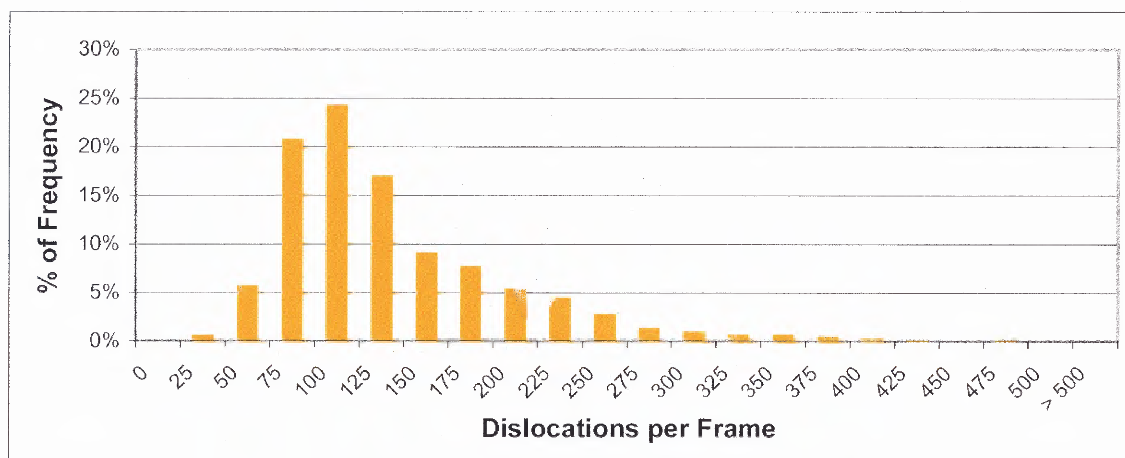

Figure 5.16 A graph showing the frequency of the number of dislocations per frame as a result of the map above.

5.2 Results and Discussion

The features tagged as micropipes in heavily doped SiC material are unquestionably super screw dislocations because they are the only hexagonal features in that example. Additionally when the microscope is defocused, the round features disappear abruptly whilst the hexagonal features can be identified continuously down to focusing on the opposite face of the crystal. However the problem in compensated and lightly doped material is pronounced because screw dislocations are also hexagonal. Hence the question of whether these features in such SiC material are truly micropipes or not arises since they cannot be distinguished from other defects, such as TDCs or just screw dislocations.

As discussed earlier, a solution to resolving micropipes is with the use of dark field microscopy. Figure 5.17 shows a dark field microscopic image of a lightly doped 6H-SiC wafer with dislocations and one micropipe. The microscope is defocused from the front-side or surface to the backside of the wafer. Clearly the characteristic micropipe tail is seen, as the microscope is progressively defocused. Also note the dislocations in the image abruptly disappear as the microscope is defocused (see Figure 5.17 c, d, e, f, g). This proves that the features are distinguishable using a simple occluding filter that captures the oblique light reflected from dislocations.

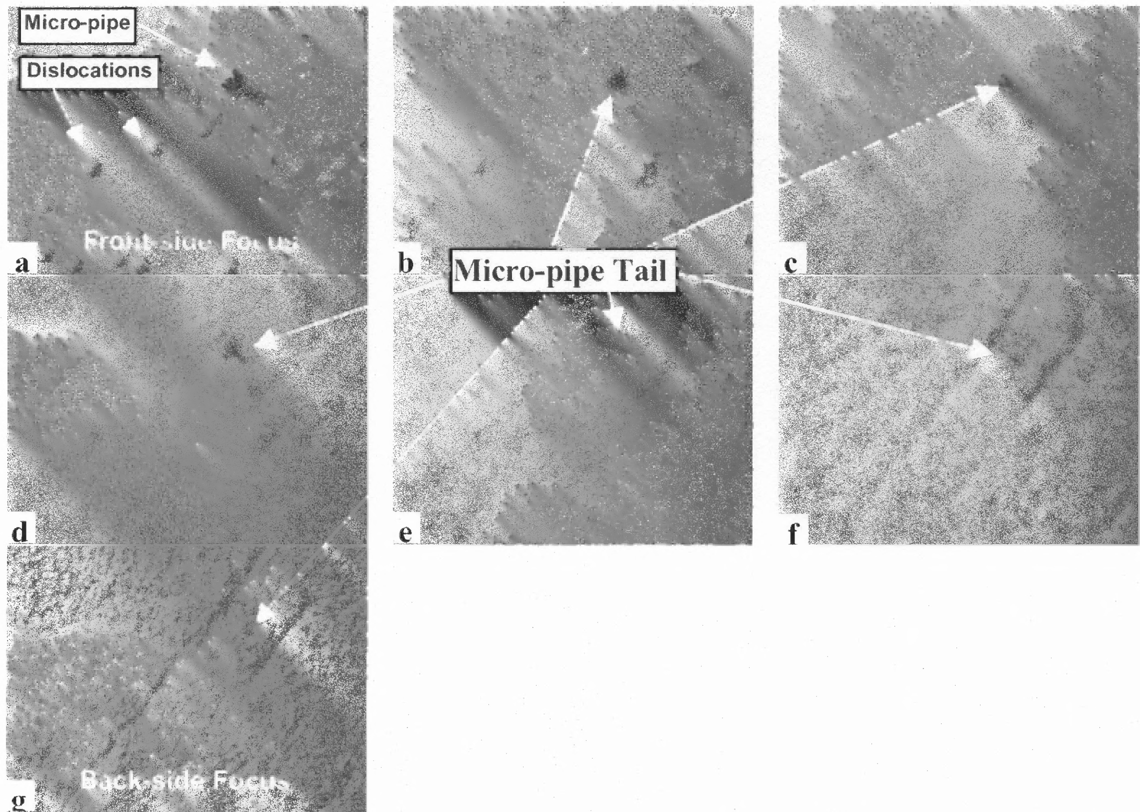

Figure 5. 17 Dark field images of a semi-insulating 6H-SiC as the microscope is defocused from the wafer's front-side (surface) **(a),** following the micropipe's tail **(b, c, d, e, f, g)** until the back-side of the wafer is visible **(g)**.

5.2.1 Measurement Comparison with Synchrotron White Beam X-ray Technique

To test the system's effectiveness and the accuracy of the dark field measurements, a 1.75-inch diameter, compensated 6H-SiC wafer grown by *II-VI Incorporated* was scanned using the automated microscope method in dark field mode and then sent for evaluation with the SWBXT method. Professor Michael Dudley of Stony Brook University of New York performed the SWBXT measurements. The SWBXT method is generally recognized as a very accurate technique for counting defects such as micropipes and dislocations in SiC material. The results from the two tests were very similar.

A micropipe density of 47cm^{-2} was measured using the automated microscope technique in dark field mode. A micropipe density in the range of 45 to 80cm^{-2} was measured using the SWBXT for the same wafer. The range in the results represent counts from two separate enlarged sections of the SWBXT image of the wafer shown in Figure 5.19 (a) and (b). These results validate the technique of qualifying micropipes using dark field microscopy. Two regions of approximately 1.5 x 1.5 cm^2 in similar positions of the wafer were analyzed in the micropipe map of this wafer (Figure 5.20). The results were 42cm^{-2} for region A and 75cm^{-2} for region B. This is a difference of ~6% for results from the two techniques.

A second heavily doped 6H-SiC wafer was measured using both techniques. The wafer was scanned using the bright field feature of the automated microscope system. A micropipe density of 80cm^{-2} was counted for the wafer. The SWBXT measurement revealed a density in the range of 50 to 100cm^{-2}. The range represents measurements made on separate enlarged section of the SWBXT image of the wafer. The relatively results for the two wafers from the two methods suggest the automated microscopic technique is accurate. The SWBXT method serves as a very good calibration tool that can be used to develop a standard.

Figure 5.18 shows the SWBXT image of a compensated 6H-SiC wafer. One advantage of the SWBXT method is the ability to acquire macro as well as micro images. The macro image in Figure 5.18 shows the general topography of the wafer. Observation of areas with problems is quick and easy. The wafer has regions of the center and right that have a relatively low density of low angle grain boundaries. This is indicative of a

very good quality crystal. Observe that on the lower left and around the edges of the crystal reveal a higher density of low angle grain boundaries.

Figure 5.19 (a) and (b) are higher magnification images of regions 'A' and 'B' marked on the wafer's macro image in Figure 5.18. The larger white spots in these images are individual or grouped micropipes. Otherwise the regions are of very good crystal quality. Region 'B' has a higher density of low angle grain boundaries, and a feature that appears to be a TDC in the top right hand corner. Analysis of the two regions reveals the micropipe density of approximately $45cm^{-2} – 80cm^{-2}$. The range represents the average densities of micropipes in regions A and B.

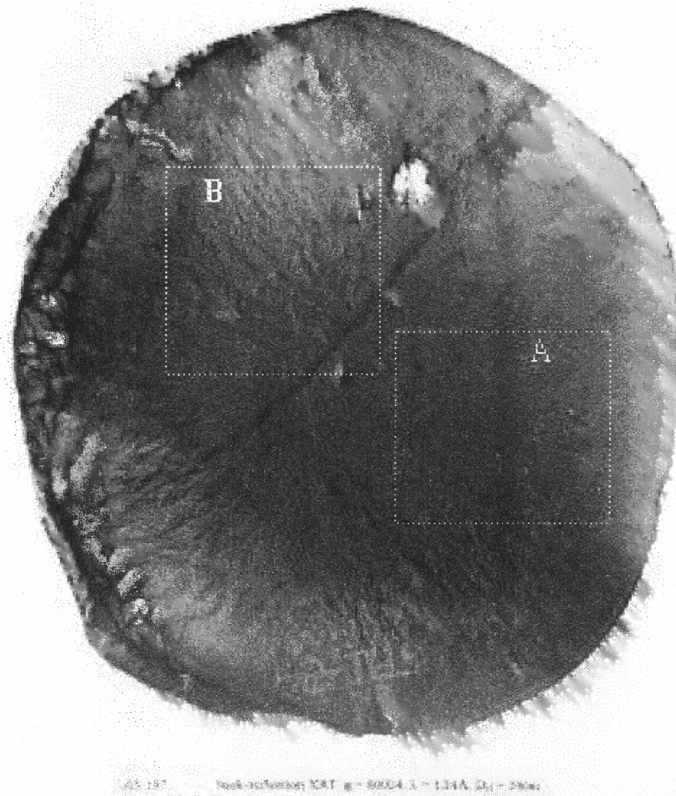

Figure 5.18 SWBXT back-reflection image recorded from compensated 6H-SiC wafer. Measurements made on regions A and B has been expanded in Figure 15.18. Images provided by *II-VI Incorporated, New Jersey.*

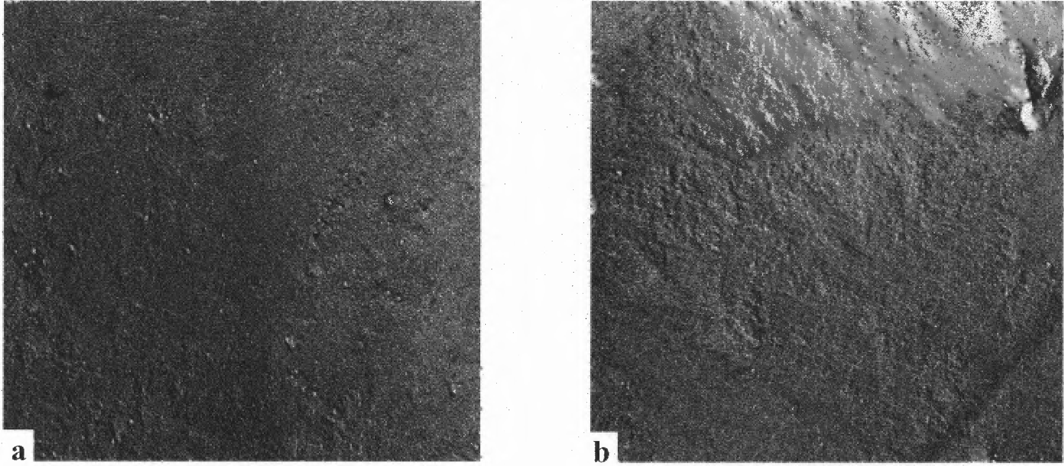

Figure 5.19 Enlargement of region A, with a low density of low angle grain boundaries **(a),** and region B, with a large density of low angle grain boundaries **(b)** from Figure 15.17. The regions are 1.5 x 1.6 cm^2 in area.

The SiC wafer measured by SWBXT was previously etched and scanned with the automated microscopic method. Figure 5.20 shows the micropipe density distribution map of the whole wafer. Notice that there is a good correlation between the map and the SWBXT image. General characteristics of the various regions in Figure 5.18 can be traced to the map. Notice that the map shows a region of the center and bottom right with very small number of micropipes. This region corresponds to the same regions in Figure 5.18 that have been recognized as having very low density of low angle grain boundaries. Also notice that the edges, top of center and lower left regions have a higher density of micropipes. The SWBXT once again reveals that these regions have a higher density of low angle grain boundaries.

The big white spot at the top of the wafer seen in the SWBXT image (Figure 5.18) corresponds to a high micropipe density region situated in approximately the same position on the map in Figure 5.20.

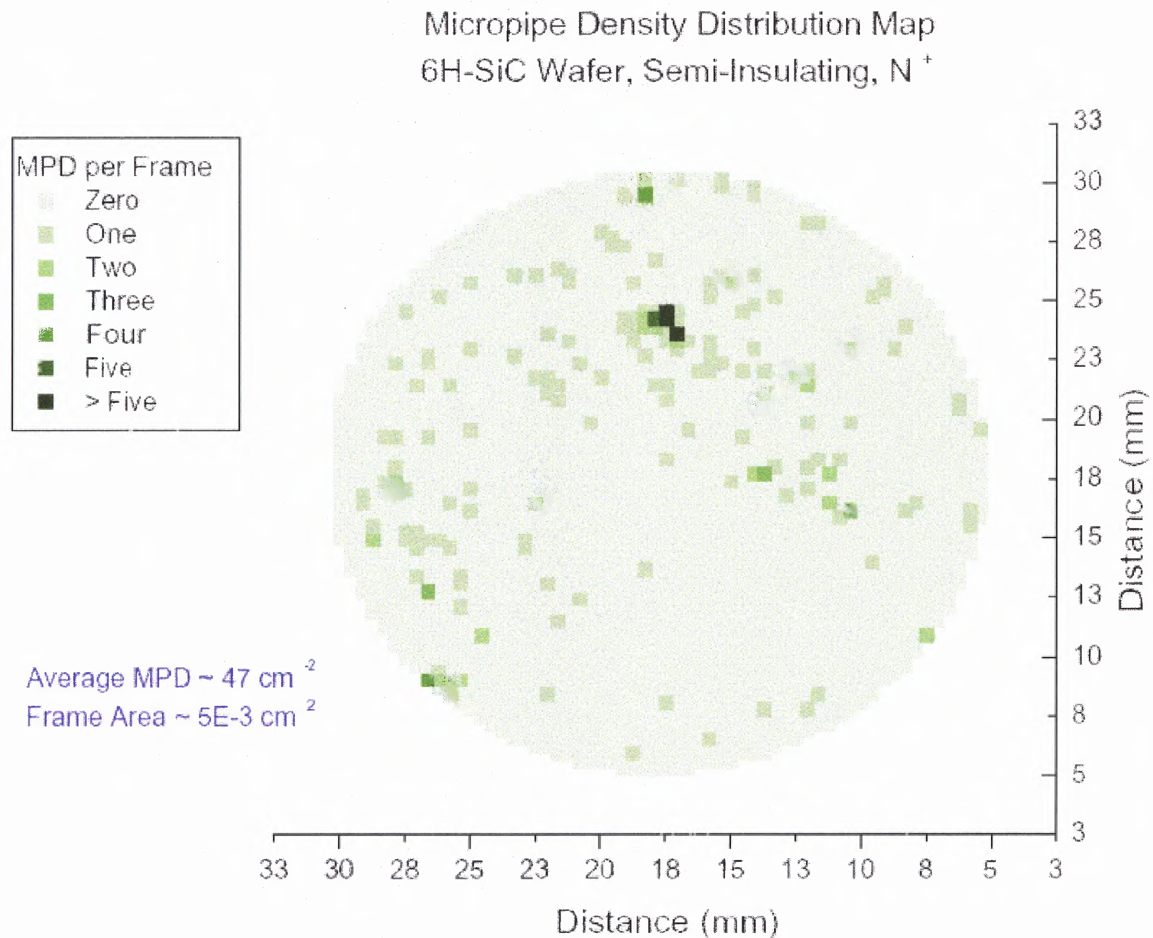

Figure 5.20 Micropipe density distribution map of a 6H-SiC, semi-insulating wafer grown at *II-VI Incorporated.* The map is of the same wafer shown in Figure 5.18 and 5.19. The average micropipe density (MPD) is $47 cm^{-2}$. There are very close similarities with between the SWBXT image and this map of the wafer.

5.2.2 Measurement Repeatability

While standard repeatability tests have not been performed on the automated microscopic counting system, a series of experiments have been performed to measure the repeatability of the system. A test that involved seven wafers was implemented to measure the consistency of micropipe counts measured on the wafers over a series of runs. The wafers were all 6H-SiC, four were heavily doped, and three were undoped. Wafers 1 and 2 were from the same boule. Wafers 3 and 4 were from another boule. Wafers 5 to 7 were all from separate boules.

The wafers were all etched and scanned. Next, they were lapped to remove approximately 60μm from the Si face. This thickness was determined from depth measurements of the micropipes using a Zygo profilometer. Figure 5.21 shows a Zygo measurement of the depth of a micropipe in the c-axis of the crystal (approximately 60μ.m). In principle, the depth measured is the depth of the etch pit of a micropipe. Practically at this depth there would be only micropipes visible on the surface, as all other surface features such as screw dislocations would be removed through polishing. The polish depth of the deepest screw dislocation etch pit was measured to be approximately 30μ.m. Figure 5.22 shows the Zygo plot of the dislocation etch pit (depth ~ 27μ.m).

Therefore after lapping to the depth of 60μ.m, only micropipe defects were visible and other defects such as dislocations had been removed. Scanning system parameters such as the scan settings (light intensity, threshold level, and filter settings) were adjusted for each wafer scan.

Three of the seven wafers used had very poor surfaces. The wafers had extremely high peak to valley height variations (PV ~ 60μm).

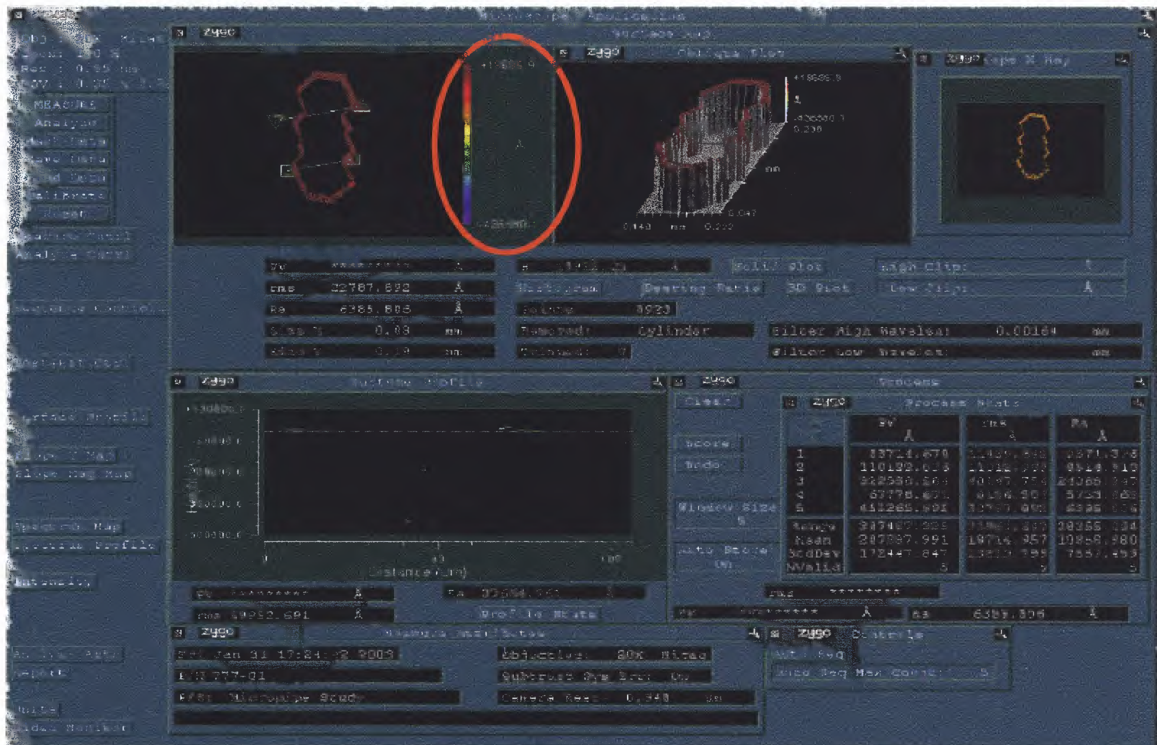

Figure 5.21 Depth measurement of a micropipe etch pit. Measured etch pit depth in the figure is approximately 60μm.

Figure 5.22 Depth measurement of a micropipe etch pit. Measured etch pit depth in the figure is approximately 27μm.

The mechanical polish process performed on these wafers made delineation of micropipes difficult. The laser auto-focus went out of range during the first run due to the high PV values. This led to wrong measurements during runs for all three wafers. These measurements have wafer been excluded from the test because of their unreliability.

The average MPD from the two runs (before and after lapping) revealed a close correlation between the average counts for the four wafers. Figure 5.23 shows a graph of the average micropipe density measured per wafer.

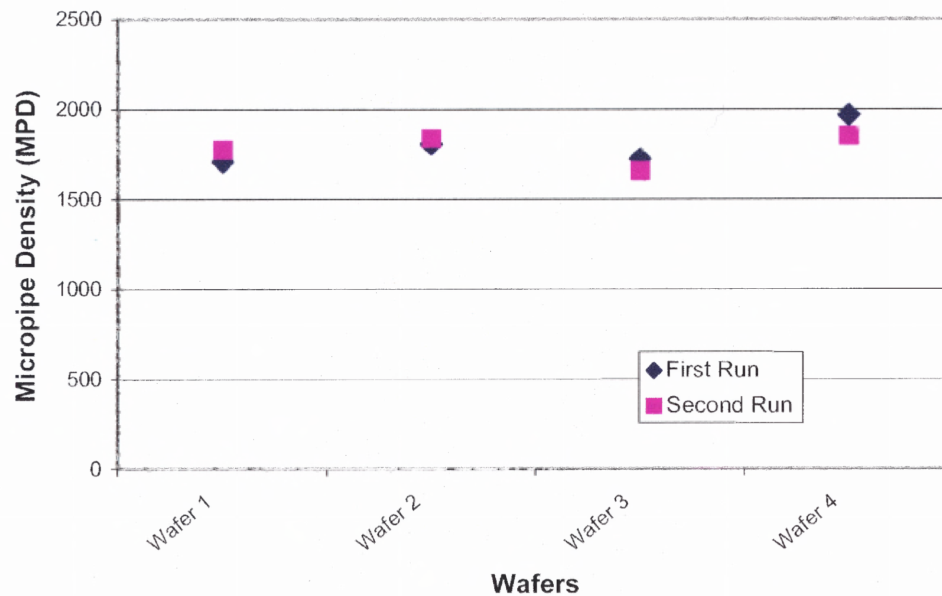

Figure 5.23 Graph showing average micropipe density per wafer. Run 1 was done before and Run 2 after lapping.

As the graph shows, the difference between the two runs in the average micropipe counts is very small; the average variability is approximately 4%. Notice also that the variability from wafer one to wafer two in both runs is very small. The same is observed

for wafers three and four. This result is expected as wafers 1 and 2 are from the same boule, and wafers 3 and 4 are from another boule.

Another experiment was performed to test the repeatability of the equipment. A wafer was mapped twice and the resulting maps were evaluated for similarities or differences. Parameters such as the light intensity, threshold level and filter setting were held constant, but the runs were performed a day apart. Figure 5.24 and 5.25 shows the two maps acquired from the wafer. Notice that the maps are almost identical. The degree of variability is calculated from the average MPD measured (variability ~ 3.5%). This result is similar to the variability measured across the four samples.

Notice that the maps show very similar characteristics. There is a characteristic 'horn' shaped feature to the bottom right corner of both maps. Observe also that on both maps there is a dense network of micropipes on the top-half and the right-side of the wafer. Additionally, notice that the center and the left-side of both maps have the lowest density of micropipes. All these similarities of the maps show a good degree of repeatability of the system. However, there are small variations from map to map. These variations are mainly in the quantity of micropipes in a frame, and not the location of micropipes. Since the average MPD are very similar (variation ~ 3.5%) this variation is acceptable.

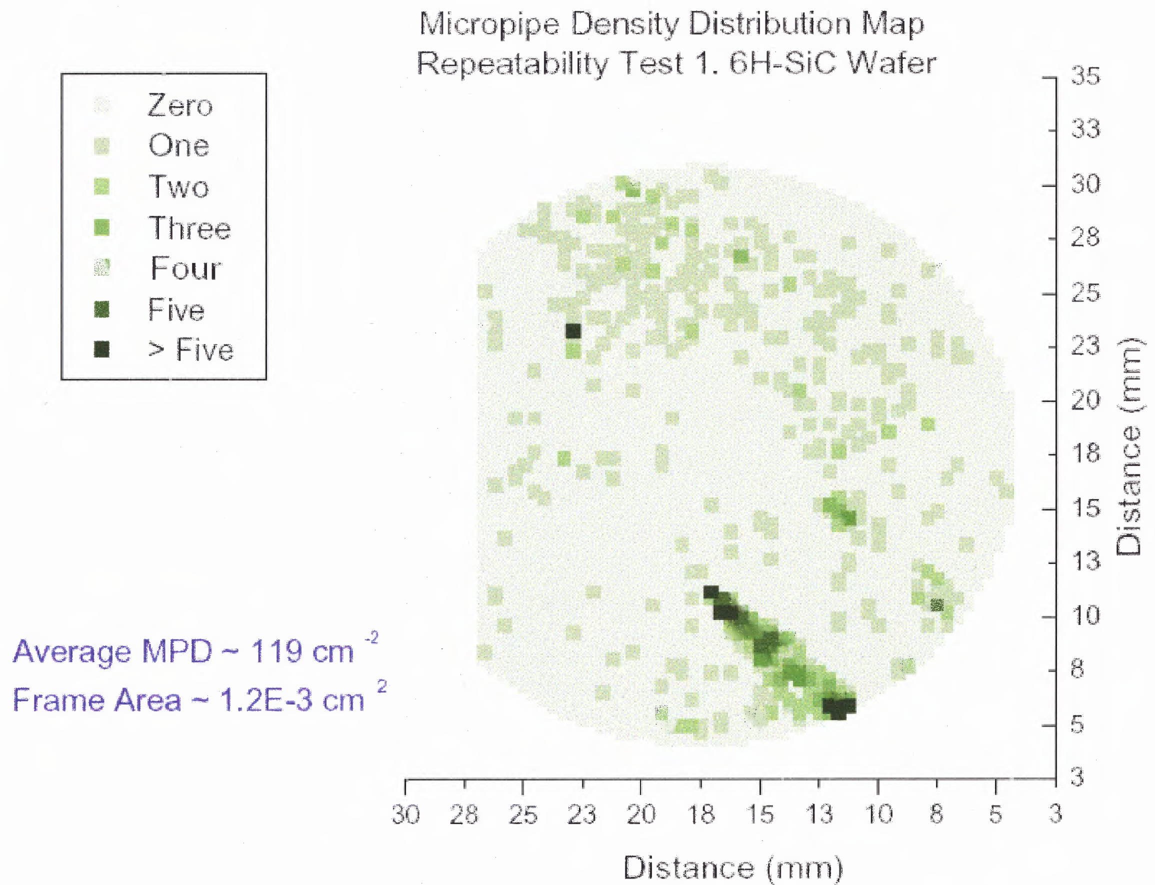

Figure 5.24 First run map of a repeatability test of a doped 6H-SiC wafer. Two-thirds of the wafer is mapped. The MPD is 119. Notice the characteristic features to the left corner of the map.

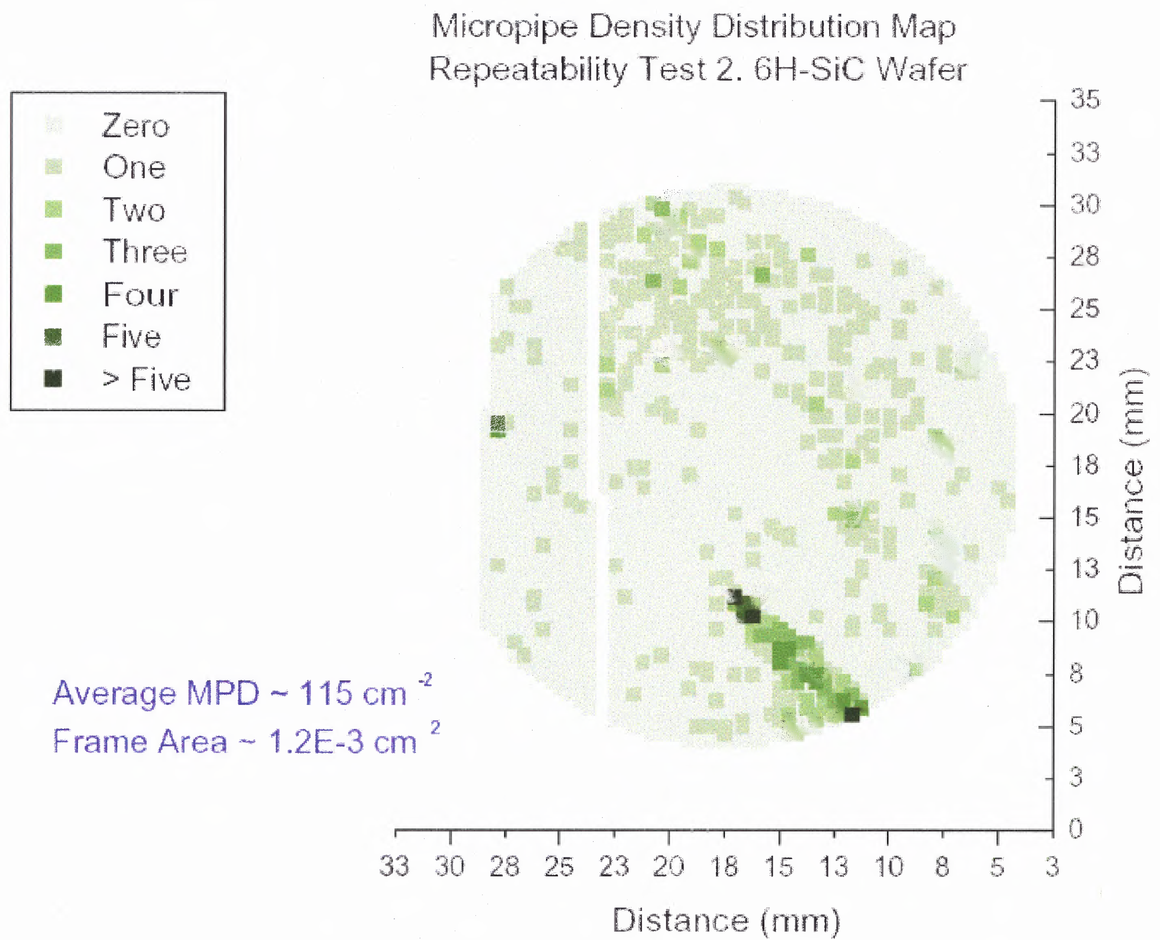

Figure 5.25 Second run map of a repeatability test of a doped 6H-SiC wafer. Two-thirds of the wafer is mapped. The MPD is 115. Notice the characteristic features to the left corner of the map are the same as that in Figure 15.24. The two maps on Figure 5.24 and 5.25 are nearly identical.

CHAPTER 6

SUMMARY

Accurate and comprehensive defect (micropipe and dislocation) counting and mapping of SiC wafers has been achieved using etching in molten KOH and optical microcopy. Although etching of SiC wafers is a destructive process, it is a relatively simple and economical method of delineating defects. Wafers can be etched at 450°C and for as long as 10 to 15 minutes. The defects revealed in the process include micropipes and dislocations. The etch depth of these defects range from 10μm to 60μm. Etch rates of SiC varies significantly depending on the surface finish of the wafers. As-sawn surfaces etch significantly faster than a polished surface. The KOH etch rate significantly slows down after the damage layer is removed and the graph of the material removal versus time follows the $y{\sim}log_{1.6}t$ trend line. The polytype of the etched SiC material also affects the etch rate.

The defects revealed by etching can be characterized using numerous techniques including AFM, SWBXT, optical transmission and reflective light microscopy. The SWBXT gives very accurate macro and micro images of the SiC wafer topology and defect densities. However this technique is very expensive. Transmission microscopy is not very sensitive can be used to count only large micropipes, but it misses smaller micropipes. This technique cannot delineate dislocations and requires long process time.

Optical reflective microscopy of etched samples is a relatively quick method of producing defect distribution maps of wafers. The author designed a system to acquire images of KOH etched SiC wafers and to analyze defects and count micropipes and

dislocations in the material. The system has been shown to be effective for wafers of different polytypes, doping concentrations and of different orientations. The results have been compared to those obtained by another, much more complicated and costly technique, SWBXT, and were shown to be very similar.

The ability to generate defect maps of SiC wafers will help to reveal the conditions under which micropipes are formed, and may ultimately lead to developing methods of their reduction. Since there is a well-established theory that screw dislocations play a role in the generation of micropipes, the correlation between micropipe and dislocation maps will help to validate it.

As an industrial equipment, the setup helps maintain constant validation of product quality and is helpful for showing trends in the processes used to grow these crystals.

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