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An interface chip for saw based sensor in an ad-hoc network

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ABSTRACT

AN INTERFACE CHIP FOR SAW BASED SENSOR
IN AN AD-HOC NETWORK

by
Yagneshwara Ramakrishna Vadapalli

The design of a smart integrated chemical sensor system that will enhance sensor performance and compatibility to ad hoc network architecture remains a challenge. This work involves the design of an interface chip for a Surface Acoustic Wave (SAW) based chemical sensor where the sensor reflects the RF input and introduces a time delay proportional to the concentration of the vapors absorbed by it. The interface chip detects the frequency shift as a function of the chemical species absorbed by the sensor and alerts the ad hoc network controller when a monitored parameter exceeded some threshold, based on local processing and measurements. System components are designed in an RF environment to carry out the local processing and estimation of the chemical absorbed. Simulation results for individual circuit components as well as the complete chip outline the robust performance of the system that improves chemical target detection and reduce false alarms. The design takes into account a sensor system with ten chemical SAW sensors operating at a resonant frequency of 1 GHz and an attenuation of 30 dB. The circuit is designed in to produce an alarm signal for a frequency shift of 1kHz due to a change in chemical concentration at the sensor, in 0.35 μ technology. The performance of the chip can be improved by scaling the design to 0.18 μ technology.

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IN AN AD-HOC NETWORK

by
Yagneshwara Ramakrishna Vadapalli

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APPROVAL PAGE

AN INTERFACE CHIP FOR SAW BASED SENSOR IN AN AD-HOC NETWORK

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To my dearest Mother and Father

ACKNOWLEDGEMENT

TABLE OF CONTENTS

TABLE OF CONTENTS
(Continued)

LIST OF FIGURES

LIST OF FIGURES
(Continued)

LIST OF FIGURES
(Continued)

CHAPTER 1

INTRODUCTION

With the development of information society, sensors are getting more and more challenges. Detecting and monitoring are becoming more and more complicated issues. There are many environments unsuitable to humans, therefore use of sensors is only solution. Remote monitoring and detection with quantitative measurement of toxic chemical or an environmental emission is of considerable importance. Detection of volatile organic compounds at trace levels in air emissions is also of high significance. The threat of terrorism is also prompting innovative approaches. Therefore it is required to design and develop the technologies that are rapid and cost effective deployment of sensor based systems in an ad-hoc fashion, where the signal from the sensors can be monitored remotely using advanced wireless technologies. For such applications a surface wave (SAW) based sensor with a gas-sensitive chemical layer can be used as a chemical or biochemical sensor. The SAW based sensor introduces a delay into the input signal proportional to the increase in concentration of a gas or organic vapor. In order for this type of chemical sensors to be useful in wireless applications in an ad-hoc network, it is required to have an interface circuit integrated in the device that alarms the network system for considerable atmospheric changes.

Many circuits are available for implementing SAW based chemical sensor for remote monitoring. None of them were applied for ad-hoc network since the decision process is left with every single node and unique interface circuit is required for this type of application. However, some of the signal-conditioning circuits are common.

In this thesis, we are designing an interface circuit that interfaces with the chemical sensor as well as the network processor. It is therefore required to understand the characteristics of the SAW based sensors. Chapter 2 describes the requirements of the network when, the interface circuit will be integrated and it also outlines the properties of SAW based sensors for chemical and biological applications. Chapter 3 explains the specifications required for such a chip and the architecture required to make appropriate decisions. Chapter 4 explains the functioning of the complete circuit along with building blocks used in the interface circuit along with simulation results using TSMC 0.35 μ SCMOS Technology. Chapter 5 summarizes the design and discusses the implementation issues involved in integrating this interface chip.

CHAPTER 2

WIRELESS INTEGRATED NETWORK SENSORS

2.1 Sensor Network

The Wireless Integrated Network Sensors provides a new monitoring and control capability for environmental safety and security. The WINS architecture includes sensing, signal processing, decision c apability and wireless network [1-3] as shown in Figure 2.1. The micro-sensors and interface circuit are continuously operating, whereas the ad-hoc network controller and wireless network interface are activated by the alert signal from the interface circuit. The micro-sensor senses the environment whereas interface circuit involves in decision-making process. When the controller receives an alert signal from the interface circuit it in turn sends the event to the neighboring nodes through t he w ireless n etwork i nterface. T he W INS a rchitecture i s d eveloped t o e nable continuous sensing and event detection at low power. When the controller detects the alert signal the wireless network interface starts operating.
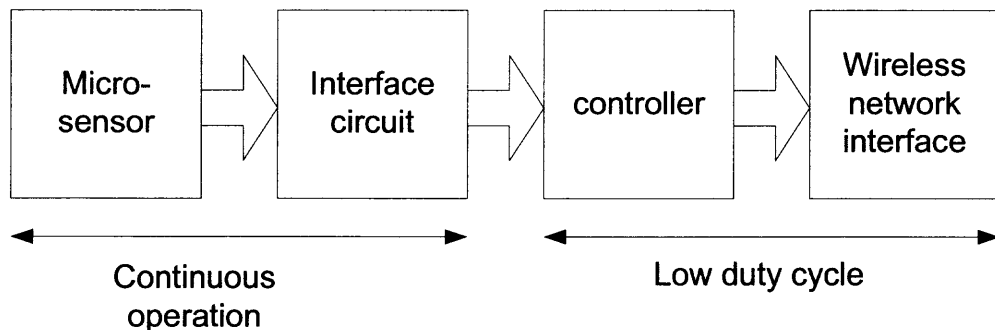
Figure 2.1 Wireless Integrated Network Sensor Architecture.

A highly sensitive micro-sensor is required to detect the change in concentration of the organic or inorganic vapor. As discussed in Chapter 1 a surface acoustic wave based chemical sensor is well suited for the application.

2.2 Surface Acoustic Wave (SAW) Sensor

A surface acoustic wave sensor is made up of a piezoelectric substrate (interdigital transducer) with metallic structures (reflection coupler gratings) on a polished surface. An electric input signal fed to a so-called inter-digital transducer (IDT) is transformed by the piezoelectric effect into a micro-acoustic wave propagating on the surface of the SAW device. In turn, the surface acoustic wave generates an electric charge distribution on an IDT, which results in an electric output signal [4-11].

Coating the SAW surface with chemical layers sensitive to a vapor makes SAW devices useful as chemical or biological sensors [4,9,16,17,18]. The chemical coated SAW sensor when exposed to a vapor undergoes mass loading. When a input signal is applied at the input of the sensor the IDT converters the signal into micro acoustic waves on the substrate. The mass loading of the adsorbed species reduces the phase velocity of the micro acoustic waves on the substrate, leading to a reduction in resonant frequency. This shift in frequency is proportional to the mass of vapor adsorbed [4,5].

IDT can transform the received RF-signal, which is typically in the range between 500MHz to 2.5 GHz into a micro-acoustic wave [4-8]. Hence the frequency of operation of the SAW sensor can be in the range of 500MHz to 2.5GHz. The SAW device can be operated at considerably higher frequencies leading to higher detectable frequency shifts i.e. higher sensitivity. (A dual delay line configuration with one bare (reference) channel

used in subtraction mode with layer-coated channel to reduce spurious temperature fluctuation effects are proposed in [4].) (Other variations include the use of a high Q resonator mode produced by a pair of reflecting arrays on either side of the IDTs and the use of multi-strip couplers in the two channels to reduce temperature effects by an order of magnitude [10].)

The Figure 2.1 shows the lateral view of a SAW sensor. When a RF input is given to the IDT, it converts the electric waves into micro-acoustic oscillations due to piezoelectric effect. These micro-acoustic waves propagate on the surface of the SAW device and get reflected by the reflectors and are transformed in to electric waves by the IDT and are obtained as the output at the other end of the IDT.
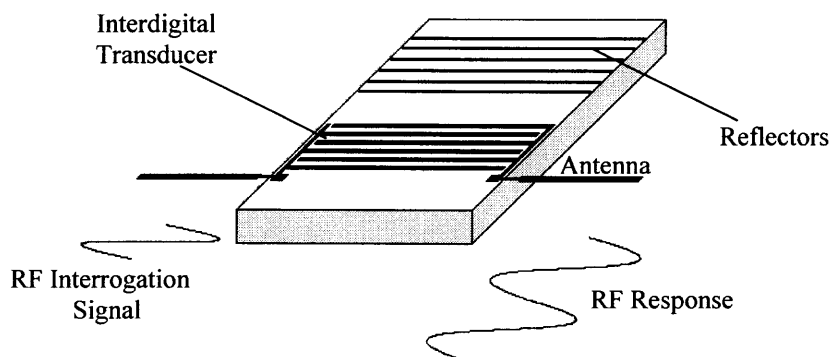
Figure 2.2 A Passive SAW Sensor with RF Input and Outputs.

2.2.1 Reusing the SAW Sensor

Once the absorbent on the SAW sensor adsorbs the volatile organic vapors, it is not easily desorbed the absorbed species. However, the SAW sensor can release the adsorbed vapor only when it is heated to an appropriate high temperature [7,12,13]. The inability of the SAW sensor to release the gases makes the device to be used only once before it

undergoes mass loading. Hence, it is clear that once there is a shift in frequency, then the shift in frequency can only increase with increasing concentration of the vapor when compared to a control device.

2.2.2 Frequency Shift

The frequency at the output of SAW device is shifted with respect to the input depending upon the increase in concentration of the vapor. The shift in frequency for a unit increase in vapor concentration is dependent on various factors like the Q-factor of the inter-digital transducer and absorption ability of the chemical coated on the sensor [1-4]. A SAW based sensor with a LiNbO$_3$ substrate and coated with the cavity compound dio-β-cyclodextrin (60nm) exhibits a frequency shift of 1 kHz for minimum gas concentration to be detected [5,13,14]. Hence the frequency shift for which the interface circuit should produce an alarming signal is assumed as 1 KHz for a LiNbO$_3$ substrate sensor with resonant frequency of 1 GHz.

2.2.3 Losses in SAW sensor

A SAW sensor introduces a loss of 20 to 40dB into the signal [1,5,6]. The attenuation of the SAW sensor depends on the Q-factor of the IDT. The losses occur due to the conversion of electric waves to acoustic waves by piezoelectric effect of the IDT, in addition to surface losses that occur due to the substrate and absorbing chemical. The loss in LiNbO3 substrate coated with cavity compound dio-β-cyclodextrin (60nm) is estimated as 40dB [5,15].

2.3 Circuit Requirements

The advantage of being sensitive to all physical quantities turns out to be a problem, if one parameter is to be detected. The frequency difference may no be due to an increase in chemical vapor concentration alone. To avoid this problem, a pair of exposed and unexposed chemical sensors is required. The exposed chemical sensor is an identical sensor, sensitive to all the ambient physical quantities, whereas unexposed chemical sensor is a SAW based chemical sensor identical to exposed chemical sensor and is exposed to all physical quantities except the vapor. Hence, if both chemical sensors are fed with same inputs and their output frequencies are compared then the frequency shift indicates the shift due to chemical vapor concentration.

CHAPTER 3

THE INTERFACE CHIP

3.1 Sensor System

The Figure 3.1 shows the complete Block Diagram of the interface chip. As shown in Figure 3.1 the local oscillator feeds the exposed (ECS) and unexposed chemical sensors (UCS) with a 1GHz signal with amplitude of 1.1 V and a dc level of 2.2 V. Four sets of different chemical sensors considered in this work. In each set one is exposed to the vapor and the other is kept unexposed. The output frequencies from exposed chemical sensors are compared with the output frequencies of unexposed chemical sensors in each set. For four different chemical sensors, there are four interface circuits, simultaneously detecting the frequency difference for the oscillations received from unexposed chemical sensor and exposed chemical sensor.

It is assumed that the chemical sensors are coated with four absorbent chemicals to detect different organic and inorganic vapors. As discussed earlier the frequency shift at the output of the SAW based sensor can be due to many physical variations such as temperature, pressure, etc. In addition, the type of absorbent material on the SAW sensor can contribute to the frequency shift. Therefore, outputs of exposed and unexposed chemical sensors are frequency compared to check for an increase in vapor concentration. Since both devices are operating in same physical environment, all variations except the vapor concentration constitute in common mode. Therefore, the frequency difference between the outputs of exposed and unexposed chemical sensors gives an estimate of

absorbed vapor concentration. The output signals of each exposed and unexposed

chemical sensors is given to each individual interface circuit as shown in Figure 3.1.
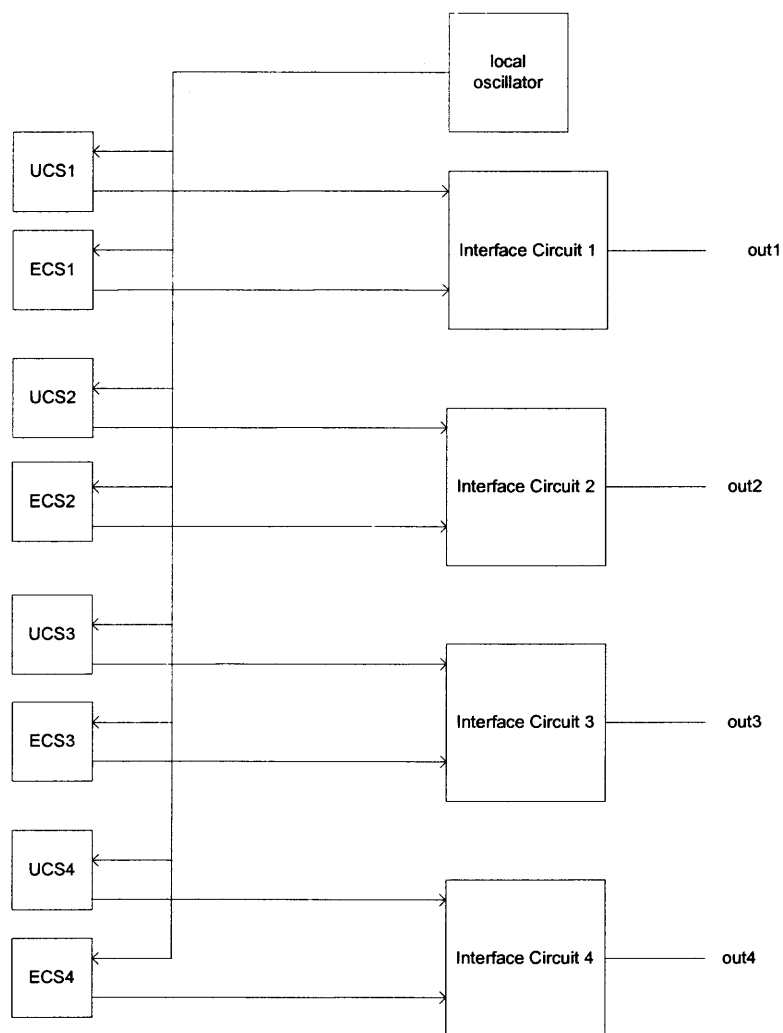

Figure 3.1 Sensor System.

3.2 Principle of Operation of Interface Circuit

The interface circuit is designed to alarm for frequency shifts greater than 1kHz.

Thus a part of quadricorrelator frequency [19,20] detector modified to meet the

specifications is used. The principle of operation of the interface circuit is shown in

Figure 3.2. Initially the outputs of the exposed and unexposed chemical sensors are multiplied. The output of the multiplier has both the sum and the difference frequency components of output signals from exposed and unexposed chemical sensors. These signals are then passed through a low pass filter. The low pass filter is designed to filter the frequency difference component alone. As the gain of a low pass filter is inversely proportional to the frequency, the peak-to-peak amplitude of 1 KHz output of the low pas filter is less than the peak-to-peak amplitude of 500Hz. A threshold level detector that follows the low pass filter produces a constant DC high for frequencies greater than 1 KHz and a series of pulses for frequencies less than 500 Hz.
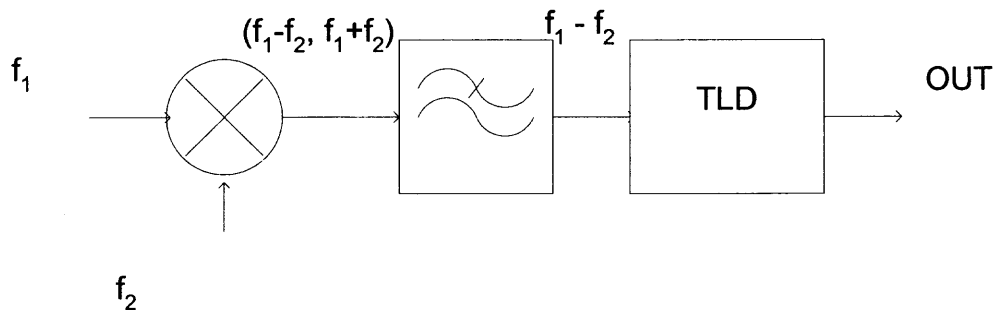
TLD: threshold level detector

Figure 3.2 Principle of Operation of the Interface Circuit

The output signals from the exposed and unexposed chemical sensors have to be passed through a voltage level shifter, single to differential converters and amplifier, before they are fed to a mixer. It is because the mixer is a differential circuit and needs a dc common-mode voltage. The output from the SAW sensor is single-ended, attenuated due to conversions from electric to micro-acoustic wave and back to electrical signal and has a zero dc common mode. Hence, the output signals have to have a shift in voltage level, and the signals need to be amplified and converted to differential signals.

The o rder i n w hich t hese t hree c omponents are placed, s hown i n F igure 3 .3 i s determined by their functionality. A simple RC ladder is used to obtain 90^0 leading and lagging outputs with respect to input. The leading output always has a zero dc common mode independent of the dc voltage level of the input signal, which will be discussed in detail in Section 4.2. Therefore, if the single to differential converter follows a voltage level shifter, the cause of the voltage level shifter goes in vain. Thus, the single to differential converter should be the first component of the interface circuit.

In order to amplify the differential signal obtained from the single to differential converter, the differential signal has to be voltage level shifted to the dc common mode of the input of the amplifier, which is accomplished by a voltage level shifter. The differential output from the voltage level shifter is amplified by a differential input differential output (DIDO) amplifier and fed to the mixer, a Gilbert's cell. The output of the mixer is the product of the two input signals obtained from amplifier stage and has two major components, the sum and the difference of the two input frequencies.
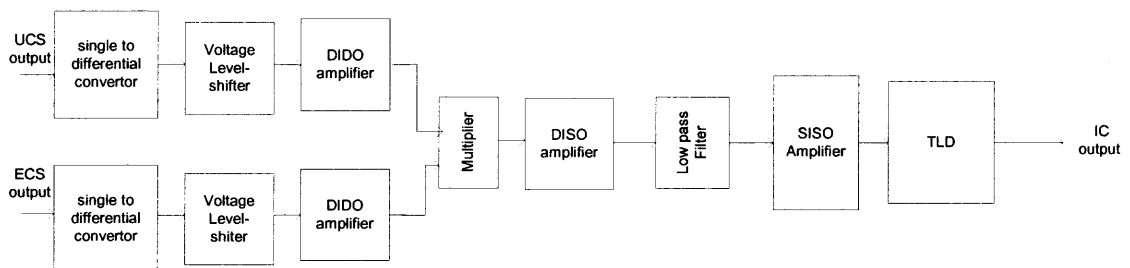
TLD: threshold level detector, **SISO**: single-ended in single-ended out, **DISO**: differential in single-ended out, **DIDO**: differential in differential out.

Figure 3.3 Internal Components of Each Interface Circuit.

The output of the Multiplier is fed to a Differential Input Single-ended Output (DISO) Amplifier, which not only amplifies the signal but also converts the differential input to a single-ended output. The output of the DISO amplifier is passed through a low pass filter, which filters the required frequency shift component from the amplified output of the multiplier. Low Pass Filters causes a difference in gains between two adjacent frequencies.

The next stage to the Low Pass Filter is a Single-ended Input Single-ended Output (SISO) amplifier with a diode-connected transistor and current source as its load. This stage is carefully designed to amplify and set the signal dc common mode voltage for the threshold level detector stage that follows the SISO. The common-mode voltage of the output of this stage can be adjusted by changing the bias voltage of the current source.

The output of the SISO amplifier is fed to a threshold level detector, which is a three-stage inverter. The first stage of the threshold level detector is a PMOS amplifier with a large resistive load. The threshold voltage of the PMOS-transistor of the inverter and the dc common mode voltage of the output of the previous stage are adjusted such that the PMOS-transistor conducts for the frequency less than 1 KHz. The low pass filter insures this, because the gain on frequencies less than 1 kHz will always be greater than the gain on frequencies greater than 1 kHz. Hence, the peak-to-peak voltage of frequencies less than 1 kHz will be more than the peak-to-peak voltage of frequencies greater than 1 kHz. Adjusting the common mode of the output of the SISO amplifier and threshold voltage of the PMOS-transistor, the PMOS-inverter is designed to conduct for frequencies below 1 kHz and remain cut-off region for frequencies above 1 kHz.

A NMOS- inverter stage follows with a large resistive load follows the PMOS-Common Source Amplifier. If the input to the PMOS-transistor just causes the gate-to-source voltage to go below the threshold voltage, then the output of the Amplifier may not reach full 3.3V and also for frequencies just above 1 kHz the gate-to source voltage reaches close to threshold voltage in which case, there is some leakage current flowing, which causes little spikes which is to be considered as noise. Hence to improve the output for the above two cases a NMOS- inverter is used. The size of the NMOS-transistor is very big to insure full swing from 3.3V to 0V. A third stage of PMOS-inverter is used for the same purpose.

CHAPTER 4

COMPONENTS

This chapter describes the components used to build the interface circuit. Each circuit is designed such that its output is compatible with input of the next component that follows it. Each individual circuit is explained with their post layout responses.

4.1 Local Oscillator

An o scillator p roduces a p eriodic o utput, u sually i n t he f orm o f v oltage. A s s uch, t he circuit has no input while sustaining the output indefinitely. A feedback Amplifier can act as an oscillator, if overall feedback gain becomes positive. If the closed-loop gain becomes infinity for its own noise component at frequency equal to w_0, then the feedback amplifier produces oscillations with frequency equal to w_0 [20, 21].

A typical ring oscillator is designed with odd number of gain stages in a loop. A three-stage feedback amplifier shown in Figure 4.1, acts as a ring oscillator provided the minimum gain of each stage must be at least equal to two. The circuit oscillates at a frequency of $1.732\ w_0$, where w_0 is the 3-dB bandwidth of each stage. The output of each stage is 240^0 out-of-phase with respect to neighboring outputs.
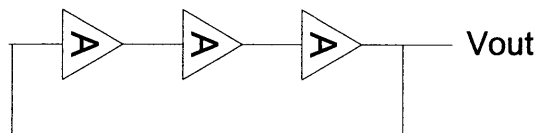

Figure 4.1 A 3-Stage Ring Oscillator.

The frequency of operation of the N stage ring oscillator is $(2NT_D)^{-1}$, where T_D denotes the large-signal delay of each stage. Hence, by varying T_D of each amplifier stage

different frequencies can be obtained. This can be achieved by changing the load impedance of the amplifier stage. A common source amplifier shown in Figure 4.2 employed as a delay stage. The advantages of using a diode connected PMOS load over a resistive load are: large load impedance can be obtained with low area, low power dissipation, low thermal noise (PMOS transistor compared to a resistive load) and high gain. However, the diode-connected load consumes voltage headroom, creating a trade-off between output voltage swing, voltage gain and input common-mode ranges. In order to achieve high gains, the (W/L) $_P$ of the diode-connected PMOS transistor has to be reduced, however this reduces the common-mode of the output signals. To solve this problem, a PMOS current source is connected to by-pass 90% of the current flowing through the driver transistor and still keeping the output common-mode and gain of the amplifier high [20,21].

Figure 4.2 Delay Stage used in Figure 4.1.

Figure 4.3 depicts the layout of the ring oscillator in 0.35 micron TSMC process. It can be seen from the layout that two metal layers are used for routing. The post layout transient response of the ring oscillator is shown in Figure 4.4.
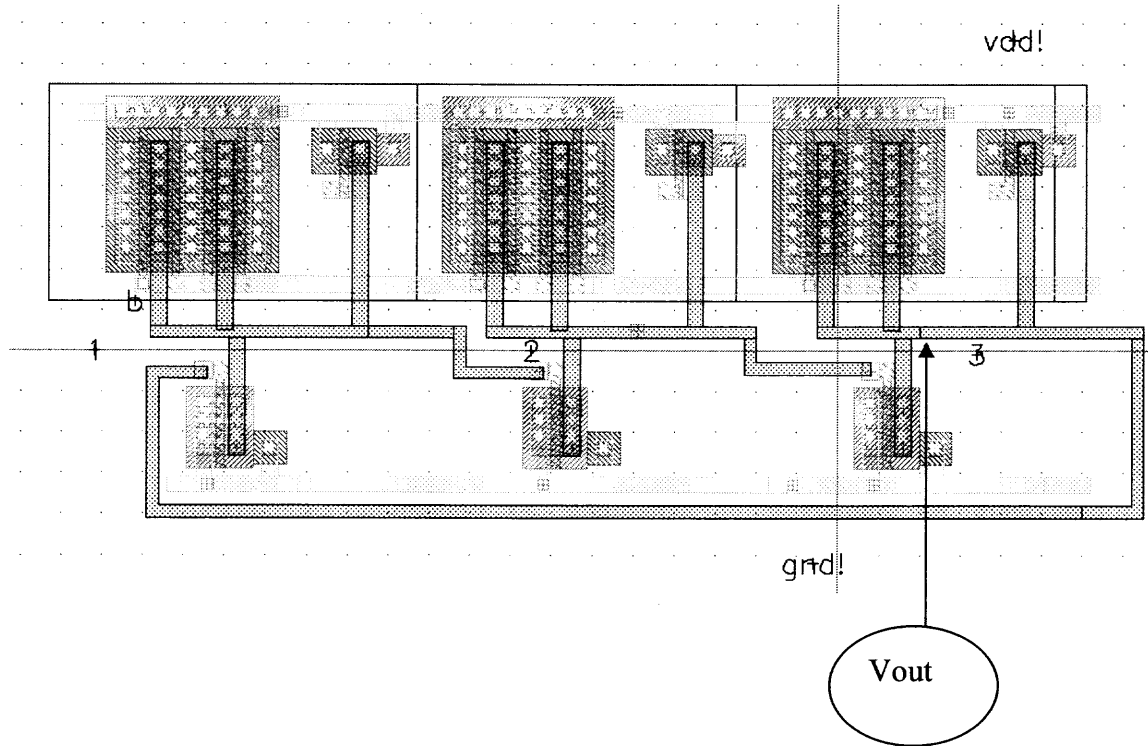
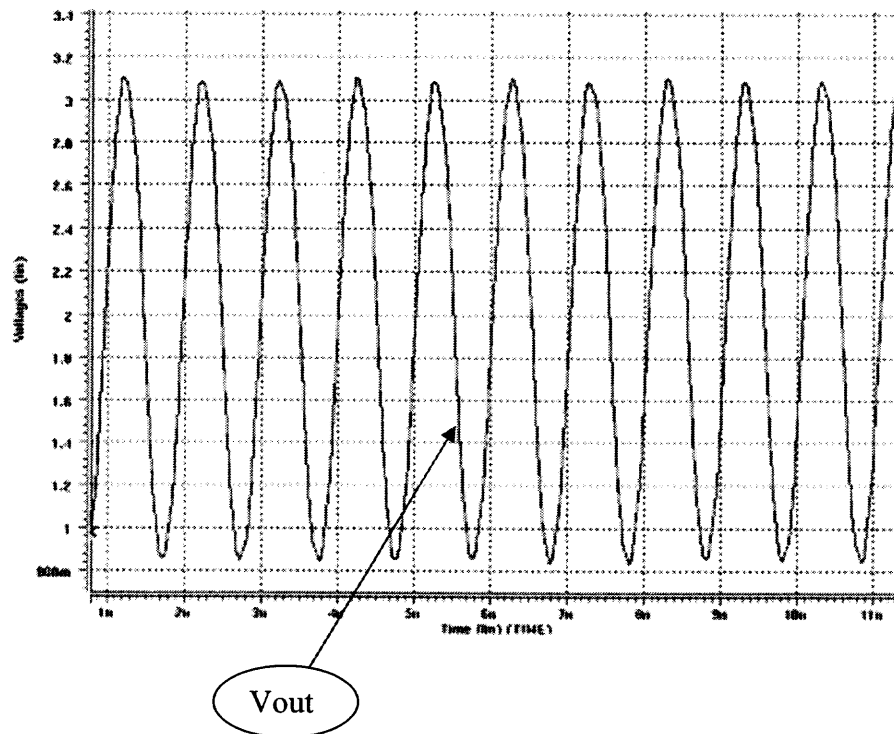**Figure 4.3** Layout of the 3-stage Ring Oscillator.

Figure 4.4 Post Layout Transient Response of Ring Oscillator shown in Figure 4.3.

It can be observed from the Figure 4.4 that output of the oscillator is a 1GHz sinusoidal signal with a common mode voltage of 2 V and a has voltage swing of 2.2V. The Fast Fourier Transform response of the oscillator is shown in Figure 4.5. The gain of the ring oscillator at 1Ghz frequency is the highest and is greater than the gain at any other frequency. The eye-diagram for a period of 1200ns is shown in Figure 4.6. A jitter less than 0.01ns is observed in the oscillations which ensures stable oscillations.
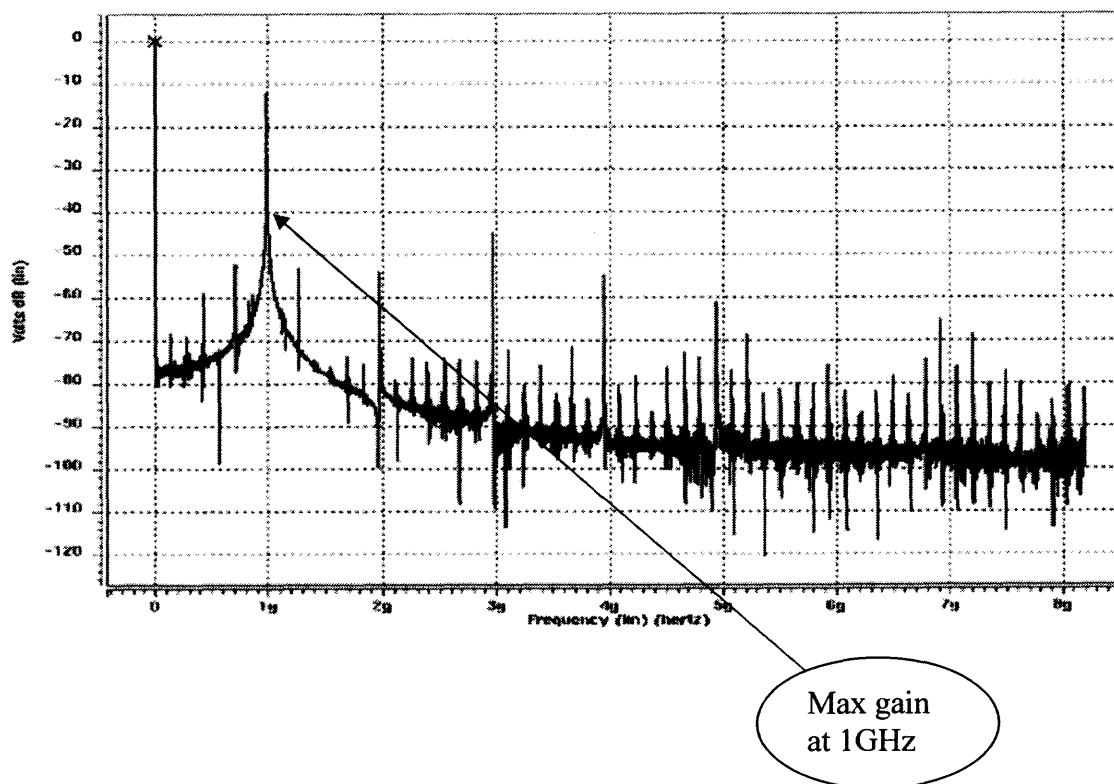
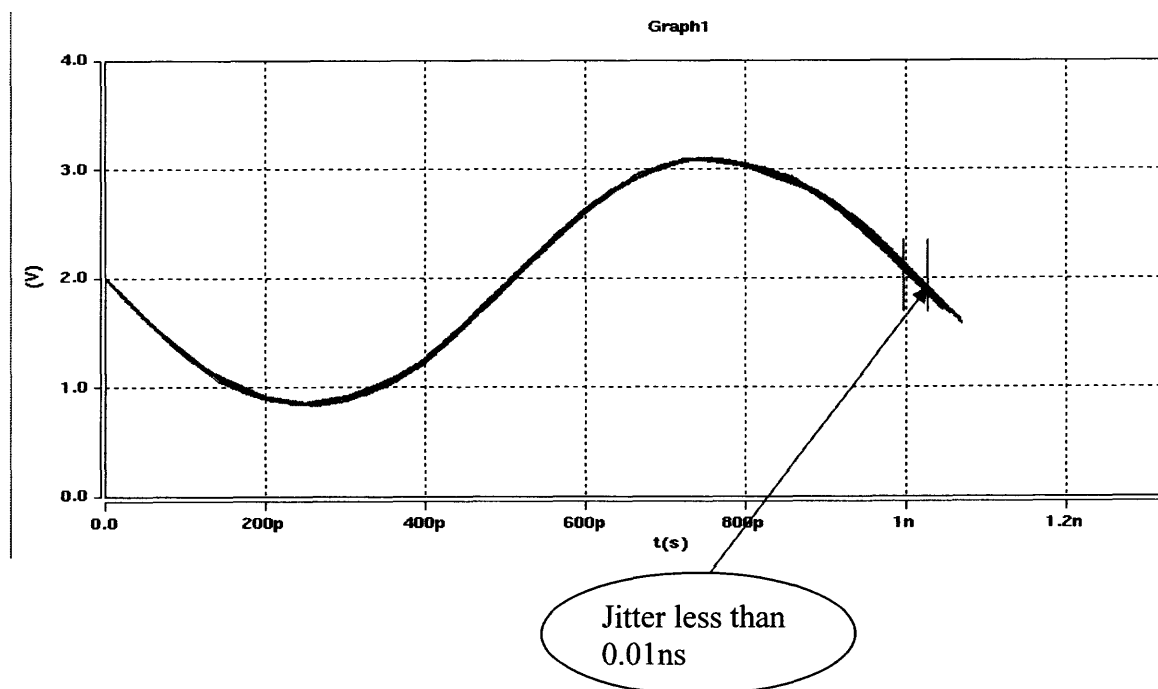**Figure 4.5** Post Layout Fast Fourier Response of Oscillator shown in Figure 4.3.

Figure 4.6 Eye Diagram of the Oscillator shown in Figure 4.3.

4.2 Single – Differential Converter

A mixer is used to multiply the outputs of unexposed and exposed chemical sensors as discussed in section 3.1. A Gilbert's cell, which is a differential circuit, is used as an analog multiplier. However, the outputs of the chemical sensors are single-ended. To convert the single-ended signals to differential signals a single to differential converter is required. Several circuits are proposed with the combination of opamp and RC network in [23]. However, due to the available frequency margin of 500 Hz to compensate for the variations due to temperature, a simple RC network shown in Figure 4.7 is used as a single to differential converter.

A RC combination produces a 45^0 lead or lag depending upon where the output is collected. Cascading two RC- circuits whose outputs are collected across the Resistor produces a lead of 90^0, and cascading two RC- circuits whose outputs are collected across the Capacitor produces a lag of 90^0. The amplitude of the outputs obtained from the two circuits will be equal if the input frequency is equal to the resonant frequency of the R-C circuit. Thus, the design shown in Figure 4.7 can be employed as a single to differential converter [20]. The outputs V1 will be 90^0 lagging and V2 will be 90^0 leading with respect to the input Vin. Hence the two outputs are out-of-phase by 180^0. The circuit is designed to have its resonant frequency at 1 GHz, and thus the two outputs V1 and V2 will have same peak-to-peak amplitudes and 180^0 out-of-phase.
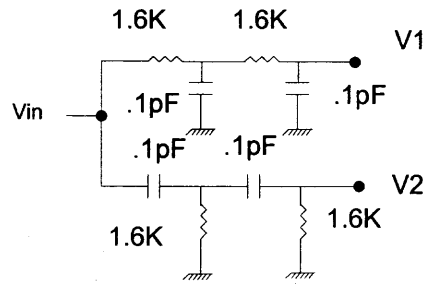
Figure 4.7 Single to Differential Converter.

The layout of the single to differential converter designed for 1 Ghz resonant frequency is shown in Figure 4.8. The post layout transient response of the single to differential converter is shown in Figure 4.9. It can be seen from Figure 4.9 that the output waveforms of the converter are 180^0 out of phase and are having equal amplitude.
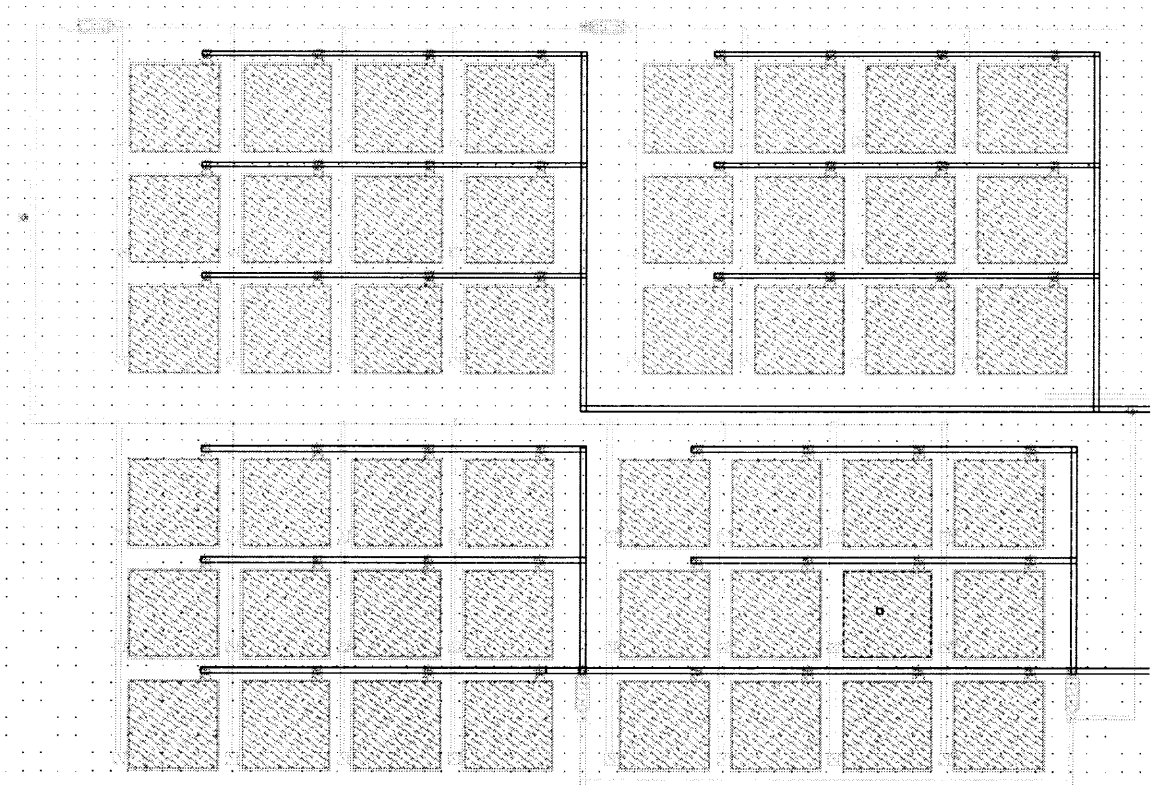

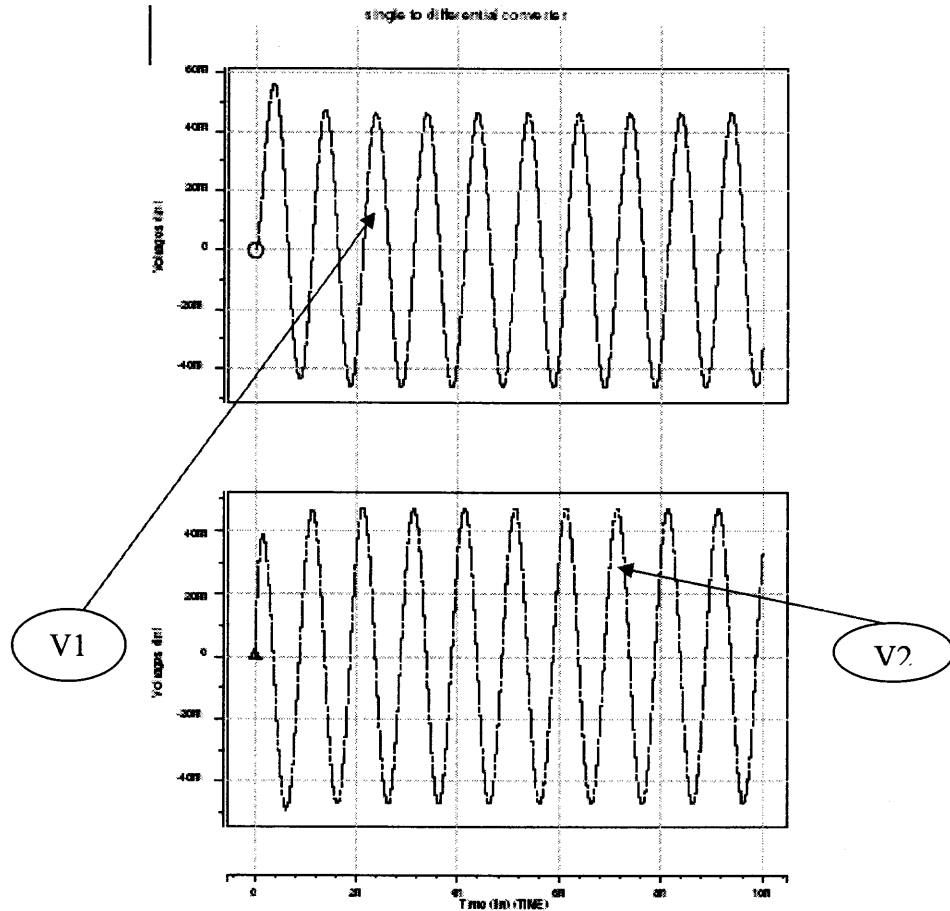**Figure 4.8** Layout of the Single to Differential Converter.

Figure 4.9 Output Waveforms of Single to Differential Converter.

4.3 Voltage Level Shifter

Voltage level shifter is the second stage of the interface circuit that follows the single to differential converter. As discussed in Section 3.1, the voltage shifter is used to shift the common-mode of the differential signals obtained from single to differential converter. A voltage level shifter designed for 1 GHz input frequency is shown in Figure 4.10. The common mode of the output voltage can be adjusted by varying the reference voltage (Vref) or by changing the width of diode connected transistor.

The input to the chemical sensors is a 1 GHz frequency signal from an oscillator, which has a dc-common-mode voltage of 2V (refer to Figure 4.4). If the output from the chemical sensor has a common-mode voltage then the capacitor in the voltage level shifter circuit acts as a blocking capacitor.
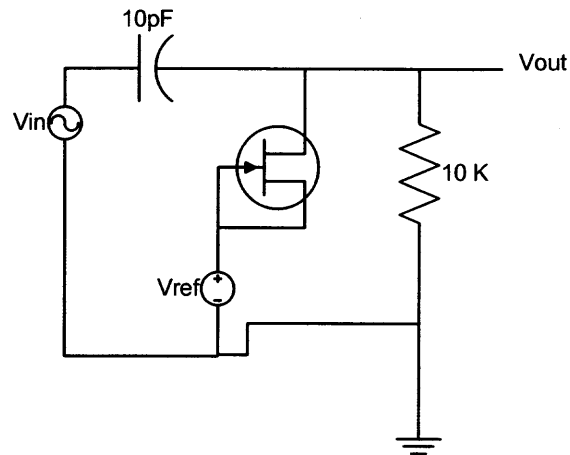

Figure 4.10 A Voltage Level-Shifter with a Diode-connected MOS Transistor.

The layout of the level-shifter with diode-connected MOS transistor is shown in Figure 4.11. The post-layout transient response of the voltage level shifter for the level-shifter is shown in Figure 4.12. The input to the voltage level-shifter is 1 GHz signal with common-mode voltage of 1V and peak-to-peak voltage of 0.2V. The output of the level-shifter circuit has a dc common mode of 2.4V with a peak-to-peak swing of 0.1V.
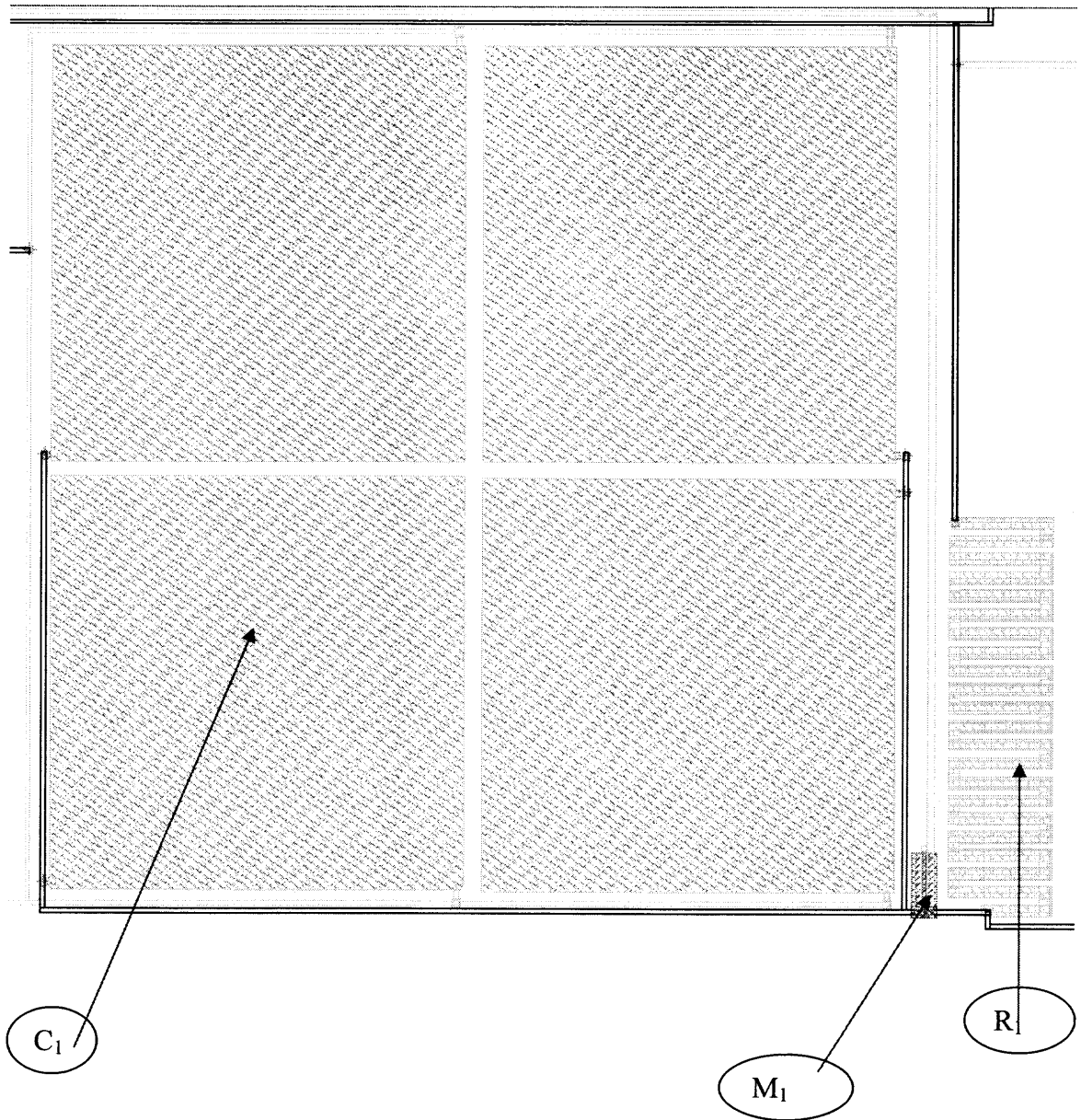
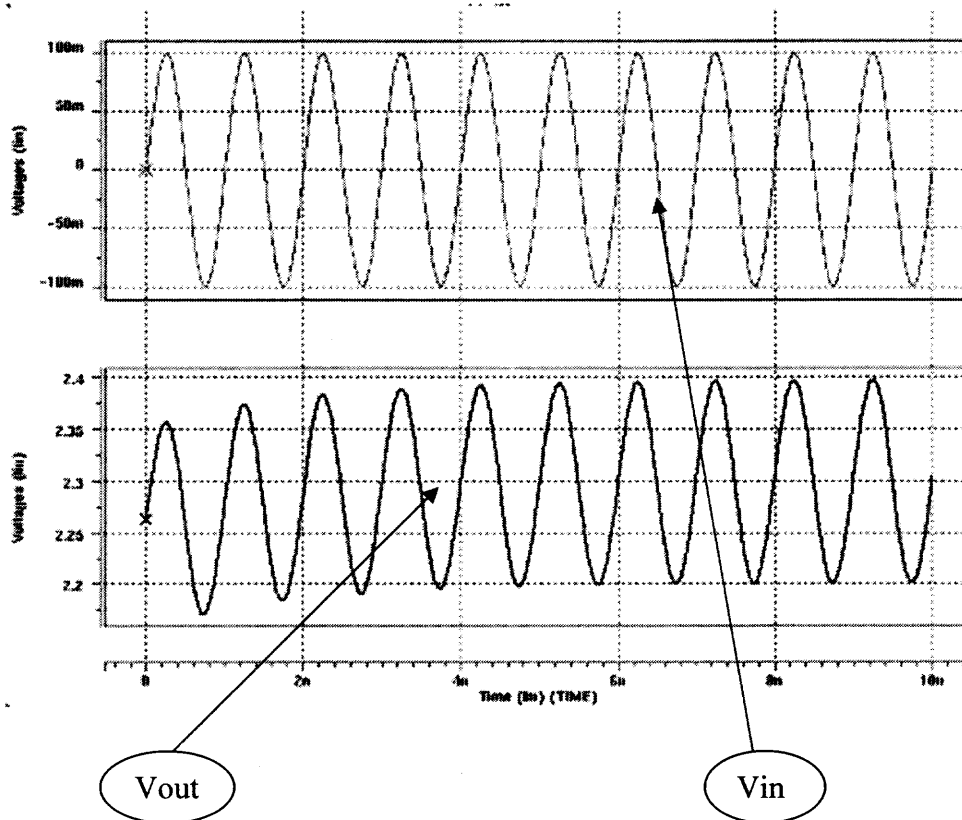**Figure 4.11** Layout of Level-Shifter shown in Figure 4.10.

Figure 4.12 Input and Output Waveforms of a Level Shifter.

4.4 Multiplier/Mixer

A Gilbert's cell is used to multiply the outputs of exposed and unexposed chemical sensors after they are converted to differential, voltage level shifted and amplified. The small signal gain of a differential pair is a function of the tail current [20]. The two driver transistors of the differential pair provide a simple means of steering the tail current. By combining these two properties, if a control voltage controls the tail current of the Differential pair, then the gain of the amplifier is a function of controlled voltage, such an amplifier is called as Variable Gain Amplifier (VGA) shown in Figure 13.
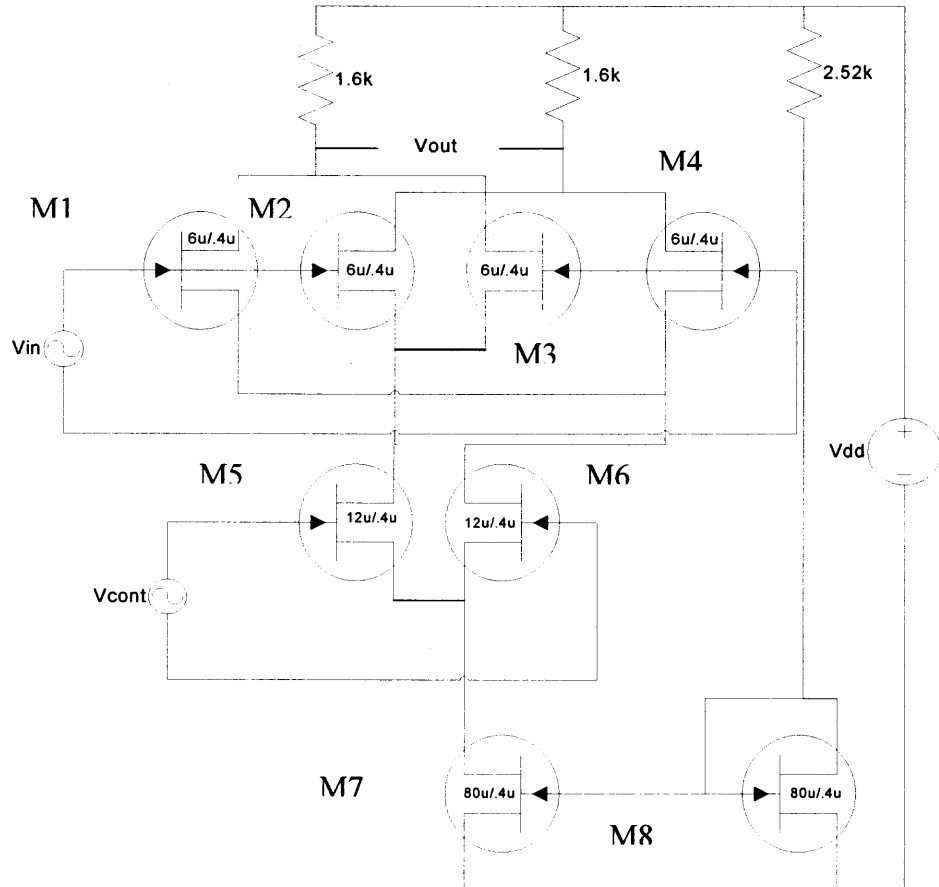
Figure 4.13 A Gilbert's Cell.

The output voltage of the variable gain amplifier is the product of the input voltage (V_{in}) and the gain (A_v). However, gain (A_v) is a function of control voltage (V_{cont}). Thus, the output voltage (V_{out}), can be expressed as follows

$$V_{out} = V_{in} * f(V_{cont}) \qquad (4.1)$$

For small values of V_{cont}, the Taylor's expansion of f (Vcont) is approximately equal to V_{cont}. Hence, the Output Voltage is the product of input voltage (V_{in}) and Control Voltage (V_{cont}).

$$V_{out} = (V_{in} * V_{cont}) \qquad (4.2)$$

Thus, the output can be approximated to the product of the two inputs by making both input voltages small.

As a cascode structure, the Gilbert cell consumes greater voltage headroom than a simple differential pair does. This is because the two differential pairs M1-M2 and M3-M4 are stacked on top of the control differential pair. In order for the transistors M5-M6 to be in saturation the difference of the common mode levels of the input and control voltage must be atleast $V_{GS1} - V_{TH5}$.

4.4.1 Design of the Multiplier

The current in the current mirror is assumed to be equal to 1mA. Large current is assumed to make the Mixer operate at 1 GHz frequency. The drain voltage Vdd, is assumed as 3.3V. As there are four cascode stages the V_{ds} across current mirror is assigned as 0.3V, the voltage across transistors M5-M6 as 0.8V the voltage across M1-M4 as 0.8V and across the resistors as 0.8V.

The W/L values of the transistors are obtained from the following formula:

$$I_{ds} = K` \ W/L \ V_{ds}{}^2$$

Also the gain of the Gilbert's cell is adjusted to produce an output compatible in both gain and voltage level.

4.4.2 Layout and Results

The layout of the Multiplier is shown in Figure 4.14. The post layout transient response of the Gilbert's Cell is shown in Figure 4.15. The inputs to the Gilbert's cell are stimulated with a 1GHz signal with peak-to-peak amplitude of .2V. As shown in the Figure 4.15, the output is a 2 GHz, differential sinusoidal signal and with its minimum voltage at zero volts.
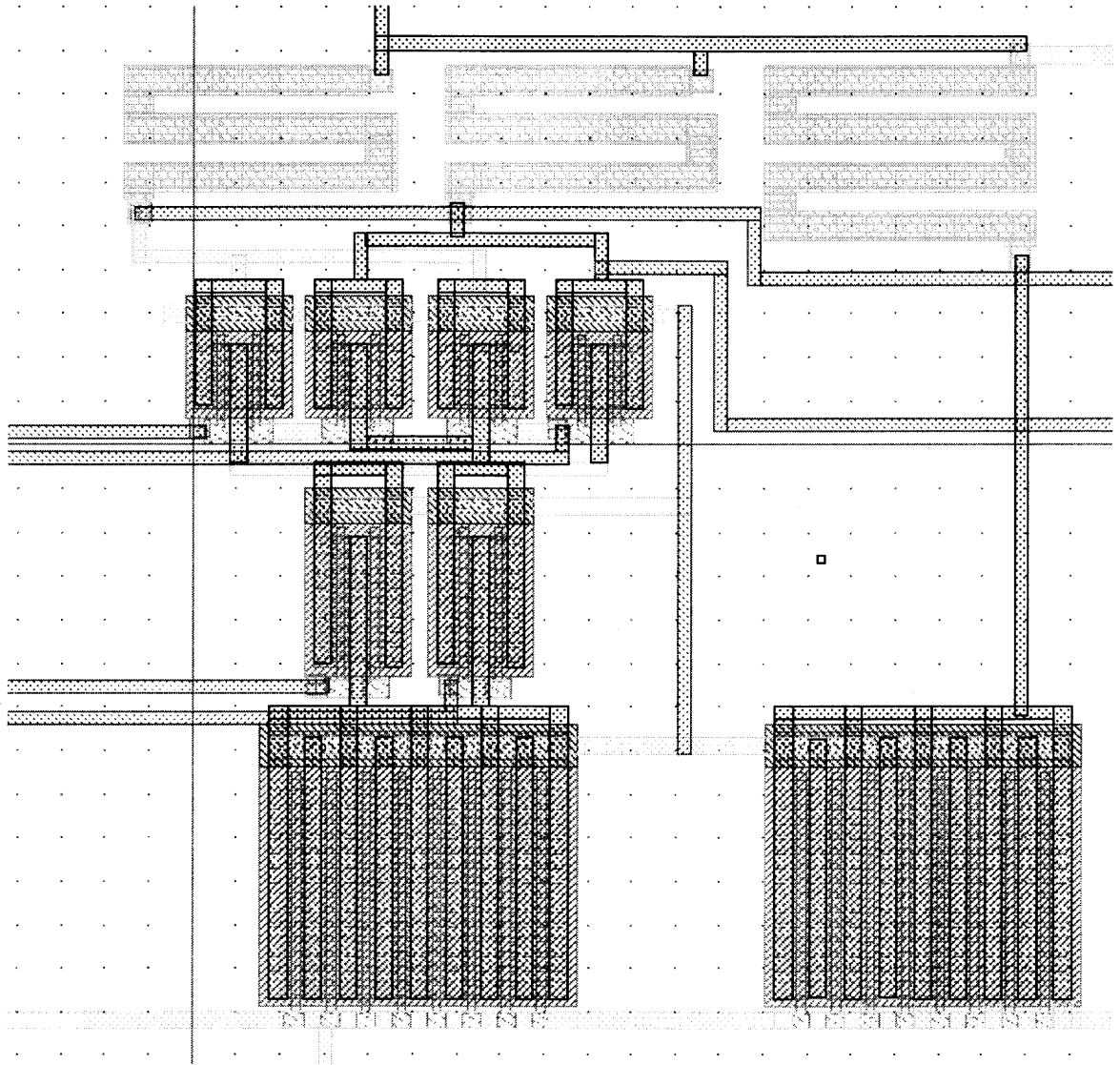
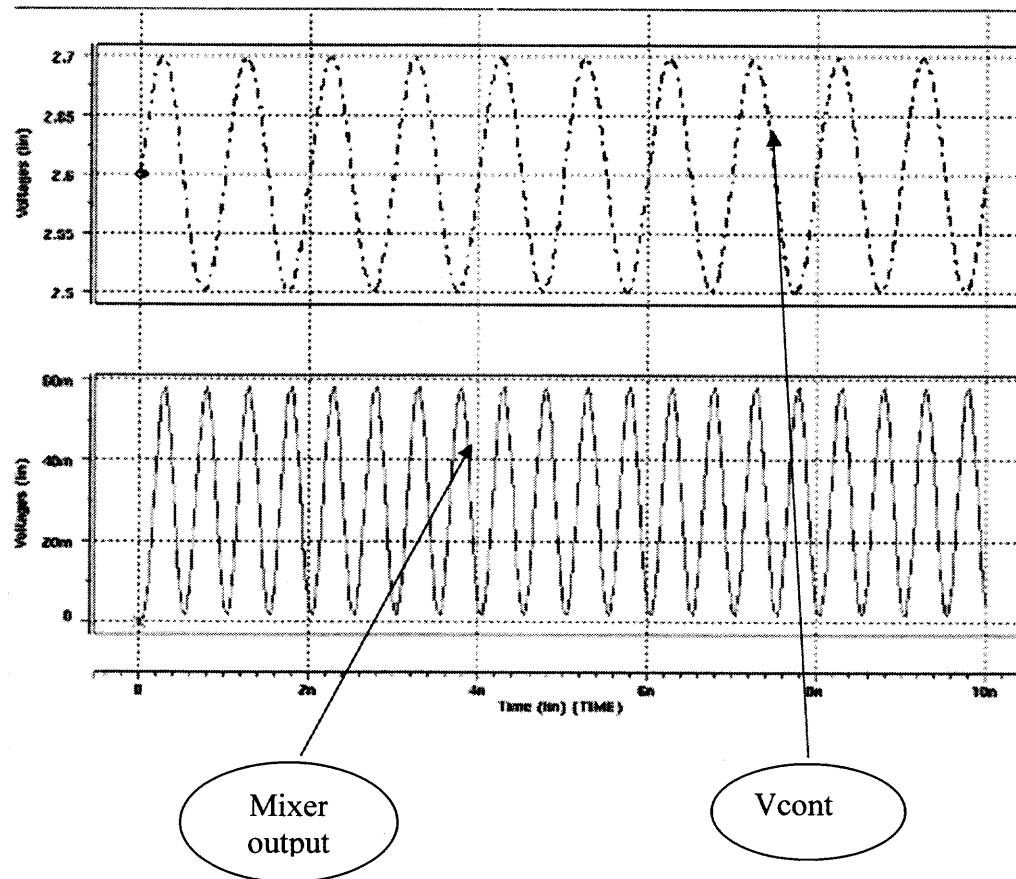**Figure 4.14** Layout of Gilbert's Cell shown in Figure 4.13.

Figure 4.15 Post Layout Transient Response of Gilbert's Cell shown Figure 4.14.

4.5 Low Pass Filter

A simple R-C circuit shown in Figure 4.16 is used as a low pass filter [21]. The cut-off

frequency of the low pass filter is determined by the values of R and C. The low pass

filter is to be designed for a frequency range of 1 KHz. A proper design of low pass filter

is needed such that there is a gain difference of 6 dB between 1000Hz and 500 Hz. The

gain of the low pass filter is inversely proportional to the frequency of the input signal.

Hence, the gain of the low pass filter for a 500Hz signal is more than the gain for 1KHz

signal. The range of frequencies between 500 Hz and 1KHz acts as a transition range and

compensates for the shifts caused by the changes in temperature. The low pass filter is designed to obtain a gain difference of 6dB between 500 Hz and 1KHz.
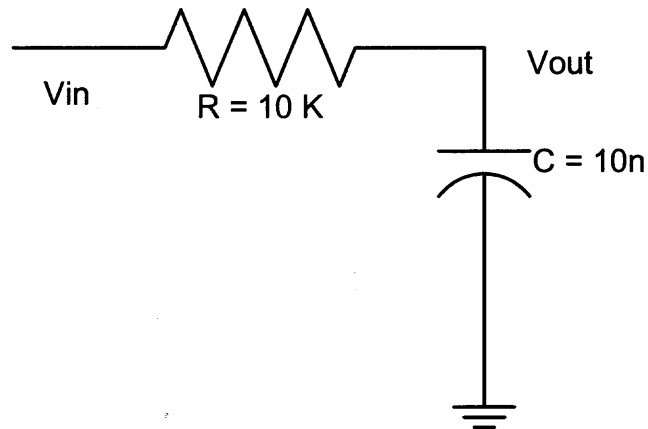

Figure 4.16 Low Pass Filter.

4.5.1 Analysis of the Results of a Low Pass Filter

The post layout frequency response of the low pass filter is shown in Figure 4.17. It can be seen from the Figure 4.17 that there is a gain difference of 6 dB between 500 Hz and 1 KHz.
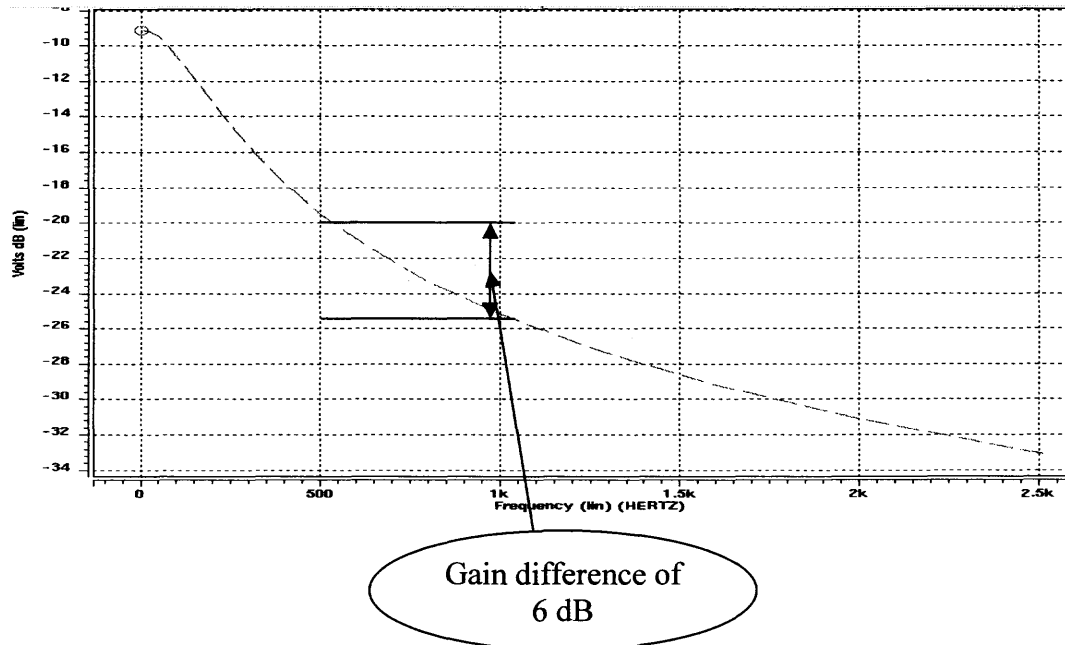
Figure 4.17 Post Layout Frequency Response of the Low Pass Filter.

The Figures 4.18 and 4.19 show the transient response of the low pass filter for input frequencies of 500 Hz and 1 KHz. It can be observed that there is a voltage difference of 0.2 V in amplitudes of the two outputs.
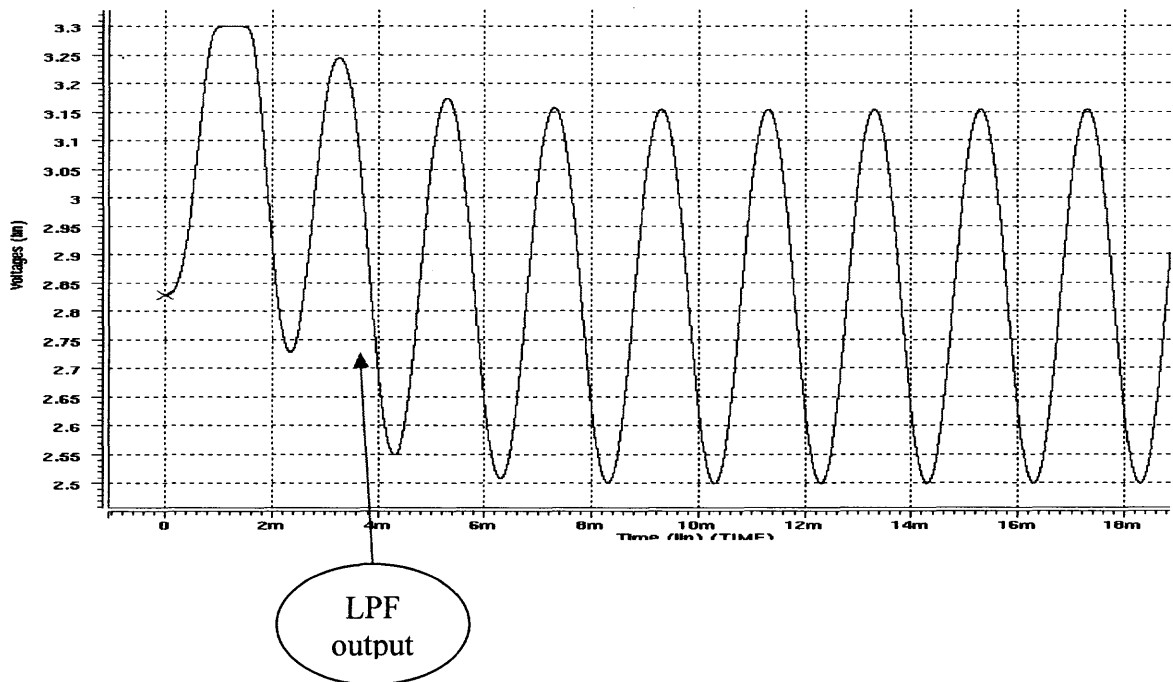

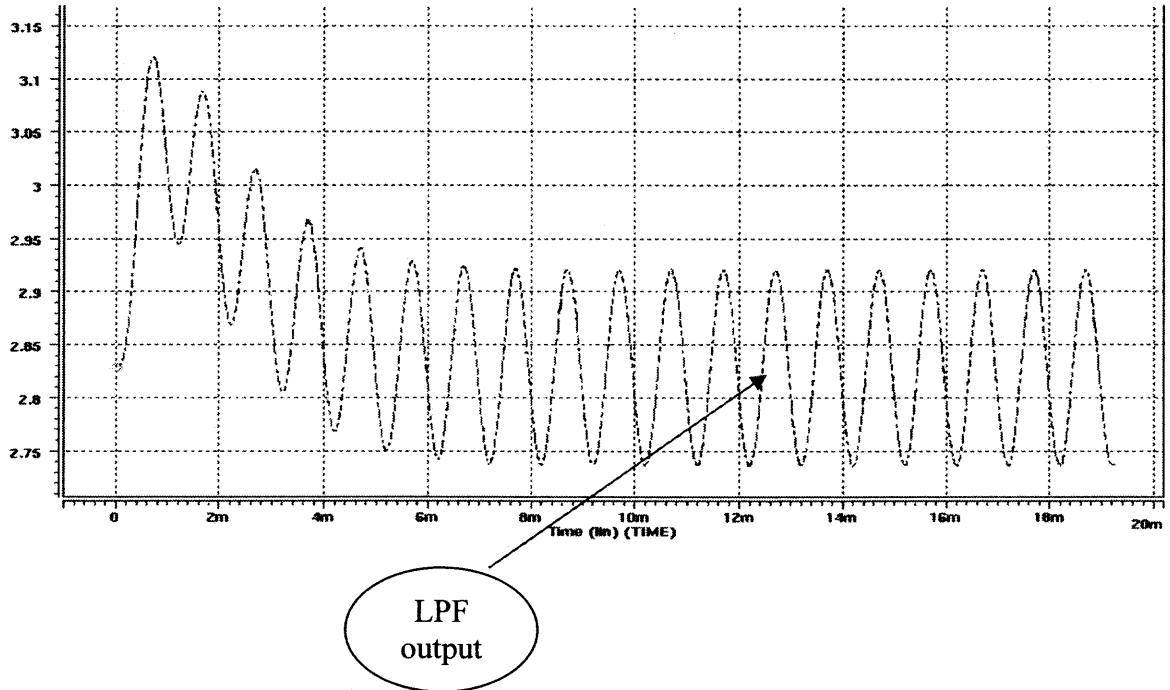Figure 4.18 Post Layout Transient Response of the LPF for 500 Hz Input.

Figure 4.19 Post Layout Transient Response of the LPF for 1 KHz signal.

4.6 Amplifier

Amplifier stages with different gains are used in different stages of the inter face circuit to match the common-modes of the stage and to amplify the signals. In general amplifiers can be classified into open loop and feedback amplifiers, former are being used in the interface circuit. The load and transconductance of the driving transistor determine the voltage gain, output voltage swing and input common mode range. Diode connected or current source loads shown in Figures 4.20 and 4.21 have higher gain than resistive load. The voltage gain of the amplifier shown in Figure 4.20 is given by the following formula.

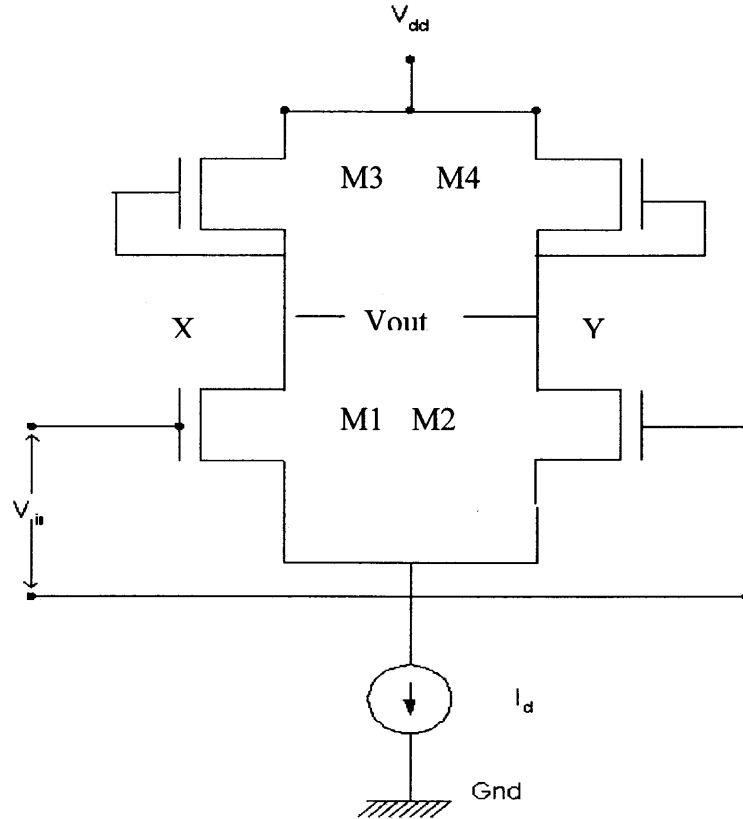$$A_v = - g_{mN}(r_{ON} \| r_{OP}) \tag{4.3}$$

Figure 4.20 An Amplifier with Diode-Connected Load.

In the circuit shown in Figure 4.20, the diode-connected loads consume voltage headroom, thus creating a trade-off between the output voltage swings, the voltage gain, and the input CM range. For a given bias current and input device dimensions, the circuit's gain and the PMOS overdrive voltage scale together. To achieve higher gain, $(W/L)_P$ must decrease, thereby increasing $|V_{GSP} - V_{THP}|$ and lowering the CM level at nodes X and Y[11]. In order to solve the above difficulty, part of the bias currents of the input transistors can be provided by PMOS current sources. By adding the current sources the g_m of the load devices reduces, because the current through load reduces with same aspect ratio. As shown in Figure 4.21, if the transistors M5 and M6 carry 80% of the drain current of M1 and M2, the current through M3 and M4 is reduced by a factor of five.
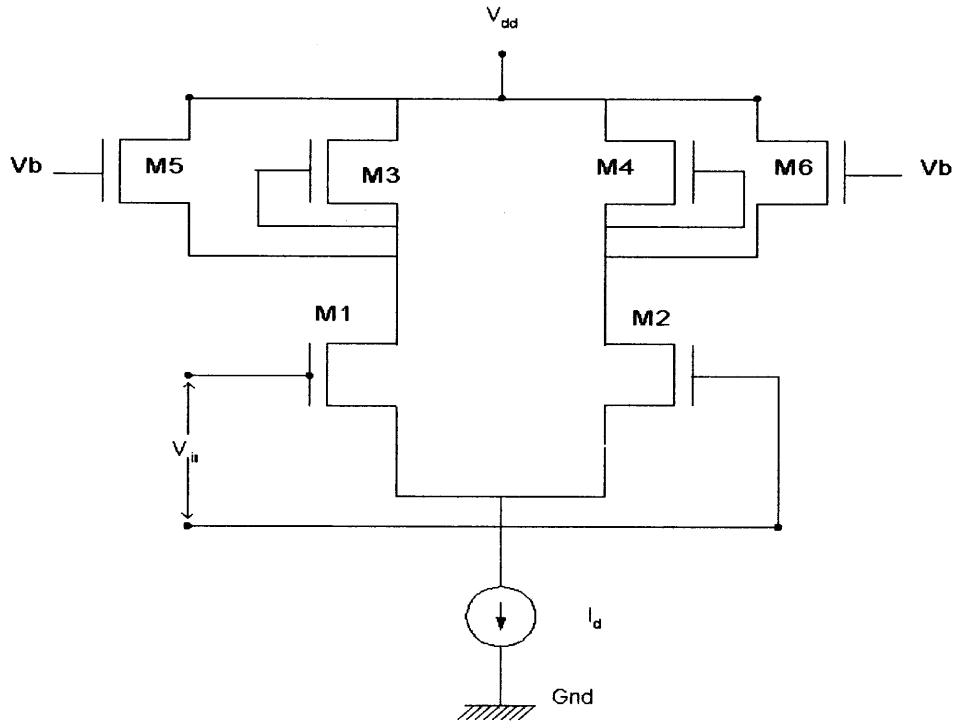
Figure 4.21 An Amplifier with Diode-Connected Load along with a Current-Source.

4.7 Threshold Level Detector

A 3-stage inverter as shown in Figure 4.22 is used to detect if output of low pass filter crosses the threshold voltage. Input voltage at each stage is compared with threshold voltage of the driving transistor in the Amplifier. Two stages are cascaded to insure complete swing from 0 to 3.3 V at the output for the input voltage just above the threshold voltage.
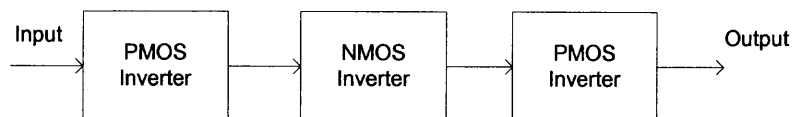

Figure 4.22 A Three-stage inverter used as Threshold Level Detector.

A Simple PMOS Inverter is used as a voltage level detector. The PMOS transistor will be in cutoff region until the source-gate voltage V_{sg} is greater than $|V_{THP}|$. Thus, the Threshold voltage of the PMOS transistor acts as a reference voltage for comparison. A circuit equivalent of the Figure 4.22 is shown in Figure 4.23. The size of the PMOS transistor is chosen very high and resistance of the load should also be very high, so that the circuit 's sensitivity is high. The level-shifter adjusts the common-mode voltage at the input, such that the negative peaks of the frequencies below 1 KHz switch on the PMOS transistor. For the frequencies close and below 1 KHz, the negative peaks switch on the transistor for very less time, which may not be sufficient for full output swing from 0 to 3.3V, a large transistor would ensure higher current and large resistance ensures higher output voltage, thus higher sensitivity.
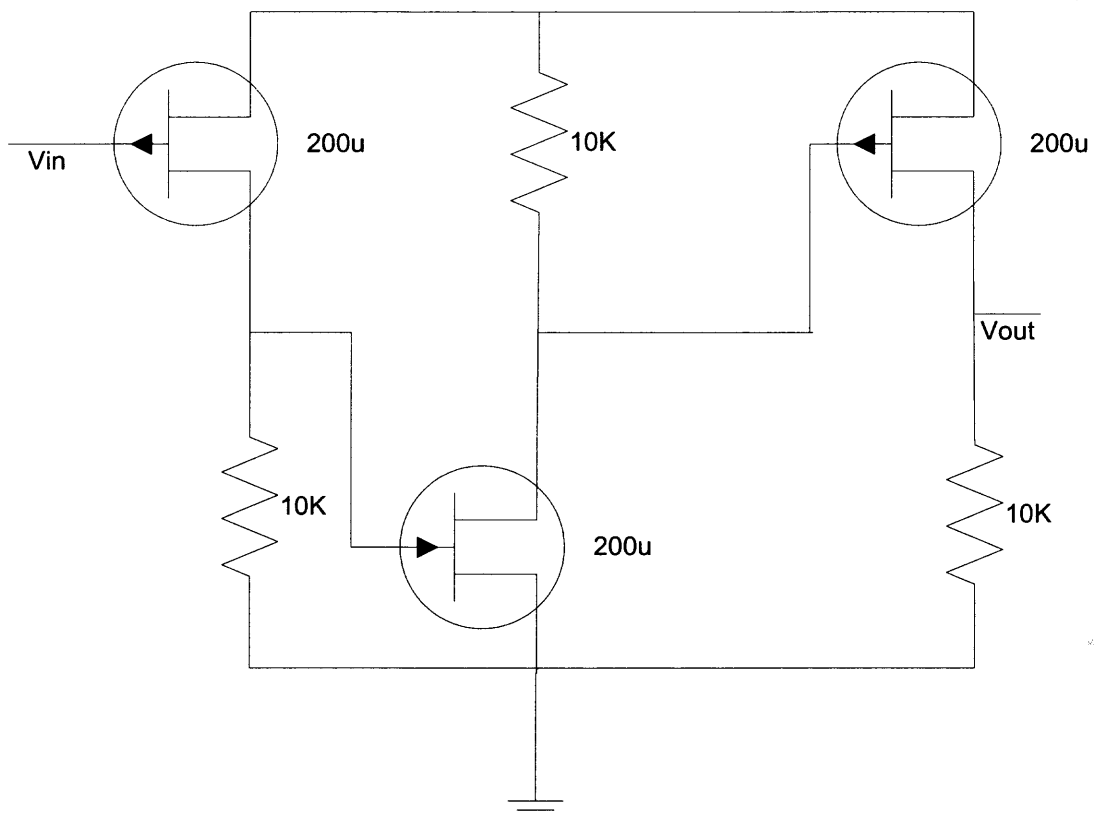
Figure 4.23 Circuit Diagram for TLD shown in Figure 4.22.

For the frequencies close to 1 KHz, the output of the PMOS inverter is not perfect because of spikes for the frequencies higher than 1 KHz and incomplete swings for the frequencies less than 1 KHz. These spikes and incomplete swings may lead to ambiguity between 1 and 0. This problem can be solved using an NMOS inverter with a large resistive load and transistor width, which ensures higher sensitivity with negligible spikes. A third stage of inverter has been used for the same purpose.

4.8 Interface Circuit

The complete layout of an interface chip is shown in Figure 4.24. The layout consists of four interface circuits in parallel. The local oscillator is placed over the top of the interface circuit. The layout of the single interface chip is shown in Figure 4.25. It can be seen from the Figure 4.25 that three metal layers have been used for routing (blue, yellow, brown).
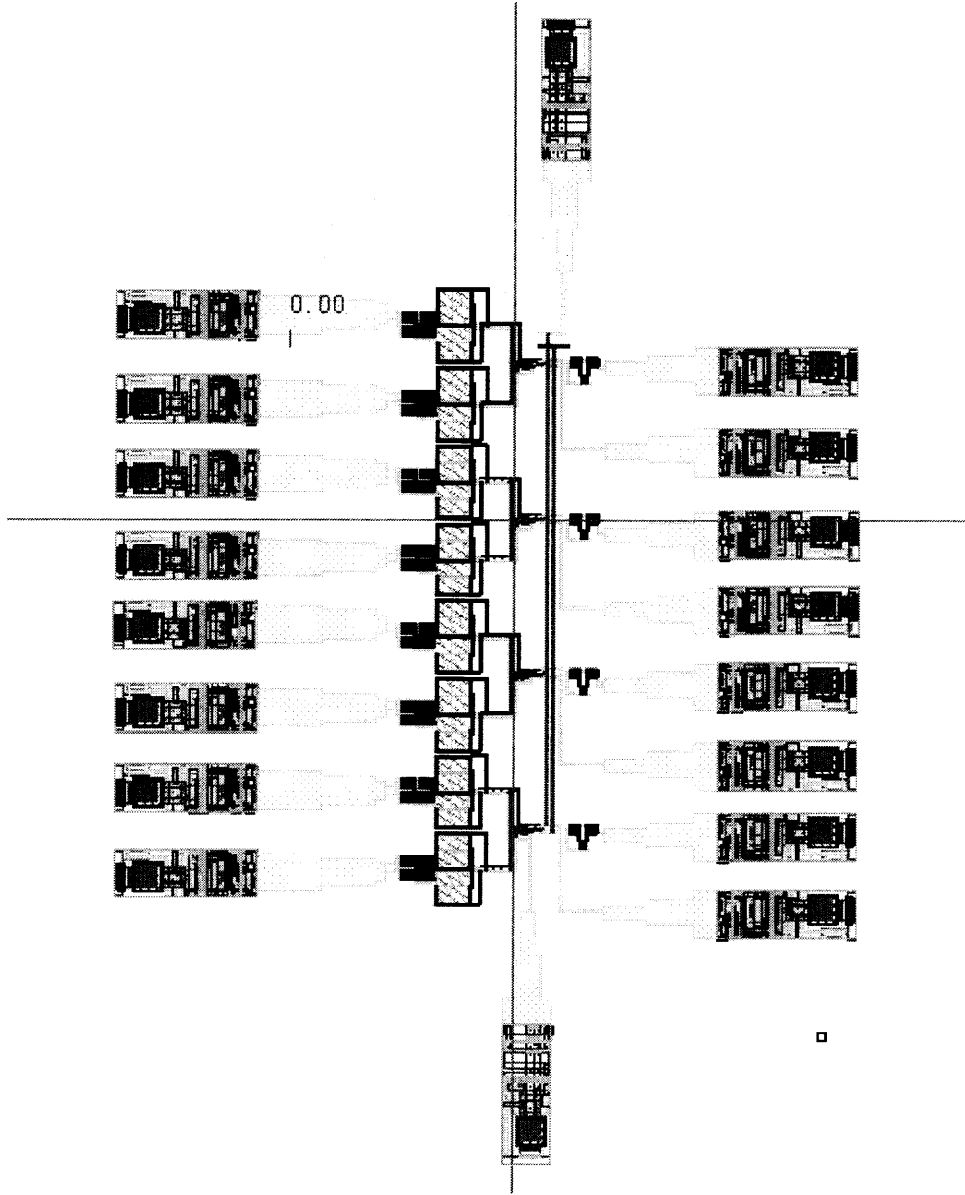
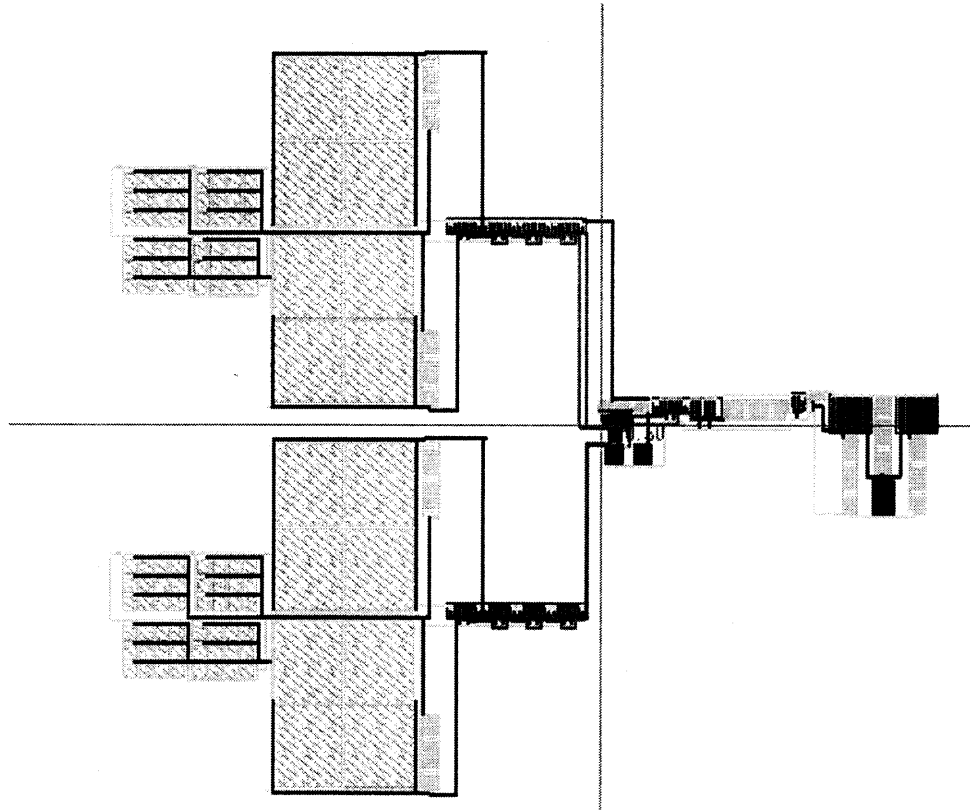**Figure 4.24** Layout of Complete Interface Chip.

Figure 4.25 Layout of Single Interface Circuit.

4.8.1 Analysis of the Results

The complete circuit is simulated in HSPICE. Two input signals with a frequency a difference of 500 Hz is fed to the circuit and the resultant response for a period of 20 ms is shown in Figure 4.26. It can be seen from Figure 4.26 that the response of the Interface circuit for a frequency difference of 500 Hz between the two input signals is a series of pulses.
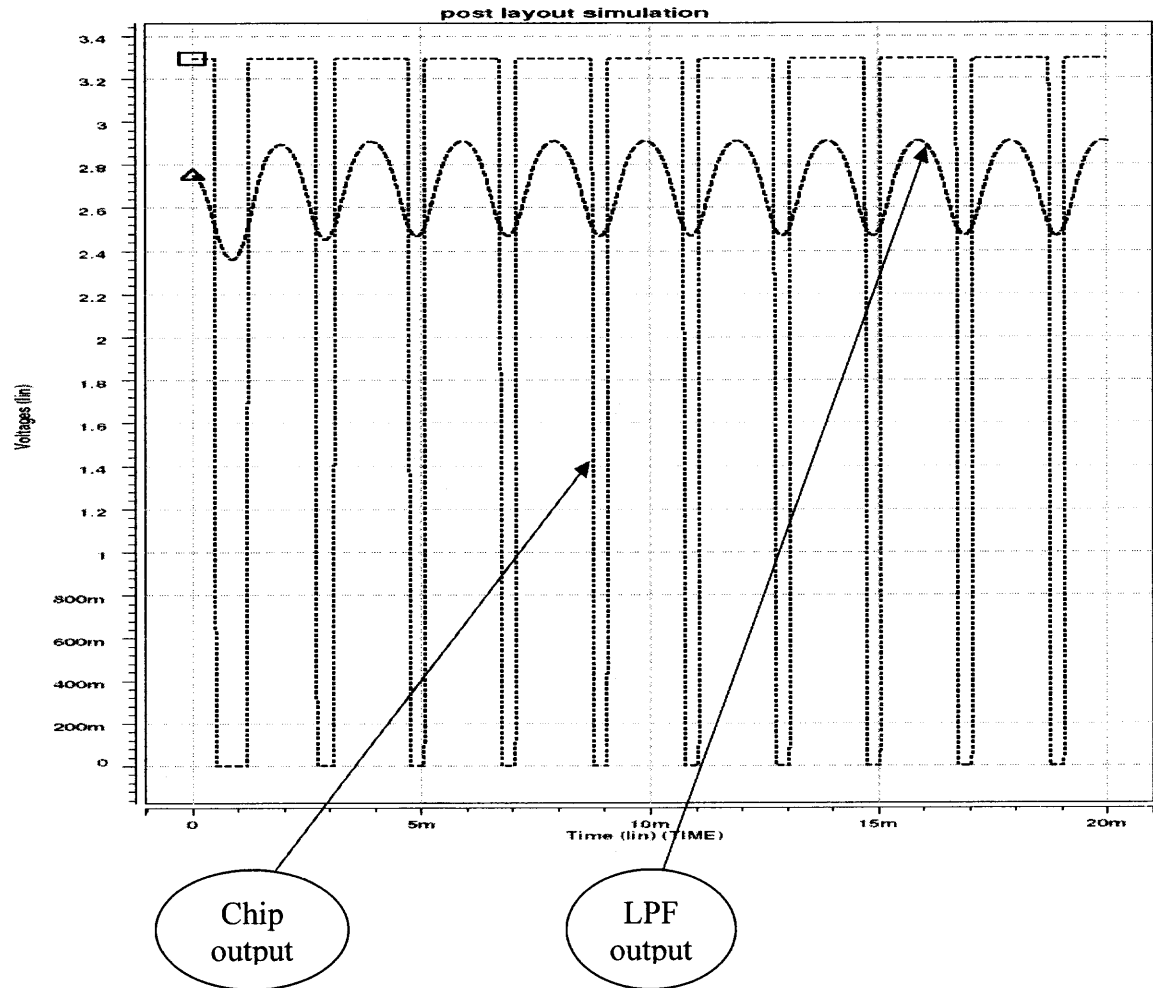
Figure 4.26 Post Layout Transient Response for a Frequency Difference of 500 Hz at the Input of the Interface Circuit.

Similarly the transient response of the interface circuit for frequency difference of 600 Hz, 700 Hz, 800 Hz, 900 Hz and 1KHz, 2 KHz, 3 KHz are shown in Figures 4.27, 4.28, 4.29, 4.30, 4.31, 4.32 and 4.33, respectively. It can be seen that the output swings of the interface circuit is reducing as the frequency difference at the input is increasing. For a frequency difference of 900 Hz and more the output transient response is a constant zero.
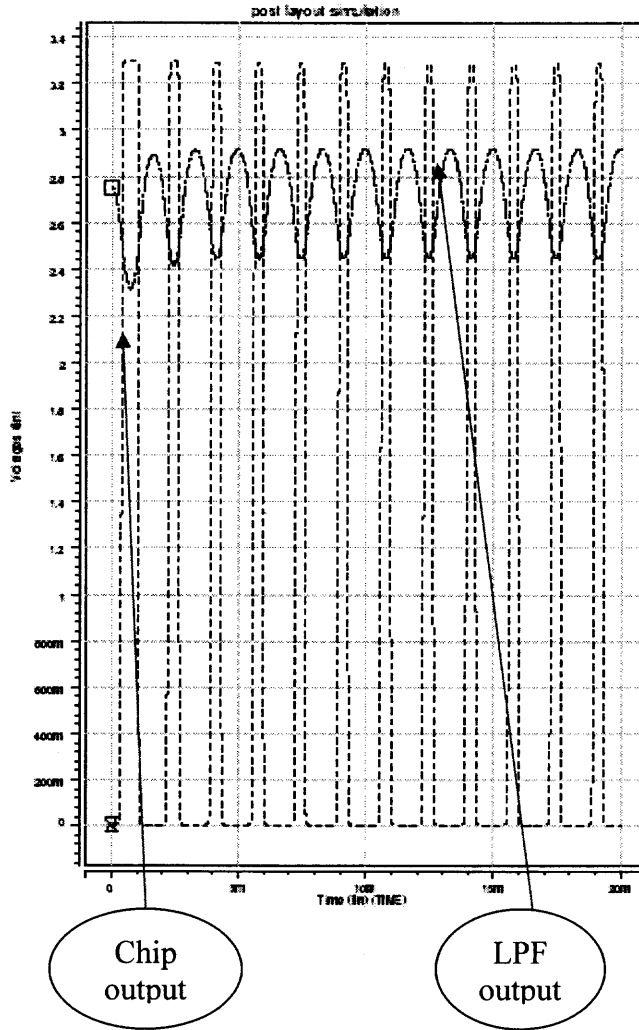
Figure 4.27 Post Layout Transient Response for a Frequency Difference of 600 Hz at the Input of the Interface Circuit.

Figure 4.28 Post Layout Transient Response for a Frequency Difference of 700 Hz at the Input of the Interface Circuit.

Figure 4.29 Post Layout Transient Response for a Frequency Difference of 800 Hz at the Input of the Interface Circuit.

Figure 4.30 Post Layout Transient Response for a Frequency Difference of 900 Hz at the Input of the Interface Circuit.

Figure 4.31 Post Layout Transient Response for a Frequency Difference of 1 KHz at the Input of the Interface Circuit.
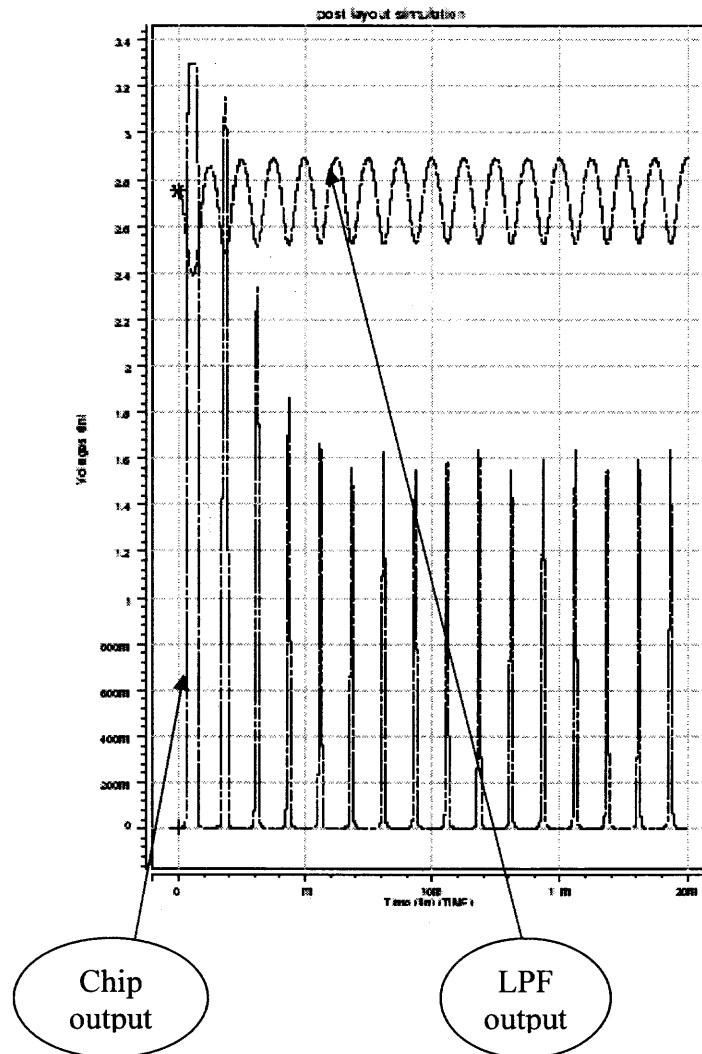
Figure 4.32 Post Layout Transient Response for a Frequency Difference of 2 KHz at the Input of the Interface Circuit.
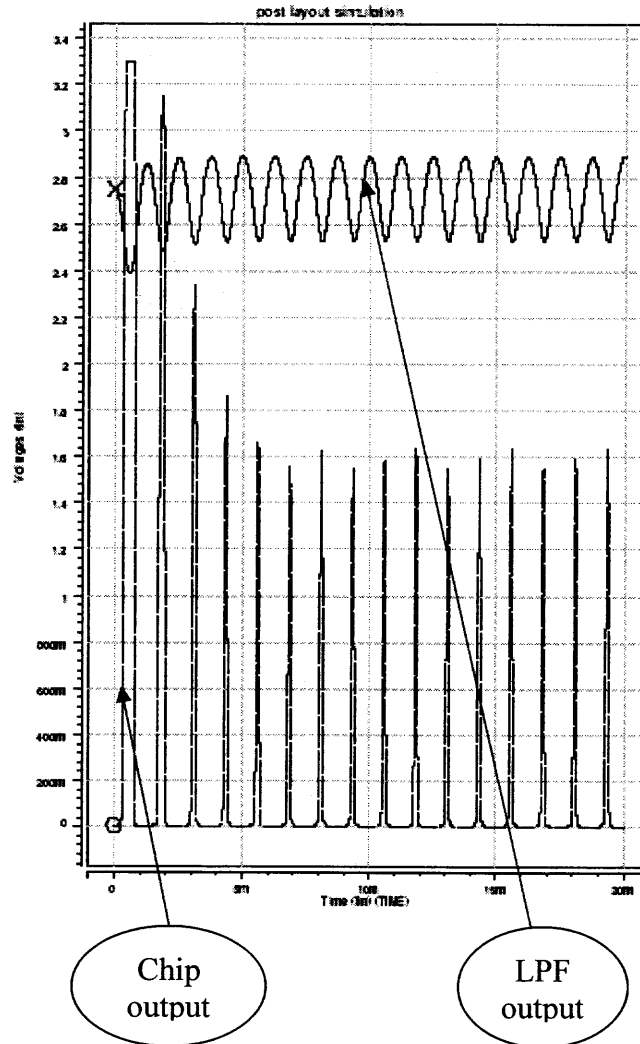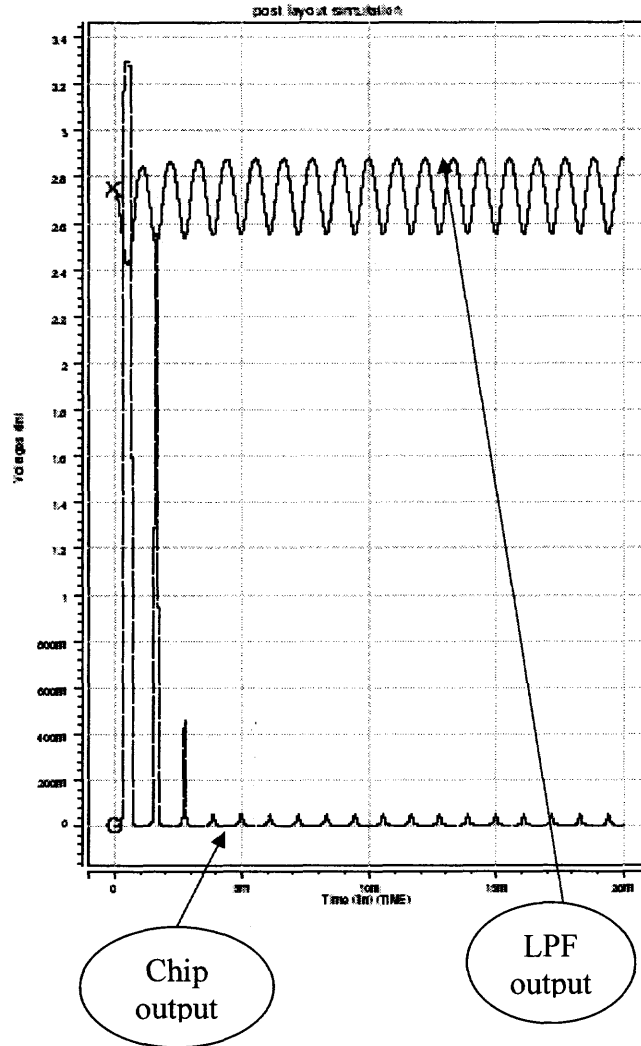
Figure 4.33 Post Layout Transient Response for a Frequency Difference of 3 KHz at the Input of the Interface Circuit.

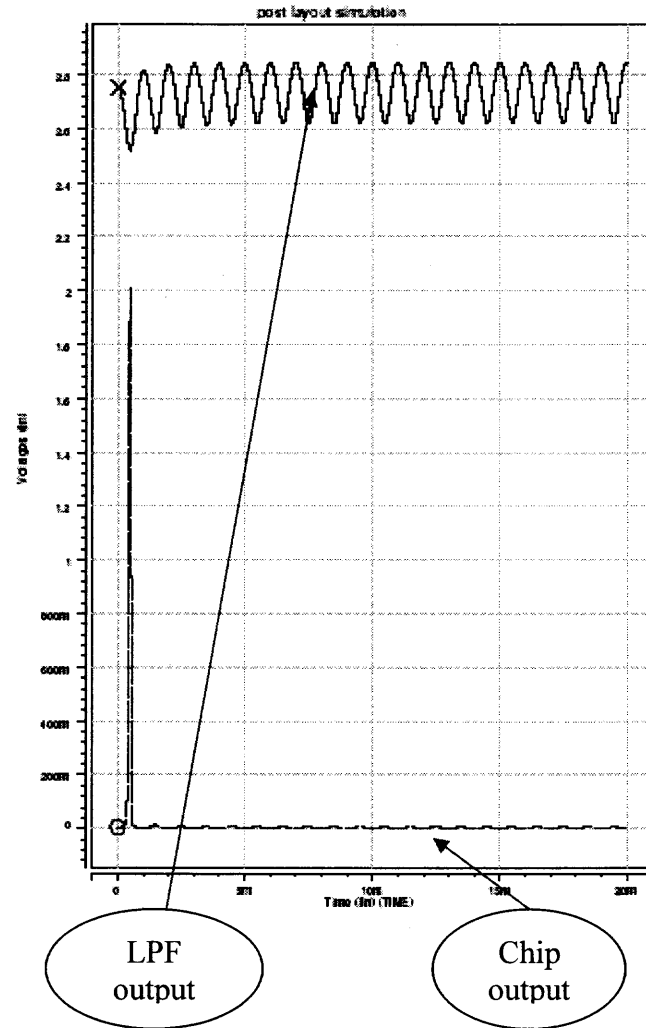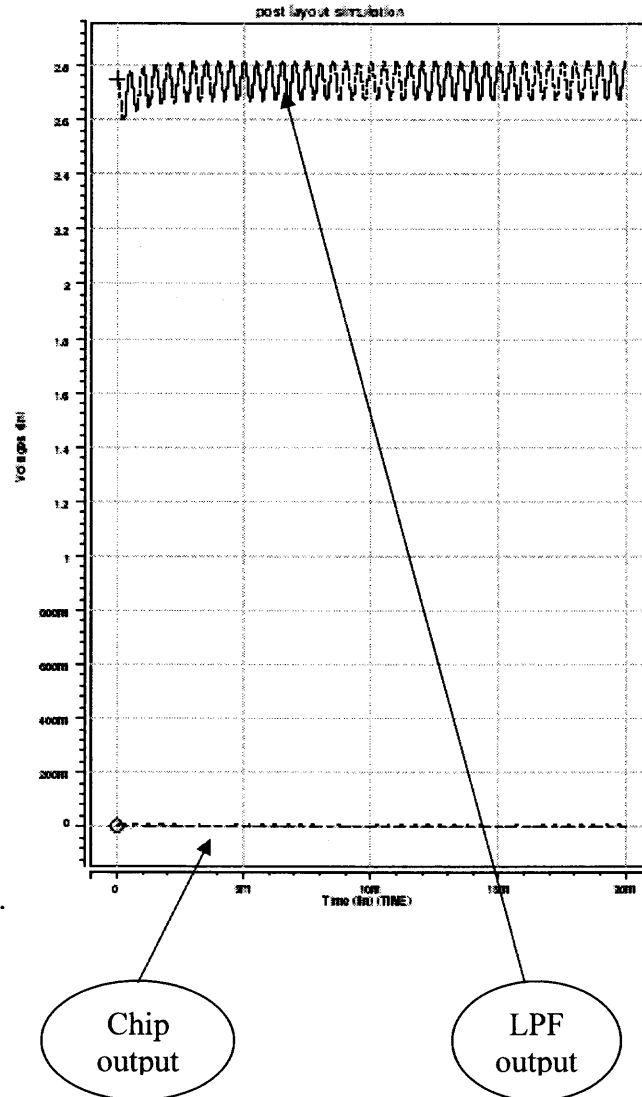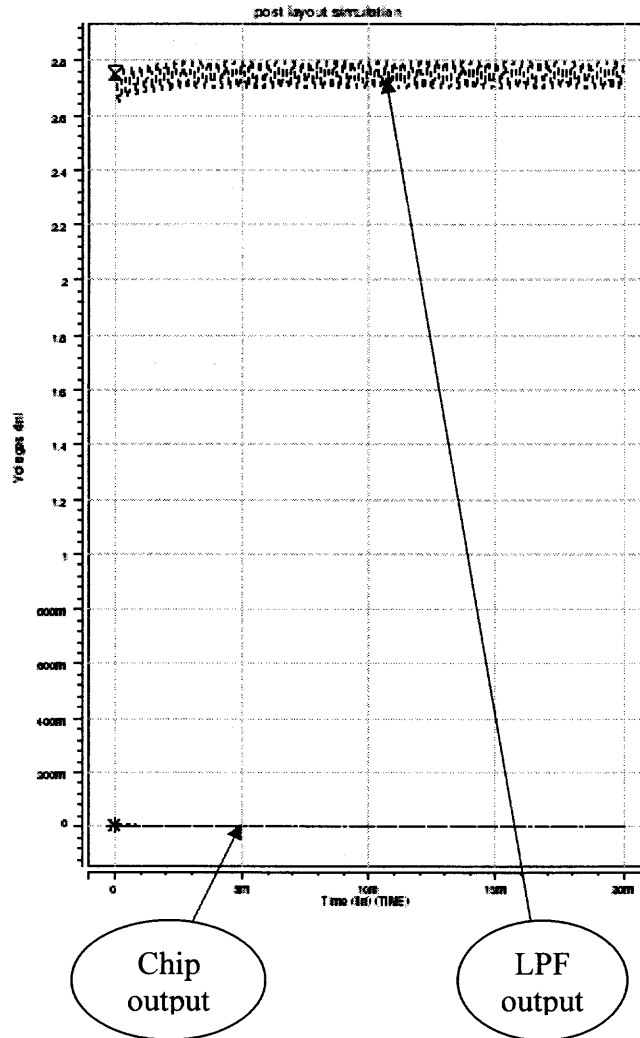The graph showing the variation in amplitude of the pulses with respect to the frequency shift at the input of the interface circuit is shown in Figure 4.34.
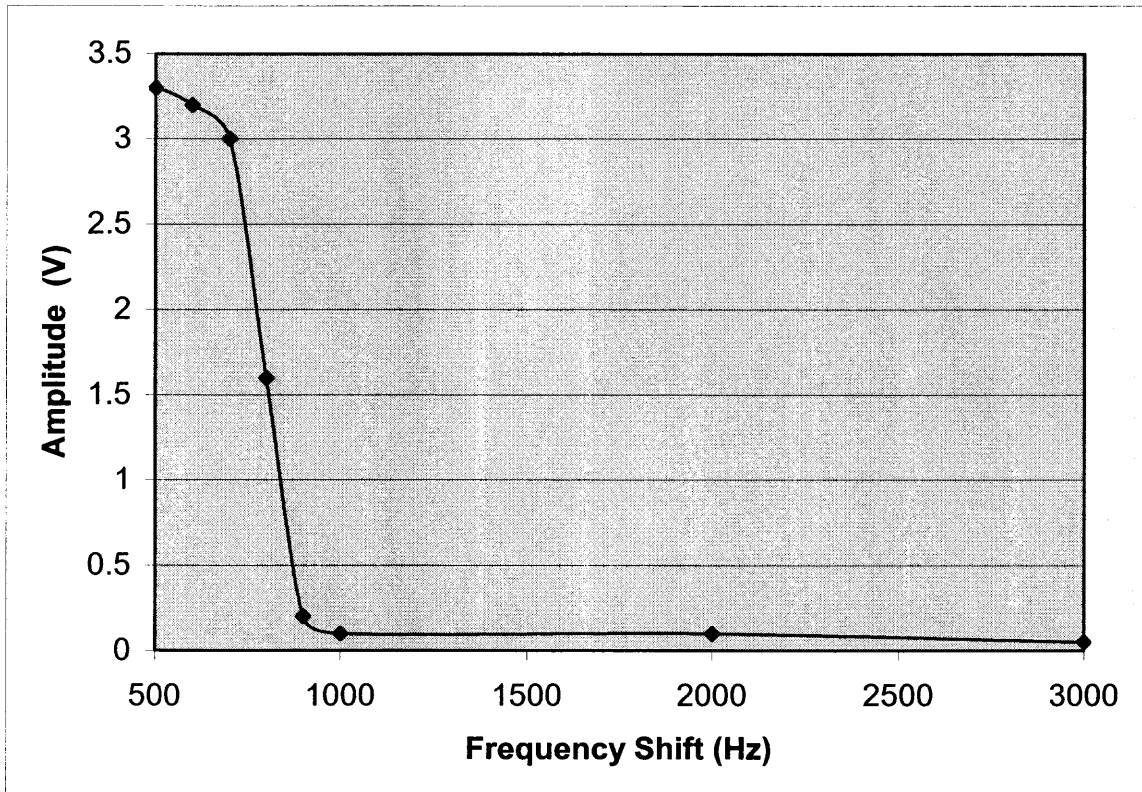

Figure 4.34 Amplitude of the Pulses at the Output of the chip
Versus Frequency shift at the input.

CHAPTER 5

CONCLUSIONS

The interface chip detects the frequency shift as a function of the chemical species absorbed by the sensor and alerts the ad hoc network controller when the concentration of a vapor exceeds some threshold, based on local processing and measurements. System components are designed in an RF environment to carry out the local processing and estimation of the chemical absorbed. Simulation results for individual circuit components as well as the complete chip outline the robust performance of the system that improves chemical target detection and reduce false alarms. The design takes into account a sensor system with eight chemical SAW sensors operating at a resonant frequency of 1 GHz and an attenuation of 30 dB. The interface circuit can detect the critical change in the chemical vapor concentration in the atmosphere through a SAW based chemical sensor. The interface circuit compares the output signals from the exposed and unexposed chemical sensors and an alert signal is generated for frequency shift greater than 1 KHz. It is also designed to produce no alert signal for a frequency shift less than 500 Hz. The interface circuit can monitor four different chemical vapors. The power consumption of the chip is about 400 µW. The power consumption of the chip can be reduced by scaling the design to 0.18 or .13 µ technology. The circuit performance can be improved by replacing the resistors with MOS-transistors.

The interface circuit can be used in wireless integrated network system architecture to build a robust sensor network.

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