New Jersey Institute of Technology
Digital Commons @ NJIT

Theses | Theses and Dissertations

Spring 2004

Study of design tradeoffs of DRAM and SRAM memories, using HSPICE computer simulation

Bageshri Kale
New Jersey Institute of Technology

Follow this and additional works at: https://digitalcommons.njit.edu/theses

 Part of the Electrical and Electronics Commons

Recommended Citation
Kale, Bageshri, "Study of design tradeoffs of DRAM and SRAM memories, using HSPICE computer simulation" (2004). *Theses*. 551.
https://digitalcommons.njit.edu/theses/551

This Thesis is brought to you for free and open access by the Theses and Dissertations at Digital Commons @ NJIT. It has been accepted for inclusion in Theses by an authorized administrator of Digital Commons @ NJIT. For more information, please contact digitalcommons@njit.edu.

Copyright Warning & Restrictions

The copyright law of the United States (Title 17, United States Code) governs the making of photocopies or other reproductions of copyrighted material.

Under certain conditions specified in the law, libraries and archives are authorized to furnish a photocopy or other reproduction. One of these specified conditions is that the photocopy or reproduction is not to be "used for any purpose other than private study, scholarship, or research." If a, user makes a request for, or later uses, a photocopy or reproduction for purposes in excess of "fair use" that user may be liable for copyright infringement,

This institution reserves the right to refuse to accept a copying order if, in its judgment, fulfillment of the order would involve violation of copyright law.

Please Note: The author retains the copyright while the New Jersey Institute of Technology reserves the right to distribute this thesis or dissertation

Printing note: If you do not wish to print this page, then select "Pages from: first page # to: last page #" on the print dialog screen

NJIT New Jersey's Science & Technology University

The Van Houten library has removed some of the personal information and all signatures from the approval page and biographical sketches of theses and dissertations in order to protect the identity of NJIT graduates and faculty.

ABSTRACT

STUDY OF DESIGN TRADEOFFS OF DRAM AND SRAM MEMORIES, USING HSPICE COMPUTER SIMULATION

by

Bageshri Kale

Semiconductor random access memories are complex systems that can be described by performance parameters such as memory cycle time, access delays, storage capacity, bit packing density, chip area and retention time. In this thesis, tradeoffs between cycle time, chip area, and storage size as reflected by bit line capacitance (Cbl) were studied as a function of particular design variables: memory cell capacitance (Cc); CMOS flip-flop sense amplifier (SA) transistor sizes; and size of precharge (PC), and word line (WL) switches. Performance was optimized using circuit simulation software, HSPICE, to observe DRAM and SRAM waveforms. With TSMC 0.18 micron technology, minimum cycle times of 2.11ns (DRAM) and 1.18ns (SRAM) were achieved (Cbl = 100FF), by optimizing the k_r values of the SA transistors, for a fixed SA area of 1 μm^2, and finding the optimum PC switch width (1.6μm).To maintain the same cycle time when the Cbl of both SRAM and DRAM increased by N, the required total chip area was found to be increased by N^2. For a constant memory capacity, the ratio of the change in the sense amplifier area to the change in memory cycle time for DRAM was found to be between 1.25 to three times that of SRAM, varying somewhat with cycle time. To optimize SRAM cycle time, the criteria of a bit line difference of 10% of 3V determined the time to terminate the connection of the bit line to the SRAM cell so as to avoid the loading of the parasitic Cc cell by the larger Cbl.

STUDY OF DESIGN TRADEOFFS OF DRAM AND SRAM MEMORIES, USING HSPICE COMPUTER SIMULATION

by

Bageshri Kale

A thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering

Department of Electrical and Computer Engineering

May 2004

APPROVAL PAGE

STUDY OF DESIGN TRADEOFFS OF DRAM AND SRAM MEMORIES, USING HSPICE COMPUTER SIMULATION

Bageshri Kale

Dr. Roy Cornely, Thesis Advisor — Date
Professor of Electrical and Computer Engineering, NJIT

Dr. Durgamadhab Misra, Committee Member — Date
Professor of Electrical and Computer Engineering, NJIT

Dr. Marek Sosnowski, Committee Member — Date
Professor of Electrical and Computer Engineering, NJIT

Dr. Leonid Tsybeskov, Committee Member — Date
Associate Professor of Electrical and Computer Engineering, NJIT

BIOGRAPHICAL SKETCH

Author: Bageshri Kale

Degree: Master of Science

Date: May 2004

Undergraduate and Graduate Education:

- Master of Science in Electrical Engineering,
  New Jersey Institute of Technology, Newark, NJ, 2004

- Bachelor of Science in Electronics and Telecommunication Engineering,
  Cummins College of Engineering for Women, Pune, India, 2000

Major: Electrical Engineering

This thesis is dedicated to my family and my fiancée whose constant love and support helped me throughout my graduate studies.

ACKNOWLEDGMENT

From the formative stages of this thesis to the final draft, I owe an immense debt of gratitude to my advisor, Dr. Roy Cornely. His sound advice and careful guidance were invaluable during the course of my research for this thesis. I would also like to thank Dr. Durgamadhab Misra, Dr. Leonid Tsybeskov, and Dr. Marek Sosnowski for being part of the thesis evaluation committee and for their suggestions and comments. I want to thank Mr. James Dawson and John Davis from IBM, and Mr. Philip Diodato from Lucent, for their valuable guidance.

Finally, sincere thanks and appreciation to my parents, friends and family members for their constant moral support and help throughout my course of study.

Last, but not the least, my heartfelt thanks to my beloved Amit, without whose love and help, I would have never made it this far.

TABLE OF CONTENTS

TABLE OF CONTENTS
(Continued)

LIST OF FIGURES

LIST OF FIGURES
(Continued)

LIST OF FIGURES
(Continued)

LIST OF FIGURES
(Continued)

LIST OF FIGURES
(Continued)

LIST OF TABLES

LIST OF TABLES
(Continued)

CHAPTER 1

INTRODUCTION

1.1 Motivation

The study of semiconductor memories has been an important aspect of semiconductor technology. In the past three decades, engineers have strived to invent different types of memories and to improve their performance. Various performance criteria for memories are low cost, high performance, high density (less chip area), latency, low power dissipation, non-volatility, memory capacity and memory size. To improve the memory performance, it is very important to understand the tradeoffs between these performance criteria.

Of the different types of memories, MOS memories are dominating the memory market today. These fall into two categories – Read/Write Memories [Dynamic Random Access Memories (DRAM) and Static Random Access Memories (SRAM)] and Read Only Memories (ROMs). This thesis was initiated to obtain a better understanding of why some memory manufacturers in Japan have emphasized DRAM while those in USA have emphasized SRAM. The author was curious about the advantages and disadvantages of the two memory approaches.

1.2 Objectives

This work presents the design tradeoffs between the three most important performance parameters for both DRAM and SRAM Memories. These parameters are the memory cycle time which is the time between subsequent memory operations, packing density

described in terms of the space consumed on the chip by the memory and the memory size in terms of number of bits. Each of these parameters can be effectively controlled by the memory designer by controlling various device and circuit variables.

1.3 Background

The DRAM and SRAM allow the user both to read information from memory and to write new information into the memory while it is still in the system. The various components of the memory system include an array of memory cells, decoders and drivers to access a particular cell from the entire memory array and sense amplifiers to read the information stored in the cell (and to restore its information in case of DRAM). The memory array contains columns (bit lines) and rows (word lines). The intersection of a bit line and a word line constitutes a memory cell address. To select a particular memory cell from the array, initially a row is selected by activating a word line corresponding to the address and then a column is selected by activating the bit line. Data can then be written into or read from that memory cell.

Information is stored in DRAM by the presence or absence of charge on a memory capacitor, whereas in SRAM it is stored as a four transistor flip-flop state. The main difference amongst the two is that the DRAM memory capacitor loses its charge over a period of time and hence, DRAM memory has to be refreshed periodically. This increases the memory cell recovery time of DRAM. The SRAM does not lose its information as long as the power supply is kept on, but gains its speed at the cost of its chip area consumed per bit. The DRAM is more cost effective as compared to SRAM,

since due to its small size, its packing density is more and hence the number of bits stored in a chip area is more.

In order to read a memory cell, the word line switch transistor is turned on. The charge on the memory cell is shared with the bit line. This causes a reduction in the signal level and hence, a sensitive sense amplifier is required to detect this charge. A flip-flop is used as a sense amplifier throughout the thesis.

This thesis focuses on optimization of the memory cell and sense amplifier design. The variables used to optimize the design are widths and lengths of the transistors in the sense amplifier, precharge switch, memory cell access switch, memory capacitance, bit line capacitance and the k_r ratio of the invertors in the sense amplifier.

A circuit simulation software, HSPICE, has been used to simulate the memory behavior. Various design variables such as the width and length values for various transistors, memory cell and bit line capacitances are varied using HSPICE. CMOS 0.18μm technology has been used for describing the transistors, as this is now the industry standard. The input file for HSPICE describes the memory system, and on simulating this input file, an output file is generated. This output can be viewed graphically by using a post processor, AWAVES. Thus, performance goals as the cycle time can be measured and compared for variable design parameter values.

1.4 Organization of Thesis

Chapter 2 describes the experimental setup. Chapter 3 presents the experimental results and Chapter 4, the experimental data obtained have been analyzed and tradeoffs have been discussed. In Chapter 5, conclusions are drawn based on the experiments.

CHAPTER 2

EXPERIMENTAL APPROACH

2.1 DRAM

During the design of the memory system, emphasis was placed on optimizing the design of the DRAM memory cell and the sense amplifier. The one transistor and capacitor memory cell was selected for the DRAM memory cell as it is the industry standard. A circuit that either detects a change in voltage or a change in current could be chosen as a sense amplifier. Here a simple flip-flop sense amplifier that detects a change in voltage, ΔV, has been selected. This sense amplifier has very low power dissipation. The figure below shows the circuit configuration for the DRAM Memory Cell, along with the bit lines, word lines, the sense amplifier, the dummy memory cell and the pre-charge signal.

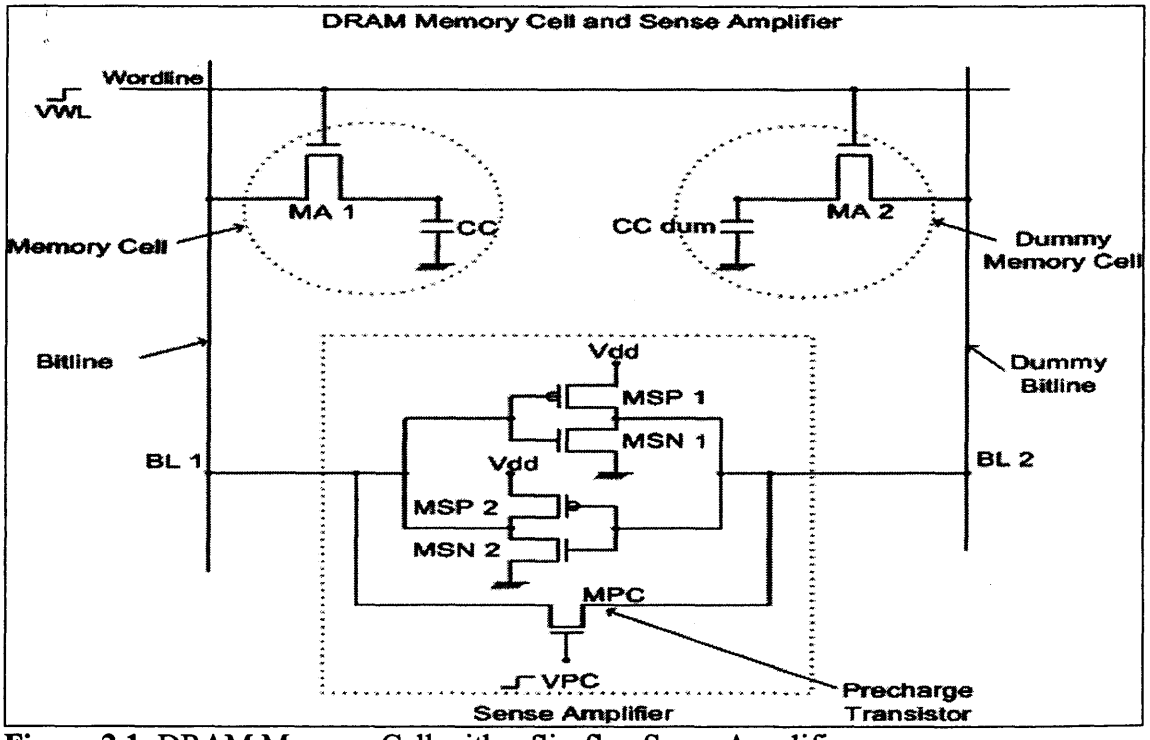


Figure 2.1 DRAM Memory Cell with a flip-flop Sense Amplifier.

The circuit above was simulated using HSPICE. The HSPICE template used to describe it is shown below

```
DRAM
.options list node post
VPC 2 0 DC 0 PULSE(0 3 0NS 0.001NS 0.001NS  0.6NS 5NS)
VWL 6 0 DC 0 PULSE(0 3 0.6NS 0.001NS 0.001NS 4.4NS 5NS)
VDD 3 0 DC 3
CBL1 5 0 100FF
CBL2 4 0 100FF
*STORAGE CELL
MA1 5 6 1 0 NCH W=0.3U L=0.2U
CC 1 0 50FF
MA2 4 6 7 0 NCH W=0.3U L=0.2U
CCdum 7 0 50FF
*SENSE AMPLIFIER
MSN1 4 5 0 0 NCH W=0.952U L=0.18U
MSP1 4 5 3 3 PCH W=2U L=0.18U
MSN2 5 4 0 0 NCH W=0.952U L=0.18U
MSP2 5 4 3 3 PCH W=2U L=0.18U
MPC 5 2 4 0 NCH W=1.62U L=0.18U
*
.OP
.TRAN 0.01NS 10ns start=5NS
.INCLUDE PCH.M
.INCLUDE NCH.M
.PROBE V(1) V(2) V(3) V(4) V(5) V(6) V(7)
.END
```

Figure 2.2 HSPICE file template for DRAM.

The memory cell capacitance, "CC", is connected to bit line "CBL1" using the word line switch transistor "MA1". The sense amplifier consists of two invertors connected back to back. Transistors "MSN1" and "MSP1" form one inverter, "MSN2" and "MSP2" form the other inverter. A dummy memory cell "CCdum", word line switch "MA2" and dummy bit line "CBL2" are used to balance the sense amplifier. To get both

bit lines to have the same voltage, a pulse "VPC" is applied to the pre charge transistor "MPC". After the bit lines voltages are merged, "VPC" goes low and a pulse, "VWL", is applied at the gate of the word line switches, thus switching on the access transistors. The charge stored in the memory cell capacitor is shared with the bit line, causing the voltage on the bit line to change. The same operation is performed on the dummy memory cell. This generates a differential voltage, ΔV, on the bit line pair which is applied to the sense amplifier for amplification. An analysis of the charge sharing between Cc and Cbl that occurs when the word line switch goes high, under the assumption of an ideal word line switch results in equation 2.1.

$$\Delta V = \frac{Vc-Vbl}{1+Cbl/Cc} \qquad (2.1)$$

Referring to Equation 2.1, Vc is the initial voltage on the memory cell, Vbl is the common voltage to which the bit lines are pre charged, Cbl is the bit line capacitance and Cc is the memory cell capacitance.

The CMOS 0.18μm technology was used to describe all the transistors in use. All N Channel transistors have been described using the model file "NCH.M" and P Channel transistors using the model file "PCH.M" The lengths of all transistors were restricted to 0.18μm and 3V power supply was used in all the experiments. Initially, memory cell capacitance value (Cc) was chosen as 50ff and bit line capacitance value (Cbl1 and Cbl2) as 100ff so that enough ΔV was generated for the sense amplifier.

The width (W)/length (L) ratio of the access switches was kept at 0.3μm/0.2μm. The W values of the sense amplifier and pre charge (PC) transistors were varied such that

minimum memory cycle time was achieved. The chosen Wn = 0.952μm, Wp = 2 μm giving k_r = 0.476. PC width = 1.62 μm, giving a total sense amplifier area of 1.35μm^2.

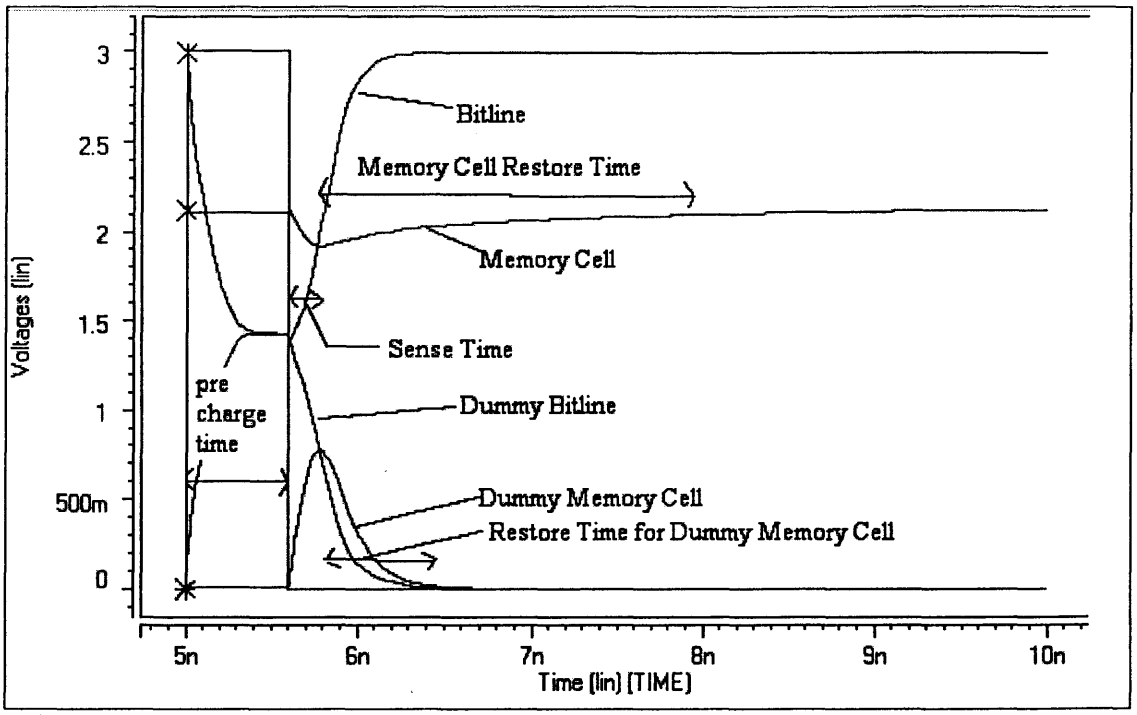


Figure 2.3 Figure showing various times such as memory cycle time and bit line recovery time. Components of the memory cycle time – pre charge time, read and restore time.

As can be seen in Figure 2.3, the memory cycle time consists of the pre charge time and the memory cell recovery time (for DRAM). For SRAM, it is equal to the PC time plus the worst case recovery time. The worst case recovery time is the maximum recovery time of the "1" cell, the "0" cell, the bit line and the dummy bit line. The pre charge time is the time required to merge the two bit lines to the same voltage value. Memory cell recovery time consists of the time required by the sense amplifier to read the charge on the memory cell and the time required to restore the memory cell to its initial value. All times have been measured by considering 0% to 99% swing of the voltage waveform.

2.2 SRAM

The difference between SRAM and DRAM lies in their memory cell structure. The SRAM memory cell gets its static nature because of the cross coupled four transistor flip-flop it uses. The circuit configuration for SRAM is shown in Figure 2.4 below. An SRAM memory cell uses two invertors connected back to back. Data are stored in this flip flop latch as a "1" state or a "0" state. When a high voltage (3V) is present on the left node (connected to access transistor MA1) of the flip-flop and a low voltage (0V) on the right node (connected to access transistor MA2), a "1" is present and when a high voltage (3V) is present on the right node and low voltage (0V) on the left node, a "0" is present. Memory access transistors MA1 and MA2 are used to connect the memory cell to the bit line BL1 and dummy bit line BL2. Other than the memory cell structure, all other components remain the same as DRAM.

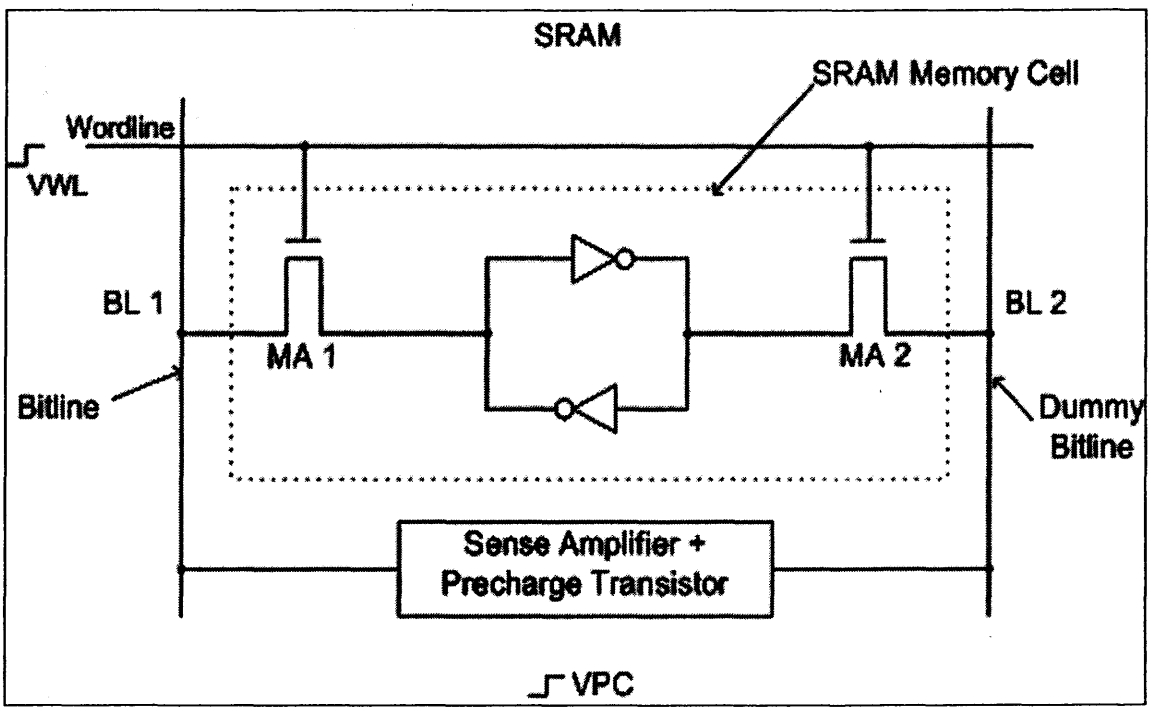


Figure 2.4 SRAM Memory Cell with a flip-flop Sense Amplifier.

The HSPICE file used to describe the circuit in Figure 2.4 is given below

```
SRAM -
.options list node post
vpc 7 0 dc 0 pulse(0 3 0ns 0.01ns 0.01ns 1.5ns 5ns)
vwl 6 0 dc 0 pulse(0 3 1.5ns 0.01ns 0.01ns 3.5ns 5ns)
vdd 3 0 dc 3
cbl1 4 0 100FF
cbl2 5 0 100FF
*storage cell
MCN1 2 1 0 0 NCH W=0.245U L=0.18U
MCP1 2 1 3 3 PCH W=0.2U L=0.18U
MCN2 1 2 0 0 NCH W=0.245U L=0.18U
MCP2 1 2 3 3 PCH W=0.2U L=0.18U
MA1 4 6 2 0 NCH W=0.3U L=0.2U
MA2 5 6 1 0 NCH W=0.3U L=0.2U
*SENSE AMPLIFIER
MSN1 4 5 0 0 NCH W=0.6U L=0.18U
MSP1 4 5 3 3 PCH W=2.5U L=0.18U
MSN2 5 4 0 0 NCH W=0.6U L=0.18U
MSP2 5 4 3 3 PCH W=2.5U L=0.18U
MRS 5 7 4 0 NCH W=1.6U L=0.18U
*
.OP
.TRAN 0.001NS 5NS
.NODESET V(1)=3 V(2)=0
.INCLUDE PCH.M
.INCLUDE NCH.M
.PROBE V(1) V(2) V(3) V(4) V(5) V(6) V(7)
.END
```

Figure 2.5 HSPICE file template for SRAM.

Transistor MCN1 and MCP1 form one invertor and MCN2 and MCP2 form the other invertor of the memory cell. The dimensions chosen for the memory cell transistors are – N Channel = 0.245um/0.18um, P Channel = 0.2um/0.18um. At these values, the charge sharing voltage dip in the "1" and "0" memory cell waveforms are observed to be

equal. The dimensions chosen for the sense amplifier transistors are – N Channel = 0.6um/0.18um, P Channel = 2.5um/0.18um. Using these values, $k_r = 0.24$ and bit line and dummy bit line show perfect symmetry in recovery time.

2.3 Basic Experiments

Performance goals for DRAM and SRAM memories are controlled by design variables. These design variables include the W/L ratio of the pre charge transistor, the value of Cbl, the W/L ratio of the transistors in the sense amplifier, the k_r ratio of the invertors in the sense amplifier, the value for Cc in case of DRAM, the W/L ratio of the transistors in the memory cell (for SRAM), the k_r ratio of the invertors in the memory cell (for SRAM) and the W/L ratio of the word line switch transistors. The effect of these parameters on the performance goals can be observed by designing a set of experiments in which each of these variables are varied and their influence on one or more performance goals is observed.

2.3.1 W/L Ratio of the Pre Charge Transistor

Objectives – The objective of this experiment was to observe in which way the pre-charge transistor W/L effects the pre-charge time, the bit-line recovery and memory cycle times. It is expected that as width of PC increases, the current flowing through PC transistor increases and hence the time required to merge the bit lines should reduce resulting in a reduction in the recovery time.

Experimental Setup and Parameters varied –

The DRAM – PC transistor L was kept at 0.18μm and W was varied from 0.9μm to 1.98μm. All other parameter values were as follows – Cbl = 100ff, Cc = 50ff, Pass

Switch = 0.3/0.2μm, Sense amplifier – Wn = 0.952μm, Ln = 0.18μm, Wp = 2μm, Lp = 0.18μm, k_r = 0.476.

The SRAM – PC transistor L was kept at 0.18μm and W was varied from 1.2μm to 1.8μm. All other parameters values were as follows – Cbl = 100ff, Pass Switch = 0.3/0.2μm, Memory Cell – Ln = Lp = 0.18μm, Wn = 0.245μm, Wp = 0.2μm, Sense amplifier – Wn = 0.6μm, Ln = 0.18μm, Wp = 2.5μm, Lp = 0.18μm, k_r = 0.24.

2.3.2 Bit line length (Cbl value)

Objectives – To observe the effect of varying the length of the bit line and thus the bit line capacitance (Cbl), on the bit lines and the memory cell recovery time. As the total memory size increases, the total length of the bit line increases, which leads to an increase in the bit line capacitance value. This experiment is performed to observe the effect that Cbl (and hence memory size) has on the system.

Referring to Equation 2.1, Vc depends upon the supply voltage and threshold voltage of the word line switch. Vbl depends on the k_r value of the invertors in the sense amplifier. Since these are held constant, Vc-Vbl is constant. Hence, as Cbl is increased, Vc and Vbl being constant, ΔV should reduce. With the reduction in ΔV, it should take more time for the sense amplifier to restore the memory cell and bit lines to their initial value. Thus, recovery time and cycle time should increase. Also, as Cbl is increased, it should take more time for the bit lines voltages to merge together.

Experimental setup and parameters varied –

The DRAM – The Cbl value was varied from 50 ff to 1000 ff. All other parameter values were as follows – Cc = 50ff, Pass Switch = 0.3/0.2μm, Sense amplifier – Wn = 0.952μm, Ln = 0.18μm, Wp = 2μm, Lp = 0.18μm, k_r = 0.476, PC Switch = 1.62μm /0.18μm.

The SRAM – The Cbl value was varied from 50 ff to 1000 ff. All other parameter values were as follows – Pass Switch = 0.3/0.2μm, Memory Cell – Ln = Lp = 0.18μm, Wn = 0.245μm, Wp = 0.2μm, Sense amplifier – Wn = 0.6μm, Ln = 0.18μm, Wp = 2.5μm, Lp = 0.18μm, k_r = 0.24, PC Switch = 1.62μm /0.18μm.

2.3.3 W/L Ratio of Sense Amplifier Transistors Keeping k_r Constant

Objectives – To observe the effect of increasing the sensitivity of the sense amplifier on the memory cycle time and the bit line recovery time. The sensitivity of the sense amplifier can be increased by increasing the W/L ratio of the transistors in the sense amplifier. The area of the sense amplifier is given by

Area = $WL_{N1} + WL_{N2} + WL_{P1} + WL_{P2}$ + non transistor area

Due to an increase in the W/L ratio of the transistors in the sense amplifier, the area of the sense amplifier unfortunately increases. The objective of this experiment is to study the tradeoff between the sense amplifier area and the memory cycle time.

Experimental setup and parameters varied – W/L ratio of transistors in the sense amplifier was varied, keeping all other parameters constant as follows –

The DRAM – Sense amplifier: Ln = Lp = 0.18μm. Wn was varied from 0.238μm to 1.666μm and Wp was varied from 0.5μm to 3.5μm, such that k_r was constant at 0.476.

All other variable values were kept constant as follows – Cbl = 100ff, Cc = 50ff, Pass Switch = 0.3/0.2μm, PC Switch = 1.62μm /0.18μm.

The SRAM – Sense amplifier: Ln = Lp = 0.18μm. Wn was varied from 0.192μm to 0.84μm and Wp was varied from 0.8μm to 3.5μm, such that k_r was constant at 0.24. All other variable values were kept constant as follows – Cbl = 100ff, Pass Switch = 0.3/0.2μm, PC Switch = 1.62μm /0.18μm, Memory Cell – Ln = Lp = 0.18μm, Wn = 0.245μm, Wp = 0.2μm.

2.3.4 Variation of the k_r Ratio of the Sense Amplifier Transistors Keeping Wn Constant

Objectives – To observe the effect of varying k_r on performance goals. As k_r is varied, the unstable operating point voltage for the bit lines varies. This results in variance in the bit line and memory cell recovery time and also the PC time. In this experiment Wn was kept constant, and Wp was varied to vary k_r. The PMOS affects the bit line. As Wp is increased, the bit line recovery time should be reduced.

Experimental setup and parameters varied –

The DRAM – Value of Wp was varied, such that k_r was varied from 0.25 to 3 and all other parameters were kept constant as follows – Cbl = 100ff, Cc = 50ff, Pass Switch = 0.3μm /0.2μm, Sense amplifier – Wn = 0.952μm, Ln = 0.18μm, Lp = 0.18μm, PC Switch = 1.62μm /0.18μm.

The SRAM – Value of Wp was varied, such that k_r was varied from 0.2 to 0.7 and all other parameters were kept constant as follows – Cbl = 100ff, Pass Switch = 0.3/0.2μm, Memory Cell – Ln = Lp = 0.18μm, Wn = 0.245μm, Wp = 0.2μm, Sense amplifier – Ln = Lp = 0.18μm, Wn = 0.6μm, PC Switch = 1.6μm /0.18μm.

2.3.5 Variation of the k_r Ratio of the Sense Amplifier Transistors Keeping Wp Constant

Objectives – The k_r ratio of the transistors in the sense amplifier can be varied by varying the width of the NMOS transistors and keeping the width of the PMOS transistors constant. The NMOS transistor affects the dummy bit line. Therefore, when the width of the NMOS transistor (Wn) is increased, the dummy bit line recovery time should be reduced.

Experimental setup and parameters varied –

The DRAM – Value of Wn was varied, such that k_r was varied from 0.25 to 2.25 and all other parameters were kept constant as follows – Cbl = 100ff, Cc = 50ff, Pass Switch = 0.3μm /0.2μm, Sense amplifier – Wp = 2.5μm, Ln = 0.18μm, Lp = 0.18μm, PC Switch = 1.62μm /0.18μm.

The SRAM – Value of Wn was varied, such that k_r was varied from 0.2 to 1 and all other parameters were kept constant as follows – Cbl = 100ff, Pass Switch = 0.3/0.2μm, Memory Cell – Ln = Lp = 0.18μm, Wn = 0.245μm, Wp = 0.2μm, Sense amplifier – Ln = Lp = 0.18μm, Wp = 2.5μm, PC Switch = 1.6μm /0.18μm.

2.3.6 Memory Cell Parameters

One of the factors influencing the memory cycle time is the value of the memory cell capacitance. A small memory cell capacitance can be charged and discharged faster as compared to a large value of Cc. But, to detect the charge stored on a very small capacitance, a very sensitive sense amplifier is required. There seems to be a tradeoff between the memory cell capacitance and the sense amplifier size.

In case of DRAM, the memory cell capacitance is equal to value of Cc and in SRAM it is the parasitic capacitance of the left and right nodes of the flip-flop memory cell. This value of capacitance depends on the W/L ratio of the transistors and the k_r value of the invertors in the memory cell.

Objectives – To observe the effect of varying memory cell capacitance on the performance goals. Referring to equation 2.1, it can be seen that Cc affects ΔV and the recovery time.

Experimental setup and parameters varied –

The DRAM – Cc was varied from 10ff to 100ff and all other parameter values were kept constant as follows – Cbl = 100ff, Pass Switch = 0.3/0.2μm, Sense amplifier – Wn = 0.952μm, Ln = 0.18μm, Wp = 2μm, Lp = 0.18μm, k_r = 0.476,

PC Switch = 1.62μm/0.18μm

The SRAM –

a) k_r of the memory cell was kept constant at 1.225 and W/L ratios of the transistors in the memory cell were varied. All other parameter values were kept constant as follows – Cbl = 100ff, Pass Switch = 0.3/0.2μm, Sense amplifier – Wn = 0.6μm, Ln = 0.18μm, Wp = 2.5μm, Lp = 0.18μm, k_r of Sense Amplifier = 0.476, PC Switch = 1.6μm /0.18μm.

b) The k_r of the memory cell was varied by varying the value of Wp and keeping Wn constant at 0.245μm. All other parameter values were kept constant as follows – Cbl = 100ff, Pass Switch = 0.3/0.2μm, Sense amplifier – Wn = 0.6μm, Ln = 0.18μm, Wp = 2.5μm, Lp = 0.18μm, k_r of Sense Amplifier = 0.476, PC Switch = 1.6μm /0.18μm.

c) The k_r of the memory cell was varied by varying the value of Wn and keeping Wp constant at 0.2μm.

All other parameter values were kept constant as follows – Cbl = 100ff, Pass Switch = 0.3/0.2μm, Sense amplifier – Wn = 0.6μm, Ln = 0.18μm, Wp = 2.5μm, Lp = 0.18μm, k_r of Sense Amplifier = 0.476, PC Switch = 1.6μm /0.18μm.

2.3.7 Word Line Switch

The memory access transistor, being a non ideal switch, presents some resistance while turning on and off. It also possesses sub threshold leakage. This resistance, leakage current and the memory capacitance constitute towards the time required to charge and discharge the memory capacitor. To reduce the charging time, it is necessary to reduce the resistance by making the switch wider. At the same time, widening of the switch leads to an increase in memory cell area. There is again a tradeoff between the two. To reduce the sub threshold leakage, it is necessary to increase the threshold voltage of the switch.

Objectives – The width of the word line switch affects the current flowing through it. As width is increased, it should charge up the memory capacitance faster and the memory cycle time should reduce.

Experimental setup and parameters varied –

The DRAM – Width of the word line switch is varied from 0.2μm to 2μm and all other parameter values were kept constant as follows – Cbl = 100ff, Cc = 50ff, Pass Switch Length = 0.2μm, Sense amplifier – Wn = 0.952μm, Ln = 0.18μm, Wp = 2μm, Lp = 0.18μm, k_r = 0.476, PC Switch = 1.62μm /0.18μm.

The threshold voltage of the word line switch was varied from 0.1V to 0.7V and the leakage current and memory cycle time were noted.

The SRAM – Width of the word line switch is varied from 0.2μm to 1μm and all other parameter values were kept constant as follows – Cbl = 100ff, Memory Cell – Ln = Lp = 0.18μm, Wn = 0.245μm, Wp = 0.2μm, Pass Switch Length = 0.2μm, Sense amplifier – Wn = 0.6μm, Ln = 0.18μm, Wp = 2.5μm, Lp = 0.18μm, k_r = 0.24,

PC Switch = 1.6μm /0.18μm.

2.4 Three Dimensional Plots

The set of experiments in Section 2.3 described how each design variable affects the performance parameters. Once this relationship is known, desired performance goals can be obtained by adjusting the values of the design variables. Desired performance goals are minimum memory cycle time, minimum space occupied on chip and maximum size. The three performance goals are interrelated. For example to reduce memory cycle time, the area of the sense amplifier has to be increased, resulting in increase in chip area. The sets of experiments in this section have been designed to study this dependency, or in other words, the tradeoffs between the performance goals.

The concept of operating point has been used. An operating point has three coordinates. The X coordinate corresponds to a particular value of cycle time, Y coordinate corresponds to a particular value of chip space and Z coordinate corresponds to a particular value of memory size. The memory size has been specified in terms of the value of Cbl, due to the direct relation between memory size and Cbl. Experiment I deals with studying the tradeoffs using various operating points. In Experiment II, the value of one performance goal is held constant and the other two values are varied and their relation is studied.

2.4.1 Experiment I – 3D Point Plots

Initially, five points are plotted as follows – Memory Cycle Time has been plotted on X axis, Chip Space (in terms of sense amplifier area and PC transistor area) is plotted on Y axis and Memory Size (in terms of Cbl) on Z axis.

2.4.1.1 Point 1. Point D1 (DX1, DY1, DZ1) was the operating point that was fundamental for all the DRAM experiments and Point S1 (SX1, SY1, SZ1) was the operating point that was fundamental for all the SRAM experiments

2.4.1.2 Point 2. Next, another Operating Point D2 (DX2, DY2, DZ2) was arrived at, such that this point had cycle time value lesser than that of Point D1. Similarly Point S2 (SX2, SY2, SZ2) was also designed.

2.4.1.3 Point 3. After this, Points D3 (DX3, DY3, DZ3) and S3 (SX3, SY3, SZ3) were plotted, which demonstrated the effect of increasing memory size. Cbl has been increased from an initial value of 100ff to 500ff. While arriving at these points, keeping cycle time minimum was the priority. Hence the tradeoff between cycle time and chip space was seen from this point

2.4.1.4 Point 4. Next, Points D4 (DX4, DY4, DZ4) and S4 (SX4, SY4, SZ4) were plotted by increasing memory size to 500ff. This experiment was similar to the one described in Section 2.3.1.3 except for the fact that priority was keeping chip space minimum by letting the increase in cycle time.

2.4.1.5 Point 5. Next, Points D5 (DX5, DY5, DZ5) and S5 (SX5, SY5, SZ5) were plotted by reducing chip space in comparison with Points D1 and S1 and observing the effect on other performance parameters.

2.4.2 Experiment II – 3D Line Plots

In this experiment, 3D line graphs have been plotted. To plot a line graph, initially a performance parameter was held constant and various operating points were obtained. All the operating points were then connected by a line. This experiment is again divided into sub experiments described by the following sections.

While plotting the three dimensional line graphs, chip space refers to the area consumed on the chip by the entire memory array and all the sense amplifiers and pre charge switches.

Procedure to calculate the total memory array area is as follows – The dimensions for the DRAM cell are given in literature as 4F * 2F, for a folded bit line architecture, where "F" is the lithography feature size, which is 0.18um. This gives an area of $8F^2$ = 0.2592 um^2, for one memory cell. Considering the capacitance of the bit line to be 0.3ff/um, the total length of the bit line is known once the Cbl value is known. For example for Cbl = 100ff, Bit line length = 333um. The number of cells per bit line = 333 um/4F = 462. Considering an array of 462 * 462 cells, the total memory array area would then be 55324.68 um^2 or 0.0553mm^2. Similarly, the dimensions of an SRAM Cell are 2.63um * 1.57um, giving a memory cell area of 4.129um^2 . Following similar calculations, number of cells for a 100ff bit line capacitance are 126 and total memory array area would then be 126 * 126 * 4.129um^2 = 0.0655 mm^2. Also there exist as much number of sense amplifiers and pre charge switches as the number of cells placed along the word line (462 for DRAM and 129 for SRAM). Total sense amplifier and PC area can be calculated by multiplying the area of a single cell by the number of cells along the word line. In this way, total area or chip space can be calculated.

2.4.2.1 Sense Amplifier and Pre Charge Area Constant. In this experiment, the area of a single sense amplifier and the pre charge switch was kept constant at 1.35 um^2 (for DRAM) and 1.4 um^2 (for SRAM), and the memory size was increased from Cbl = 50FF to 1000FF. The tradeoff between cycle time and memory size was studied.

2.4.2.2 Memory Size (Cbl) Constant. In this experiment, memory size (Cbl) was held constant. Sense amplifier and pre charge switch area were varied and its effect on cycle time was observed. The tradeoff between chip space and cycle time can thus be studied. K_r of the invertors in the sense amplifier was kept constant at 0.476(DRAM) and 0.24(SRAM) for symmetry in bit lines recovery. Also PC width was varied in such a manner that the PC time was kept almost constant, in order to compare memory cycle recovery time. Word line switch = 0.3u/0.2u.

2.4.2.3 Memory Cycle Time Constant. In this experiment, the memory cycle time was kept constant at 2.1ns (DRAM) and 1.24ns (SRAM) and Cbl was increased. As Cbl was increased, the sense amplifier and pre charge area had to be increased to obtain the same memory cycle time.

CHAPTER 3

EXPERIMENTAL RESULTS

This chapter presents the variable values in terms of experimental data tables. Waveforms observed using AWAVES have been produced, and graphs have been plotted so that design issues can be studied.

3.1 DRAM

The net list file shown in Figure 2.2, describing the DRAM Memory cell with the Sense amplifier and pre charge circuit was run using HSPICE. The waveforms observed are shown in Figure 3.1.

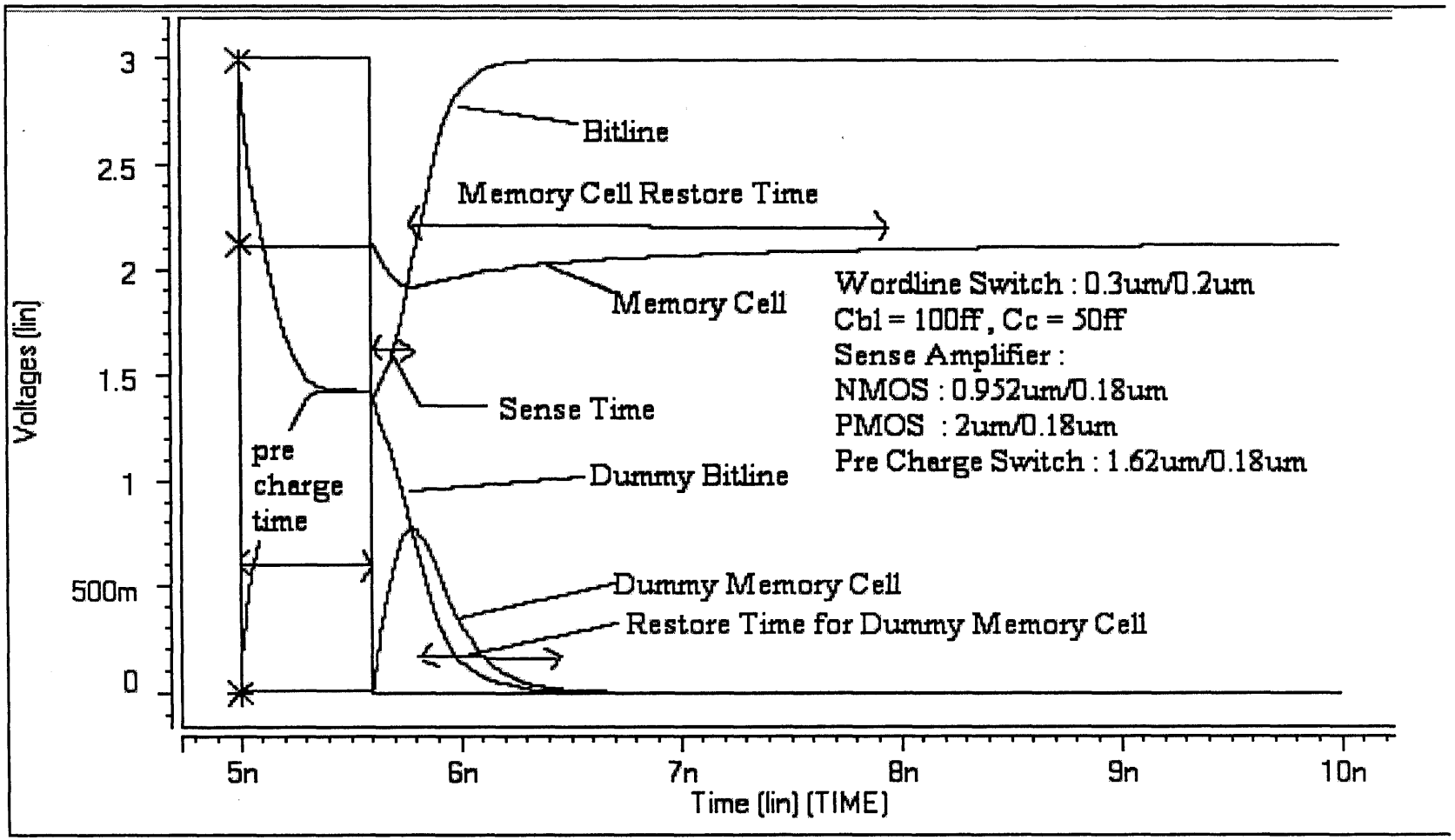


Figure 3.1 HSPICE Waveforms for a DRAM Memory Cell and Dummy Memory Cell and Sense Amplifier Showing the Pre Charge Time, Bit Line, Dummy Bit Line, Memory Cell and Dummy Memory Cell Response.

From the waveforms in Figure 3.1, it can be seen that the memory system and sense amplifier are working as expected. The time to merge the bit lines was observed to be 0.42 ns. During calculating the recovery times for the bit lines and the memory cell, 0% to 99% of the swing of the waveform was considered. The recovery time observed for the memory cell to recover to its initial value was 1.68ns, dummy memory cell was 0.6ns, bit line was 0.58ns and dummy bit line was 0.61ns. Thus, the bit lines were observed to be symmetrically recovering. This is due to the adjustment in k_r value of the inverters in the sense amplifier to 0.476. At this k_r value speed of the NMOS comes out to be 2.1 times that of PMOS.

Total Memory Cycle Time = Time to merge Bit lines + Memory Cell Recovery Time

$$= 0.42 \text{ ns} + 1.68 \text{ ns} = 2.1 \text{ ns}$$

3.2 SRAM

The net list used to describe the SRAM Cell, shown in Figure 2.5 of Chapter 2 was run using HSPICE. The waveforms observed are shown in Figure 3.2.

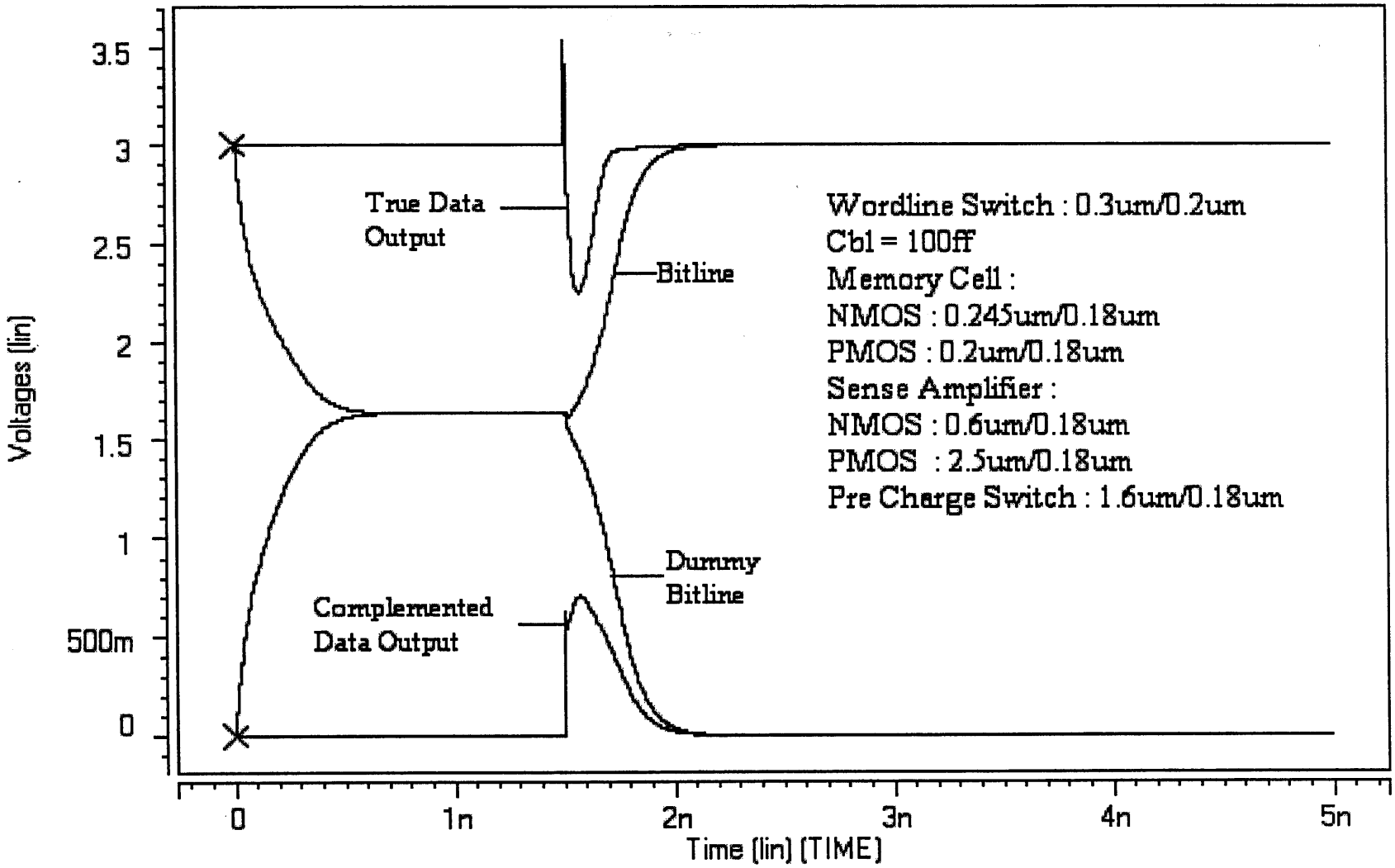


Figure 3.2 HSPICE Waveforms For an SRAM Memory Cell and Sense Amplifier Showing the Pre Charge Time, Bit Line, Dummy Bit Line and True and Complemented Data Response.

The time to merge the bit line and dummy bit line to the same voltage level of 1.64V was 0.66ns. The bit line recovery time was 0.51ns and dummy bit line recovery time was 0.52ns. Both recovery times were made almost the same by adjusting k_r value of the inverters in the sense amplifier to 0.24. Referring to Figure 3.2, it can be seen that the true data output recovers faster than the complemented data output. Recovery time of the true data output was 0.26ns and that of the complemented data output was 0.49ns. On conducting experiments, to reduce the complemented data output recovery time, it was found that Wn of the memory cell had to be increased a lot, which would result in an increase in chip space. Also, during considering the worst case recovery time, the dummy bit line recovery was slower than "0" memory cell. Hence, value of Wn was kept the same value.

Total Memory Cycle Time = Time to merge Bit lines + Worst Case Recovery Time

$$= 0.66 \text{ ns} + 0.52 \text{ ns} = 1.18\text{ns}$$

3.3 Basic Experiments

3.3.1 W/L Ratio of the Precharge Transistor

The experimental results when the width of the precharge switch was varied are shown below. The experimental data used such as the widths of the precharge transistor and the observations regarding timing have been recorded in Tables 3.1 and 3.2 below.

Table 3.1 Bit line and Memory Cell Times as a Function of Precharge transistor W/L Ratio for the DRAM

Width of PC (μm)	W/L of PC	Time to merge bit lines (ns)	Bit line recovery time (0 to 99 %) (ns)	Dummy Bit line recovery time (0 to 99 %)	memory cell recovery time (0 to 99 %) (ns)	total memory cycle time (ns)
0.9	5	1.35	0.59	0.62	1.7	3.05
1.08	6	0.82	0.57	0.62	1.69	2.51
1.26	7	0.63	0.59	0.62	1.69	2.32
1.44	8	0.55	0.58	0.61	1.69	2.24
1.62	9	0.42	0.58	0.61	1.68	2.1
1.8	10	0.39	0.6	0.61	1.75	2.14
1.98	11	0.36	0.6	0.61	1.75	2.11

Table 3.2 Bit line and Memory Cell Times as a Function of Precharge transistor W/L Ratio for the SRAM

Wn (um)	W/L	Time to merge bit lines (ns)	Bit line recovery time (ns)	Dummy Bit line recovery time (ns)	True Data Recovery Time (ns)	Complemented Data Recovery Time (ns)	total memory cycle time (ns)
1.2	6	1.12	0.51	0.52	0.35	0.58	1.7
1.4	7	0.87	0.51	0.52	0.35	0.58	1.45
1.6	8	0.66	0.51	0.52	0.35	0.58	1.24
1.7	8.5	0.58	0.51	0.52	0.35	0.58	1.16
1.8	9	0.56	0.51	0.52	0.35	0.58	1.14

A number of iterations were done by varying the width of the precharge transistor and the results of all these are shown below for comparison purpose. The waveforms obtained for DRAM are shown in Figure 3.3, and those for SRAM are shown in Figure 3.4. Graphs using the experimental results, are shown in Figures 3.5 and 3.6.

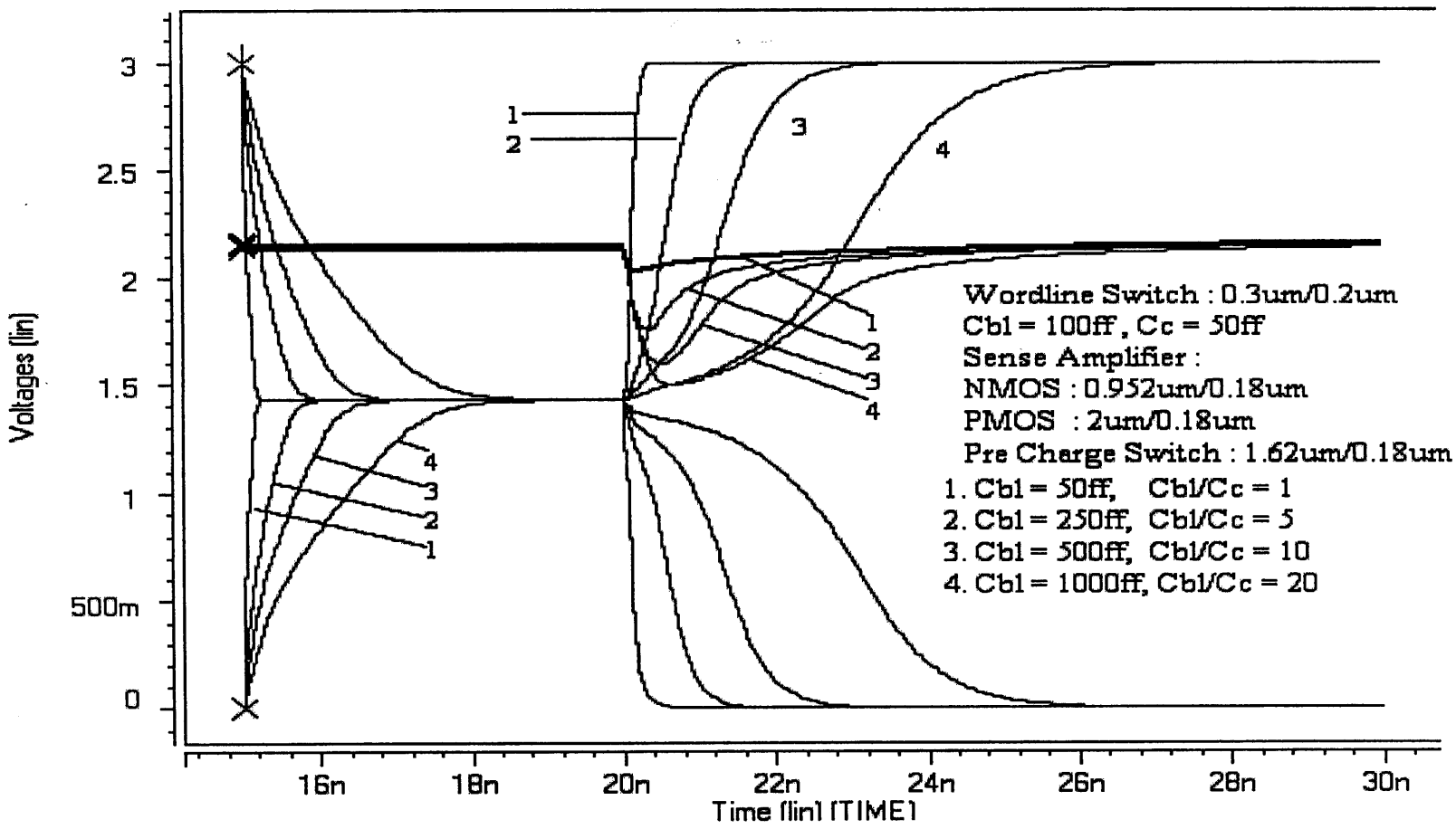


Figure 3.3 Effect of Varying Width of Pre Charge Transistor in the DRAM on Bit lines and Memory Cell.

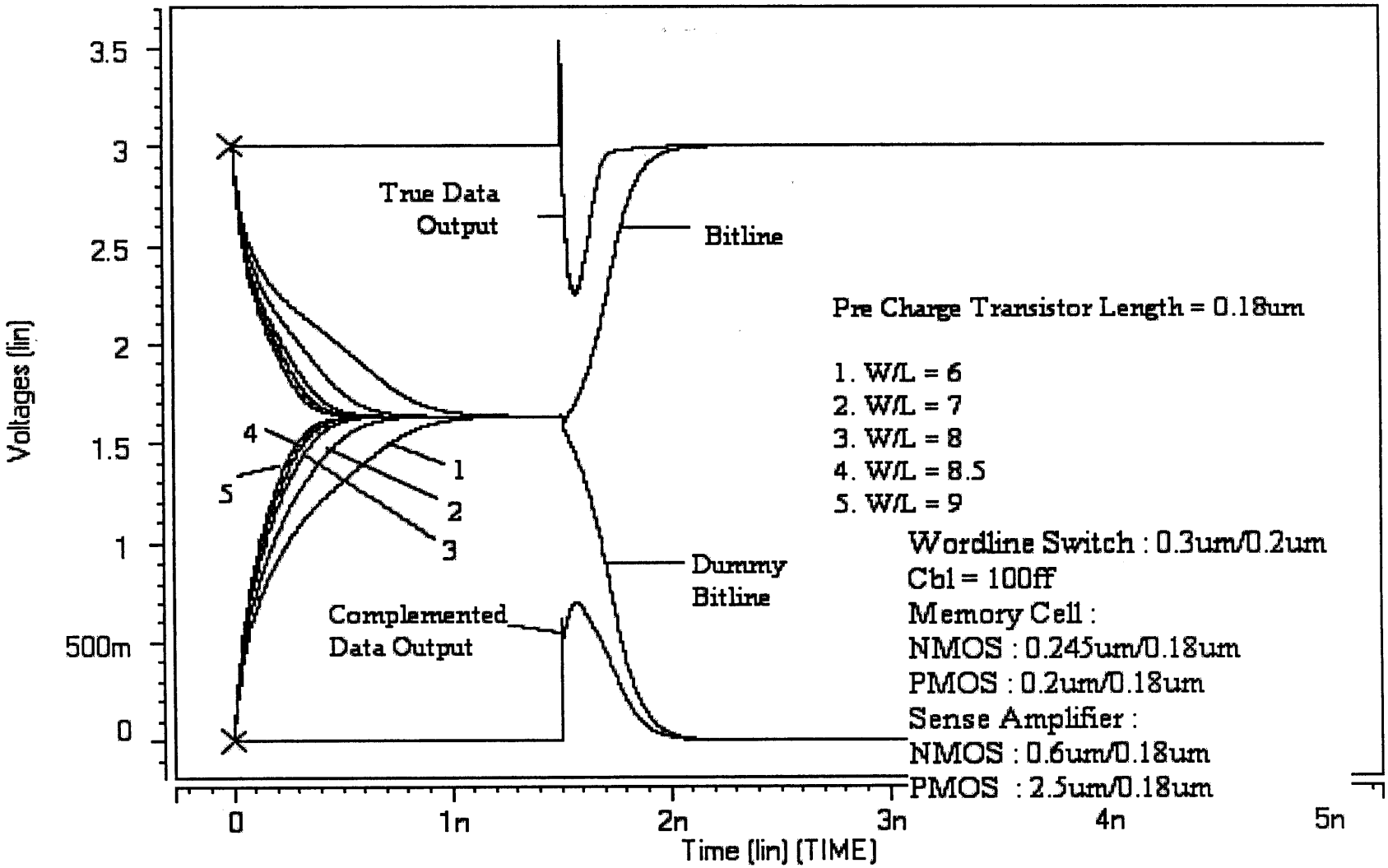


Figure 3.4 Effect of Varying Width of Pre Charge Transistor in the SRAM on Bit lines and Memory Cell True and Complemented Data Outputs

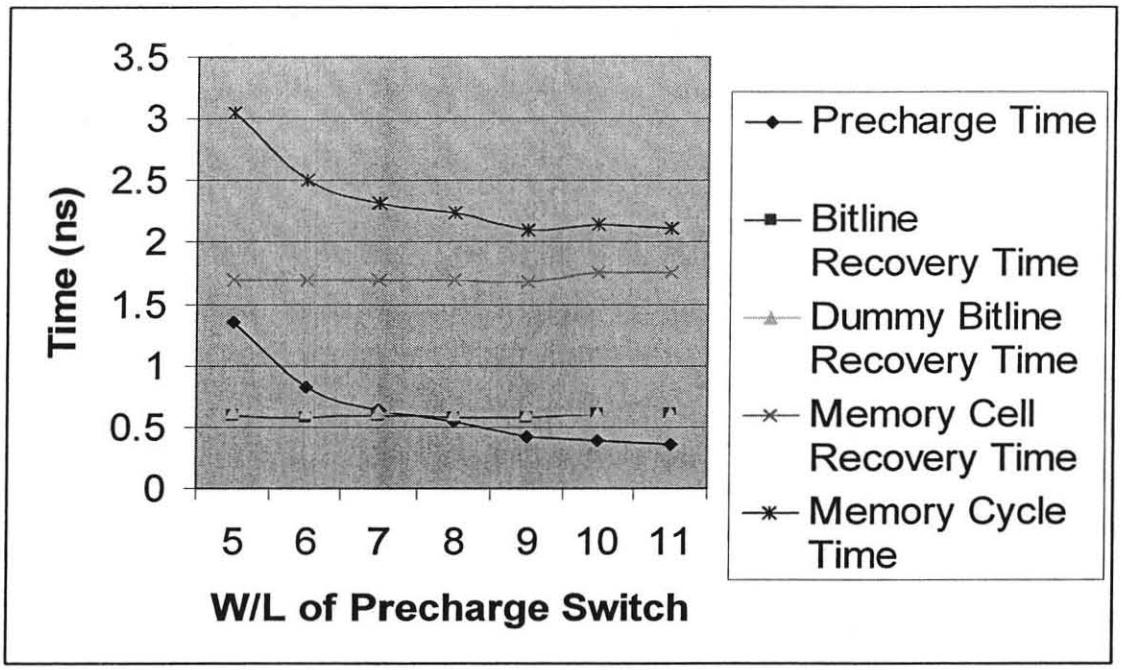


Figure 3.5 Effect of varying W/L of Pre Charge Transistor for DRAM on PC Time, Bit Line Recovery Time, Dummy Bit Line Recovery Time, Memory Cell Recovery Time and Memory Cycle Time.

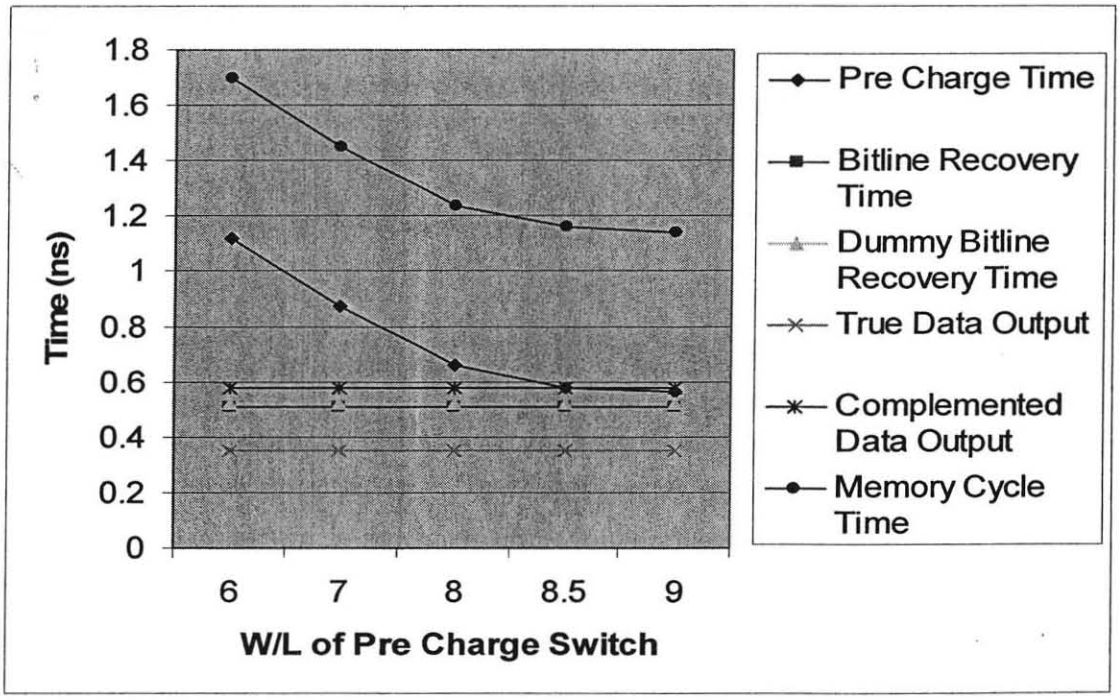


Figure 3.6 Effect of varying W/L of Pre Charge Transistor for DRAM on PC Time, Bit Line Recovery Time, Dummy Bit Line Recovery Time, Memory Cell Recovery Time and Memory Cycle Time.

Referring to Figures 3.5 and 3.6, it can be seen that as the W/L ratio of the PC transistor was increased, the time required to merge the bit lines to their unstable operating point reduced, as expected. The bit line recovery time, bit line voltage level and memory cell recovery time remain unaffected. However, due to decrease in PC time, the overall memory cycle time is reduced. These observations are common for DRAM and SRAM. Also as PC transistor W/L ratio was increased, the precharge time and the memory cycle times were reduced exponentially to a value where they could not be reduced further. This is the optimum value for W/L of PC = 9 for DRAM, which corresponds to **Wn=1.62μm**. Similarly **Wn=0.6μm** was the value chosen for the SRAM PC width.

Thus, the PC switch directly affects the PC time and hence indirectly the memory cycle time. However increase in W/L leads to an increase in chip space. Hence, PC width affects two of the three performance goals – Memory Cycle time and Space consumed on Chip in a give and take manner.

3.3.2 Bit line length (Cbl Value)

The experimental results when the bit line length value (Cbl) was varied from 50ff to 1000ff are shown below. The data used and observations made are shown in Table 3.3.for DRAM and Table 3.4 for SRAM.

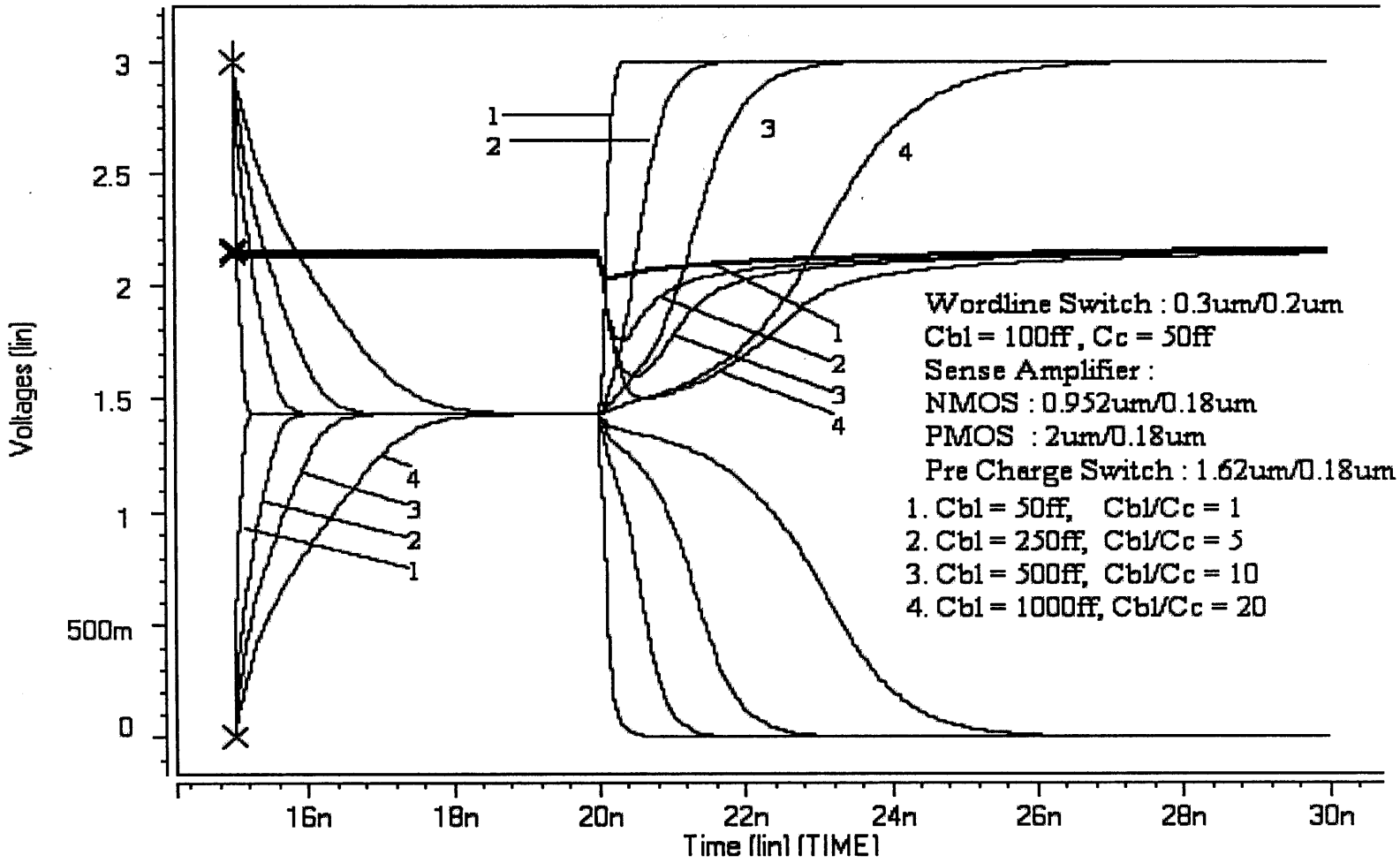
Table 3.3 Bit line and Memory Cell Behavior as a Function of Cbl/Cc Ratio for DRAM

Cbl/Cc	Time to merge bit lines (ns)	Bit line recovery time (ns)	Dummy Bit line recovery time (ns)	Memory Cell Read time (ns)	Memory Cell Restore time (ns)	memory cell recovery time (ns)	total memory cycle time (ns)	initial dip in memory cell voltage (V)	ΔV (V)
1	0.25	0.32	0.41	0.3	0.92	1.22	1.47	0.1	0.355
2	0.42	0.59	0.61	0.3	1.4	1.7	2.12	0.17	0.236
3	0.58	0.86	0.82	0.4	1.52	1.92	2.5	0.25	0.178
4	0.78	1.14	1.04	0.4	1.72	2.12	2.9	0.31	0.142
5	0.9	1.39	1.26	0.4	1.92	2.32	3.22	0.37	0.118
6	1.1	1.66	1.5	0.5	1.91	2.41	3.51	0.41	0.101
10	1.76	2.81	2.49	0.6	2.39	2.99	4.75	0.53	0.064
20	3.3	5.9	5.2	0.8	3.9	4.7	8	0.63	0.035

Table 3.4 Bit line and Memory Cell Behavior as a Function of Cbl for SRAM

Cbl (ff)	Time to merge bit lines (ns)	Bit line recovery time (ns)	Dummy Bit line recovery time (ns)	True Data Recovery Time (ns)	Complemented Data Recovery Time (ns)	total memory cycle time (ns)
50	0.41	0.29	0.3	0.25	0.33	0.74
100	0.66	0.51	0.52	0.35	0.58	1.24
250	1.5	1.12	1.19	0.54	1.33	2.83
500	2.76	2.29	2.39	1.08	2.65	5.41
1000	5	4.52	4.75	2.07	5	10

A number of iterations were done by varying the Cbl value and the results of all these are shown below for comparison purpose. The waveforms for DRAM are shown in Figure 3.7 and for SRAM are shown in Figures 3.8 and 3.9. Using the experimental results, graphs have been plotted in Figures 3.10, 3.11 and 3.12 for DRAM and Figure 3.13 for SRAM.



Effect of varying Cbl/Cc ratio on bitlines and memory cell

Figure 3.7 Effect of Varying Cbl/Cc Ratio in DRAM on Bit lines and Memory Cell, When Cc=50ff.

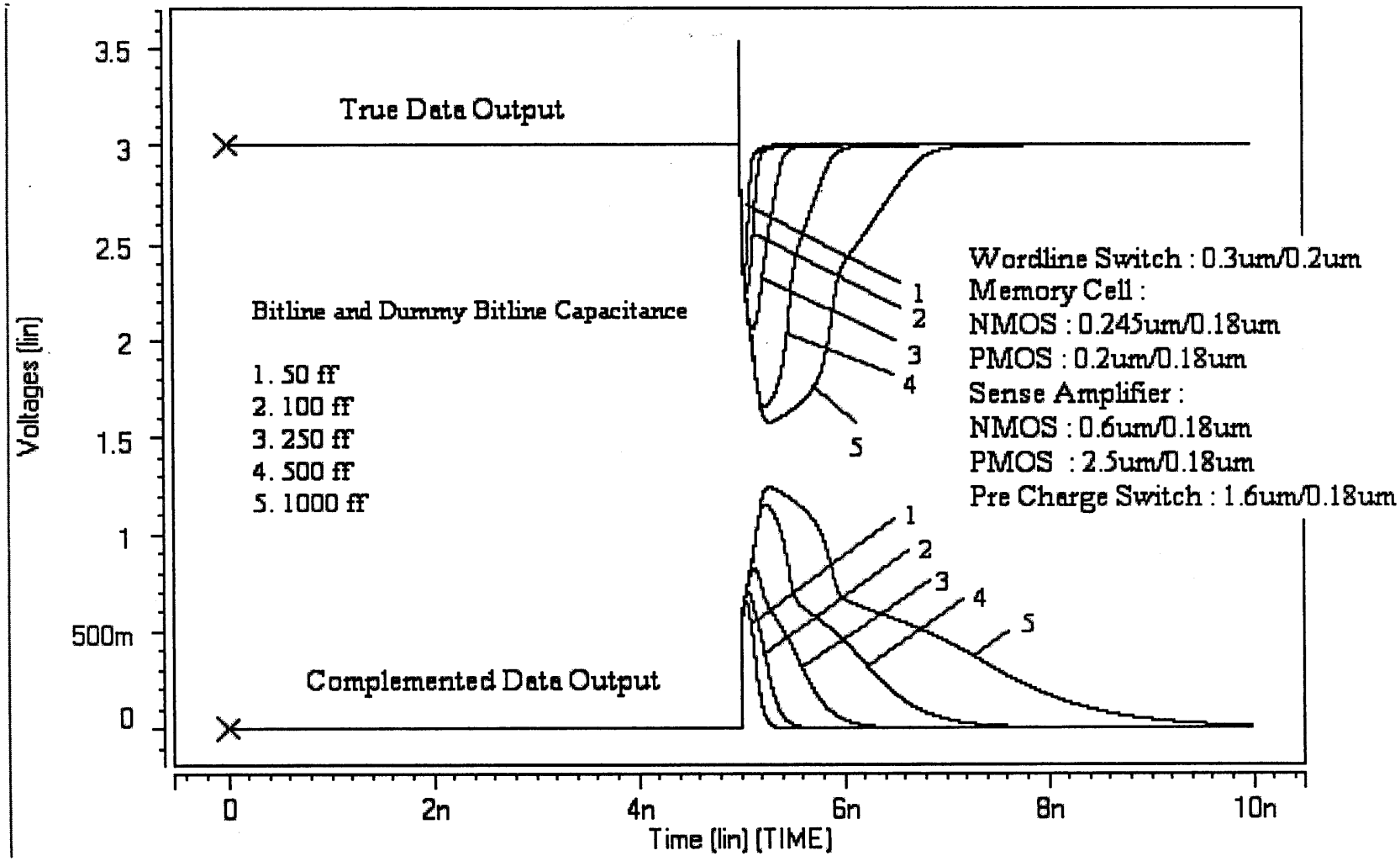


Figure 3.8 Effect of Varying the Value of Cbl in SRAM on True and Complemented Data Outputs when all Parameters of the Memory Cell are Kept Constant.

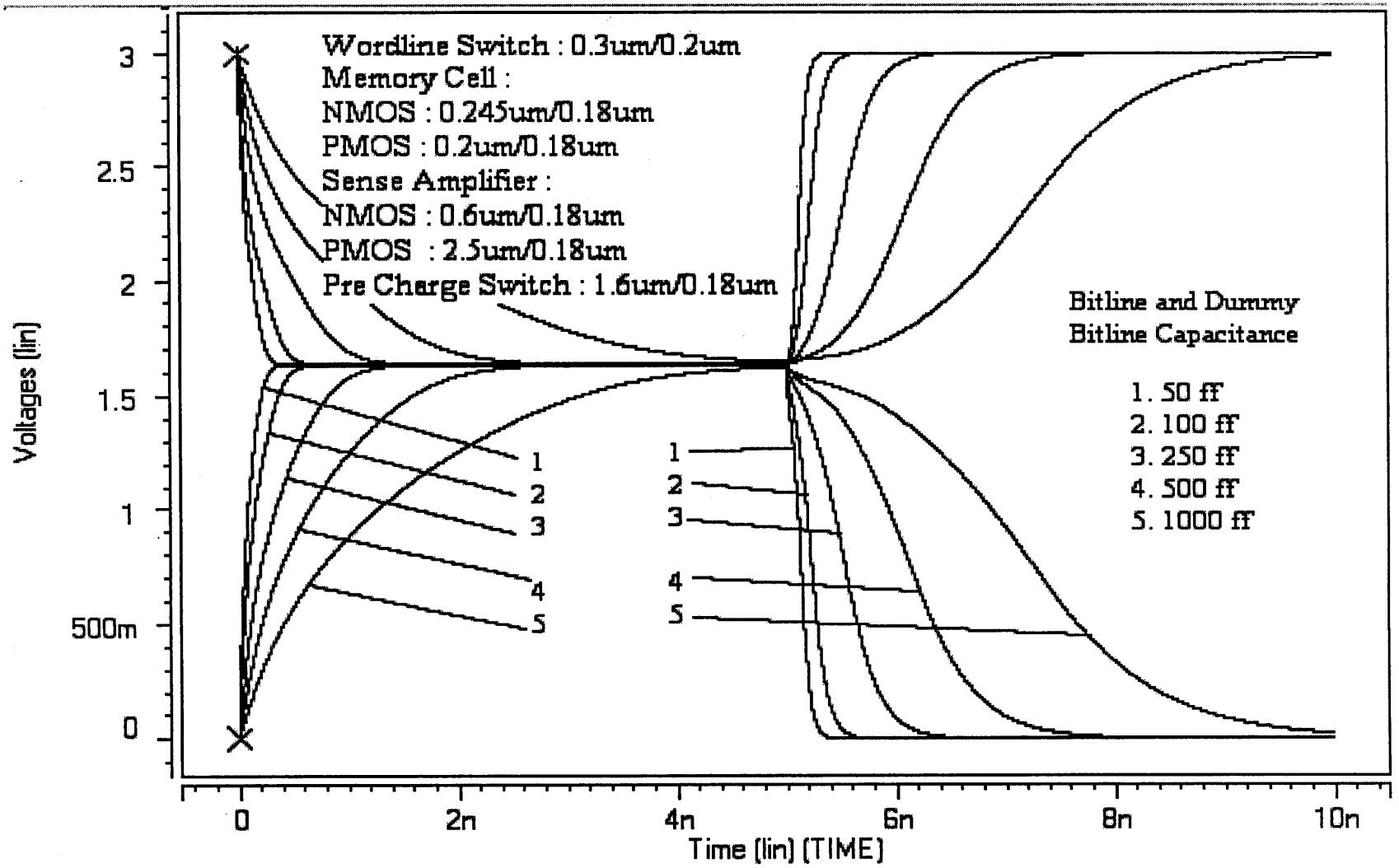


Figure 3.9 Effect of Varying the Value of Cbl in SRAM on Bit line and Dummy Bit line when all Parameters of the Memory Cell are kept Constant.

When memory size in increased, the length of the bit line increases. This leads to an increase in the total bit line capacitance value (Cbl). The increased capacitance on the bit lines slows down their recovery. However, they still maintain the symmetry in recovery (as k_r value is kept constant). Also, it takes more time to precharge the bit lines to the same voltage level. This slowing down effect is due to the large capacitance that the precharge transistor has to face while merging the two bit lines to the same voltage level.

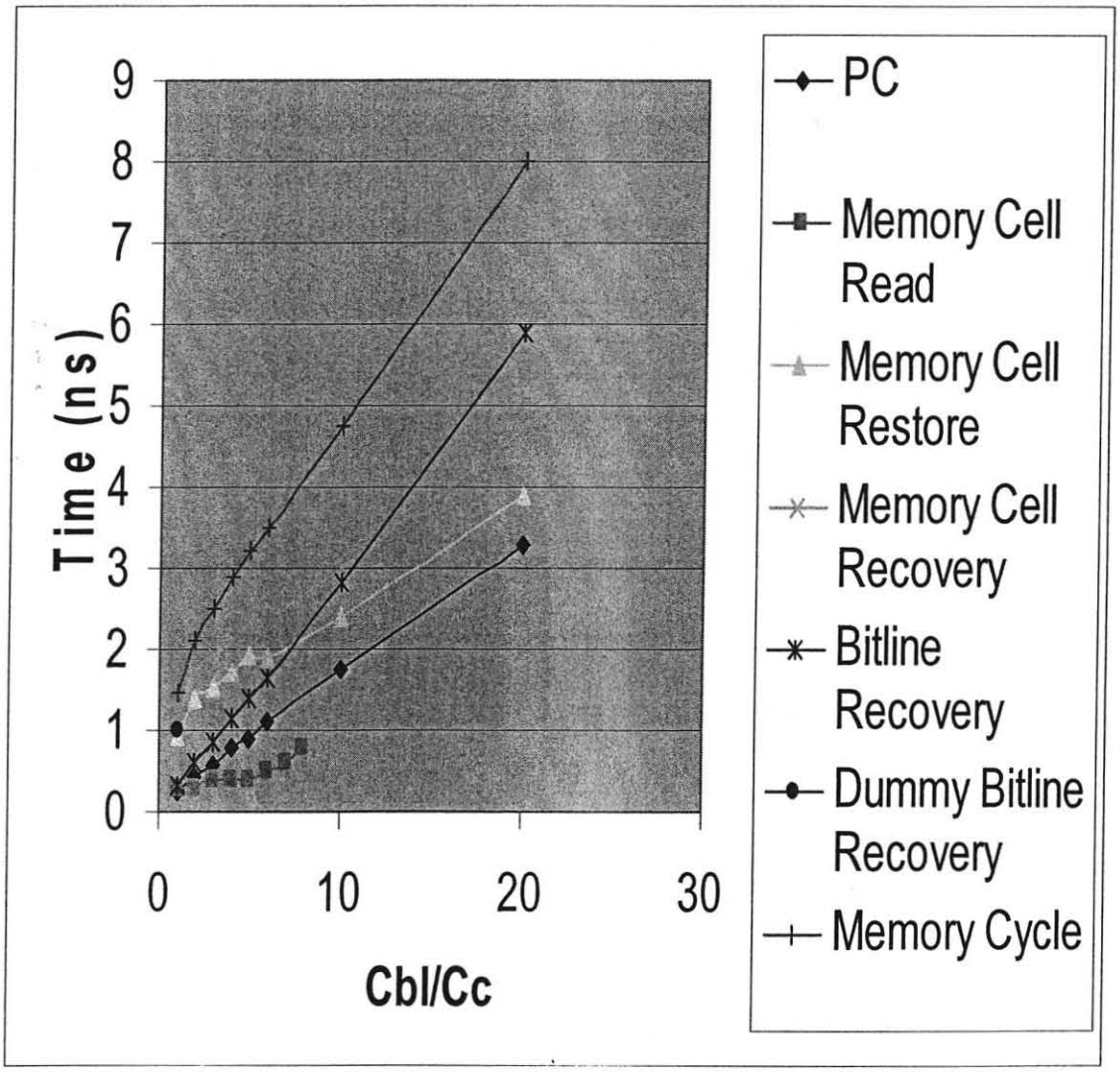


Figure 3.10 Effect of varying Cbl/Cc by varying Cbl, for DRAM on PC Time, Bit Line Recovery Time, Dummy Bit Line Recovery Time, Memory Cell Read, Restore and Recovery Time and Memory Cycle Time.

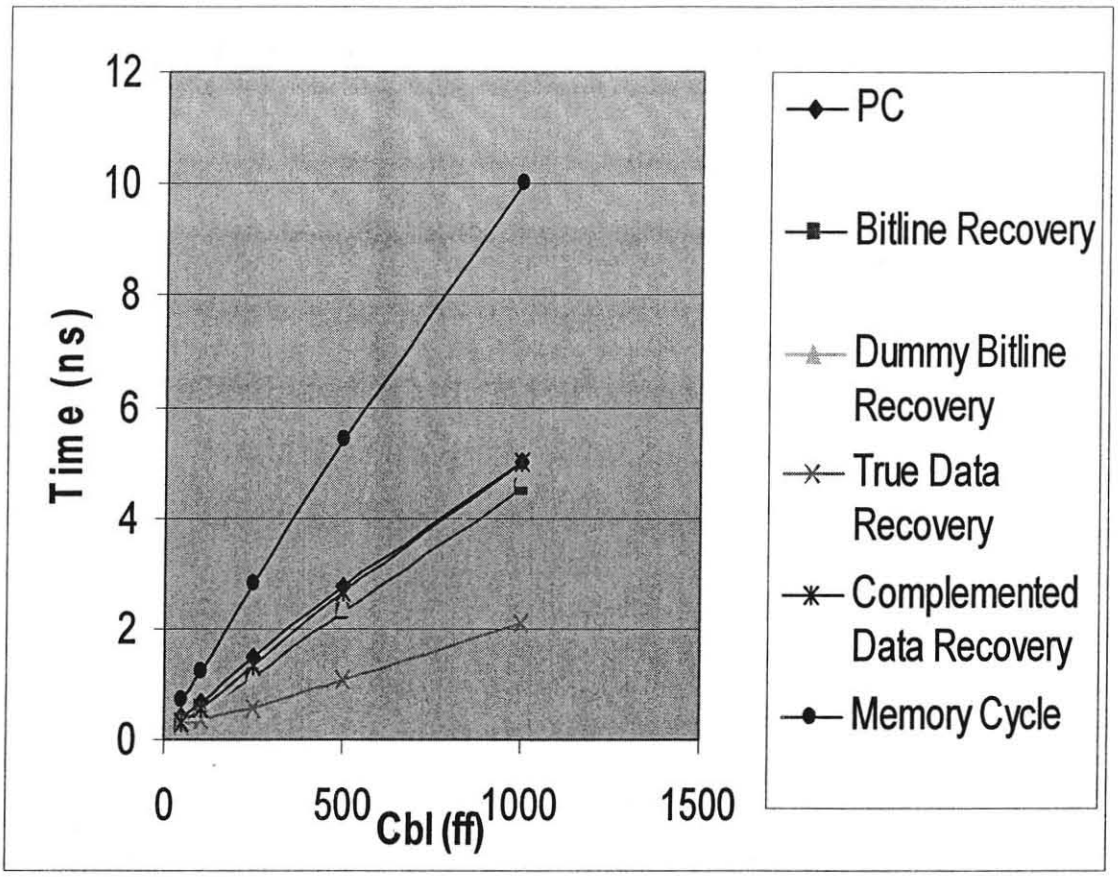


Figure 3.11 Effect of varying Cbl value for SRAM on PC Time, Bit Line Recovery Time, Dummy Bit Line Recovery Time, True and Complemented Data Recovery Time and Memory Cycle Time.

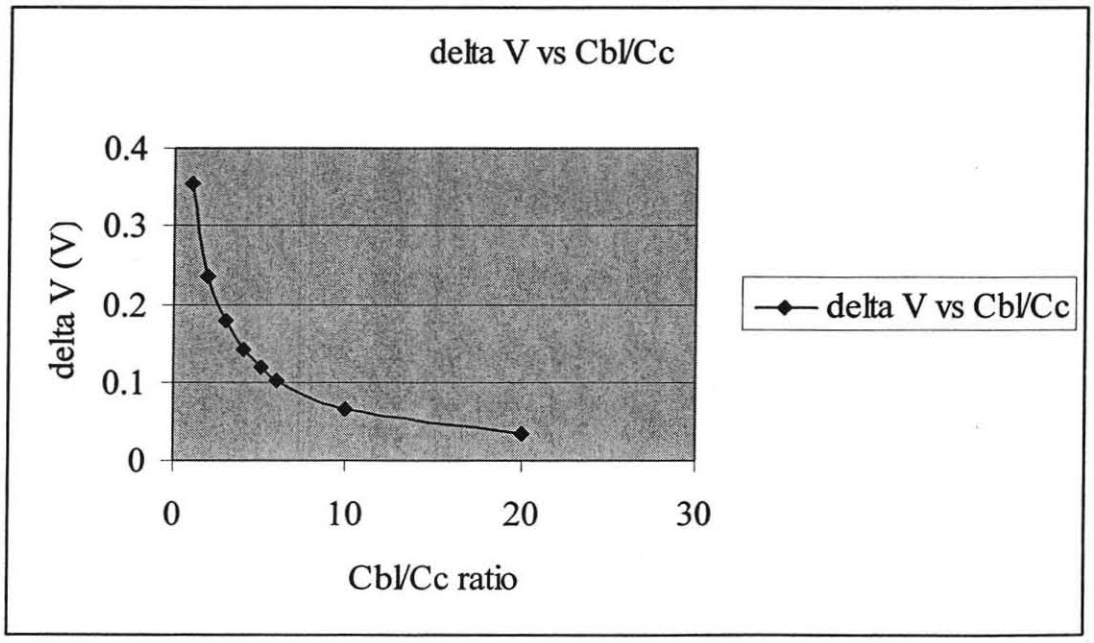


Figure 3.12 ΔV Versus Cbl/Cc Ratio for DRAM.

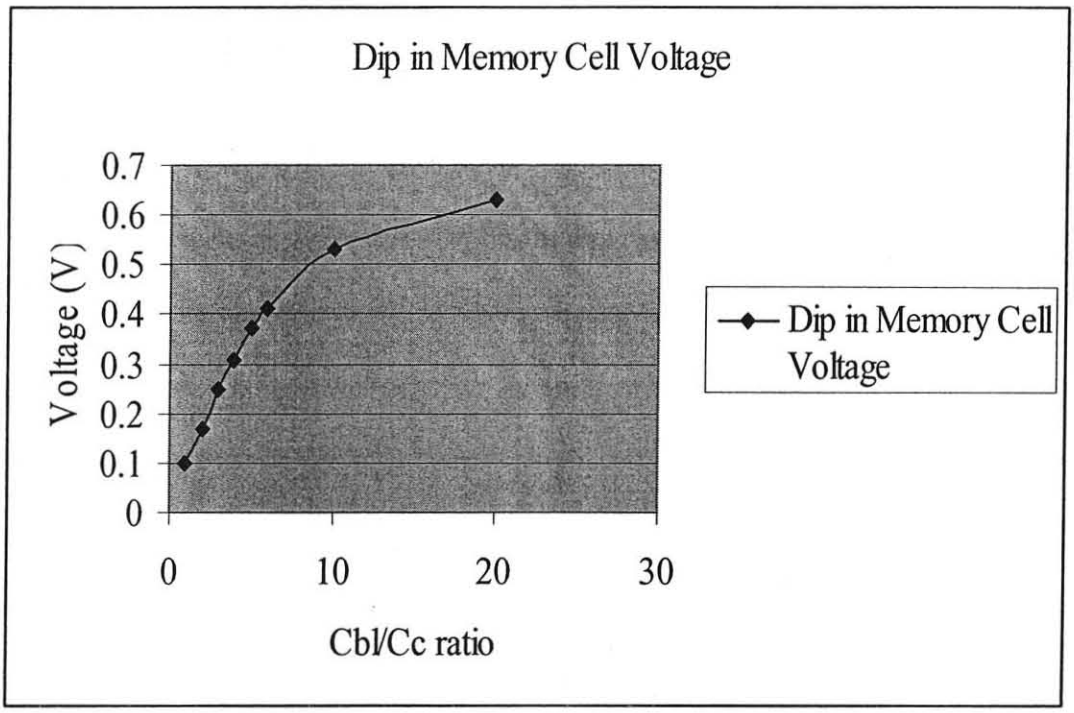


Figure 3.13 Initial Dip in Memory Cell Voltage (During Read Operation) Versus Cbl/Cc Ratio for DRAM.

Referring to Figure 3.12, as the Cbl/Cc ratio increases, ΔV reduces. This proves Equation 2.1 given in Chapter 2. As ΔV reduces, it takes longer for the sense amplifier to drive the memory cell back to its final voltage. It should take longer for the sense amplifier to get activated. Consequently, the memory cell discharges for a longer time leading to an increased dip in the memory cell voltage, which is shown in Figure 3.13.

3.3.3 Effect of Varying the W/L of Sense Amplifier Keeping k_r Constant

The experimental results for the increase in the W/L values of the transistors in the sense amplifier, which results in an increase in the total sense amplifier area, are shown below. During this experiment widths of N-Channel and P-Channel transistors were varied such that k_r kept constant. The effect of changing the W/L of the sense amplifier on the memory parameters are shown in Tables 3.5 and 3.6.

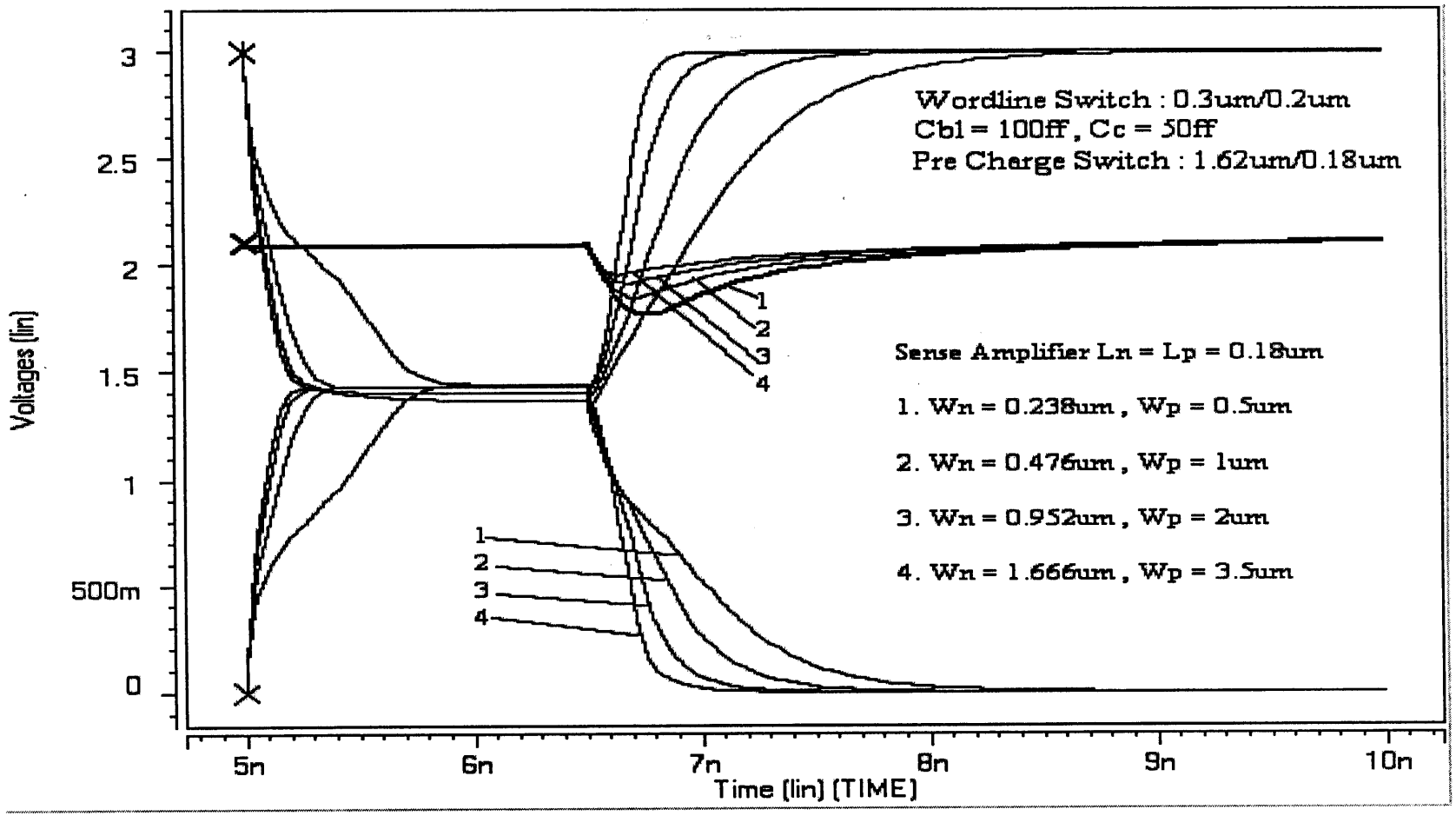
Table 3.5 Bit Line and Memory Cell Behavior as a Function of W/L Ratio of Sense Amplifier for DRAM

Wn (μm)	Wp (μm)	Sense Amp Area (sq-um)	time to merge bit lines (ns)	Bit line recovery time (ns)	Dummy Bit line recovery time (ns)	Memory Cell Read Time (ns)	Memory Cell Restore time (ns)	memory cell recovery time (ns)	total memory cycle time (ns)	Memory Cell initial dip (V)	Vbl (V)
0.238	0.5	0.26568	0.28	1.79	1.41	0.31	1.86	2.17	2.45	0.33	1.36
0.476	1	0.53136	0.32	0.99	0.93	0.27	1.65	1.92	2.24	0.26	1.4
0.714	1.5	0.79704	0.36	0.74	0.73	0.24	1.64	1.88	2.24	0.22	1.42
0.952	2	1.06272	0.42	0.57	0.61	0.22	1.47	1.69	2.11	0.19	1.43
1.428	3	1.59408	0.68	0.42	0.48	0.21	1.38	1.59	2.27	0.16	1.44
1.666	3.5	1.85976	0.95	0.38	0.43	0.19	1.32	1.51	2.46	0.15	1.44

Table 3.6 Bit line and Memory Cell Behavior as a Function of W/L Ratio of Sense Amplifier for SRAM

Wn (um)	Wp (um)	Sense Amplifier area (sq-um)	Time to merge bit lines (ns)	Bit line recovery time (ns)	Dummy Bit line recovery time (ns)	True Data Recovery Time (ns)	Complemented Data Recovery Time (ns)	total memory cycle time (ns)	Vbl (V)
0.192	0.8	0.645	0.4	1.09	0.76	0.38	0.87	1.49	1.54
0.36	1.5	0.9576	0.47	0.68	0.63	0.36	0.71	1.18	1.6
0.48	2	1.18	0.62	0.58	0.56	0.36	0.6	1.22	1.62
0.6	2.5	1.404	0.66	0.51	0.52	0.35	0.58	1.24	1.64
0.84	3.5	1.854	1.14	0.42	0.44	0.32	0.5	1.64	1.65

The waveforms for DRAM are shown in Figure 3.14 and those for SRAM are shown in Figure 3.15. Graphs have been plotted, using the experimental results in Figures 3.16 and 3.17.



Effect of varying W/L of sense amplifier, by keeping Kr constant on Memory Cell and Bitlines

Figure 3.14 Effect of Varying W/L Ratio of Transistors in the Sense Amplifier Keeping k_r Constant, on Bit lines and Memory Cell for DRAM.

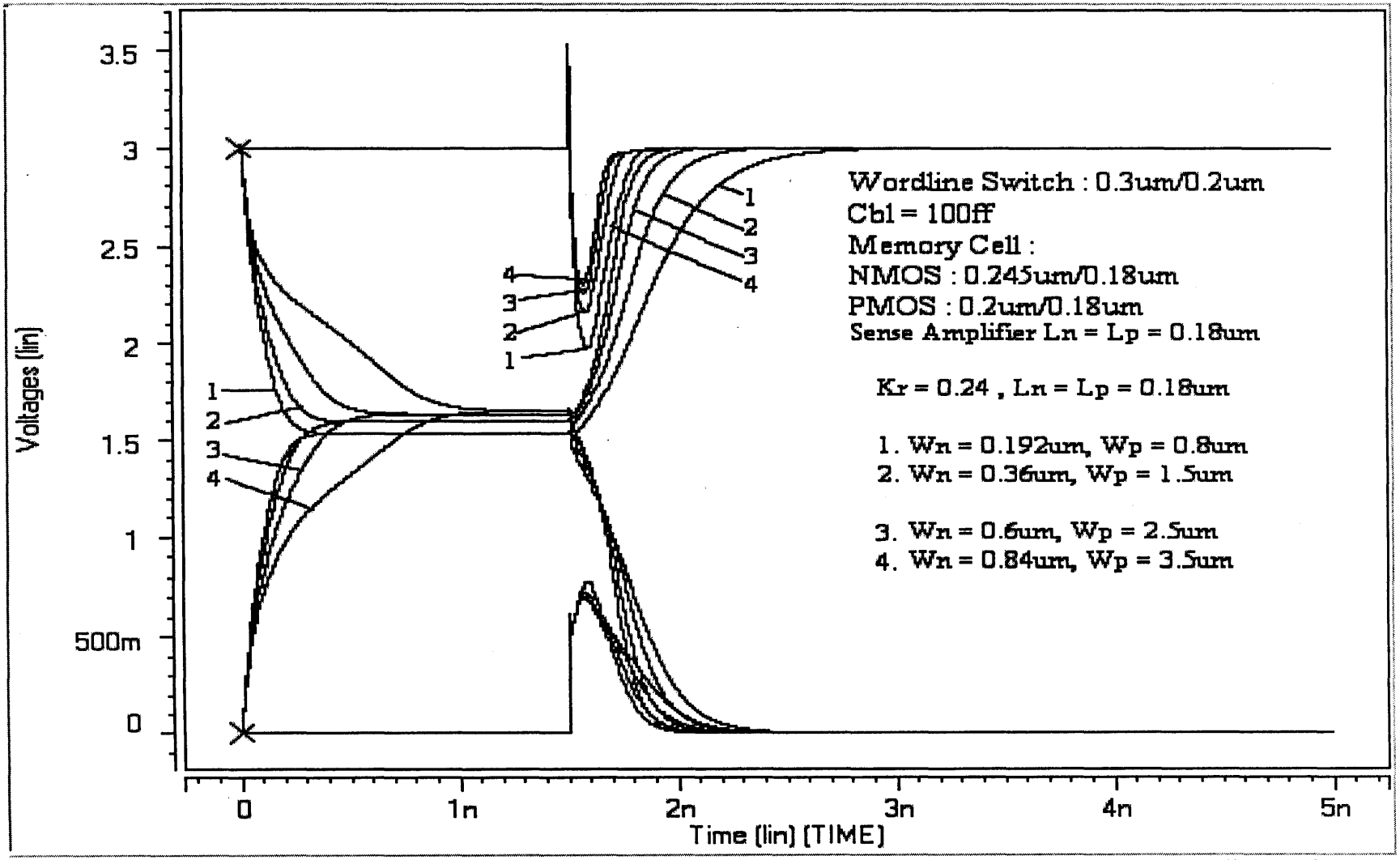


Figure 3.15 Effect of Varying W/L Ratio of Transistors in the Sense Amplifier Keeping k_r Constant at 0.24, on Bit lines and True Data and Complemented Data Output for SRAM.

Referring to Tables 3.5 and 3.6, it can be seen that common bit line voltage level, Vbl remains almost constant. It is around 1.4V for DRAM and 1.6V for SRAM. This is expected, since the k_r value was kept nearly constant. As the W/L Ratio and the sense amplifier area were increased, current supplied was increased which led to a reduction in bit line and memory cell recovery times. The read as well as restore times were reduced. The time to merge bit lines increased with increase in sense amplifier W/L.

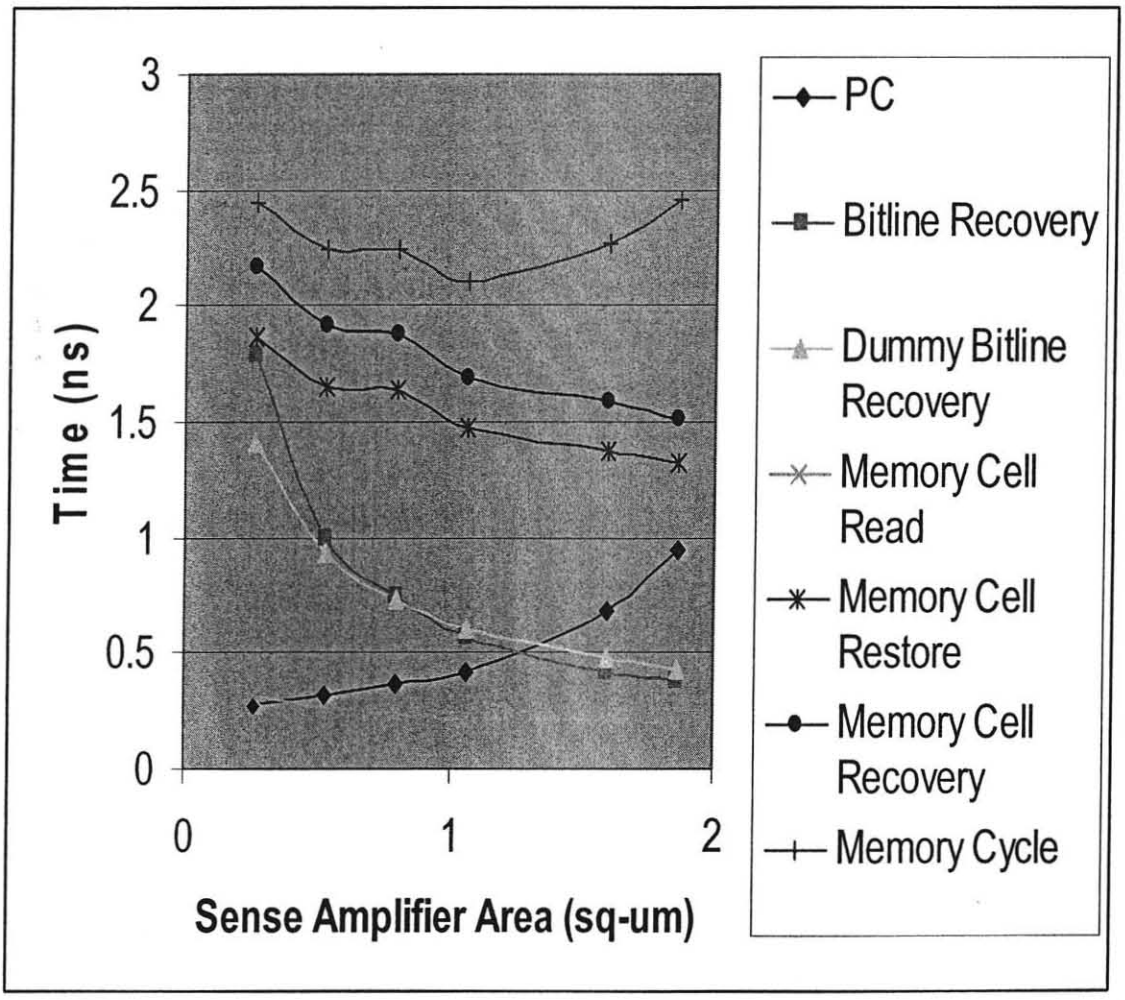


Figure 3.16 Effect of Increasing the W/L Ratio and the Sense Amplifier Area for DRAM, keeping k_r Constant at 0.476, on PC Time, Bit Line Recovery Time, Dummy Bit Line Recovery Time, Memory Cell Read, Restore and Recovery Time and Memory Cycle Time.

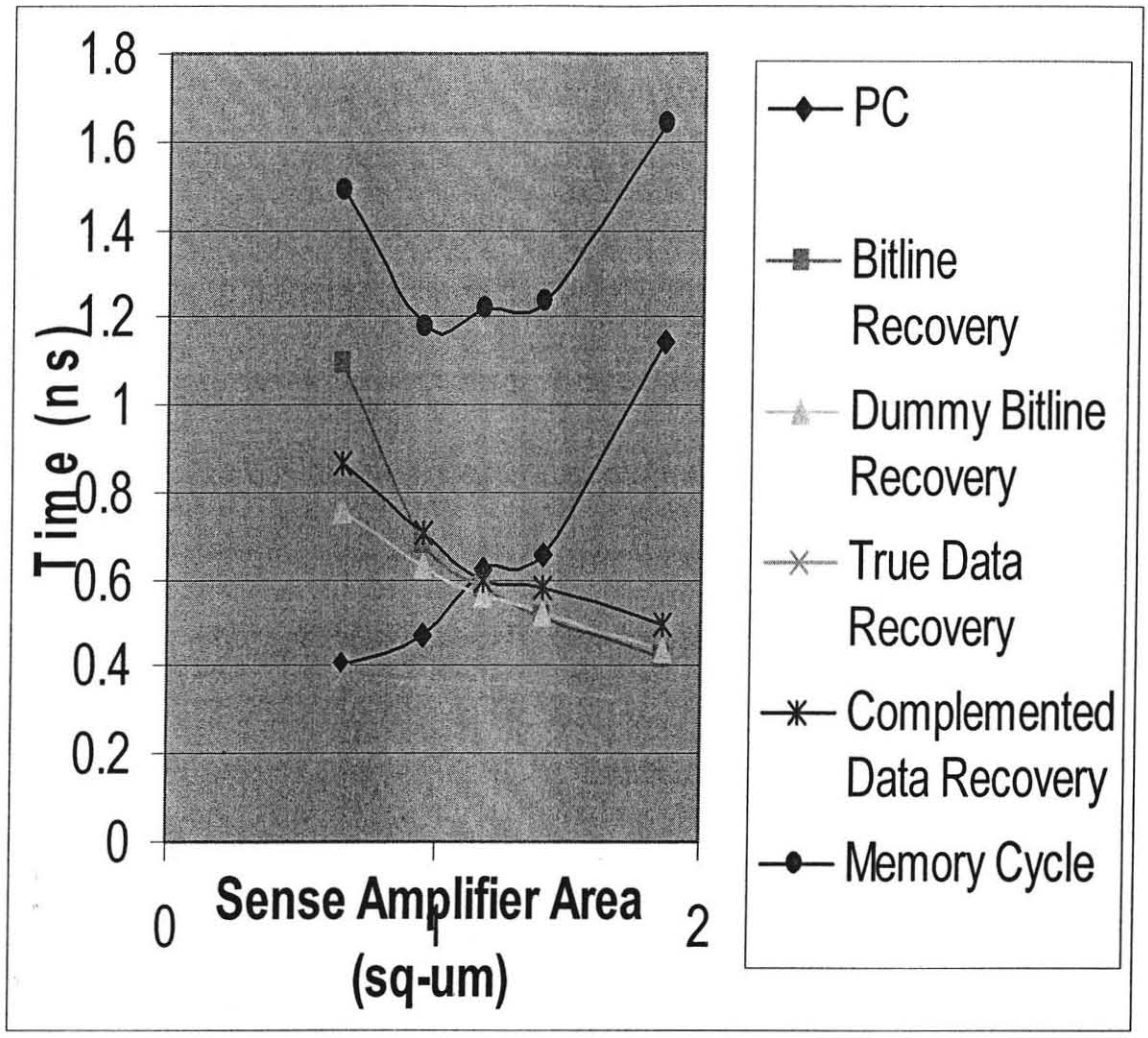


Figure 3.17 Effect of Increasing the W/L Ratio and the Sense Amplifier Area for SRAM, keeping k_r Constant at 0.24, on PC Time, Bit Line Recovery Time, Dummy Bit Line Recovery Time, True and Complemented Data Recovery Time and Memory Cycle Time.

Referring to Figures 3.16 and 3.17, when the sense amplifier area was approximately $1um^2$, an optimum point was observed in the memory cycle time. Increasing the sense amplifier area beyond this, would increase the memory cycle time. This happened because the precharge transistor value was fixed. In order to decrease memory cycle time with the increase in area, precharge transistor also has to be widened along with the transistors in the sense amplifier. An optimal design value is Wn=0.952μm and Wp=2μm, for DRAM, at which minimum memory cycle time of 2.1ns is observed. This

gives sense amplifier area of 1.06μm^2. Hence, these values have been selected for the design henceforth. Similarly for SRAM, optimum values are Wn = 0.6μm and Wp=2.5μm, at which minimum memory cycle time of 1.24ns is observed and sense amplifier area is 1.4μm^2. With increase in W/L, the dip in the memory cell voltage during sense amplifier read reduces. This occurs because the amplifier becomes more sensitive and can restore the cell to its initial value quickly, reducing the read time.

A complex tradeoff was observed between chip space consumed by the sense amplifier and memory cycle time. In order to obtain a minimum memory cycle time, an optimum W/L value has to be found by trial and error. In this case it results in a SA area of 1.06μm^2 and 2.19ns for DRAM and 1.11μm^2 and 1.24ns for SRAM.

3.3.4 Variation of the k_r Ratio of the Sense Amplifier Keeping Wn Constant

The experimental results when the k_r values of the transistors in the sense amplifier are varied, by varying only Wp and keeping Wn, Ln and Lp constant are shown below. The data used and observations made are shown in Tables 3.7 and 3.8.

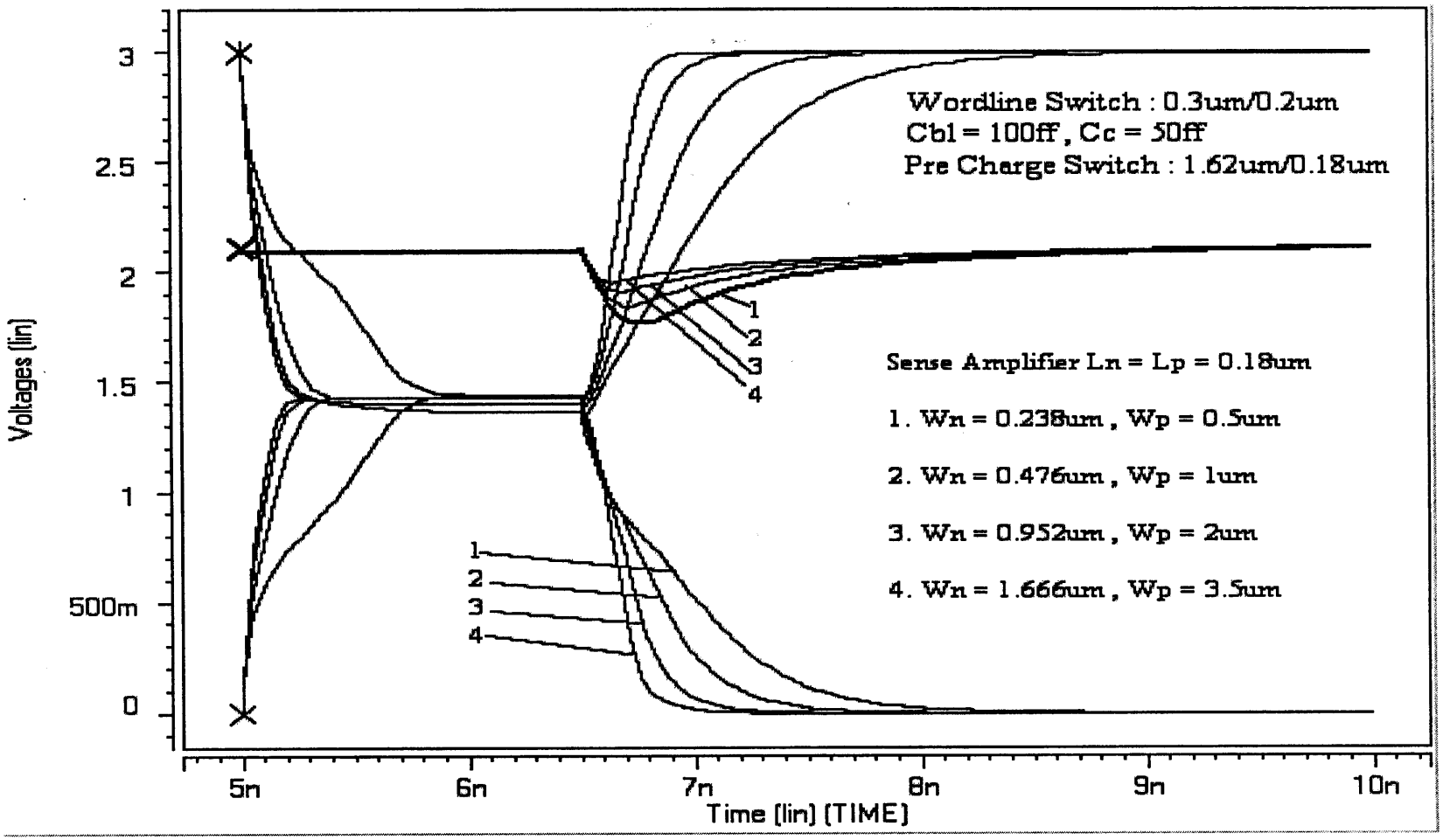
Table 3.7 Bit line and Memory Cell Behavior as a Function of k_r Ratio of Sense Amplifier by Varying Wp for DRAM

Wp (μm)	Kr	time to merge bit lines (ns)	Bit line recovery time (ns)	Dummy Bit line recovery time (ns)	memory cell recovery time (ns)	total memory cycle time (ns)	Bit line common voltage (V)
3.808	0.25	1.03	0.39	0.63	1.11	2.14	1.65
2	0.5	0.46	0.6	0.62	1.73	2.19	1.41
1.269	0.75	0.36	0.83	0.61	1.94	2.3	1.29
0.952	1	0.33	1.11	0.61	2.05	2.38	1.2
0.793	1.2	0.34	1.24	0.61	2.14	2.48	1.18
0.6346	1.5	0.3	1.5	0.62	2.22	2.52	1.12
0.476	2	0.29	1.92	0.64	2.36	2.65	1.05
0.317	3	0.25	2.68	0.64	2.53	2.78	1.02

Table 3.8 Bit line and Memory Cell Behavior as a Function of k_r Ratio of Sense Amplifier by Varying Wp for SRAM

Wp (μm)	kr	Time to merge bit lines (ns)	Bit line recovery time (ns)	Dummy Bit line recovery time (ns)	True Data Recovery Time (ns)	Complemented Data Recovery Time (ns)	total memory cycle time (ns)	Bit line common voltage
3	0.2	0.86	0.45	0.52	0.35	0.59	1.45	1.7
2.5	0.24	0.66	0.51	0.52	0.35	0.58	1.24	1.64
1.5	0.4	0.44	0.68	0.52	0.35	0.58	1.12	1.47
1	0.6	0.37	0.93	0.52	0.38	0.6	1.3	1.34
0.857	0.7	0.35	1.05	0.52	0.38	0.61	1.4	1.29

The waveforms for DRAM are shown in Figure 3.18 and those for SRAM are shown in Figures 3.19 and 3.20. Experimental results are presented using the Figures 3.21, 3.22 and 3.23.



Effect of varying W/L of sense amplifier, by keeping Kr constant on Memory Cell and Bitlines

Figure 3.18 Effect of Varying k_r Ratio of Transistors in the Sense Amplifier by Varying Wp, on Bit lines and Memory Cell for DRAM.

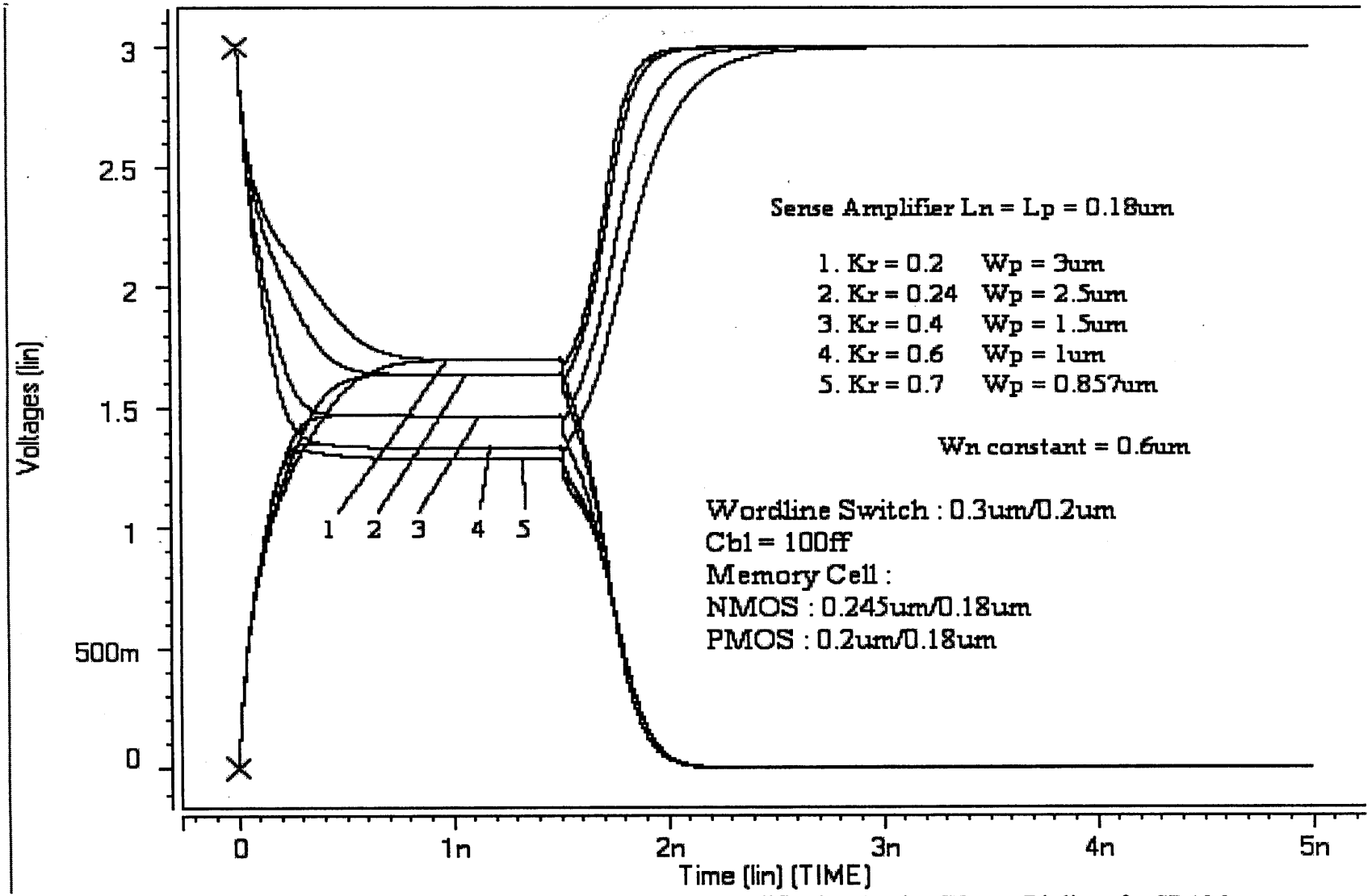


Figure 3.19 Effect of Varying k_r Ratio of Transistors in the Sense Amplifier by Varying Wp, on Bit lines for SRAM.

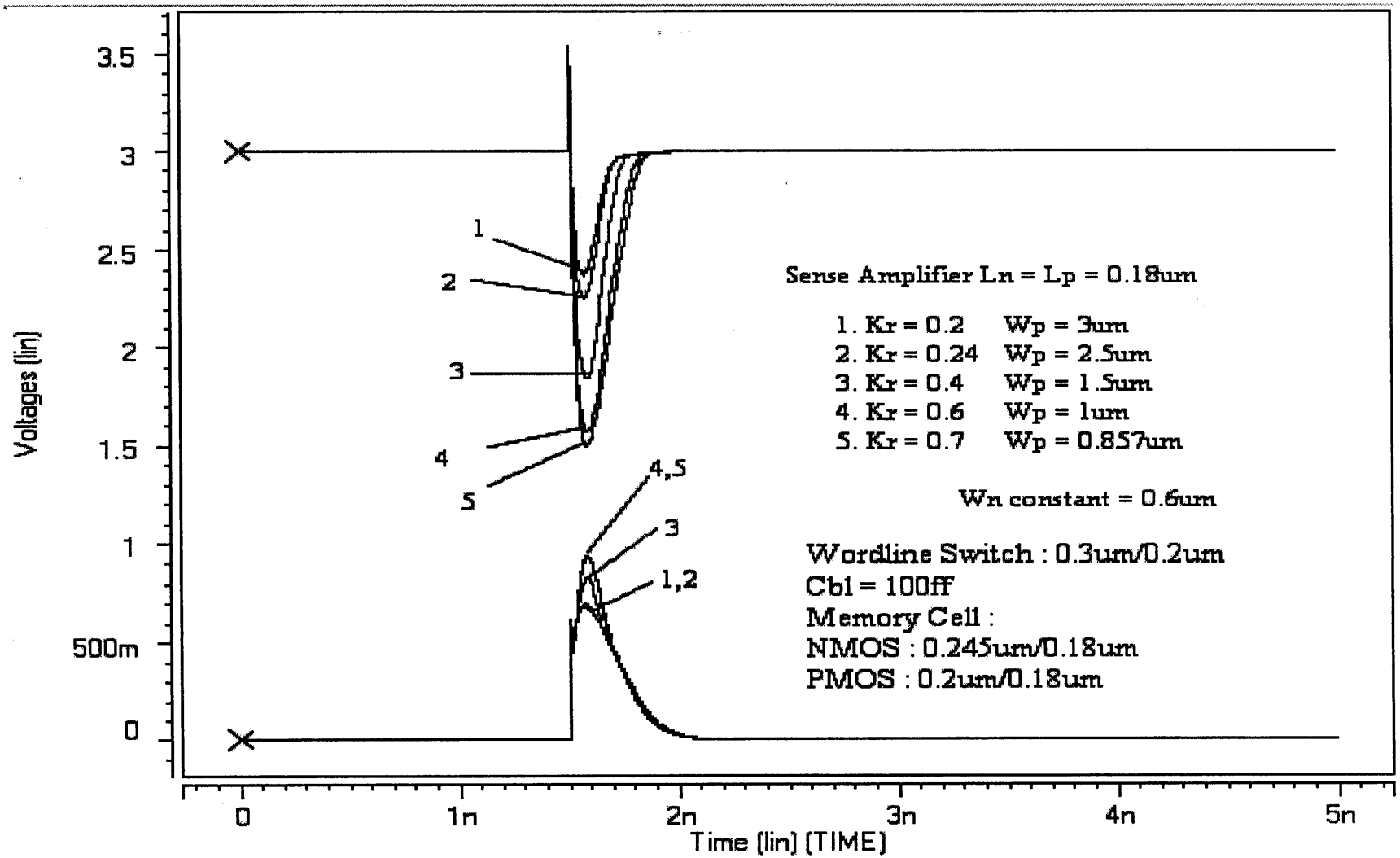


Figure 3.20 Effect of Varying k_r Ratio of Transistors in the Sense Amplifier by Varying Wp, on the True and Complemented Data Outputs for the SRAM.

The width of the P Channel transistor of the SA directly affects the bit line. Hence, when the width of Wp is increased, it should reduce the recovery time of the bit line. This result is observed in Figures 3.18 and 3.19. The dummy bit line recovery time is not affected, as its width is kept fixed.

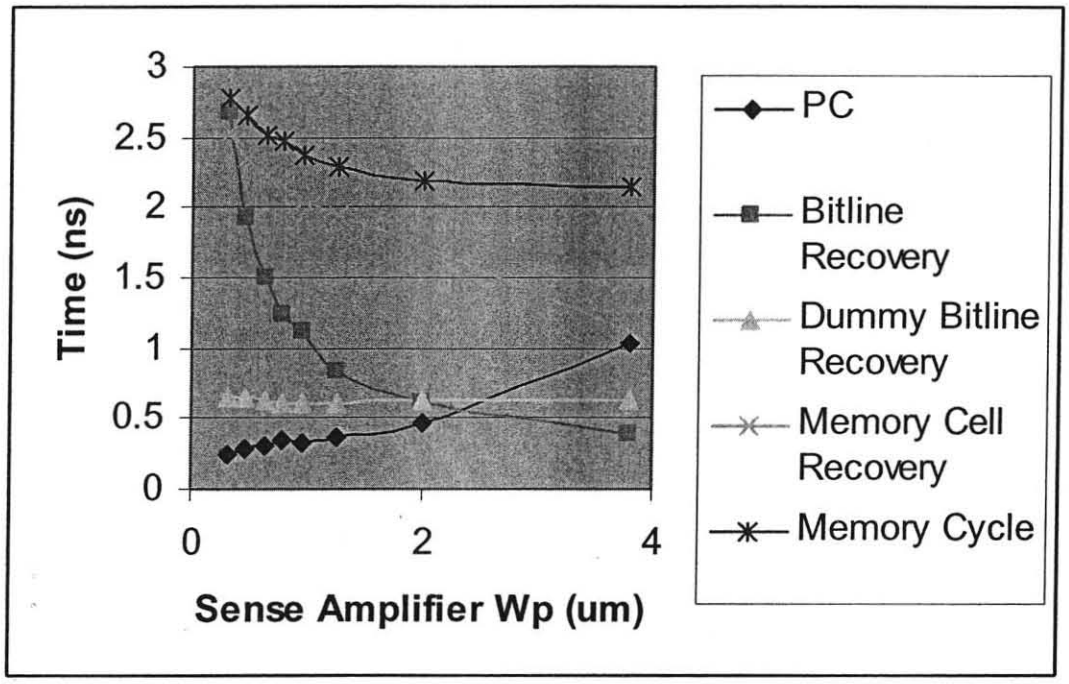


Figure 3.21 Effect of Increasing Sense Amplifier Wp on Bit lines and Memory Cell for DRAM.

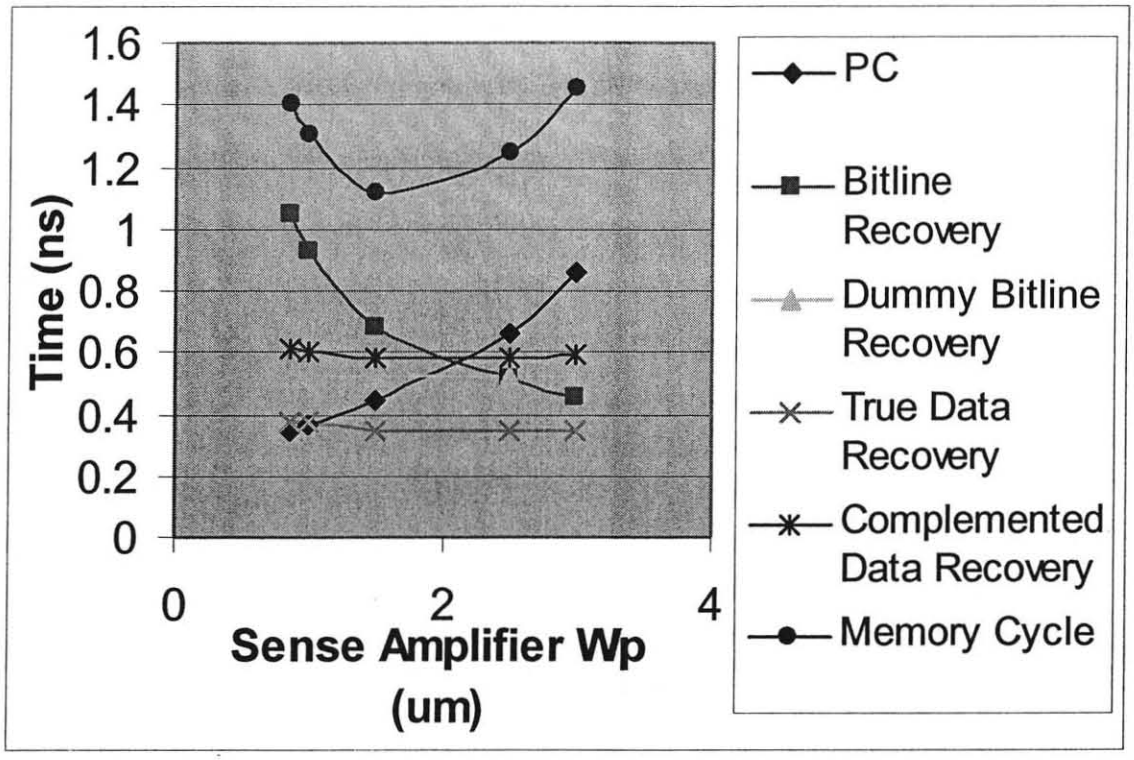


Figure 3.22 Effect of Increasing Sense Amplifier Wp, on Bit lines and True and Complemented Data Output for SRAM.

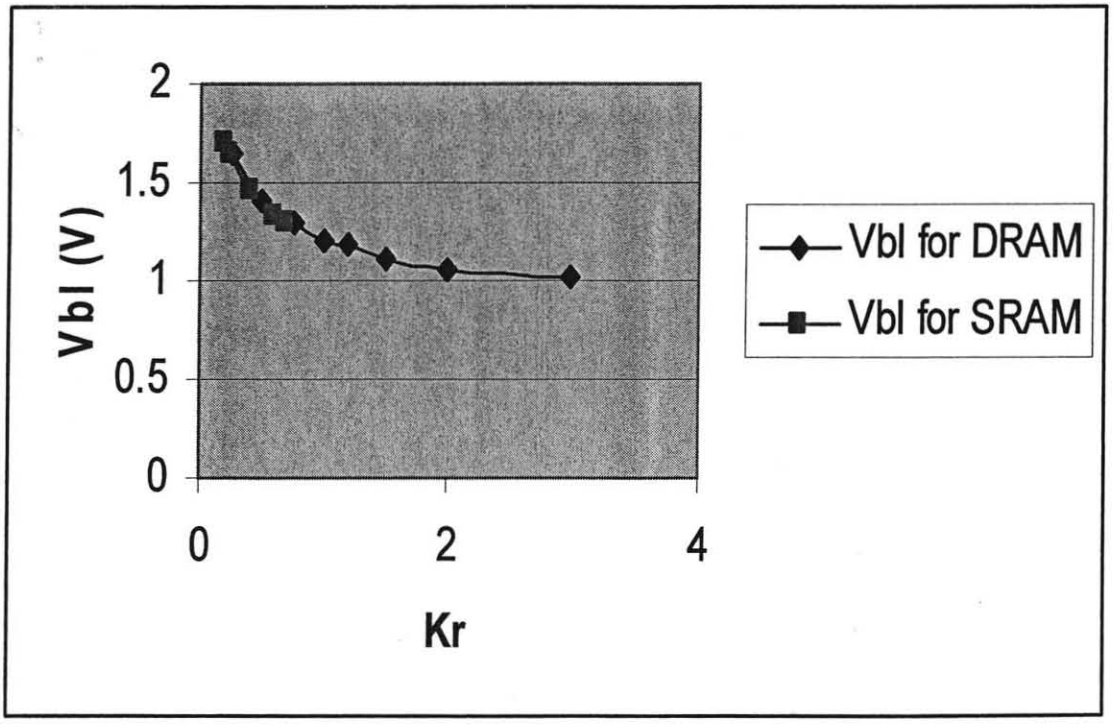


Figure 3.23 Effect of Increasing kr Ratio of Transistors in The Sense Amplifier on the Bit line Common Voltage for DRAM and SRAM.

As k_r is reduced, Wp is increased, thus increasing the parasitic capacitance of the sense amplifier. This adds to the bit line capacitance and hence, it takes more time to merge the bit lines, as seen in Figures 3.19 and 3.22. As the k_r value nears 1.5 for DRAM, a saturation effect is observed and PC time cannot be reduced further.

Memory cell recovery time reduces with an increase in Wp, however the bit lines recovery asymmetrically. For symmetry in bit line recovery, it is necessary to maintain k_r. Whether to keep k_r constant, or to vary k_r, depends on what is the requirement. If minimum cycle time is desired, irrespective of symmetry in bit line recovery, then k_r has to be adjusted accordingly.

With increasing k_r, memory cycle time increases. This is because of the reduction in Wp, which makes the sense amplifier less sensitive.

From Figure 3.23, as k_r increases, the common bit line voltage level continues to decrease. Using equation 2.1, it is expected that ΔV should increase resulting in quicker flipping of the flip flop and reduction in memory cycle time. However, this is not observed because flip flop action is also dominated by the areas and parasitic capacitance of the transistors. This shows that recovery time depends on k_r as well as the current flowing through the sense amplifier.

At $k_r = 0.476$ for DRAM and 0.24 for SRAM, bit line and dummy bit line recovery times are almost symmetric. Hence, this value has been used throughout the design.

As k_r increases, the PC time reduces less as compared to the increase in memory cell recovery time. Hence, memory cycle time gradually increases.

3.3.5 Variation of the k_r Ratio of the Sense Amplifier Keeping Wp Constant

The experimental results when the k_r values of the transistors in the sense amplifier are varied are shown below. Wn was varied and Wp, Ln and Lp were kept constant The waveforms for DRAM are shown in Figure 3.24 and those for SRAM are shown in Figures 3.26 and 3.27. The data used and observations made are shown in Tables 3.9 and 3.10. Experimental results are presented using graphs in Figures 3.25, 3.28, 3.29.

Table 3.9 Bit Line and Memory Cell Behavior as a Function of k_r Ratio of Sense Amplifier by Varying Wn for DRAM

Wn (μm)	Kr	time to merge bit lines (ns)	Bit line recovery time (ns)	Dummy Bit line recovery time (ns)	memory cell recovery time (ns)	total memory cycle time (ns)	Bit line common voltage (V)
0.5	0.25	0.48	0.62	0.92	1.42	1.9	1.61
1	0.5	0.46	0.59	0.59	1.71	2.17	1.41
1.5	0.75	0.47	0.59	0.46	1.83	2.3	1.29
2	1	0.49	0.56	0.39	1.89	2.38	1.2
2.25	1.125	0.48	0.57	0.35	1.86	2.34	1.17

Table 3.10 Bit Line and Memory Cell Behavior as a Function of k_r Ratio of Sense Amplifier by Varying Wn for SRAM

Wn (um)	kr	Time to merge bit lines (ns)	Bit line recovery time (ns)	Dummy Bit line recovery time (ns)	True Data Recovery Time (ns)	Complemented Data Recovery Time (ns)	total memory cycle time (ns)	Bit line common voltage (V)
0.5	0.2	0.66	0.51	0.76	0.36	0.64	1.47	1.69
0.6	0.24	0.66	0.51	0.52	0.35	0.58	1.24	1.64
1.25	0.5	0.67	0.51	0.37	0.27	0.41	1.18	1.42
2.5	1	0.8	0.51	0.27	0.23	0.3	1.3	1.2

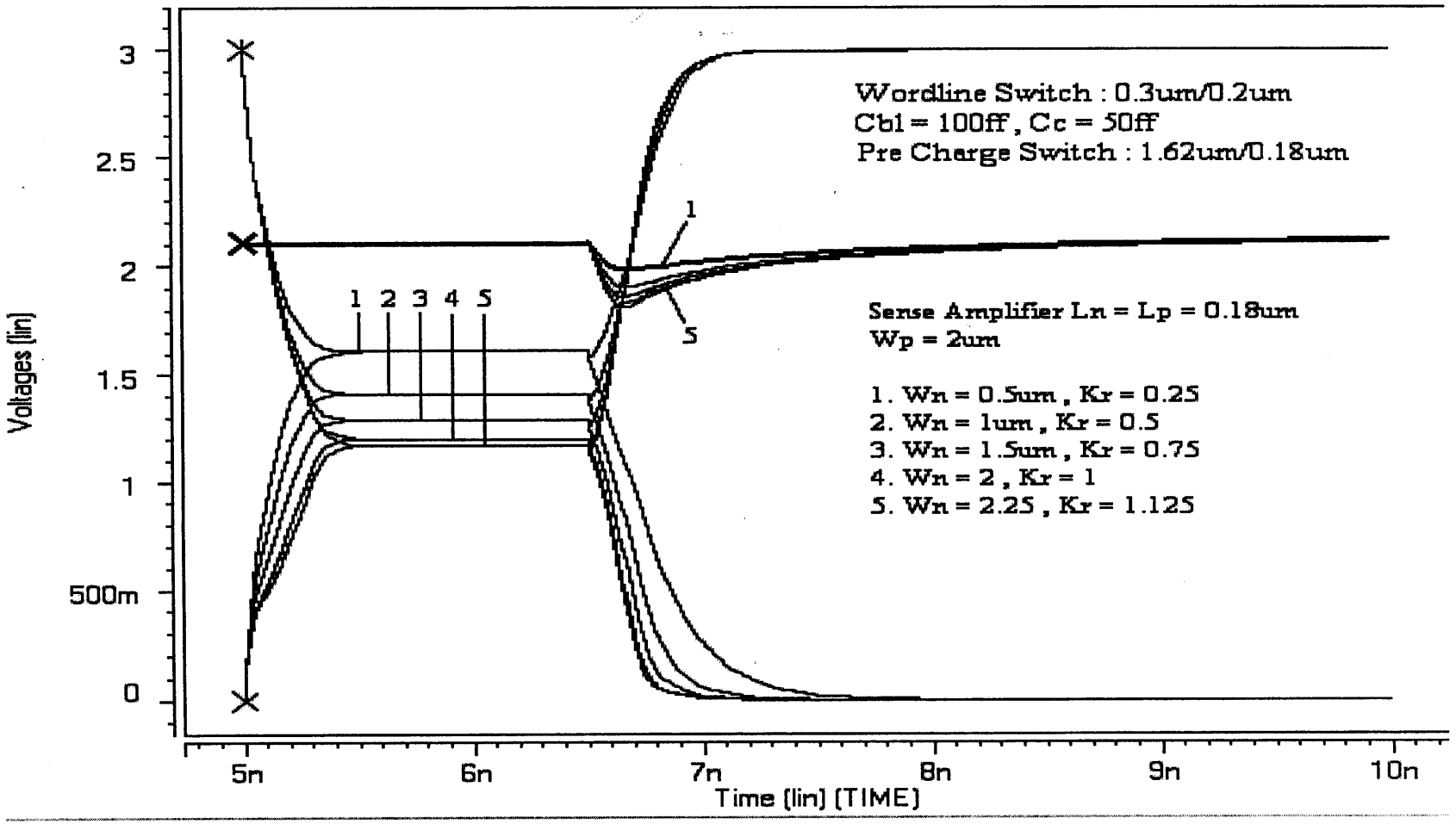


Figure 3.24 Effect of Varying k_r Ratio of Transistors in the Sense Amplifier, by Varying Wn, on Bit lines and Memory Cell for DRAM.

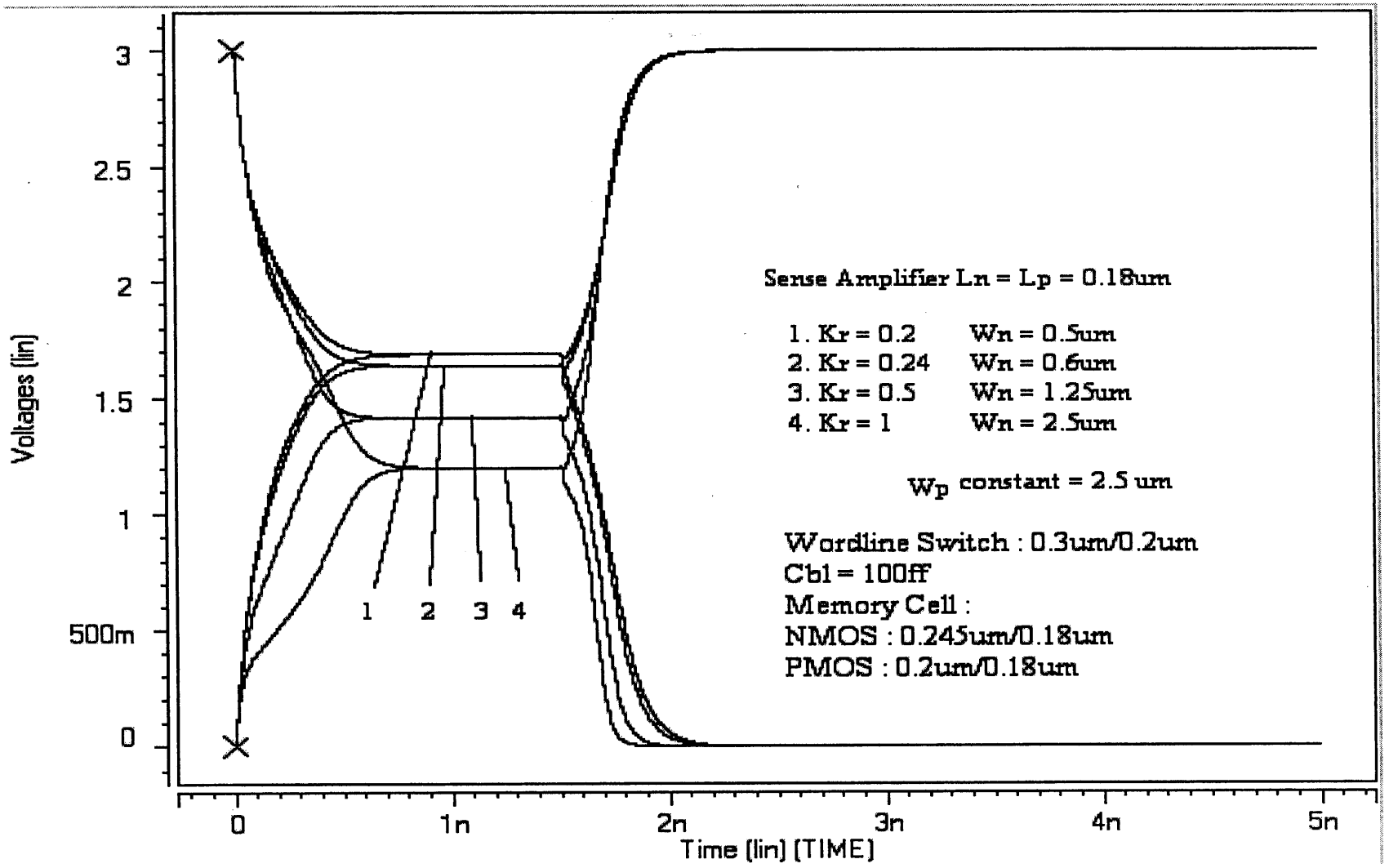


Figure 3.25 Effect of Varying k_r Ratio of Transistors in the Sense Amplifier by Varying Wn,, on Bit lines for SRAM.

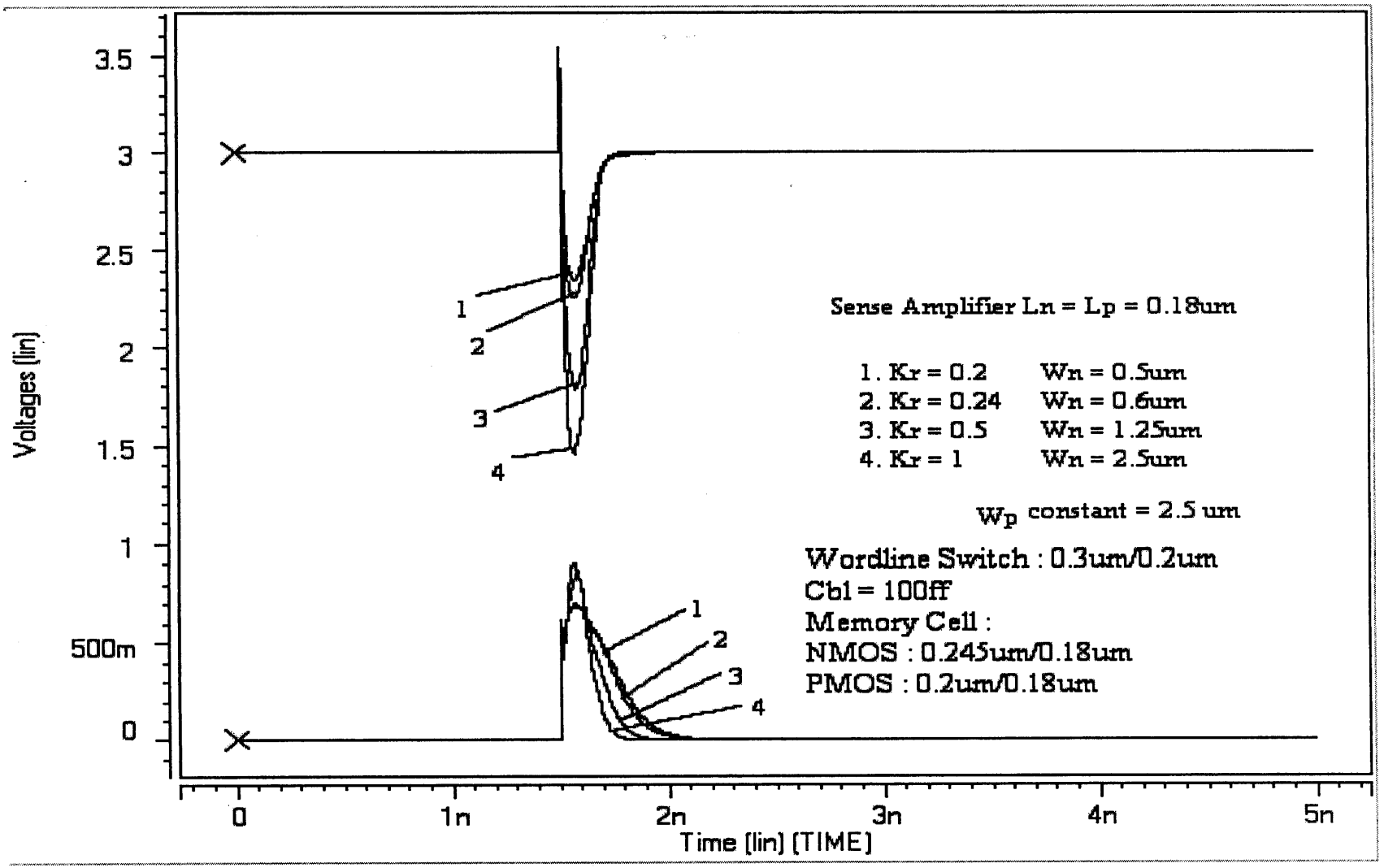


Figure 3.26 Effect of Varying k_r Ratio of Transistors in the Sense Amplifier, by Varying Wn,, on True and Complemented Data Outputs for the SRAM.

The Wn directly affects the dummy bit line. Hence when the width of Wn is increased, it should reduce the recovery time of the dummy bit line. This result is observed in Figures 3.24 and 3.25. The bit line recovery time is not affected, as its width is kept fixed. All other experimental results and their explanation is same as Experiment 3.3.4.

Using the experimental data and observations, graphs have been plotted below.

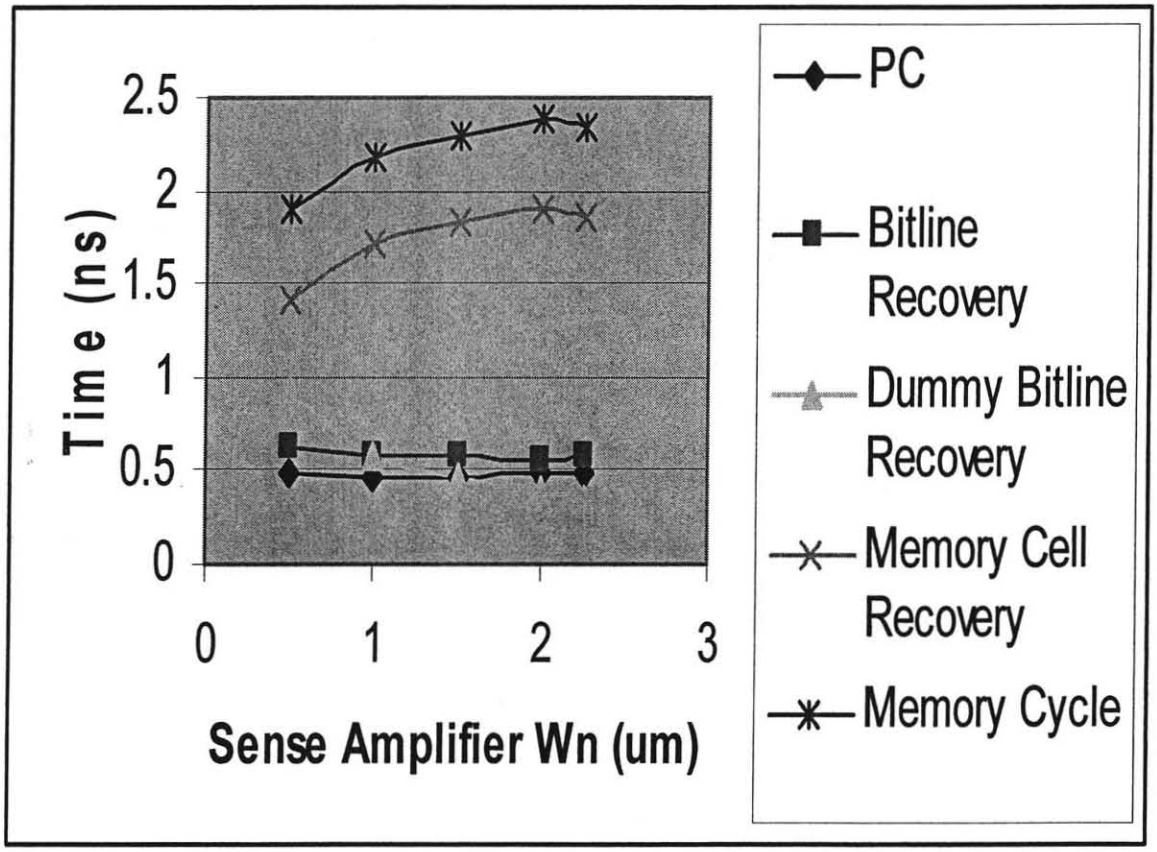


Figure 3.27 Effect of Increasing Sense Amplifier Wn, on Bit lines and Memory Cell for DRAM.

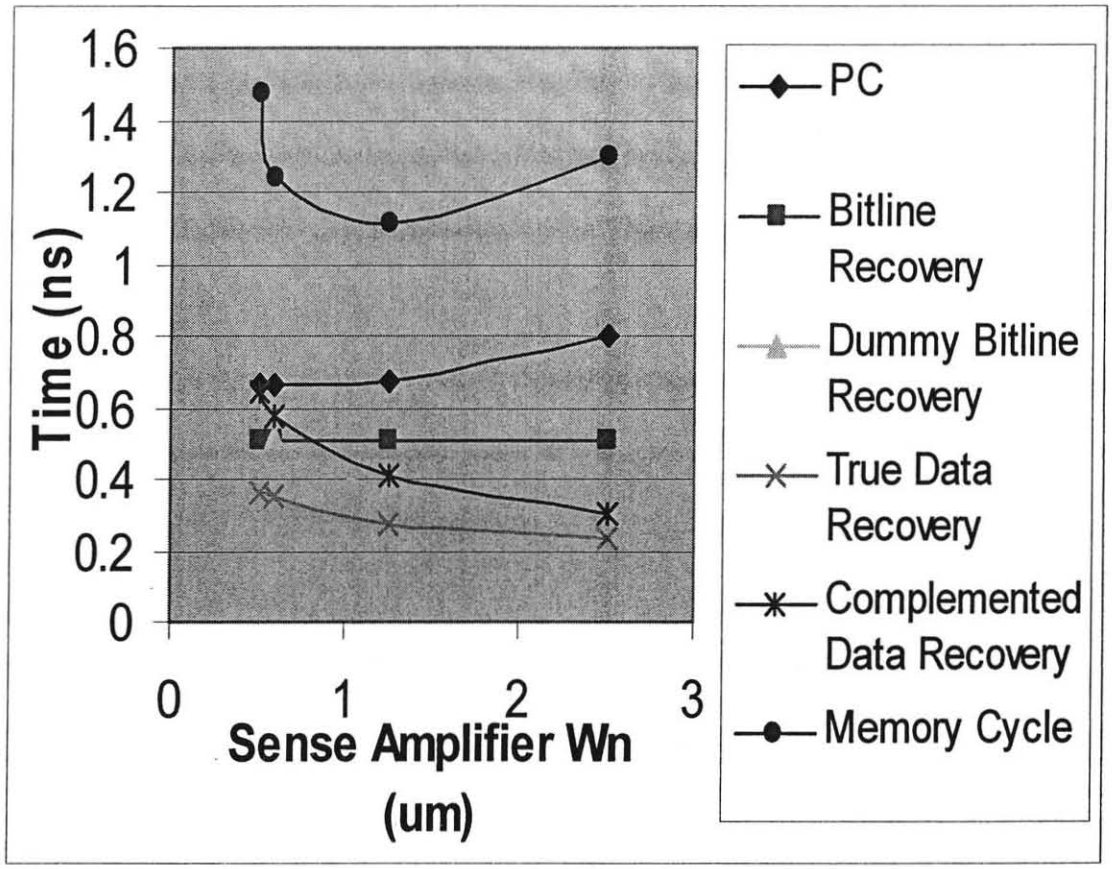


Figure 3.28 Effect of Increasing Sense Amplifier Wn, on Bit lines and True and Complemented Data Outputs for SRAM.

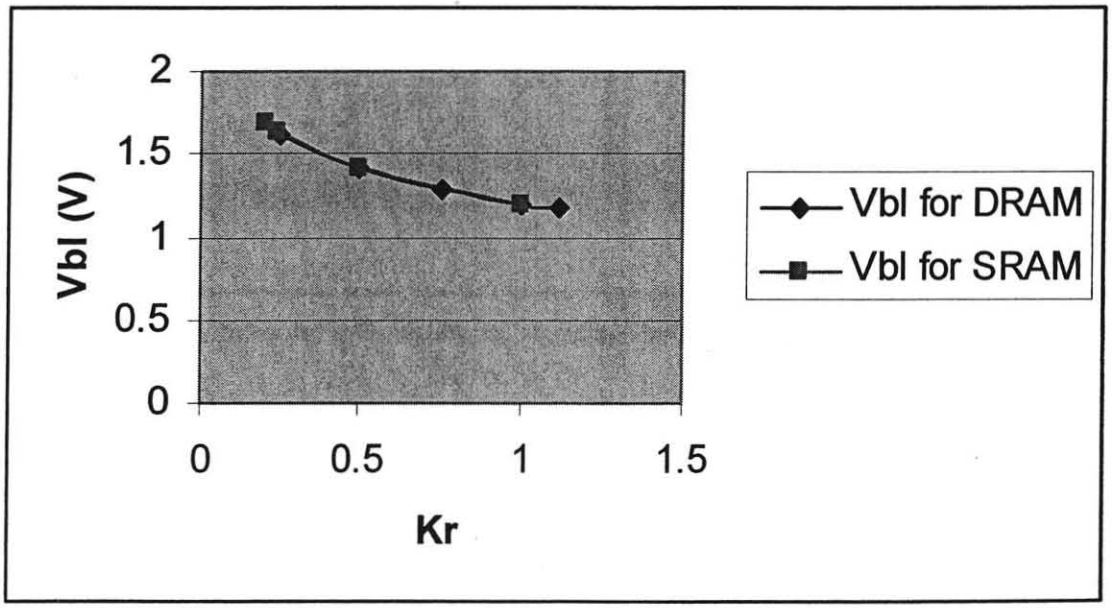


Figure 3.29 Effect of Increasing kr Ratio of Transistors in The Sense Amplifier, on the Bit line Common Voltage for DRAM and SRAM.

3.3.6 Memory Cell Parameters

The experimental results when the value of the memory capacitance Cc for DRAM was varied, by keeping the bit line capacitance constant are shown. The waveforms are shown in Figures 3.30 and 3.31 and the data used and observations made are shown in Table 3.11.

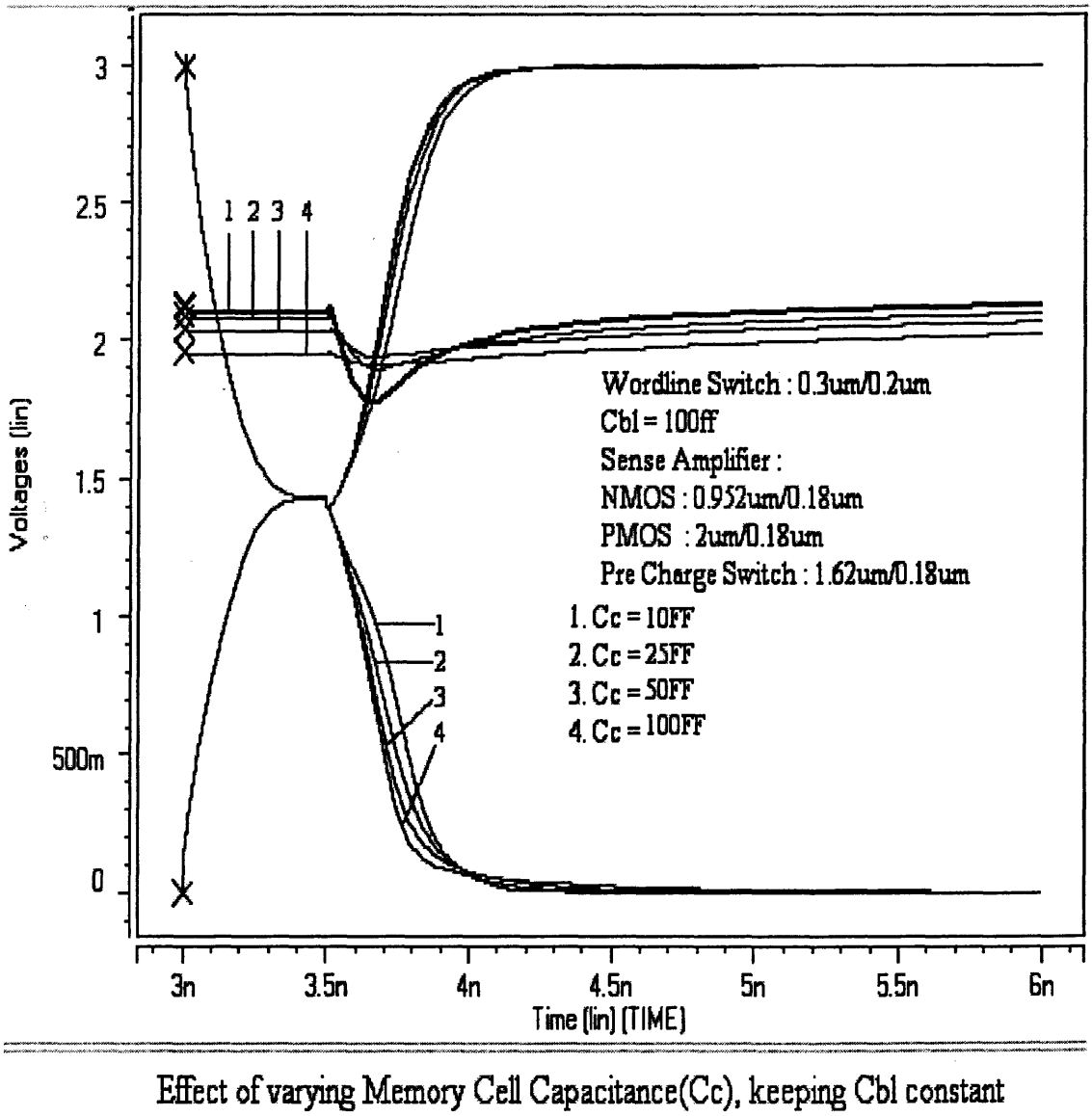
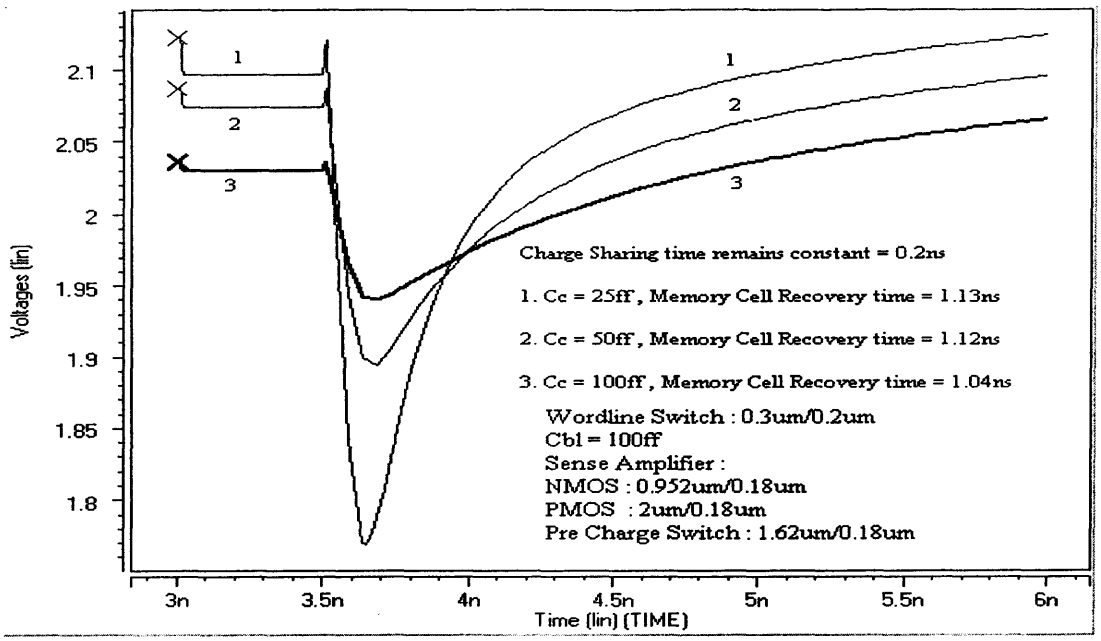


Figure 3.30 Effect of Varying Memory Cell Capacitance, on Bit lines and Memory Cell for DRAM.



Effect of varying Memory Cell Capacitance (Cc) on Memory Cell

Figure 3.31 Effect of Varying Memory Cell Capacitance, on Memory Cell for DRAM.

Table 3.11 Bit Line and Memory Cell Behavior as a Function of Memory Cell Capacitance for DRAM

Cc	Cbl/Cc	Time to merge bit lines (ns)	Bit line recovery time (ns)	Dummy Bit line recovery time (ns)	Initial voltage on memory cell (V)	memory cell recovery time (ns)	total memory cycle time (ns)
10	10	0.45	0.64	0.63	2.1	0.73	1.18
25	4	0.45	0.64	0.64	2.1	1.24	1.69
50	2	0.45	0.65	0.72	2.07	1.27	1.72
100	1	0.45	0.67	0.91	2.03	1.27	1.72

Figure 3.32 shows the waveforms observed when the area of the SRAM memory cell was increased by increasing the W/L ratio of memory cell transistors and keeping k_r constant. The experimental data and results for this experiment are tabulated in Table 3.12.

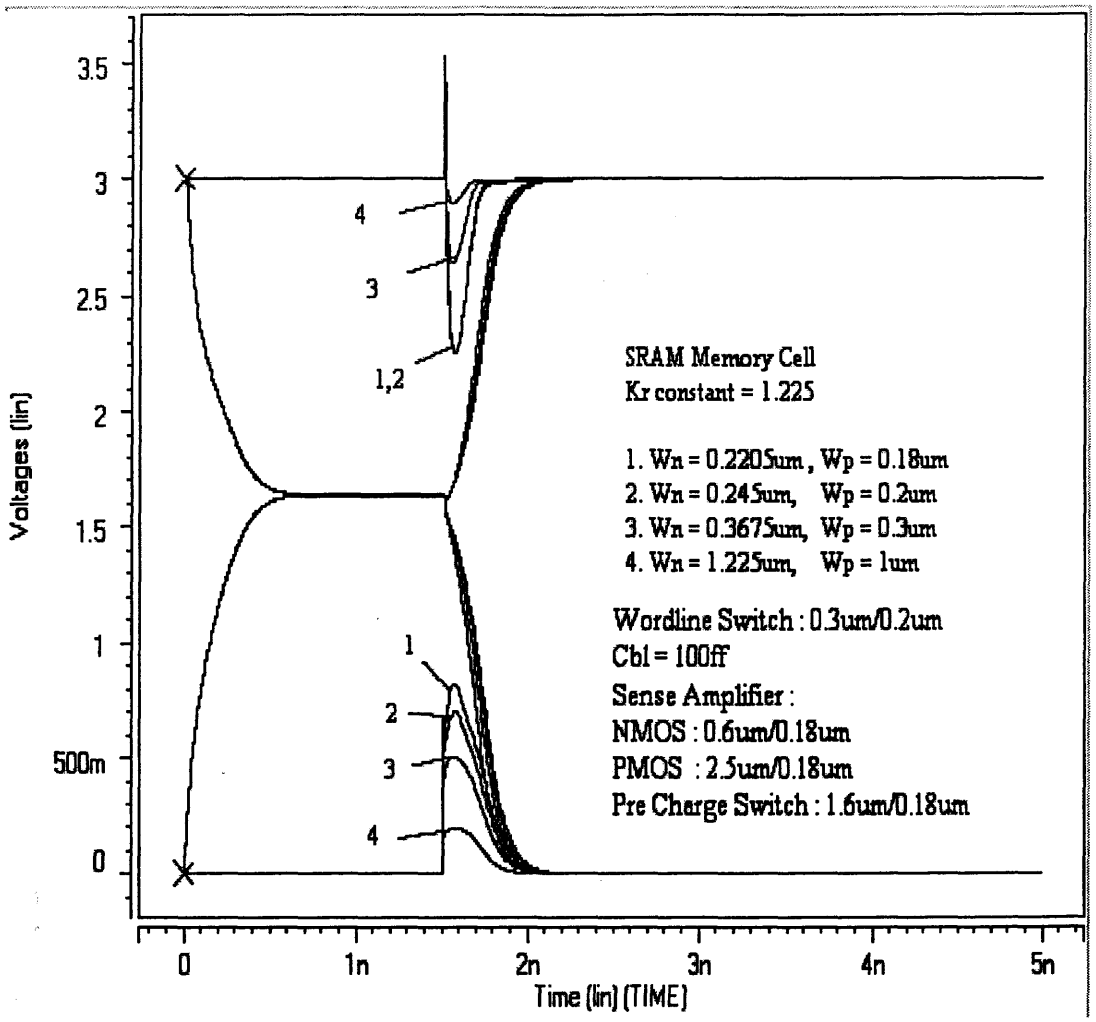


Figure 3.32 Effect of Varying Widths of the Transistors in the Memory Cell, Keeping k_r Constant, on Bit lines and True and Complemented Data for SRAM.

Table 3.12 Bit line and Memory Cell Behavior as a Function of Varying Widths of the Transistors in the Memory Cell for SRAM

Wn(um)	Wp(um)	Memory Cell Area (excluding access transistors) (sq-um)	True Data Recovery Time (ns)	Complemented" Recovery Time (ns)
0.2205	0.18	0.144	0.36	0.61
0.245	0.2	0.16	0.35	0.58
0.3675	0.3	0.2403	0.26	0.55
1.225	1	0.801	0.24	0.45

Figures 3.33 and 3.34 show the waveforms obtained when the k_r was varied by varying Wp and Wn respectively of the memory cell transistors. The results for these experiments have been tabulated in Tables 3.13 and 3.14.

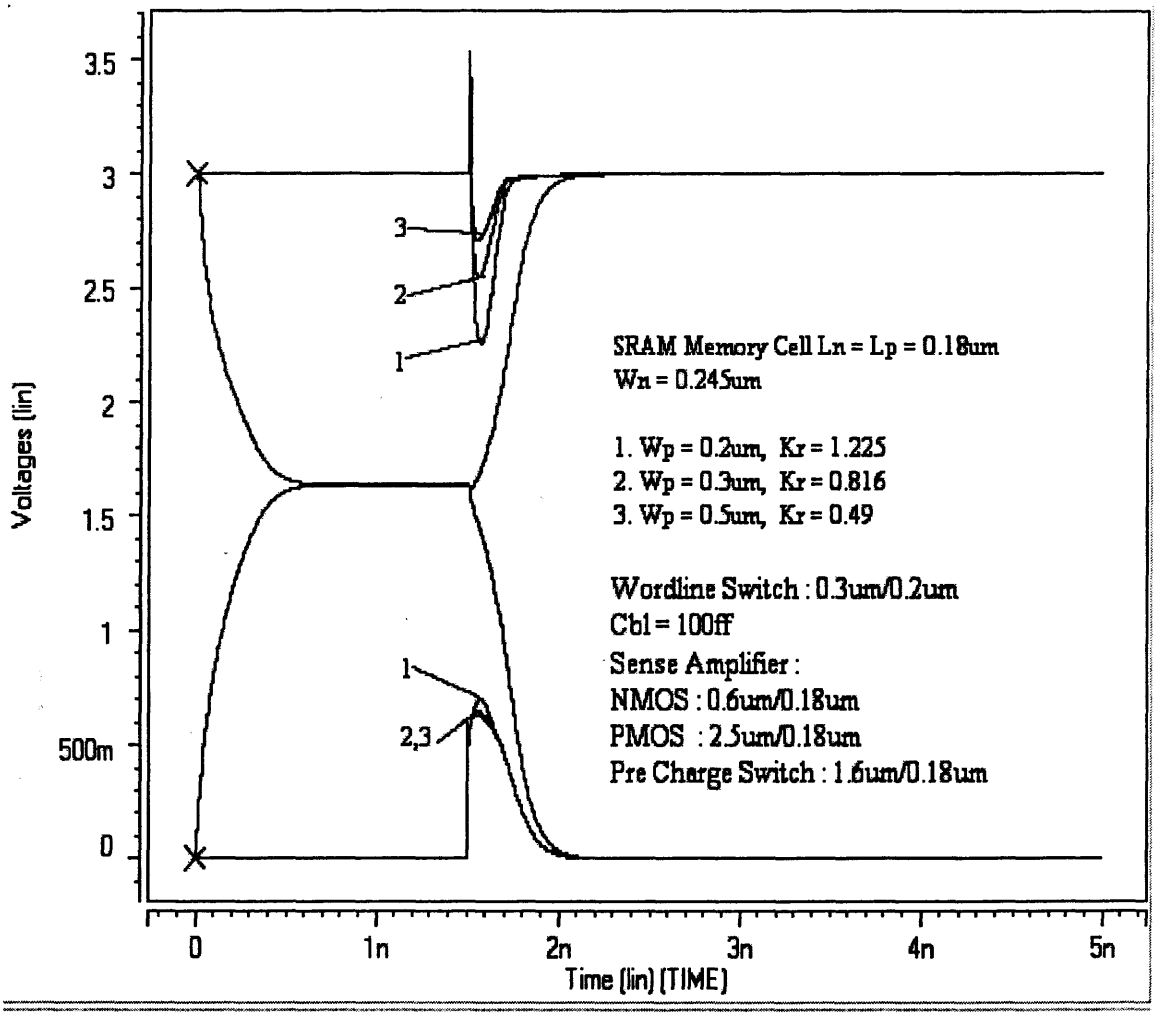


Figure 3.33 Effect of Varying k_r of Memory Cell by Varying Wp and Keeping Wn Constant, on Bit lines and True and Complemented Data for SRAM.

Table 3.13 Bit line and Memory Cell Behavior as a Function of k_r of Memory Cell by Varying Wp for SRAM

Wp (um)	kr	True Data Recovery Time (ns)	Complemented Data Recovery Time (ns)
0.2	1.225	0.35	0.58
0.3	0.816	0.28	0.58
0.5	0.49	0.25	0.58

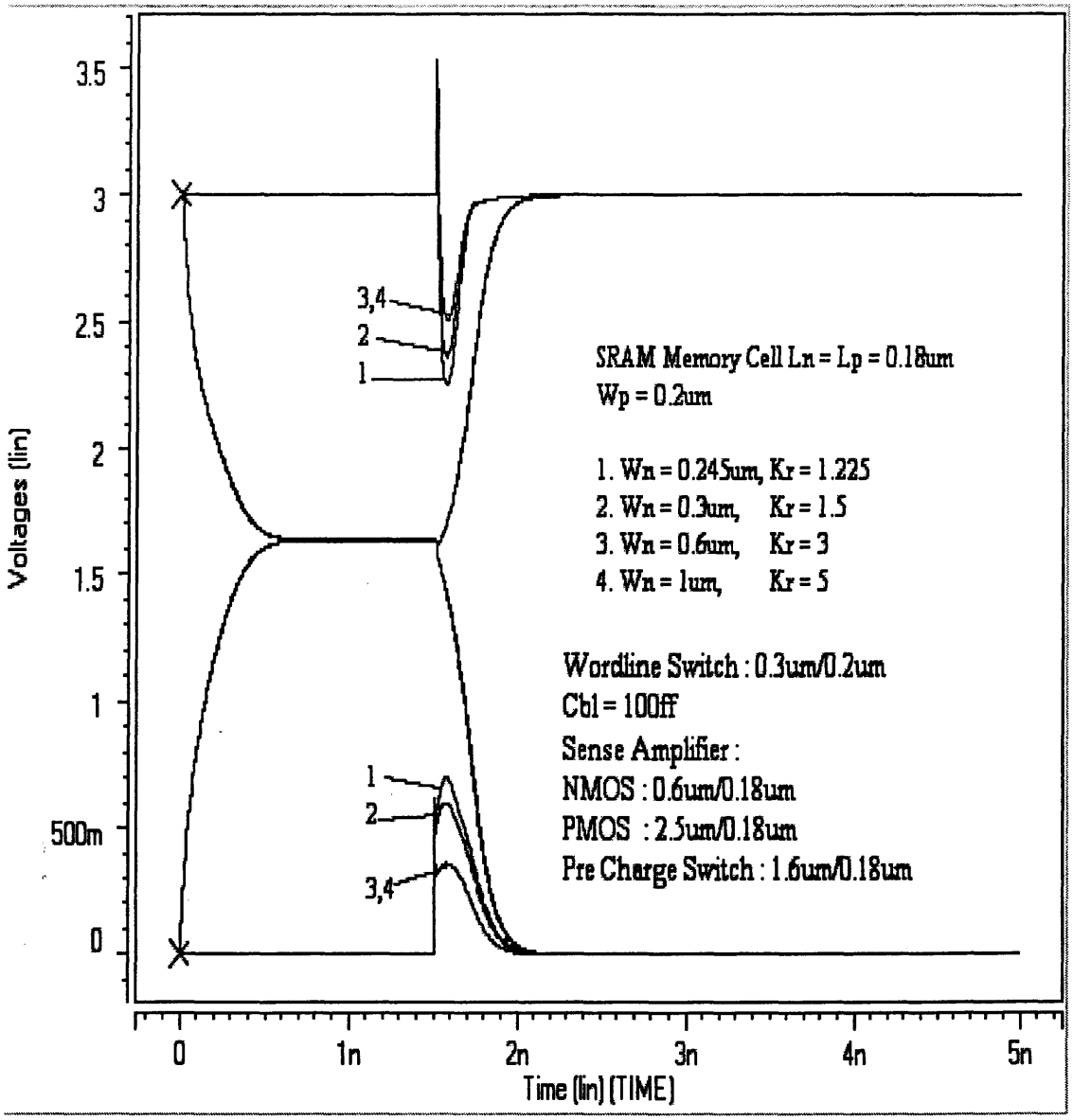


Figure 3.34 Effect of Varying k_r of Memory Cell by Varying Wn and Keeping Wp Constant, on Bit lines and True and Complemented Data for SRAM.

Table 3.14 Bit line and Memory Cell Behavior as a Function of k_r of Memory Cell by Varying Wn for SRAM

Wn(um)	kr	True Data Recovery Time (ns)	Complemented Data Recovery Time (ns)
0.245	1.225	0.35	0.58
0.3	1.5	0.35	0.57
0.6	3	0.36	0.51
1	5	0.36	0.51

Using experimental data from Tables 3.11, 3.12, 3.13 and 3.14, and from the observations recorded, graphs for the above experiments have been plotted in Figures 3.35, 3.36, 3.37, 3.38 and 3.39 below.

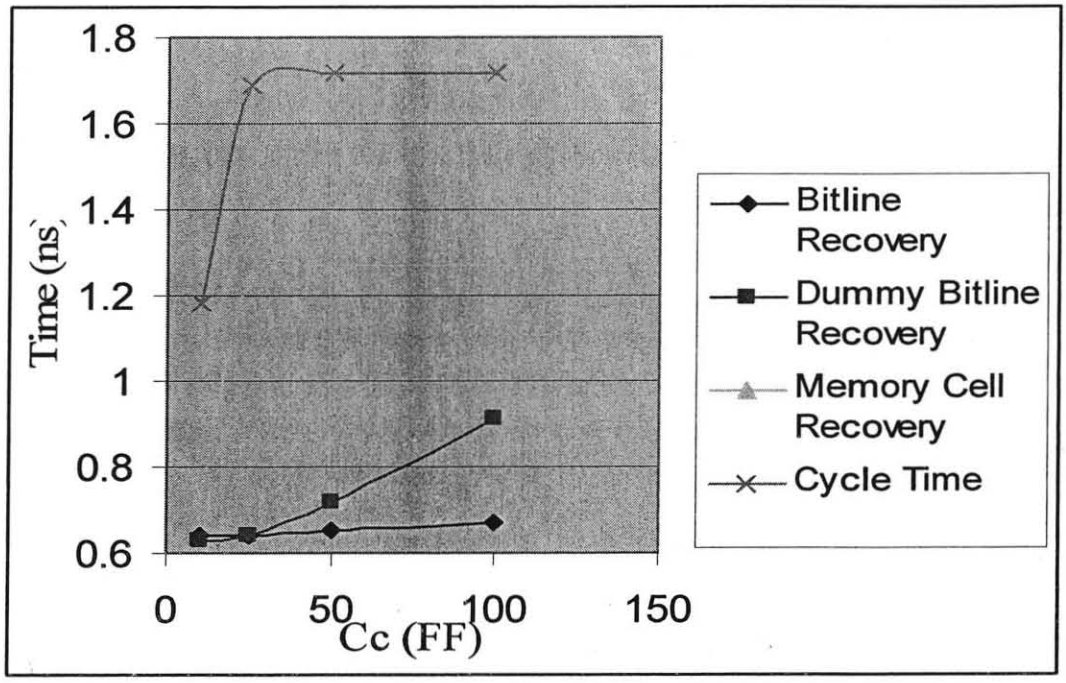


Figure 3.35 Effect of Increasing Memory Cell Capacitance, Cc, on Bit lines and Memory Cell for DRAM.

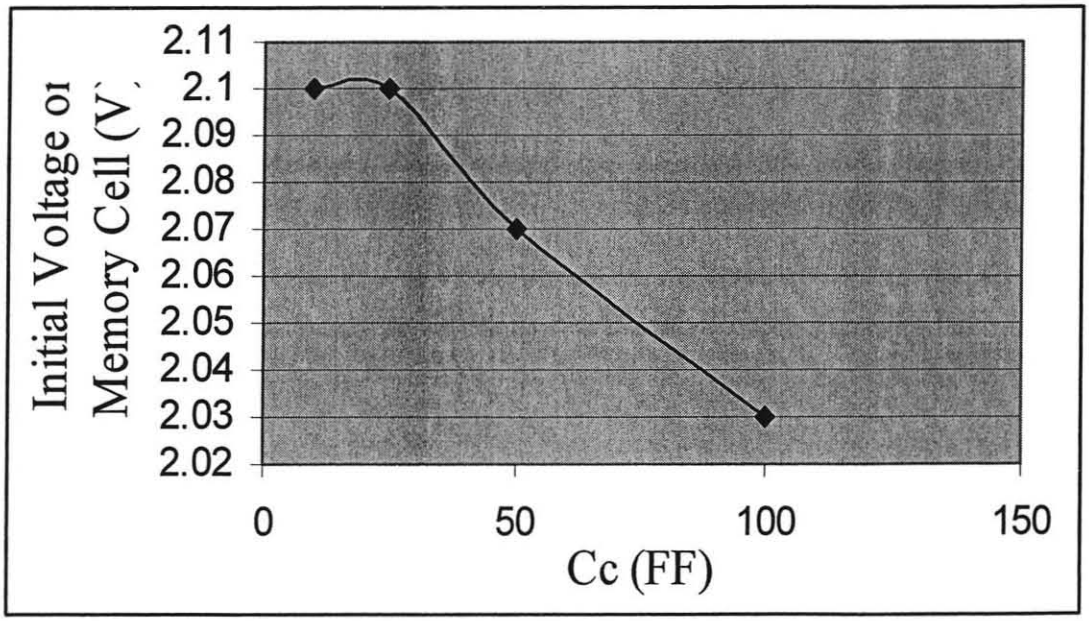


Figure 3.36 Initial Voltage on Memory Cell Versus Cc for DRAM.

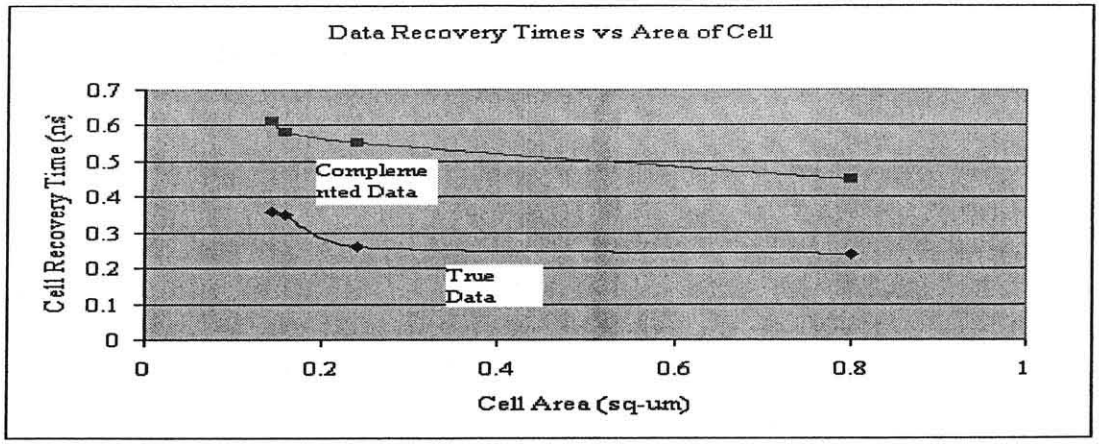


Figure 3.37 Effect of Increasing Area of Memory Cell by Increasing Wn and Wp of the Transistors in the Memory Cell, on the Memory Cell True and Complemented Data" Recovery Time for SRAM.

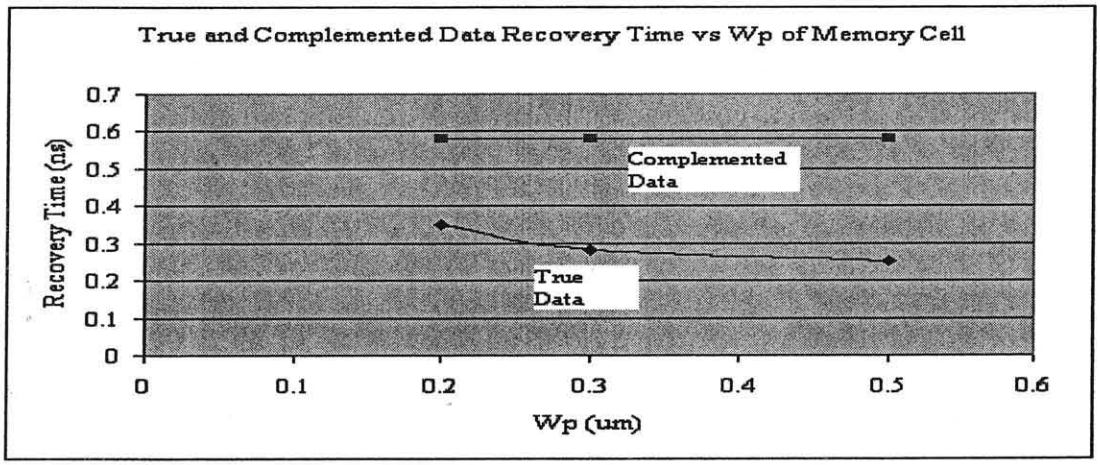


Figure 3.38 SRAM Memory Cell True and Complemented Data Recovery Time Versus Wp of Memory Cell, Keeping Wn Constant.

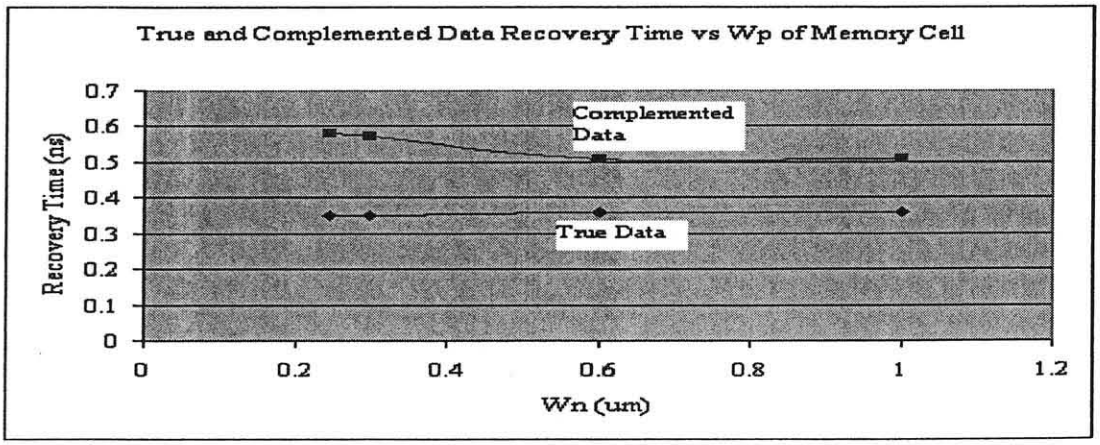


Figure 3.39 SRAM Memory Cell True and Complemented Data Recovery Time Versus Wn of Memory Cell, Keeping Wp Constant.

The memory cell capacitance directly affects the charge sharing process, and hence it should affect the ΔV. As Cc increases, the initial voltage on the memory cell goes on decreasing, but ΔV increases. Thus, a smaller sense amplifier could be used to detect the same amount of charge. Ideally, it would take more time to charge a higher memory capacitance, resulting in an increased memory cell recovery and cycle time. This theory is reinforced in Figures 3.30, 3.31 and 3.35 where, at Cc = 10ff, memory cell recovery time = 1.18 ns and at Cc = 100ff, memory cell recovery time = 1.72ns, for DRAM. In case of SRAM, as the memory cell area in increased, the parasitic capacitance of the nodes increases, reducing the initial dip in the memory cell true and complemented data output voltages, leading to reduced recovery time. This is seen in Figures 3.32 and 3.37. So, with a decrease in memory cell recovery time, and time to merge bit lines remaining almost constant, the memory cycle time is reduced.

The behavior of the bit lines is decided mostly by the sense amplifier. Since the sense amplifier dimensions were kept constant, the bit lines were unaffected as observed in Figures 3.32, 3.33 and 3.34. In case of DRAM, from Figure 3.35, the dummy bit line recovery time was slightly increased due to increase in Cc. One reasoning for this is that as the Cc increases, more current would be required to drive the bit line, but as word line width is fixed, this current cannot be supplied hence the bit line is slowed down.

As seen in Figure 3.36, as Cc increases, the initial voltage on the DRAM memory cell decreases slightly. Also, it is interesting to notice the fact that the read time of the memory cell is constant (Figure 3.31) at 0.15ns. It is the restore time and hence the memory cell dip that the memory cell capacitance affects.

The P Channel transistors in SRAM Cell affect the true data output and N Channel affect the complemented data output. Increasing Wp, should make the true data output recover faster and increasing Wn should make the complemented data output recover faster. This is seen in Figures 3.33, 3.34, 3.38 and 3.39.

3.3.7 Word Line Switch

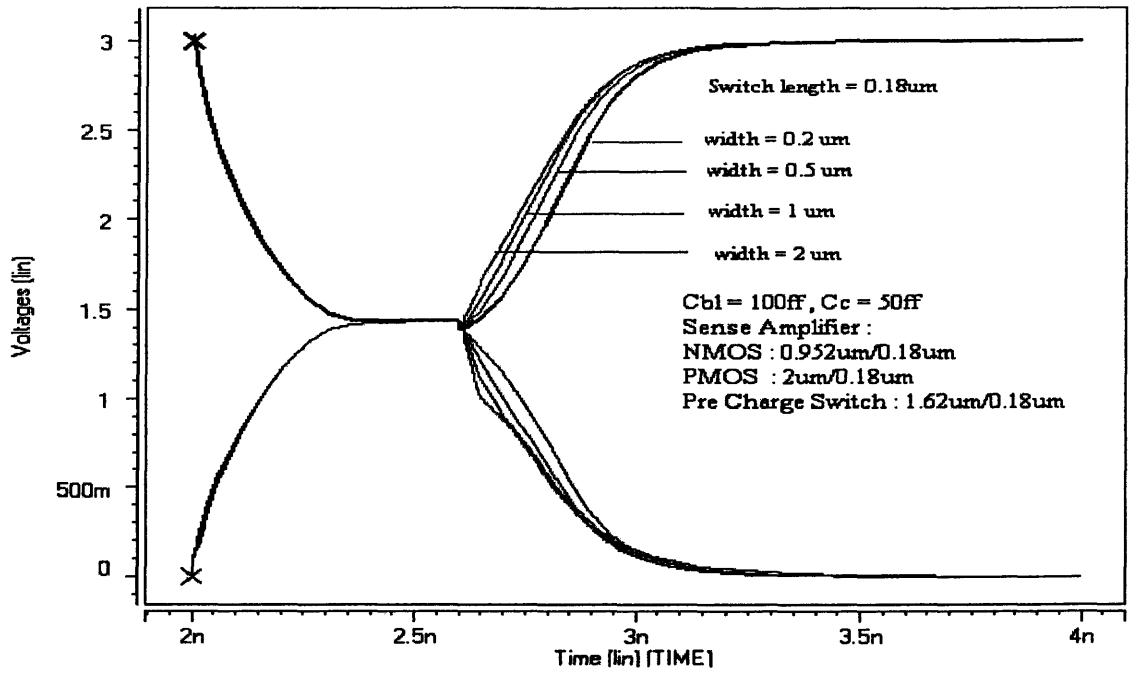
The experimental results when the width of the word line switch was varied, keeping all other parameters constant are shown below. The waveforms for DRAM are shown in Figures 3.40 and 3.41 and the data used and observations made are shown in Table 3.15. The waveforms for SRAM are shown in Figures 3.42 and observations are recorded in Table 3.16.

Table 3.15 Bit line and Memory Cell Behavior as a Function of Word Line Switch Width for DRAM

Word line width (µm)	Memory cell initial voltage (V)	Initial dip in memory cell voltage (V)	Memory Cell Read time (ns)	Memory Cell Restore time (ns)	Memory Cell Recovery time (ns)
0.2	2.01	0.15	0.21	0.61	0.82
0.5	2.04	0.205	0.16	0.53	0.69
1	2.05	0.22	0.12	0.37	0.49
2	2.03	0.235	0.1	0.2	0.3

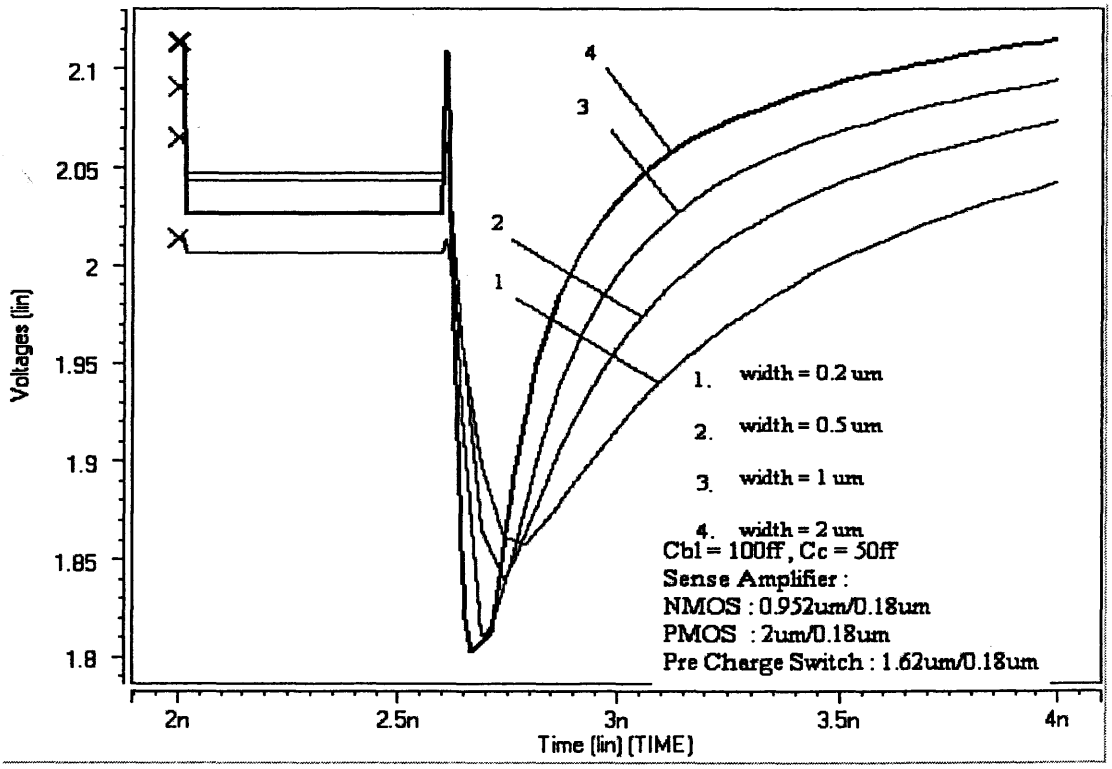
Table 3.16 Bit line and Memory Cell Behavior as a Function of Word Line Switch Width for SRAM

width	True Data Recovery Time (ns)	Complemented Data Recovery Time (ns)
0.2	0.34	0.6
0.3	0.35	0.58
0.5	0.34	0.58
1	0.39	0.59
2	0.44	0.59



Effect of varying wordline switch width on Bitlines

Figure 3.40 Effect of Varying Word Line Switch Width on Bit lines for DRAM.



Effect of varying wordline switch width on the memory cell

Figure 3.41 Effect of Varying Word Line Switch Width on Memory Cell for DRAM.

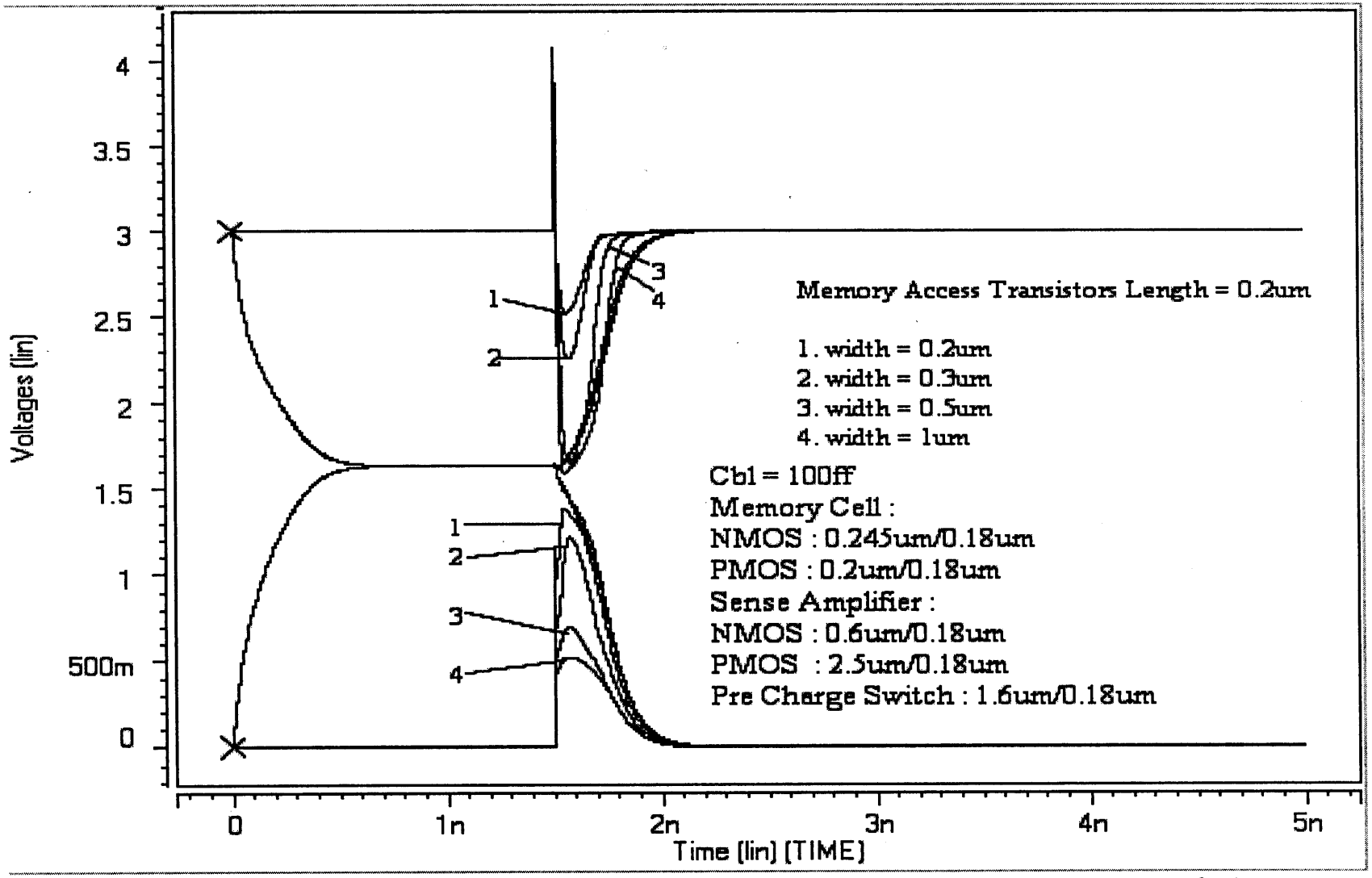


Figure 3.42 Effect of Varying Word Line Switch Width on Bit Lines and True and Complemented Data Outputs for SRAM.

Table 3.18 SRAM Three Dimensional Plot Points and Variables Used to Plot These Points

Point	Cycle Time (ns)	Chip Space (um^2)	Cbl (ff)	Sense nch (um)	Sense pch (um)	PC (um)	WL switch (um)	Cell nch (for SRAM)	Cell pch (for SRAM)	PC Time (ns)	Recovery Time (ns)
S1	1.24	1.404	100	0.6/0.18	2.5/0.18	1.6/0.18	0.3/0.2	0.245/0.18	0.2/0.18	0.66	0.58
S2	0.94	4.291	100	1.92/0.18	8/0.18	4/0.18	0.3/0.2	0.245/0.18	0.2/0.18	0.59	0.35
S3	1.28	8.856	500	3.6/0.18	15/0.18	12/0.18	0.3/0.2	0.245/0.18	0.2/0.18	0.43	0.85
S4	3.17	2.016	500	0.6/0.18	2.5/0.18	5/0.18	0.3/0.2	0.245/0.18	0.2/0.18	0.63	2.54
S5	1.27	0.626	100	0.24/0.18	1/0.18	1/0.18	0.3/0.2	0.245/0.18	0.2/0.18	0.68	0.89

By using the cycle time, chip space and Cbl values given in Tables 3.17 and 3.18, the 3D plots were plotted for DRAM and SRAM. These are shown if Figures 3.44 and 3.45.

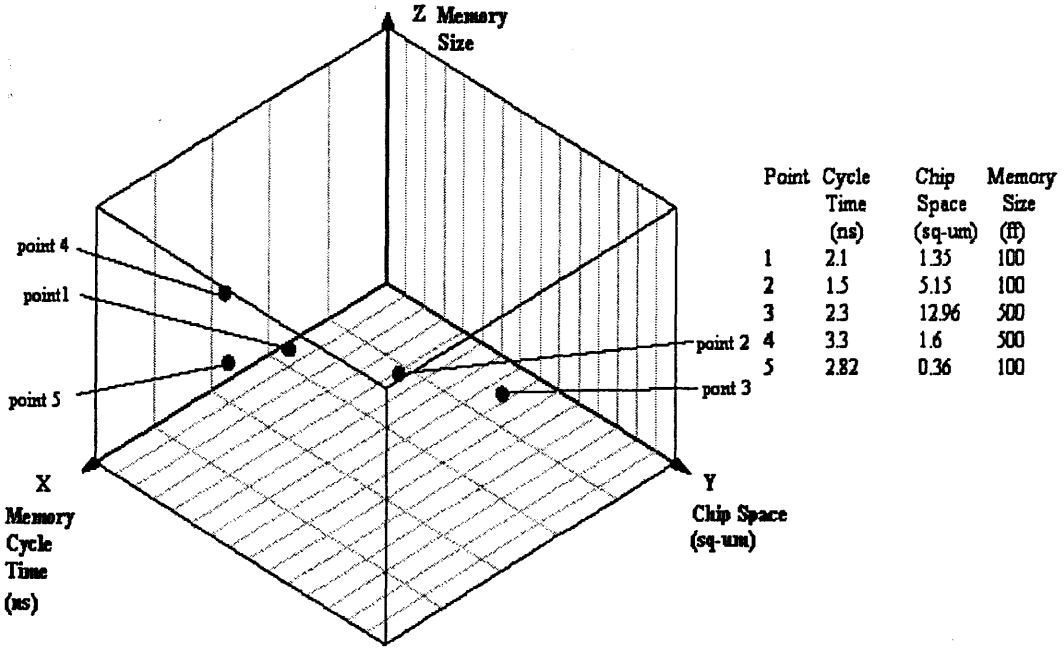
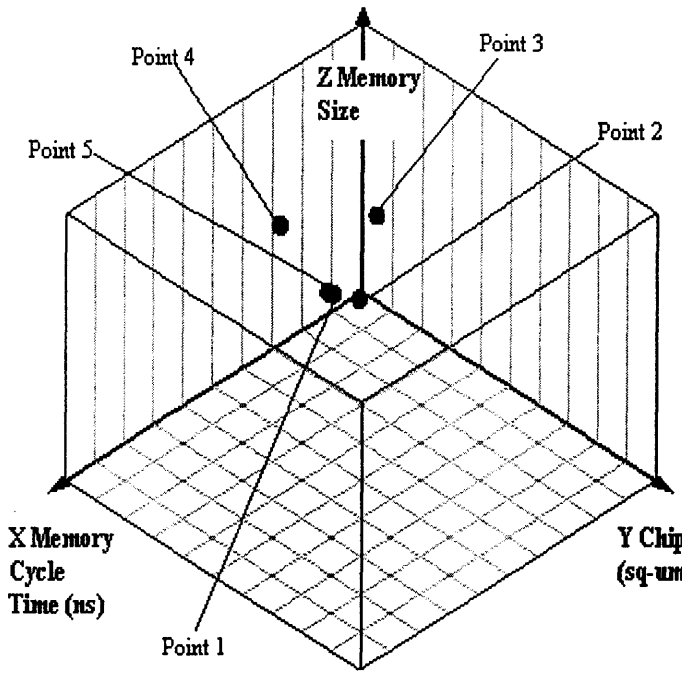


Figure 3.46 Three Dimensional Plot Showing Various Operating Points for DRAM.



Point	Cycle Time (ns)	Chip Space (sq-um)	Memory Size (ff)
1	1.24	1.404	100
2	0.94	4.291	100
3	1.28	8.856	500
4	3.17	2.016	500
5	1.27	0.626	100

Figure 3.47 Three Dimensional Plot Showing Various Operating Points for SRAM.

Point 1 has been considered as the reference point. Referring to Point 2 for both DRAM and SRAM, it can be seen that at the same value of Cbl, to reduce the memory cycle time to two thirds of its initial value, the sense amplifier area had to be increased by three to four times. This would lead to a "3-4N" fold increase in Chip Area, for an N x N bit Memory array size. Conversely, in case of Point 5, where the focus was on reducing the sense amplifier area, it can be seen that when the sense amplifier area was reduced to half to one fourth of its initial area, the memory cycle time increased to approximately $4/3^{rd}$ of the initial cycle time. In Point 3 for DRAM and SRAM, the Cbl value was increased to five times the original Cbl value. To keep the memory cycle time constant, the sense amplifier area had to be increased by ten times for DRAM and approximately six times for SRAM. This proved the fact that SRAM is much more sensitive than DRAM.

3.4.2 Experiment II – 3D Line Plots

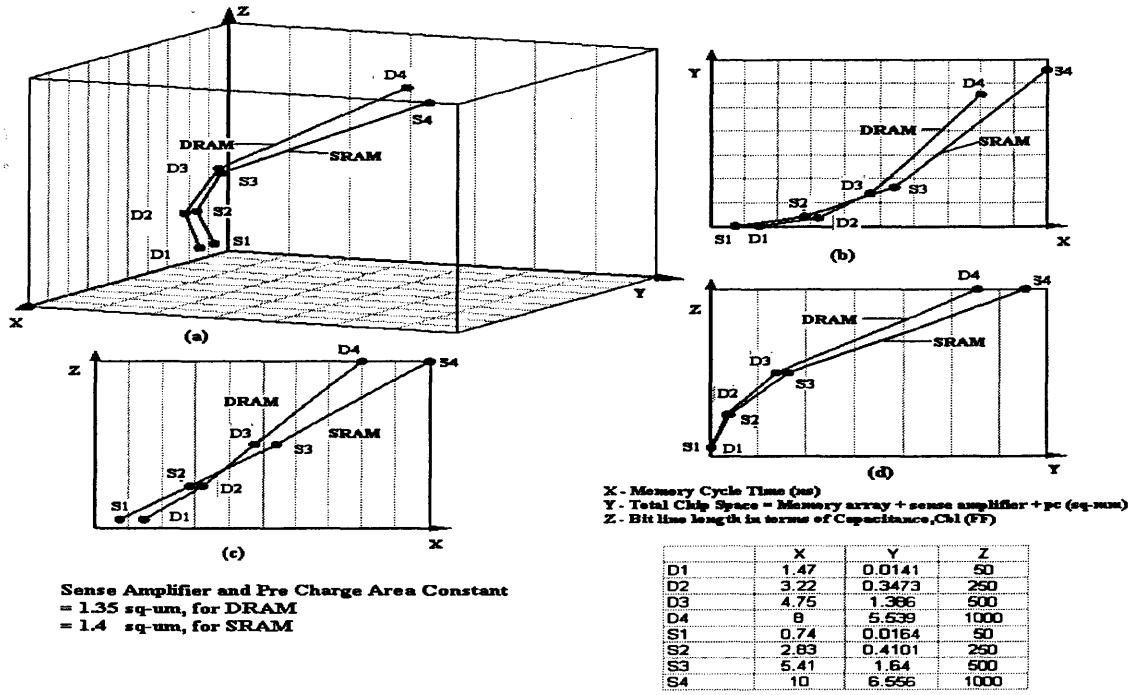
3.4.2.1 Sense Amplifier and Precharge Area Constant. The experimental results obtained when the dimensions of the sense amplifier and precharge switch were kept constant, are shown in Tables 3.19 and 3.20 for DRAM and SRAM respectively. The area of the sense amplifier and PC switch were kept constant at 1.35um^2 (for DRAM) and 1.404 um^2 (for SRAM). Figure 3.46 shows three dimensional line plots demonstrating the tradeoffs between the three performance parameters, when sense amplifier and precharge switch dimensions were kept constant.

Table 3.19 Operating Points Showing Performance Parameters and Variable Values for Line Graph Keeping Sense Amplifier and Precharge Area Constant at 1.35um^2 for DRAM

Point	total memory cycle time (ns)	Cbl (ff)	Time to merge bit lines (ns)	memory cell recovery time (ns)	#Cells	Total sense amp + pc area(sq-um) (a)	Total memory array area (0.2592 * # cells) (sq-um) (b)	total chip area (sq-um) (a) + (b)	total chip area (sq-mm) (a) + (b)
Point D1	1.47	50	0.25	1.22	231*231	311.85	13831.1	14143	0.0141
Point D2	3.22	250	0.9	2.32	1155*1155	1559.25	345778.7	347338	0.3473
Point D3	4.75	500	1.76	2.99	2310*2310	3118.5	1383115	1386233	1.3862
Point D4	8	1000	3.3	4.7	4620*4620	6237	5532460	5538697	5.5386

Table 3.20 Operating Points Showing Performance Parameters and Variable Values for Line Graph Keeping Sense Amplifier and Pre Charge Area Constant at 1.4um^2 for SRAM

Point	total memory cycle time (ns)	Cbl (ff)	Time to merge bitlines (ns)	Worst Case Recovery time (ns)	#Cells	Total sense amp + pc area(sq-um) (a)	Total memory array area (4.129 * # cells) (sq-um) (b)	total chip area (sq-um) (a) + (b)	total chip area (sq-mm) (a) + (b)
Point S1	0.74	50	0.41	0.33	63*63	88.2	16388	16476.2	0.0164
Point S2	2.83	250	1.5	1.33	315*315	441	409700.02	410141.02	0.4101
Point S3	5.41	500	2.76	2.65	630*630	882	1638800.1	1639682.1	1.6396
Point S4	10	1000	5	5	1260*1260	1764	6555200.4	6555696.44	6.5556



	X	Y	Z
D1	1.47	0.0141	50
D2	3.22	0.3473	250
D3	4.75	1.366	500
D4	8	5.539	1000
S1	0.74	0.0164	50
S2	2.83	0.4101	250
S3	5.41	1.64	500
S4	10	6.556	1000

Figure 3.48 (a) Three Dimensional Line Plot Showing Tradeoffs Between Memory Cycle Time(ns), Total Chip Space(mm^2) and Bit Line Capacitance(ff), for DRAM and SRAM. The Sense Amplifier and Pre Charge Area was Constant at 1.35um^2 for DRAM and 1.4um^2 for SRAM. (b) Tradeoff Between Total Chip Space(mm^2) and Memory Cycle Time(ns). (c) Tradeoff Between Bit Line Capacitance(ff) and Memory Cycle Time(ns). (d) Tradeoff Between Bit Line Capacitance(ff) and Total Chip Space(mm^2).

Since the sense amplifier and precharge switch dimensions were kept constant, the sensitivity of the sense amplifier was fixed. Sensitivity being fixed, increasing the Cbl value would lead to an increase in memory cycle time. This result was observed in Figure 3.46(c). Referring to Figure 3.46(c), it was observed that SRAM was faster than DRAM at lower values of Cbl but as Cbl value was increased from 250ff to 500ff, memory cycle time for DRAM reduced as compared to SRAM.

Total chip space depends on the size of the memory array and the dimensions of the sense amplifier and precharge switch. Memory array size is decided by the length of the Bit line. Thus, the longer the bit line, the higher the Cbl value and the Chip Space. Figure 3.62(d) shows this tradeoff.

Referring to Figure 3.46(b), it can be seen that, given a particular value of bit line length, SRAM occupied more chip space and held fewer number of cells as compared to DRAM. This effect was more pronounced when the values of Cbl was increased beyond 500ff. Also, for high values of Cbl, SRAM becomes slower than DRAM.

3.4.2.2 Memory Size(Cbl) Constant. The experimental results obtained when the Cbl was kept constant at 100ff, are shown in Tables 3.21 and 3.22 for DRAM and SRAM respectively. The number of memory cells along the length of the Bit Line was constant at 462 for DRAM and 126 for SRAM. A symmetrical array has been considered for calculation purpose. Thus, the total memory array size was constant at 462*462 for DRAM and 126*126 for SRAM. Figure 3.47 shows three dimensional line plots demonstrating the tradeoffs between the three performance parameters for the case of Cbl held constant. Time to merge Bit lines was kept constant at 0.42ns for DRAM and 0.61ns for SRAM, by adjusting the width of the precharge switch. This was done to observe the

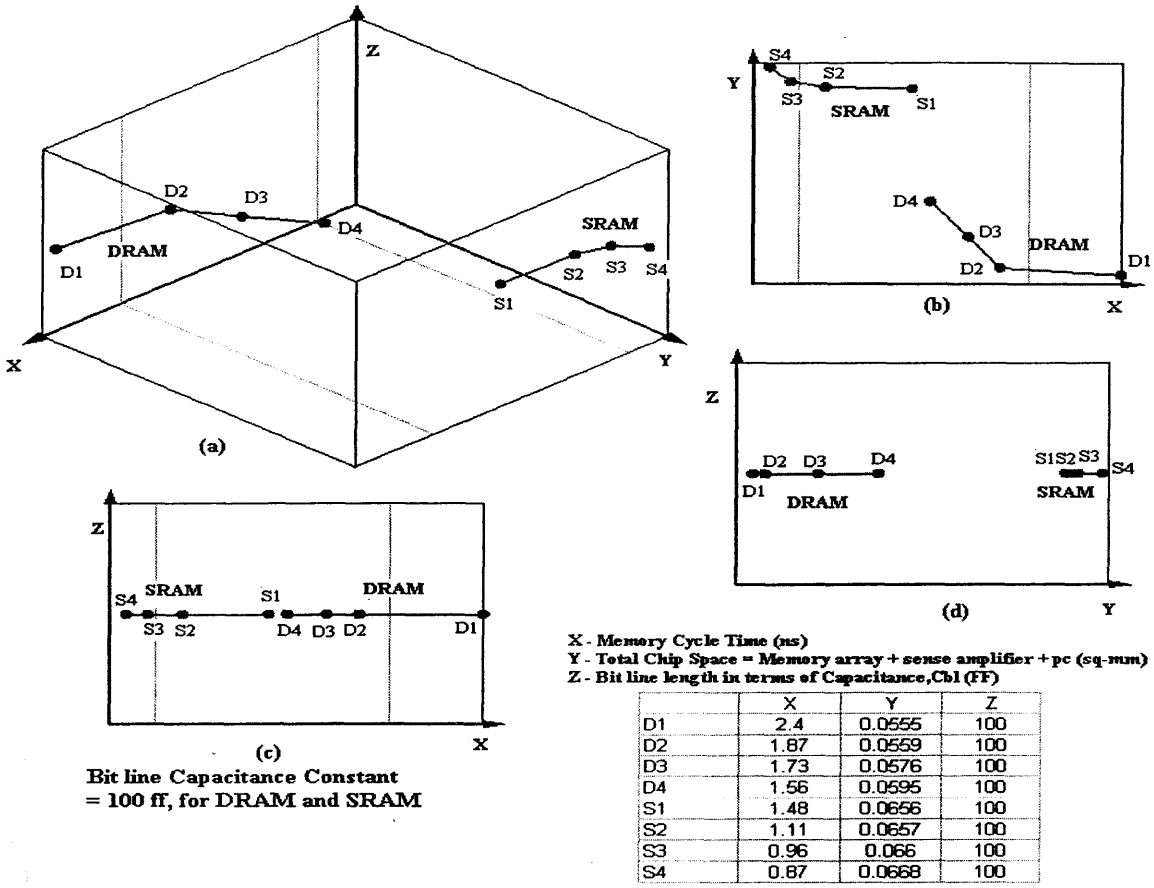
effect of increasing the bit line capacitance value on the memory cell (or worst case) recovery time.

Table 3.21 Operating Points Showing Performance Parameters and Variable Values for Line Graph for DRAM Keeping Cbl Constant at 100ff

Point	Sense Amp Wn (um)	Sense Amp Wp (um)	PC width (um)	Cycle time (ns)	Sense Amp + PC Area (sq-um)	Memory Cell Recovery Time (ns)	Total sense amp + pc area(sq-um) (a)	total chip area (sq-um) (a) + 0.2592*#Cells	total chip area (sq-mm) (a) + (b)
Point D1	0.238/0.18	0.5/0.18	1/0.18	2.4	0.445	1.98	205.59	55530.19	0.0555
Point D2	0.952/0.18	2/0.18	1.62/0.18	1.87	1.35	1.45	623.7	55948.3	0.0559
Point D3	3.8/0.18	8/0.18	4.2/0.18	1.73	5	1.31	2310	57634.6	0.0576
Point D4	7.14/0.18	15/0.18	7.2/0.18	1.56	9.2	1.14	4250.4	59575	0.0595

Table 3.22 Operating Points Showing Performance Parameters and Variable Values for Line Graph for SRAM Keeping Cbl Constant at 100ff

Point	Sense amp Wn (um)	Sense amp Wp (um)	PC width (um)	total memory cycle time (ns)	Sense Amp + PC Area (sq-um)	Worst Case recovery time (ns)	Total sense amp + pc area(sq-um) (a)	total chip area (sq-um) (a) + 4.129*#Cells	total chip area (sq-mm) (a) + (b)
Point S1	0.192	0.8	1	1.48	0.537	0.87	67.662	65619.666	0.0656
Point S2	0.84	3.5	2	1.11	1.922	0.5	242.172	65794.176	0.0657
Point S3	1.92	8	4	0.96	4.3	0.35	541.8	66093.804	0.066
Point S4	4.8	20	9	0.87	10.5	0.26	1323	66875.004	0.0668



	X	Y	Z
D1	2.4	0.0555	100
D2	1.87	0.0559	100
D3	1.73	0.0576	100
D4	1.56	0.0595	100
S1	1.48	0.0656	100
S2	1.11	0.0657	100
S3	0.96	0.066	100
S4	0.87	0.0668	100

Figure 3.49 (a) Three Dimensional Line Plot Showing Tradeoffs between Memory Cycle Time(ns), Total Chip Space(mm^2) and Bit Line Capacitance(ff). The Bit Line Capacitance was Constant at 100ff for Both DRAM and SRAM. (b) Tradeoff Between Total Chip Space(mm^2) and Memory Cycle Time(ns). (c) Tradeoff Between Bit Line Capacitance(ff) and Memory Cycle Time(ns). (d) Tradeoff Between Bit Line Capacitance(ff) and Total Chip Space(mm^2).

To study the design tradeoffs between memory cycle time and chip space, when Cbl is kept constant, the chip space has to be varied. Two constituents of the chip space are the memory array area and the sense amplifier and precharge area. Cbl being fixed, the memory array area is constant and the total chip space is varied by varying the sense amplifier and precharge switch dimensions.

As the sense amplifier and precharge switch areas are increased, the sensitivity of the sense amplifier should be increased, leading to a reduced memory cycle time. Figure 3.47 (b) shows this tradeoff between chip space and memory cycle time, for DRAM and

SRAM. When the chip space was varied, the curves for DRAM and SRAM showed slight variation in the memory cycle time around their optimal operating points. Both curves show a negative slope meaning an increase in chip space leads to a reduction in memory cycle time.

The slope ($\Delta y/\Delta x$) for the DRAM curve is more than SRAM. Here, Δy is the change in chip space and Δx is the change in memory cycle time. Using the observed data in Tables 3.21 and 3.22, calculated value of DRAM slope is approximately twice that of SRAM. Thus, for reduction in the cycle time (Δx) by the same amount, DRAM chip space has to be increased (Δy) by twice that of the SRAM chip space. This is also seen in Figure 3.47(d), where the SRAM operating points are closely spaced as compared to DRAM. Similarly, a reduction in the chip space (Δy) by the same amount, would result in a memory cycle time increase (Δx) for the SRAM which is twice that of the DRAM.

From Figure 3.47(b), Memory Cycle time for DRAM is always more than that for SRAM, but the chip space for DRAM is always less than that of SRAM. This result proves the theory that was stated in the beginning of this thesis – SRAM obtains its speed at the cost of its size.

To reduce cycle time, the chip space had to be increased. Iit is required to increase the dimensions of both the sense amplifier and the PC switch. A dimension increase of only the sense amplifier, keeping PC constant, does not lead to a decrease in cycle time. This gives an optimal operating point, beyond which the cycle time increases again (Refer to experiment 3 – Vary W/L of sense amplifier by keeping PC width constant, for this result). This can be explained as follows. When the N Channel and P Channel are

the N Channel and P Channel are made wider, they require more current, which would be supplied when the PC was made wider.

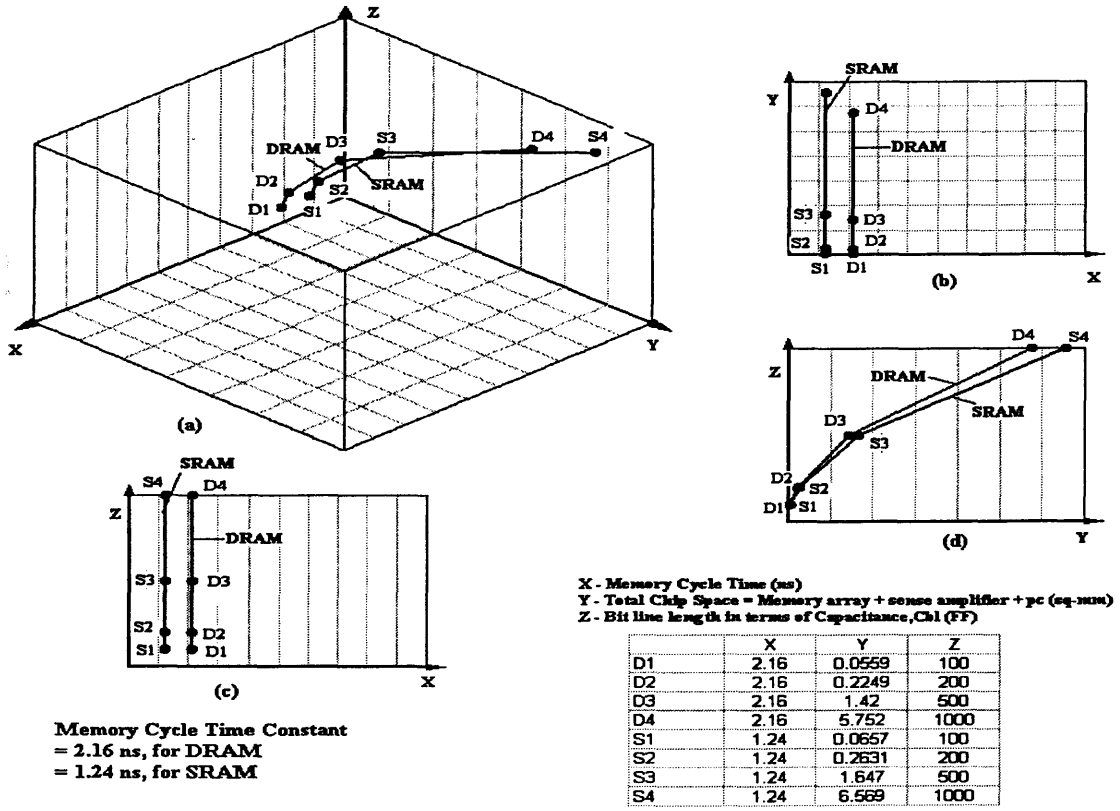
3.4.2.3 Memory Cycle Time Constant. The experimental results obtained when the Memory Cycle Time was kept constant, at 2.16ns for DRAM and 1.24ns for SRAM, are shown in Tables 3.23 and 3.24 for DRAM and SRAM respectively. For DRAM, the time to merge the bit lines to the same voltage level was kept constant at 0.42ns, and the memory cell recovery time was kept constant at 1.74ns by adjusting the pre charge switch and sense amplifier dimensions. In case of SRAM, the time to merge bit lines to the same voltage level and the worst case recovery time was adjusted to keep the memory cycle time constant.

Table 3.23 Operating Points Showing Performance Parameters and Variable Values for Line Graph for DRAM Keeping Memory Cycle Time Constant at 2.16ns.

Point	Sense amp Wn (um)	Sense amp Wp (um)	PC width (um)	Sense Amp + PC Area (sq-um)	Memory Size (ff)	#cells	Total sense amp + pc area(sq-um) (a)	Total memory array area (0.2592 * # cells) (sq-um) (b)	total chip area (sq-mm) (a) + (b)
Point D1	0.952/0.18	2/0.18	1.62/0.18	1.35	100	462*462	623.7	55324.68	0.0559
Point D2	2.856/0.18	6/0.18	4.5/0.18	4	200	924*924	3696	221298.4	0.2249
Point D3	11.9/0.18	25/0.18	15/0.18	15.98	500	2310*2310	36913.8	1383117.1	1.42
Point D4	35.7/0.18	75/0.18	42/0.18	47.41	1000	4620*4620	219034.2	5532468.5	5.7515

Table 3.24 Operating Points Showing Performance Parameters and Variable Values for Line Graph for SRAM Keeping Memory Cycle Time Constant at 1.24ns.

Point	Sense amp Wn (um)	Sense amp Wp (um)	PC width (um)	Sense Amp + PC Area (sq-um)	Memory Size (ff)	#cells	Total sense amp + pc area(sq-um) (a)	Total memory array area (4.129 * # cells) (sq-um) (b)	total chip area (sq-mm) (a) + (b)
Point S1	0.6/0.18	2.5/0.18	1.6	1.4	100	126*126	176.4	65552.004	0.0657
Point S2	1.68/0.18	7/0.18	4.5/0.18	3.93	200	252*252	990.36	262208.016	0.2631
Point S3	6/0.18	25/0.18	14/0.18	13.68	500	630*630	8618.4	1638800.1	1.6474
Point S4	14.4/0.18	60/0.18	32/0.18	32.54	1000	1260*1260	41000.4	6555200.4	6.5692



	X	Y	Z
D1	2.16	0.0559	100
D2	2.16	0.2249	200
D3	2.16	1.42	500
D4	2.16	5.752	1000
S1	1.24	0.0657	100
S2	1.24	0.2631	200
S3	1.24	1.647	500
S4	1.24	6.569	1000

Figure 3.50 (a) Three Dimensional Line Plot Showing Tradeoffs between Memory Cycle Time(ns), Total Chip Space(mm^2) and Bit Line Capacitance(ff), for DRAM and SRAM. Memory Cycle Time was Constant at 2.16ns for DRAM and 1.24ns for SRAM. (b) Tradeoff Between Total Chip Space(mm^2) and Memory Cycle Time(ns). (c) Tradeoff Between Bit Line Capacitance(ff) and Memory Cycle Time(ns). (d) Tradeoff Between Bit Line Capacitance(ff) and Total Chip Space(mm^2).

To study the tradeoff between performance parameters when memory cycle time is kept constant, the memory size (in terms of Cbl) is increased. As the bit line capacitance is increased, it leads to an increase in total memory array size and its area. To keep the cycle time constant, the sense amplifier has to be made wider. This increases the sense amplifier and pre charge switch area. Thus, the chip space increases with an increase in the memory size. This result is observed in Figure 3.48(d). It is seen that the total chip space consumed by DRAM is lesser than SRAM. This difference becomes significant at high values of Cbl. At low values of Cbl, SRAM occupies almost the same space as DRAM.

CHAPTER 4

DISCUSSION

When the memory size increases, the length of the bit line is increased, leading to a higher value of bit line capacitance. This is shown in Figure 4.1 below.

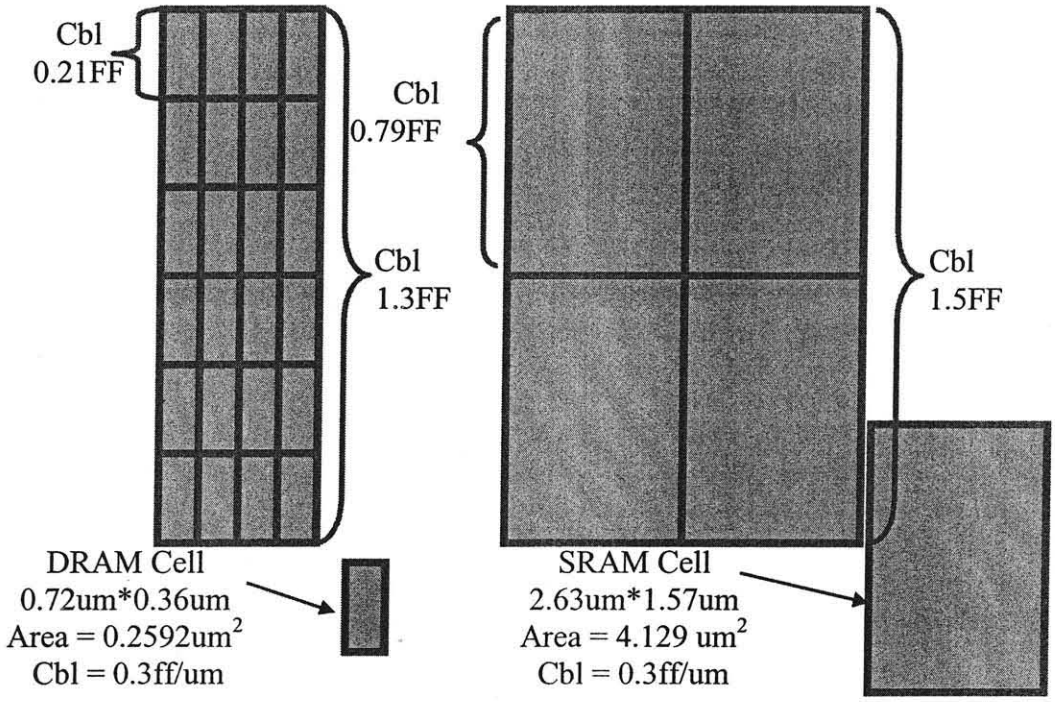


Figure 4.1 Relation Between Memory Size and Bit Line Capacitance.

For each sense amplifier area value, there exists an optimum precharge switch width, at which minimum memory cycle time is obtained. Minimum memory cycle time of 2.11ns for DRAM and 1.18ns for SRAM, is obtained for a sense amplifier area of $1\mu m^2$. When the sense amplifier area is increased (by increasing the W/L ratio of the transistors in the sense amplifier and keeping the k_r ratio and the precharge switch width constant), the memory cycle time also continues to increase. This is due to the added parasitic capacitance of the sense amplifier transistors as shown in the Figure 4.2 below.

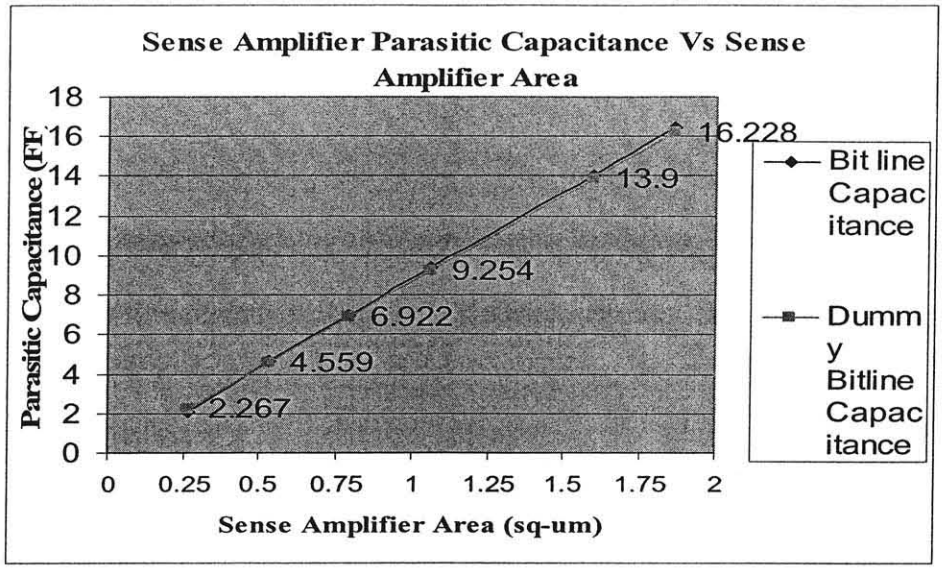


Figure 4.2 Parasitic Capacitance of the Sense Amplifier Transistors Versus Sense Amplifier Area.

To reduce the memory cycle time, more current is required to overcome this added parasitic capacitance and to merge the bit lines to the same voltage level. This current can be obtained by widening the switch.

In case of DRAM, the read time for the memory cell can be reduced slightly by increasing the word line switch width. The read and restore time for the SRAM is dominated by the regenerative flip-flop action of its memory cell, causing it to recover quickly. However, for high Cbl values (1000femto-farads), a tail effect is observed on the SRAM memory cell, due to the loading of the large Cbl value on the small parasitic capacitance (octo-farads) of the memory cell. The recovery time for the SRAM memory cell increases drastically. To solve this problem, it is necessary to turn off the word line pulse once the differential voltage on the sense amplifier output reaches a typical value between 10% to 20% of the supply voltage. The value would depend on factors associated with the memory output circuitry driven by the sense amplifier.

The ratio of the change in the sense amplifier area to the change in memory cycle time for DRAM is a factor betwen1.25 to 3 times greater than that of SRAM. For a sense amplifier and precharge area increase by the same amount, the cycle time reduction obtained for SRAM, is between 1.25 to 3 times the cycle time reduction obtained for DRAM. Also, to obtain a cycle time reduction by the same amount, the increase in the sense amplifier and precharge area for DRAM, has to be between 1.25 to 3 times the increase in sense amplifier and precharge area for SRAM. If the Cbl value is increased by a factor of N as a result of increasing memory size, the total chip area has to be increased by a factor of N^2, to keep the memory cycle time constant,. This holds true, for both DRAM and SRAM. The predicted increase in sense amplifier and precharge area is $5.075N^2 - 17.711N + 21.1704$ (for DRAM) and $2.7874N^2 - 3.6992N + 1.8628$ (for SRAM). Figure 4.3 shows the predicted increase in sense amplifier and precharge area, when the Cbl is increased by a factor of one to 50.

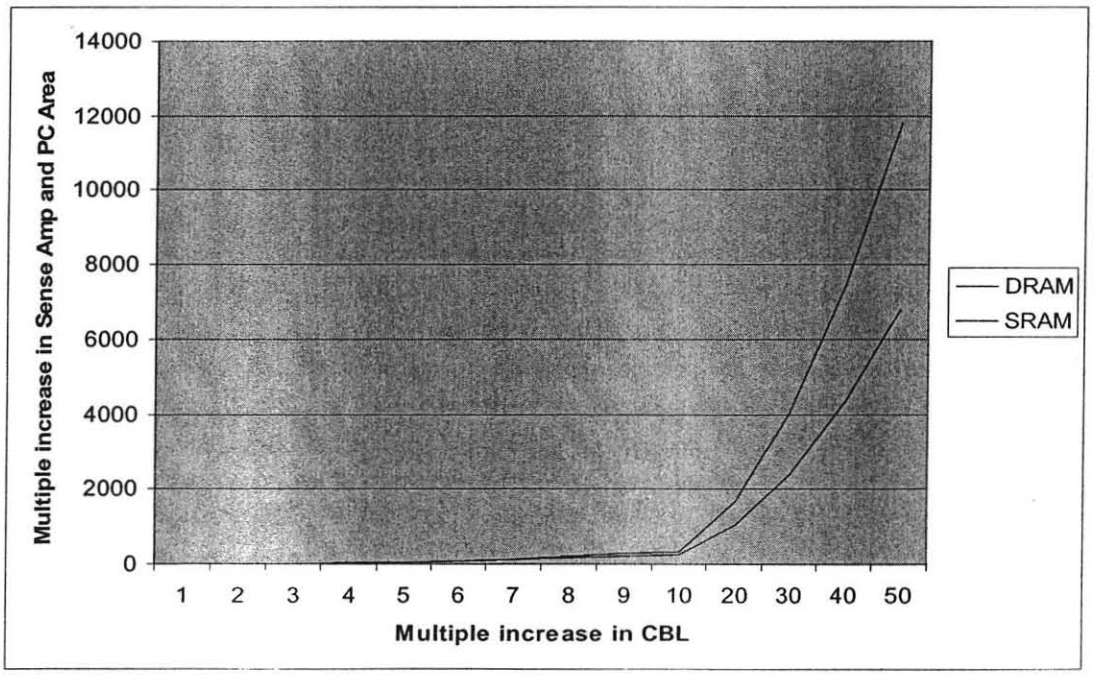


Figure 4.3 Predicted Increase in Sense Amplifier and Precharge Area, as a Funtion of Increase in Cbl.

A reduction in memory cycle time can be obtained by lowering the threshold voltage of the word line switch. This leads to an increased leakage current. The tradeoff between the threshold voltage, memory cycle time and leakage current is shown in Figure 4.4 below. Leakage current can be reduced slightly by precharging both the bit lines to 3V instead of mid way between 0V and the supply voltage.

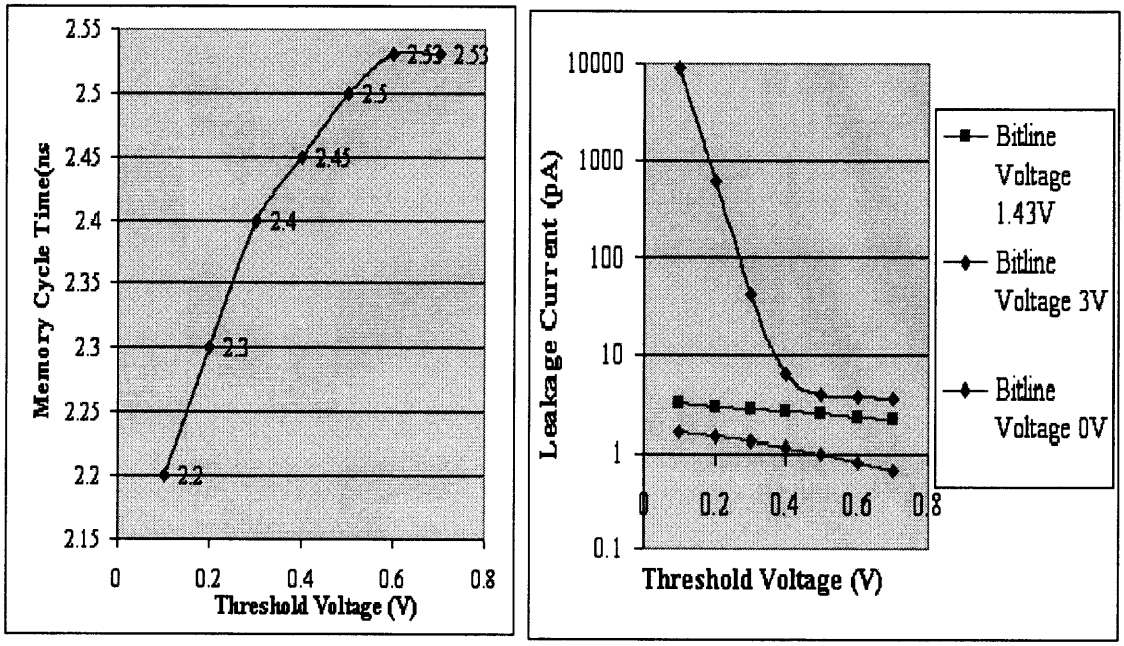


Figure 4.4 Tradeoff Between Threshold Voltage of the Word Line Switch, Memory Cycle Time and Leakage Current for DRAM.

The Figure of Merit (FM) is defined in equation 4.1 below.

$$FM = Cbl(ff) / [Cycle\ Time(ns) \times Chip\ Area(sq\text{-}mm)] \quad (4.1)$$

The FM is plotted as a function of individual sense amplifier and precharge area in Figure 4.5 below.

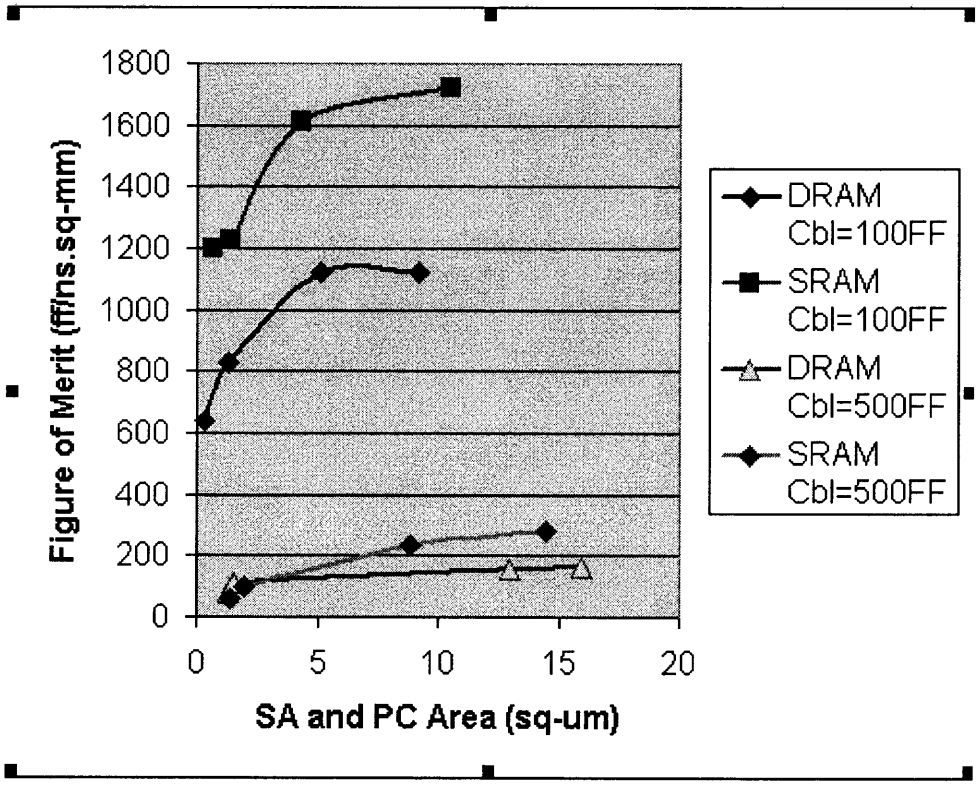


Figure 4.5 Figure of Merit as a Function of Sense Amplifier and Precharge Area.

The Figure of Merit for SRAM is higher than that for DRAM, for the same sense amplifier and precharge area value. Hence, SRAM has superior performance over DRAM. The performance of both the memories drops drastically, as Cbl is increased from 100FF to 500FF. This happens because the huge Cbl value prevents the quick restore action of the sense amplifier. In such cases, a multiplexer can be used, to isolate the bit line capacitance from the sense amplifier.

CHAPTER 5

CONCLUSIONS

5.1 Conclusions

Various design issues relating to design of DRAM and SRAM memories were studied and the tradeoffs amongst the design variables and the performance goals were understood. The DRAM and SRAM memory design was optimized, for a standard 0.18*um* logic process. For a sense amplifier area of $1\mu m^2$, and a Cbl value of 100FF, the memory cycle times obtained for DRAM and SRAM, were 2.11ns and 1.18ns, respectively. This reinforced the theory that SRAM is faster than DRAM, due to its regenerative flip-flop action. A bit line capacitance (Cbl) value of 100FF corresponds to a DRAM memory size of 213.44K-bits and occupies a chip area of $0.055mm^2$. For the SRAM, a Cbl value of 100FF, corresponds to 15.8K-bits and occupies a chip area of $0.065mm^2$. Thus, DRAM has a higher packing density than SRAM. To maintain the same memory cycle time, when Cbl is increased by a factor of N, total chip area has to be increased by a factor of N^2. The ratio of the change in the sense amplifier area to the change in memory cycle time for DRAM is 1.25 – 3 times greater than that of SRAM. This indicates that the SRAM Cell is more sensitive than the DRAM Cell. It was concluded that, at high values of Cbl, turning off the word line pulse results in a reduction in cycle time, for SRAM. While studying the effect of increasing the area of the sense amplifier on the cycle time, it was found that, the minimum width of the pre charge switch is limited by the parasitic capacitance of the sense amplifier. The tradeoffs between the memory cycle time and the leakage current, as a function of word line switch

threshold voltage, were studied. The results suggest pre charging the bit lines to the power supply voltage, instead of the conventional Vdd/2 pre charging, to reduce the leakage current.

5.2 Suggestions for Future Work

This thesis focused on minimizing the speed of the DRAM and SRAM. A simple flip-flop sense amplifier was used to minimize the cycle time. To minimize the power consumed by the circuit, a clocked sense amplifier could be used. This would possibly affect the cycle time. This complex circuit could be studied and optimized. The tradeoff between cycle time and power dissipation could be studied.

To add more value to this thesis, other design issues such as time delays involved in the decoders and word line, area consumed on the chip by peripheral circuits as the decoders and output circuits, can be considered. It would be of special interest to study the threshold voltage mismatch issues amongst the sense amplifier transistors, the word line switches, and the SRAM memory cell transistors. Various sense amplifier circuit configurations could be studied and the advantages/disadvantages of using a current sense amplifier versus a voltage sense amplifier could be discussed. A study of output circuits, driven by differential sense amplifier output, would help to better optimize the design of the sense amplifier and the memory system, in general.

REFERENCES

1. Robert H Dennard, Croton-on-Hudson, N.Y, "Field-Effect Transistor Memory," United States Patent 3,387,286, June 4, 1968.

2. R Rainer Kraus, "Analysis and Reduction of Sense-Amplifier Offset," IEEE Journal of Solid State Circuits, Vol. 24, No. 4, 1028-1033, August 1989.

3. Karl U. Stein, Aarne Sihling, and Elko Doering, "Storage Array and Sense/Refresh Circuit for Single-Transistor Memory Cells," IEEE Journal of Solid State Circuits, Vol. SC-7, No. 5, 336-340, October 1972.

4. William K Hoffman and Howard L. Kalter, "An 8K b Random-Access Memory Chip Using the One-Device FET Cell," IEEE Journal of Solid State Circuits, Vol. SC-8, No. 5, 298-305, October 1973.

5. Robert H Dennard, Croton-on-Hudson; Dominic P. Spampinato, Ozone Park, both of N.Y., "Differential Charge Transfer Sense Amplifier," United States Patent 3,949,381 Dennard et al., April 6,1976.

6. Niantsu N. Wang, "On the Design of MOS Dynamic Sense Amplifiers," IEEE Transactions on Circuits and Systems, Vol CAS-29, No. 7, 467-477, July 1982.

7. Keith Boland, AT&T Global Information Solutions and Apostolos Dollas, Technical \\\\University of Crete, "Predicting and Precluding Problems with Memory Latency," IEEE Micro, 59-66, August 1994.

8. David Burnett, Kent Erington, Chitra Subramanian, and Kelly Baker, "Implications of Fundamental Threshold Voltage Variations for High-Density SRAM and Logic Circuits," Symposium on VLSI Technology Digest of Technical Papers, 15-16, 1994.

9. M Yasunao Katayama, "Trends in Semiconductor Memories," IEEE Micro, 10-17, November/December 1997.

10. Philip W. Diodato, Lucent Technologies, Bell Laboratories, "Embedded DRAM: More than Just a Memory," IEEE Communication Magazine, 118-126, July 2000.

11. "Process Integration, Devices, and Structures and Emerging Research Devices," International Technology Roadmap for Semiconductors, 2001 Edition.

12. R J.A.Mandelman, R.H.Dennard, G.B.Bronner,J.K. DeBrosse,R. Divakaruni, Y. Li, and C.J. Radens, "Challenges and future directions for the scaling of dynamic random-access memory(DRAM)," IBM Journal of Research and Development, October 2001.

13. Duane G. Laurent, Senior Member, IEEE, "Sense Amplifier Signal Margins and Process Sensitivities," IEEE Transactions on Circuits and Systems-I:Fundamental Theory and Applications, Vol. 49, No. 3, 269-275, March 2002.

14. J.E. Barth,Jr., J.H. Dreibelbis, E.A. Nelson, D.L. Anand, G. Pomichter, P. Jakobsen, M.R. Nelms, J. Leach, and G.M. Belansek, "Embedded DRAM design and architecture for the IBM 0.11-um ASIC offering," IBM Journal of Research and Development Vol. 46, No. 6, 675-689, November 2002.

15. Y. Nakagome, M. Horiguchi, T. Kawahara, and K. Itoh, "Review and future prospects of low-voltage RAM circuits," IBM Journal of Research and Development Vol. 47, No. 5/6, 525-552, September/November 2003.

16. Uk-Rae Cho, Tae-Hyoung Kim, Yong-Jin Yoon, Jong-Cheol Lee, Dae-Gi Bae, Nam-Seog Kim, Kang-Young Kim, Young-Jae Son, Jeong-Suk Yang, Kwon-Il Sohn, Sung-Tae Kim, In-Yeol Lee, Kwang-Jin Lee, Tae-Gyoung Kang, Su-Chul Kim, Kee-Sik Ahn, and Hyun-Geun Byun, "A 1.2-V 1.5-Gb/s 72-Mb DDR3 SRAM," IEEE Journal of Solid State Circuits, Vol. 38, No. 11, 1943-1951, November 2003.

17. Yasuhiko Taito, Tetsushi Tanizaki, Mitsuya Kinoshita, Futoshi Igaue, Takeshi Fujino, and Kazutami Arimoto, "An Embedded DRAM with a 143-MHz SRAM Interface Using a Sense-Synchronized Read/Write," IEEE Journal of Solid State Circuits, Vol. 38, No. 11, 1967-1973, November 2003.

18. Harold Pilo, Darren Anand, John Barth, Steve Burns, Phil Corson, Jim Covino, and Steve Lamphier, "A 5.6-ns Random Cycle 144-Mb DRAM With 1.4 Gb/s/pin and DDR3 RAM Interface," IEEE Journal of Solid State Circuits, Vol. 38, No. 11, 1974-1980, November 2003.

19. Betty Prince, Semiconductor Memories : A handbook of Design, Manufacture and Application, Second Edition, New York: John Wiley & Sons, 1991.

20. Jaeger, C. Richard, Microelectronic Circuit Design, Massachusetts: Irwin McGraw-Hill Press, 1997.