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Reliability Studies of TiN/Hf-Silicate Based Gate Stacks

Naser Ahmed Chowdhury
New Jersey Institute of Technology

ABSTRACT

RELIABILITY STUDIES OF TiN/Hf-SILICATE BASED GATE STACKS

by
Naser Ahmed Chowdhury

Hafnium-silicate based oxides are among the leading candidates to be included into the first generation of high-κ gate stacks in nano-scale CMOS technology because of their distinct advantages as far as thermal stability, leakage characteristics, threshold stability and low mobility degradation are concerned. Their reliability, which is limited by trapping at pre-existing and stress induced defects, remains to be a major concern.

Energy levels of electrically active ionic defects within the thick high-κ have been experimentally observed in the context of MOS band diagram for the first time in Hf-silicate gate stacks from low temperature and leakage measurements. Excellent match between experimental and calculated defect levels shows that bulk O vacancies are probably responsible for electron trapping at both shallow and deep levels. Their role in trapping and transport under different gate polarity and band bending conditions has been determined. For gate injection, electron transport through mid-gap states dominates, which leads to slow transient trapping at deep levels. Under substrate injection field and temperature dependent transport through conduction-edge shallow levels or trap-assisted tunneling due to *negative-U* transition occurs depending on bias condition. The former gives rise to fast transient trapping, whereas the latter is responsible for slow transient trapping.

Mixed degradation, due to trapping of both electrons and holes in the trap levels within the bulk high-κ, was observed under constant voltage stress (CVS) applied on n-channel MOS capacitors with negative bias condition. Mixed degradation resulted in turn-around effect in flat-band voltage shift (ΔV_{FB}) with respect to stress time. Under CVS with positive bias, applied on nMOSFETs, lateral distribution of trapped charges in the deep levels causes turn-around effect in threshold voltage shift (ΔV_T) with respect to stress levels.

For the incident carrier energies above the calculated O vacancy formation threshold and thick high-κ layer, both flatband voltage shift, due to electron trapping at the deep levels, and increase in leakage current during stress follow t^n (n $\approx$ 0. 4) power-law dependence under substrate hot electron injection. *Negative-U* transitions to deep levels are shown to be responsible for the strong correlation between slow transient trapping and trap assisted tunneling.

As far as negative bias temperature instability, NBTI effects on pMOSFETs is concerned, ΔV_T is due to the mixed degradation within the bulk high-κ for low bias conditions. For moderately high bias, ΔV_T shows an excellent match with that of SiO_2 based devices, which is explained by reaction-diffusion (R-D) model of NBTI. Under high bias condition at elevated temperatures, due to high Si-H bond-annealing/bond-breaking ratio, the experimentally observed absence of the impact ionization induced hot holes at the interfacial layer (IL)/Si interface probably limits the interface state generation and ΔV_T as they quickly reach saturation.

Time-zero dielectric breakdown (TZBD) characteristics of TiN/HfO_2 based gate stacks show that thickness and growth conditions significantly affect the BD field of IL. For the thin high-κ layers, BD of IL triggers BD of the gate stack. Otherwise, BD of high-κ layer initiates it. During time dependent dielectric breakdown, TDDB, four regimes of degradation are observed under CVS with high gate bias conditions: (i) charge trapping/defect generation, (ii) soft breakdown (SBD), (iii) progressive breakdown and (iv) hard breakdown (HBD). Activation energy of bond-breakage, found from Arrhenius plots of 63% failure value of T_{BD}, shows that IL degradation triggers gate stacks BD, and the wear-out during TDDB.

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Naser Ahmed Chowdhury

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APPROVAL PAGE

RELIABILITY STUDIES OF TiN/Hf-SILICATE BASED GATE STACKS

Naser Ahmed Chowdhury

11/11/06

Dr. Durgamadhab Misra, Dissertation Advisor — Date
Professor of Electrical and Computer Engineering, NJIT

Nov. 11, 2006

Dr. Arvind Kumar, Committee Member — Date
Member of Technical Staff, IBM T J Watson Research Center,
Yorktown Heights, NY

Nov. 11, 2006

Dr. Leonid Tsybeskov, Committee Member — Date
Associate Professor of Electrical and Computer Engineering, NJIT

Nov 11, 2006

Dr. Marek Sosnowski, Committee Member — Date
Professor of Electrical and Computer Engineering, NJIT

11-11-2006

Dr. Anthony Fiory, Committee Member — Date
Research Professor of Physics, NJIT

11 | 11 | 2006

Dr. N.M. Ravindra, Committee Member — Date
Professor of Physics, NJIT

BIOGRAPHICAL SKETCH

Author: Naser Ahmed Chowdhury

Degree: Doctor of Philosophy

Date: May 2007

Undergraduate and Graduate Education:

- Doctor of Philosophy in Electrical Engineering,
  New Jersey Institute of Technology, Newark, NJ, 2007

- Master of Science in Electrical Engineering,
  University of Texas at Arlington, Arlington, TX, 2001

- Bachelor of Science in Electrical and Electronic Engineering,
  Middle East Technical University, Ankara, Turkey, 1995

Major: Electrical Engineering

Presentations and Publications:

N. A. Chowdhury, P. Srinivasan and D. Misra,
"Trapping in Deep Defects under Substrate Hot Electron Stress in TiN/Hf-Silicate Based Gate Stacks".
Solid State Electronics,
(Accepted for publication).

N. A. Chowdhury and D. Misra,
"Charge Trapping at Deep States in Hf-Silicate based High-κ Gate Dielectrics".
Journal of Electrochemical Society,
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N. A. Chowdhury, D. Misra and N. Rahim,
"Negative Bias Temperature Instability in TiN/Hf-Silicate Based Gate Stacks".
International Journal of High Speed Electronics and Systems,
(Accepted for publication).

D. Misra, R. Garg, P. Srinivasan, N. Rahim and N.A. Chowdhury,
"Interface Characterization of High-k Dielectrics on Ge Substrates",
Materials Science in Semiconductor Processing,
(Accepted for publication).

N. A. Chowdhury, G. Bersuker, C. Young, R. Choi, S. Krishnan and D. Misra,
"Breakdown Characteristics of nFETs in Inversion with Metal/HfO_2 Gate Stacks",
Microelectronic Engineering,
(Accepted for publication).

P. Srinivasan, N.A. Chowdhury and D. Misra,
"Charge trapping in Ultra-thin Hafnium silicate/Metal gate stacks",
Electron Device Letters,
Vol.26, No. 12, pp. 913-915, 2005.

N. A. Chowdhury, R. Garg and D. Misra,
"Charge Trapping and Interface Characteristics of Thermally Evaporated HfO_2",
Applied Physics Letters,
Vol. 85, No. 15, pp. 3289-3291, 2004.

R. Garg, N. A. Chowdhury, M. Bhaskaran, P. K. Swain and D. Misra,
"Electrical characteristics of thermally evaporated HfO_2",
Journal of Electrochemical Society,
Vol. 151., No.10, pp. F215-F219, 2004.

N. A. Chowdhury, G. Bersuker, C. Young, R. Choi, S. Krishnan, and D. Misra,
"Time Zero Dielectric Breakdown Characteristics of TiN/HfO_2 Based High-k Gate Stacks",
IEEE Transactions on Device and Materials Reliability,
(In preparation).

N. A. Chowdhury, G. Bersuker, R. Choi, H. Alshareef, N. Rahim and D. Misra,
"Low Temperature Mobility Characteristics of Hf-Silicate Based nMOSFETs with Optimized N-metal Gate"
Electrochemical and Solid-State Letters,
(In preparation).

N. A. Chowdhury, G. Bersuker, C. Young, R. Choi, N. Rahim and D. Misra,
"Temperature Dependent TDDB Characteristics of TiN/ HfO_2 Based Gate Stacks",
Electrochemical and Solid-State Letters,
(In preparation).

T. Kundu, R. Garg, N. A. Chowdhury and D. Misra,
"Electrical Techniques for the Characterization of Dielectric Films",
Electrochemical Society Interface,
Vol. 14, No. 3, pp.17-20, 2005.

N. A. Chowdhury and D. Misra,
"NBTI Effects in pMOSFETS with TiN/Hf-Silicate Based Gate Stacks",
ECS Trans. on Physics and Technology of High-k Gate Dielectrics IV,
Cancun, Mexico, pp. 215-224, October, 2006.

N. Rahim, N. A. Chowdhury and D. Misra,
"Role of Experimentally Observed Defect Energy Levels in Carrier Transport and Charge Trapping in Metal Gate/Hf-Silicate Based Gate Stacks",
The 210^{th} Electrochemical Society Meeting, Cancun, Mexico, October, 2006.

N. A. Chowdhury, G. Bersuker, C. Young, S. Krishnan, R. Choi and D. Misra,
"Breakdown characteristics of TiN/HfO_2 based high-κ gate stacks",
The 3^{rd} International Workshop on Advanced Gate Stacks Technology,
Austin, Texas, September, 2006.

D. Misra, N. A. Chowdhury and N. Rahim,
"Negative bias Temperature Instability in TiN/Hf-silicate Based Gate Stacks" ,
IEEE Lester Eastman Conference on High Performance Devices,
Cornell University, Itahaca, NY, August, 2006.

D. Misra and N. A. Chowdhury,
"Charge Trapping in High-k Gate Dielectrics: A Recent Understanding",
ECS transactions on Dielectrics for Nanosystems II: Materials Science, Processing, Reliability, and Manufacturing,
Denver, Colorado, pp. 311-321, May, 2006.

N. A. Chowdhury, P. Srinivasan and D. Misra,
"Trapping in Deep Defects under Substrate Hot Electron Stress in TiN/Hf-Silicate Based Gate Stacks" ,
Proceedings of International Semiconductor Device Research Symposium,
Bethesda, Maryland, pp. WP1-03 to 04, December, 2005.

N. A. Chowdhury, P. Srinivasan and D. Misra,
"Evidence of deep energy states from low temperature measurements and their role in charge trapping in metal gate/Hf-silicate gate stacks" ,
ECS transactions on Physics and Technology of High-k Gate Dielectrics III,
Los Angeles, California, pp. 767- 776, October, 2005.

N. A. Chowdhury, P. Srinivasan, D. Misra, R. Choi and B. H. Lee,
"Observation of deep bulk defects using low temperature techniques in $TiN/HfSi_xO_y$ gate stack and their role in BTI and HCS effects",
The 2nd International Symposium on Advanced Gate Stacks Technology,
Austin, Texas, September, 2005.

P. Srinivasan, N. A. Chowdhury, A. Peralta, D. Misra, R. Choi and B. H. Lee,
"Charge Trapping in Metal Gate/High- k n-MOSFETS during Substrate Injection",
Proceedings of International Symposium on Advanced Gate Stack, Source/Drain and Channel Engineering for Si-Based CMOS: New Materials, Processes and Equipment,
Quebec City, Canada, pp. 366- 373, May, 2005.

D. Misra, N. A. Chowdhury, R. Garg and P. Srinivasan,
"Integration of High-k Dielectrics into Sub-65nm CMOS Technology: Requirements and Challenges",
Proc. of the IEEE TENCON,
Chiang Mai, Thailand, pp. 1401-1405, November, 2004.

N. A. Chowdhury, P. Srinivasan, D. Misra, R. Choi and B. H. Lee,
"Charge Trapping Characteristics of $TiN/HfSi_xO_y/SiO_2/p$-Si MOS Devices under Stress",
Int. SEMATECH Workshop on Electrical Characterization and Reliability of High-k Devices,
Austin, Texas, Nov., 2004.

N. A. Chowdhury, R. Garg and D. Misra,
"Time Dependent Dielectric Breakdown of Thermally Evaporated HfO_2 for Nanoscale Devices",
Proc. of 1st Intl. Symp. on Dielectrics for Nanosystems: Mat. Science, Processing, reliability and Manufacturing,
Honolulu, Hawaii, pp. 381-390, October, 2004.

N. A. Chowdhury, R. Garg and D. Misra,
"Charge Trapping and Interface Characteristics of Thermally Evaporated HfO_2",
The 205th Electrochemical Society Meeting, San Antonio, TX, May, 2004.

R. Garg, N. A. Chowdhury, M. Bhaskaran, P. K. Swain and D. Misra,
"Electrical Characteristics of Thermally Evaporated HfO_2",
Proceedings of the Second International Symposium on High Dielectric Constant Materials,
Ontario, Florida, pp. 385-394, October, 2003.

Dedicated To My Father, Mother, Wife and Son

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CHAPTER 1

INTRODUCTION, MOTIVATION AND OBJECTIVES

1.1 Introduction

Unabated demands for higher density and faster operational speed of transistors, and lower power consumption in integrated circuits (IC) have pushed complementary metal oxide semiconductor (CMOS) technology into the forefront of the microelectronics industry. Transistor scaling has so far achieved a remarkable success in optimizing these diverse objectives. However, further downscaling of MOS field effect transistor (MOSFET) dimensions, specifically for oxide thickness (t_{ox}) below 1.6 nm, increases transistor leakage current to levels unacceptable for low power applications [1]. An attractive solution is to replace SiO_2 with high-κ dielectric materials (mostly Hf, Zr and Al-based) while retaining the standard MOSFET design [2], [3]. This has the prospect of resulting in higher effective thickness t_{ox} for equivalent oxide capacitance, which in turn reduces gate leakage but not drive current, i.e., maintains the edge in the electrical performance comparable to SiO_2.

Stringent application of the physical and electrical criteria like permittivity, band structure offset, thermodynamic stability, interface quality, gate electrode compatibility, process compatibility, reliability etc. show Hf-based oxides to be the most potential candidates out of many alternatives available in the silicon IC industry [4]-[7]. In particular, Hf-silicates and their nitrided alloys, are likely to be the first generation of materials that can be implemented as high-κ dielectrics [3]. They have

a moderately high dielectric constant (~8-15), depending on the Hf content, but, it is compensated by higher thermal stability, better leakage characteristics, improved threshold voltage stability and lower mobility degradation compared to HfO_2 [8]-[12]. In addition, silicates form better interfaces with Si than metal oxides. As far as circuit fabrication is concerned, CMOS process compatibility of Hf-silicates has been achieved. However, reliability remains to be the most critical factor to hold back its successful incorporation into the mainstream commercial intergraded circuits (IC) [12]-[15].

1.2 Motivation

For high-κ gate stacks, shown in Figure 1.1, trapping within the bulk dielectric is widely reported to be one of the most critical reliability issues [16]-[18]. Firstly, significant hystersis due to very fast charging and discharging of the trapped carriers causes transient threshold voltage instability, ΔV_T. This hampers high frequency

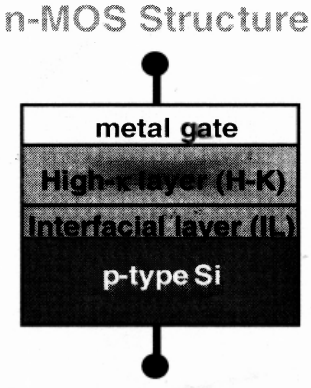


Figure 1.1 An n-channel MOS structure of high-κ gate stack showing bulk high-κ and interfacial layer.

switching operations. Secondly, ΔV_T due to comparatively stable trapping is a serious concern for the long-term operational performance of MOS devices. Thirdly, trapping has the most detrimental effect on the degradation of the channel carrier mobility in high-κ MOSFETS. Fourthly, bulk trapping distorts the internal electric field and modifies V_T/V_{FB} and leakage characteristics. Fifthly, defects responsible for trapping also assist in tunneling, which gives rise to high gate current and diminishes the advantages of high-κ oxides. Sixthly, charging of midgap trap levels, specifically near the metal gate electrode/high-κ interface, modifies the gate Fermi level. This gives rise to gate Fermi level pinning, which results in higher V_T. Therefore, it is obvious that studying and understanding the charge trapping induced degradation of high-κ gate stacks is key to improving its reliability as it is the ultimate limiting factor for its long term performance.

The other vital issues of reliability of high-κ gate stacks are related to stress-induced breakdown. Studies of breakdown characteristics of high-κ gate stacks are made complicated by the fact that potential drop/electric field across interfacial and high-κ layers are different due to the differences in the value of their dielectric constants, κ and thickness [19]. This, along with the differences in their respective atomic structures [20], leads to the difference in the degradation in interfacial layer (IL) and high-κ layer as the stress bias is applied. Breakdown field, E_{BD} decreases and the field acceleration factor, γ of dielectrics increases with the increase in κ because local field at the atomic level increases with κ [20]. This suggests the inherent difference between the breakdown characteristics of IL and high-κ layer of

MOS devices. IL determines the gate stacks breakdown under substrate injection for thick high–κ layers [21]. Hard breakdown (HBD) is observed for n-channel MOS (nMOS) devices under substrate injection [22]. For gate injection, progressive breakdown (PBD) of IL triggers the soft breakdown (SBD) at the high-κ layer, which leads to device failure [16]. It is, therefore, imperative to examine the roles of IL and high-κ layer in the breakdown characteristics of the overall gate stacks.

Charge trapping and breakdown characteristics can be investigated by conducting a number of electrical tests such as hot carrier stress (HCS), positive/negative bias temperature instability (PBTI/NBTI), time dependent dielectric breakdown (TDDB), charge-to- breakdown (Q_{BD}), stress induced leakage current (SILC) etc. as shown in Figure 1.2 [23]. The success of these studies depends on the formulation of effective physical models, which can comprehensibly describe the

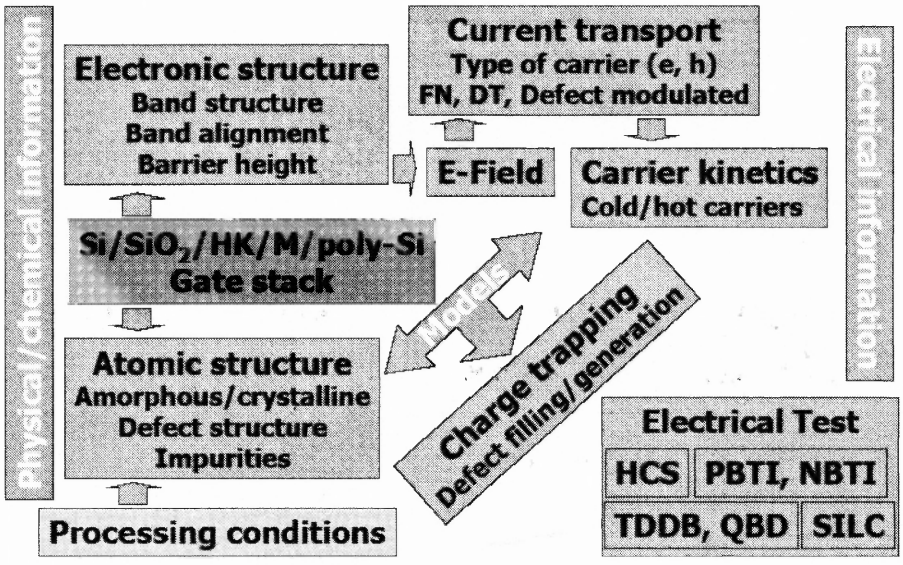


Figure 1.2 Different components of the charge trapping induced degradation studies of the high-κ gate stacks [21].

trapping and breakdown characteristics. As far as high-κ gate stacks are concerned, this can be achieved by understanding the atomic structure and electronic properties of the defects within the high-κ dielectrics, electronic structure of the gate stack, and carrier transport and kinetics under various oxide electric field conditions in conjunction with critical analysis of the results observed from the electrical experiments. However, processing conditions such as deposition techniques, precursors for deposition, anneal conditions etc. affect atomic/electronic structures of the gate stack as shown in the Figure. It is, therefore, imperative that high-κ reliability studies be carried out on case-by-case basis.

1.3 Objectives

The primary objective of this research is to propose a comprehensive reliability model, which will be able to provide a physical insight into charge trapping related phenomena under various stress conditions. To this end, the goals are to (1) experimentally observe pre-existing and stress induced defect energy levels using electrical characterization techniques, (2) find their relative locations in the context of MOS energy band structure, (3) establish their physical origins on the basis of calculation based models, (4) investigate the role of defect levels in carrier transport and charge trapping under different bias and temperature conditions, (5) study charge trapping induced degradation of critical device parameters like threshold/flatband voltage shift, sub threshold swing etc., under bias temperature stress, and (6) understand time zero and time dependent dielectric breakdown (TZBD and TDDB)

characteristics, specifically breakdown mechanisms, role of high-κ and interfacial layer in breakdown etc. The following Chapters describe the findings from the studies that were carried out in this dissertation to meet theses objectives.

1.4 Scope of Work

Hafnium-based high-κ devices, used for the reliability studies in this work, were fabricated using standard CMOS technology at SEMTECH, Austin, Texas. The sample sets comprised of both n- and p-channel MOS capacitors and transistors. Devices with TiN/Hf-Silicate and TiN/HfO_2 based gate stacks with different area ($1x10^{-8}$ to $1x10^{-3}$ cm^2), IL thickness (0.7 to 2.1 nm) and high-κ thickness (2 to 10 nm) conditions were investigated. Most of the reliability work like defect energy level and their role in trapping and transport, and NBTI/PBTI/SHE/SHH were performed using Hf-silicate based gate stacks at New Jersey Inst. of Technology by the author. Time zero and time dependent dielectric breakdown (TZBD/TDDB) studies were partially performed at SEMATECH by the author using HfO_2-based gate stacks.

1.5 Dissertation Organization

In this dissertation Chapter 2 contains a detailed literature review on the 'root cause' of trapping in high-κ oxides. Calculation based theoretical models focusing on physical origins, energy levels and formation energies of the most crucial electrically active ionic defects in Hf-based oxides are thoroughly scrutinized. The recent experimental models of fast and slow transient trapping are discussed in details.

Chapter 3 gives an overvihe ew on the fabrication of MOS devices with metal organic chemical vapor deposited (MOCVD) $TiN/HfSi_xO_y$, and atomic layer deposited (ALD) TiN/HfO_2 based gate stacks. Major electrical characterization techniques used in this research are also discussed. Details about the automation of the fundamental electrical measurements in LabView environment are provided.

Chapter 4 deals with the experimentally observed defect levels in the context of MOS energy band diagram. Low temperature measurements were employed to find deep defect levels. Leakage measurements at elevated temperatures not only gave information about defect levels but also clarified the conduction mechanisms under various polarity and band bending conditions. Characterization of time and temperature dependent de-trapping from stress-induced defects is shown to be an effective method to understand defect levels. Physical origins of the defects are evaluated on the basis of matching experimental and theoretical defect levels.

Chapter 5 presents trapping characteristics under different stress conditions such as constant voltage stress in both substrate and gate injection modes, substrate hot electron and hole stress. Physical models are developed on the basis of defect levels and transport mechanisms to explain the experimentally observed trapping characteristics.

Chapter 6 reports the effects of NBTI on p-channel MOSFETS with $TiN/HfSi_xO_y$ based high-κ gate stacks under different gate bias and elevated temperature conditions. For low bias conditions, ΔV_T is due to the mixed degradation within the bulk high-κ material. For moderately high bias conditions, H-species dissociation in the presence of holes and subsequent diffusion are initially responsible

for interface state and positively charged bulk trap generation. Initial time, temperature and oxide electric field dependence of ΔV_T in the devices, investigated in this study, shows an excellent match with that of SiO_2 based devices, which is explained by reaction-diffusion (R-D) model of NBTI. Under high bias condition at elevated temperatures, interface state generation and ΔV_T quickly reach saturation.

Chapter 7 deals with the breakdown mechanisms of metal gate/high-κ/IL based gate stacks. The role of IL and high-κ layer in TZBD and TDDB are determined from different splits of sample sets of TiN/HfO_2 based gate stacks with varying IL and high-κ layer thickness, IL growth conditions, and pre and post deposition anneal conditions (PreDA and PDA). For the thin high-κ layers (< 3.5 nm) under substrate injection, breakdown (BD) of IL triggers the BD of the gate stack under ramped voltage stress (RVS). Otherwise, BD of high-κ layer initiates it. Four consecutive regimes of degradation are observed under constant voltage stress (CVS) with high gate bias conditions during TDDB: (i) charge trapping/defect generation, (ii) soft breakdown (SBD), (iii) progressive breakdown and (iv) hard breakdown (HBD). Temperature dependent time-to-breakdown, T_{BD} studies show that the breakdown is field-driven under substrate injection and is initiated by IL.

Chapter 8 summarizes the major findings of this research work. Suggested future work is also described in Chapter 8.

CHAPTER 2

LITERATURE REVIEW: CHARGE TRAPPING IN HIGH-K DIELECTRICS

2.1 Introduction

Recently many theoretical and experimental studies are conducted on charge trapping in high-κ dielectric materials, specifically for the case of Hf-based oxides. Charge trapping in the pre-existing defects and trap generation within high-κ dielectric materials are the major concerns for the reliable operation of the MOS devices [24]. Conduction edge shallow electron traps are found to be inherent in the high-κ materials in the most recent studies and identified to be the "root cause" of trapping [25], [26]. Specifically under substrate injection, these traps have been found to be contributing to (i) electron transport through gate stack, (ii) localized electron trapping and the redistribution of the trapped charge, and its subsequent precipitation to deeper states located at different energy levels with different time constants during stress [27], [28] and (iii) electron de-trapping and redistribution during relaxation after removal of stress. Photo-generation of carriers [29] under low stress voltages was also used to induce electron trapping within the bulk [HfO_2, ZrO_2 and Al_2O_3] and hole trapping within the interfacial layer (IL). Trap generation may not be possible for low stress levels in bulk high-κ materials as effects of charge trapping, like threshold voltage (V_t) instability, are shown to be reversible by applying stress of opposite polarity [25]. However, M. Houssa [29], [30] reported neutral trap and positive charge generation at the bulk high-κ (ZrO_2) and at the IL (SiON),

respectively under high negative stress voltage (gate injection). Furthermore, stress induced leakage current (SILC) is observed under high stress conditions in HfO_2 films [31]. Negative bias temperature instability (NBTI) experiments further confirms that defect generation is possible in HfO_2 films for high stress levels at elevated temperature [32]. Consequently, depending on the stress conditions, both negative and positive charge trapping along with defect generation may occur at different energy levels and locations within the high-κ gate stack. Calculations typically focus on energy level, formation energy etc. of the defects once their origins (O vacancies/interstitials etc.) are determined [33]-[37]. Physical models of trapping and transport are formulated mostly on the basis of experimental results [26]-[31]. Only a few studies relate physical origins and corresponding electronic properties of defects to experimentally observed trapping and transport in a coherent manner [35], [37]-[39]. The following Sections describe the topics pertaining to the issues stated above.

2.2 Charge Trapping in Hf-based High-κ Oxides

Literature survey shows that charge trapping within the high-κ gate stacks is generally based on the role of the pre-existing defects in trapping mechanisms. Most of the physical models of trapping are based on experimental results obtained for Hf-based oxides since they are the most studied high-κ oxides.

Transient trapping in Hf-based gate dielectrics has been a point of critical investigation in the most current studies on high-κ reliability [36]-[43]. Depending on detrapping characteristics, it may be broadly categorized into two groups: fast and

slow. Fast transient trapping mostly occurs at the bulk defects with energy levels near high-κ band edges under resonant tunneling conditions at 'non-zero' gate bias [41]. This is why, its effect in degradation like threshold voltage shift, ΔV_T, is found to be quickly reversible under post-stress low 'non zero' gate bias condition [42]-[45]. On the other hand, slow transient trapping occurs at the defects with energy levels lying deep within the bulk high-κ bandgap, specifically within Si bandgap range in the context of MOS band diagram, and is shown to inhibit fast ΔV_T recovery even under high post-stress bias conditions [13]-[15], [18], [41]. Consequently, trapping at pre-existing or stress induced deep defects can be reasonably considered to be the ultimate limiting factor for the long-term reliability of the Hf-based high-κ MOS devices. Physical models are developed to individually account for the fast and slow transient trapping. The former leads to hysteresis and the latter to more stable trapping. They are described separately in Section 2.2.

2.2.1 Fast Transient Trapping

Charge trapping characterization is usually based on quasi-static or dc measurement techniques. However, such techniques are not adequate for fast transient trapping analysis since they have low ramp rate (10 V/s maximum) [42]. Fast measurement techniques, like multiple-pulsed technique has been proposed for better evaluation of the fast charging and discharging effects on V_{th} hysteresis for SiO_2/HfO_2 gate stacks. This technique is based on monitoring drain current transients of MOSFETS.

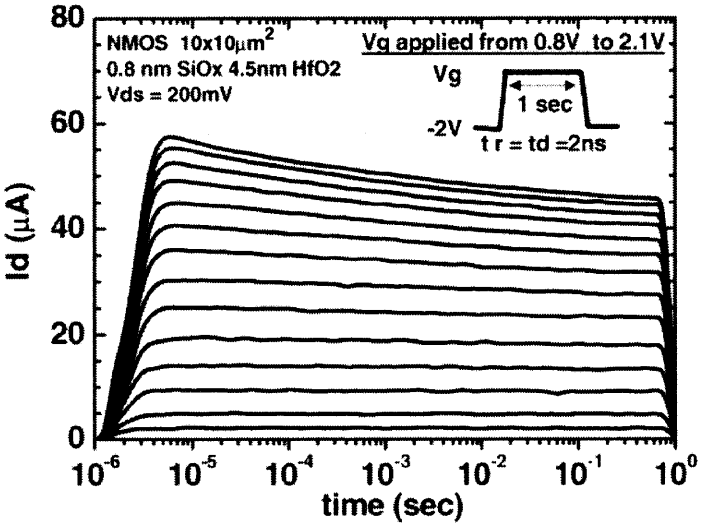


Figure 2.1 Transient behavior of drain current (I_d) under multiple-pulsed technique. Source: [42]

Typical $I_d(t)$ transients from μs up to seconds are depicted in Figure 2.1 using several gate voltage pulses with 2ns rise/fall time. Time-dependent reduction in $I_d(t)$ during the application of the pulse is mostly due to the fast transient trapping. Similarly, detrapping transients of $I_d(t)$ can be observed by changing the gate voltage pulse from high to low. By sampling these $I_d(t)$ and $V_g(t)$ curves at a specific time, an $I_d(V_g)$ parametric plot can be constructed as shown in Figure 2.2. For static and ramp measurements, hysteresis is obvious in the Figure. However, trapping and de-trapping occurs even during the application of ramp, so that, proper characterization of fast transient trapping is not possible. On the other hand, $I_d(V_g)$ plot acquired using transient techniques at the shortest possible time (5μs) is significantly devoid of trapping when applied pulse is moved up from –2 V to a particular value of V_g. The same is true as far as detrapping during pulling down of pulse height from V_g to –2 V

is concerned. As a result, the correct measure of hysteresis due to fast transient

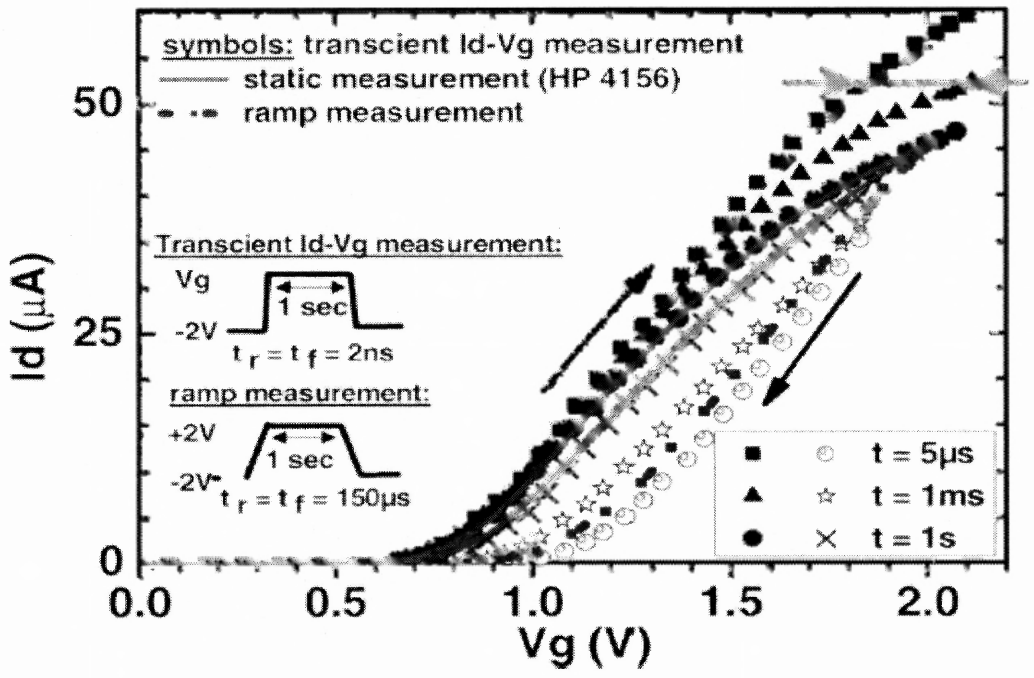
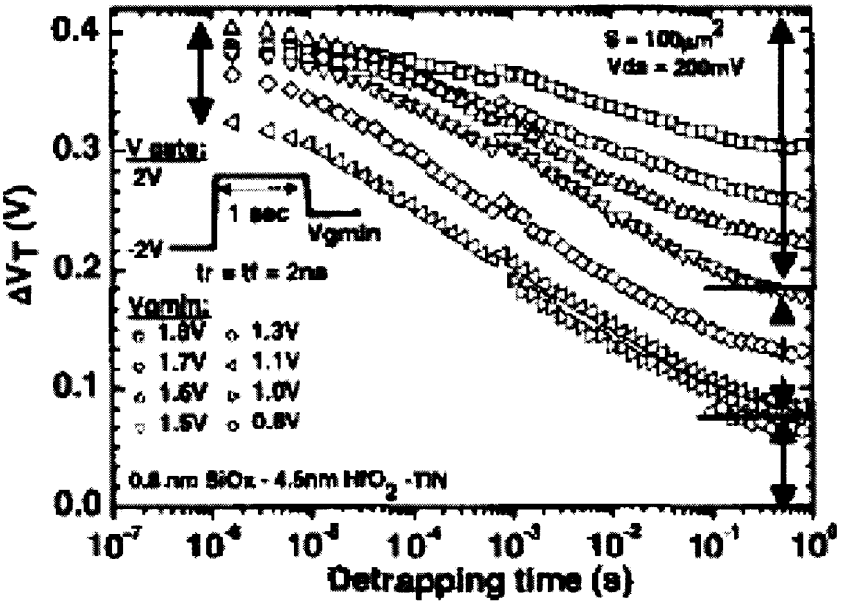
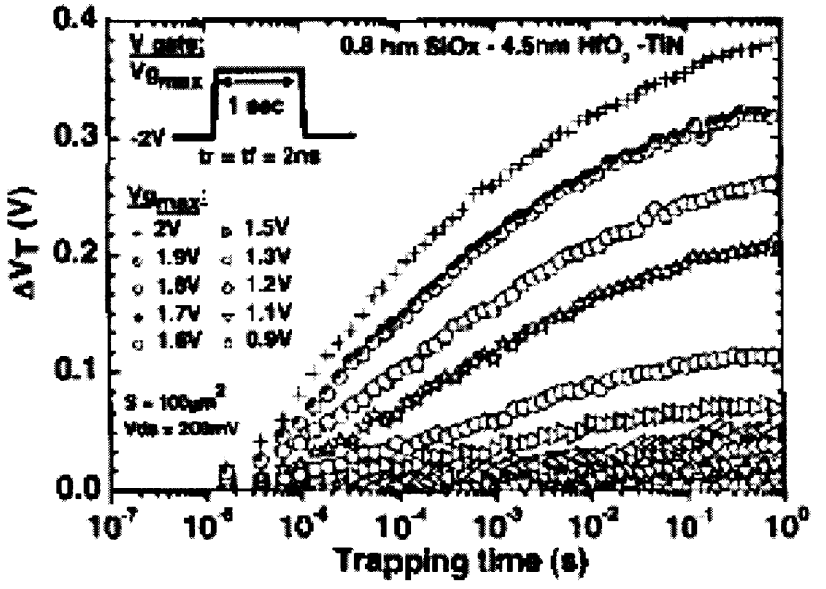


Figure 2.2 Hysteresis in I_d-V_g characteristics under transient, static and ramp measurement techniques.
Source: [39]

trapping can be observed. Moreover, this $I_d(V_g)$ plot for 5μs can be used as a reference to understand fast transient trapping induced ΔV_T for other drain current transients observed at different times as shown by the horizontal arrow in the Figure. ΔV_T, thus acquired, is plotted with respect to time for different gate biases during trapping and detrapping in Figures. 2.3 (a) and (b), respectively. It is obvious that trapping increases with gate bias and time. Fast detrapping even for moderate reductions in gate bias shows that trapping mostly occurred at the shallow levels.





(b) (a)

Figure 2.3 **(a)** Fast transient trapping induced positive ΔV_T shift for different gate bias conditions. **(b)** Detrapping from shallow electron trap level induced fast reduction in ΔV_T at different reduced post-stress gate bias conditions.
Source: [24]

To understand the influence of the high-κ gate stack architecture on hysteresis, dynamic ΔV_T due to the application of ramp is shown in Figure 2.4. It is obvious that trapping decreases as the physical thickness of the bulk high-κ decreases. However, as the interfacial layer (IL) decreases trapping increases. This shows that trapping mostly occurs at the bulk high-κ, and as IL decreases direct tunneling to the bulk oxide traps resonant with Si conduction band increases under positive gate bias condition.

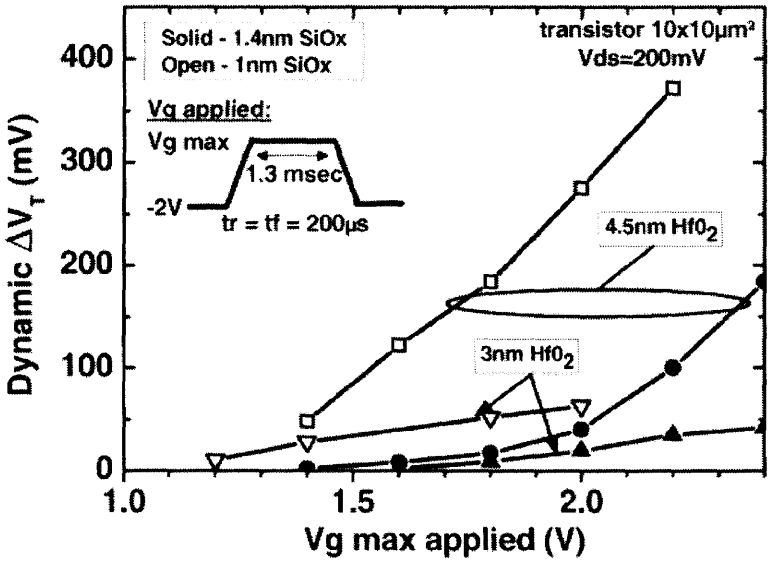


Figure 2.4 Ramp measurement technique induced ΔV_T with respect to different gate biases for different HfO_2/SiO_x-based gate stack architectures.
Source: [16]

The major models for the fast transient trapping, specifically to account for hysteresis, are shown in Figure 2.5. To account for the time dependence of ΔV_T, initially a simple model was proposed with defects physically located at HfO_2/IL

interface but having energy levels in between the conduction bands of HfO_2 and Si as

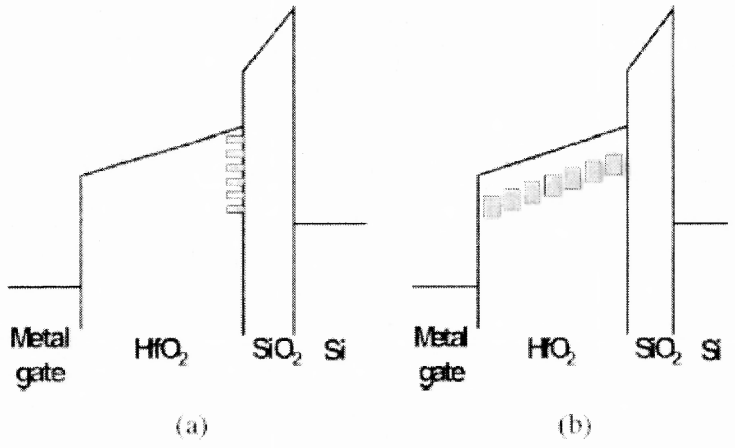


Figure 2.5 Physical models for fast transient trapping with defect levels located at **(a)** SiO_2/HfO_2 interface and **(b)** in the bulk high-κ oxide.
Source: [39]

shown in Figure 2.5(a). Although it explains direct tunneling of carriers of the defects, it fails to address the issue that trapping predominantly occurs at the bulk as observed in Figure 2.9. This leads to the model in Figure 2.5 (b), where it is shown that shallow defect levels lie within the bulk oxide and are physically distributed.

Depending on the thickness of IL trap filling mechanism in model in Figure 2.5 (b) changes. Under substrate injection condition, for thin IL (~1nm) channel-to-defect direct tunneling takes place, specifically for the traps near high-κ/IL interface. Subsequent filling of neighboring shallow traps under positive gate bias condition occurs due to trap-to-trap conduction. For thick IL (~2nm) trap filling by the capture of HfO_2 conduction band electron occurs during substrate injection. This is why, the model successfully depicts the experimental observation.

2.2.2 Slow Transient Trapping

Slow transient trapping is characterized by slow post-stress recovery of $\Delta V_{FB}/\Delta V_T$ under 'no bias' or 'low reverse bias' condition. Two different models based on mode of injection are described in Section 2.2.

2.2.2.1 Slow Transient Trapping under Substrate Injection. Stress/ relaxation cycles were applied on Hf-silicate based gate stacks as shown in Figure 2.6. It is obvious that electron trapping occurred during stress; however, only ~25% recovery of ΔV_T could be achieved during relaxation induced de-trapping at 'no bias'

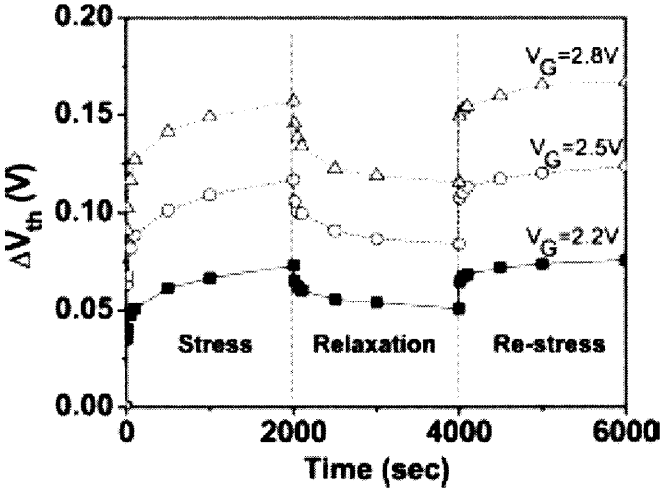


Figure 2.6 ΔV_T w.r.t. time under stress/relaxation cycle.
Source: [18]

condition. If trapping occurs at the shallow levels under substrate injection, de-trapping takes place even at the reduced positive bias condition as observed in Figure 2.3 (b). This is why, trapping at the deep levels also takes place.

During stress, electrons injected from the Si conduction band fills the shallow levels under the given band bending condition as shown in the physical model in Figure 2.7(a). Accumulation of the trapped charge in the localized states quickly modifies the internal electric field as shown in Figure 2.7 (b). This gives rise to the subsequent redistribution of the trapped charge to deep levels and the movement of the charge centroid toward the gate as illustrated in Figure 2.7 (c). The model is consistent the initial sharp rise in ΔV_T followed by its slow change as stress time is increased.

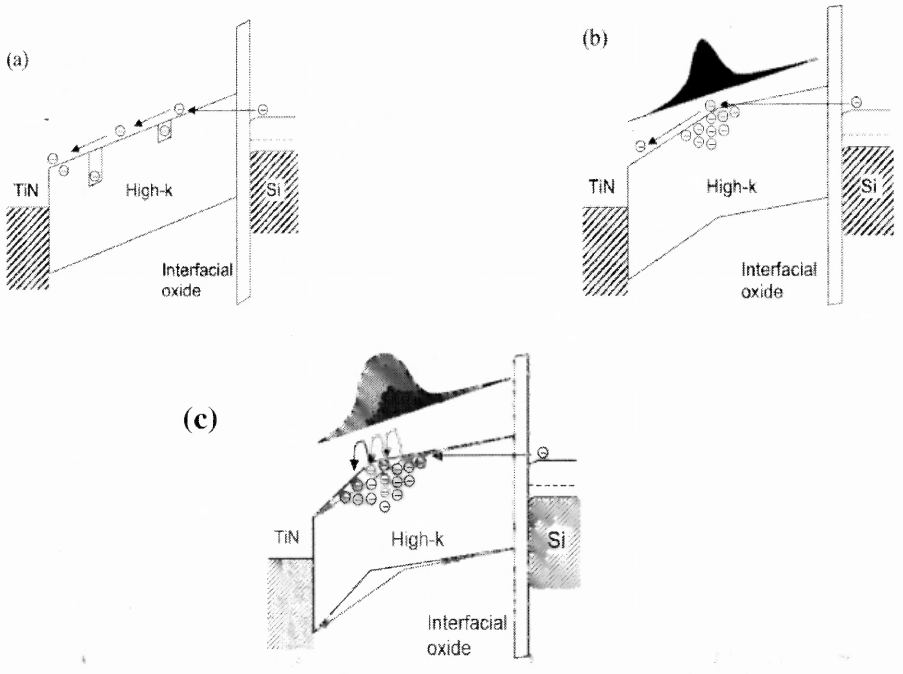


Figure 2.7 MOS band diagram during stress: **(a)** initial electron trapping at conduction edge shallow trap levels. **(b)** Internal electric field distortion due to accumulation of localized trapping. **(c)** Charge redistribution to deeper levels induce stable trapping.
Source: [25]

During relaxation at 'no bias' condition, internal field, built during stress, gives rise to the release and subsequent redistribution of the trapped charges as shown in Figure 2.8. Thus, the model explains relaxation induced slow de-trapping.

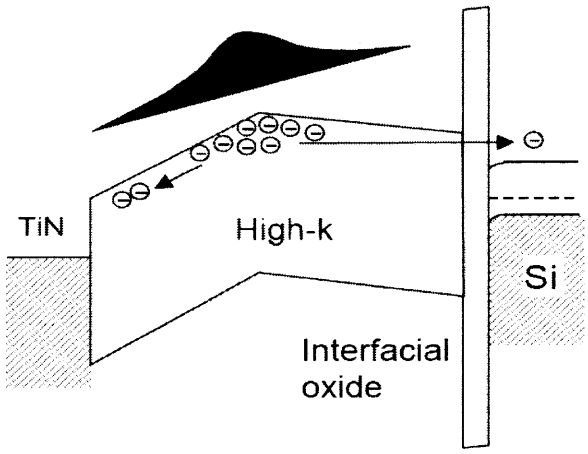


Figure 2.8 Relaxation induced slow release and redistribution of trapped charges. Source: [25]

2.2.2.2 Slow Transient Trapping under Gate Injection. In order to model ΔV_T instability under gate injection, negative gate bias was applied on a Hf-silicate based pMOS transistor, followed by different positive bias as shown in Figure 2.9. Positive charge trapping occurred during gate injection as $\Delta V_T < 0$. Application of high post-stress positive bias results in $\Delta V_T > 0$, i.e, electron trapping took place. Low positive bias apparently reduces post-stress ΔV_T, but full recovery is not achieved. This reduction may be due to electron trapping. These observation, as a result, point to the trapping at deep states.

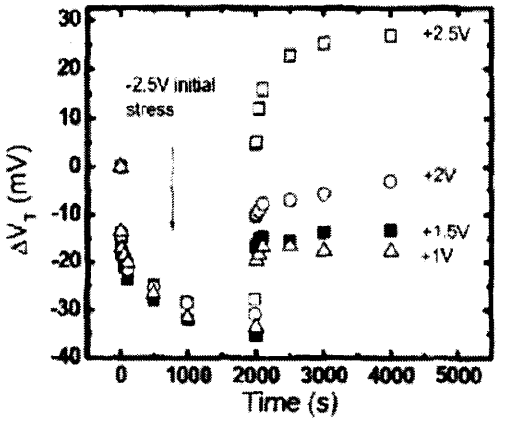


Figure 2.9 ΔV_T vs. time during stress with negative gate bias followed by positive bias.
Source: [45]

Suggested physical model that satisfies the above observations is depicted in Figure 2.10. In Hf-based oxides, shallow electron traps are filled due to direct tunneling during substrate injection, leading to $\Delta V_T > 0$. In addition, deep electron levels lying blow Fermi level also remained filled. When the opposite bias is applied, these shallow traps are easily discharged to high-κ conduction band making $\Delta V_T < 0$. However, de-trapping from these deep states occurs slowly. Because traps that are located within tunneling distance from the substrate with energy level in resonance with the holes in inversion layer may discharge. When the trap in close proximity to the substrate is emptied, electron migration from the neighboring deep trap "re-fills" it. Consequently, negative ΔV_T builds-up slowly over time.

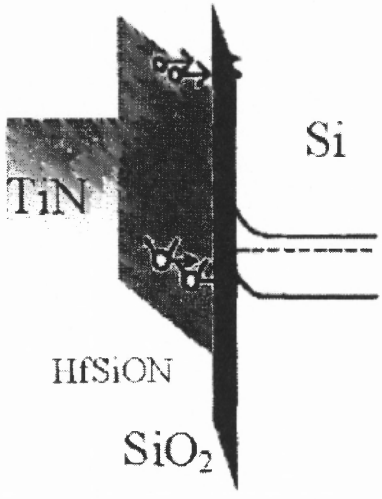


Figure 2.10 Physical model of deep defect induced slow transient trapping during gate injection.
Source: [45]

2.3 Defect Energy Levels and Trapping

The electrically active defect levels, responsible for electron/hole trapping, can be classified into three groups according to their locations within the bulk high-κ bandgap in the context of MOS band diagram, specifically with respect to Si band edges, as shown in Figure 2.11. Their effects on tapping/de-trapping are described below:

Group A: Defect levels lie above Si conduction edge, E_C^{Si} remain empty under 'zero bias', i.e., zero electric field and thermal equilibrium conditions. However, under 'non-zero' gate bias, i.e., substrate/gate injection conditions, such states are available

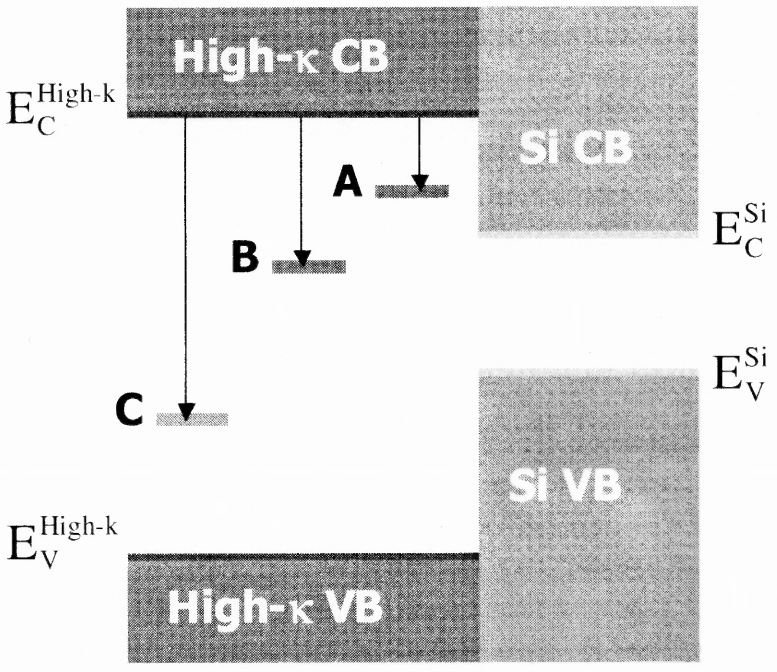


Figure 2.11 Defect levels within bulk high-κ in the context of MOS band diagram. Source: [41]

for resonant tunneling of electrons from E_C^{Si}/gate. Thus, they serve as electron traps. It may be noted here that trapping near the substrate is mostly responsible for flatband/threshold voltage shift ΔV_{FB} / ΔV_T. Once the bias is removed, very fast de-trapping to substrate/gate, in the order of μs for gate stacks with thin interfacial layers, occurs from these states. Consequently, these shallow levels give rise to fast transient trapping of electrons, which is mostly responsible for hysteresis and mobility degradation.

Group B: Defect levels lie within Si bandgap range. Electron/hole trapping in them can occur due to substrate/gate injection. Under 'zero bias' condition, carriers trapped in these deep states de-trap slowly to substrate depending on physical

distance from substrate and activation energy w.r.t. to E_C^{Si} ($E_a = E_T - E_C^{Si}$), which gives rise to slow transient trapping. ΔV_{FB} / ΔV_T due to trapping at these deep levels is the most critical reliability factor for the high-κ MOS devices as stated in the Chapter 1. Transient trapping will be described in more details in the following Chapters.

Group C: Electrons trapped at levels below E_V^{Si} give rise to fixed oxide charges. However, shallow hole trap levels, resonant with E_V^{Si}, are responsible for fast transient trapping under 'non-zero' bias conditions.

2.4 Physical Origins and Electronic Properties of Defects

Physical origins and electronic properties of defects, which mostly affect the performance and reliability of the high-κ gate stacks, are described in Section 2.4.

2.4.1 Why do High-κ oxides Have More Defects than SiO_2?

The reason for the presence of a large number of pre-existing intrinsic defects in the high-κ oxides compared to SiO_2 lies in the difference in their atomic properties [14], [28]. The high amount of heat required for the formation of SiO_2 makes the off-stoichiometry defects like O vacancies energetically costly. Moreover, SiO_2 has polar covalent bonds with a low coordination. This makes SiO_2 an excellent glass former, so that it remains amorphous. In addition, bonding in amorphous SiO_2 can relax locally to minimize defect concentration. The more prevalent bonds are the dangling bonds, specifically at Si/SiO_2 interface, and they can be removed due to rebonding.

Unlike SiO_2, high-κ oxides (e.g. HfO_2, ZrO_2 etc.) have higher atomic coordination numbers and greater ionic nature in their bonding due to large difference in electronegativity of the metal and O atoms [28]. This is why, high-κ oxides are poor glass formers, which is also evident from experimental observations as they cease to remain amorphous when subjected to high temperature processing. This is why, HO_2 is preferred to ZrO_2, silicates to pure oxides and N is added to inhibit crystallization.

2.4.2 Physical Origin of Defects in High-κ Oxides

In addition, ionic bonding and higher coordination mean that the atomic structure of high-κ materials does not easily relax to rearrange and rebond to remove the possible intrinsic defects [14]. Formation of metal (Hf, Zr etc)-site defects is comparatively costly in terms of formation energy due to the difference in valence between metal and O. For these reasons, O-site defects like O vacancies and interstitials are the defects of interest to the high-κ community.

2.4.3 Calculation of Electronic Properties of O Vacancies/Interstitials

As Hf-based high-κ oxides are the leading candidates and O vacancies/interstitials are the prime defects, Sub-section 2.4.3 dwells on reviewing the calculation-based studies focusing on them. Different positively/negatively charged states of O vacancies/interstitials, which induce energy levels of electron traps belonging to groups A and B in Figure 2.11 and hole traps to groups C and A, are particularly described in Section 2.4.

2.4.3.1 Calculation Methods. Formation and ionization energies, and electron/hole affinity of the charged defect states are calculated from the change in the total energies of the dielectric material system before and after the incorporation of the charged defects [10]. The monoclinic structure of hafnia is used as the building block of the system since it is the most stable phase, even for thin films. One such 12 atom monoclinic structure, comprised of fourfold-coordinated tetragonal and threefold-coordinated trigonal bonding of O ions in the monoclinic phase of hafnia, was used by Foster et al. [10] as shown in Figure 2.12. The monoclinic structure is extended in three dimensions to form supercells, which are used for calculations. O vacancy/interstitial formation energies, $E_{for}(D)$ is calculated as the energy difference between the fully relaxed neutral supercell with a single defect in charge state q (0, ±1, ±2 etc.), E_D^q, and the perfect neutral supercell E_0^0 as shown in Eq. 2.1 [33],

$$E_{for}(D) = E_D^q - (E_0^0 \pm E_O^q) \tag{2.1}$$

Here, E_O^q is the total energy of the isolated molecule O atom/molecule in the charge state q. It is subtracted for a vacancy and added for an interstitial.

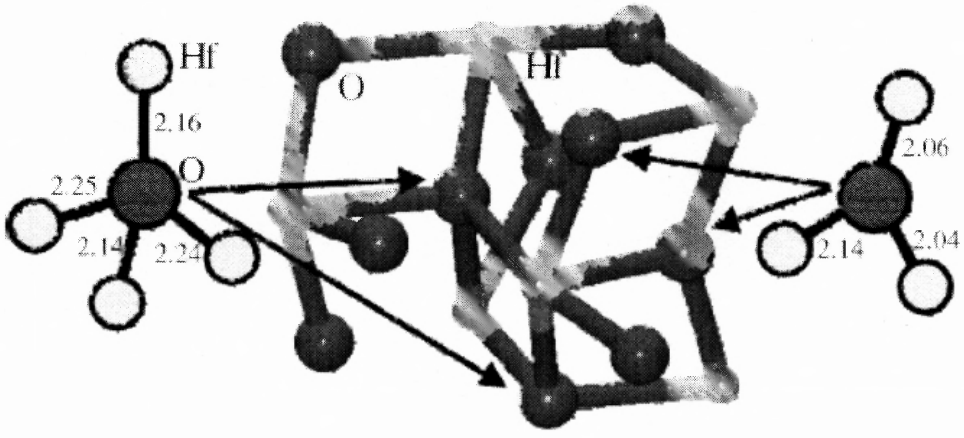


Figure 2.12 12-atom monoclinic hafnia cell having 3- and 4-fold coordinated O ions. Distances are in Armstrong.
Source: [33]

In order to study the stable charged defect states and understand their role in charge trapping as stipulated in Section 2.2, it is necessary to know electron affinities and ionization energies of the defect states with respect to the bottom of the conduction band of hafnia, and to the other source of charged carriers, i.e., Si substrate as shown in Figure 2.11. To realize this, comparison is made between the initial and final systems with the same number of electrons.

The absolute value of the defect ionization energy $I_p(D^q)$ as the vertical excitation energy of an electron from the defect with charge state q to the bottom of the conduction band may be defined with the following equation [33]:

$$I_p(D^q) = E_0^- + E_D^{q+1} - E_0^0 - E_D^q + \varepsilon_1 \qquad (2.2)$$

Here, E_0^- and E_0^{q+1} are the calculated energies of the perfect supercell with charge state -1 and 0, respectively, E_D^q is the energy of the defect with the charge state q. In Eq. 2.2 the value E_D^{q+1} is calculated for the geometry of the relaxed defect with charge state q and ε_1 is a correction for the bottom of the conduction band. Similarly, the electron affinity of the defect at the charge state q, $\chi_e(D^q)$, i.e., the energy gain when electron from the bottom of the conduction band is trapped at the defect can be defined using the following equation [33]:

$$\chi_e(D^q) = E_0^- + E_D^q - E_0^0 - E_D^{q-1} + \varepsilon_2 \tag{2.3}$$

Here, ε_2 is the correction factor. One can consider both "vertical" and "relaxed" electron affinities. For the latter case, the lattice relaxation after the electron trapping is included in E_D^{q-1}. One can also define the hole affinity of the defect, $\chi_h(D^q)$, i.e., the energy gain when a free hole is trapped from the top of the valence band to the defect as [33]:

$$\chi_h(D^q) = E_0^+ + E_D^q - E_0^0 - E_D^{q+1} + \varepsilon_3 \tag{2.4}$$

Again, ε_3 is the correction factor and E_D^{q+1} takes into account the lattice relaxation after hole trapping from the top of the valence band.

Defect levels within the bandgap of Hf-based oxide can be found from the calculated affinities after relaxation. However, to match with practical MOS devices it is approximated that

$$\chi_e(D^q) + \chi_h(D^q) = E_g(Expmntl) \tag{2.5}$$

Here, E_g is the bandgap of the oxide. To realize Eq. (2.5), approximation regarding the correction factors also needs to be made: $\varepsilon_1=\varepsilon_2=\varepsilon$ and $\varepsilon_3=0$. In the calculations, ε is defined as the following difference between experimental and theoretical values of E_g:

$$\varepsilon = E_g(Expmntl) - E_g(Thertcl) \tag{2.6}$$

Calculations based models assign different charge states to O vacancies/interstitials, and then calculate their formation and ionization energies, and affinities using the equations stated above. By optimizing ε, they place the defect levels within high-κ bandgap in the context of MOS band diagram. Their role as shallow/deep traps, as far as injection from gate/substrate is concerned, is then decided using the benchmarks described in Section 2.2.

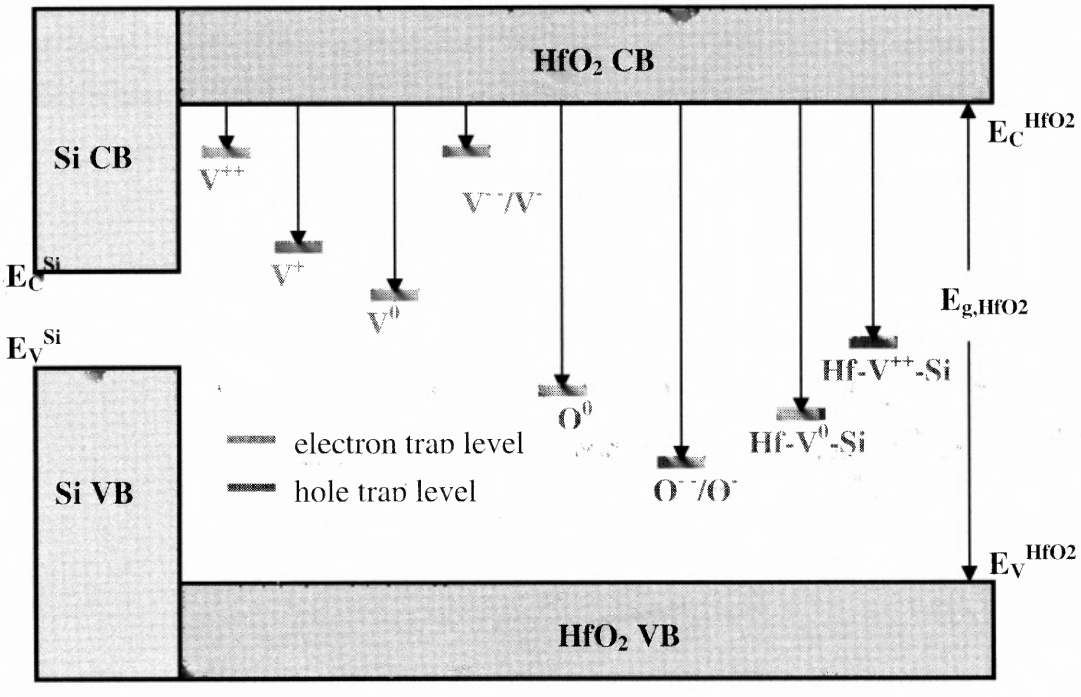


Figure 2.13 Calculated defect levels in the context of MOS diagram.

2.4.3.2 Calculation-based Models. Calculation-based models show that charged and neutral O vacancies $V^{++}/V^{+}/V^{0}/V^{-}/V^{--}$ are the potential electron traps in the bulk HfO_2 as shown in Figure 2.13. V^{++}, resonant with Si conduction band at positive gate bias (substrate injection) due to its shallow level, relaxes to deep V^{+} level after trapping an electron ($V^{++} + e \rightarrow V^{+}$). After trapping another electron V^{+} further relaxes to even deeper V^{0} level ($V^{+} + e \rightarrow V^{0}$). V^{0} level lies within Si bandgap in the context of MOS band diagram. Thus, negative-U behavior of V^{++}, due to strong electron-lattice interaction, is responsible for deep electron trapping which gives rise to slow transient trapping. On the other hand, V^{-}/V^{--}, lying near the oxide conduction edge, shows no such electron trapping induced relaxation ($V^{-} + e \rightarrow V^{--}$). Thus, V^{-} acts as a shallow traps and induces fast transient trapping.

O interstitials in the bulk HfO_2 are responsible for hole trapping. O^{--} and O^{-} have energy levels below Si valence band and after capturing holes ($O^{--} + h \rightarrow O^{-}$; $O^{-} + h \rightarrow O^{0}$), O^{0} level, resonant with Si valence band moves to its vicinity due to the negative-U behavior of O^{--}/O^{-}.

Calculations show that another potential hole trapping center is O 'arm' vacancy, i.e., Si-V^{0}-Hf, which induces energy levels below E_V^{Si} [3]. This vacancy is located at IL/high-κ interface. After capturing holes, Si-V^{++}-Hf induces energy levels above E_V^{Si}, but within Si bandgap range.

In the following tables, defect levels and formation energies found by the different groups are stated. It is obvious that, each group used different set of parameters as far as oxide bandgap, offset in Si/HfO^2 conduction edges are

concerned. This along with number of atoms used in unit supercell formation and level of optimization used in their calculations gave rise to variation in the values. However, the general trend as far as trapping induced relaxation is concerned is obvious.

Table 2.1 Calculated Defect Levels within HfO_2 Band-gap Responsible for Transient Trapping

Ref.	V^{++}	V^{+}	V^{0}	V^{+}/V^{++}	O^{-}/O^{--}	O^{0}	Hf-V^{++}-Si	Hf-V^{0}-Si	Ec^{HfO_2}-Ev^{HfO_2}	Ec^{HfO_2}-Ec^{Si}
Torii et al. [35]	0.3eV	1.3eV	1.6eV	____	Below E_V^{Si}	Below E_V^{Si}	___	___	5.6 eV	1.5eV
Gavartin et al. [38]	0.8eV	3.4eV	3.1eV	0.4eV	___	___	Above E_V^{Si}	Below E_V^{Si}	6.1 eV	2eV
Robertson et al. [36]	0.4eV	1.3eV	2eV	0.7eV	5.5eV	5.5eV	___	____	5.8 eV	1.5 eV
Foster et al. [33]	2.93eV	2.76 eV	___	___	4.8eV	___	___	____	5.7 eV	1.5 eV

Table 2.2 Calculated Formation Energies of Defects Responsible for Transient Trapping

Ref.	$V^{++}/V^{+}/V^{0}$	Hf-V^{++}-Si/Hf-V^{0}-Si
Gavartin et al.[38]	7 eV	4 eV
Foster et al. [33]	9 eV	-----

2.5 Experimental Evidence of Presence of O Vacancies

Electron transfer from O vacancies adjacent to the gate within the bulk high-κ oxide to high work function metal gate ($V^0 - 2e \rightarrow V^{++}$) leads to the formation of dipole layer, which shifts flatband voltage (V_{FB}) [29]. This is illustrated for Re/HfO_2/n-Si gate stacks in Figure 2.14. The magnitude of V_{FB} shift depends on the concentration of O vacancies and their distribution within the bulk oxide. V_{FB} shifts can be induced in oxidizing ambient without incurring interfacial re-growth, due to O diffusion toward substrate and subsequent oxidation, if low temperature and low O_2 partial

partial pressures are used. This is evident from Figure 2.15(a) that V_{FB} increases with annealing in dilute N_2/O_2 mixtures at low temperatures. The almost constant capacitance at the accumulation regime shows that interfacial growth has not

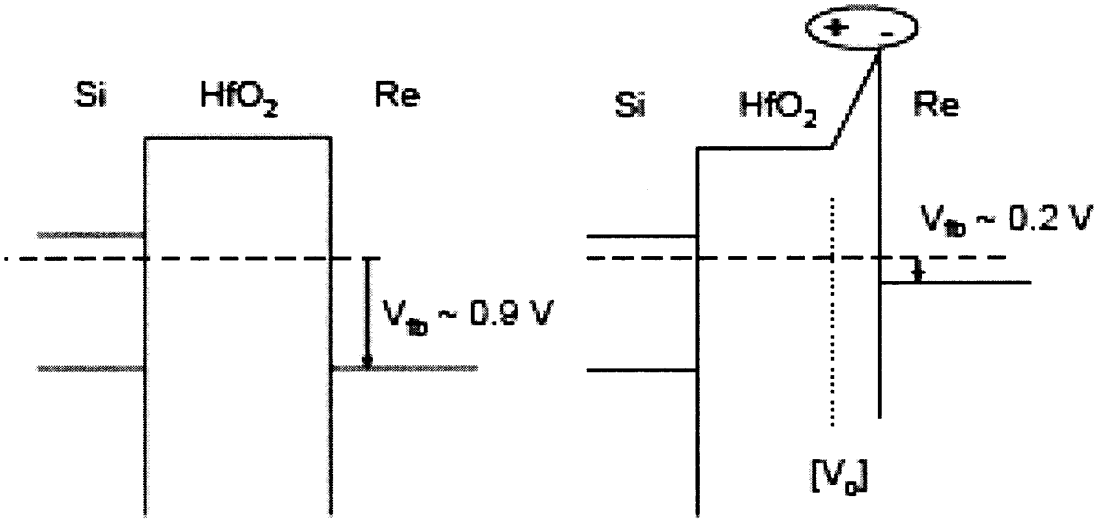


Figure 2.14 MOS band diagrams showing flatband voltage (V_{FB}) shift due to dipole formation between positively charged O vacancy and metal gate Re.
Source: [46]

been experimentally observed to decrease the dipole induced reduction in effective work function difference. As a further evidence, it is shown in Figure 2.15(b) that V_{FB} shift after O_2 anneal can be reversed if FGA is applied afterward. Reducing ambient of FGA increases O vacancies, and thus increases V_{FB}. These experimental observations clearly show the presence of O vacancies in Hf-based oxides.

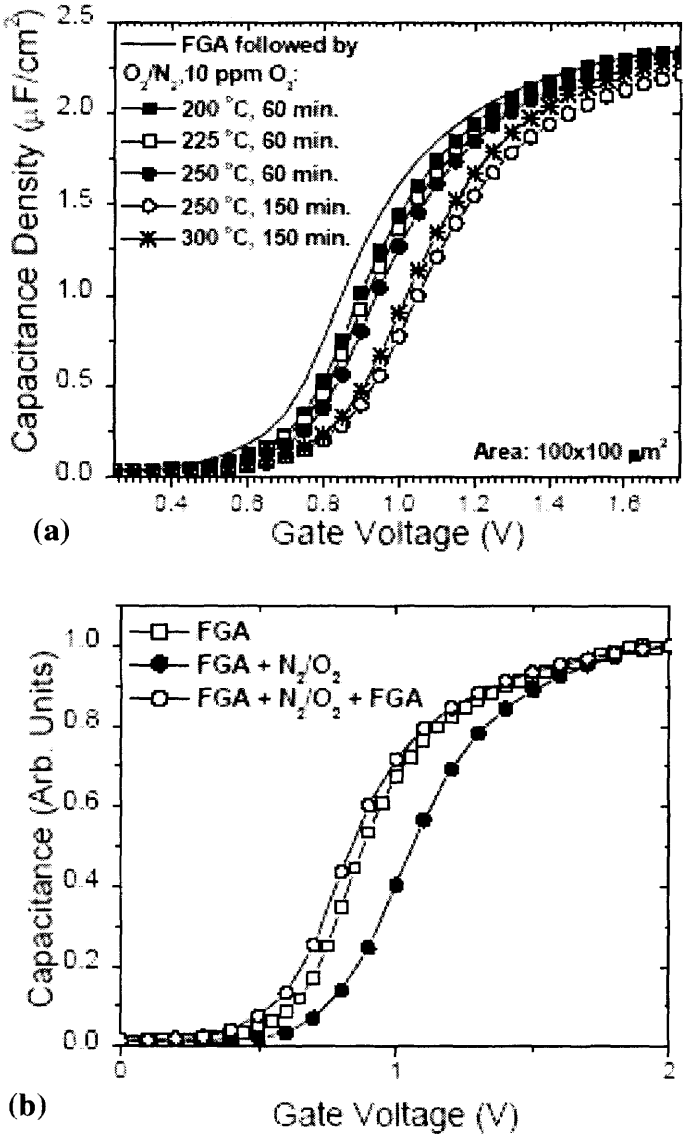


Figure 2.15 **(a)** Shift in C-V for N_2/O_2 anneal at different low temperatures and time conditions. **(b)** Shift in C-V under oxidizing and reducing conditions [46].

2.6 Summary

In Chapter 2, calculation based model of defect levels as par their physical origins are described in details for high-κ gate stacks. The effect of the relative location of the defect level on transient trapping is stated. Physical models of fast and slow transient trapping based on experimental observations are also discussed. However, a comprehensive model incorporating experimentally observed defect levels, and their roles in trapping and transport is yet to be systematically formulated for the candidate high-κ gate stacks.

CHAPTER 3

DEVICE FABRICATION AND ELECTRICAL CHARACTERIZATION

3.1 Introduction

In Chapter 3 fabrication of MOS devices TiN/$HfSi_xO_y$ based gate stacks are described. Different electrical characterization techniques used in the course of this research are discussed. For fast and efficient characterization, automation of different types of measurements is imperative. As part of this research, such automation programs were developed in LabView environment, details of which are provided in Chapter 3.

3.2 TiN/$HfSi_xO_y$ based MOS Devices Fabrication

3.2.1 MOCVD and ALD

Metal organic chemical vapor deposition (MOCVD) is a process by which gaseous molecular precursors are converted into solid-state materials, usually in the form of a thin film, on a heated surface [47], [48]. Ease of manufacture, high controlled deposition rate, good film conformity and ability to control deposition easily are the major advantages. This is why this is extensively used for high-κ deposition on Si substrate. Since MOCVD process involves the decomposition of a molecular precursor, careful choice of precursors is vital. If precursors are poorly chosen unacceptable level of residual impurities may reside in the film, which leads to a large number of trap sites and adversely affect reliability of MOS devices. Like MOCVD, atomic layer deposition (ALD) is a chemical gas phase thin film deposition method

atomic layer deposition (ALD) is a chemical gas phase thin film deposition method [49], [50]. In ALD method, the film is grown through sequential saturative surface reactions that are realized by pulsing the two or more precursors into the reactor alternatively, one at a time, separated by purging or evacuation steps. The major advantage is that film growth is self-limiting. This is why film thickness is dependent only on the number of deposition cycles. This leads to an accurate and simple thickness control, which is ideal for large area uniformity and conformity. Moreover, binary processes are easy to combine using ALD method, which is the key to the preparation of multi-component and multi-layer materials. Hence, it is an ideal m choice for good quality metal gate/high-κ deposition. The major drawback is the low deposition rate, which is due to the deposition of a fraction of a monolayer in one cycle.

3.2.2 TiN/Hf-Silicate Based MOS Device Fabrication

Hafnium silicate ($HfSi_xO_y$ –20% SiO_2) film and TiN metal gate were deposited by MOCVD technique [51] on both n- and p-type Si substrates after ozone treatment had been performed for the pre-dielectric deposition cleaning, which resulted in ~10Å of chemical oxide growth at the dielectric and Si substrate interface [51]. Isolation edge and n^+/p^+-ringed MOS capacitors of different gate areas, and n- and p-channel MOSFETS of different lengths were fabricated using the standard CMOS process flow. Using HRTEM, the physical thickness has been measured to be 4.5nm including an interfacial layer (IL) of 1nm [52], [13]. These devices were further subjected to NH_3 PDA at 700°C for 60s to improve leakage performance. Physical

characterization details can be found elsewhere. An effective oxide thickness (EOT) of 1.8-2 nm was estimated from high-frequency C-V measurements after quantum mechanical corrections.

3.2.3 TiN/HfO_2based MOS Devices Fabrication

HfO_2 film and TiN metal gate were deposited by ALD method on p-type Si substrates to fabricate high-κ MOS devices [50]. TEMA Hf, $Hf[N(CH_3)(C_2H_5)]_4$ was used as precursor in O_3 ambient. N^+-ringed nMOS capacitors, and nMOSFETs were fabricated using the standard CMOS process flow. The lots of sample sets and their corresponding splits, used in this work, are specified in Table 1. Three different lots are used. Lot1 has three splits with $t_{H\text{-}K}/t_{IL}$ combinations of 2.6 nm/1.1 nm, 2.7 nm/0.7 nm, and 3.3 nm/0.7 nm. Here, 0.7 nm of IL was achieved by scavenging O from in-situ steam generated, ISSG IL after the deposition of high-κ. Lot 2 has seven splits having different IL quality for fixed $t_{H\text{-}K}$ of 3 nm. In splits 1 and 2, high-κ was deposited after HF cleaning of substrate before deposition, which resulted in IL growth of 1.1 nm. In splits 3 and 4, ISSG IL of 2.1 nm was grown first. Then it was etched back to 0.7 nm. Afterwards, ALD HfO_2 was grown. For splits 5 and 6, IL was etched back to 1.1 nm. HfO_2 was grown above 2.1 nm of ISSG IL in split 7. Pre-depostion surface treatment by annealing in NH_3 ambient was done for splits 2, 4, 6 and 7. Lot3 has seven splits of different $t_{H\text{-}K}$ (3/5/7/10 nm) for 1.1 nm of t_{IL}. High-κ layer was grown after O_3 cleaning of surface for splits 1, 3 , 4 and 6. This resulted

Table 3.1 Description of Different Splits from Various Lots Tested in the Work.

High-κ based MOS structures:

Lot#	Split#	Gate	High-κ	IL	PreDA	PostDA
1	1	ALD TiN	2.6 nm ALD HfO_2	1.1 nm ISSG	None	NH_3 700C 60s
	2	ALD TiN	2.7 nm ALD HfO_2	0.7 nm Getterred	None	NH_3 700C 60s
	3	ALD TiN	2.6 nm ALD HfO_2	0.7 nm Getterred	None	NH_3 700C 60s
2	1	ALD TiN	3 nm ALD HfO_2	1.1 nm HF-last	None	NH_3 700C 60s
	2	ALD TiN	3 nm ALD HfO_2	1.1 nm HF-last	NH_3 700C 60s	NH_3 700C 60s
	3	ALD TiN	3 nm ALD HfO_2	0.7 nm ISSG	None	NH_3 700C 60s
	4	ALD TiN	3 nm ALD HfO_2	0.7 nm ISSG	NH_3 700C 60s	NH_3 700C 60s
	5	ALD TiN	3 nm ALD HfO_2	1.1 nm ISSG	None	NH_3 700C 60s
	6	ALD TiN	3 nm ALD HfO_2	1.1 nm ISSG	NH_3 700C 60s	NH_3 700C 60s
	7	ALD TiN	3 nm ALD HfO_2	2.1 nm ISSG	NH_3 700C 60s	NH_3 700C 60s
3	1	ALD TiN	3 nm ALD HfO_2	1.1 nm O_3 clean	None	N_2 600C 60s
	2	ALD TiN	3 nm ALD HfO_2	1.1 nm ISSG	None	N_2 600C 60s
	3	ALD TiN	5 nm ALD HfO_2	1.1 nm O_3 clean	None	N_2 600C 60s
	4	ALD TiN	7 nm ALD HfO_2	1.1 nm O_3 clean	None	N_2 600C 60s
	5	ALD TiN	7 nm ALD HfO_2	1.1 nm ISSG	None	N_2 600C 60s
	6	ALD TiN	10 nm ALD HfO_2	1.1 nm O_3 clean	None	N_2 600C 60s
	7	ALD TiN	10 nm ALD HfO_2	1.1 nm ISSG	None	N_2 600C 60s

SiO_2 based MOS structures:

Lot#	Split#	Gate	Oxide	PreDA	PostDA
4	1	ALD TiN	1.6 nm ISSG		NH_3 700C 60s

HfSiO based MIM structures:

Lot#	Split#	Top metal	High-κ	Bottom metal	PostDA
5	1	ALD TiN	4 nm ALD $HfSi_xO_y$ (10% SiO_2)	ALD TiN	N_2 800C 20s

in the growth of 1.1 nm of chemical SiO_x as IL. For the rest of the splits, 1.1 nm of IL was grown using ISSG method. Post-deposition anneal, PDA was done in NH_3 ambient at 700°C for 60 secs in lots 1 and 2. For lot 3, PDA was done at 600°C for 60 secs in N_2 ambient. MOS devices with ISSG 1.6 nm SiO_2 and TiN metal gate are ALD method for MIM structures in lot 5. They were subjected to 800°C PDA in N_2 ambient for 60 secs. ALD TiN was used as the bottom and top electrodes.

3.3 Electrical Characterization

Measurements of the electrical properties, parameters extracted from these measurements and control over these parameters lead to stable and high performance MOS devices. Bulk oxide and oxide-substrate interface are two major regions of the MOS system. Charges in these two regions are undesirable because they adversely affect the device performance and stability. The MOS capacitors and transistors are being used to study the electrical characteristics as they have the advantage of simplicity of fabrication and analysis. Following measurements techniques have been employed in characterizing the charges present in MOS capacitors and transistors using HfO_2 as gate dielectric.

3.3.1 High Frequency and Low Frequency C-V measurements

A dielectric material is deposited as a thin film, on p- or n-type semiconductor surfaces (e.g., Si, Ge) by various techniques including thermal oxidation, sputtering, and chemical vapor deposition [53]. On top of that, gate metals like Al and Pt are deposited to complete the MIS structure (Figure 3.1). Inside the dielectric, there are

four different types of charges that contribute to the capacitance: (i) fixed oxide charge, primarily due to the structural defects in the dielectric; (ii) oxide trapped charge, whose origin is due to trapped electrons or holes in the bulk of the dielectric; (iii) mobile ionic charge, if ionic impurities are present in the dielectric; and (iv) interface charge, formed due to oxidation-induced structural defects and by broken bonds at the interface. These charges can be measured by measuring the capacitance as a function of voltage. During the measurement a dc voltage is swept from the negative to positive direction and is superimposed by an ac signal with a small amplitude of 10-15 mV. The dc voltage determines the bias condition while the ac voltage is necessary to measure the capacitance.

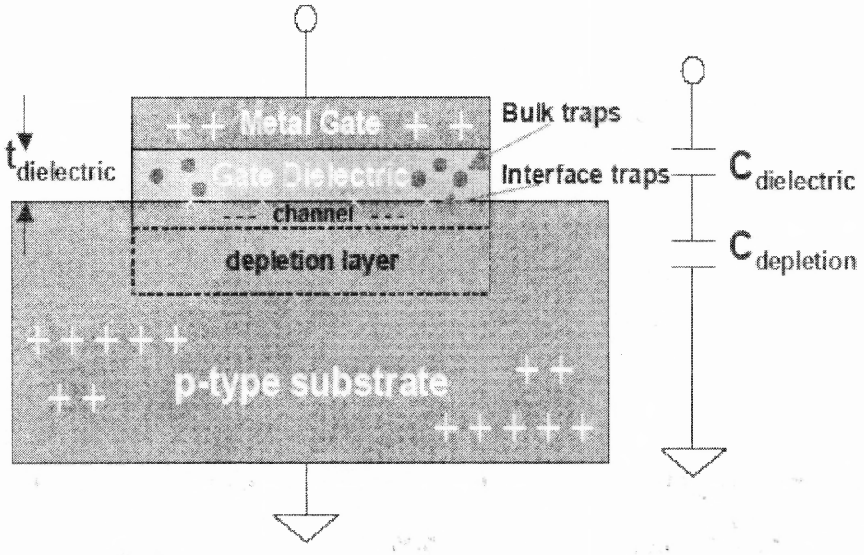


Figure 3.1 A metal/insulator/semiconductor (p-type) (MIS) structure is shown that is used extensively to characterize dielectric films. Dielectric/semiconductor interface traps and bulk traps are shown. For positive gate bias, semiconductor and metal gate act as cathode and anode, respectively, whereas for negative gate bias, the opposite holds. The equivalent circuit of the series capacitance of dielectric and depletion capacitances is also provided.
Source: [53]

When the voltage is swept across the MIS device, the semiconductor surface goes through an accumulation of majority carriers (electrons for n-type and holes for p-type), depletion of majority carriers, or inversion with minority carriers. For example, if a p-type semiconductor is considered for a MIS device and a negative potential is applied at the metal electrode (gate), mobile positive holes, the majority carriers accumulate at the dielectric-semiconductor interface during accumulation. These carriers form a thin layer, which acts much like a parallel plate capacitor equal in area to the gate. Once the voltage is raised to a small positive value, the holes are repelled, causing depletion. Raising the voltage further attracts electrons to the interface. The electrical equivalent circuit of a MIS capacitor is, therefore, a series combination of a fixed voltage-independent gate oxide (insulator) capacitance and a voltage-dependent semiconductor capacitance due to depletion (Figure 3.1). Figure 3.2 shows the C-V characteristics of MIS structures with a dielectric deposited on a p-type semiconductor. Both the cases of dielectric with and without traps (ideal case) are considered. The capacitance in the accumulation region is defined by the gate area (A) and the dielectric thickness ($t_{dielectric}$) and is designated as $C_{dielectric}$ (the accumulation capacitance). The dielectric constant (κ) can be obtained from the following equation:

$$K = \frac{C_{dielectric}\ t_{dielectric}}{A} \tag{3.1}$$

The central region of the C-V curve, where the capacitance changes rapidly with the gate voltage, is the depletion region that contributes to a depletion

capacitance, $C_{depletion}$, further separating the effective capacitor plates and decreasing the device capacitance (as two capacitances in series reduce the overall capacitance). The depletion region starts at a voltage defined by the flatband voltage (V_{FB}). The effective value of capacitance is now given by Equation 3. 2:

$$C_{total} = \frac{C_{dielectric}\ C_{depletion}}{C_{dielectric} + C_{depletion}} \quad \text{(farads)} \tag{3.2}$$

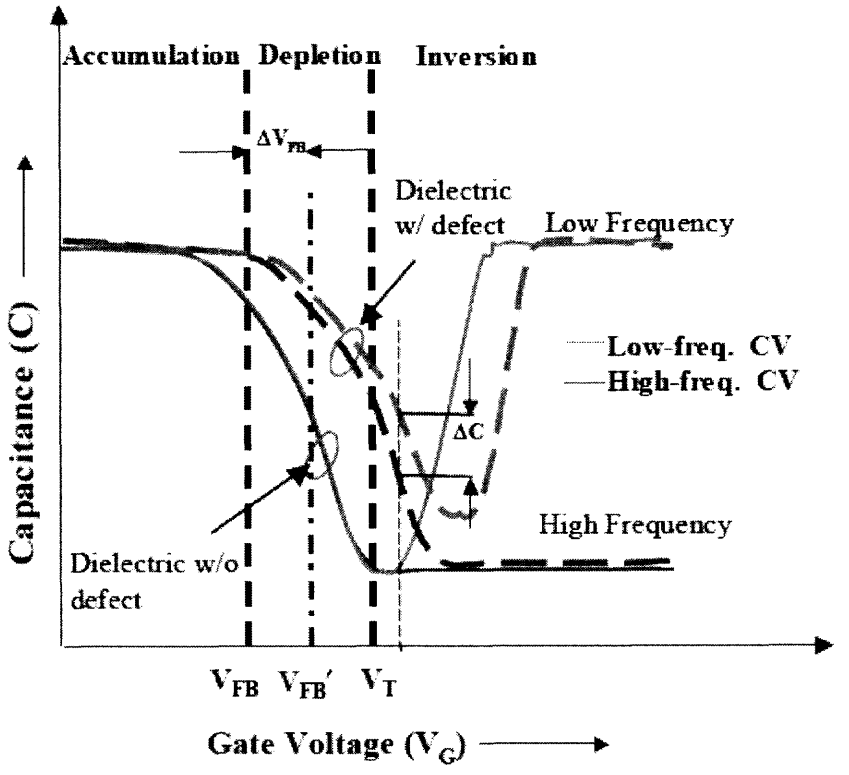


Figure 3.2 High-frequency (hf) and low-frequency (lf) capacitance-voltage (C-V) characteristics of MIS structure for dielectric films with and without (ideal) defects are shown. Flatband voltage shift of hf C-V, $\Delta V_{FB} = (V_{FB}' - V_{FB}) > 0$ indicates negative charge trapping. For a film with defects, stretch-out of hf C-V, and offset in capacitance, ΔC, in between hf and lf C-V indicate the presence of interface traps. Source: [53]

The capacitance decreases till the depletion width reaches a maximum and inversion sets in. Inversion forms a layer of minority carriers (electrons in this case)

—hence, called inversion layer. In the inversion region, the value of the capacitance depends on whether the measurement is conducted at low-frequency (0.01 to ~1 Hz) or at high frequency (~1 MHz). When measured at high frequency, the charges are not able to follow the signal and the capacitance is clipped to the capacitance at maximum depletion width. The low-frequency capacitance includes the contribution from the minority carriers also and, consequently, the capacitance increases. At strong inversion, the minority carriers become more significant and, this is why, the capacitance is only due to the inversion capacitance. As shown in Figure 3. 2, the presence of negatively charged traps in the bulk dielectric and interface traps cause the high frequency C-V plot to shift in parallel to the right of the ideal curve, and to stretch out along the bias axis, respectively. The shift in flatband voltage, $\Delta V_{FB} = V_{FB}' - V_{FB}$ is used in Equation 3.3 to calculate the total trapped charge in the dielectric, Q_{tot}:

$$Q_{total} = C_{dielectric}\, \Delta V_{FB} \text{ (coulombs)} \tag{3.3}$$

Due to capacitance across the dielectric film, negative charge trapping in film translates to $\Delta V_{FB} > 0$, whereas for positive charge trapping, it is $\Delta V_{FB} < 0$.

Interface traps also cause an offset in between low-frequency and high-frequency C-V plots (ΔC) as shown in Figure 3.2. This offset can be utilized to calculate interface trap level density (D_{it}) from the measured high-frequency

capacitance (C_{hf}) and low-frequency capacitance (C_{lf}) at a certain gate bias:

$$D_{it} = \frac{C_{dielectric}}{q}\left(\frac{C_{lf}/C_{dielectric}}{1-C_{lf}/C_{dielectric}} - \frac{C_{hf}/C_{dielectric}}{1-C_{hf}/C_{dielectric}}\right) \quad (3.4)$$

$(cm^{-2}\ eV^{-1})$

Here, q is charge of an electron. D_{it} can be measured for different gate biases in the depletion regime.

3.3.2 Conductance Measurement

The measurement of surface conductance also enables computation of the interface state density, D_{it}, especially for devices with low interface trap density. Difficulty arises in capacitance measurements because the interface-trap capacitance must be extracted from the measured capacitance that consists of oxide capacitance, depletion-layer capacitance, and interface-trap capacitance. While the capacitance and conductance as functions of voltage and frequency contain identical information about the interface, greater inaccuracies arise in extracting this information from the measured capacitance, because difference between two capacitances must be used. In the conductance method this difficulty does not apply as the measured conductance is directly related to the interface traps.

Interface traps maintain electrical communication with the semiconductor substrate by capturing and emitting carriers (electrons/holes) depending on the gate bias, which induces a change of occupancy in them. If a dc bias is kept constant and simultaneously an ac test signal is applied, a change of occupancy causes an energy

loss, which depends on test signal frequency for the given dc bias. If frequency is too low, traps respond immediately; if too high, they do not respond at all. Energy loss, which is due to capture/emission of carriers by interface traps, and is represented by an equivalent conductance, G_p, of the MIS structure, is minimal in both the cases. However, in the low frequency range, for a given bias if frequency is increased gradually, energy loss increases as more interface traps respond with a time lag. If the frequency is increased further, it starts to decrease as fewer traps respond. Maximum energy loss occurs when most of the interface traps respond. So, G_p, measured over a wide range of frequencies and gate voltages, is a measure of D_{it} with

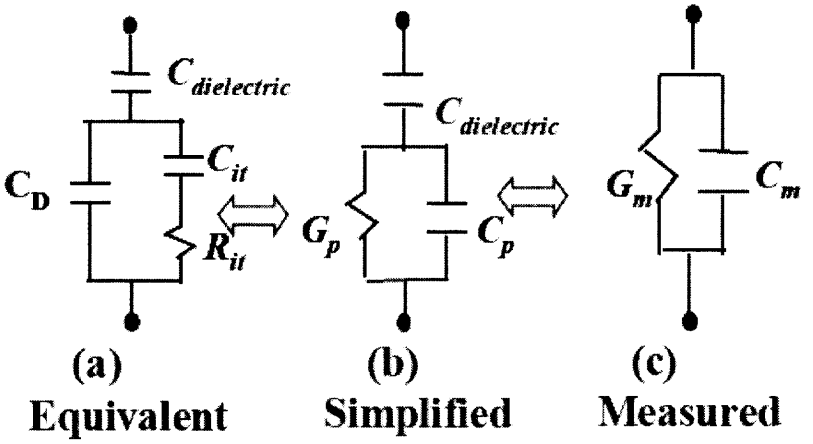


Figure 3.3 (**a**) Equivalent circuit for MIS structures with interface traps. R_{it} and C_{it} represent interface traps induced energy loss and charge storage, respectively. (**b**) Simplified circuit, derived from (**a**), for analysis. Equivalent conductance, G_p, is computed from measured data as a function of both test (ac) signal frequency and gate bias (dc). (**c**) Circuit representing parallel capacitance (C_m) and conductance(G_m), which is measured across two-terminal MIS structures for different frequencies and biases using conventional instruments (e.g., LCR meter).
Source: [53]

respect to gate bias. An equivalent circuit as shown in Figure 3.3(a) represents a MIS structure with interface traps. Here, R_{it} represents the energy loss due to interface

traps, while C_{it} represents the capacitance due to charge stored in those traps. Formation of a depletion region, whose capacitance is represented by CD, takes place along with interaction of semiconductor carriers with interface traps. Hence, CD is shown in parallel with the series combination of C_{it} and R_{it}. Storage of charge across the dielectric material occurs in addition to that in the depletion region and at the interface traps. Thus $C_{dielectric}$ remains in series with the network mentioned above. A simplified circuit (Figure 3.3 (b)) contains the parallel combination of equivalent conductance, G_p, and capacitance, C_p, which can be derived from the parallel network of Figure 3.3 (a). The measured parallel conductance, G_m, and capacitance, C_m, are also indicated (Figure 3.3 (c)) across the two-terminal MIS structure using conventional measurement instruments (e.g., a LCR meter). To find G_p from the measured data, the following equation is used:

$$G_p / \omega = \frac{\omega G_m C_{dielectric}^2}{G_m^2 + \omega^2 (C_{dielectric} - C_m)^2} \quad (F/cm^2) \tag{3.5}$$

where $\omega=2\pi f$ is the radian frequency. G_p is estimated as a function of both gate bias and frequency, especially in the depletion regime, and G_p/ω vs. log(f) is plotted for each gate bias (Figure 3.4). Dit can be calculated from the highest peak of G_p/ω vs. log(f) plots using Equation 3.6:

$$D_{it} = \frac{2.5}{q} \left(\frac{G_p}{\omega} \right)_{max} \quad (cm^{-2} eV^{-1}) \tag{3.6}$$

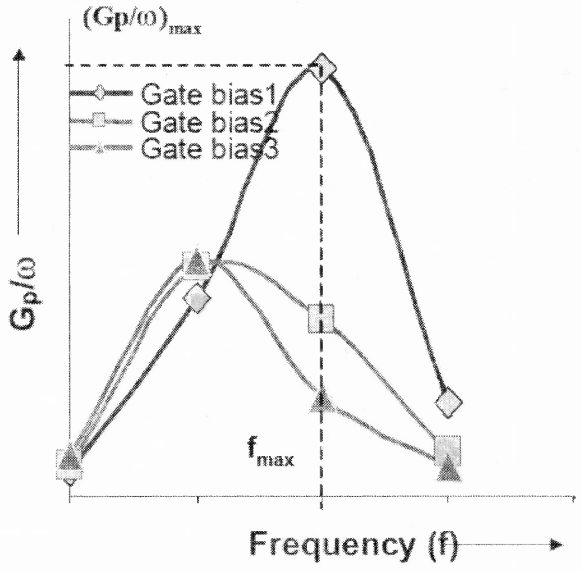


Figure 3.4 Gp/ω vs. log(f) plots for different gate biases in the depletion regime. D_{it} is computed from the highest peak of the plot.
Source: [53]

The leakage current through the dielectric material can be measured by varying the gate bias. For ultrathin films significant leakage current occurs via quantum mechanical tunneling of electrons from cathode to anode under the electric field across the dielectric, $E_{dielectric} = (V_G - V_{FB})/t_{dielectric}$, where $t_{dielectric}$ is film thickness. Defects in the films may also assist in tunneling, which is more pronounced for low gate bias values. Thus leakage current flow at low bias is a good indication of presence of defects in dielectric films. In summary, the MIS device structure seems to be ideal for electrical characterization of dielectric films. Parameters like the dielectric constant can be measured and pre-existing defects can be quantified in the dielectric bulk and at the semiconductor/dielectric interface. The measurement techniques described above are quite versatile for the characterization of a wide range of dielectric materials used not only in the electronics industry but also in other disciplines.

3.3.3 I-V Measurements

Gate current-voltage (I-V) measurements are crucial to understanding the reliability of oxides in MOS devices. For the stacked structures of the high-κ devices, I-V characteristics is dependent on the polarity and band-bending conditions, and the defect energy levels lying within the high-κ bandgap. These factors, in this way, determine the type of the dominant conduction mechanism for a particular gate bias condition. Increase in stress-induced leakage current (SILC), due to higher post-stress trap assisted tunneling (TAT), is widely used to study the reliability of the gate oxides. However, its applicability in the high-κ devices is limited under nominal stress conditions as defect generation within the bulk oxide is energetically costly.

Dominant conduction mechanisms under substrate and gate injection conditions are shown in Figure 3.5 for high-κ gate stacks. For low bias conditions under substrate injection, direct tunneling (DT) dominates. For a comparatively high bias, DT and Poole-Frenkel (PF) dominates. For higher bias, PF dominates. Under gate injection, DT and trap-assisted tunneling dominates unless gate bias is high. For high bias, FN dominates. Direct tunneling is the flow of electrons through the full oxide thickness as illustrated in Figure 3.6. The leakage current density is given by the following equation:

$$J_{DT} = AE_{ox}^{2} \exp\left(\frac{-B\left[1-\left(1-qV_{ox}/\Phi_{B}\right)^{1.5}\right]}{E_{ox}}\right) \tag{3.7}$$

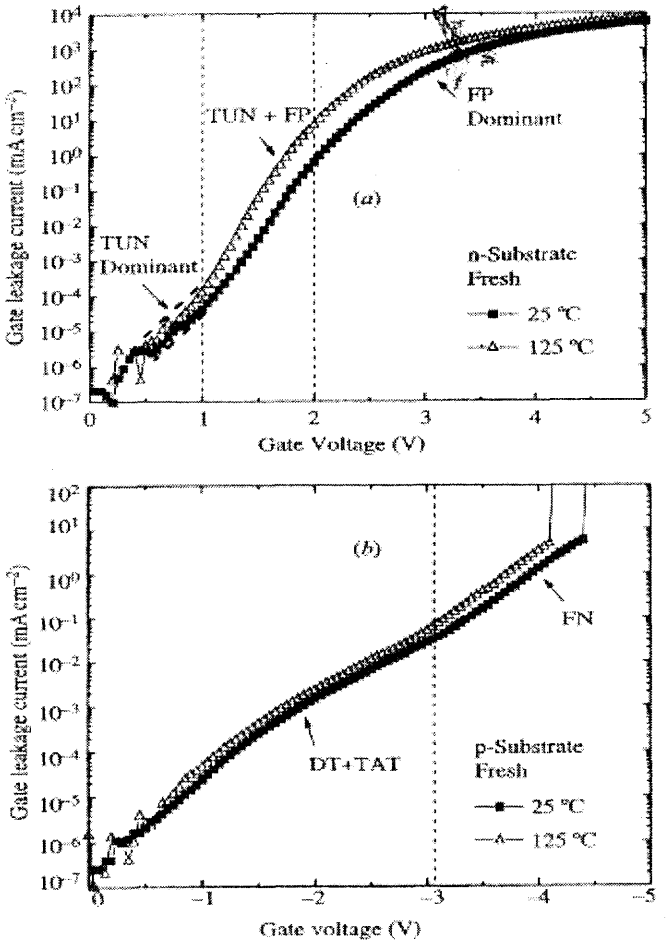


Figure 3.5 I-V characteristics for TiN/HfO_2(4 nm)/SiO2(1 nm) gate stack under **(a)** substrate and **(b)** gate injection conditions.
Source: [54]

Here, A and B are constants, E_{ox} is oxide electric field, V_{ox} is the potential difference across the gate oxide and Φ_B is the barrier height seen by injected electrons. It is obvious that DT does not depend on temperature. FN tunneling is the flow of electrons through a triangular potential barrier illustrated in Figure 3.6. FN current

density is given by the following expression:

$$I_{FN} = A_G A E_{OX}^2 \exp\left(\frac{-B}{E_{OX}}\right) \tag{3.8}$$

$$A = 1.54\times10^{-6}\frac{(m/m_{OX})}{\Phi_B}\left[\frac{A}{V^2}\right] \tag{3.9}$$

$$B = 6.83\times10^{7}\sqrt{((m/m_{OX})\Phi_B^3)}\left[\frac{V}{cm}\right] \tag{3.10}$$

Here, A_G is the gate area, E_{ox} the oxide electric field, and A and B are usually considered to be constants. For Equations (3.9) and (3.10) m_{ox} is the effective electron mass in the oxide, m is the free electron mass and Φ_B is the effective barrier height at semiconductor/oxide interface which takes in to account barrier height lowering and quantization of electrons at the semiconductor surface. Here,

$$E_{OX} = \frac{V_{OX}}{t_{OX}}; V_{OX} = V_G - V_{FB} - \phi_S \tag{3.11}$$

Where, ϕ_S is the surface potential and V_{FB} flatband voltage. If V_{OX} is lower than Φ_B

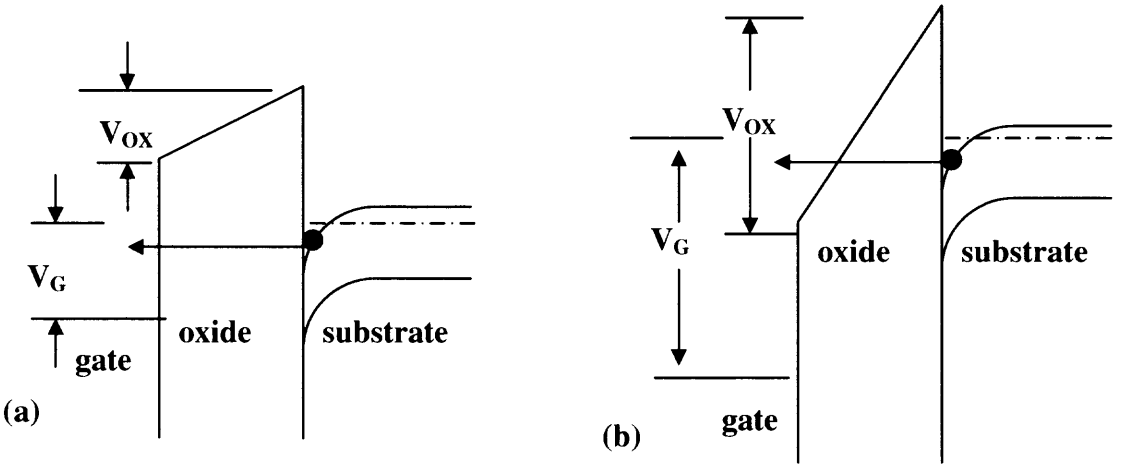


Figure 3.6 Band diagram for **(a)** direct tunneling and **(b)** F-N tunneling.

then DT dominates, otherwise FN tunneling occurs for high VG as shown in Figures 3.6 (a) and (b).

Poole-Frenkel (PF) emission is due to the field-enhanced thermal excitation of trapped electrons into conduction as shown in Figure 3.7. Conduction across the oxide in MOS structure due to PF emission can be described with the following equation [55]:

$$J \approx E_{OX} \times \exp\left[\frac{-q \times \left(\phi_B - \sqrt{qE_{OX} / \pi\varepsilon_i}\right)}{kT}\right] \tag{3.12}$$

Here, J is the leakage density, E_{OX} is the oxide electric field, q is electron charge, ϕ_B is the barrier height of the trap, ε_i is the insulator permittivity, k is the Boltzmann's constant and T is temperature. It is obvious that the trap barrier heights can be determined from Arrehinius plot of $\ln(J/E_{ox})$ if leakage current is measured under substrate and gate injection conditions at the elevated temperatures. It may be noted that the observed barrier height is δE less than the original ($= E_C - E_T$) value under the electric field induced band bending condition as illustrated in the Figure.

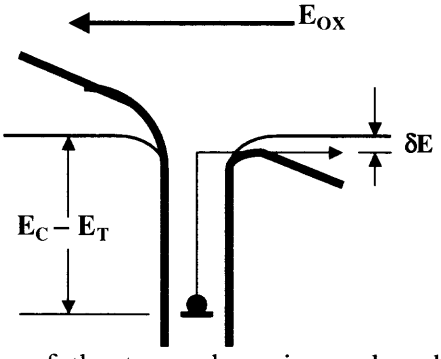


Figure 3.7 P-F emission of the trapped carrier under electric field and elevated temperature conditions.

3.3.4 I_d-V_g Measurements

Drain current-gate voltage measurements by simultaneously applying sweeping bias at the gate and drain and grounding substrate and source is an effective way to measure thresold voltage, V_T of an nMOSFET as shown in Figure 3.8. V_T can be also

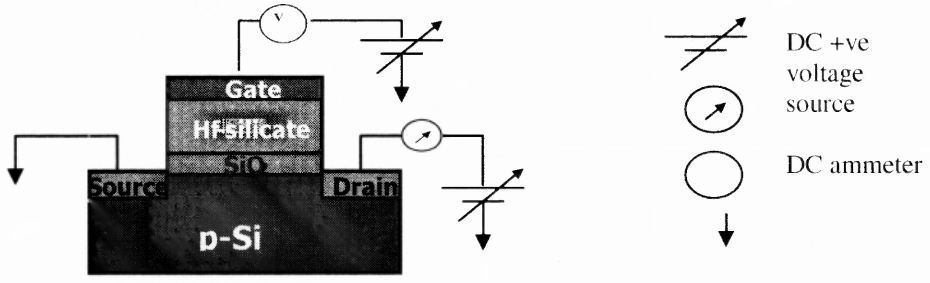


Figure 3.8 I_d-V_g measurement set-up for an n-channel MOSFET.

Be determined in the MOSFET saturation regime. The drain current in saturation is as follows [55]:

$$I_{D,sat} = \frac{mW}{L} \mu eff C_{OX} (V_{GS} - V_T)^2 \qquad (3.13)$$

where m is function of doping density , W and L are effective width and length of MOSFET, μ_{eff} is effective mobility of the carriers at the channel, C_{ox} is the oxide capacitance and V_{GS} is drain-to-source voltage. V_T is determined by plotting $I_D^{0.5}$ vs. V_{GS} and extrapoltaing the curve to zero drain current as shown in Figure 3.9. Since I_d is dependent on mobility degradation and series resistance, V_T is extrapolated at the point of maximum slope. Setting V_{GS}=V_{DS} ensures operation in the saturation region. Moreover, the maximum slope is equal to (mW/L) $\mu_{eff}C_{OX}$ [57], and, consequently, prortional to effective mobility.

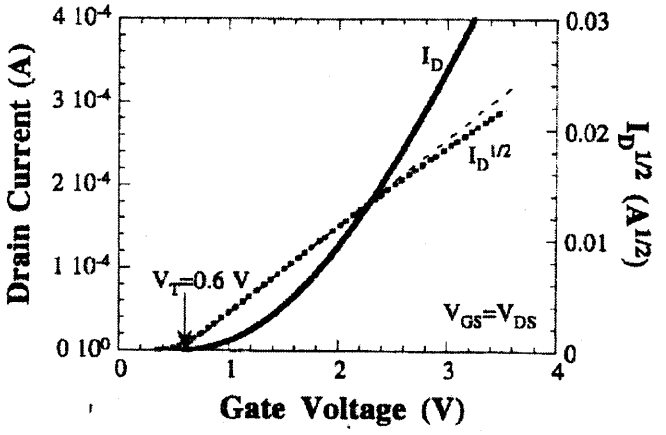


Figure 3.9 V_T determination from $I_d^{0.5}$-V_g plot.
Source: [57]

3.3.5 Subthreshold Current Method

The drain current of a MOSFET operated at gate voltages below threshold can be as follows [57]:

$$I_D = I_{D1} \exp\left(\frac{q(V_G - V_T)}{nkT}\right)\left(1 - \exp\left(\frac{-qV_D}{kT}\right)\right) \tag{3.14}$$

Where, I_{D1} is a constant that depends on temperature, device dimensions and substrate doping density; n, given by $n = 1 + (C_b + C_{it})/C_{ox}$. Here, C_b, C_{it} and C_{ox} are space-charge region, interface states and oxide capacitances, respectively. This accounts for the charge placed on the gate that does not result in inversion layer charge. Some gate charge is imaged as space-charge region charge and some as interface trap charge. Ideally n= 1, but n> 1 as the doping density increase. ($C_b \sim N_A^{0.5}$) and as the interface trap density increases ($C_{it} \sim D_{it}$).

The usual subthreshold plot is one of log (I_D) vs. V_G for $V_D >> kT/q$. The measurement is simple to do, requiring merely a current-voltage measurement of a

MOSFET. Such a plot has a slope of q/[ln(10)nkT]. The slope is usually expressed as the subthreshold swing S, which is that gate voltage necessary to change the drain current by one decade, and is given by

$$S = [\ln(10)nkT]/q \approx 60n(T/300) \text{ mV/decade} \tag{3.15}$$

The interface trap density obtained from a plot of $\log(I_D)$ vs. V_g is

$$D_{it} = \frac{1}{q}\left(\frac{qS}{2.3kT} - 1\right)C_{OX} - C_b \tag{3.16}$$

requiring an accurate knowledge of C_{ox} and C_b. An additional complication is the dependence of the slope on surface potential fluctuations. For this reason, this method is used as a comparative technique to understand electrical stress or energetic radiation induced damage to the interface by measuring S before and after stress or radiation. ΔS is easier to interpret. A typical subthreshold MOSFET curve is shown in Figure 3.10 by plotting $\log_{10}(I_D)$ vs. V_G plot. V_T is measured using the technique in Section 3.2. S is measured in the subthreshold region.

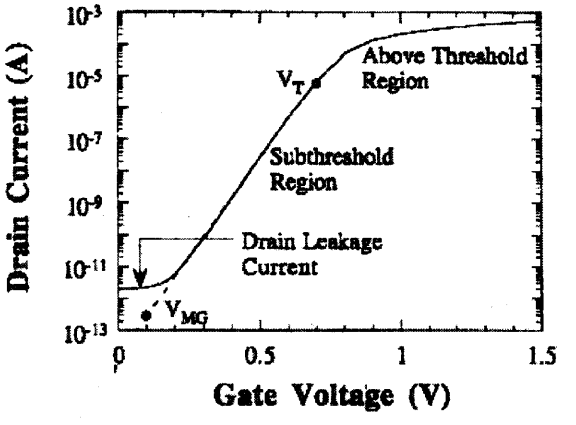


Figure 3.10 Subthreshold swing determination from subthreshold slope.
Source: [57]

3.3.6 Stress Measurement

High field stress in ultra thin gate oxides in MOS devices is known to degrade the oxide quality and eventually lead to oxide breakdown. Charge trapping in the oxide is used to monitor the degradation of the oxide. To these ends, oxide integrity is studied by time-dependent measurements by applying bias or injecting current and simultaneously measuring current and voltages at different nodes of MOS devices.

3.3.6.1 Constant Voltage Stress. Constant voltage stress (CVS) is implemented by applying positive or negative bias on gate while keeping substrate grounded as shown for MOS-capacitor. For MOSFETs or active-edge (ringed) MOS-capacitors, source/drain and the ring is also grounded as shown in the Figure 3.11. During stress,

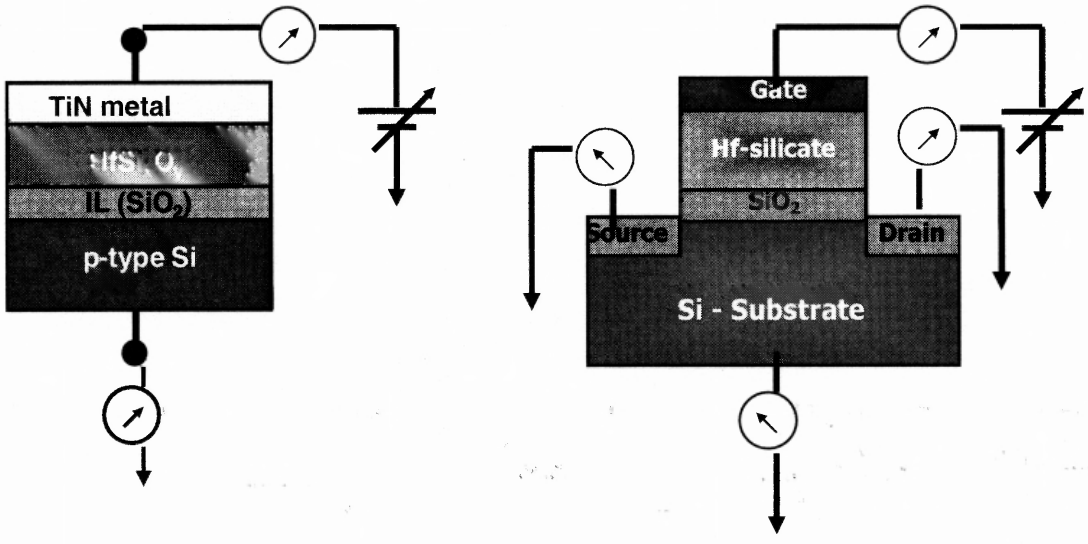


Figure 3.11 (a) MOS-Capacitor and **(b)** MOSFET set-up for constant voltage stress (CVS).

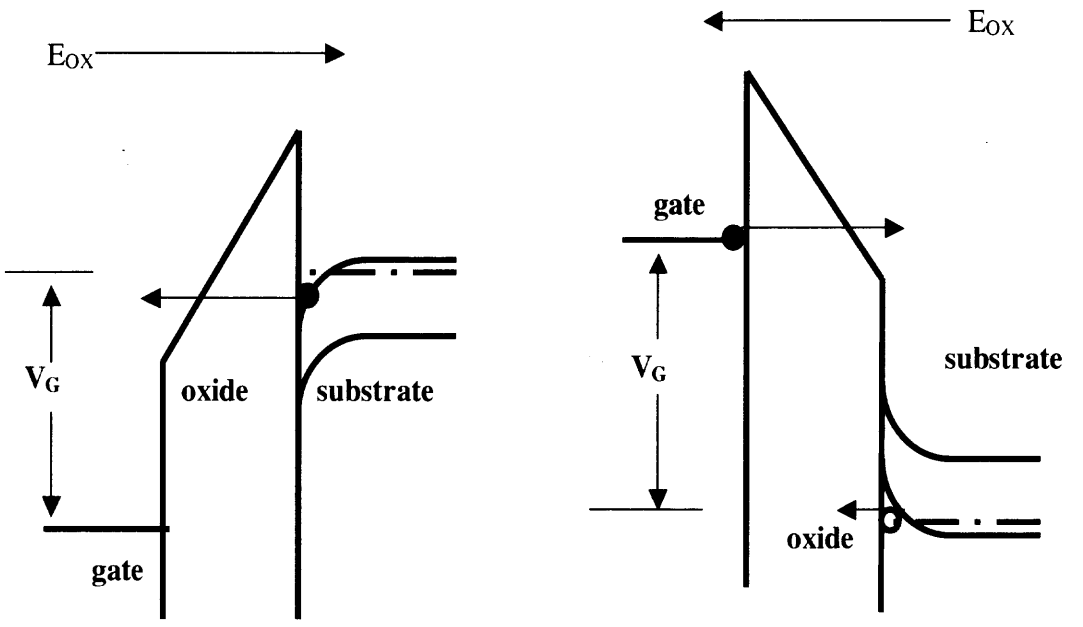


Figure 3.12 Band diagram for **(a)** substrate and **(b)** gate injection during CVS with positive and negative gate bias, respectively.

gate current is measured to estimate charge by integrating gate current over time as shown below [57]:

$$Q_{inj} = \int_{t_1}^{t_2} J_g(t)dt \tag{3.17}$$

Band diagrams for substrate and gate injection are shown in Figure 3.12. For gate stacks with metal gate electron injection from Si conduction band dominates during substrate injection. However, during gate injection not only electrons from gate, but also holes from the channel are injected. This is specifically pre-dominant in the case of MOSFETS. This is why, source and drain currents are also monitored during stress. $J_S + J_D$ can be integrated over time, as in (3.17) to estimate hole injection into the oxide.

To understand trapping at pre-existing and/or stress-induced defects gate current is monitored during stress (Figure 3.13). If J_g increases during stress time, hole trapping or/and elrectron trap generation takes place. If J_g does not change much, neither electron nor hole trapping dominantes. If J_g decreases, electron trapping is significant.

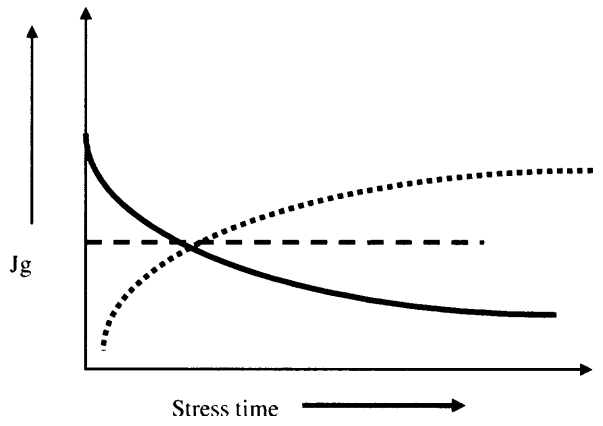


Figure 3.13 Gate current vs. time during CVS.

3.3.6.2 Substrate Hot Electron Stress. SHE stress was applied on n^+-ringed nMOS-C using the arrangement shown in Figure 3.14. SHE injection was realized by keeping the gate voltage (V_g) and substrate voltage (V_s) at low positive and high negative bias, respectively, while the ring voltage (V_{ring}) was kept grounded. V_{inj} is the bias applied on n^+-ring of the adjacent capacitor located around 10μm away, which forms a p/n^+ junction and acts as an electron injector. For low gate bias (V_g = 0.75V), the gate current during SHE injection increases by one order of magnitude compared to the cold carrier case [57]. As a result, during SHE stress, gate current comprises mostly of hot electrons injected into the oxide. In addition, the gate

current, that is hot electron injection, increases when injector bias is increased for a given V_s.

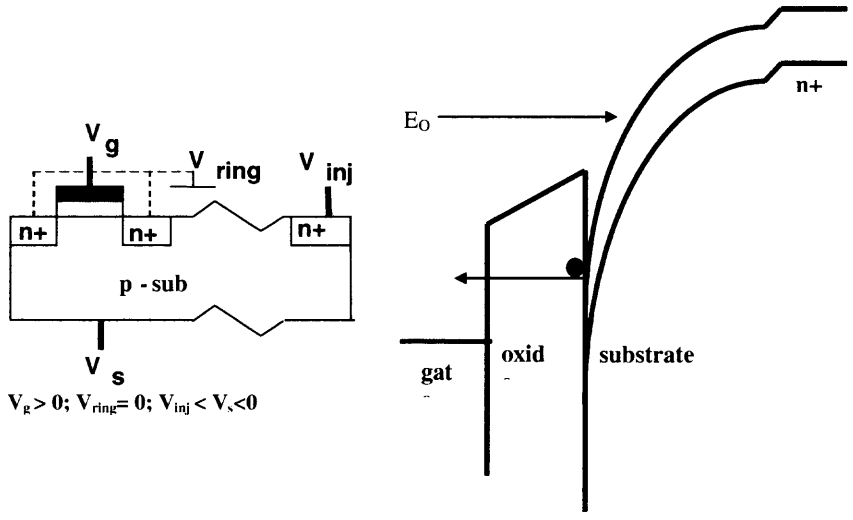


Figure 3.14 Arrangements for (a) SHE stress on n+-ringed nMOS-C and (b) band diagram under SHE stress.

3.3.6.3 Substrate Hot Hole Stress. To study the characteristics of the generated defects, SHH stress was applied using the arrangement shown in Figure 3.15. SHH injection was realized by keeping gate voltage (V_g) and substrate voltage (V_s) at low negative and high positive bias, respectively, while the ring voltage (V_{ring}) was kept grounded. V_{inj} is the bias applied on p^+-ring of the adjacent capacitor located around 20μm away, which forms a p^+/n junction and acts as a hole injector. Hole injection into the gate stack can be controlled independent of the gate bias by varying V_{inj} ($V_{inj} > V_s$) for a given V_s, while the energy of the incident carriers can be controlled by varying V_s. For low gate bias (V_g = –0.75V), the current during SHH injection

increases by one order of magnitude compared to the cold carrier case. This why, during SHH stress, gate current mostly comprises of hot holes injected into the oxide.

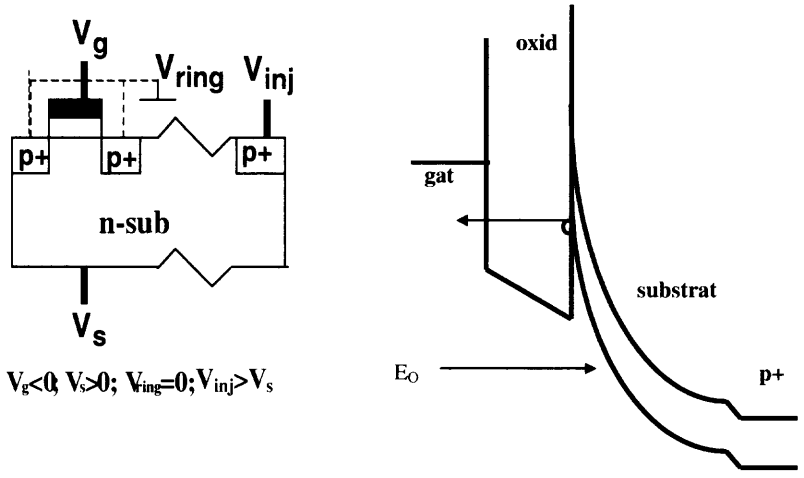


Figure 3.15 **(a)** Arrangements for SHH stress and **(b)** band diagram under SHH stress.

In addition, the gate current increases when injector bias is increased for a given V_S. These experimental results validate the setup for SHH injection.

3.3.7 Low Temperature Measurements

Low temperature characterization is useful in understanding the bulk oxide charges and interface traps behavior. It provides detailed description of the type of trapping taking place in the bulk oxide as well as at the interface. Furthermore, activation energy (E_t) of traps from the band edges can be calculated from flatband voltage shift (ΔV_{FB}) at different temperatures. A temperature range of 300°K to 130°K has been used for measurements. CTI Cryogenics M22 closed loop helium cooled refrigeration system and Palm Beach Cryophysics model 4075 temperature controller were used for low temperature measurements.

3.3.8 Time Zero Dielectric Breakdown (TZBD)

To understand TZBD characteristics, ramped voltage stress (RVS) is applied on the gate of MOS devices at a certain rate in both inversion and accumulation [57]. During the application of RVS, I_g is monitored. Gate current increases as voltage is ramped to high values. Hard breakdown occurs when the applied electric field breaks the bonds and bandgap collapse occurs. This results in a highly conductive path, which lets gate current to reach thermal run-away levels. Only then catastrophic thermal or thermodynamic breakdown occurs. Gate bias at which I_g increases sharply is defined as breakdown voltage, V_{BD}. Breakdown field of the dielectrics, E_{BD} can be found from V_{BD}. The quality of the dielectric can be understood from E_{BD}. This is why it is extensively used to monitor the quality of oxide during different phases of fabrication.

3.3.9 Time Dependent Dielectric Breakdown (TDDB)

In order to comprehensively understand the reliability of the gate stacks, TDDB is studied by applying either constant voltage or current stress [12]. During CVS and CCS, I_g–t and V_g–t are monitored. Soft breakdown (SBD) occurs as a temporary percolating path is formed across cathode and anode due to stress-induced defects. This results in a small but sharp increase of gate current with respect to stress time. As percolating path becomes more stable due to defect generation, conductivity across cathode and anode increases. This results in noisy but gradual increase in gate current, which is known as progressive breakdown (PBD). When a stable conductive path is formed, hard breakdown (HBD) occurs. As stress is continued further,

thermal runaway current gives rise to catastrophic breakdown. For sub-2 nm oxides, these breakdown phenomena are widely observed.

Time-to-breakdown (T_{BD}) is defined as the moment when HBD occurs. For CVS, charge-to-breakdown (Q_{BD}) is defined as area under I-t plot till T_{BD}. For CCS, it is defined as the product of current stress level and stress time. Slopes of weibull plots of T_{BD} and Q_{BD} for different areas under different stress levels are used to understand the quality of oxide as well as the uniformity in distribution. Moreover, 63% failure values of T_{BD}, found from weibull plots, are plotted with respect to stress bias to project 10-year life-time and to optimize the operating voltage.

3.4 Measurement Automation

In order to have fast and accurate measurements from the experiments designed in the

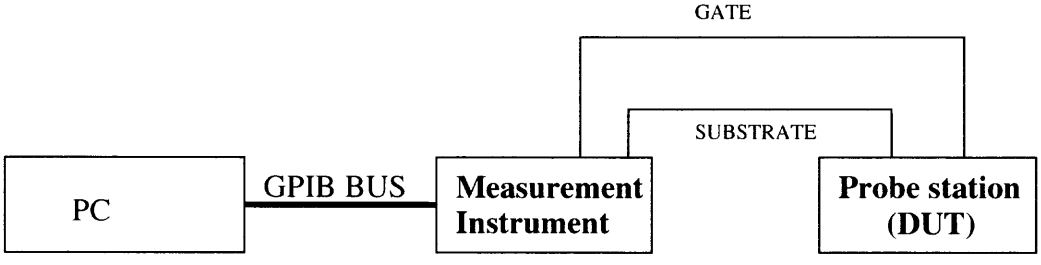


Figure 3.16 Basic arrangement for electrical measurement automation of a simple two-terminal device, e.g. MOS-Capacitor.

course of this research, the basic measurements like C-V/G-V, I-V, Id-Vg, CVS, SHE, SHH etc were automated. Measurement automation involves remotely programming the measurement instrument for a particular set of measurements, the parameters of which are provided by the user. To this end, GPIB (general purpose

instrumentation bus) protocol is widely used. For example to take I-V measurement for a MOS-C, the user sets the start and end gate biases along with inter step voltages. It is also possible to provide inter-step delay, how the data will be displayed in the instrument and which file in PC measured data will be stored. All these data can be supplied via a man-machine interface of the resident program like LabVIEW at the PC (personal computer). LabVIEW based automated software converts the user-defined data to commands understood by instrument and evokes GPIB commands to write these command data to the instrument. After successful transmission of command data to the instrument, it triggers the instrument to run the measurement. After the completion of measurement, automation software stores a copy of data at the instrument. It opens the file again and evokes it to transmit back to PC and store them in a user- defined file. Figure 3.16 shows the basic building blocks. Algorithms and instruments used for measurement automation of simple experiments like I-V/C-CV/G-V/CVS/I_d-V_g are described in the following sections.

3.4.1 I-V Measurements Automation

For I-V measurements HP4156B semiconductor parameter analyzer, Cascade Microtech probe station (for room temperature measurements) and Micrmanipulator hot stages (for elevated temperatures) are used. Man machine interface (MMI) of I-V automation system is shown in Figure 3.17. This system can be used for gate leakage from measurements of both isolated edge and active-edge MOS capacitors. It can be noticed from MMI that user can apply bias on both gate and ring, define start and end gate voltages along with number of steps. Mode of digital integration of raw data can

also be selected as par requirement. Inter-step voltage is evenly distributed within the specified range of gate bias. User can obtain both gate and substrate currents from I-V measurements and save them in a user-defined file in PC where corresponding gate voltage and gate and/or substrate currents stored in array forms, which is ready for further data analysis using commercial spreadsheet software. Moreover, obtained I-V results are shown in graphical form for better user comprehension. The algorithm of I-V automation is given in Figure 3.18 using flow chart.

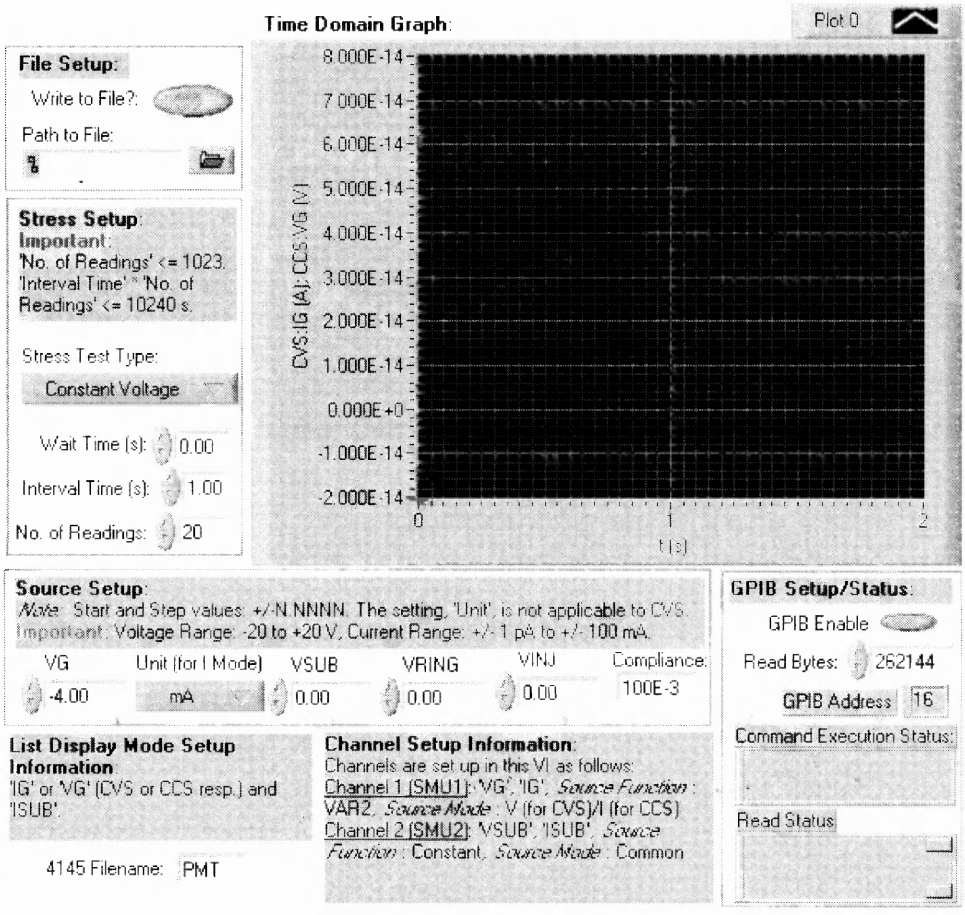


Figure 3.17 View of the man machine interface (MMI) of I-V measurement automation system.

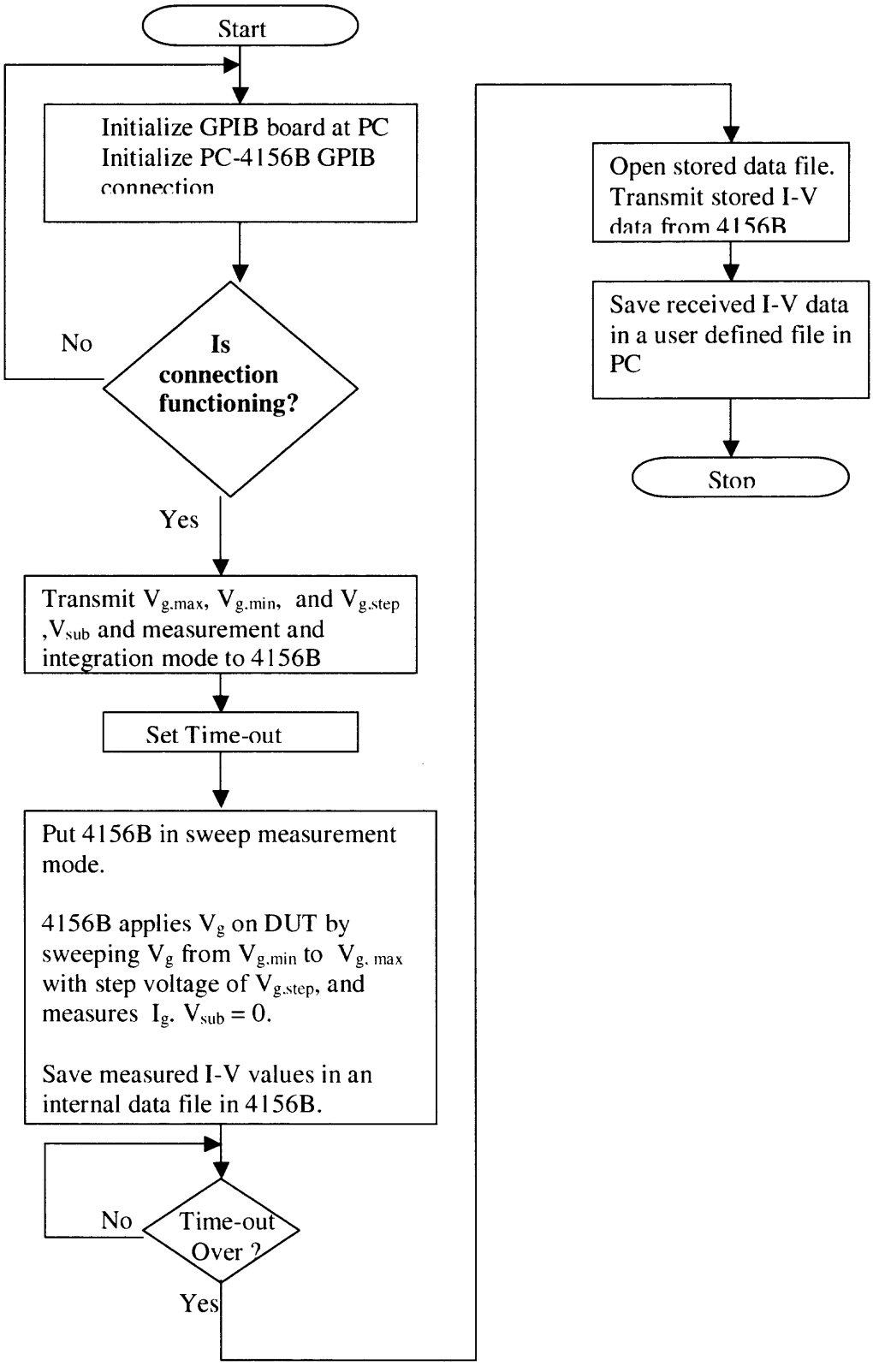


Figure 3.18 Flow chart of I-V automation algorithm.

3.4.2 C-V and G-V Measurements Automation

For parallel capacitance and conductance measurements of MOS capacitors at different frequencies in 1 MHz-20 Hz range, HP4284A LCR meter is used. MMI is shown in Figure 3.19. User can define dc sweep level from positive to negative voltages and vice versa. Inter-step voltages can also be defined along with inter-step delay. Frequency can be set in 1MHz-20Hz range for ac signals of 10 mV peak value. Measured parallel capacitance and conductance values are saved in arrays of C-V and G-V format in user-defined file in PC. Measured C-V is also plotted on the MMI widow. The algorithm for C-V/G-V measurement automation is shown in Figure 3.20.

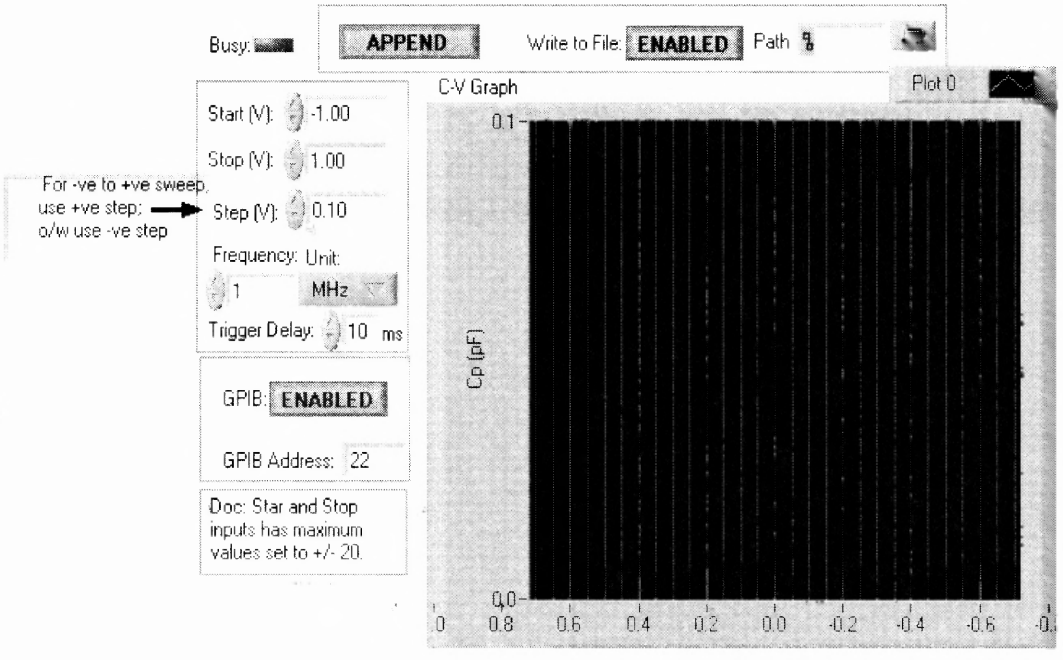


Figure 3.19 View of the man machine interface (MMI) of C-V and G-V measurement automation system.

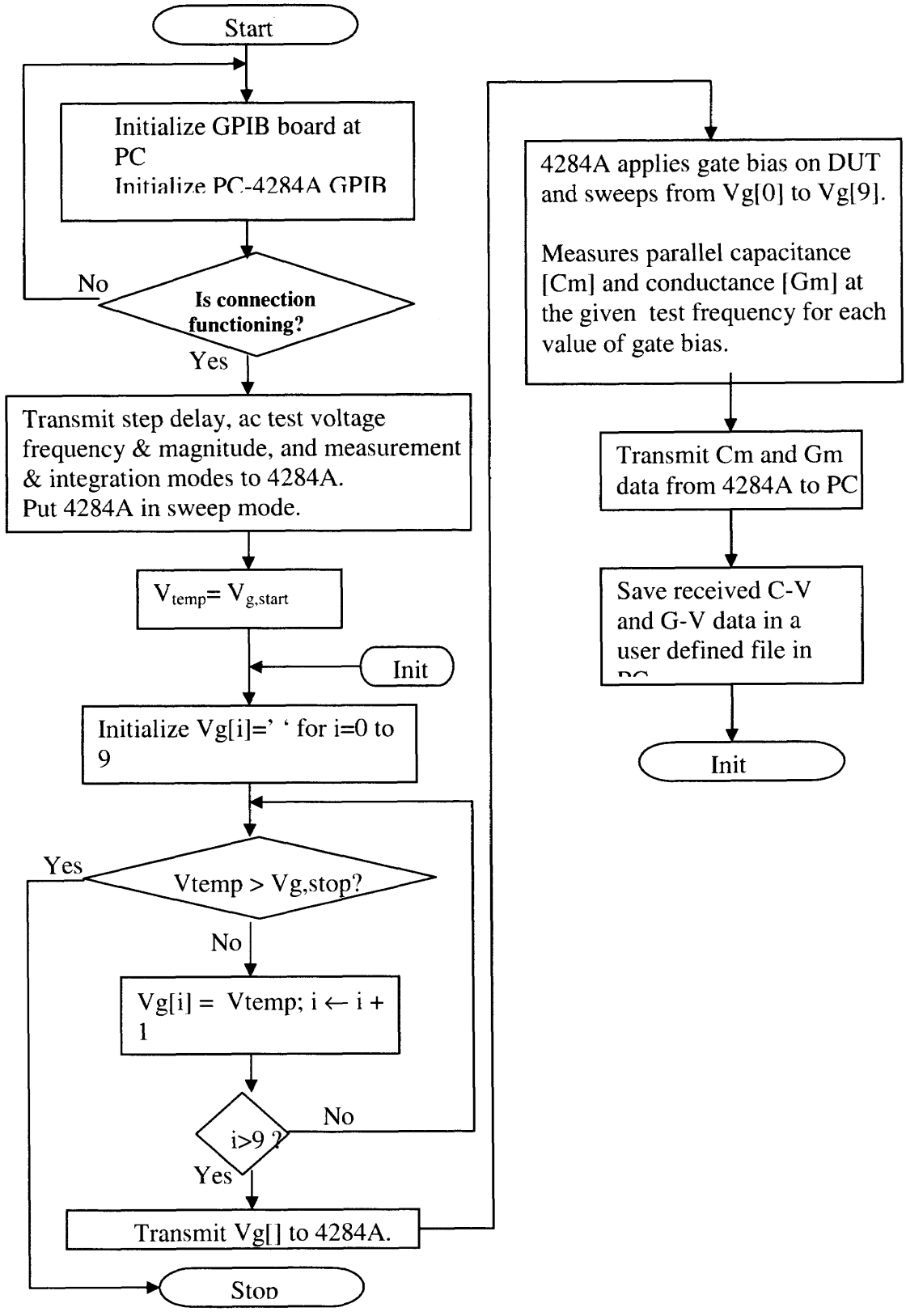


Figure 3.20 Flow chart of C-V/G-V automation algorithm.

3.4.3 CVS Measurements Automation

Constant voltage stress (CVS), applied on MOS capacitors, is automated using HP4156B semiconductor parameter analyzer. User-defined stress bias is provided for a given period of time. Number of time steps and delay in each step are provided. Gate and substrate current during stress is measured and saved in user-defined file in PC as shown in MMI (Figure 3. 21). I-t is plotted after stress. Same program can be used for constant current stress by changing "stress test type" option on MMI window.

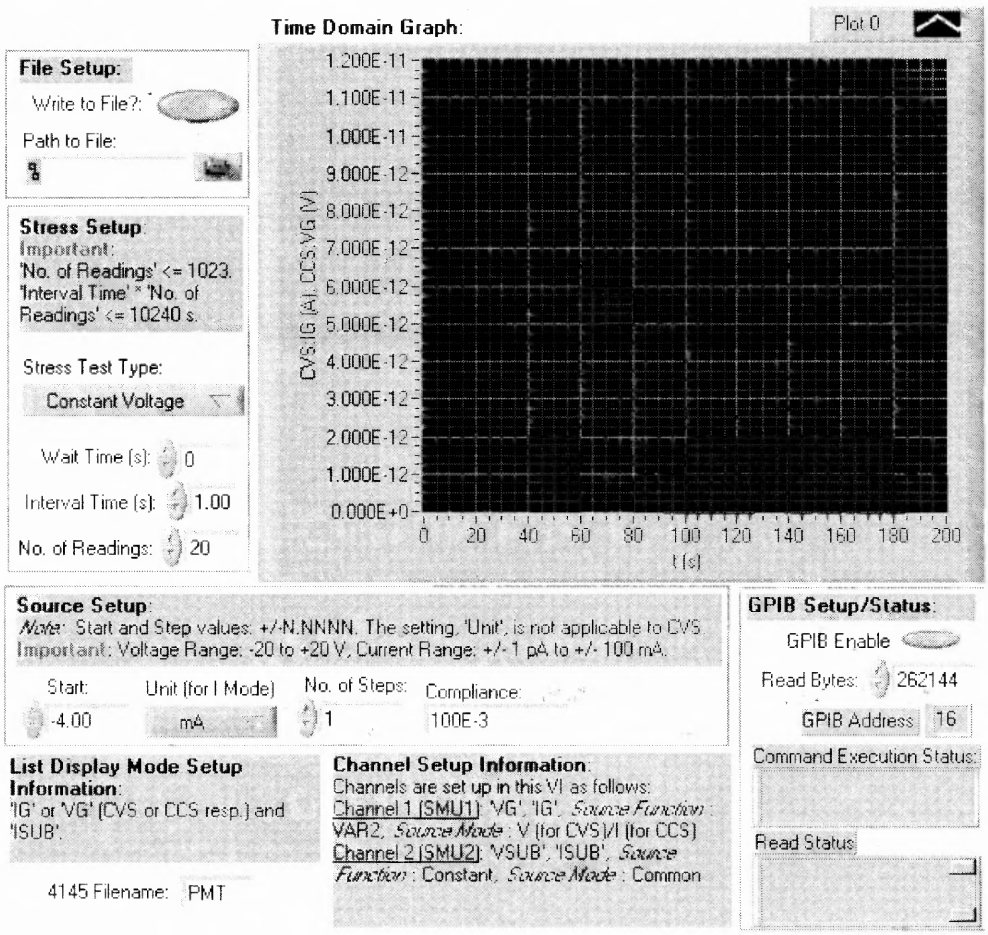


Figure 3.21 View of the MMI of CVS automation system.

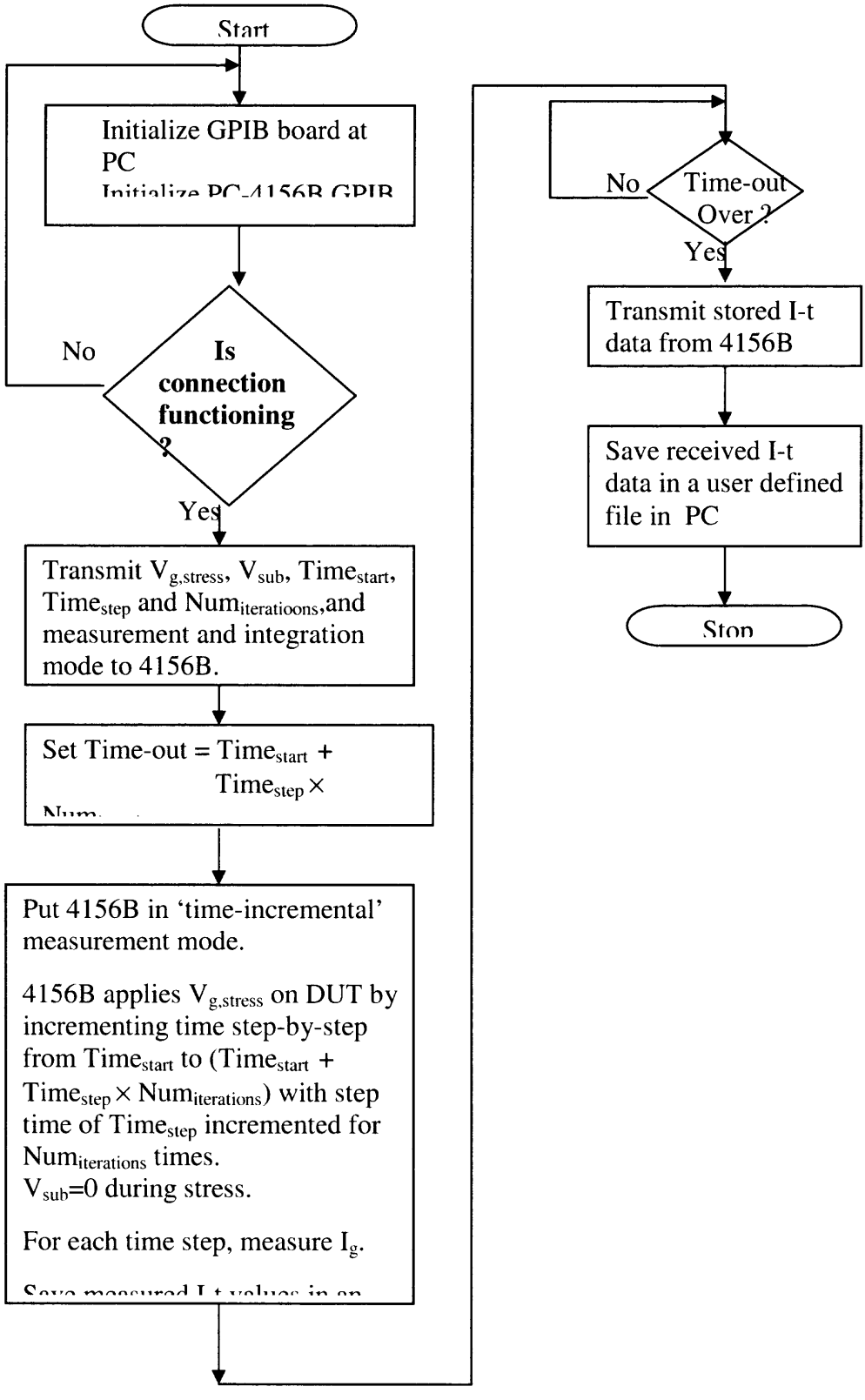


Figure 3.22 Flow chart of CVS automation algorithm.

3.4.4 I_d-V_g Measurement Automation

I_d-V_g measurement automation of MOSFETs is implemented using HP4156B semiconductor parameter analyzer. By applying V_{GS}=V_{DS}, $I_{D,sat}$ is measured w.r.t. of V_g in the given range. User defined start and stop values are transmitted to the instrument. After taking the measurement I_d-V_g data is displayed at MMI window as shown in Figure 3.23. During I_d-V_g measurement, gate leakage is also measured and saved in user defined file.

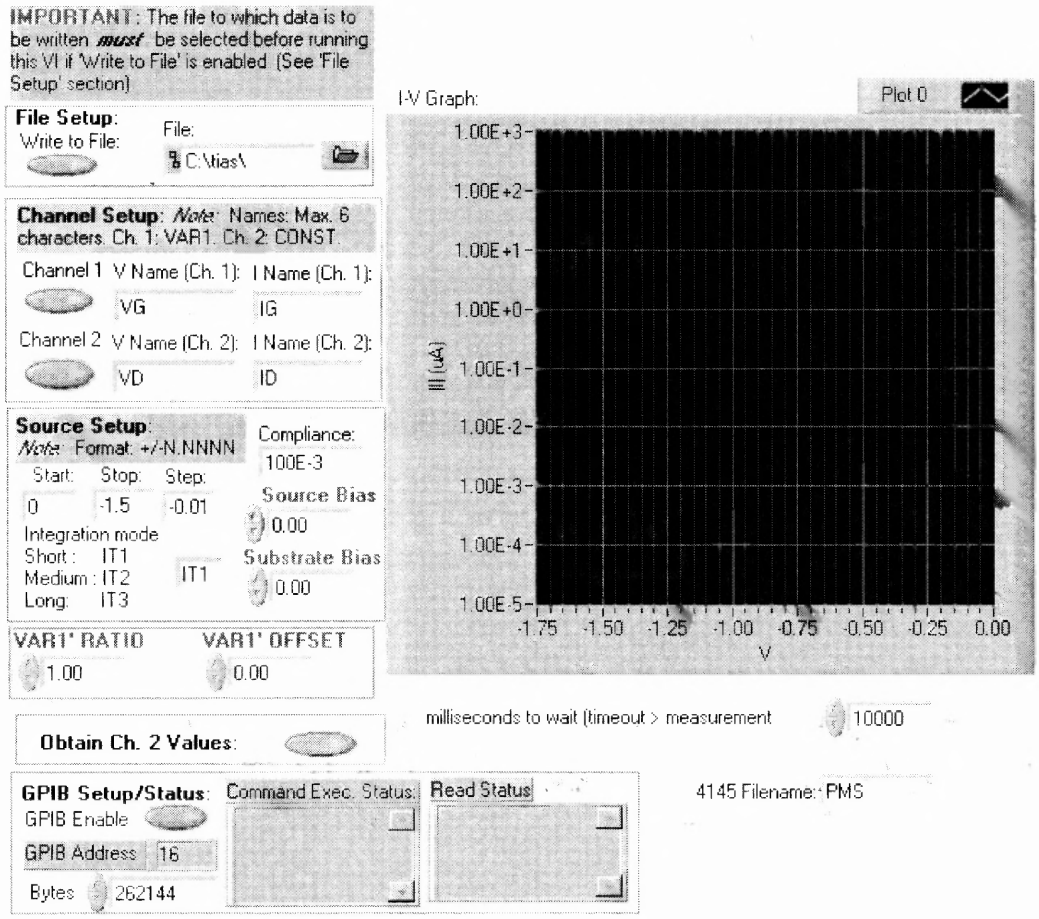


Figure 3.23 View of the MMI of I_d-V_g measurement automation system.

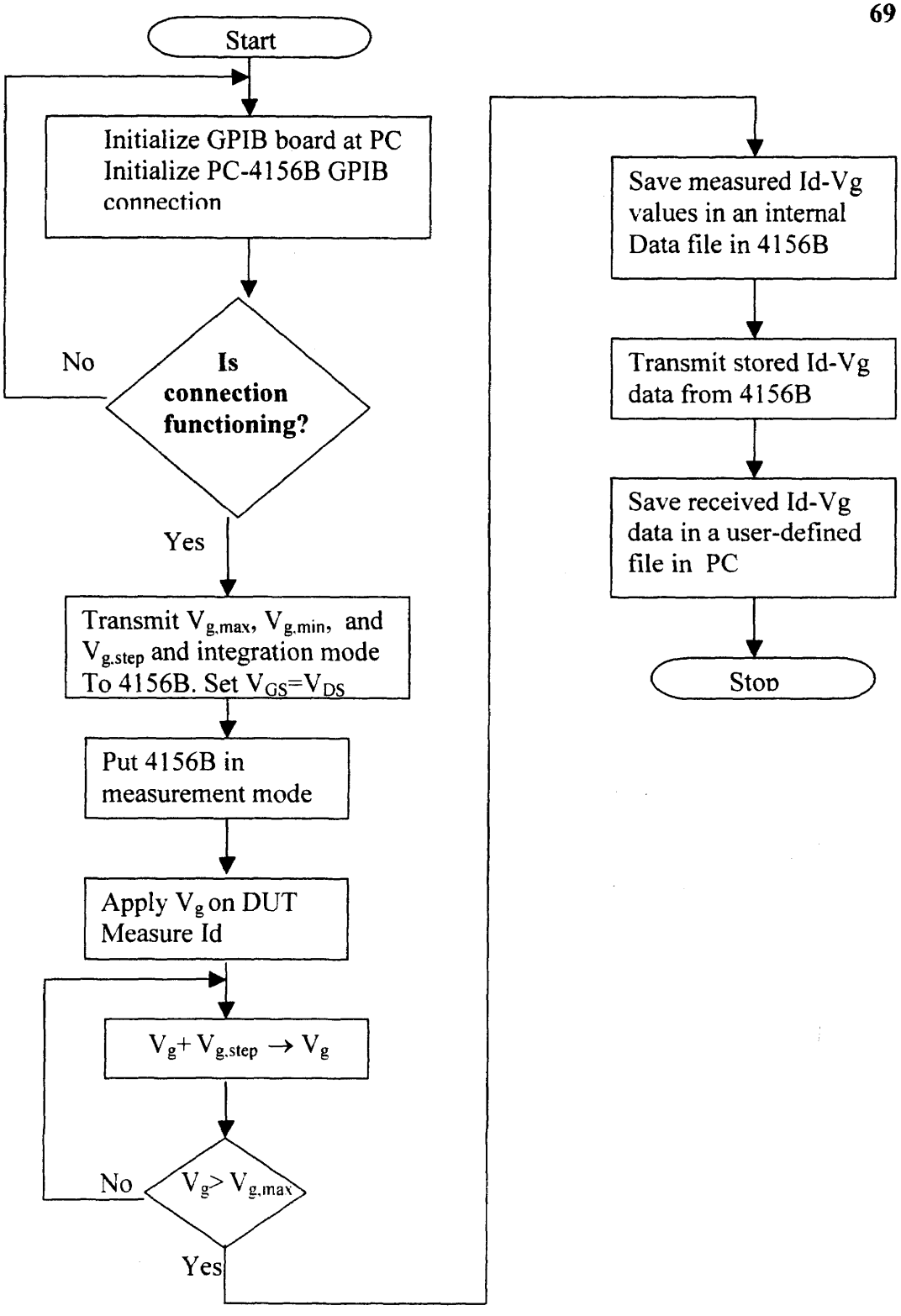


Figure 3.24 Flow chart of I_d-V_g automation algorithm.

3.4.5 SHC Measurements Automation

Substrate hot carrier (SHC) stress is applied on n+-/p+-ringed nMOS-C and pMOS-C respectively using HP4156B semiconductor parameter analyzer. Discrimination between hot electron and hot hole injection can be made by modifying gate, ring and injection biases in the same program as shown in Figure 3.25. The rest is same as CVS.

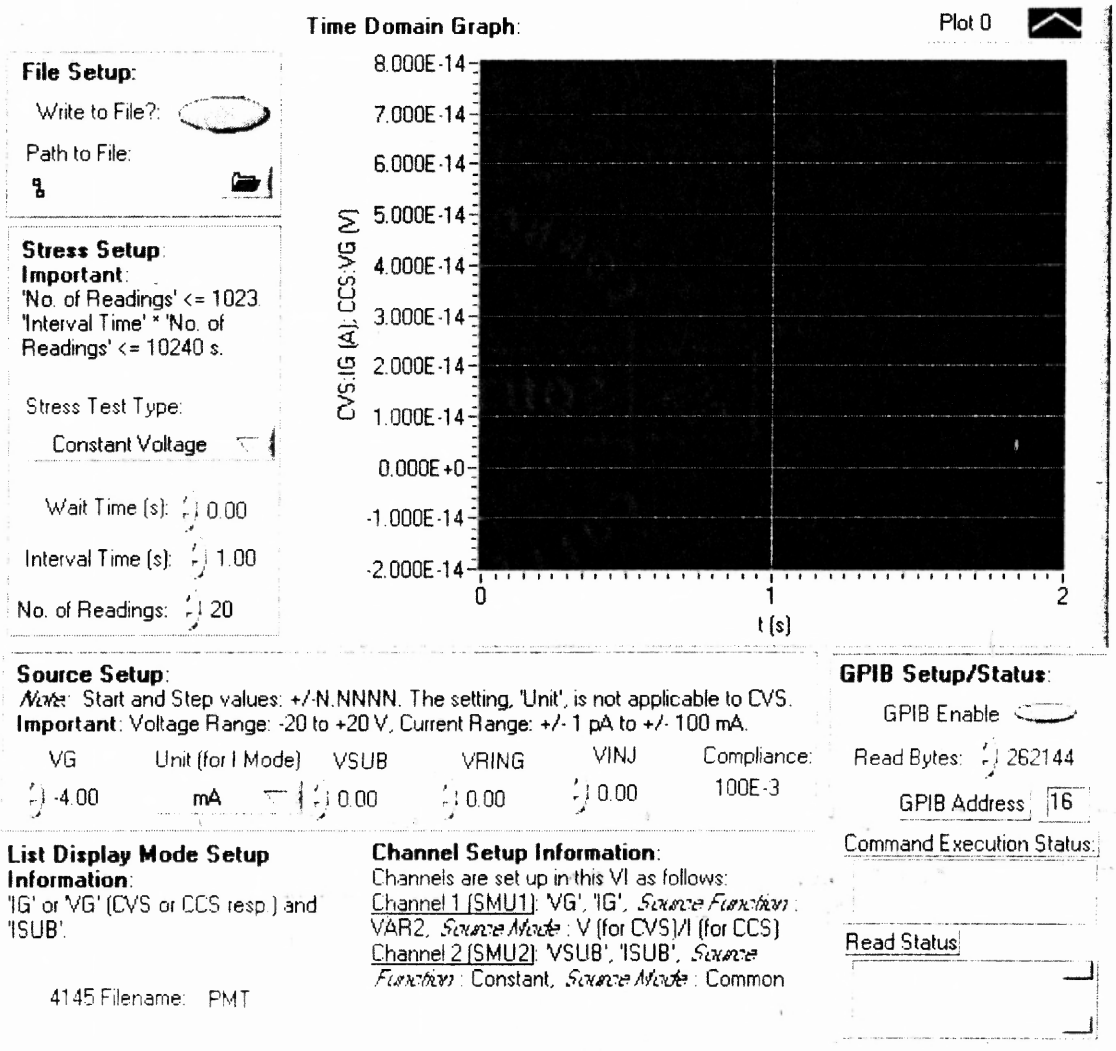


Figure 3.25 View of the MMI of SHC stress automation system.

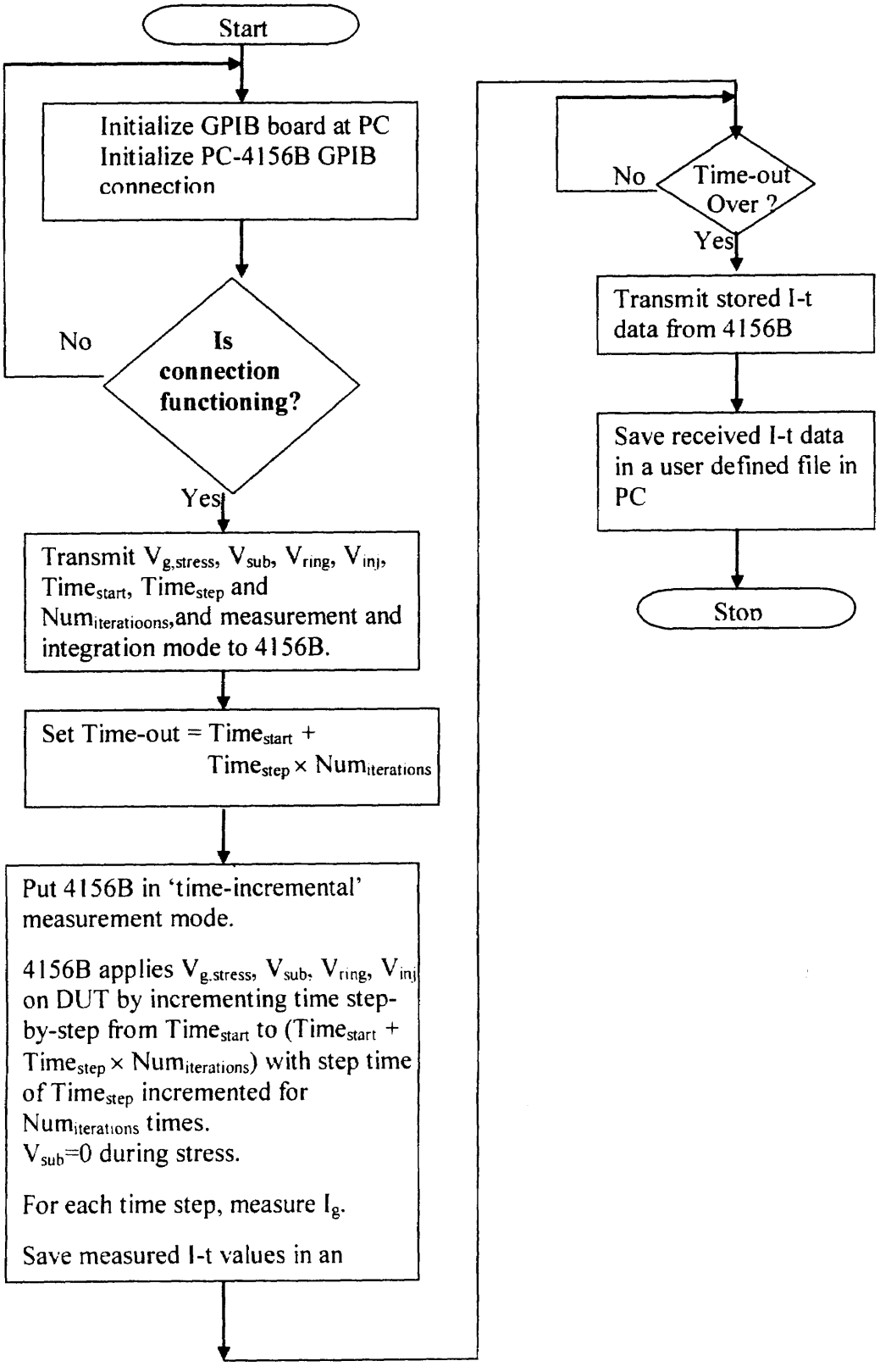


Figure 3.26 Flow chart of SHC stress automation algorithm.

3.4.6 Transistor Stress Measurement Automation

Automation program is modified to accommodate applying CVS on MOSFETS, which is done using HP4156B semiconductor parameter analyzer. Gate, drain, source and substrate bias can be gin individually for CVS as shown in Figure 3.27. The rest is same as CVS applied on MOS capacitors.

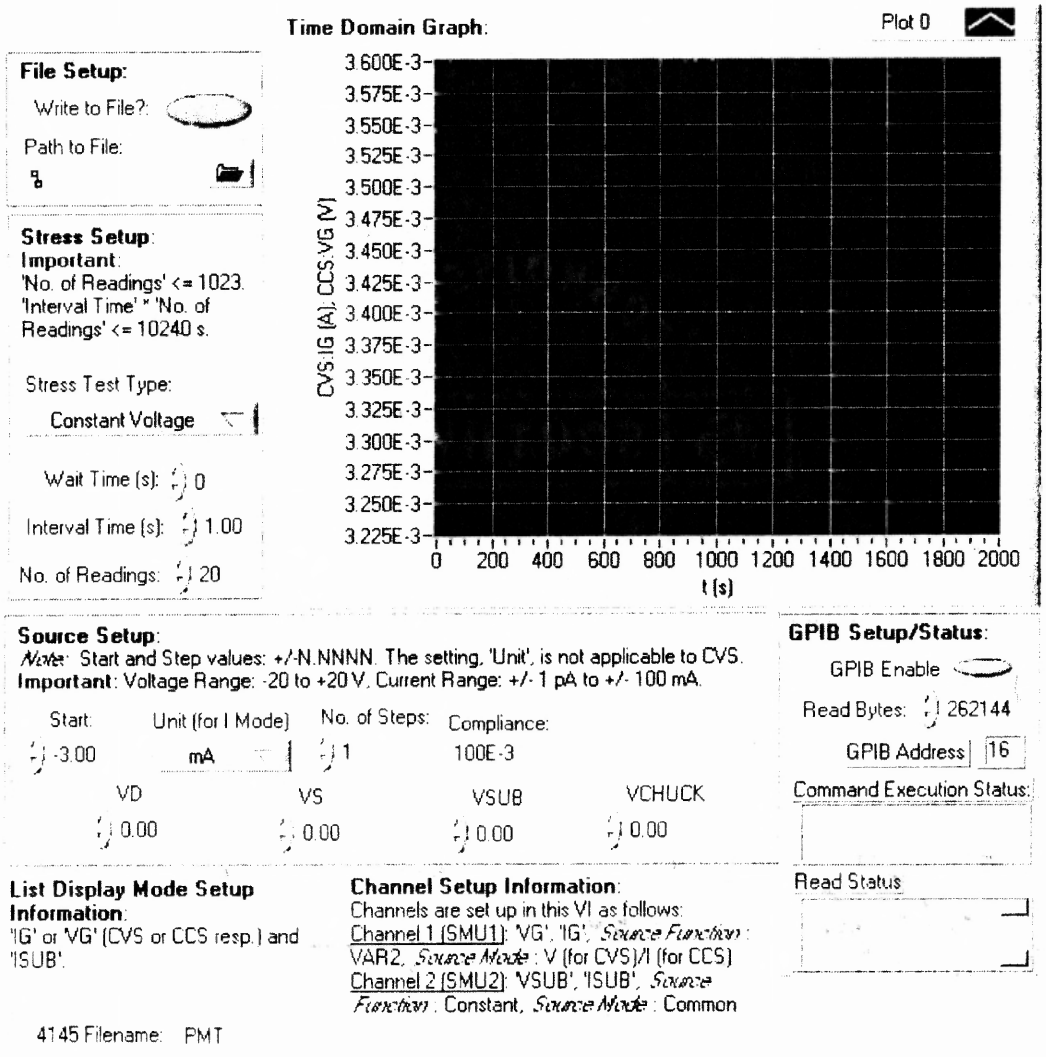


Figure 3.27 View of the MMI of CVS automation system for transistors.

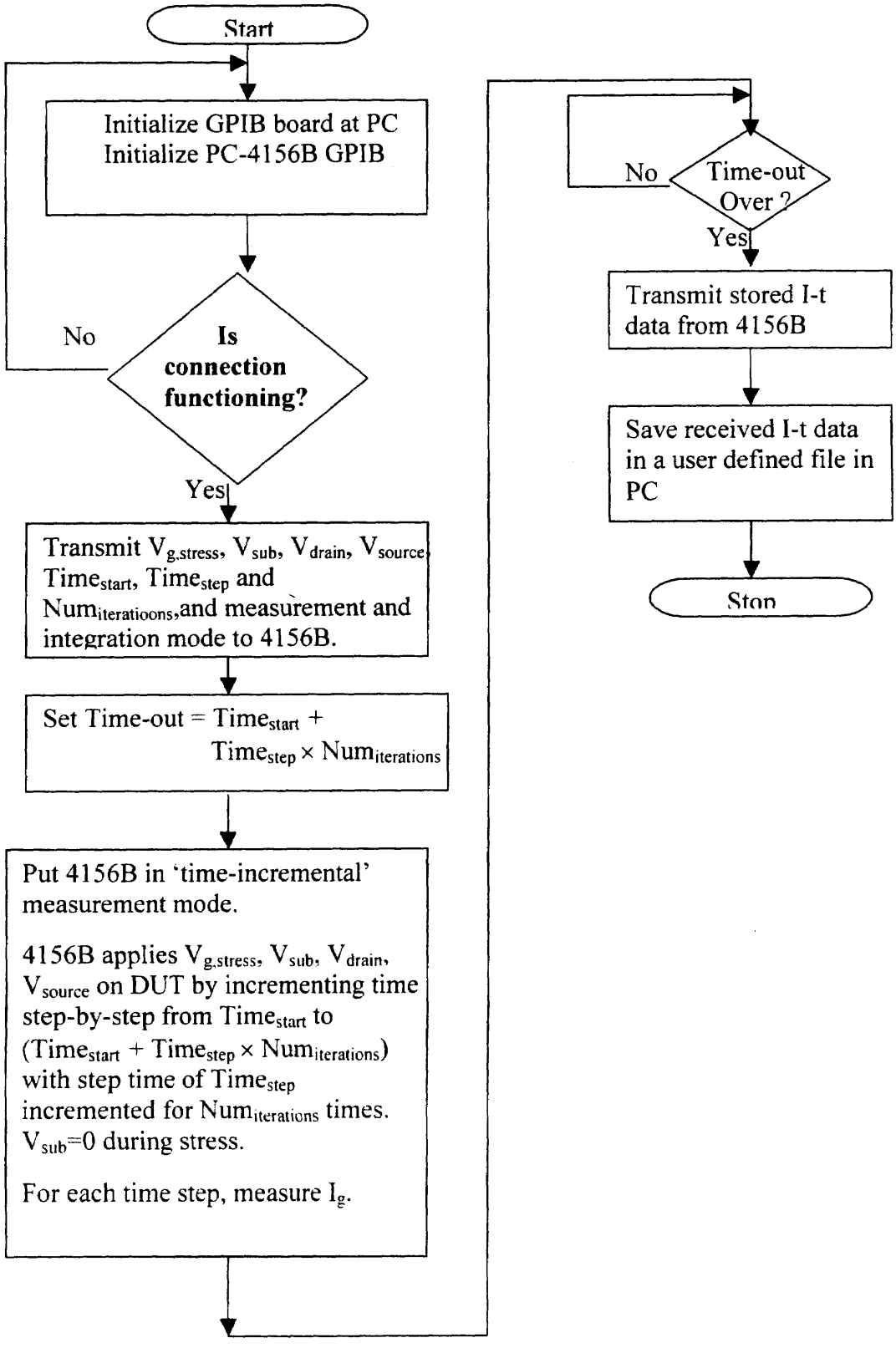


Figure 3.28 Flow chart of CVS for transistors automation algorithm.

3.5 Summary

Fabrication of TiN/$HfSi_xO_y$ based devices is discussed in this chapter. Basic principles of the fundamental measurement techniques like I-V, C-V, G-V, CVS etc. are elaborately described. Automation of simple and complex measurements is implemented on LabVIEW platform. Man-machine interfaces and automation algorithms are comprehensively analyzed.

CHAPTER 4

EXPERIMENTAL OBSERVATION OF DEFECT LEVELS IN TiN/$HfSi_xO_y$ BASED GATE STACKS

4.1 Introduction

In order to observe the electrically active ionic defect levels within TiN/Hf-silicate based gate stacks, a number of studies were performed. It is obvious from calculations that the defect energy states, responsible for electron and hole trapping, lie at the various levels within the bulk high-κ bandgap. In the context of MOS band diagram, they are resonant with the injecting sides (metal gate and Si band edges) under different band bending conditions. Electrical experiments need to be carefully designed to find the defect levels.

Observation of ΔV_{FB}, leakage etc. with respect to temperature is the key to finding the activation energies of the defects. Techniques like low temperature C-V/G-V measurements at different frequencies, leakage measurements at the elevated temperatures, and flatband voltage measurement during temperature and time dependent carrier de-trapping from stress-induced defects were employed. Moreover, observed defect levels were compared with the calculated values to relate to the physical origins of the defects.

4.2 Characteristics of Detrapping from Deep Defects

In order to understand the effects of both the spatial location and the energy level of the deep bulk traps, as shown in Figure 4.1, on detrapping time to the substrate, the following modified Shockley-Read-Hall (SRH) model of carrier emission rate, $e_{n/p}$ can be used [58]:

$$e_{n/p} \propto \exp(-E_a / KT) \times T_{n/p} \tag{4.1}$$

$$T_{n/p} \propto \exp(-\Phi_B \times d_T) \tag{4.2}$$

Here, E_a is the activation energy of the deep bulk high-κ trap with energy level lying within Si bandgap range and is measured from Si band edge, K is Botzman's constant, $T_{n/p}$ is the tunneling transparency, Φ_B is the barrier height seen by the trapped carriers and d_T is the distance of the trap location from the IL/high-κ interface provided IL is less than 2nm to accommodate direct tunneling to/from bulk high-κ traps.

It is obvious that detrapping time, which is the inverse of the emission rate, increases with E_a and d_T under 'no-bias' condition at a fixed temperature for the deep defects near the substrate. But, for the same defects detrapping time decreases with increase in temperature under 'no-bias' condition. It is further understood that for an electron trap level above E_c^{Si} or a hole trap level below E_v^{Si} in the bulk high-κ, detrapping time primarily depends on tunneling transparency. Detrapping time from these traps is considerably fast even under 'no-bias' condition especially for the traps located near the substrate and is independent of temperature. However, thermally and field activated discharging from them appears as an additional but a competing

detrapping process only at comparatively high temperature and bias conditions [39]. Simulation with HfO_2 based gate stacks with ~1nm of IL shows that for levels 0.5eV above E_c^{Si}, i.e., shallow traps, de-trapping time to the substrate approaches ~10^{-10} sec for traps near the substrate under 'no-bias' condition at room temperature [59]-[77]. For levels 0.05 eV and 0.5 eV below E_c^{Si}, i.e., deep traps, it increases to ~10^0 and 10^7 sec, respectively. Experimental results reported by [39], [58] conform to these observations. This is why, detrapping time at room and elevated temperature under 'no bias' condition can be probed to understand whether trap levels lie within Si bandgap range, especially for those located near the substrate.

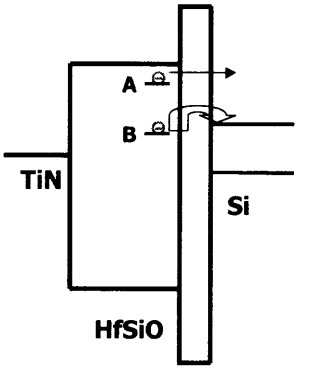


Figure 4.1 Detrapping characteristics from shallow (A) and deep (B) traps under idealized 'no bias' condition for $TiN/HfSi_xO_y$ based gate stacks.

4.3 Defect Levels from Low Temperature Measurements

The electrically active ionic defects are found to be mostly responsible for the trapping within the bulk high-κ oxides. For Hf-based gate stacks with the thin IL (< 2 nm), simulations show that it is possible to quickly (~10s of ms) charge and discharge deep electron traps by applying moderately high positive and negative bias (~ ±2 V) [1]. To characterize the defects with the deep levels, specially lying within Si

bandgap range, C-V measurement at low temperatures can be used as an effective method. It is possible to fill the deep bulk traps with the majority carriers injected from the substrate and subsequently empty them if the gate bias (V_g) sweep levels from the accumulation to inversion regimes are carefully selected [59]. The temperature dependent response of the majority carrier traps leaves its signature in ΔV_{FB} and, thus, enables the defect characterization. In this work, the focus is on studying the deep electron and hole traps. Essentially, C-V measurements are taken for pMOS-C and nMOS-C with TiN/$HfSi_xO_y$ based gate stacks at low temperatures within 275K-78K and 275K-100K ranges, respectively.

4.3.1 Low Temperature C-V and G-V for pMOS-C

C-V measurements in 275-78K temperature range are plotted in Figure 4.2(a) for pMOS-C. Shift of C-V to the right with decreasing temperature indicates that electron trapping had occurred. 10 KHz G-V measurements in 275-78K range are shown in Figure 4.2 (b). Horizontal shift of the peak of the G-V plots to the right also confirms that electron trapping had occurred as the temperature was lowered [59]. It is obvious from Figure 4.2(b) that the change in trapping at the interface states is negligible, as the magnitude of the peak does not change with temperature. This affirms that electron trapping took place at the bulk high-κ.

As V_g is swept from the accumulation to depletion regimes the deep bulk traps, with the energy level lying below Fermi level, become filled with electrons injected from the substrate. As V_g is swept from the depletion to inversion regimes, the bulk trap energy levels move above Fermi level and these traps tend to become

empty as a result of the detrapping of electrons to Si conduction band, E_c^{Si}. However, this detrapping process is thermally activated. As a consequence, the detrapping of

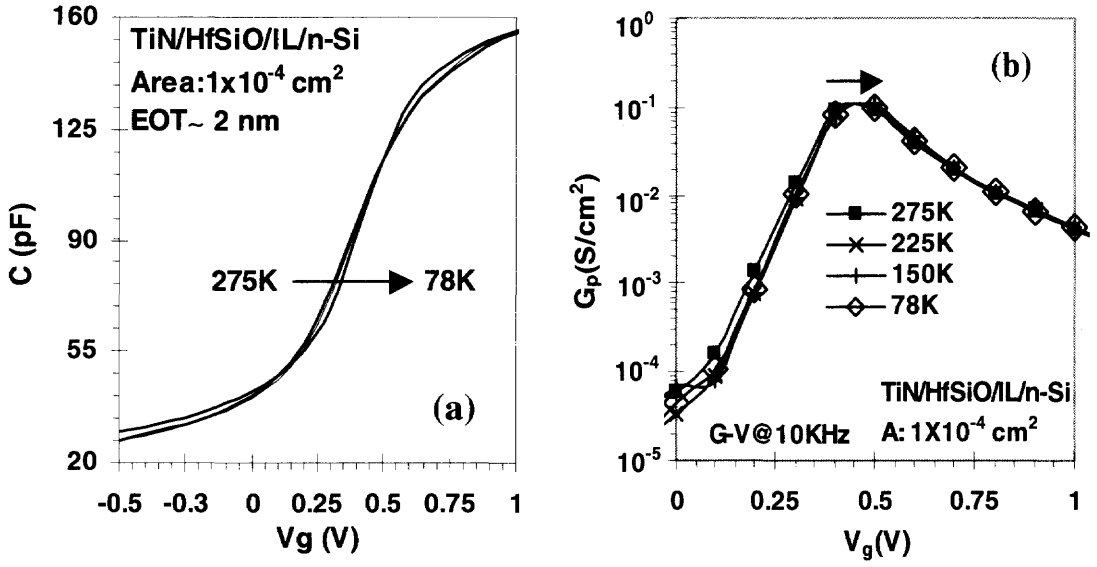


Figure 4.2 (**a**) 1 MHz C-V plots, and (**b**) 10 KHz G-V plots in 275 K-78 K temperature range for pMOS-C.

electrons decreases as temperature is decreased. As V_g is swept from the depletion to inversion regimes, the bulk trap energy levels move above Fermi level and these traps tend to become empty as a result of the detrapping of electrons to Si conduction band, E_c^{Si}. However, this detrapping process is thermally activated. Thus, the detrapping of electrons decreases as temperature is lowered, which results in the increase in ΔV_{FB}, determined after the temperature and quantum mechanical corrections, with low temperatures as observed in Figure 4.3. This is why the activation energies of these deep defects, responsible for electron trapping, can be determined from Arrhenius plots as shown in the inset of Figure 4.3. The energy levels of these deep

defects, consequently, can be determined with respect to the E_c^{Si} from their activation energies. The activation energies, E_a, of these deep defects were found to be 122meV and 6meV.

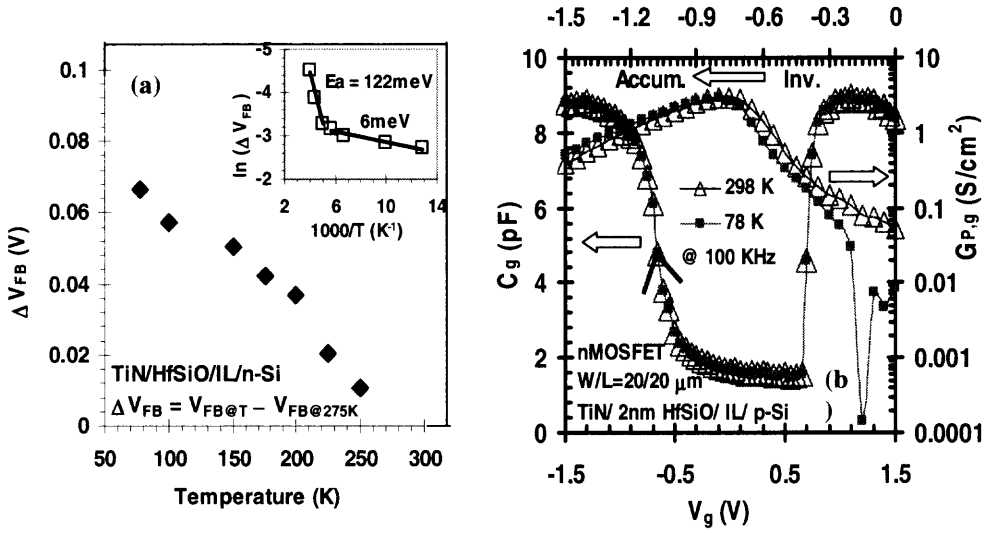


Figure 4.3 Flatband voltage shift (ΔV_{FB}) vs. temperature for pMOS-C. (**Inset**) Arrhenius plot of ΔV_{FB}. (**b**) 100 KHz C-V and G-V for 2 nm Hf-silicate/IL at 298 K and 78 K for nMOSFET.

The objective was to inject electrons into the gate stack and observe its effect on ΔV_{FB}. Voltage across gate stack, $V_{OX} = V_{H\text{-}K} + V_{IL}$. , where, $V_{H\text{-}K}$ and V_{IL} are the potential drops at the high-κ and interfacial layer, respectively. In this case, EOT is ~2 nm and physical thickness of Hf-silicate and interfacial layers are 3.5 and 1 nm, respectively. Consequently, $V_{H\text{-}K} / V_{IL} \approx 1$. Furthermore, $V_{H\text{-}K} = V_{IL} = V_{OX} / 2 = (V_g - V_{FB} - \Psi_s) / 2$, where Ψ_s is the surface potential. For p-MOS-C, $V_{FB} \approx 0.4$ V, and for $V_g = +1.75$ V, $V_{IL} \approx 0.7$ V. The offset between Hf-silicate and Si conduction bands ≈ 1.5 eV. As far as band bending conditions during sweep are concerned, shallow electron trap energy levels lying within ~ 0.1 eV of Hf-silicate conduction

band are not resonant with Si conduction band, which prevents them from being populated [60]. For this reason, the observed activation energies do not correspond to them.

To understand whether the deep defects, responsible for electron trapping, are located within the IL or high-κ layer of TiN/ 3.5 nm $HfSi_xO_y$/ 1 nm IL gate stacks, a new sample with a different high-κ layer and the same IL needs to be used. To this end, 100 KHz C-V and G-V measurements of nMOSFETs with TiN/2nm $HfSi_xO_y$ /1 nm IL gate stack were taken at room and low (78 K) temperatures. To initially inject electrons into the gate stack and observe its effect on ΔV_{FB}, V_g was swept from +1.5 V to –1.5V, i.e., from the inversion to the accumulation regime as shown in Figure 4.3.(b). $V_{IL} \approx 0.8$ V for $V_g = +1.5$ V, which allows the deep levels to be filled with electrons during sweep. It may be noted that the minority carrier (electrons) shortage during the substrate injection was avoided as source/drain were grounded. C-V measurements, however, showed a negligible change in V_{FB} as temperature was lowered. Moreover, the peak value of G-V showed no change as temperature was lowered. Trapping at the interface states was also negligible. Very fast de-trapping from the bulk defects in 2 nm high-κ layers due to the very short tunneling distances (< 2 nm) were reported [60]. If electron trapping in IL had dominated, ΔV_{FB} would have been significantly high positive value (see Figure 1) irrespective of the high-κ layer thickness. As this is not the case, it may be argued that electron trapping mostly occurred within the bulk high-κ layer in 3.5 nm Hf-silicate/ 1 nm IL gate stack.

4.3.2 Low Temperature C-V and G-V for nMOS-C

For nMOS-C, the C-V plots in Figure 4.4(a) shift to the left as the temperature is varied from 275K to 100K. This indicates that hole trapping dominates. Arrhenius plot of the corrected $-\Delta V_{FB}$ in the inset of Figure 4.4(a) shows a dominant defect level with activation energy of 20 meV. Figure 4.4(b) shows that peak of 10KHz G-V plots shifts to the left as hole trapping took place, whereas the magnitude of the peak does not change as the trapping predominantly occurred within the bulk. The arguments, which were put forth earlier to show that low temperature induced shift in flatband voltage is due to trapping at the deep defect levels, are also valid in this case. As a result, the deep defect levels, which are physically located within the bulk high-κ and are responsible for hole trapping, lies within Si bandgap in the gate stacks. Moreover, this defect level can be determined with respect to Si valence band from the observed activation energy.

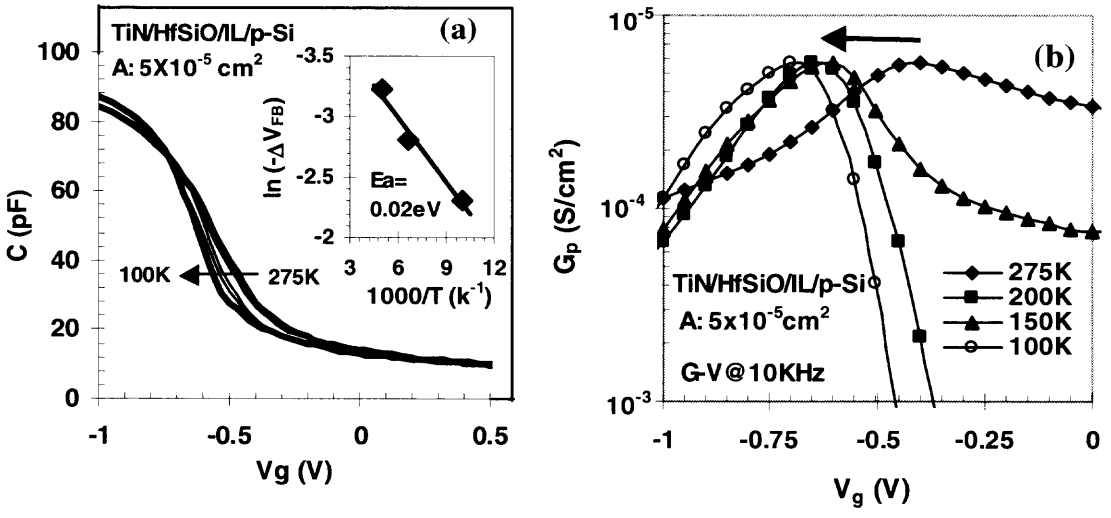


Figure 4.4 **(a)** 1MHz C-V in 100-275K temperature range for nMOS-C. **(Inset)** Arrhenius plot of $-\Delta V_{FB}$ shows a single bulk defect level. **(b)** 10KHz G-V in 100-275K range for nMOS-C.

4.3.3 Low Temperature C-V at Different Frequencies

At low temperatures, the dopant atoms activation at the surface has been reported to cause dispersion in the C-V plots, especially at the flatband region [76]. When Fermi level crosses dopant-atom energy level at the surface during C-V measurement, dopant atom charging/discharging responds to ac test frequency. This results in the observation of the 'dip and peak' in the measured capacitance near flatband region at

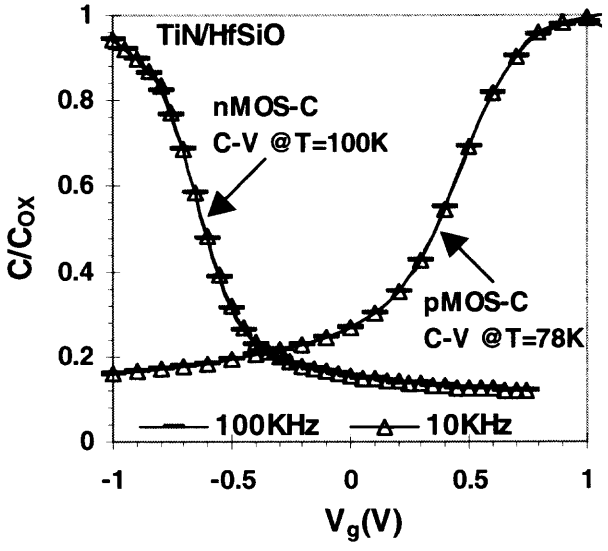


Figure 4.5 100 KHz and 10 KHz normalized C-V plots for nMOS-C at low temperature of 100K and for p-MOS-C at 78K.

low temperatures as reported in [75]-[77]. In this case, any such discrepancies in the capacitance were not observed in the flatband region even when the test frequency was varied at low temperatures as shown in Figure 4.5. The Figure illustrates 10KHz and 100KHz C-V plots for nMOS-C and pMOS-C at 100K and 78K, respectively. This furthers confirms the earlier assumption that low temperature induced dispersion in C-V is due to the trapping within the bulk high-κ.

4.3.4 Defect Levels in the Context of MOS Energy Band Diagram

As stated earlier, the energy levels of these deep defects, as stated earlier, can be determined with respect to the Si band edges from their activation energies as shown in Figure 4.6. The bulk electron (E_T and E_T') and hole (E_T'') trap levels are shown with respect to E_c^{Si} and E_v^{Si}, respectively in the context of MOS band diagram in Figure 4.6.

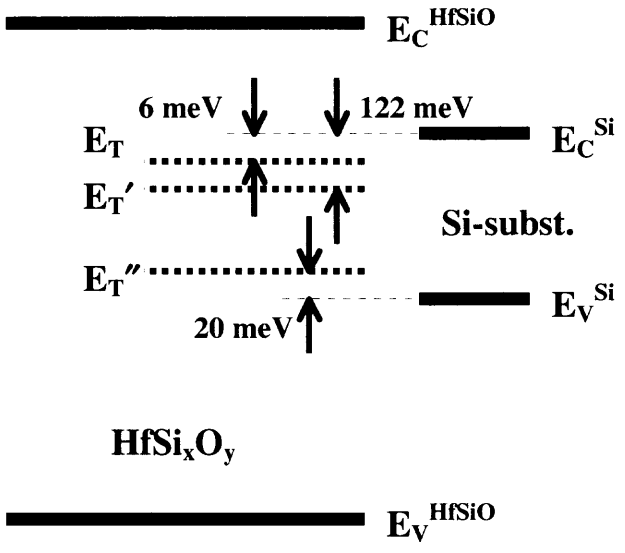


Figure 4.6 Deep bulk electron (E_T and E_T') and hole (E_T'') trap levels in the context of MOS band diagram.

As stated earlier, O vacancies ($V^{++}/V^{+}/V^{0}$) are the prime candidates for electron trapping at the deep levels within the Hf-based high-κ dielectrics, which are shown to be O deficient [10]. Moreover, O diffusion during growth is also observed [68]. Following defect reactions are highly possible between vacancies (V^{0}/V^{+}) and

interstitials (O^0/O^-), as calculated in [33], at the high temperatures during the growth:

$$O^0 + V^0 \Rightarrow O^- + V^+ \quad (4.3)$$

$$O^- + V^+ \Rightarrow O^{--} + V^{++} \quad (4.4)$$

As PDA at 700^0C took place during the fabrication of the devices, which was subject to the conventional CMOS process flow, it is quite reasonable to expect that such charged vacancies are present in the films. As such, the equilibrium in the numbers of charged vacancies and interstitials, i.e., the charge neutrality is maintained in the fresh devices.

It is reported in [48] that PDA at 700^OC/60s in NH_3 ambient does not significantly increase N and simultaneously reduce O in Hf-silicate films as does PDA at higher temperature (e.g. 900^OC/15s) in the same ambient. Basically, O vacancies are less under the former condition [48], which in turn reduces electron trapping and leakage, and, thus, improves electrical performance.

Atomic N concentration was ~10% in Hf-silicate films [48] after 700^OC/60s PDA in NH_3 ambient. One of the plausible reactions for NH_3 dissociation is $NH_3 \Rightarrow (NH_2)^- + H^+$, which has been calculated to be occurring within 1-2 ps of PDA at T > 600 K [33]. This is why H incorporation into the film can be expected to be at the order of that of N. Interfacial layer (IL) is chemically grown SiO_2 in the devices. H passivates interface states after PDA and D_{it} is in range of 10^{12} $cm^2.ev^{-1}$ in this type of devices. Considering reduction of O at higher temperatures and NH_3 dissociation starting above 600 K, it is believed that PDA at 700^OC/60s is probably optimized. As clearly mentioned in Section 2.3.3.2, shallow V^{++} level shows the negative-U

transition to deep V^0 level after successively capturing two electrons ($V^{++} + e \rightarrow V^+$; $V^+ + e \rightarrow V^0$). After capturing two electrons, V^0 puts an end to the charge neutrality discussed above and the film becomes negatively charged [62]. According to the calculation by Torii et al. [35], V^0 lies ~1.6eV below the conduction edge, which was also experimentally observed. It may be immediately mentioned that considering Hf-silicate/Si conduction edge band offset to be ~1.5eV [66], E_T' lie ~1.6eV below the high-κ conduction edge in these films. It affirms the assumption regarding the presence of O vacancy defects in these bulk high-κ films. Furthermore, V^0 level lies within Si bandgap range, i.e., it induces deep defect level and gives rise to the slow transient trapping. Moreover, in order to maintain charge neutrality, O^{--}/O^- levels also need to be present in this film. After capturing hole, O^0 level moves upward and may lie within Si bandgap range. Based on this, E_T' and E_T''' can be tentatively assigned to V^0 and O^0 defect levels, respectively.

4.4 Defect Levels from Leakage Measurements

Defect energy levels, observed from leakage measurements, in the context of MOS energy band diagram are introduced in Section 4.4.

4.4.1 P-F Plots under Gate Injection

Gate current vs. gate voltage (I-V) measurements were taken for negative gate bias conditions in 273K-398K temperature range as shown in Figure 4.7. It is obvious from the Figure that a thermally and field activated conduction mechanism dominates

during gate injection. This is further evident from Figure 4.8, which shows the straight-line behavior of Arrhenius plots of $\ln(-J_g/E_{OX})$ for different negative gate biases applied on nMOS-C. Activation energy, E_a was calculated to be ≈ 0.3eV for $V_g = -2V$ to $-4V$.

The ratio of the potential drops at the high-κ layer (V_{HK}) and IL (V_{IL}) are estimated from their respective dielectric constants (κ_{HK} & κ_{IL}) and thicknesses (t_{HK} & t_{IL}) using the following equation [17]:

$$\frac{V_{HK}}{V_{IL}} = \frac{\kappa_{IL}}{\kappa_{HK}} \times \frac{t_{HK}}{t_{IL}} \tag{4.6}$$

As $t_{HK}/t_{IL} \approx 3.5$ and $\kappa_{HK}/\kappa_{IL} \approx 3.5$ in these gate stacks, equal potential drops at the high-κ layer and IL occur. Here, resultant electric field, $E_{OX} = E_{HK} + E_{IL} = V_{HK}/t_{HK} + V_{IL}/t_{IL}$. Furthermore, $V_{HK} = V_{IL} = V_{OX}/2 = (V_g - V_{FB} - \Psi_s)/2$, where Ψ_s is the surface potential. Therefore, $E_{OX} \approx V_{OX}/0.15 = (V_g - V_{FB} - \Psi_s)/0.15$ (MV/cm).

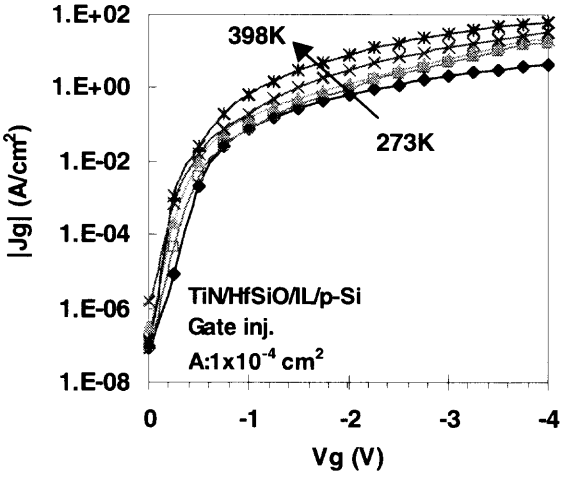


Figure 4.7 I-V measurements in 273K-398K temperature range.

Moreover, V_{HK} and V_{IL} are directly related to the band bending in high-κ layer and IL, respectively, and $V_{HK} = (V_g - V_{FB} - \Psi_s)/2$, where $V_{FB} + \Psi_s \approx -1V$ in these nMOS-C devices. Considering the barrier height at TiN/Hf-silicate interface to be ~2eV [67], the band bending at the bulk high-κ for $V_g = -2V$ ($V_{HK} \rightarrow -0.5$) is not enough for electrons to tunnel from the gate into the shallow traps with levels 0.3eV below the bulk high-κ conduction edge. The same also holds for $V_g = -4V$ ($V_{HK} \rightarrow -1.5V$) as far as the traps located within the direct tunneling distance from the gate are concerned. Electrons do not enter the bulk high-κ conduction band, due to the thermal emission or field-assisted tunneling [69], at any stage during their transport across the gate stack. Transport rather takes place through the deep localized states within the high-κ bandgap [19], [20] as shown in the inset of Figure 4.9.

Calculations show that the midgap V^0 and V^+ states are the potential candidates for electron transport [14], [20]. The strong possibility of the presence of V^0/V^+ levels in this oxide is already shown. Moreover, difference between V^0 and V^+ levels was calculated to be 0.3 eV, which shows an excellent match with the experimentally observed E_a. It is possible that electrons tunnel from metal gate to V^+ level, which relaxes to V^0 level after trapping an electron. Under strong electric field it thermally emits to the adjacent V^+ level, which lies 0.3 eV above. Thus, carrier transport may take place across the oxide during gate injection. This in turn gives rise to the experimental observation of V^+ level in this film.

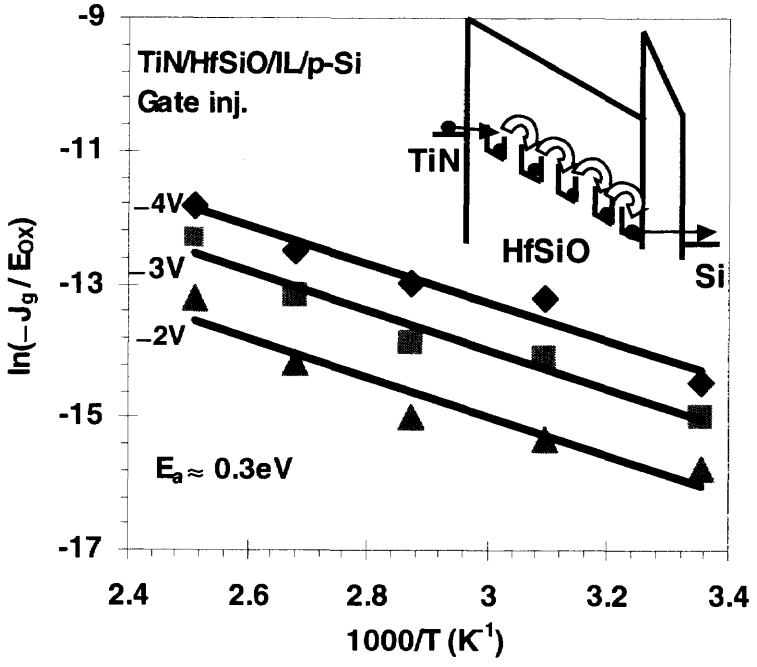


Figure 4.8 Arrehnius plot of $\ln(-J_g/E_{OX})$ for nMOS-C for different negative gate biases. (**Inset**) Transport through deep localized states under gate injection.

4.4.2 P-F Plots under Substrate Injection

P-F plots are shown in Figure 4.9 for different positive gate biases, applied on n+-ringed nMOS-C. N+-ring was grounded to prevent minority carrier shortage during substrate injection. For positive gate biases (V_g), it can be approximated that $V_{FB} + \Psi_s \approx -0.5$ V, so that, $V_{HK} = (V_g + 0.5)/2$.

For very low V_g (~0.5 V) conduction through deep states dominates as described earlier. E_a of ~0.25 eV implies that $V^{+/}V^0$ pair, predicted for gate injection, may be responsible for substrate injection also. This is shown in Figure 4.10(a). The

difference in activation energies may be due to the different band bending conditions as specified in the P-F emission model (see Figure 4.7).

For moderate Vg (~1 V), leakage shows almost no change with temperature below 200K. At this bias, band bending does not allow F-N tunneling. Direct tunneling is another possibility; however, high leakage points to the fact that the high concentration of defects within high-κ oxides makes the trap assisted tunneling, TAT,

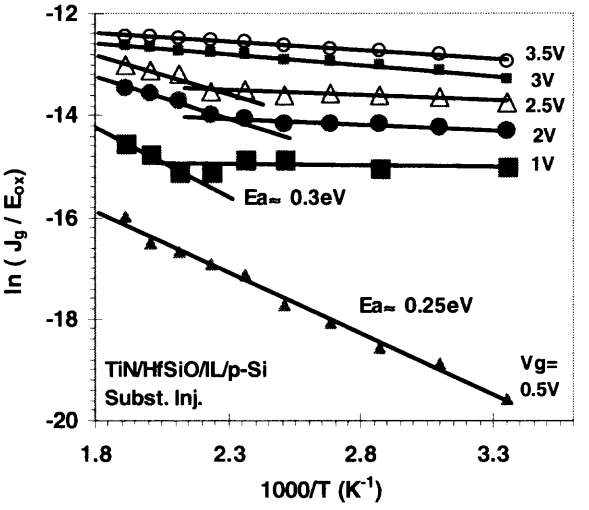


Figure 4.9 Arrehnius plot of $\ln(-J_g/E_{OX})$ for n^+-ringed nMOS-C for different positive gate biases (substrate injection). N^+-ring is grounded.

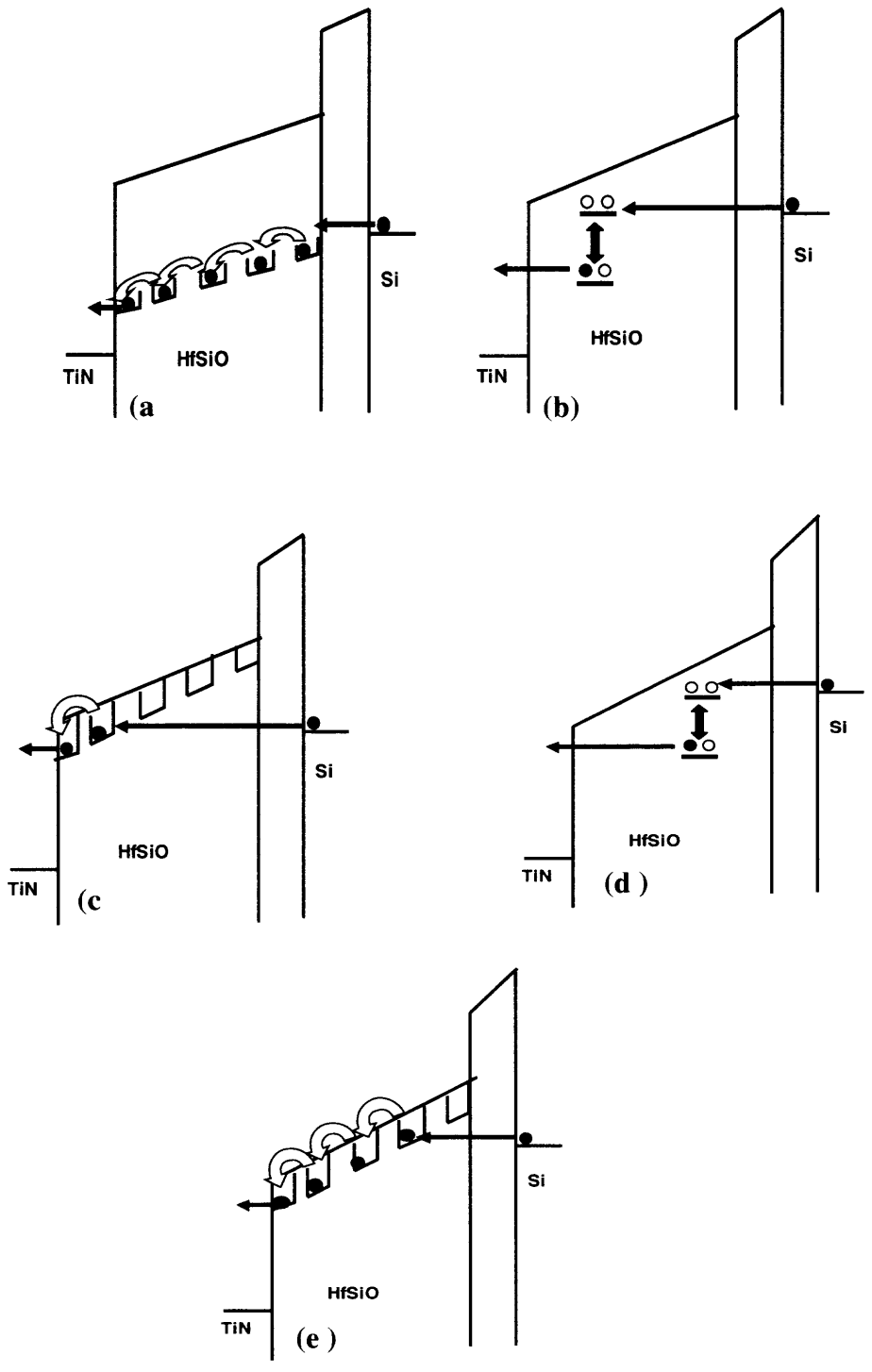


Figure 4.10 Transport mechanisms during substrate injection TiN/$HfSi_xO_y$ based gate stacks: **(a)** low gate bias, V_g (~0.5 V); **(b)** moderate V_g (~1 V) and temperature, T < 200 K; **(c)** moderate V_g (~1 V) and T > 200 K; **(d)** high V_g (~2 V) and T < 175 K and **(e)** high V_g (~2 V) and T >175 K.

a more probable option. Negative-U transition of shallow V^{++} levels, which are resonant with Si conduction band, is a possible fit to TAT. This is depicted in Figure 410(b). Above 200K, P-F emission to high-κ conduction edge dominates. $E_a = E_C - E_T \approx 0.3$ eV matches with V^{-}/V^{--} trap levels. This shows that negatively charged vacancy levels are possibly present in these films. This is depicted in Figure 4.10(c). For moderately high Vg (~2 V), TAT due to negative-U transitions dominates below 175K, whereas P-F emission to the conduction band is significant above 175K as shown in Figures 4.10(d) and (e), respectively. For high Vg (~3 V), dependence of leakage on temperature is not noticeably high.

4.4.3 Defect Levels in the Context of MOS Energy Band Diagram

The defects levels observed from leakage current measurements under substrate and gate injection conditions are depicted in Figure 4.11. Both theoretical and experimental studies by different groups, thoroughly reviewed in Chapter 2, clearly indicate that O vacancies are the primary defect centers for electron trapping. Calculations further indicate that these centers are responsible for electron transport. Torii et al. [35] reported TAT due to the negative-U transition of V^{++} levels. The presence of O vacancies in these films is reasonably established from low temperature measurements. Shallow level, E_T^{1} are observed to be lying 0.3 eV below the bulk high-κ conduction edge in this case. It is a good match with the calculated value of ~0.4 eV for V^{-}/V^{--} in bulk HfO_2, shown by Gavartin et al. [38]. It can be reasonably expected that such shallow vacancies are also present in Hf-silicates. The likely role of mid-gap V^{+}/V^{0} states in P-F- like conduction is explained in Section 4.4. Such P-

F-like conduction was also reported by Ribes et al. [39]. It may be argued that relative locations of the defect levels E_T^2 and E_T^3, shown in Figure 4.11, is consistent with the observations of this work. Hence, tentative physical origins of E_T^1, E_T^2 and E_T^3 are V^-/V^{--}, V^+ and V^0, respectively. For E_T', it is speculated to be V^{++}.

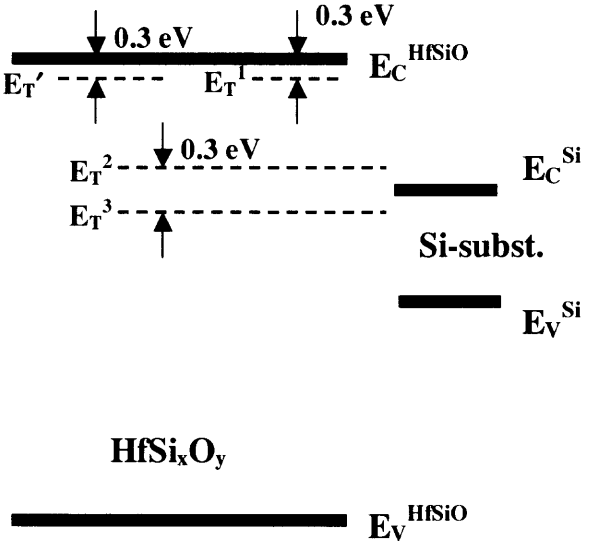


Figure 4.11 Defect levels in the context of MOS band diagram.

4.5 Defect Levels from Time and Temperature Dependent Detrapping

To determine defect levels responsible for hole trapping, substrate hot hole (SHH) stress was applied. Details of substrate hot carrier stress are described in Chapter 3. Carriers impinge on Si/IL interface with incident carrier energy, $E_{inc} \approx q|V_s|$, where V_s is the applied substrate bias. Calculated formation energy of Hf-V^{++}-Si is ~4eV. As a result, SHH stress with $E_{inc} \approx 4$ eV, i.e., Vs = 4V is expected to generate Hf-V^{++}-Si defects. Experiment involving time and temperature de-trapping of holes to Si substrate is designed to find the defect levels with respect to Si valence band, E_V^{Si}.

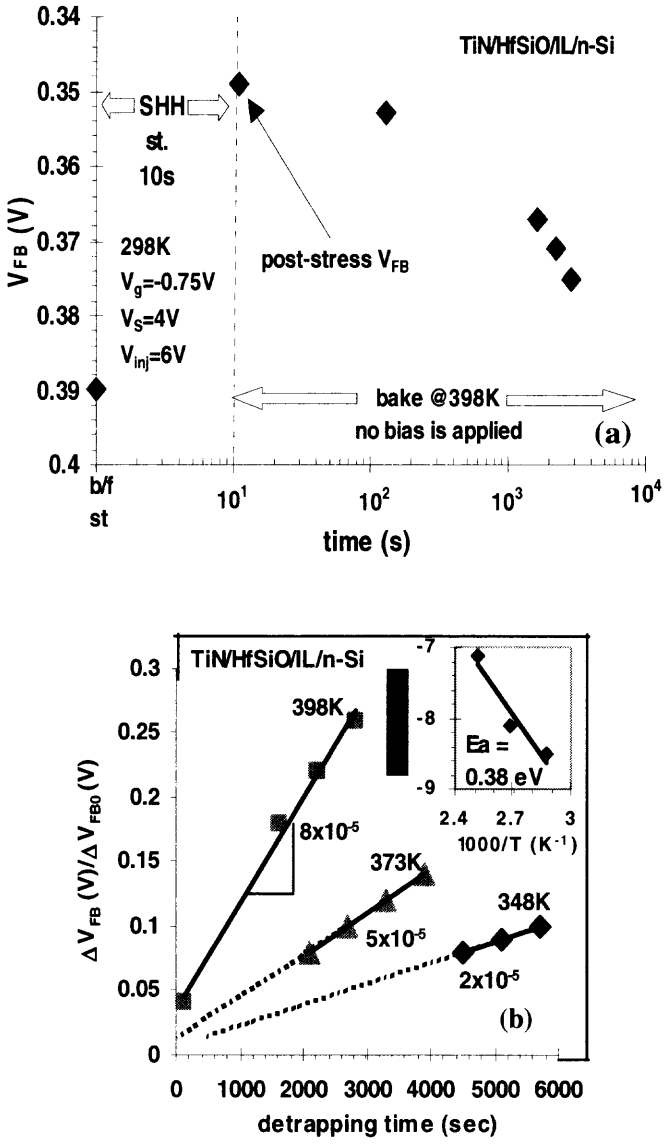


Figure 4.12 **(a)** V_{FB} during 10s of SHH stress followed by bake at 398K under 'no bias' condition. Bake is periodically interrupted to measure V_{FB} at room temperature. **(b)** ΔV_{FB} = V_{FB}@bake time – post-stress V_{FB}. ΔV_{FB} is normalized w.r.t. initial increase in V_{FB} during stress (ΔV_{FB0}) and $\Delta V_{FB}/\Delta V_{FB0}$ is plotted for different bake temperatures. Slopes are calculated from normalized ΔV_{FB} vs. de-trapping time curves and are shown in the Figure. **(Inset)** Arrhenius plot of the slopes shows a single bulk defect level.

In order to determine the generated defect energy level, 10s of SHH stress with V_s = 4V was followed by the bake at 398K under 'no bias' condition as shown in Figure 4.12(a). Periodically the bake was interrupted to measure V_{FB} at room temperature. It can be observed from the Figure that V_{FB} decreased after stress, which signifies hole trapping in the generated traps. During the bake, V_{FB} increased as hole de-trapping to substrate occurred. ΔV_{FB} is calculated from the difference of V_{FB} during the bake with respect to post-stress V_{FB}. It is normalized with respect to the initial increase in V_{FB} during stress ($\Delta V_{FB} / \Delta V_{FB0}$) and plotted as a function of de-trapping time for different bake temperatures in Figure 4.12(b). It is obvious from the Figure that slopes of hole de-trapping, that is, hole emission rate, increases with even moderate increment in temperature under 'no bias' condition. Based on the discussion in the Section 4.2, it may be further affirmed that the generated bulk high-κ trap levels lie within Si bandgap range. Arrhenius plot of the slopes (Figure 4.12(b) inset) shows an activation energy of ~0.4V. It is concluded that the physical origin of the stress-induced defects is 'arm' vacancy. After capturing holes Hf-V^0-Si level, which lies below E_V^{Si}, relaxes to Hf-V^{++}-Si level (Hf-V^0-Si + 2h $\rightarrow$ Hf-V^{++}-Si), lying within Si bandgap.

4.6 Defect Levels in Context of MOS Energy Band Diagram

Defect levels, observed from different types of experiments, are shown in a comprehensive manner in the context of MOS band diagram in Figure 4.13. All the major defect levels, stipulated by theoretical models to be responsible for transient trapping and trap-assisted carrier conduction across the gate stack, have been put in Figure 4.13. Speculated physical origins of the defects are also stated. Calculated V^{+} and V^{++} levels are also shown for the sake of completeness. It may be safely stated that these observations support the values of these levels.

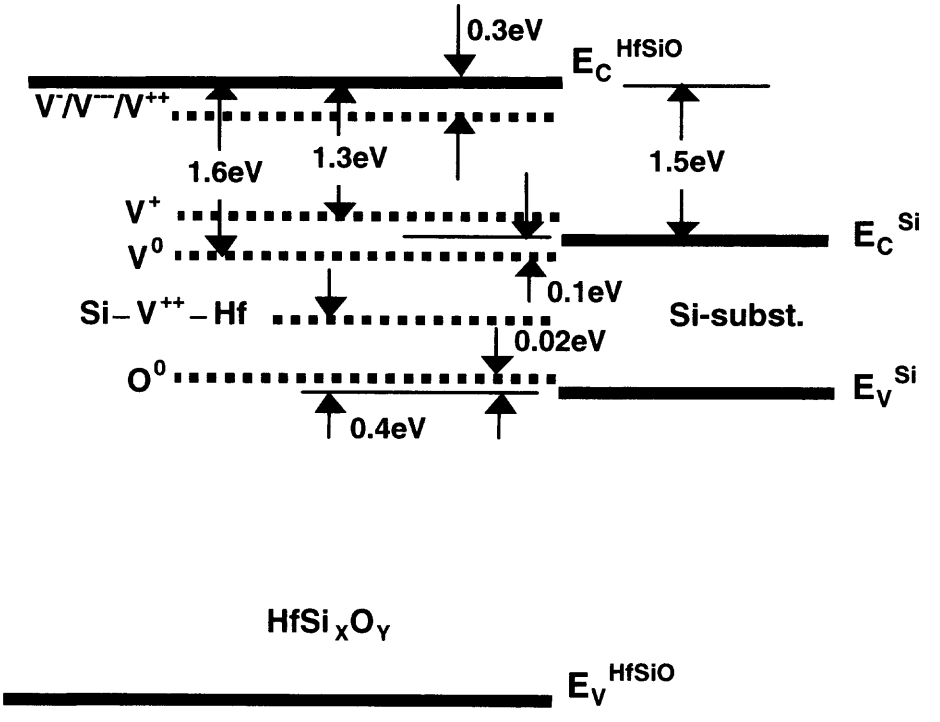


Figure 4.13 Defect levels in the context of MOS band structure.

4.7 Summary

Different types of experiments were successfully designed and their results were critically analyzed to find the dominant defect levels, which are responsible for both trapping and transport in TiN/$HfSi_xO_y$ based gate stacks, in the context of MOS band structure. Excellent match with calculations based theoretical models have been observed. As a result, the probable physical origins of the defects have been tentatively stipulated. On the basis of these observed defect levels, effective physical models can be formulated to provide relevant explanation to the results obtained from different electrical stress tests, which are the integral parts of the high-κ reliability studies. Thus, an essential step toward the comprehensive understanding of the high-κ reliability has been taken.

CHAPTER 5

TRAPPING CHARACTERISTICS OF TiN/$HfSi_xO_y$ BASED GATE STACKS UNDER STRESS

5.1 Introduction

Trapping characteristics of under both constant voltage stress (CVS) and substrate hot carrier (SHC) stress conditions were studied during the course of the research work. The experimentally observed defect levels, which are responsible for electron and hole trapping in these as-grown bulk high-κ films, are expected to primarily influence the trapping characteristics under different band bending conditions as the electrical stress CVS is applied. Trapping characteristics due to stress-induced defects are studied by applying substrate hot electron (SHE) and hole (SHH) stress. Moreover, robustness of the bulk Hf-silicate against hot electron and hole with high incident carrier energies (E_{inc}) can be studied with SHC injection. Furthermore, SHE stress with E_{inc} more than the calculated O vacancy formation energy can be applied on these devices. Thus O vacancy induced trapping and transport characteristics can be studied using electrical characterization technique. In addition, based on the experimental results, physical models for both gate and substrate injections are developed.

5.2 Understanding Defect Levels from Detrapping Characteristics

For traps near the substrate, detrapping time, which is the inverse of the emission rate, is thermally activated for the deep defects with constant E_a under 'no bias' condition. Hence, it is slow at room temperature. It is further understood that for an electron trap level above E_c^{Si} or a hole trap level below E_v^{Si} within the bulk high-κ, detrapping time primarily depends on the tunneling transparency. Hence, it is considerably fast, and does not depend on temperature under 'no-bias' condition (Figure 5.1(b)).

On the other hand, the lateral distribution of trapping (high d_T) is possible for stress with long periods of time. For the shallow traps with high d_T, the fast detrapping to the high-κ band edges occurs under a 'low bias' condition as shown in Figure 5.1 (a). But, for the deep traps with similar spatial distribution detrapping is considerably slow because of the tunneling transparency factor.

Therefore, time dependent post-stress ΔV_{FB} recovery characteristics need to be studied under both 'no bias' and 'low bias' conditions to correctly understand the trapping level (shallow/deep). However, re-stressing may occur for the latter, which limits the conclusions drawn from the observations of the detrapping characteristics.

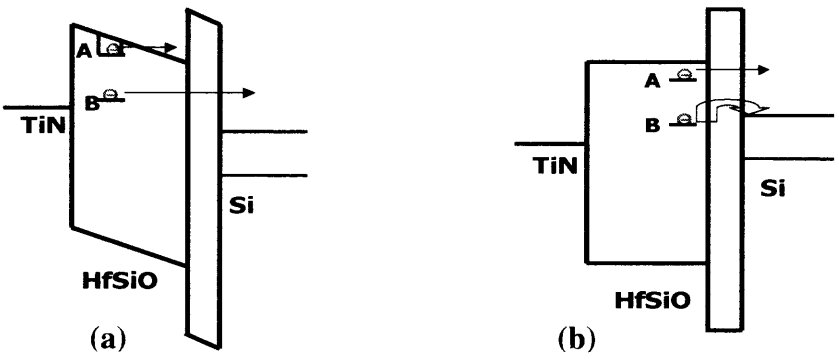


Figure 5.1 Detrapping characteristics from shallow (A) and deep (B) traps under **(a)** idealized 'non-zero bias' and **(b)** 'no bias' conditions for TiN/$HfSi_xO_y$ based gate stacks.

5.3 CVS with Negative Gate Bias (Gate Injection)

In order to understand the effects of the pre-existing defects, CVS was applied on nMOS-C with different negative gate biases at room and elevated temperatures.

5.3.1 CVS at Room Temperature

CVS was applied on nMOS-C with different negative gate biases for 2,000 seconds. For better comparison purposes ΔV_{FB} is plotted as a function of charge injection, Q_{inj} in Figure 5.2(a) for $V_g = -3V$ and $-4V$. It is obvious from Figure 5.2(a) that hole trapping dominates, but it shows a turn-around effect as Q_{inj} is gradually increased. It is further observed that for a given Q_{inj} the trapping increases with the gate bias.

To understand the cause of the turn-around effect, the post-stress and post-relaxation C-V plots, shown in Figure 5.2(b), need to be carefully analyzed. Slight dispersion in V_{FB} is observed for 2,000s of stress with $V_g = -4V$. However, 48 hours

after removal of stress V_{FB} shifts significantly to left. This shows that electron de-trapping occurred at the beginning of the post-stress relaxation period, which in turn shows the true extent of hole trapping. However, for longer relaxation times (120 hours), hole de-trapping shifts V_{FB} towards its pre-stress value. It may be concluded that hole trapping occurs initially near the substrate during stress. The gradual build-up of electron trapping near the substrate offsets hole trapping later, which results in the turn-around effect. It may be further concluded that after 2,000s of stress negligible ΔV_{FB} is observed because of the significant presence of both trapped electrons and holes near the substrate. However, significantly long electron and hole de-trapping time can be observed under 'no bias' condition. Based on the discussions in the previous Section 5.2, it may be inferrred that both electron and hole trapping occurred at the deep bulk defects lying within Si bandgap range.

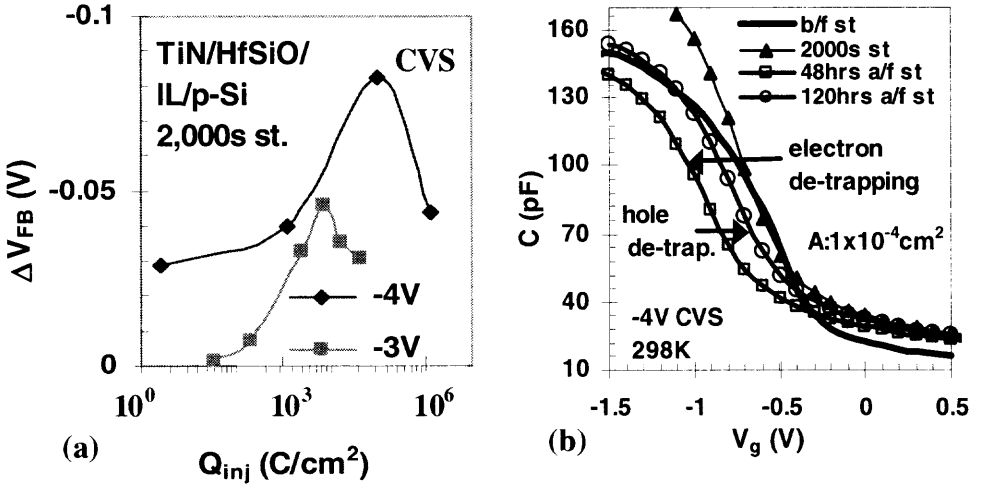


Figure 5.2 **(a)** ΔV_{FB} vs. Q_{inj} for V_g = – 4V and –3V under CVS applied on nMOS-C for 2,000s. **(b)** Before stress, post-stress and post-relaxation C-V under CVS at V_g = –4V.

To investigate whether the trapping occurred at the pre-existing bulk traps, two successive cycles of 2,000s of stress and 48 hours of relaxation were applied on a fresh nMOS-C device for stress level of – 4V as shown in Figure 5.3. Difference between post-relaxation and post-stress ΔV_{FB} indicates the magnitude of stress-induced trapping. It is obvious from Figure 5.3 that, after 2nd 2,000s stress trapping increased by only ~10%, indicating that the trapping mostly occurred at the pre-existing traps. Therefore, it may be assumed that the pre-existing deep bulk electron and hole traps, observed during low temperature measurements, are responsible for the mixed degradation in the films under gate injection.

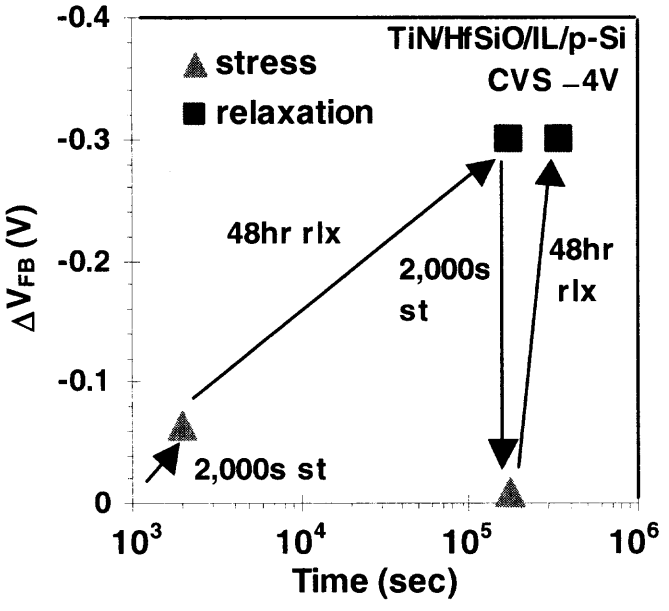


Figure 5.3 Post-stress (2,000s st) and post-relaxation (48 hours of relaxation) V_{FB} for two successive stress/relaxation cycles applied on nMOS-C.

5.3.2 CVS at Elevated Temperature

CVS was applied at 125^{0}C on nMOS-C for different gate bias conditions as shown in Figure 5.4(a). A similar turn-around effect is observed. Therefore, mixed degradation also occurred at high temperatures. Increase in the magnitude of V_{FB} with temperature is obvious. Normalized change in interface state density, D_{it} is shown for different gate biases at room and elevated temperatures. Insignificant change in D_{it} shows that trapping mostly occurred at the bulk, which is consistent with the earlier observations.

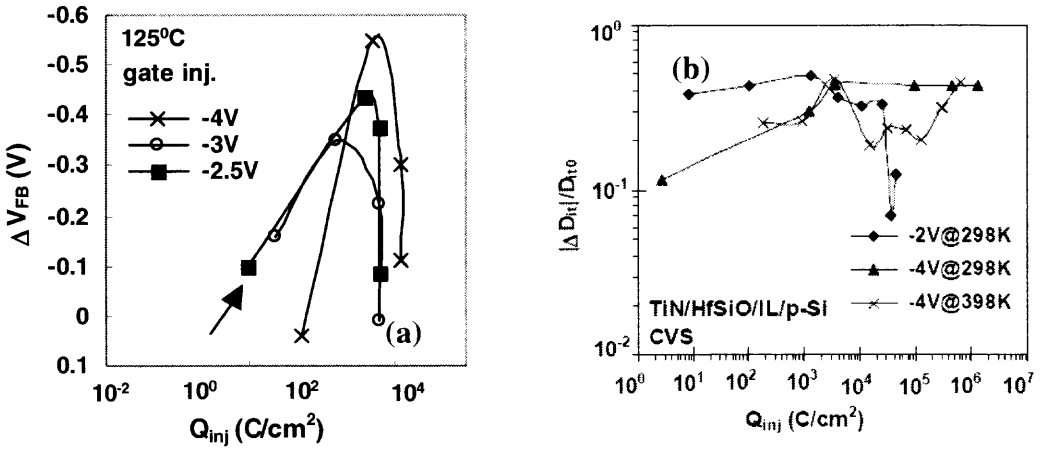


Figure 5.4 **(a)** ΔV_{FB} vs. Q_{inj} under CVS at 125^{0}C for different gate biases for nMOS-C. **(b)** Normalized change in D_{it} vs. Q_{inj} for different gate bias at room at elevated temperatures.

By providing adequate relaxation time, separate effects of electron and hole trapping on ΔV_{FB} can be differentiated as hole de-trapping follows that of electron. At high V_g of -4 V, ΔV_{FB} vs. stress time is plotted on log-log scale for room and

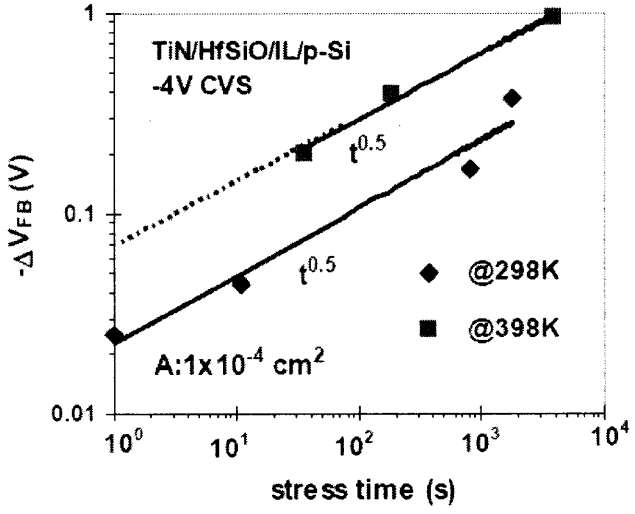


Figure 5.5 ΔV_{FB} vs. stress time in log-log scale.

elevated temperatures as shown in 55.6. Figure 5.5 confirms that ΔV_{FB} shows a t^n dependence with n~0.5 for both temperatures. It is well established that this high value of the exponent is characteristic of trap generation. The same value of the exponent further implies that the trap generation mechanism probably remains same as temperature is varied at high gate bias.

5.3.3 Physical Model for Gate Injection

It is obvious that mixed degradation, due to both electron and hole trapping at the deep defects, occurs in these films. It is further understood that trapping increases with temperature. The thermal activation of the trap generation clearly implies that H species induced trapping needs to be analyzed for this case [69]-[72]. The cause of H species release is commonly related to breaking of Si-H bonds at the Si/IL interface.

Two visible signatures of this process are interface state generation and decrease of inversion capacitance with time [73]. In this case, however, both are absent.

As far as hole trapping is concerned in this case, O^-/O^{--} trap holes and O^0 may lie within Si bandgap as stated earlier. O 'arm' vacancies at the IL/high-κ interface are more potential speculated candidates since hole trap levels within Si band-gap range have been experimentally observed. Moreover, its formation energy ≈ 4eV and at V_g = 4V under gate injection, hole trap generation is clearly observed from Figure 5.6.

In order to understand electron trapping near the gate in this case, electron transport during gate injection needs to be understood. It may be reasonable to assume that electrons tunnel from the gate into the deep bulk traps during gate injection, which initiates thermally and field activated conduction from trap to trap towards the substrate as shown in Chapter 4. It may be further assumed that beside transport, these localized deep bulk high-κ states also trap injected electrons and the centroid of electron trapping moves towards the substrate. This is consistent with the gradual negative charge build-up at the deep bulk defects near the substrate, which is observed to increase with gate bias during the application of gate injection on these devices and thus, to cause turn-around effect.

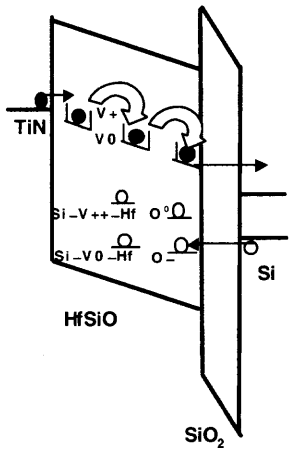


Figure 5.6 Physical model of charge trapping under gate injection. Speculated physical origins of the observed defect levels are also shown.

Based on this, physical model of charge trapping under gate injection is depicted in Figure 5.7. Speculated physical origins of the observed defect levels are also shown. P-F- type conduction of electrons through deep traps under gate injection, shown in Figure 5.7(a), does not give rise to significant energy release at the anode, i.e, substrate side. Hence, anodic hot hole injection induced Si-H bond breaking at SiO_2/Si interface and subsequent interface state generation and H diffusion are not observed in these experiments. Therefore, this model is valid.

5.4 CVS with Positive Gate Bias (Substrate Injection)

In order to avoid minority carrier shortage during substrate injection instead of nMOS-Cs, nMOSFETs were used. Grounding source/drain, CVS was applied for different gate bias conditions. Threshold voltage shift, ΔV_T is shown with respect to stress time and Q_{inj} in Figures 5.7(a) and (b), respectively.

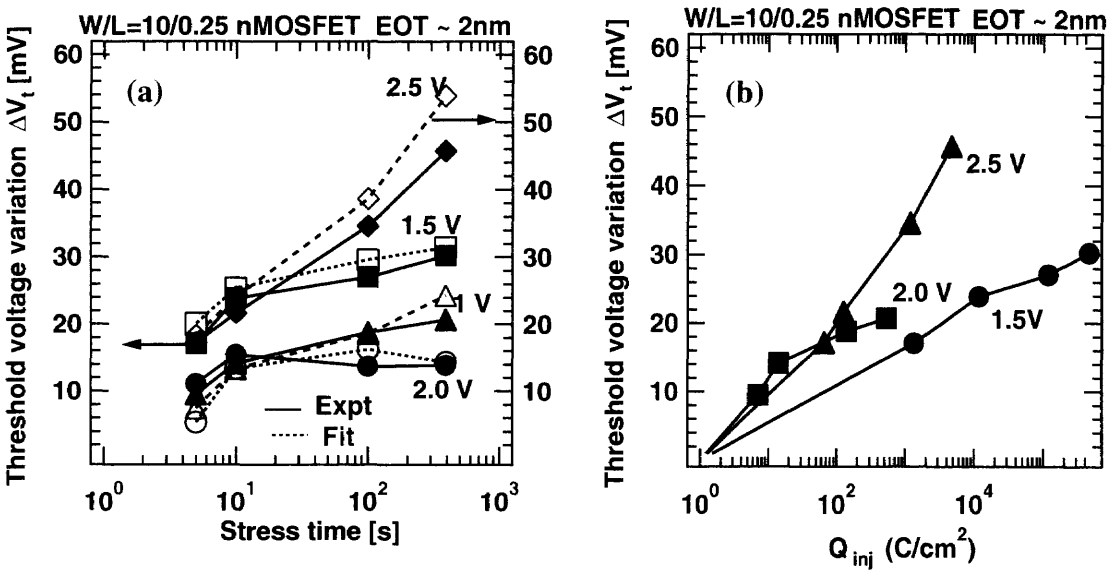


Figure 5.7 **(a)** ΔV_T vs. stress time and **(b)** ΔV_T vs. Q_{inj} for different gate biases under gate injection.

The slope of the voltage shift (ΔV_T) increases with the applied stress voltage indicating that electron trapping rate increases with time. A close curve fit of the experimental data was done using the equation [4], $\Delta V_T(N_{inj}) = \Delta V_{max} \times (1-\exp(-\sigma_0 \times N_{inj})^{\beta})$ where ΔV_{max} is the total trap density, σ_0 and β are model parameters [4]. A value of 1×10^{12} #/cm^2 was taken for ΔV_{max} based on experimentally calculated values, and σ_0 and β were fitted for the values of 1×10^{-14} and 0.37~0.45, respectively. The injected charge N_{inj} was found to be much lower than the $1/\sigma_0$ confirming that the ΔV_T follows the power law equation.

During CVS, as the injected charge in the oxide increases, increased charge-trapping results in increased threshold voltage variation. Also note that the slope of the curve was greater for higher stress voltages. The slope variation of ΔV_T is higher

for stress voltage of 2.5V compared to that of 2 or 1.5V. This further suggests that the electron-trapping rate increases with the increase in applied stress voltage and stress current.

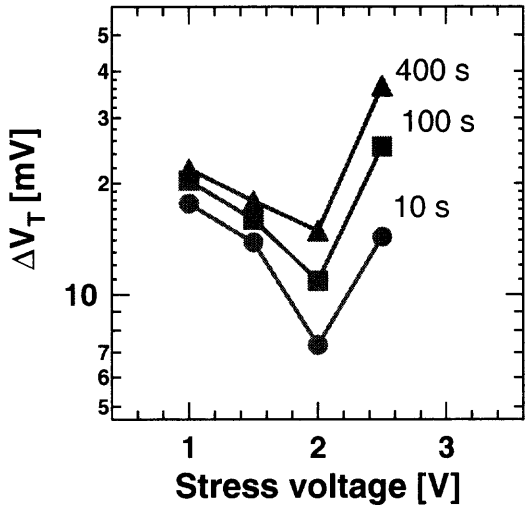


Figure 5.8 ΔV_T vs. stress voltage for different stress times under substrate injection.

The threshold variation is also plotted with applied stress voltage in Figure 5.8. It is obvious that as far as stress level is concerned, it shows a turn-around effect. The reason for this will be explained later with physical models.

Pre-exiting defect levels and transport mechanisms need to be invoked to formulate models for substrate injection. It is understood that trapping at the deep levels are mostly responsible for observed ΔV_T, since de-trapping from shallow levels are difficult to detect with conventional measurement systems as described in Chapter 2.

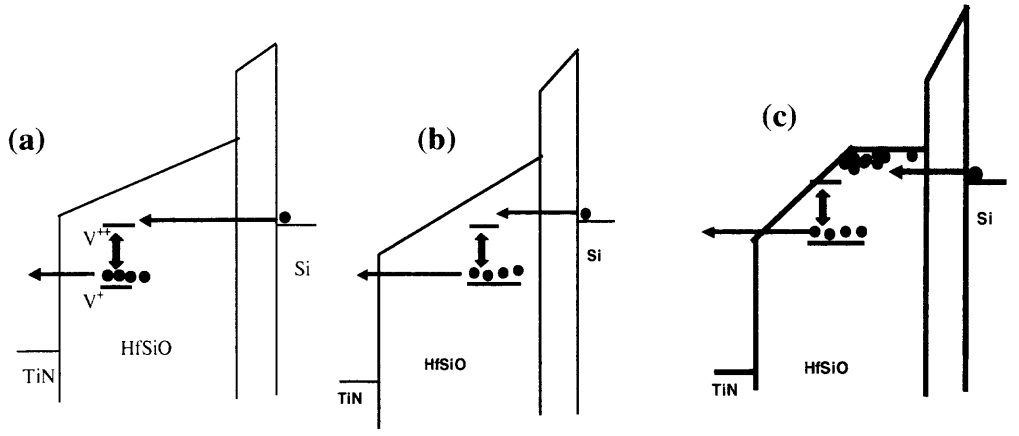


Figure 5.9 MOS band diagrams under substrate injection for **(a)** $V_g \sim 1$ V, **(b)** $V_g \sim 2$ V and **(c)** $V_g \sim 2.5$ V.

For $V_g \sim 1$V, electrons injected from Si conduction edge relax to V^+ level due to negative-U transition as shown in Figure 5.9(a). Although most of the injected electrons tunnel to the anode, there is a very small probability ($\Delta V_T \times C'_{ox} / \Delta Q_{inj} \approx 1\times10^{-10}$) of their being trapped. Therefore, charge accumulation at the deep levels away from the substrate give rise to slow transient trapping since it takes long time to de-trap once stress is removed. This has already been explained with tunneling transparency factor.

For $V_g \sim 2$V, similar phenomenon is observed as shown in Figure 5.9 (b). However, trapped charge accumulation occurs nearer to substrate compared to the previous case. Hence, fast charge de-trapping to substrate takes place, which reduces measured ΔV_T. Hence, the dip is observed in Figure 5.9.

For $V_g \sim 2.5V$, electron trapping, occurring at shallow levels near the substrate modifies the internal electric field as shown in Figure 5.9(c). Hence, deep trapping occurs at a distance away from the substrate, which results in higher ΔV_T compared to $V_g \sim 2V$ case.

5.5 Substrate Hot Electron (SHE) Stress

SHE stress was applied on n^+-ringed nMOS-C using the arrangement shown in Chapter 3. SHE injection was realized by keeping the gate voltage (V_g) and substrate voltage (V_s) at low positive and high negative bias, respectively, while the ring voltage (V_{ring}) was kept grounded. V_{inj} is the bias applied on n^+-ring of the adjacent capacitor located around 10μm away, which forms a p/n^+ junction and acts as an electron injector. For low gate bias ($V_g = 0.75V$), gate current during SHE injection

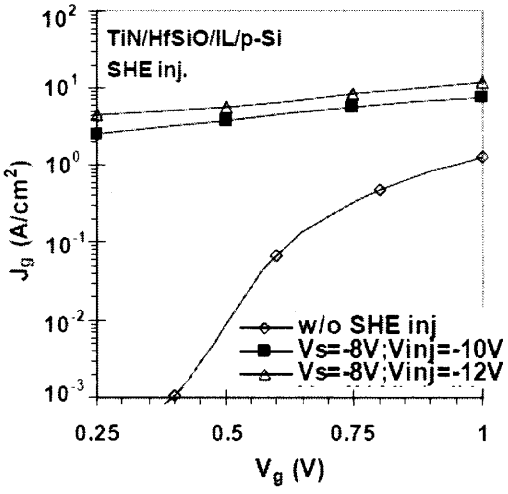


Figure 5.10 I-V characteristics under hot and cold carrier injection conditions.

increases by one order of magnitude compared to the cold carrier case as shown in Figure 5.10. Therefore, during SHE stress, gate current comprises mostly of hot electrons injected into the oxide. In addition, the gate current, that is hot electron injection, increases when injector bias is increased for a given V_S.

SHE stress is applied on n^+-ringed nMOS-C with V_s = –4V, –6V, –8V, –9V and –10V for ~4,000s. For V_s= –10V, significant electron trapping occurred as 1 MHz C-V plots shift to the right in the flatband region as shown in Figure 5.11. Peaks of 10KHz G-V plots shift to the right due to electron trapping. However, no change in the magnitude of the peaks is observed as the interface states generation was negligible and trapping mostly occurred within the bulk high-κ [15]. It is further observed that 18 hours of de-trapping at 'no bias' condition achieved only a partial ΔV_{FB} recovery.

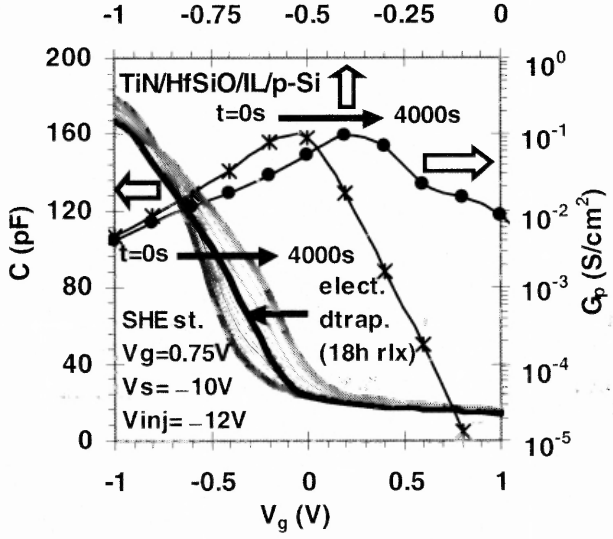


Figure 5.11 Pre- and post-stress, and post-relaxation 1MHz C-V and 10KHz G-V plots for SHE stress.

Figure 5.12(a) depicts ΔV_{FB} during SHE stress with V_s = –9V, post-stress ΔV_{FB} recovery at different reverse gate biases and post-stress relaxation at 'no bias' conditions. Detrapping at –1V recovers ΔV_{FB} by almost 30% very quickly (~1s), but later it saturates. It shows that the shallow trapping at the conduction edge traps located away from the substrate occurs during the stress. This is consistent with the earlier observations under substrate injection. On the other hand, detrapping at –1.5V and –2V shows comparatively slow reduction followed by saturation, which can be attributed to the trapping at the deep defects with lateral distribution. Relaxation at 'no bias' condition for 54 hours, however, shows that hole trapping is partly responsible for the

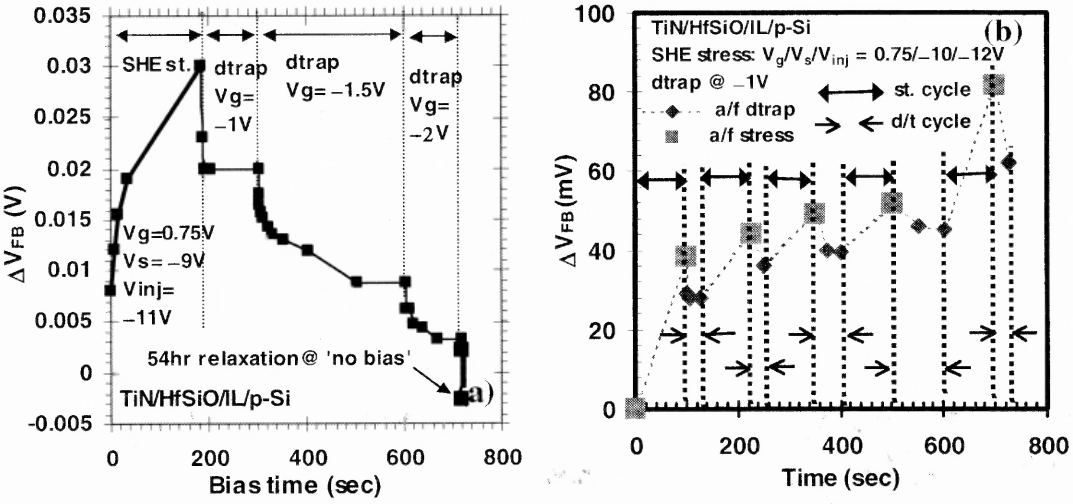


Figure 5.12 **(a)** Time-dependent electron de-trapping characteristics under different post-stress reverse bias conditions. **(b)** ΔV_{FB} during SHE stress/ detrap cycles. SHE stress was applied with $V_g/V_s/V_{inj}$ = 0.75/ –10/ –12 V. During detrapping cycle, V_s = –1V.

observed decrease in ΔV_{FB} under the negative gate bias. In the previous experiments, significant hole trapping was observed at the deep defects when constant voltage stress applied was on nMOS-C with the negative gate bias. Stress/detrapping cycles were repeated for several times in Figure 12(b). Steady increase in the pre-stress and the post stress ΔV_{FB} (> 0) is observed, which shows that the traps are generated during the stress.

The slow ΔV_{FB} recovery time under 'no bias' condition, observed in Figure 5.13, therefore, shows that ΔV_{FB} is due to both the fast and slow transient trapping. However, the latter dominates and is the focus of the investigations in this work. This is why the effect of the fast trapping on ΔV_{FB} needs to be eliminated to study the trapping at the deep defects. But longer de-trapping time under 'non-zero' bias conditions initiates re-stressing. Hence, after each period of SHE stress −1V of reverse bias was applied for 1s before ΔV_{FB} is measured in the following experiments.

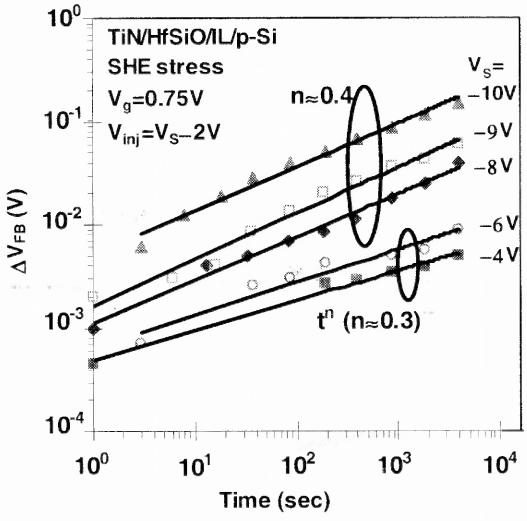


Figure 5.13 ΔV_{FB} vs. stress time in log-log scale for different substrate biases.

Flat-band voltage, ΔV_{FB}, thus corrected for the conduction edge trapping, is plotted as a function of the stress time in log-log scale for different stress levels as shown in Figure 5.14. Power law fits clearly show that t^n dependence dominates for all stress levels due to the generation of the deep bulk defects. Figure 5.14 shows ΔV_{FB} vs. injected charge, Q_{inj} for different stress levels. It is obvious from the power law fits of that the deep bulk defect generation increases with the stress level for a given Q_{inj}. It may be noticed that for V_s= –8V to –10V, the exponents n and $\beta \approx 0.4$ whereas, they are ≈ 0.3 for V_s= –6V. This disparity may be due to the difference in the defect generation mechanisms. This anomaly is also visible from the values of coefficient A, shown in the inset of Figure 5.14. The value of A increases with stress level for V_s= –8V to –10V, which suggest similar defect

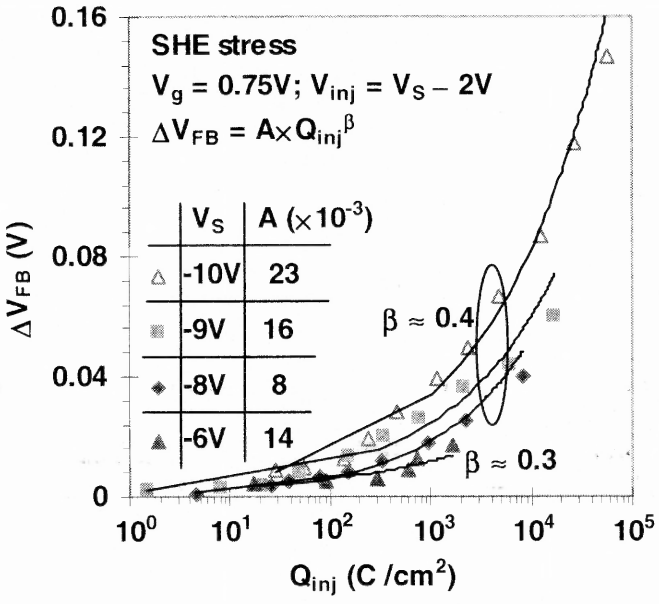


Figure 5.14 ΔV_{FB} vs. Q_{inj} under SHE stress at different V_s ($V_{inj} = V_s - 2V$) bias conditions. (**Inset**) Table showing the value of the coefficient A for different V_s.

generation mechanism. But, this trend is not seen for $V_s = -6V$. This further affirms the earlier assumption.

Change in the leakage $\Delta J_g(t) = J_g(t) - J_g(0)$ vs. stress time in Figure 5.15 shows that it also follows t^n power law dependence. The bulk defect generation is responsible for the enhanced trap-assisted tunneling induced increase in the leakage especially at low V_g [64]. Another reason for increase in $\Delta J_g(t)$ may be due to the positive charge build-up near the substrate [64]. The release of the energy of plasmons at the metal/high-κ interface induces the energetic anodic hole injection [64], which initiates the positive charge build-up. But, the most obvious signature of this process is the interface state generation [8], which is not observed in this case. Hence, the latter option can be ruled out. Therefore, the stress induced defects, which

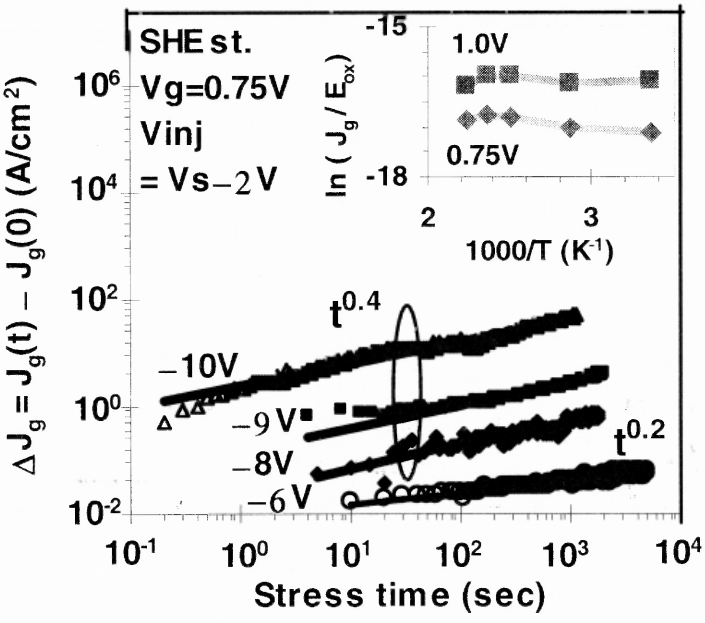


Figure 5.15 $\Delta J_g(t)$ vs. stress time in log-log scale under SHE stress at different V_s ($V_{inj} = V_s - 2V$) bias conditions. (**Inset**) Arrehnius plot of ln (J_g/E_{ox}) for different V_g.

are responsible for the enhanced slow transient trapping and trap-assisted tunneling, may be the same as they show the same value of n, especially for $V_s = -8V$ to $-10V$. The value of n, however, does not follow this trend for $V_s = -6V$, which is expected from previous discussion.

The inset of Figure 5.15 shows Arrhenius plot of ln $(-J_g/E_{OX})$ for n^+-ringed nMOS-C under substrate injection at low gate bias and high temperature conditions. It is obvious that a thermally and field activated conduction mechanism (e.g. Poole-Frenkel-type) is absent for $V_g = 0.75V$ and 1V in the gate stacks as Arrhenius plots do not show a straight-line behavior [66]. Here, electric field, $E_{OX} = (V_g - V_{FB} - \Psi_s)/t_{OX}$, where Ψ_s and t_{OX} are the surface potential and the gate stack thickness, respectively. Moreover, the change of the leakage with temperature is negligible, which is suggested by the earlier assumption that the trap-assisted tunneling dominates during SHE injection. The shortage of the minority carriers did not occur under the substrate injection, as n^+-ring was kept grounded during the leakage measurements. It may be mentioned here that if trapping had occurred mostly at the shallow levels, which are resonant with electrons injected during SHE stress at low V_g, the fast transient trapping would have dominated. The following parts of Section 5.5 will explain why it did not happen; rather significant slow transient trapping occurred.

In this work, deep trap generation and subsequent trapping in them were mostly observed. Hence, ΔV_{FB} reflects amount of trapped charge in stress-induced defects. De-trapping under post-stress reverse bias condition further supports this

observation (see Figure 5.16). The amount of trapped charge, $\Delta Q_{trapped}$ (= $\Delta V_{FB} \times C'_{ox}$; C'_{ox}: oxide capacitance per unit area) is plotted in Figure 5.17 for different V_s under SHE stress. Here, it is considered that charge centroid is located near the substrate.

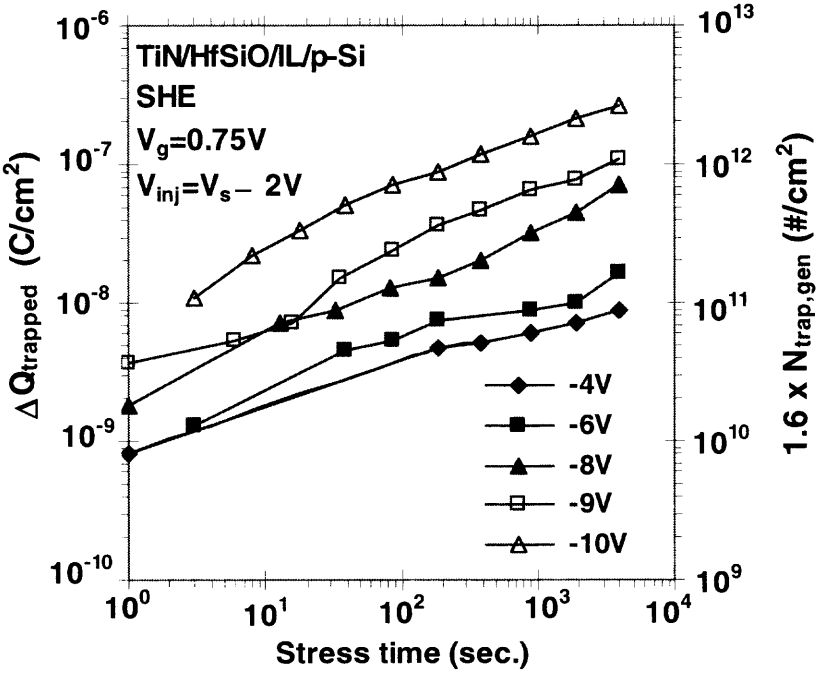


Figure 5.16 Amount of stress induced trapped charge, $\Delta Q_{trapped}$ and number of stress induced traps, $N_{trap,gen}$ as a function os stress time for different V_s conditions under SHE stress.

Number of generated traps, $N_{trap,gen}$ is also shown as the secondary axis in the same plot. Initially, pre-existing traps are filled. Hence, $N_{trap,gen}$ does not show much difference for low V_s conditions. It is reported that trap generation probability, P_g (=$\Delta V_{FB} \times C'_{ox} / \Delta Q_{inj}$) varies with E_{inc} under SHE stress conditions in SiO_2 [71]. Moreover, defect generation by substrate hot electrons impinging on substrate/oxide interface follows the same dependence on energy as that from Fowler-Nordheim (F-

N) injection through the oxide under different positive gate bias [71]. It is further reported that P_g is independent of SiO_2 growth condition and physical thickness in ~1 nm to 5 nm regime. Considering $q|V_s| \approx E_{inc}$ [64], comparison of P_g of these devices (4.5 nm of physical thickness) with that of SiO_2 shows that for low $|V_s|$ (~ 4 V), P_g is almost same (1×10^{-11}). However, for high V_s (≥ 6 V), P_g is in 1×10^{-11} to 1×10^{-10} range in these devices, whereas it is in 1×10^{-7} to 1×10^{-6} range in SiO_2 devices. Significant trap generation most probably occurs within IL even during SHE stress with low V_s, which results in ΔV_{FB}. However, for SHE stress under high V_s conditions, trap generation within the bulk high-κ dominates. High formation energies of O vacancies in the bulk oxide most likely make it more robust against electron injection with high E_{inc}.

Energy levels of the defects, generated within IL, needs to be resonant with the conduction band of the substrate and the bulk high-κ (3.5 nm thick) trap levels to participate in trap-assisted tunneling across the oxide [71]. However, strong correlation observed in between increase in stress induced leakage and ΔV_{FB} (see Figures 5 and 7) suggests that bulk trap generation, which dominates under high V_s conditions, is mostly responsible for both electron trapping and trap-assisted tunneling.

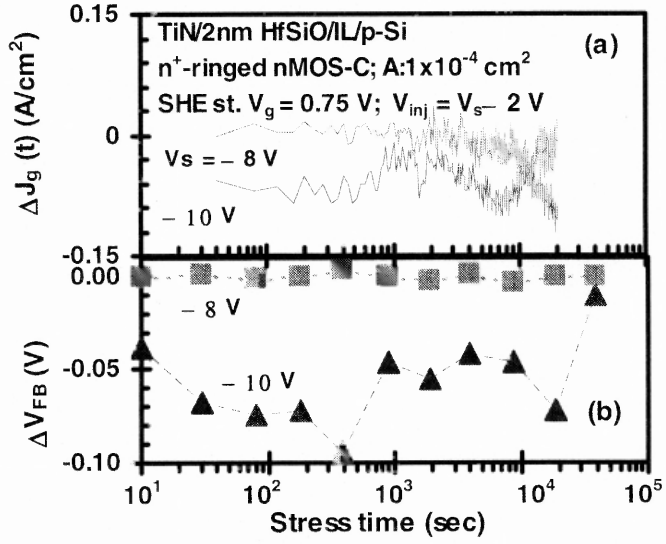


Figure 5.17 For 2 nm Hf-silicate/IL, **(a)** ΔV_{FB} and **(b)** $\Delta J_g(t)$ vs. stress time under SHE stress with $V_s = -8$ and -10 V conditions.

A convincing answer to the question whether the trap generation predominantly occurs within the IL or high-κ layer may be obtained by applying SHE stress on the gate stacks with the same IL but different high-κ layers. The original gate stack was TiN/ 3.5 nm $HfSi_xO_y$/ 1 nm IL/ p-Si. To clarify the above stand, SHE stress was applied under the same conditions on TiN/ 2nm $HfSi_xO_y$/ 1 nm IL/ p-Si gate stacks. ΔV_{FB} and $\Delta J_g(t) = J_g(t) - J_g(0)$ vs. stress time in Figure 5.17 show the strikingly different characteristics. For 2 nm Hf-silicate, the mixed degradation due to both electron and hole trapping dominates. This is in sharp contrast to 3.5 nm Hf-slicates (see Figures 7, 8, 9, 10), where the monotonously increasing electron trapping dominates. It may be concluded that the stress-induced defects are located mostly within the high-κ layer in TiN/ 3.5nm $HfSi_xO_y$/ 1nm IL gate stacks.

Incident carrier energy during SHE stress, $E_{inc} \approx q|V_s|$, where q is the charge of an electron [64]. As stated earlier, $E_{inc} \approx 4eV$ is known as the threshold for the defect generation in Hf-based dielectrics. But, O vacancy formation energy was calculated to be ~7eV under equilibrium conditions [67]. Such defect generation is possible if the incident carrier energy during SHE stress is increased to above 7eV. The enhanced slow transient trapping was observed due to the deep bulk defect generation for $V_s = -8V$ to $-10V$, and its mechanism is shown to be different from that for $V_s < -7V$.

A plausible and coherent phenomenon during SHE stress at high V_s and low V_g, which is consistent with experimental observations, is depicted in Figure 5.18. Electrons impinge on Si/IL interface with high E_{inc} and generate V^{++} defects, which act as the negative-U centers. The relaxation to V^+ and V^0 levels due to the trapping, and subsequent tunneling from them towards the gate increase the leakage. Defect levels other than V^{++}/V^+ are also possibly resonant with the injected electrons as far as the band bending at low V_g is concerned. Hence, the fast transient trapping at the shallow levels is observed; however, it is found to be partially responsible for ΔV_{FB}. A small fraction of the injected electrons ($\Delta V_{FB} \times C'_{ox} / \Delta Q_{inj} \approx 1\times10^{-10}$) becomes trapped at the stress induced V^0 level and gives rise to the significant slow transient trapping.

It may be inferred that O vacancy generation took place, which explains the simultaneous occurrences of the enhanced slow transient trapping and increased trap assisted tunneling during SHE injection with high E_{inc}. It may be further deduced that

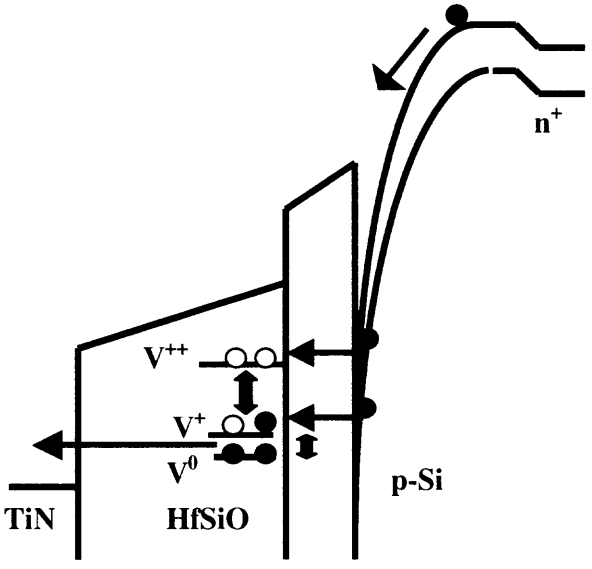


Figure 5.18 Band diagram of the MOS structure showing the negative-U behavior of the stress induced charged O vacancy defects during SHE stress.

that the slow transient trapping occurred at the deep defect level observed from the low temperature measurements in Hf-silicate films.

5.6 Substrate Hot Hole (SHH) Stress

In order to study the characteristics trapping characteristics, SHH stress was applied on p^+-ringed pMOS-C using the arrangement stated in Chapter 3. SHH injection was realized by keeping gate voltage (V_g) and substrate voltage (V_s) at low negative and high positive bias, respectively, while the ring voltage (V_{ring}) was kept grounded. V_{inj} is the bias applied on p^+-ring of the adjacent capacitor located around 10μm away, which forms a p^+/n junction and acts as a hole injector. Hole injection into the gate

stack can be controlled independent of the gate bias by varying V_{inj} ($V_{inj} > V_s$) for a given V_s, while the energy of the incident carriers can be controlled by varying V_s. For low gate bias ($V_g = -0.75V$), the current during SHH injection increases by one order of magnitude compared to the cold carrier case as shown in Figure 5.19. Therefore, during SHH stress, gate current mostly comprises of hot holes injected into the oxide. In addition, the gate current increases when injector bias is increased for a given V_s. These experimental results validate the setup for SHH injection.

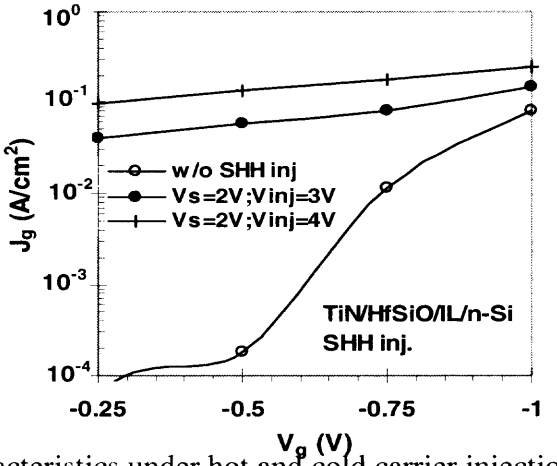


Figure 5.19 I-V characteristics under hot and cold carrier injection conditions.

Flatbnad voltage, ΔV_{FB} under SHH stress for $V_s = 4V$ and 3V is plotted as a function of Q_{inj} in Figure 5.21. It is obvious from Figure 5.20 that hole trapping increases sharply with Q_{inj}. When plotted in log-log scale, ΔV_{FB} follows t^n power law dependence with $n \approx 0.5$ and ≈ 0.25 for $V_s = 4V$ and 3V, respectively as shown in inset of Figure 5.20. These high values of the exponents are characteristic of bulk trap generation. Negligible change in the peak value of the G-V plots with stress (not

shown here) shows that hole trap generation mostly occurred at the bulk high-κ and it strongly depends on the energy of the incident holes.

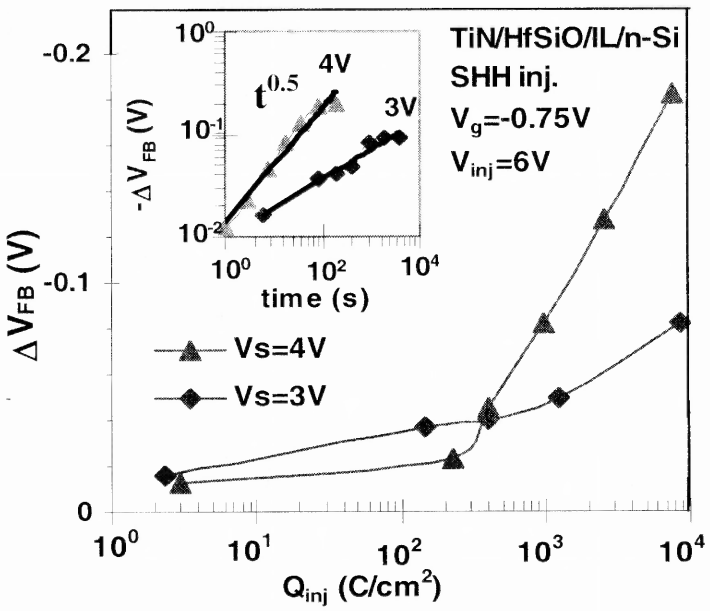


Figure 5.20 ΔV_{FB} vs. Q_{inj} under SHH injection, applied on p^+-ringed pMOS-C for V_s= – 4V and –3V. (**Inset**) ΔV_{FB} follows t^n power law dependence.

To understand the energy level and location of the generated traps, SHH stress with V_s = 4V was followed by ΔV_{FB} recovery periods under different gate bias as shown in Figure 5.21. Detrapping is negligible at V_g = 1V as ΔV_{FB} shows almost no change. This indicates that hole trapping does not occur at the valence edge traps during SHH stress as field assisted tunneling of the trapped carriers to the high-κ

band edges occurs quickly. Moreover, fast de-trapping from deep defects is prevented by the tunneling transparency factor as shown in Equations (1) and (2). Considerable decrease in $|\Delta V_{FB}|$ is observed at $V_g = 1.5V$. However, relaxation for a long period of time (~12 hours) shows that this decrease is due to electron trapping at the pre-existing deep traps and almost no hole detrapping occurred. Therefore, it is difficult to achieve fast ΔV_{FB} recovery, under bias condition, without initiating re-stressing in the gate stacks as indicated before. This study, however, shows that hole trapping mostly occurred at deep defects generated within the bulk high-κ during SHH stress.

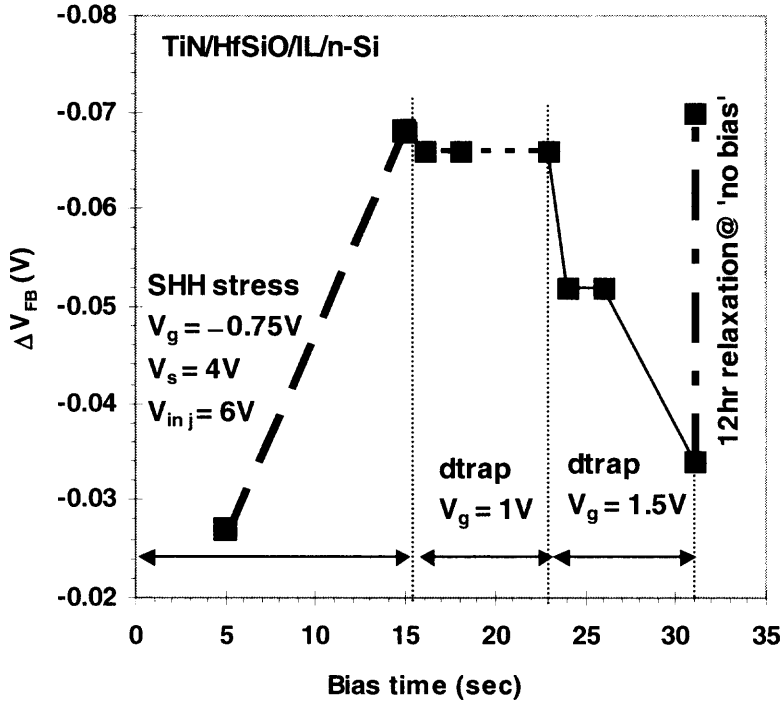


Figure 5.21 Time-dependent electron de-trapping characteristics under different post-stress reverse bias conditions.

Time and temperature dependent post-stress de-trapping studies, stated earlier, show that generated defect level lies ~0.4 eV above the Si valence band. Physical origin has been speculated to be O 'arm' vacancy according as par the match between incident carrier energy and calculated formation energy. Physical model of trapping at the stress-induced defect is shown in Figure 5.22.

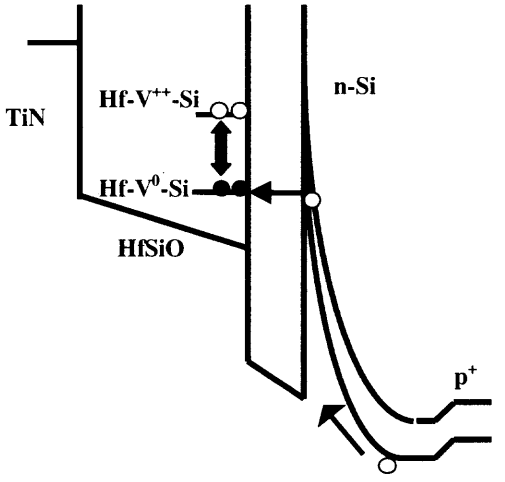


Figure 5.22 Physical model of trapping at the stress-induced defect under SHH stress with high substrate bias.

5.7 Summary

Trapping characteristics of TiN/$HfSi_xO_y$ based gate stacks under different stress conditions are described in Chapter 5. Trapping at the pre-existing deep electron and hole traps are primarily responsible for mixed degradation under gate injection. For substrate injection, precipitation to deep levels due to negative-U transition and subsequent movement of charge centroid toward the gate determines the trapping characteristics.

CHAPTER 6

NEGATIVE BIAS TEMPERATURE INSTABILITY (NBTI)

6.1 Introduction

Negative bias temperature instability (NBTI) is a serious degradation mechanism observed in modern integrated circuits, which operate at elevated temperature due to excessive power dissipation, based on SiO_2 technology [78]. It is being thoroughly studied specifically for low dimension devices. For SiO_2, interface state generation triggered by Si-H bond breaking at Si/SiO_2 interface is the point of major concern. One of the widely-used realistic NBTI models is based on reaction-diffusion (R-D) theory, which basically focus on time dependent net increase in the number of interface states, N_{it} as competing process of bond-breaking and bond-annealing takes place during gate injection. Although successful in interpreting NBTI phenomena in SiO_2 devices, it cannot fully explain the observed NBTI results in Hf-based high-κ gate stacks [79]-[82]. Bulk trap generation is reported to exceed that of interface states in all of the studies [79]-[82], specifically in the cases of low stress biases. Aoulaiche reported that both fast and slow states were generated and subsequently recovered by applying low bias (≤ -2 V) at elevated temperature on TaN/HfSiON gate stacks [79]. However, when –1.5V of NBT stress at 125°C was applied on poly-Si gate/HfO_2 devices, such recovery was not observed and it was attributed to possible generation of hydrogen-related centers within the bulk [87]. Electron trapping, interface state generation and positive charge build-up were simultaneously

observed when NBT stress bias of –1.5 to –2.5 V was applied on poly-Si gate/ HfSiON devices [79]. Interface state generation was reported to be negligible when –2 to –3 V of NBT stress was applied on TiN/$HfSi_xO_y$ devices and V_T instability was attributed on both shallow and deep electron traps within the bulk high-κ [80]. It is obvious that a common NBTI induced degradation scenario has not come out from the studies, most probably due to diversity in processing conditions. Therefore, NBTI studies need to be carried out on one-to-one basis on individual gate stacks.

Constant voltage stress with gate bias, V_g in the range of –1.5 to –3.5 V was applied on pMOSFETS with W=10 μm and L= 1 μm at room temperature (RT). Figure 6.1 shows that for high V_g conditions, positive charge trapping dominates. It is further observed that that ΔV_T finally saturates. For low bias conditions, mixed degradation occurs due to both positive and negative charge trapping within the bulk high-κ.

6.2 Stress at Room Temperature

This is consistent with the previous work with the same gate stacks [81], [82], where the presence of both deep electron and hole traps within the bulk high-κ was reported. Specifically, for –2 V, electron trapping dominates at RT. I_d-V_g plots in Figure 6.2 for –2V shows almost no change in sub-threshold swing, S. As $\Delta S \propto \Delta D_{it}$ [80], interface state generation is negligible at RT for –2 V.

In order to understand the role of holes in interface state generation during gate injection in the devices, CVS was applied with and without non-zero substrate bias,

V_b for V_g = -2.5 V and -3.5 V conditions at RT. For the sake of equivalence, V_b was kept numerically equal to V_g. Carrier separation technique, as shown in the Figure 6.3(a), shows that impact ionization induced reversal of the polarity of the source or

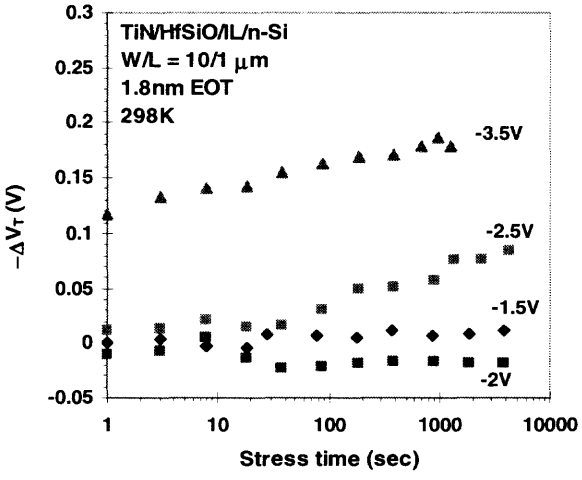


Figure 6.1 V_T vs. stress time for different V_g during CVS at room temperature.

drain current, $I_{S/D}$ [83], [84] did not occur even under V_g / V_b = – 3.5V/ +3.5V stress

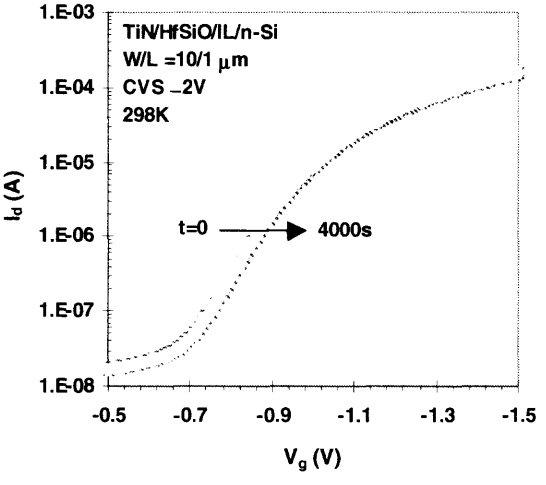


Figure 6.2 I_d-V_g plots for CVS with V_g = –2 V at RT.

condition. It is consistent with results from p^+-poly gate/n-Si structures, where $V_g = -3.5$ V was found to be the threshold for impact ionization [83]. As TiN is a mid-gap material, threshold in this case is $V_g \approx -4$ V.

Increment in I_{gate} can be attributed to increased hole trapping at the pre-existing or stress-induced hole traps. Increase in trap-assisted tunneling (TAT) due to

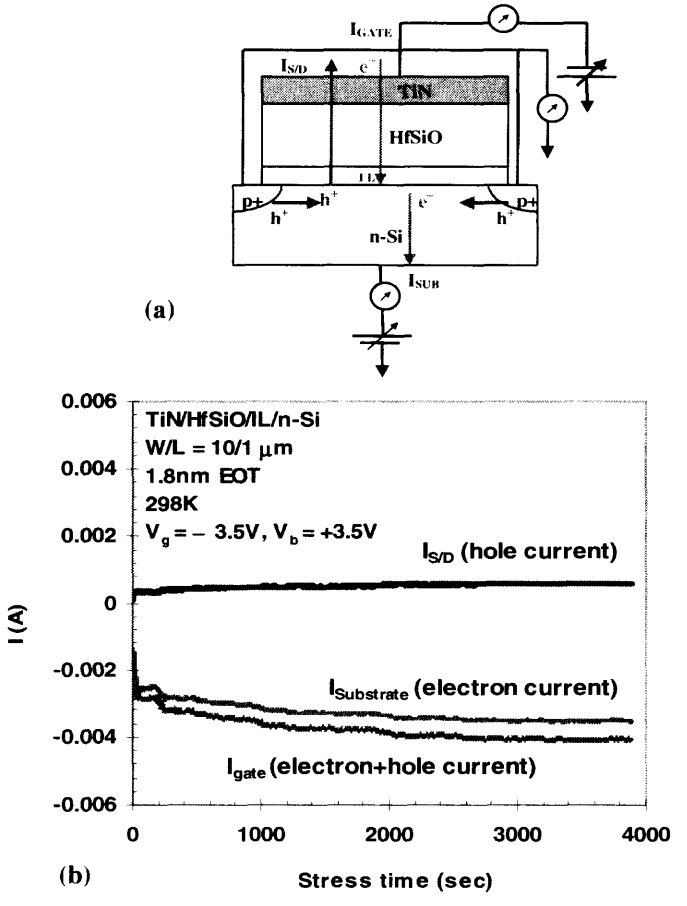


Figure 6.3 **(a)** Carrier separation technique as CVS is applied with negative gate and nonzero substrate bias. **(b)** Current vs. stress time showing electron and hole injection during CVS with nonzero substrate bias.

stress-induced traps may be another cause of increase in gate current. Increase in $I_{S/D}$ can be also attributed to increased TAT.

Figures 6.4(a) and (b) show $\Delta S/S_0$ and ΔV_T during CVS under both zero and non-zero bias conditions. It is obvious from Figure 6.4(a) that enhanced presence of holes due to $V_b > 0$ increases interface state generation. It is further observed from log-log plots that $\Delta S/S_0$ follows t^n power-law dependence. The value of exponent, n ≈ 0.2 for $V_g = -2.5$ V under both $V_b = 0$ V and $V_b = 2.5$ V conditions in this case. This value of n is related to Si-H bond breaking in the presence of low energy holes [85]. Dominance of hot holes results in, $0.2 < n < 0.5$ [85]. This is consistent with the earlier conclusion that impact ionization induced hot holes were not generated during gate injection. For $V_g \tilde{=} 0.5$ V, initial increase in interface state generation was significant. However, absence of hot holes retarded Si-H bond breaking rate under $V_b = 0$ V condition. Consequently, large increase in interface state generation required to sustain $n \approx 0.2$ was not possible. Hence, it initially increased with $n \approx 0.1$ and finally tended to saturate. Nevertheless, $n \approx 0.2$ could be retained due to the presence of increased number of low energy holes under $V_b = 3.5$ V condition. It may be noted that these observations are also supported by the previous work with MOS capacitors [86], where it was shown that for $V_g = -4$ V under CVS and $V_b = 4$ V under SHH stress, ΔV_{FB} increased with $n \approx 0.5$, which is characteristic of hot hole generation.

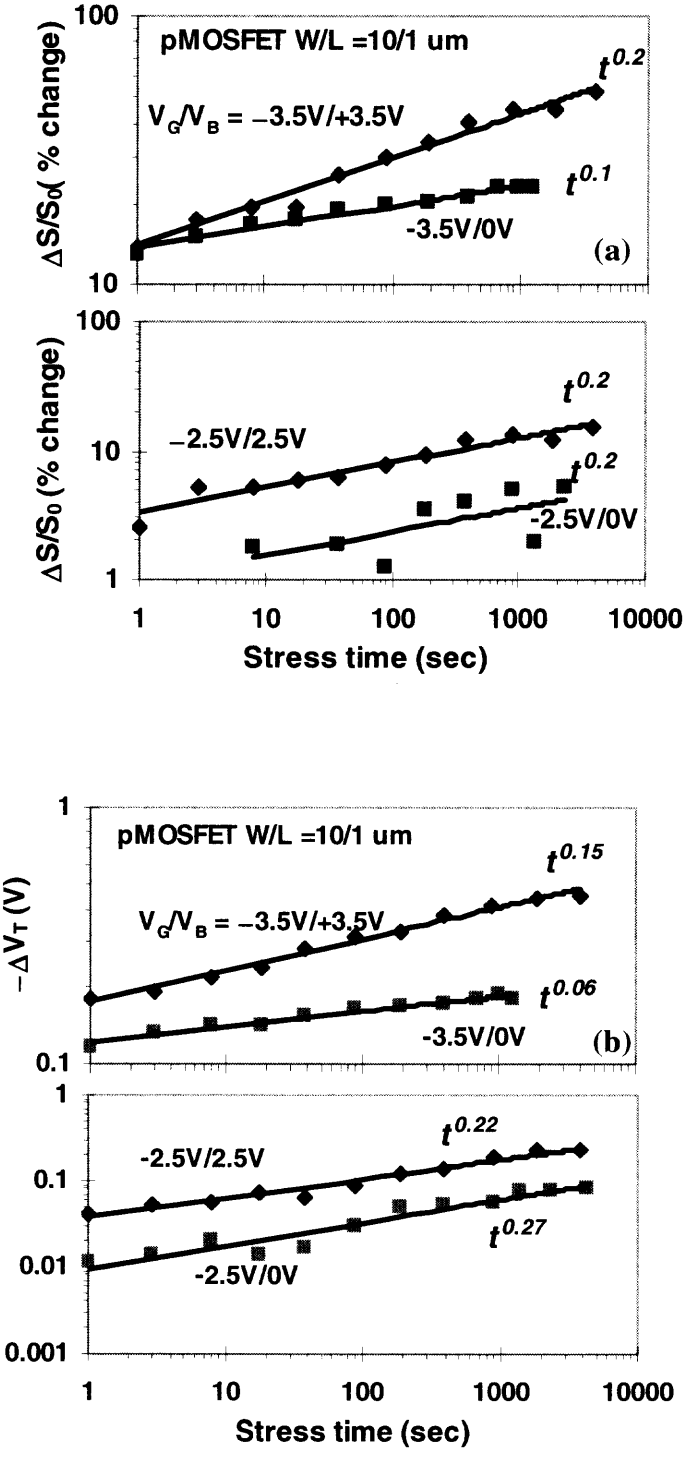


Figure 6.4 **(a)** $\Delta S/S_0$ and **(b)** ΔV_T for both zero and non-zero substrate bias conditions during CVS at RT.

It can be observed from Figure 6.4(b) that $|\Delta V_T|$ also follows t^n power-law dependence under all stress conditions. For $V_g = -2.5$ V stress level, n for ΔV_T is greater than that found for $\Delta S/S_0$ under both zero and non-zero V_b conditions. This indicates that besides interface states, positively charged bulk trap generation also take places [87]. For $V_g = -3.5$ V stress level, however, n for $|\Delta V_T|$ is lower than that for $\Delta S/S_0$ under both V_b conditions. Besides interface states and positively charged bulk trap generation, electron trapping may be slowing the increase of $|\Delta V_T|$, so that finally it saturates. This is consistent with the earlier studies [86], where it was observed that electron trapping at deep electron tarps was significantly high for high negative bias stress levels.

6.3 Stress at Elevated Temperatures

For stress at elevated temperature of 398K (125°C), it can be observed from Figure 6.5 that ΔV_T shows saturation for high bias conditions. However, for low bias conditions mixed degradation is still obvious.

To understand temperature dependence on degradation further, stress was carried out for both low and high stress conditions for extended period of time at different Elevated temperatures. It is obvious from Figure 6.6(a) that positive charge trapping is thermally activated for –2V. Initially positive charge trapping increases with time for each temperature condition; however it reaches saturation after ~300 secs of stress. Similarity in the patterns in Figures 6.6(a) and (b) suggests that

interface state generation and ΔV_T are highly correlated at elevated temperature conditions.

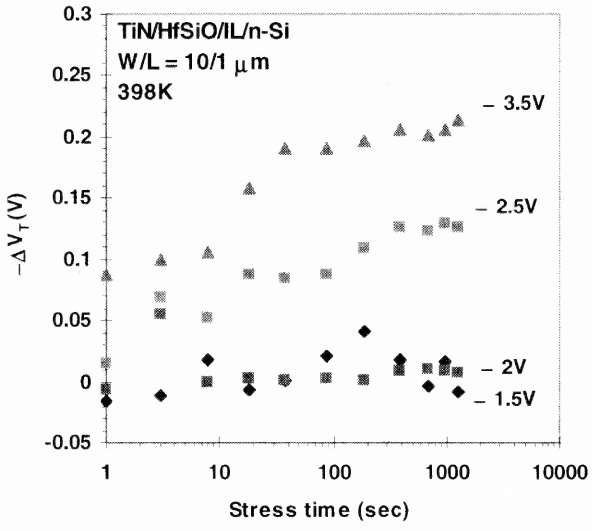


Figure 6.5 ΔV_T vs. stress time for different V_g at 398K (125°C) applied on pMOSFETS.

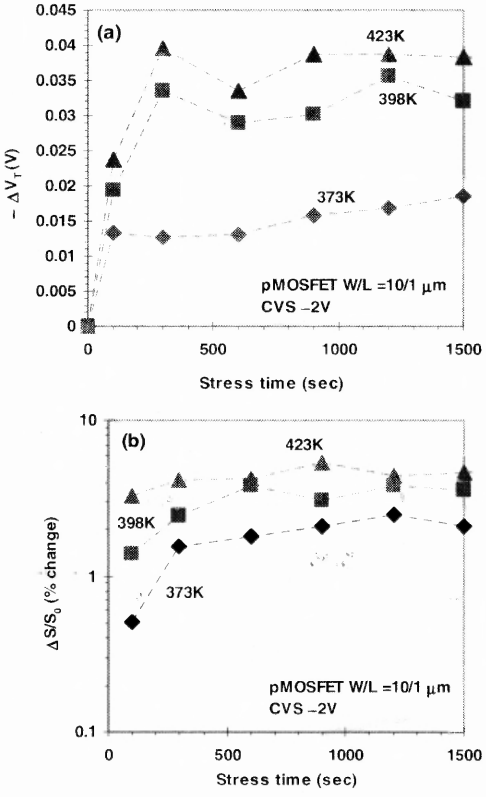


Figure 6.6 **(a)** ΔV_T and **(b)** $\Delta S/S_0$ for CVS with –2 V of stress level at elevated temperatures.

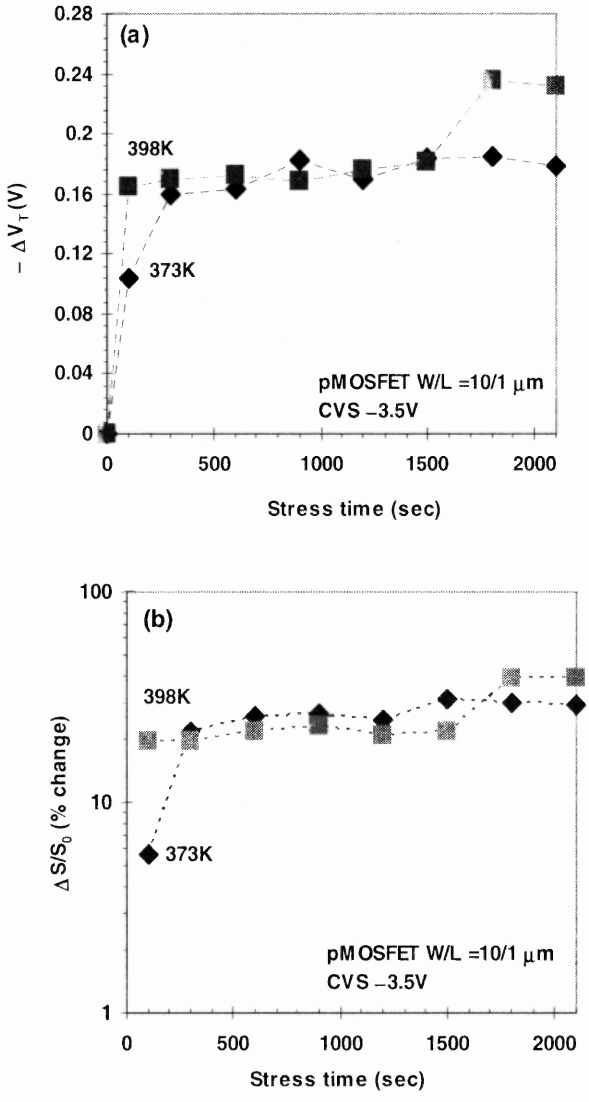


Figure 6.7 **(a)** ΔV_T and **(b)** $\Delta S/S_0$ for CVS with –3.5 V of stress level at elevated temperatures.

For –3.5 V, positive charge trapping reaches saturation earlier at elevated temperatures of 373K (100°C) and 398K (125°C), but initially it shows temperature dependence as shown in Figure 6.7(a). $\Delta S/S_0$ also shows a similar behavior (Figure 6.7(b)), which further implies the effect of the interface state generation on ΔV_T.

It is obvious from Figures 6 and 7 that at the initial stage of the stress, ΔV_T and $\Delta S/S_0$ not only depends on stress level but also temperature. In order to further understand these effects, ΔV_T and $\Delta S/S_0$ are plotted as a function of electric field (E_{ox}) for different elevated temperature conditions in Figures 6.8(a) and 8(b). Here, $E_{ox} = (V_g - V_{FB} - \Psi s)/EOT$, where Ψs is the surface potential. ΔV_T and $\Delta S/S_0$ were measured after 100s of uninterrupted CVS.

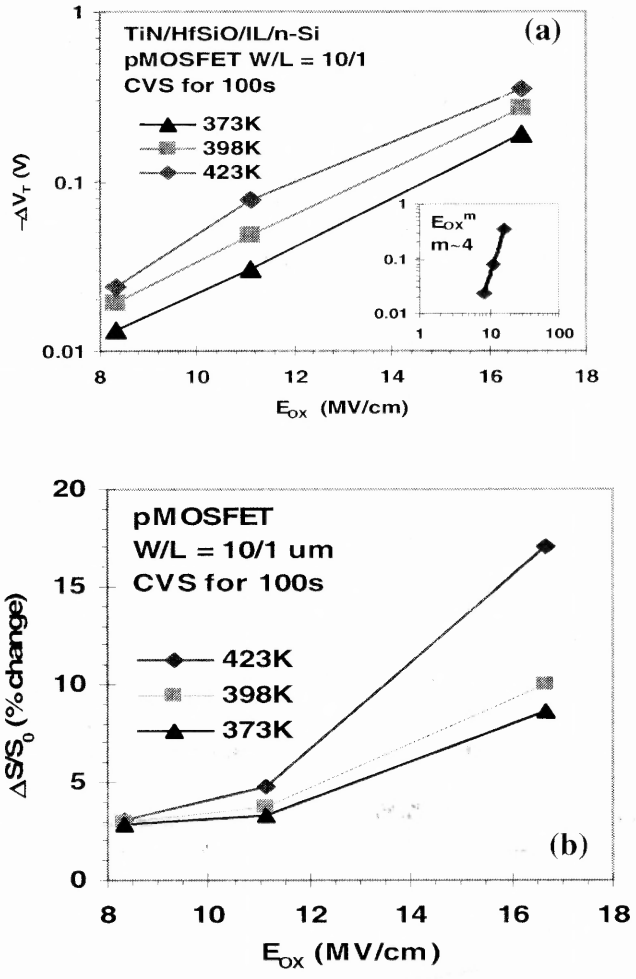


Figure 6.8 **(a)** ΔV_T and **(b)** $\Delta S/S_0$ vs. E_{ox} after initial 100s of CVS under different elevated temperatures conditions. **[Inset of (a)]** ΔV_T vs. E_{ox} at 423K (150°C).

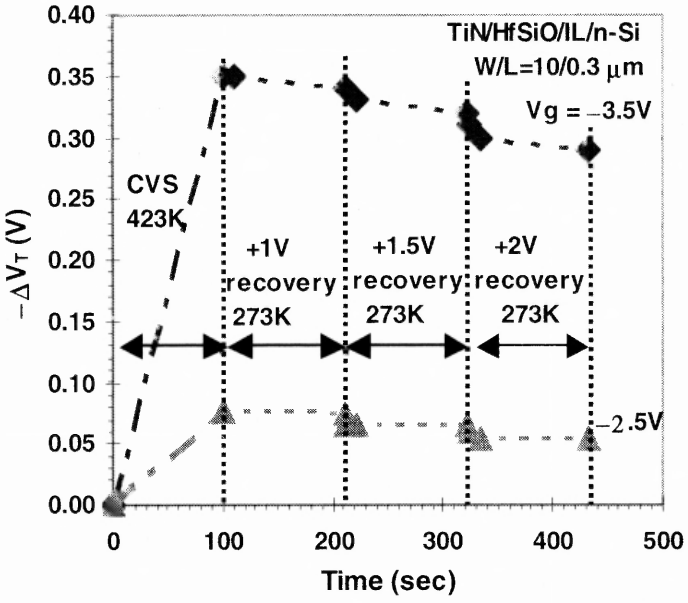


Figure 6.9 ΔV_T vs. time during CVS at 423K (150°C) with $V_g = -3.5$ V and -2.5 V, and post-stress recovery under different positive gate bias conditions.

For each field and temperature condition, a fresh device was used (total: 9). It can be observed that ΔV_T strongly depends on field and temperature conditions, specifically during the initial period of stress. Inset of Figure 6.8(a) shows that ΔV_T shows E_{ox}^{m} power-law dependence and for 423K, m ~ 4. For other temperatures, m is in the same range.

To understand post-stress recovery, injection of substrate electrons was done at different positive biases as shown in Figure 6.9. But it fails to neutralize $|\Delta V_T|$ for both –2.5 V and –3.5 V stress conditions, which suggests that H-species may be responsible for positively charged trap generation within the bulk [87].

Arrehnius plots of ΔV_T for different negative gate bias is shown in Figure 6.10. ΔV_T was measured after initial 100s of CVS with different stress level. For a particular stress and temperature condition, a fresh device was used to avoid the effects of the residual trapping. It is obvious that positive charge trapping is thermally activated in the gate stack, specifically at the initial stage of stress. For V_g = −3.5 V stress level, saturation of ΔV_T took place at less elevated temperatures. However, as temperature is raised thermal activation of positive charge build-up became obvious. Activation energies were found to be lying within 0.2 to 0.3 eV range.

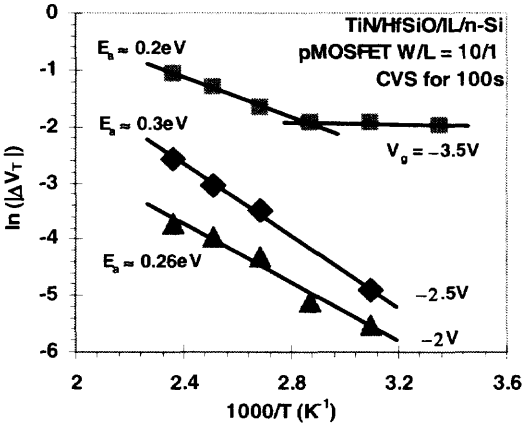


Figure 6.10 Arrhenius plots of ΔV_T for different gate bias. ΔV_T was measured after initial 100s of CVS.

6.4 Application of Reaction-Diffusion Model

Reaction-diffusion model of NBTI is based on net positive increment of interface states, N_{it} as two competing processes of Si-H bond breaking and annealing occur simultaneously [78]. The following equation describes this [78]:

$$\frac{dN_{it}}{dt} = k_f\left(N_0 - N_{it}\right) - k_r N_{it} N_H^{(0)} \tag{6.1}$$

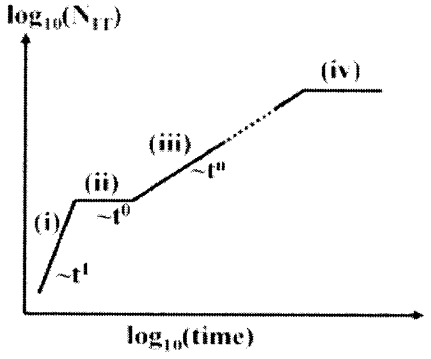


Figure 6.11 N_{it} vs. stress time as predicted by R-D model.
Source: [78]

Here, k_f / k_r: bond breaking/annealing rate, N_0: number of Si-H bond density prior to degradation, $N_H^{(0)}$: H-species density at Si/SiO_2 interface. Si-H bond breaking/annealing at the presence of holes is shown by the following electrochemical reaction:

$$Si - H + h^+ \Leftrightarrow Si\bullet + H^0 \tag{6.2}$$

Recent studies [85] show that energy of hole plays a role in bond-breaking and post-stress bond-annealing. For low energy holes, it is mostly $Si_3{\equiv}Si{-}H$ bonds are broken, and ΔN_{it} increases with a power-law exponent, $n \approx 0.2$ as stated earlier.

Moreover, a fraction of the broken $Si_3{\equiv}Si-$ bonds anneal after stress. For hot holes, besides $Si_3{\equiv}Si-$ species, $\equiv Si-O-$ defects are generated, which does not anneal after stress and raise the value of n to 0.2 to 0.5.

A closer inspection of R-D model, as shown in Figure 6.11 [78], reveals that initially (i) N_{it} increases by t^1 as $N_0 >> N_{it}$. (ii) When bond-breaking = bond-annealing, N_{it} increases by t^0. (iii) When H-species diffusion into the oxide dominates, N_{it} increases by t^n. (iv) Finally, when $N_{it} = N_0$, interface state generation stops.

It is also possible to explain time, temperature and field dependence of ΔV_T in a compact form, specifically for region (iii) in Figure 6.11. Phenomenological description of this dependence can be expressed in the following way [87]:

$$\Delta V_T = C E_{OX}^m \exp\left(\frac{-E_a}{k_B T}\right) t^{\alpha} \tag{6.3}$$

Here, C is a constant and k_B is Boltzmann's constant. For Si/SiO_2, it was found that $m \sim 3-4$, $E_a \sim 0.1-0.2$ eV and $\alpha \sim 0.2-0.25$. Comparison with the experimental results shows excellent match. This is why R-D model may be explored to interpret NBTI effects in these devices.

Initially the devices may not be in region (i) of Figure 6.11 since the initial D_{it} $\sim 1\times10^{12}$ ($cm^{-2}.eV^{-1}$). The experimental results in Figure 6. 4(a) show that initially the devices reside in region (iii). Moreover, it is supported by phenomenological model in Equation (3). While in region (iii), ΔV_T increases initially due to Si-H bond breaking, which results in both interface states and diffused H-species induced bulk

trap generation. Finally, however, ΔV_T tends to saturate. Migration to region (iv) due to usurping of all available Si-H bonds may be considered. But, Figure 6.7 shows that if stress-time is increased, more bond-breaking may occur, which increases both $\Delta S/S_0$ and ΔV_T for $V_g = -3.5V$ at 398K. Therefore, breaking of all Si-H bonds may not be the cause of saturation.

As stated earlier, lack of hot holes during CVS results in higher post-stress anneal of broken bonds [85], which may limit increase of ΔN_{it}, that is, $\Delta S/S_0$ and ΔV_T. It was experimentally observed that signatures of impact ionization induced hot

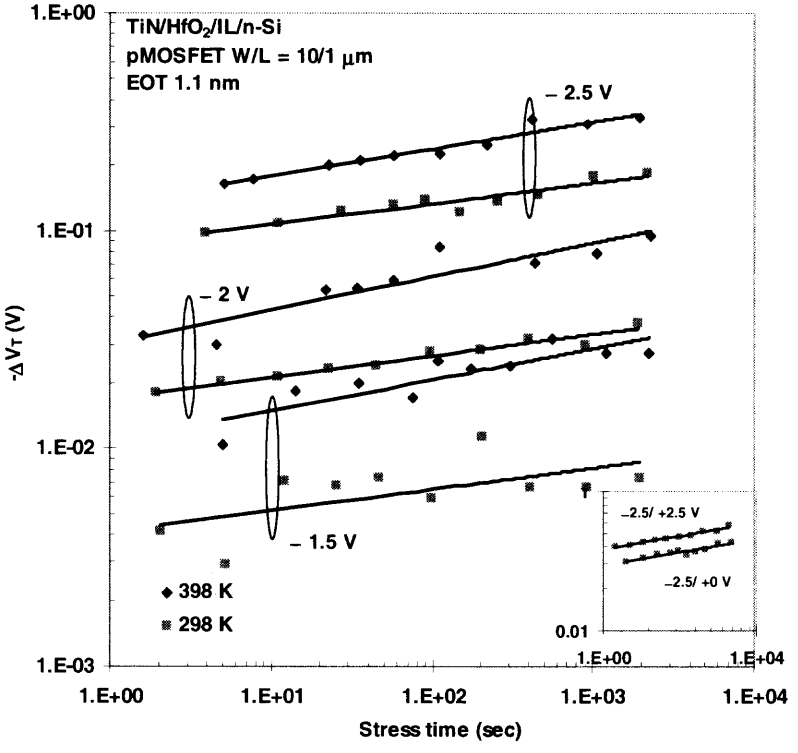


Figure 6.12 ΔV_T vs. stress time for CVS applied on pMOSFETs with TiN/HfO_2 based gate stacks under different negative bias and temperature (RT and 398 K) conditions. (**Inset**) ΔV_T vs. stress time plots for CVS under zero and non-zero substrate bias conditions at RT.

hole generation are absent even under the extreme stress conditions studied in this specific work. Moreover, the value power-law exponent, n ≈ 0.2 for $\Delta S/S_0$ also implies that low energy hole induced Si-H bond breaking dominate in this case. Based on this, it may be argued that bond-annealing due to low energy hole induced Si-H bond breaking, the number of which declines with the progress of stress, is possibly the cause of the tendency of $\Delta S/S_0$ and ΔV_T to saturate under a particular bias temperature stress condition.

To further understand the results CVS was applied on ALD deposited TiN/HfO_2 based gate stacks (with 26A HfO_2 and 11A of IL) at room and elevated (398 K) temperatures. It is obvious from Figure 6.12 that dependence of ΔV_T on stress time follows the power-law with exponent ~ 0.1. This low value of n may be due the increased negative charge trapping within the bulk oxide. Moreover, ΔV_T depends on temperature and gate bias, i.e., electric field conditions. Furthermore, inset of Figure 13 shows that positive charge trapping increases with non-zero substrate bias. These results conform to the earlier observations of the NBTI effects on TiN/Hf-silicate based gate stacks.

6.5 Summary

NBTI effects under different bias and temperature conditions were studied for TiN/$HfSi_xO_y$ (20% SiO_2) based high-κ gate stacks. For low bias conditions, mixed degradation due to both electron and hole trapping within the bulk high-κ mostly dominates ΔV_T. Interface state generation, observed from change in sub-threshold slope, $\Delta S/S_0$, was found to be negligible. For moderately high to high stress levels, initially Si-H bond breaking induced interface sates and diffused H-species induced bulk trap generation dominates. Initial temperature, time and oxide electric field dependence shows excellent match with that of R-D based NBTI model. Carrier separation technique shows that impact ionization induced hot hole generation, signature being the reversal of the polarity of source/drain current during stress, was not observed. This possibly results in higher bond-annealing/bond-breaking ratio as, with the progress of the stress, less number of bonds are available to be broken at the presence of low energy holes. This may be responsible for the observed saturation of interface state generation and ΔV_T under high bias temperature stress conditions.

CHAPTER 7

BREAKDOWN CHARACTERISTICS OF GATE STACKS

7.1 Introduction

In order to understand the breakdown mechanisms under substrate injection, ramped and constant voltage stress (RVS and CVS) were applied on atomic layer deposited (ALD) TiN/HfO_2 based nMOS devices in inversion regime. To determine relative roles of IL and high-κ layer in TZBD and TDDB, three lots of samples with splits of different IL and high-κ thickness (t_{IL} and $t_{H\text{-}K}$) combinations [lot 1: variable t_{IL} (0 .7 nm/1.1 nm) and $t_{H\text{-}K}$ (2.6/2.7/3.3 nm); lot 2: for fixed $t_{H\text{-}K}$ (3nm), different t_{IL} (0.7/1.1/2.1 nm); lot 3: for fixed t_{IL} (1.1 nm), different $t_{H\text{-}K}$ (3/5/7/10 nm)] were used. Moreover, IL breakdown field, E_{BD}^{IL} is compared for samples with and without pre-deposition surface treatment with NH_3 (lot 2), and different IL growth conditions [lot 2: HF-last and in-situ steam generated, ISSG; lot 3: chemically grown SiO_x and ISSG]. In order to compare $E_{BD}^{H\text{-}K}$ and E_{BD}^{IL} with BD fields of high-κ and SiO_2 films, respectively, RVS was also applied on HfO_2-based MIM (metal/insulator/metal) structures [4 nm ALD $HfSi_xO_y$ (10% SiO_2)] and SiO_2 based MOS devices (1.6 nm ISSG) with TiN metal gates and equivalent processing conditions. The major points reported in Chapter 7 are (1) for thin high-κ layer (≤ 3.3 nm), IL controls TZBD; otherwise, high-κ layer controls it, (2) for a fixed t_{IL}, E_{BD}^{IL} does not depend on pre-deposition surface treatment, however, its value degrades in the following order: 2.1 nm ISSG, 1.1 nm ISSG, 1.1 nm chemical SiO_x, 0.7 nm ISSG,

and HF-last, (3) four regimes of degradation are observed under CVS with high gate bias condition: charge trapping/defect generation, soft breakdown (SBD), progressive breakdown (PBD), and hard breakdown (HBD), (4) the degradation of IL triggers the breakdown of the entire gate stack, and (5) the quality of IL strongly affects time-to-breakdown (T_{BD}) of Hf-based high-κ gate stacks.

7.2 Calculation of E_{BD}^{IL} and $E_{BD}^{H\text{-}K}$

Ramped voltage stress was applied on n^+-ringed nMOS-C from lots 1, 2 and 3 to determine E_{BD}^{IL} and $E_{BD}^{H\text{-}K}$. For a given gate bias condition, fields across I L and high-κ layer are calculated from the following Equations [88]:

$$V_{OX} = E_{H-K} \times T_{H-K} \times \left(1 + \frac{EOT_{IL}}{EOT_{H-K}}\right) \tag{7.1}$$

$$V_{OX} = E_{IL} \times T_{IL} \times \left(1 + \frac{EOT_{H-K}}{EOT_{IL}}\right) \tag{7.2}$$

Here, V_{OX} is the voltage across the gate stack, $E_{H\text{-}K}$ and E_{IL} are fields across, $T_{H\text{-}K}$ and T_{IL} are the physical thickness, and $EOT_{H\text{-}K}$ and EOT_{IL} are the effective oxide thickness of high-κ and interfacial layers, respectively.

Interfacial layer quality depends on the growth condition and thickness [88]-[89]. In particular, the IL κ value was found to increase due to an influence of the high-κ film and gate electrode. High-field (~ 1 MV/cm) mobility plots of high-κ gate stacks show a considerable dispersion from the universal mobility plot of SiO_2 as

depicted in Figure 7.1. It was reported in [90]-[94] that this dispersion increases as IL quality decreases.

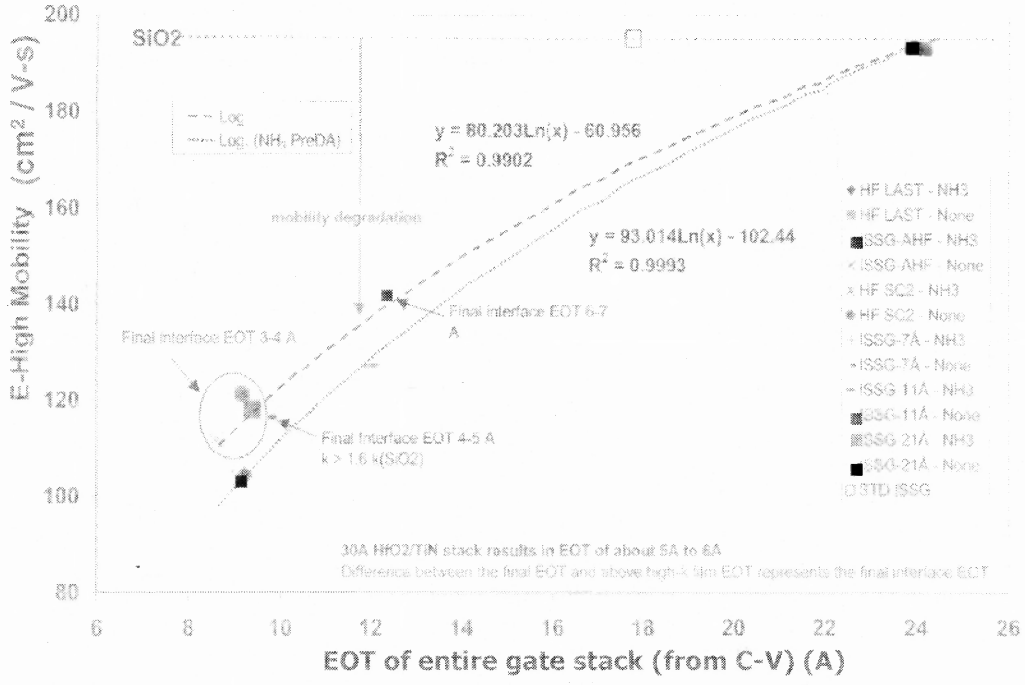


Figure 7.1 High-field (~1 MV/cm) mobility vs. final EOT of TiN/3nm HfO_2/IL/p-Si gate stacks for different IL growth conditions.

Moreover, for the same physical thickness of IL and high-κ layer, EOT of the entire gate stack, found from NCSU CVC program [4], is shown to decrease with the inferior IL quality. The EOT values of ILs were determined by subtracting $EOT_{H\text{-}K}$ (Final $EOT_{gate\ stack}$ = Final EOT_{IL} + $EOT_{H\text{-}K}$), which were determined for these high-κ films in the previous studies. In all splits (besides 2.1 nm ISSG), IL re-grew to the final post-processing thickness of 1.1 nm, as verified by HRTEM [3]. An exception is the getterred IL of 0.7 nm, whose thickness remained unchanged [3], because the

Table 7.1 Physical Thickness and Effective Oxide Thickness (EOT) for Different Interfacial Layers (IL) Growth Conditions

IL	$T_{physical}$ (nm)	EOT (nm)
2.1 nm ISSG	2.1 nm	2.0 nm
1.1 nm ISSG	1.1 nm	0.7 nm
1.1 nm Chem SiO_x	1.1 nm	0.7
1.1 nm HF-last	1.1 nm	0.4 nm
0.7 nm ISSG	1.1 nm	0.5 nm
0.7 nm getterred	0.7 nm	0.5 nm

scavenging of O from IL was done after high-κ deposition. It is, therefore, concluded that EOT of IL is significantly different from SiO_2 and it depends on growth condition and thickness [95] as shown in Table 7.1. The table also shows the final physical thickness of IL. The higher the EOT the more stoichiometric is the SiO_2 layer and, presumably, the better the IL quality.

For given bias and split conditions, E^{H-K} and E^{IL} (Figure 7.2 inset) can be calculated from Equatios (7.1) and (7.2) by using the values from Table 7.1. As an example, calculated E^{H-K} and E^{IL} for three splits of fixed t_{IL} but different t_{H-K} from lot 3 are plotted with respect to the gate bias in Figure 7.2. It is obvious from the Figure 7.2 that for a given increment in V_g, increment in E^{H-K} and E^{IL} is higher for lower t_{H-K}.

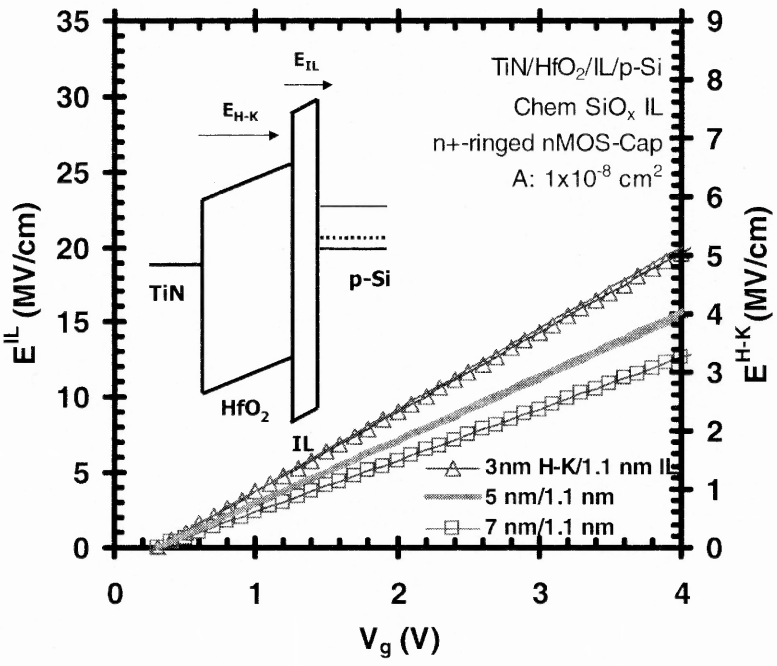


Figure 7.2 Distribution of fields across IL (E_{IL}) and high-κ layer ($E_{H\text{-}K}$) for a given stress bias. (**Inset**) Band diagram of the gate stack under positive gate bias condition.

7.3 E_{BD} of SiO_2 based MOS and HfO_2 based MIM Structures

To study TZBD characteristics of TiN/ HfO_2 based gate stacks field strength of both IL and high-κ layer need to be understood. For comparison purposes, field strengths of SiO_2 and high-κ can be experimentally found directly from SiO_2 based MOS and HfO_2 based MIM structures of equivalent thickness, and growth and anneal conditions. MIM-Capacitors (MIM-C) are particularly chosen to avoid the presence of the interfacial layer associated with Si substrate [96].

Figure 7.3 shows I-V characteristics for RVS applied on n^+-ringed nMOS-C under inversion condition (substrate injection). The n^+-ring was grounded to avoid the minority carrier shortage. Instantaneous increase of I_g by an order of magnitude is

considered as hard breakdown (HBD). Voltage across oxide, $V_{ox} = V_g - V_{FB} - \phi_s$, where ϕ_s is the surface potential. For bulk doping density $\approx 10^{17}$ cm^{-3}, $V_{FB} \approx -0.7$ V (determined from NCSU CVC program [4]), and breakdown voltage, $V_{BD} \approx 3.0$ V, $E_{BD}^{SiO2} \approx 17$ MV/cm, which is comparable to the theoretical value of 15 MV/cm [97].

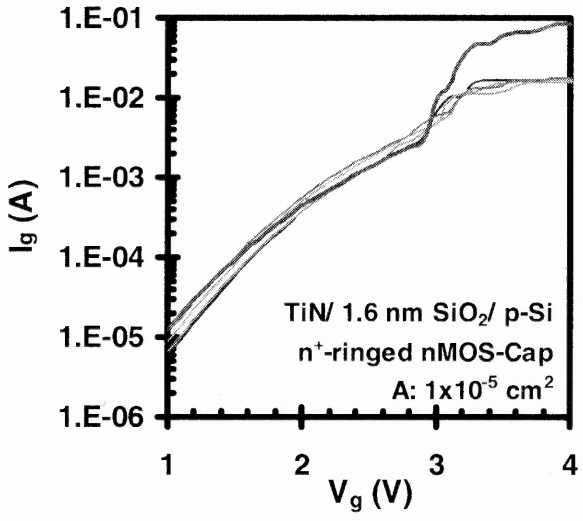


Figure 7.3 I-V characteristics under ramped voltage stress (RVS) applied on SiO_2 based n^+-ringed nMOS-C.

Figure 7.4 shows TZBD characteristics of MIM-C with 4 nm $HfSi_xO_y$ (10% SiO_2) as insulating materiel. $E_{BD}^{HfSiO} \approx 6.5$ MV/cm, which is comparable to the theoretical value of 7 MV/cm for HfSiON [89]. McPherson showed that $E_{BD} \propto \kappa^{-0.5}$ [1]. For Hf-silicate, $\kappa \approx 10$ to 15 [89], and for HfO_2, $\kappa \approx 25$; consequently, E_{BD}^{HfO2} may be expected to be from 4 to 5 MV/cm in these films. This is within the theoretical limits of 3.9 to 6.7 MV/cm [89]. In Section 7.4, experimentally observed values of E_{BD}^{IL} and E_{BD}^{H-K} will be shown for the various gate stacks, and compared with, E_{BD}^{SiO2} and E_{BD}^{HfO2}.

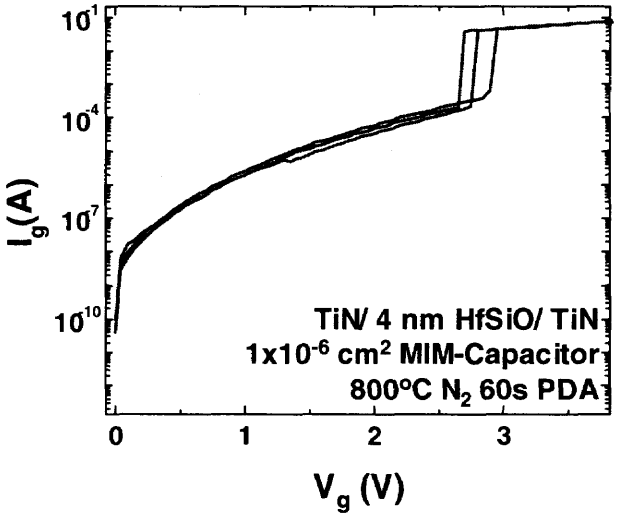


Figure 7.4 I-V characteristics under RVS applied on $HfSi_xO_y$ (10% SiO_2) based MIM capacitors. $E_{BD} \approx 6.5$ MV/cm is comparable with the theoretical value of ~ 7 MV/cm.

7.4 TZBD Characteristics

7.4.1 Lot 1

For lot 1, I-V characteristics of devices from split 1 ($t_{H\text{-}K}/t_{IL}$: 2.6 nm/1.1 nm) of lot 1 were plotted for different gate areas in Figure 7.5(a). The excellent scaling of gate current density, J_g with area, which is also observed for all the other splits, indicates the good uniformity of the gate oxide, and the absence of the peripheral current [95]. The 50% failure value of V_{BD} is shown in Figure 7.5(b) for different area and split conditions of lot 1. V_{BD} is observed to decrease with increase in area, specifically for splits 1 (2.6 nm/ 1.1 nm) and 3 (3.3 nm/ 1.1 nm). It may due to the uniform distribution of weak spots with respect to area. For the rest of the experiments, devices with the smallest areas were used.

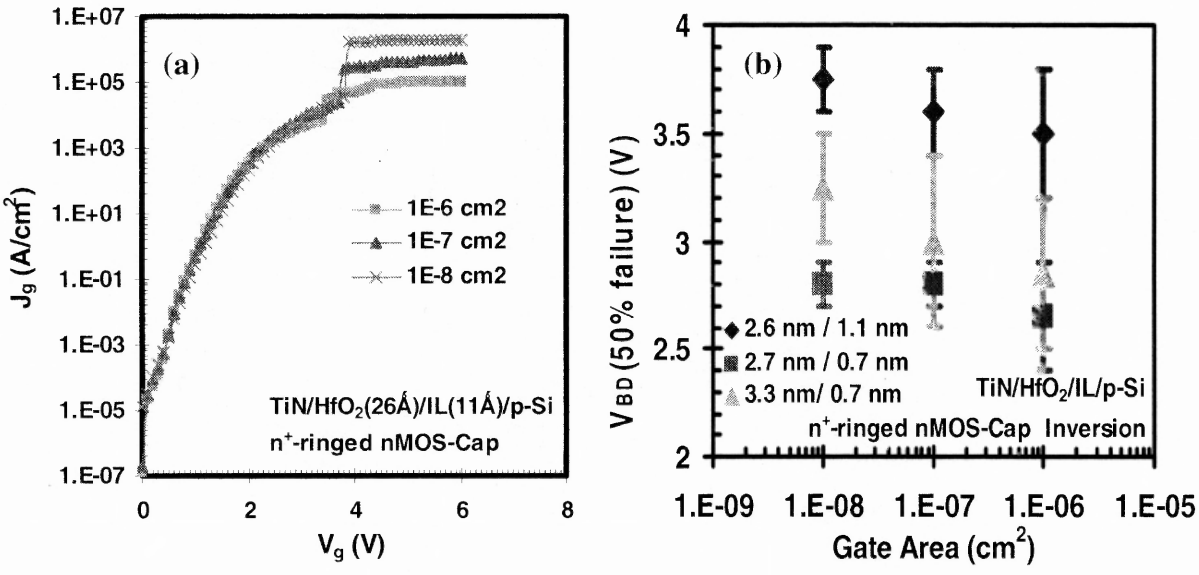


Figure 7.5 **(a)** I-V characteristics under RVS applied on n^+-ringed nMOS-C with gate stacks from split 1 of lot 1 (2.6 nm HfO_2 / 1.1 nm IL) for different area conditions. **(b)** 50% failure value of breakdown voltage, V_{BD} vs. area for different splits of lot 1.

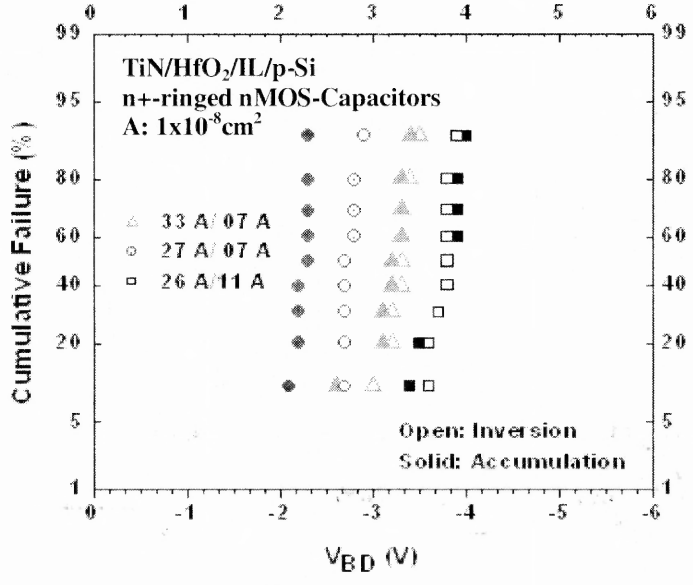


Figure 7.6 Cumulative failure distribution of V_{BD} for different splits in lot 1 under inversion and accumulation conditions.

To understand the effect of the polarity on V_{BD}, RVS was applied under both inversion and accumulation regimes for the devices in lot 1. Cumulative % failure distribution plots of V_{BD} are shown in Figure 7.6 for different splits of lot 1. Little dispersion in the distribution of a given gate stack under a given polarity supports the earlier observation regarding the uniformity of the gate stacks as far as thickness and growth conditions are concerned. Moreover, uniform failure distribution also implies that BD is intrinsic. For the gate stacks, $V_{ox} \approx V_g - 0.4$ V under inversion, and $V_{ox} \approx V_g + 0.5$ V under accumulation. Therefore, to maintain the same BD fields in each layer under both of the polarities, $V_{BD,accumulation} \approx V_{BD,inversion}$. A negligible dispersion in V_{BD} between accumulation and inversion conditions, observed for splits 1 (2.6 nm/ 1.1 nm) and 3 (3.3 nm/ 1.1 nm), supports this. Dispersion, however, is observed for split 2 (2.7 nm/ 0.7 nm). This may be due to the presence of a large

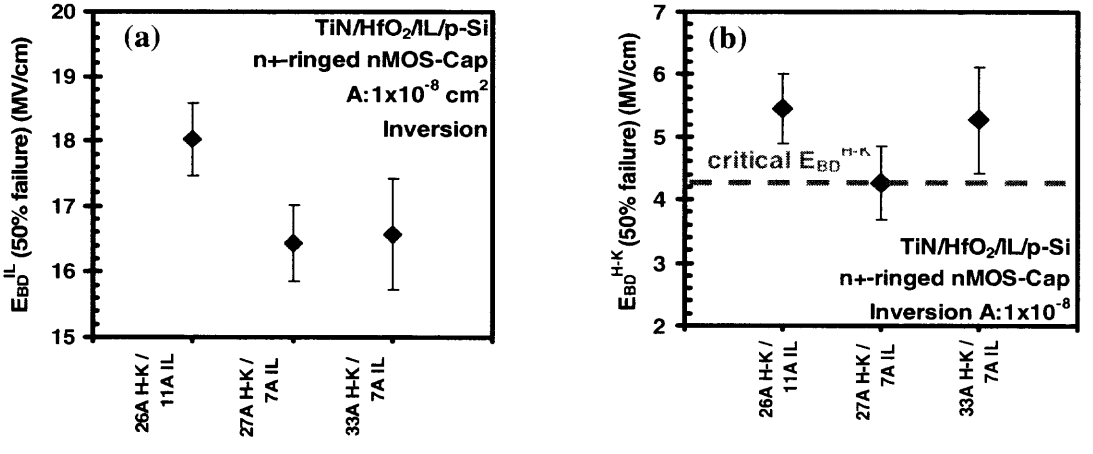


Figure 7.7 Fifty percent failure value of **(a)** E_{BD}^{IL} and **(b)** $E_{BD}^{H\text{-}K}$ under inversion for different splits of lot 1. High-κ layer BD occurs first followed by IL, which triggers gate stacks BD.

number of weak spots, which possibly is responsible for the weak area scaling of the devices from split 2.

Under inversion condition, E_{BD}^{IL} and E_{BD}^{H-K} were calculated, as shown in Figure 7.7(a) and (b), respectively, for the splits in lot 1 by using V_{BD} values at 50% cumulative distribution in Figure 7.6. Similarly, E_{BD}^{IL} and E_{BD}^{H-K} were calculated for the splits in lot 1 by using V_{BD} values in Figure 7.6 and are shown in 7.8(a) and (b), respectively. For all splits specifically under inversion condition, it can be easily

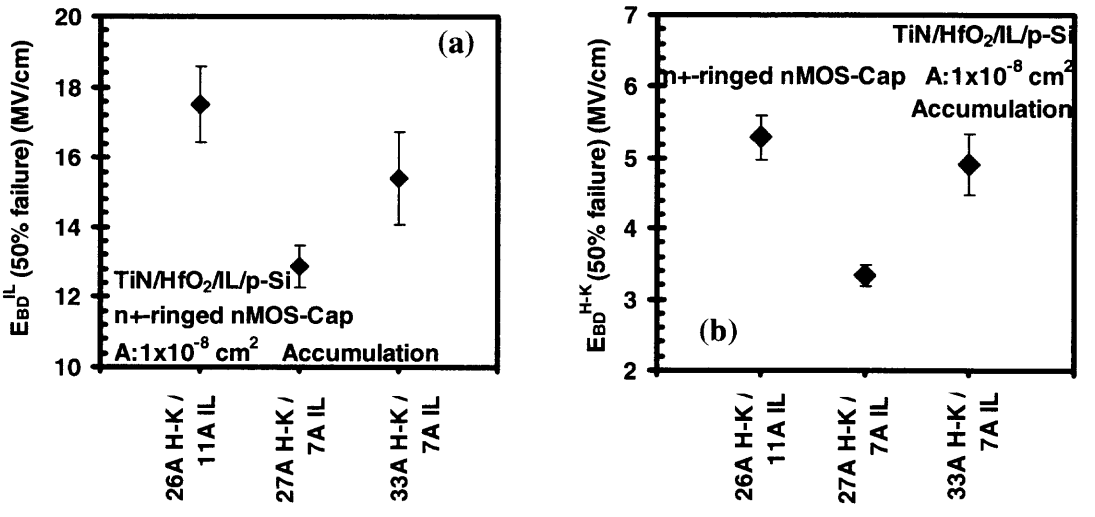


Figure 7.8 Fifty percent failure value of **(a)** E_{BD}^{IL} and **(b)** E_{BD}^{H-K} under accumulation for different splits of lot 1.

observed that both E_{BD}^{IL} and E_{BD}^{H-K} are almost equal to or above the experimental/theoretical values. It may, therefore, be concluded that BD of both the layers occur as gate stacks breakdown. As far as inversion and accumulation regimes are concerned, for splits 1 (2.6 nm / 1.1 nm) and 3 (3.3 nm/ 1.1 nm) E_{BD}^{IL} and E_{BD}^{H-K}

show negligible differences. But, significant differences are observed for split 2 (2.7 nm/ 0.7 nm).

Thermochemical model of breakdown, explained in Equation 7.3, was shown to successfully predict E_{BD} for different dielectric materials [89]:

$$E_{BD} = \frac{\Delta H_0^*}{p_0\left(\frac{2+\kappa}{3}\right)} \tag{7.3}$$

where, ΔH_0^* is the activation energy of bond-breaking in the absence of the externally applied field, p_0 is the active molecular dipole-moment component opposite to the applied field, and κ is dielectric constant. If there is a weak molecular bond then field-enhanced thermal breakage of the bond becomes much easier and faster [90]. The capture of a hole further weakens the weak bond with an energy level much above the nominal valence band. Thus, hole capture effectively reduces ΔH_0^* [90], which gives rise to an even easier bond breakage under high field conditions.

For high-κ nMOS-C with metal gate under inversion, anodic hole injection does not occur. As a result, BD is mostly field driven. Under accumulation, hole injection from the substrate side cannot be ruled out for the thin gate stacks. For split 2 (2.7 nm/ 0.7 nm), significant presence of weak bonds in both IL and high-κ layer may be responsible for the low BD fields. For this reason, V_{BD} under inversion conditions are used henceforth to analyze the field strengths of the layers in the high-κ gate stacks. V_{BD} under accumulation, on the other hand, can be probed to understand the quality of gate stacks.

It is obvious from Figure 7.7(a) that E_{BD}^{IL} varies according to the quality of IL, E_{BD} of ISSG (split 1) being better than getterred IL (splits 2 and 3). E_{BD}^{IL} is almost same for the splits with the equivalent IL. For the same quality of high-κ, however, such uniformity in E_{BD}^{H-K} is not observed. E_{BD}^{H-K} is quite different for the almost equivalent high-κ layers of splits 1 (2.6 nm/ 1.1 nm) and 2 (2.7 nm/ 0.7 nm). This implies that the high-κ layer possibly breaks first as E^{H-K} reaches the critical BD value of ~ 4 MV/cm due to the specifics of voltage division. This, however, does not immediately breaks the entire gate stack as at that instance, $E^{IL} \neq E_{BD}^{IL}$. As V_g is ramped further, E^{IL} reaches E_{BD}^{IL}, which triggers BD of the gate stack.

7.4.2 Lot 2

In order to understand the effects of IL quality and thickness, and PreDA conditions on TZBD characteristics of the high-κ gate stacks, RVS was applied on devices from

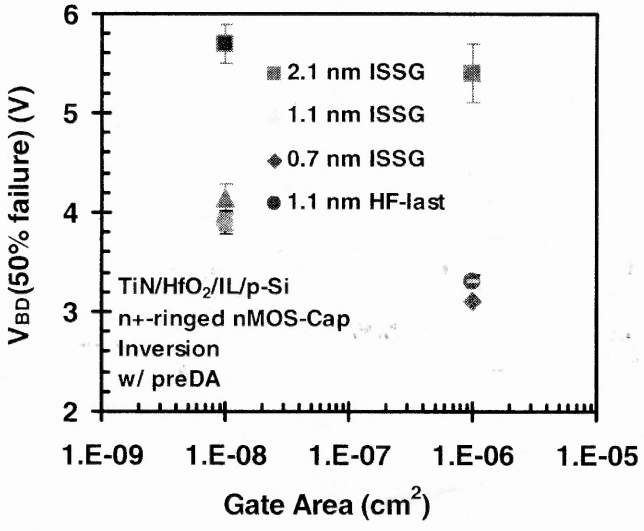


Figure 7.9 Fifty percent failure value V_{BD} vs. area for different splits of lot 2 with PreDA. Strong area dependence is observed.

the different splits in lot 2. 50% failure value of V_{BD} for splits with PreDA conditions (splits 2, 4, 6 and 7) shows good uniformity in weak spots distribution as depicted in

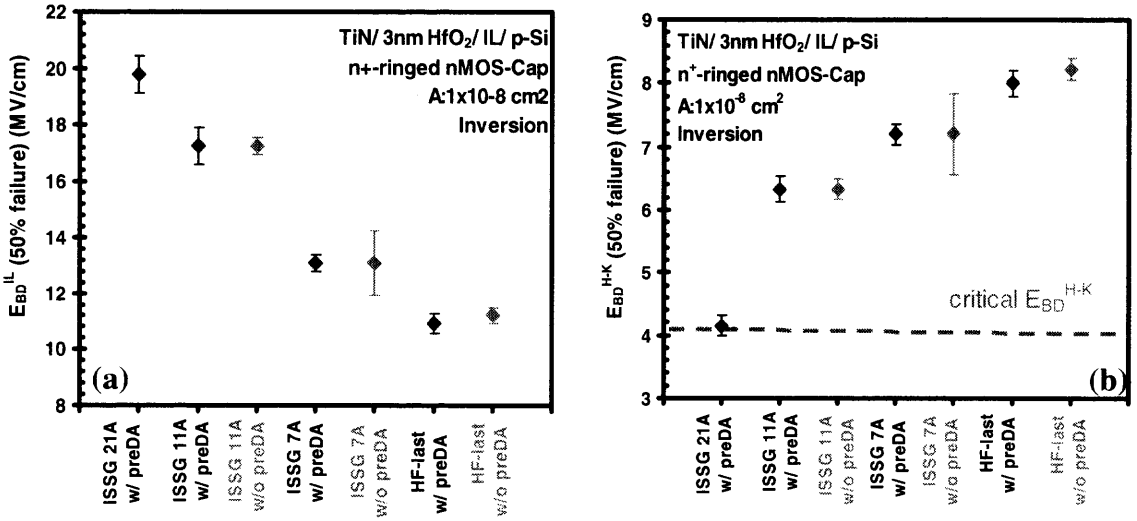


Figure 7.10 Fifty percent failure value of **(a)** E_{BD}^{IL} and **(b)** $E_{BD}^{H\text{-}K}$ under inversion for different splits of lot 2.

Figure 7.9. For splits without PreDA, similar characteristics are observed (not shows here). E_{BD}^{IL} and $E_{BD}^{H\text{-}K}$ under inversion are plotted in Figures 7.10(a) and (b), respectively for all the splits. The observed split-to-split trend of the E_{BD}^{IL} values is again consistent with the IL quality, 2.1 nm ISSG being the best followed by 1.1 nm ISSG, 0.7 nm ISSG and HF-last. Since V_{BD} values are recorded when both IL and high-κ layer are broken, data in Figure 7.10 indicates that even at $E^{H\text{-}K} > E_{BD}^{H\text{-}K}$ (intrinsic), breakdown is not observed until IL breaks (assuming similar high-κ quality for the same $t_{H\text{-}K}$). In the case of thin high-κ, IL controls the TZBD breakdown voltage since $E^{H\text{-}K}$ reaches the critical $E_{BD}^{H\text{-}K}$ value first (before E^{IL} reaches E_{BD}^{IL} while BD is not observed until $E^{IL} > E_{BD}^{IL}$) due to the specifics of the

voltage division between the high-κ and IL in the gate stack. Therefore, it is concluded that high-κ breaks first followed by IL. It may be further noted that pre-deposition surface treatment has no effect on the strength of the breakdown fields as far as inversion condition is concerned.

To understand the effect of PreDA on IL further, cumulative failure distributions of splits under accumulation and inversion conditions are plotted for cases of without and with PreDA in Figures 7.11(a) and (b), respectively. Irrespective of whether PreDA was performed or not, dispersion between accumulation and inversion conditions is small for 1.1 nm ISSG and 0.7 nm ISSG; whereas large dispersion is observed for the case of HF-last. It is expected because dispersion is a signature of IL quality. It is obvious that PreDA has almost no effect in reducing dispersion or increasing field strength, i.e., improving the quality of IL.

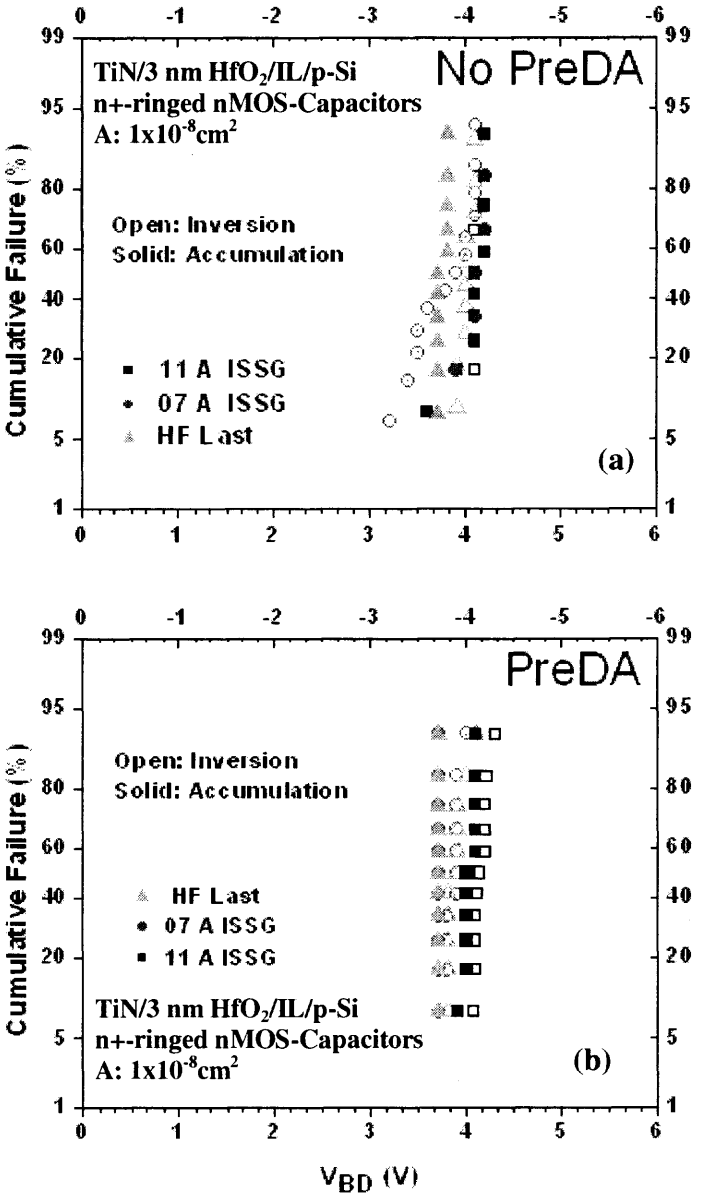


Figure 7.11 Cumulative failure distribution of V_{BD} for splits of lot 2, having **(a)** no PreDA, and **(b)** PreDA.

7.4.3 Lot 3

In order to understand the effects of high-κ thickness on TZBD characteristics of the gate stacks with both ISSG and chemical SiO_x IL, RVS was applied on the devices from lot 3. E_{BD}^{IL} and $E_{BD}^{H\text{-}K}$ are plotted for all the splits in Figures 7.12(a) and (b),

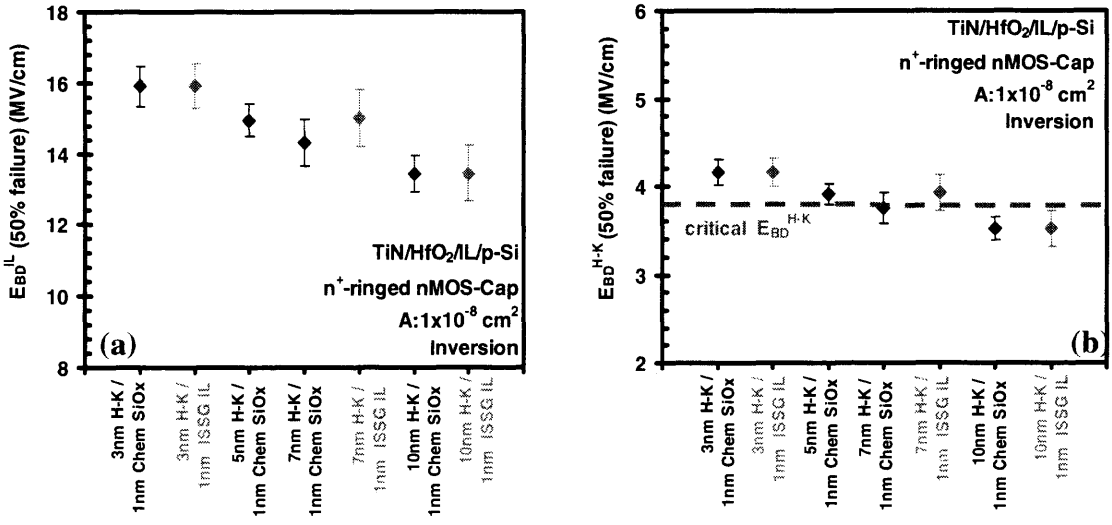


Figure 7.12 Fifty percent failure value of **(a)** E_{BD}^{IL} and **(b)** $E_{BD}^{H\text{-}K}$ under inversion for different splits of lot 3.

respectively. Even under different $t_{H\text{-}K}$ conditions, $E_{BD}^{H\text{-}K}$ is almost equal to the critical BD value of ~ 4 MV/cm for all splits. Slightly higher value of $E_{BD}^{H\text{-}K}$ is expected for thinner layers because TZBD characteristics of HfO_2 based MIM capacitors show a discernible decrease in BD field with increase in $t_{H\text{-}K}$ (to be published elsewhere by Krishnan et al.). For the same t_{IL} condition, E_{BD}^{IL} decreases with $t_{H\text{-}K}$. This is consistent with the observation that IL quality decreases with

increasing $t_{H\text{-}K}$ [95]. For split 2 (3nm HfO_2/1.1 nm ISSG IL), $E_{BD}^{IL} \approx 16$ MV/cm,

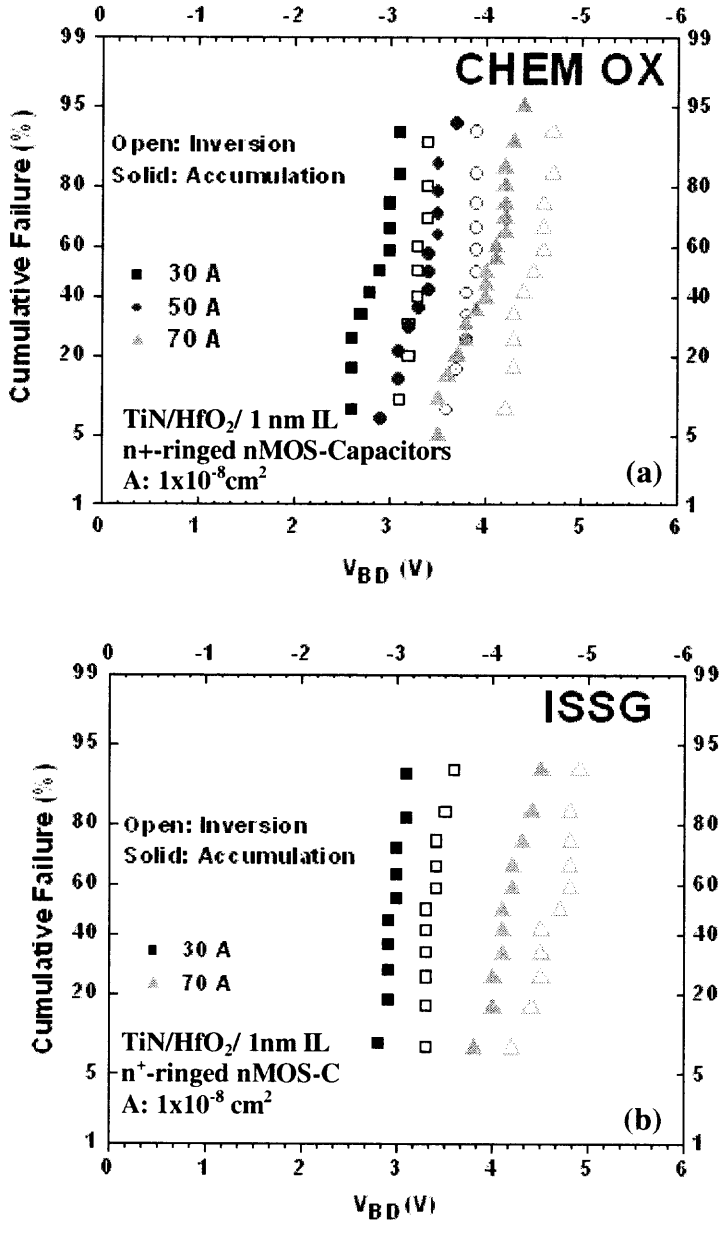


Figure 7.13 Cumulative failure distribution of V_{BD} for splits of lot 3, having **(a)** chemical SiO_x, and **(b)** ISSG IL.

which is comparable with the equivalent gate stacks in the other lots. It is concluded that as gate voltage is ramped, E_{BD} reaches critical E_{BD}^{IL} first, which breaks IL. Further application of the ramp voltage gives rise to an almost uniform $E_{BD}^{H\text{-}K}$ at hard breakdown instance, and, thus, gate stack BD occurs. It can be further observed that chemical SiO_x and ISSG ILs have similar E_{BD}^{IL} for a given $t_{H\text{-}K}$.

Cumulative failure distributions of V_{BD} under accumulation and inversion conditions are shown for chemical SiO_x and ISSG IL conditions in Figures 7.13(a) and (b), respectively. Significant dispersion can be observed for all split conditions under consideration. For lot 1 and 2 PDA was done at 600°C in N_2 ambient; whereas, for lot 3 it was done at 700°C in NH_3 ambient. Comparison of equivalent splits from the other lots implies that the observed dispersion may be due to the effect of PDA.

7.5 Wear-out Regimes during TDDB

To study TDDB under inversion, CVS was applied with high positive gate gate bias on n^+-ringed nMOS-C devices from lot 1. I-t characteristics show four regimes of degradation as shown in Figure 7.14. Stress was periodically interrupted to measure I-V, which is plotted in the inset of Figure 7.14. Initially charge trapping at pre-existing and stress-induced defects dominates, which distorts the internal the internal electric field and causes gate current to decrease with time [96]. The presence of a large number of pre-existing electrically active ionic defects in high-κ oxides, which are responsible for transient trapping, is widely known [95], [97], [98]. Relaxation induced detrapping occurs during periodic interrupts, which results in jump in I_g after

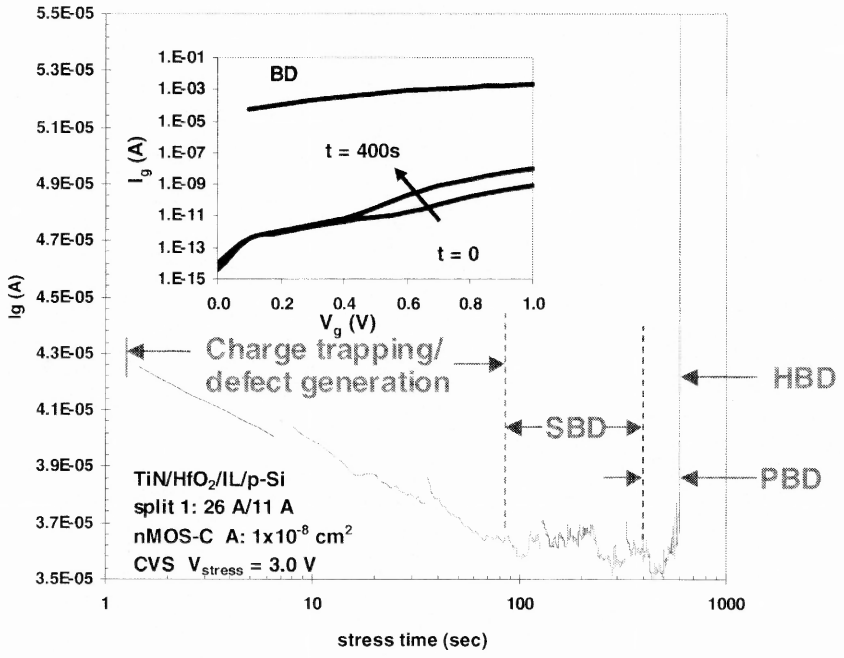


Figure 7.14 I-t characteristics of split 1 of lot 1 under CVS with positive gate bias. Different degradation regimes during TDDB are specified. (**Inset**) I-V characteristics during TDDB.

interrupt as shown by arrow in Figure 7.14. But, detrapping could not fully recover I_g as defect generation also took place. This is further confirmed by the increase in SILC, i.e., I_g sensed at low V_g (Inset of Figure 7.14) during stress.

Sudden sharp jumps and increased noise in I_g mark the soft breakdown (SBD) regime. Temporary percolating paths are formed; however, they do not stabilize to fully conducting paths [99]. This is followed by progressive breakdown (PBD) regime, which is characterized by the continuous increase in I_g leading to HBD. Progressive BD is a well understood phenomena for SiO_2 less than 2.5 nm thick. During PBD the aging of the percolating path occurs due to the defect generation around it. As such, percolating path becomes more ohmic and ultimately bridge

anode and cathode with a stable conduction path, which results in the thermal runaway current leading to HBD. I-V plots also confirm the catastrophic breakdown.

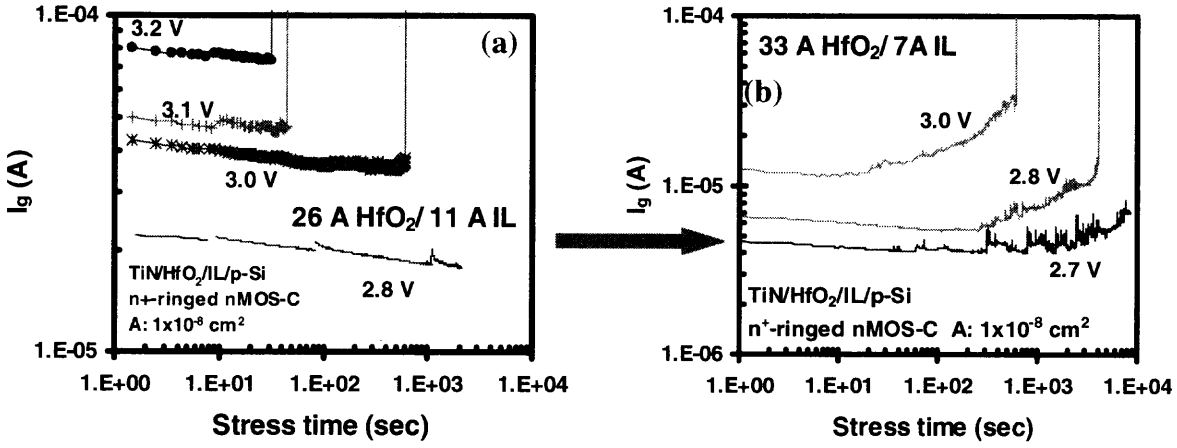


Figure 7.15 I-t characteristics during TDDB under CVS with different positive gate bias conditions for (**a**) split 1 and (**b**) split 3 of lot 1.

I-t characteristics during TDDB, as far as durations of different degradation regimes are concerned, were observed to be affected by the ratio of t_{IL} and $t_{H\text{-}K}$ in the gate stack. Data in Figure 7.15(a) and (b) shows that the duration of the PBD regime decreases in thinner high-κ/thicker IL gate stacks. With thicker high-κ/thinner IL, dominant factor controlling I_g changes from charge trapping to film degradation with V_{stress} increase. For equivalent stress bias condition of 3.0 V, $E_{H\text{-}K}$/ E_{IL} is 4.17/12 MV/cm for 2.6 nm H-K/ 1.1 nm IL case; whereas, it is 3.94/ 14.75 MV/cm for 3.3 nm H-K/ 0.7 nm IL case. Obviously, E_{IL} is higher for the latter case. Moreover, IL quality is inferior for 0.7 nm case. These two factors may be responsible for the comparatively long duration of PBD.

7.6 Effects of Charge Trapping on Degradation

In order to understand the effects charge trapping on degradation, stress/relaxation cycles were repeated a few times as shown in I-t plots in Figure 7.16(a). Considerable I_g rebound induced by the electron detrapping at Vg= −1 V, was observed. Beside this the gate stack as follows from the SILC data in Figure 7.16(b). SILC showed only minor relaxation during the de-trapping cycle suggesting that it mostly reflect effect.

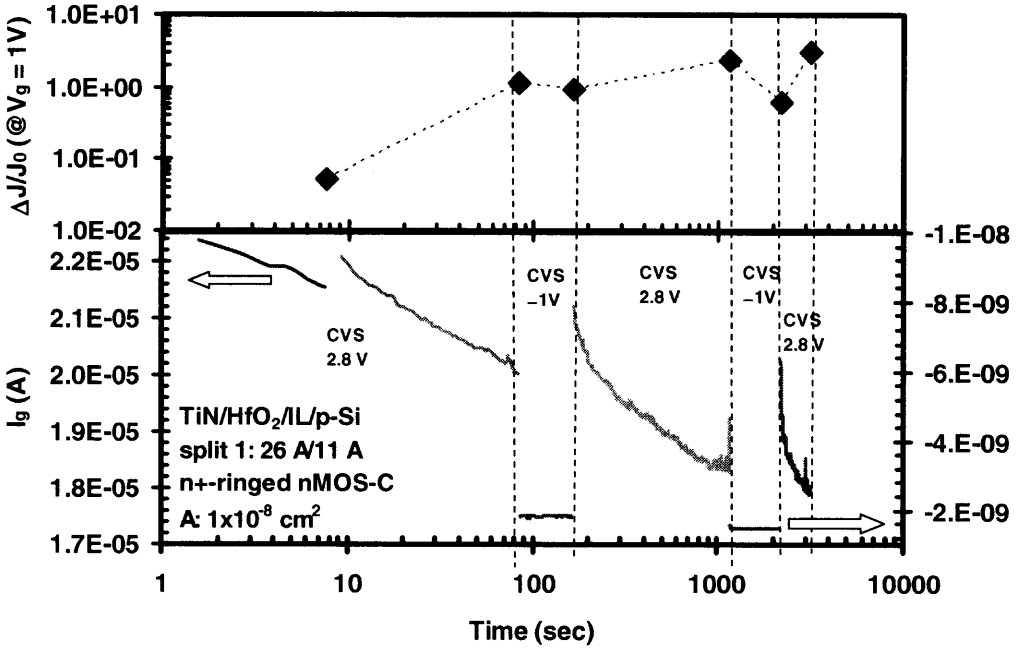


Figure 7.16 **(a)** I-t characteristics of split 1 of lot 1 under stress with 2.8V / relaxation under -1 V cycles. **(b)** Corresponding SILC, sensed at V_g = 1V w.r.t. stress/relaxation cycles.

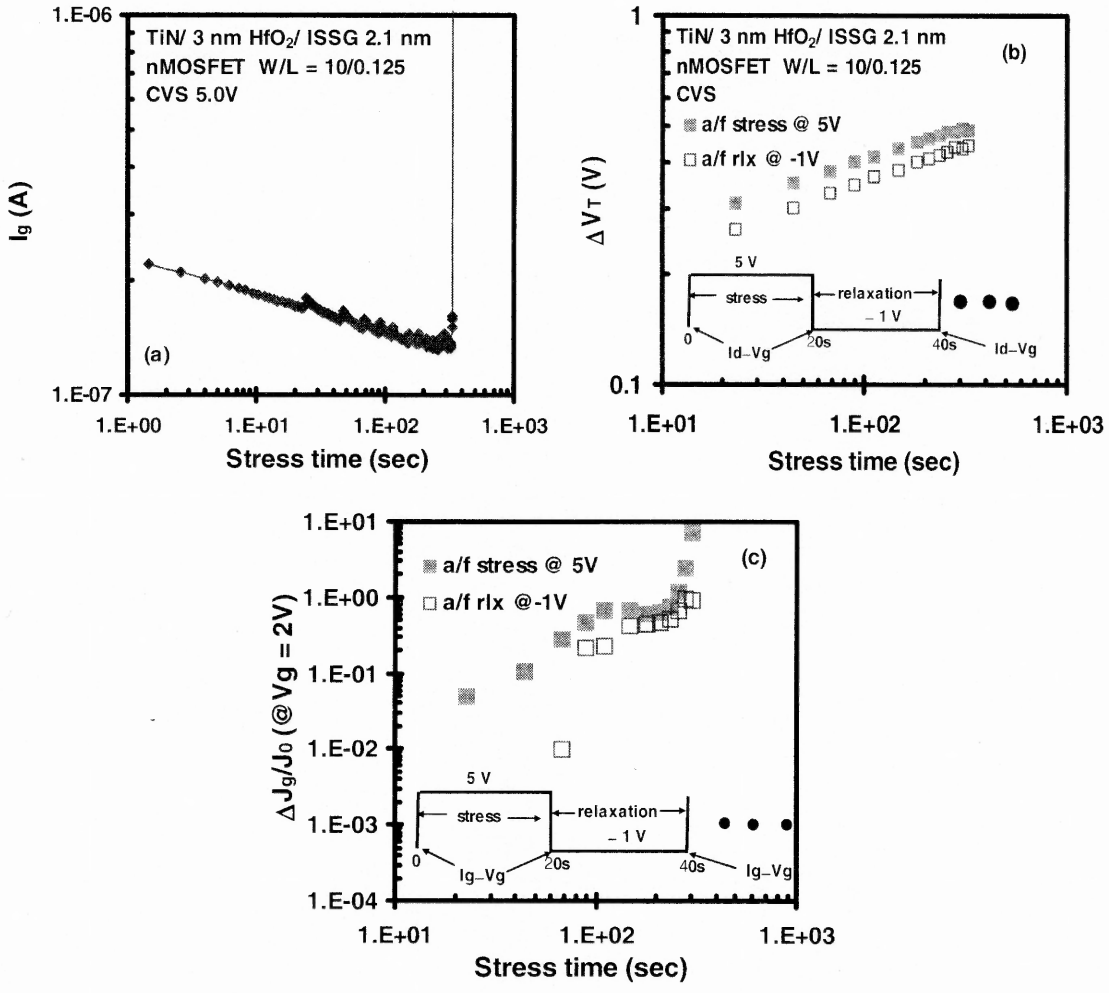


Figure 7.17 **(a)** I-t during TDDB. **(b)** ΔV_T vs. stress time during TDDB. Each 20 s of stress is followed by 20s of relaxation at −1 V. ΔV_T after relaxation period is also plotted. (**Inset**) Stress/relaxation cycle during TDDB. **(c)** $\Delta J_g / J_{g0}$ (sensed at V_g = 2 V) vs. stress time during TDDB. Each 20 s of stress is followed by 20s of relaxation at −1 V. $\Delta J_g / J_{g0}$ after relaxation period is also plotted. (**Inset**) Stress/relaxation cycle during TDDB.

To understand charge trapping effects further, stress/relaxation cycles were applied to nMOSFETs with 3 nm HfO_2/ 2.1 nm gate stack from lot 2. During each stress phase I-t was measured as shown in Figure 7.17(a). Immediately after each stress phase I_d–V_g/I_g–V_g measurements were taken as shown in the insets of Figures

7.17(b) and (c). The same measurements were taken immediately after relaxation phase. Decrease in I_g is followed by PBD regime, which terminates in HBD. Initial decrease in gate current during TDDB is due to electron trapping as follows from the increase of ΔV_T, shown in Figure 7.17(b). Detrapping cycles failed to recover ΔV_T fully as CVS generated defects. ΔV_T vs. stress time characteristics, however, does not reflect the evolution of the degradation. This suggests that ΔV_T may not be used as an effective signature of degradation in TDDB studies of the gate stacks. On the other hand, sharp increase in post-relaxation SILC, measured from $\Delta J_g / J_{g0}$ after relaxation induced detrapping, coincides with PBD as shown in Figure 7.17(c). This confirms the earlier suggestion that SILC need to be studied to understand stress-induced degradation in the gate stacks during TDDB. It is concluded that the stress-induced defects, rather than the trapping at the pre-existing defects, are responsible for the gradual wear-out of the gate stack leading to SBD, PBD and HBD.

7.7 Effect of IL Degradation on TDDB

To understand defect generation, specifically in IL, and its role in TDDB of the entire gate stack, variable-frequency charge pumping (CP) measurements were periodically taken during CVS. Low frequency CP measurements were shown to probe the defects spatially distributed deep into IL [98]. Young et al. showed that the probing depth of CP frequency in KHz order is around 1.2 nm from IL/Si interface [98]. Considering that t_{IL} ~1.1 nm, CP under the used conditions probes defect primarily within the IL.

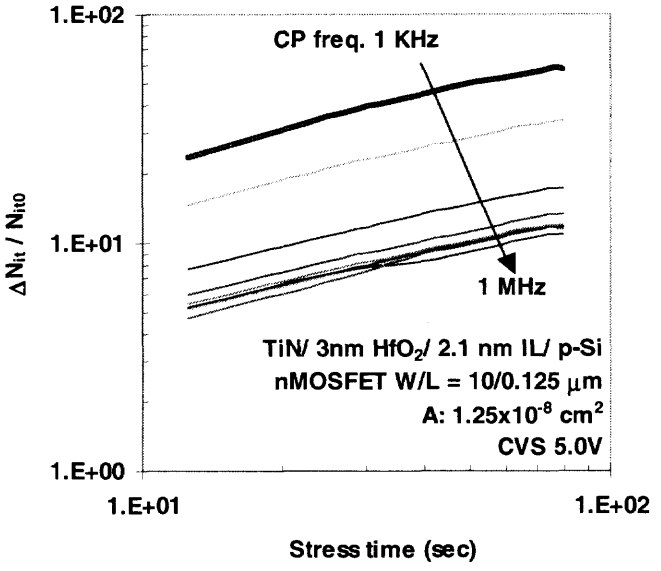


Figure 7.18 Normalized ΔN_{it} (w.r.t. initial N_{it}) vs. stress time for split 7 of lot 2. Plots for CP frequency in 1 KHz to 1 MHz range are shown.

Normalized ΔN_{it}, calculated at CP frequency of 1 MHZ to 1 KHz, is plotted with respect to stress time in Figure 7.18. During the measurement, amplitude of the pulse was kept at 1.4 V, whereas, the base was varied from -1.3 to 0 V with a step voltage of 0.1 V. Pulse rise/fall time was 100 ns. Defect generation rate (the slope of the $N_{it}(t)$ curves) is observed to be independent from the CP frequency, and, this is why, constant throughout the thickness of IL. This means that the number of generated defects is proportional to the defect density, consistent with the suggestion that the defect generation occurs at the defect precursor within IL. The same conclusion may be drawn for two other gate stacks of 3 nm HfO_2/ 1 nm IL and 7 nm HfO_2/ 1 nm IL, whose normalized $N_{it}(t)$ characteristics are shown in Figures 7.19(a) and (b), respectively. $N_{it}(t)$ follows t^n power-law dependence as observed from log-

log plots. The value of exponent, n remains almost constant as CP frequency is varied.

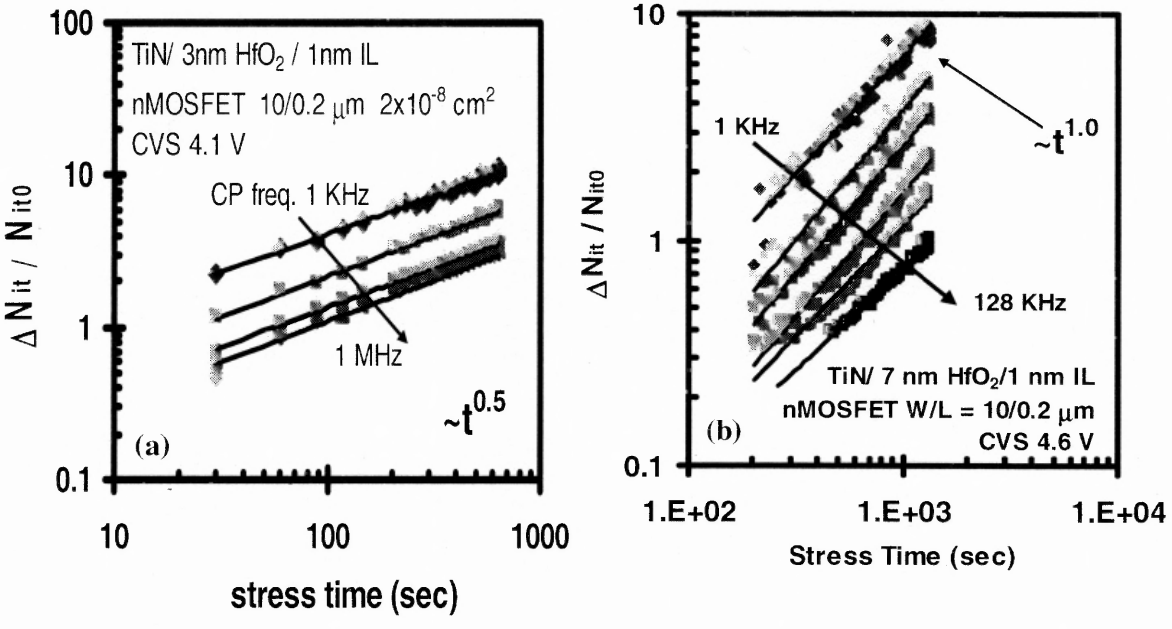


Figure 7.19 Normalized ΔN_{it} (w.r.t. initial N_{it}), measured at different CP frequencies, vs. stress time during TDDB for **(a)** 3 nm HfO_2/ 1nm IL and **(b)** 7 nm HfO_2/ 1nm IL gate stacks.

To understand the nature of SILC, the normalized SILC data sensed at $V_g = 2$ V and normalized ΔN_{it} extracted at CP frequency of 1 KHz are plotted in a log-log scale in Figures 7.20(a) and (b), respectively, which includes data for three different stacks from lot 3. Strong correlation between the power-law exponents of SILC and ΔN_{it} for each given gate stack can be readily observed. The same correlation is observed for N_{it} extracted at all other frequencies in Figures 7.19(a) and (b). Based

on this correlation, one may conclude that same defects generated within IL are responsible for both SILC and ΔN_{it}.

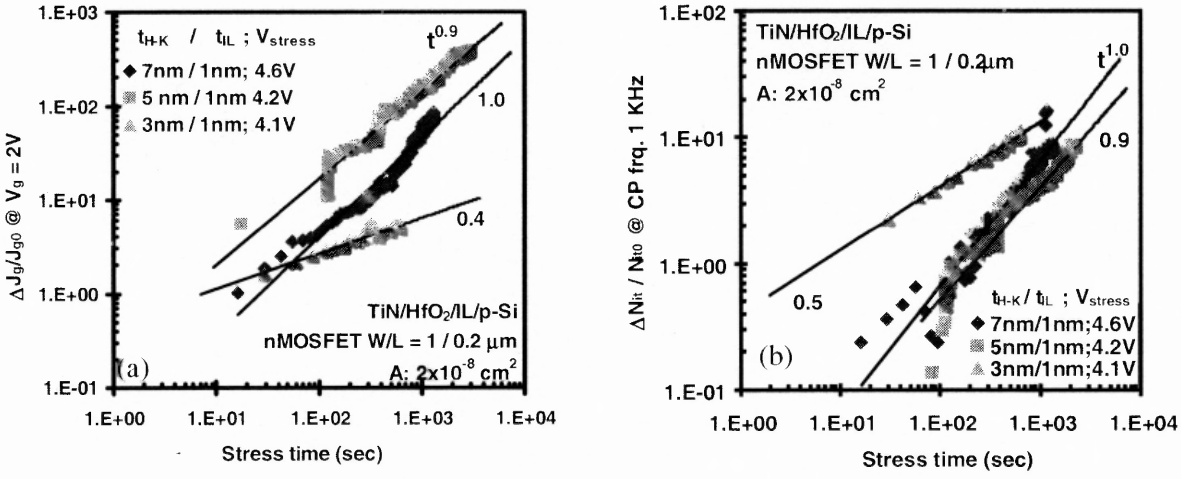


Figure 7.20 **(a)** SILC vs. stress time and **(b)** normalized ΔN_{it} vs. stress time for splits 1, 3 and 4 of lot 3. SILC is sensed at $V_g = 2$ V and N_{it} is measured at CP frequency of 1 KHz.

7.8 Breakdown Mechanisms during TDDB

To further understand wear-out during TDDB, specifically for thick high-κ conditions, compliance limits on I_g were placed while CVS was applied. Analysis of CVS data using the case of 3 nm HfO_2/2.1 nm SiO_2 stack is given. Figure 7.21 shows gate leakage current during CVS in 3nm HfO_2/2.1 nm SiO_2 gate stack nMOSFET with current compliance limits. During the initial CVS stage, stress current has been decreasing due to electron trapping in the high-κ film (V_T increased), until the soft BD (SBD) event (see inset). Figure 7.22 shows SILC data collected under the current

compliance limits (as labeled) during the stress presented in Figure 7.21. Although the current was limited, wear out continued after SBD, as seen from the SILC data in Figure 7.21, until a hard BD (HBD) occurred after ~9.875×10^3 secs of stress. In spite of increasing leakage current compliance limits, I_{lim}, SILC did not increase until I_{lim} reached 500 μA. Only after then, thermal run away current due to catastrophic/thermodynamic BD could be observed.

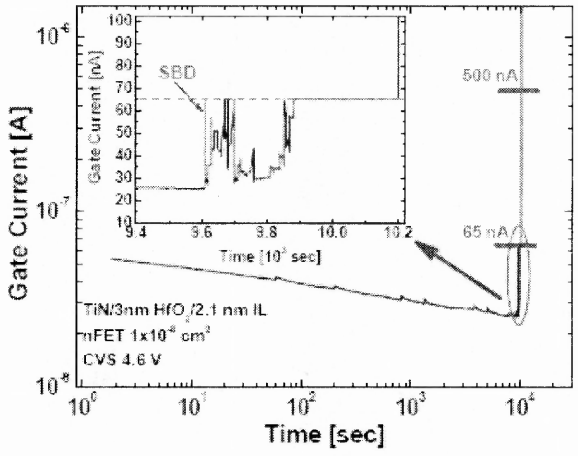


Figure 7.21 I-t characteristics during TDDB under CVS with positive gate bias condition for split 7 of lot 2. Compliance limits are applied on I_g (65 nA to 10 mA) during CVS. (**Inset**) SBD, PBD and HBD regimes are shown.

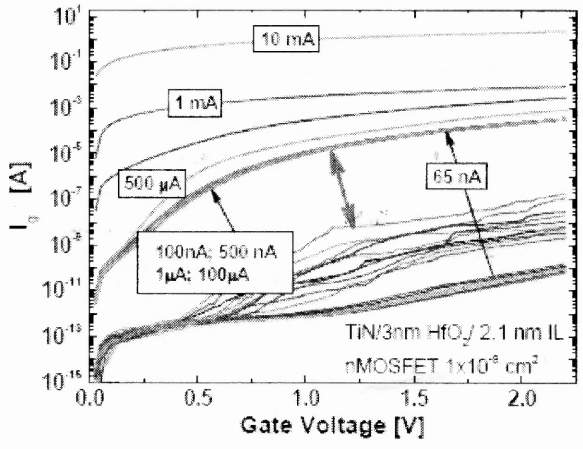


Figure 7.22 I-V plots during TDDB. Compliance limits on I_g during CVS are labeled and ,thus, specified.

Figure 7.23 shows differential resistance curves for SILC data (smoothed) in Figure 7.22. To understand the dynamics of the BD process, differential resistance $R_{diff}(V_g)$, from the SILC data and the slope of the differential resistance, S_{Rdiff} (for consistency, at a fixed V_g = 1.5V) are calculated. For pure ohmic conductance,

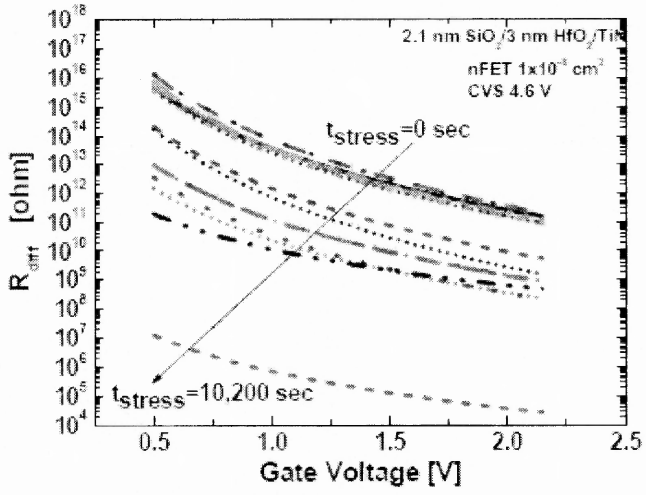


Figure 7.23. Differential resistance curves for SILC data (smoothed) in Figure 7.22.

$R_{diff}(V_g)$ = Const (i.e., S_{Rdiff}=0), the slope value $S_{Rdiff} \neq 0$ can be used as a figure of merit of ohmic vs. non-ohmic (tunneling, hopping) conductance. Changes in R_{diff} and S_{Rdif} values during the total stress time are plotted in Figure 7.24.

Figure 7.24 shows stress-induced evolution of the differential resistance, R_{diff}, and slope of the differential resistance, S_{Rdiff}. Gradual change in, R_{diff} and S_{Rdiff} suggest wer-out during defect generation/charge trapping regime. Sharp decrease signifies SBD and subsequent PBD leading to HBD.

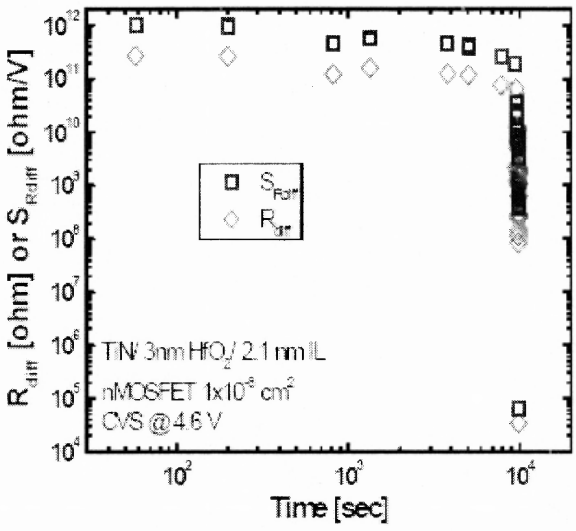


Figure 7.24 Changes in R_{diff} and S_{Rdif} values during the total stress time are plotted as a function of V_g.

Figure 7.25(a) shows evolution of the slope of the differential resistance, S_{Rdiff}, and leakage current during CVS prior to SBD. Figure 7.25(b) shows post SBD evolution of the slope of the differential resistance, S_{Rdiff}, and leakage current. Detailed variations of S_{Rdiff} during stress up to the SBD moment are shown in Figure 25(a). Until SBD, the differential resistance slightly decreased (due to higher total current) (Figure 7.24) while conductance (as reflected by $S_{R,diff}$) remained mostly unchanged (non-ohmic), which points to the generation of isolated traps as a dominant degradation mechanism. At SBD, $S_{R,diff}$ abruptly decreased by several orders of magnitude indicating that the conductance had qualitatively changed, most likely due to formation of the percolation conductive path through the dielectric. Post-SBD evolution of $S_{R,diff}$ (Figure 7.25 (b)) and R_{diff} (not shown) demonstrated a relatively rapid change in conductance towards ohmic, which is indicative of the continued degradation of the conductive percolation path; i.e., progressive BD (PBD).

This degradation is primarily driven by stress time rather than stress current (i.e., it

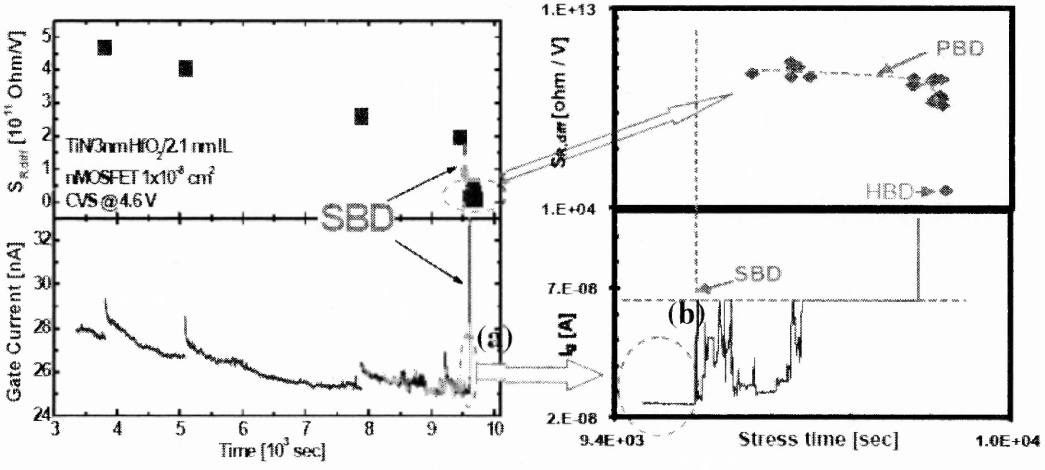


Figure 7.25 **(a)** shows evolution of the slope of the differential resistance, S_{Rdiff}, and leakage current during CVS prior to SBD. Figure 7.20 **(b)** shows post SBD evolution of the slope of the differential resistance, S_{Rdiff}, and leakage current.

compliance limit). When the current compliance limit was raised to 1 mA and above, the runaway current resulted in the formation of a near-ohmic conductive path—thermal HBD—accompanied by a several orders of magnitude drop in the S_{Rdiff} and R_{diff} values.

Figure 7.26(a) and (b) show R_{diff} and $S_{R,diff}$ as a function of V_g during CVS. It is obvious that conduction becomes less ohmic as stress progresses. Figure 7.27(a) show the evolution of the differential resistance, R_{diff}, and leakage current during CVS in 5nm HfO_2 stack. Similarly, Figure 7.27(b) show the evolution of the differential resistance, S_{Rdiff}, and leakage current during CVS For the 5 nm HfO_2/ 1 nm SiO_2 stack, both R_{diff}, and S_{Rdiff} demonstrated abrupt decreases at the SBD events; their subsequent continued decrease (i.e., changes in the conduction mechanism)

allowed the post-SBD leakage current increase to be classified as a manifestation of PBD.

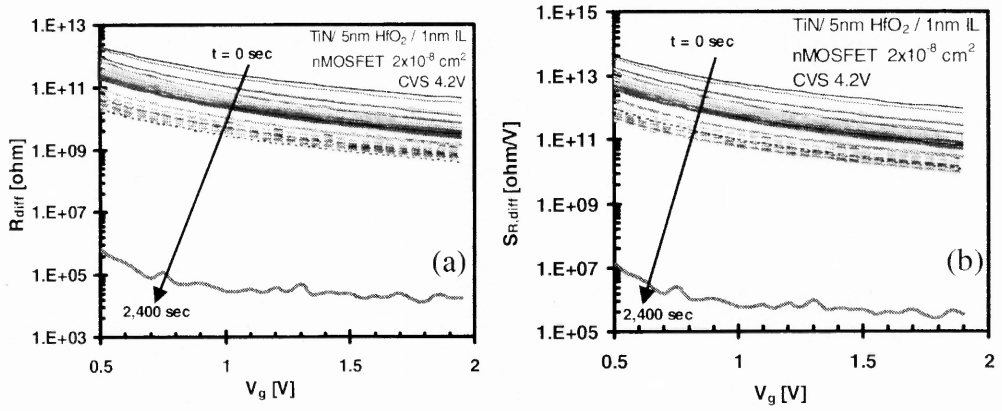


Figure 7.26 For 5nm HfO_2/ 1nm IL gate stack, **(a)** R_{diff} and **(b)** $S_{R,diff}$ vs. V_g.

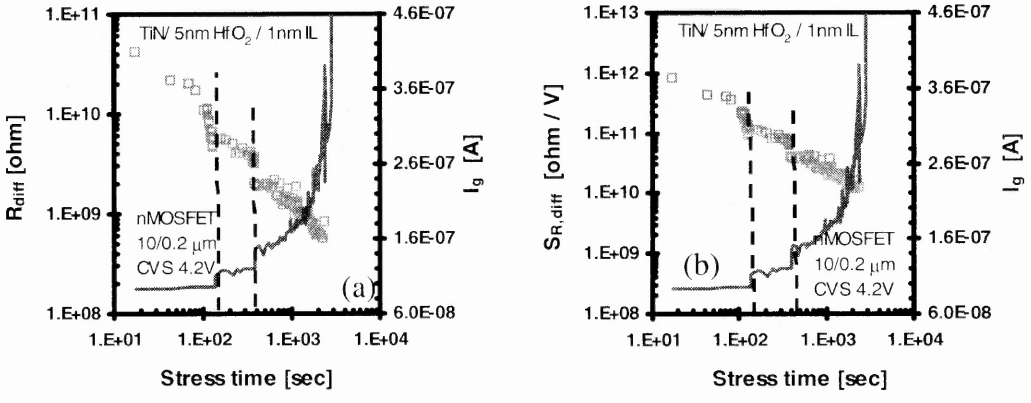


Figure 7.27 Evolution of **(a)** differential resistance, R_{diff}, and leakage current, and **(b)** S_{Rdiff}, and leakage current, during CVS in 5nm HfO_2 stack.

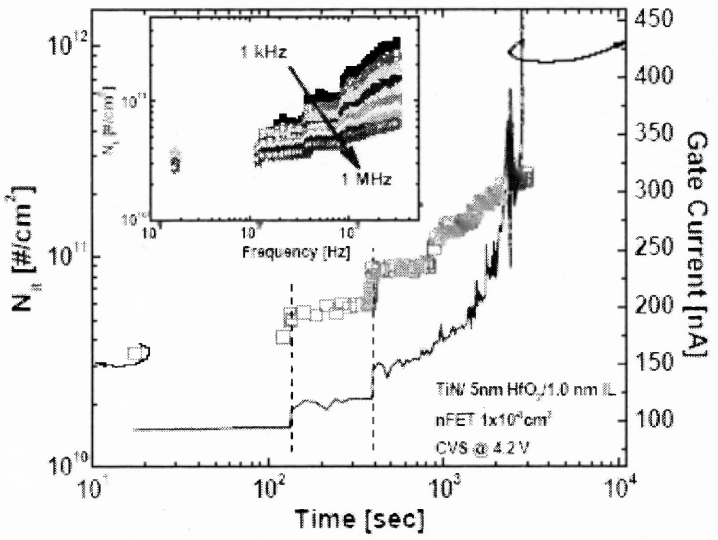


Figure 7.28 Evolution of the 1 KHz CP trap density, Nit, and leakage current during CVS on 5 nm HfO2 stack. In the inset: N_{it} vs. stress time for various CP frequencies.

Figure 7.28 shows evolution of the 1 KHz CP trap density, N_{it}, and leakage current during CVS on 5 nm HfO_2 stack. (In the inset) N_{it} vs. stress time for various charge pumping, CP frequencies are shown. A stress-induced increase in trap density, N_{it}, as measured by CP in a wide range of frequencies, showed a clear correlation with the leakage current features (SBD and PBD), Figure 7.29, and SILC. Similar growth rates of SILC and N_{it}, observed for each gate stack of a given high-κ thicknesses in Figure 7.20, indicate that their growth is most likely driven by the same underlying physical cause (i.e., by the same defects). Since the N_{it} stress time dependency (insert Figure 7.28) was similar for CP with high and low frequencies, which probe traps near the interface with the Si substrate and deeper in IL, respectively, one may conclude that the N_{it} values in Figure 7.28 correspond to the traps generated primarily within IL. This conclusion is supported by the simulation

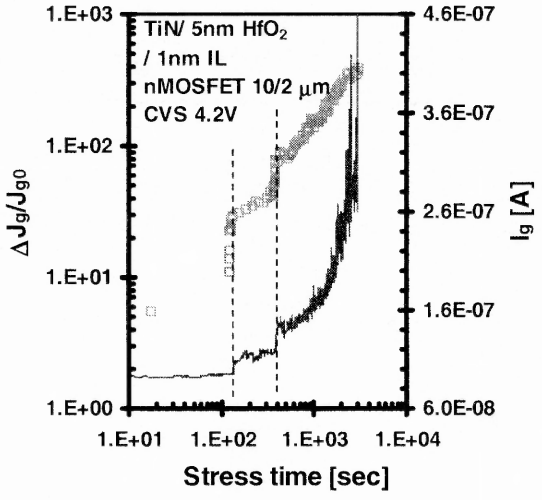


Figure 7.29 Evolution of SILC (sensed @V_g = 2V), and leakage current during CVS on 5 nm HfO2 stack.

of the CP probing depth [98], which, under the conditions used for these CP measurements, was estimated to lay within the IL. Higher density of traps in IL with closer proximity to high-κ was reported to be caused by high-κ/IL interaction [97]. Therefore, the strong correlation of SILC to N_{it} suggests that SILC is mostly controlled by IL degradation. Since leakage current evolution including BD events, correlates with SILC (in particular with to S_{Rdiff} and R_{diff}), this, in turn, suggests that BD is triggered by the degradation of the IL. Results on all other investigated gate stack combinations agree with this conclusion. PBD is readily observed in thicker gate stacks [Figures 7.30(a) and (b) for 7 nm HfO_2 gate stack] while its duration quickly diminishes in thinner samples [Figures 7.32(a) and (b) for 3nm HfO_2 gate stack].

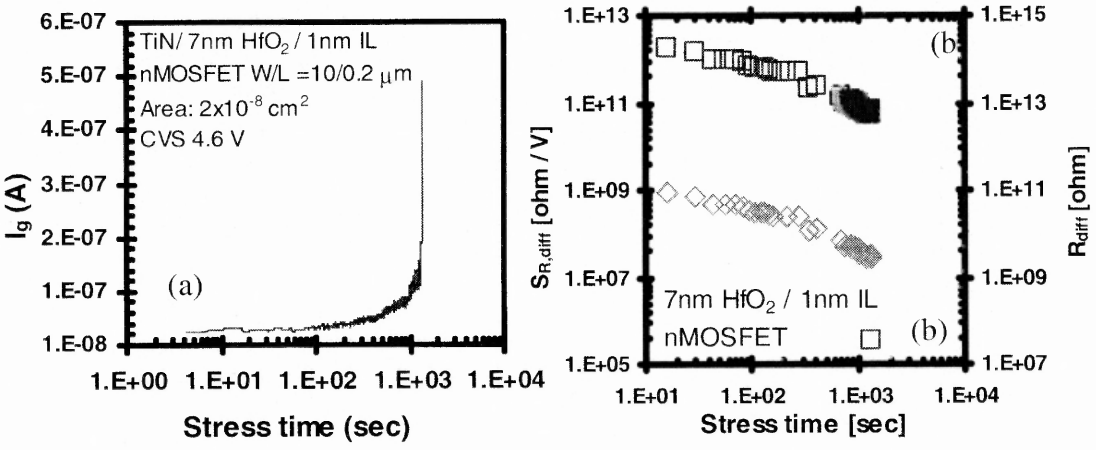


Figure 7.30 Evolution of **(a)** gate current, **(b)** R_{diff} and $S_{R,diff}$ during CVS for 7 nm HfO_2 stack.

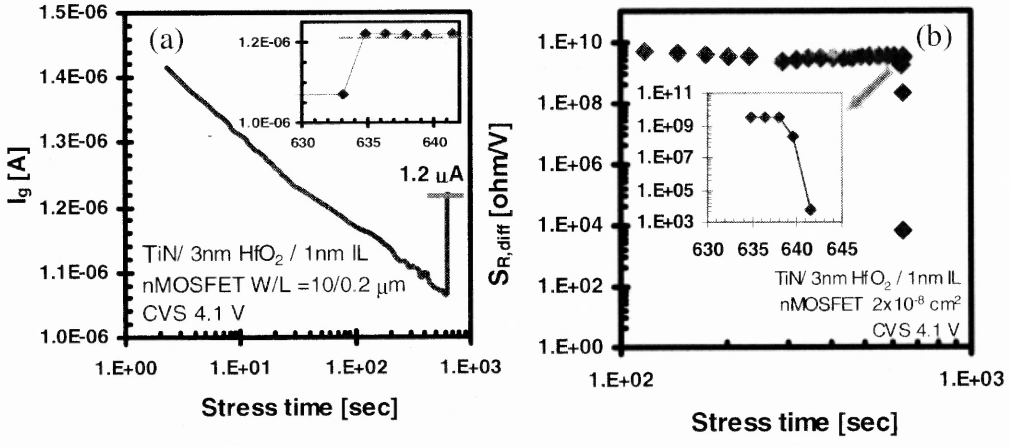


Figure 7.31 **(a)** Evolution of gate current during CVS for 3 nm HfO_2 stack. **(Inset)** Fast increase in gate current during PBD. **(b)** Evolution of $S_{R,diff}$ during CVS for 3 nm HfO_2 stack. **(Inset)** Fast decrease of $S_{R,diff}$ during PBD.

To understand breakdown mechanism further, CVS was applied on TiN/ 4 nm HfSiO/ TiN based MIM capacitors. Details of this lot can be learnt from Table 3.1. These structures are without IL. As a result, stress-induced degradation can be understood solely for the high-κ layer. Leakage current vs. stress time is shown for

the stress levels of 2.5 V and 2.7 V in Figures 7.32(a) and (b), respectively. Very

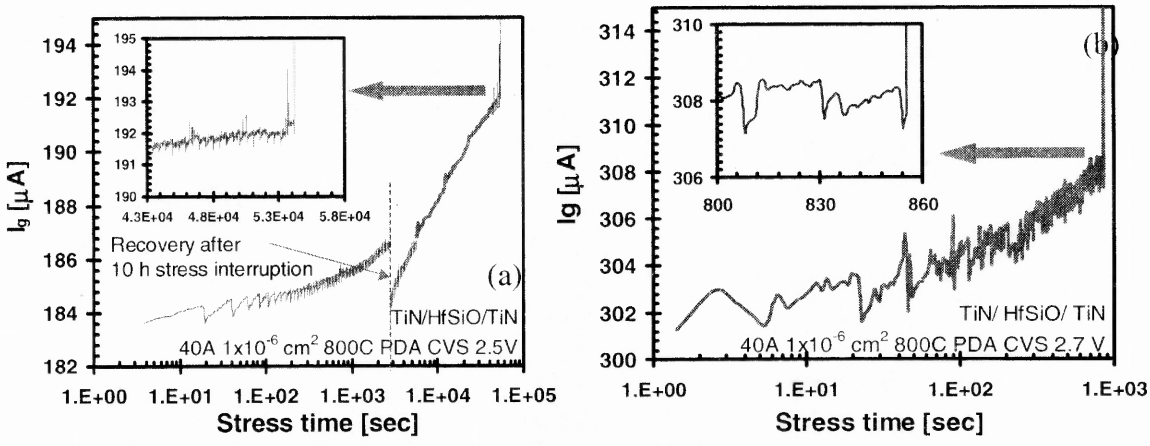


Figure 7.32 For 4 nm HfSiO based MIM capacitors, I-t characteristics under CVS applied with stress levels of **(a)** 2.5 V and **(b)** 2.7 V. **Insets** of Figures **(a)** and **(b)** show I-t immediately before HBD.

little increase in I_g is observed during CVS till BD. For 2.5 V case, 10 hours of interruption was provided. This resulted in almost complete recovery of I_g, which is in contrast with the observations made for the high-κ gate stacks as discussed above. Insets of Figures 7.32(a) and (b) show that I_g does not show the signatures of PBD before HBD, which is also different from I-t characteristics observed during TDDB of high-κ gate stacks.

To understand degradation in the oxide I-V measurements were periodically taken till BD. Figures 7.33(a) and (b) show I-V characteristics for stress levels of

2.5 V and 2.7 V, respectively. It is obvious that increase in I_g due to stress-induced defects is not observed. This is also different from I-V characteristics observed for the high-κ gate stacks. Hard BD is manifested in the thermal run away current

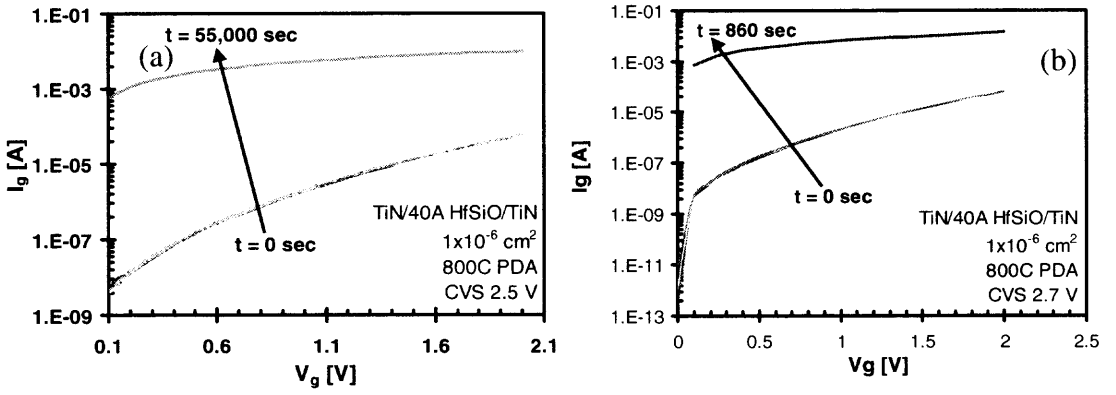


Figure 7.33 For 4 nm HfSiO based MIM capacitors, I-V characteristics under CVS applied with stress levels of **(a)** 2.5 V and **(b)** 2.7 V.

observed in Figures 7.33(a) and (b).

To understand SILC during TDDB better, normalized ΔJ_g ($\Delta J_g/J_{g0}$), sensed at V_g = 1 V, 1.5V and 2V is plotted for the stress level of 2.5 V in Figure 7.34. Little changes in SILC are observed. Interruption of stress for a long period of time shows almost full recovery. This is also in contrast to the partial recovery and significant increae of SILC observed in the case of high-κ gate stacks.

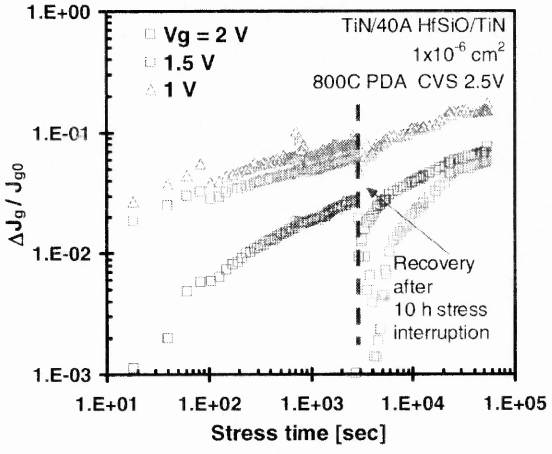


Figure 7.34 SILC sensed at different V_g.

Differential resistance and $S_{R,diff}$, found from I-V measurements in Figure 7.33(a), is plotted as a function of V_g during TDDB in Figure 7.35 (a) and (b), respectively.

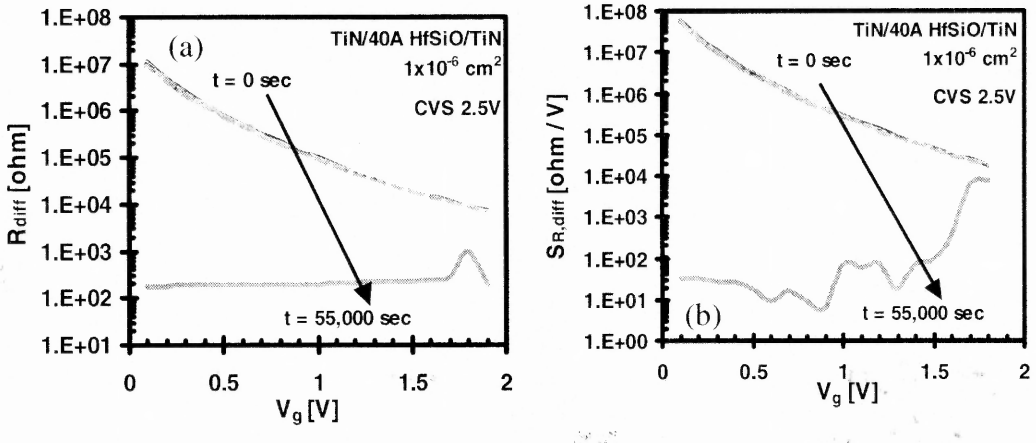


Figure 7.35 For 4 nm HfSiO based MIM capacitors, **(a)** R_{diff} vs. V_g and **(b)** $S_{R,diff}$ vs. Vg during TDDB.

Gradual decrease in R_{diff} and $S_{R,diff}$ with stress time, which are the signatures of the significant wear-out in high-κ gate stacks, is not observed. Similarly, S_{Rdiff} and R_{diff} shows no signs of PBD up to BD as shown in Figure 7.36. The proposed mechanism of the SiO_2 layer wear-out and BD suggests that as the density of the stress-generated traps increases, conductance through the dielectric changes from

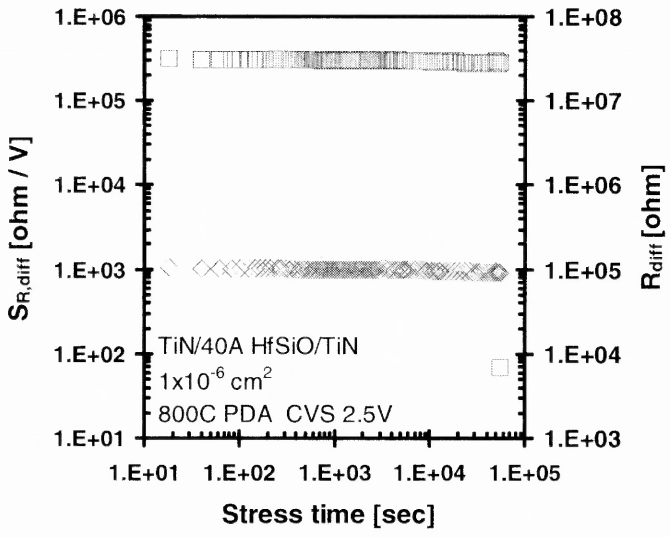


Figure 7.36 Evolution of the differential resistance, R_{diff}, and its slope, S_{Rdiff}, during CVS of MIM capacitors.

trap-assisted tunneling through isolated traps to trap-to-trap tunneling along the percolation path (post SBD) to hindered hopping (ohmic-like, post HBD) when trap potentials overlap to create a low barrier path, as shown in Figure 7.37. Creation of this path signifies local collapse of the dielectric band gap due to the high density of the unoccupied localized states associated with the broken Si-O bonds [89].

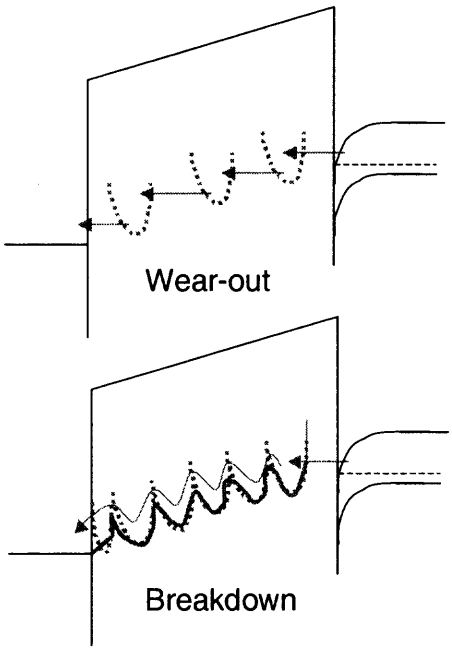


Figure 7.37 Schematic of the SiO_2 band diagram illustrating conduction mechanism during the wear-out stage (semi-isolated traps) and breakdown (overlapping traps).

7.9 Effect of IL Quality on T_{BD} and Q_{BD}

To understand the effect of the IL quality on time-to-breakdown, T_{BD} and charge-to-breakdown, Q_{BD}, CVS was applied on a large number of devices (~20) belonging to each split with pre-deposition treatment in lot 2. Weibull plots of T_{BD} and Q_{BD} are presented in Figures 7.38(a) and (b), respectively for HF-last condition (with PreDA). Similar Weibull plots are shown for 0.7 nm and 1.1 nm ISSG (with PreDA) in Figures 7.39 and 7.40, respectively. Low value of slope of Webull plots, β is consistent with β found by other high-κ groups [91]-[94]. For sub-2 nm SiO_2, it is

reported that variation in thickness results in a large dispersion in the value of β [91]. It is further shown that the larger the number of SBDs, prior to HBD, the higher the value of β [92]. It has been already shown that IL degradation initiates TDDB in the

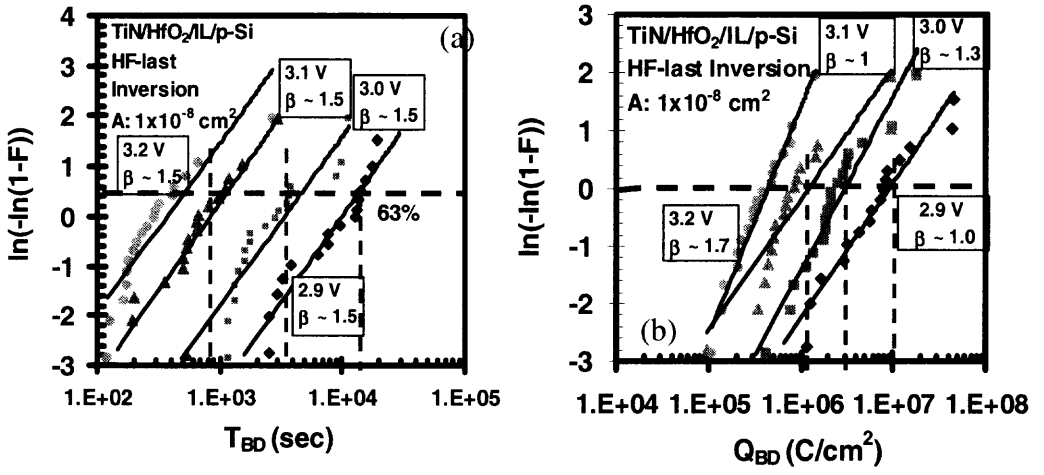


Figure 7.38 Weibull plot of **(a)** T_{BD} and **(b)** Q_{BD} for 3nm HfO_2/ 1.1 nm HF-last IL.

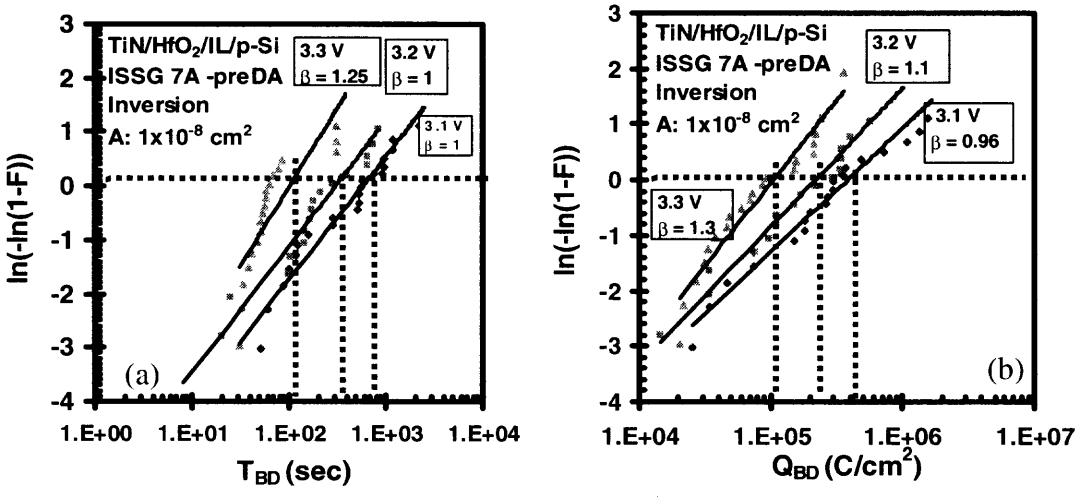


Figure 7.39 Weibull plot of **(a)** T_{BD} and **(b)** Q_{BD} for 3nm HfO_2/ 0.7 nm ISSG IL case for different bias conditions. PreDA was performed for this split.

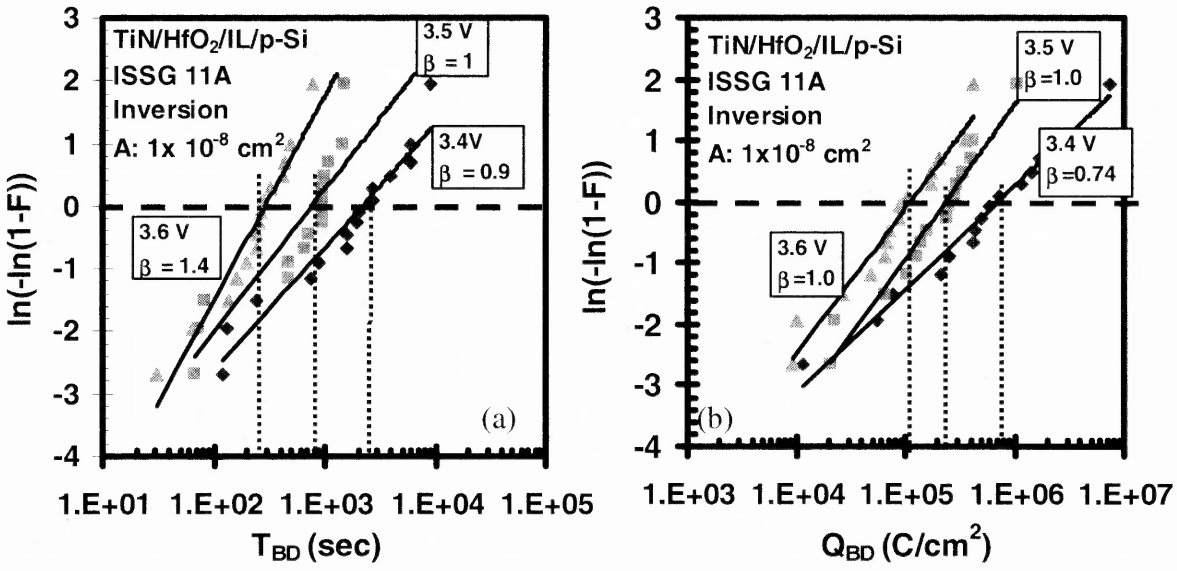


Figure 7.40 Weibull plot of **(a)** T_{BD} and **(b)** Q_{BD} for 3nm HfO_2/ 1.1 nm ISSG IL case for different bias conditions. PreDA was performed for this split.

gate stacks. It is found from TEM images that 5A of thickness variation occurs in the gate stacks, specifically for ISSG cases [97]. Moreover, the number of SBDs before PBD leasing to HBD is found to be rather small in the devices (see Section 7.8). Slope, β is expected to be low in TDDB studies. For Hf-last case, no special processing was done to grow IL. High-κ was deposited after PreDA treatment. Interfacial layer growth occurred as an natural extension. This is why thickness variation in IL can be assumed to be low compared to the other growth conditions. This assumption is supported by comparatively high value of β. For ISSG cases, 2 nm of thermal SiO_2 was grown. Then it was etched back to 0.7 or 1.1 nm or left untouched. High-κ layer was then grown on the top of IL. For the case of 0.7 nm, IL regrew to 1.1 nm after high-κ deposition. Interaction of high-κ and IL is a possibility. As a result, the thickness variation is expected to be quite high for ISSG growth conditions. Low value of β for splits with ISSG IL supports this view.

Sixty-three percent, 63% failure value of T_{BD}, t_{63} is extracted from Weibull plots. In Figure 7.41, t_{63} is plotted with respect to V_g for various IL growth conditions. Dependence of t_{63} on IL quality is obvious. Ten-year lifetime projections are made and found to be highly related to IL quality. It is readily observed that the better the IL quality, the higher the operating voltage. Operating V_g is observed to be in 1.5 V to 1.75 V range for IL with $t_{physical}$ ~ 1.1 nm.

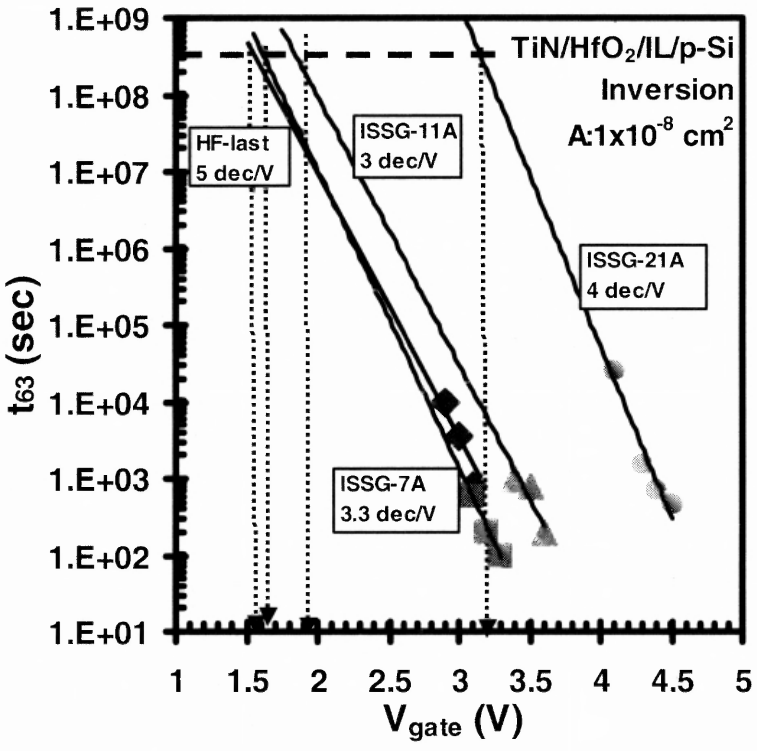


Figure 7.41 Sixty-three percent (63%) failure value of T_{BD}, t_{63} vs. Vgate for different IL growth conditions.

To understand the dependence of operating fields on IL quality, t_{63} vs. E^{IL} and $E^{H\text{-}K}$, calculated for a given split and stress bias condition, are plotted in Figures 7.42(a) and (b), respectively for ILs of different qualities. It is obvious that IL quality strongly affects T_{BD}. On the other hand, even for the same quality of high-κ, strong

dispersion is found in E^{H-K} from split to split. This reaffirms the earlier suggestion that IL degradation plays the dominant role in TDDB and conclusion that the quality of IL strongly affects the choice of the operating gate voltage.

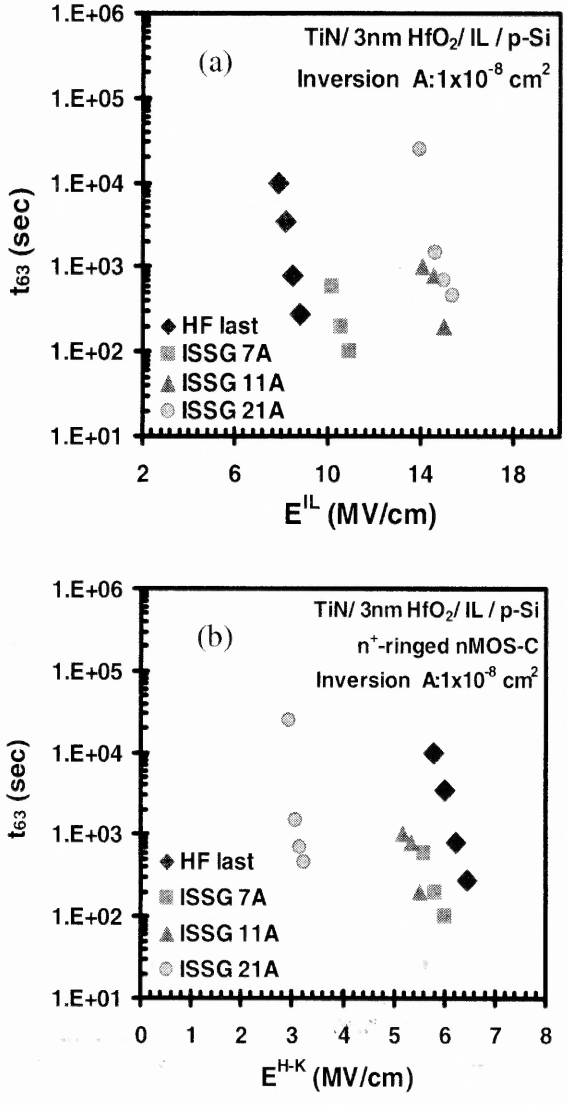


Figure 7.42 Sixty-three percent (63%) failure value of T_{BD} (t_{63}) vs. **(a)** E^{IL} and **(b)** E^{H-K} for splits with different IL conditions. PreDA was performed for each split.

Influence of both field and fluence on the breakdown of the high-κ gate stacks can be observed from TDDB studies. Sixty-three percent, 63% failure value of Q_{BD} is extracted from Weibull plots. In Figure 7.43, it is plotted with respect to V_g for various IL growth conditions. Dependence of Q_{BD} on IL quality is obvious. It is readily observed that for the same V_g, the better the IL quality, the higher the charge-to-breakdown.

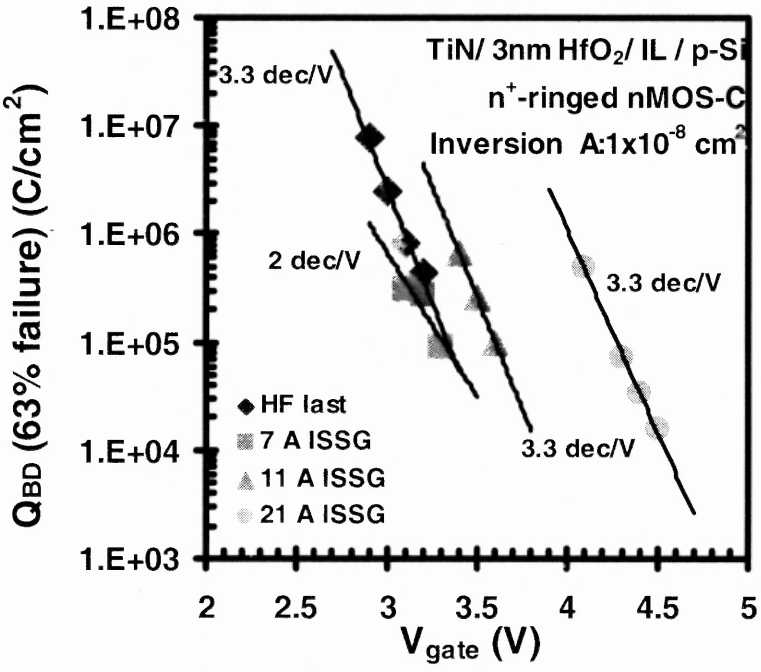


Figure 7.43 Sixty-three percent (63%) failure value of Q_{BD} vs. V_{gate} for different IL growth conditions. PreDA was performed on each split.

In order to understand the role of fluence in BD better, Q_{BD} is plotted with respect to E^{IL} and E^{H-K} for various IL growth conditions in Figures 7.44(a) and (b), respectively. It is obvious that the plots for 1.1 nm and 2.1 nm ISSG are inconsistent with the observed IL quality. For the same E^{IL}, Q_{BD} is found to be higher for 1.1 nm

cases even though 2.1 nm has a higher quality. For the same high-κ, Q_{BD} shows a large dispersion with respect to E^{H-K}. This suggests that IL initiates TDDB and T_{BD} characteristics are highly consistent with the trend in the IL quality.

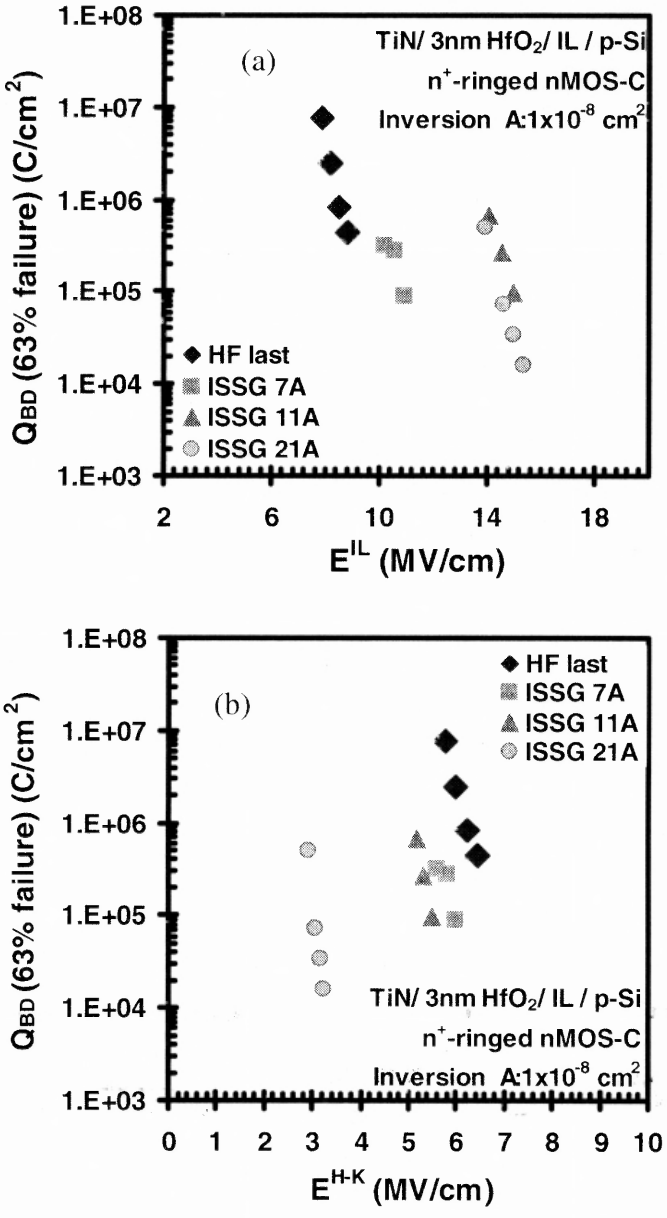


Figure 7.44 Sixty-three percent (63%) failure value of Q_{BD} vs. (**a**) E^{IL} and (**b**) E^{H-K} for splits with different IL conditions. PreDA was performed for each split.

7.10 Temperature Dependence of TBD

Field-driven E and fluence-driven 1/E are two major models that explain field and temperature dependence of dielectric degradation during TDDB as explained in the following Equations [89]:

$$\text{E model: } \ln(T_{BD}) \propto \frac{\Delta H_0}{k_B T} - \gamma E_{OX} \tag{7.4}$$

$$\text{1/E model: } \ln(T_{BD}) \propto \frac{E_a}{k_B T} + G\frac{1}{E_{OX}} \tag{7.5}$$

Here, T_{BD} is time-to-breakdown; ΔH_0 is the observed activation energy of the bond breakage, whereas E_a is the activation energy associated with the current-induced hole injection and capture into the dielectric; γ and G are the field acceleration factors; E_{ox} is the externally applied electric field and k_B is Botzmann constant.

McPherson showed that these two models are actually complementary, i.e, both the field-induced (E model) and current-induced (1/E model) degradation mechanisms occur simultaneously [89]. For metal gate/high-κ gate stacks, specifically under inversion condition, anodic hole injection does not occur. As a consequence, the field-induced degradation is expected to be significant. It is further

shown that ΔH_0 and γ decreases and increases, respectively with κ as shown below [89]:

$$\Delta H_0 = \Delta H_0^* - p_0\left(\frac{2+\kappa}{3}\right)E_{OX} \tag{7.6}$$

$$\gamma = \frac{p_0\left(\frac{2+\kappa}{3}\right)}{k_B T} \tag{7.7}$$

Here, ΔH_0^* is the activation energy in the absence of field and p_0 is molecular dipole-moment component opposite to local field.

It is obvious that the degradation in the gate stack is significantly high at elevated temperatures. Degradation of IL triggers gate stacks breakdown. At elevated temperature and field conditions, degradation may be severe within the high-κ layer as well because ΔH_0 is low. This may change the breakdown mechanism observed at room temperature.

To understand whether degradation is field or fluence driven, and whether IL initiates breakdown at elevated temperatures also, TDDB measurements were taken at different elevated temperatures for a fixed bias condition using a large number of samples (~20). Weibull plots of T_{BD} are shown for different temperatures in Figure 7.45(a), (b) and (c). Effect of temperature on T_{BD} is clearly observed. Arrhenius plot of 63% failure value of T_{BD}, t_{63}, is plotted for various IL growth conditions in Figure 7.46. It is observed that $\Delta H_0 \approx 0.5$ to 0.6 eV. For SiO_2, $p_o(2+\kappa)/3 = 13$ e-Å, where e is the charge of an electron, is widely reported [89]. It is obvious from Equation 7.6 that ΔH_0^* depends on κ and E_{ox}, which are the possible sources of errors. Charge

trapping within the oxide distorts internal electric field and reduces cathode electric field (E_c) by ΔE_c as described in Equations 7.8 and 7.9 [29]:

$$\Delta E_c = \frac{-qN_t}{\varepsilon_0 \varepsilon_{ins}}\left(1 - \frac{x_t}{t_{ins}}\right) \tag{7.8}$$

$$\frac{qN_t}{\varepsilon_0 \varepsilon_{ins}}\left(1 - \frac{x_t}{t_{ins}}\right) \approx \frac{C_{ox}\Delta V_T}{\varepsilon_0 \varepsilon_{ins}} \approx \Delta V_T\left(\frac{1}{EOT}\right) \tag{7.9}$$

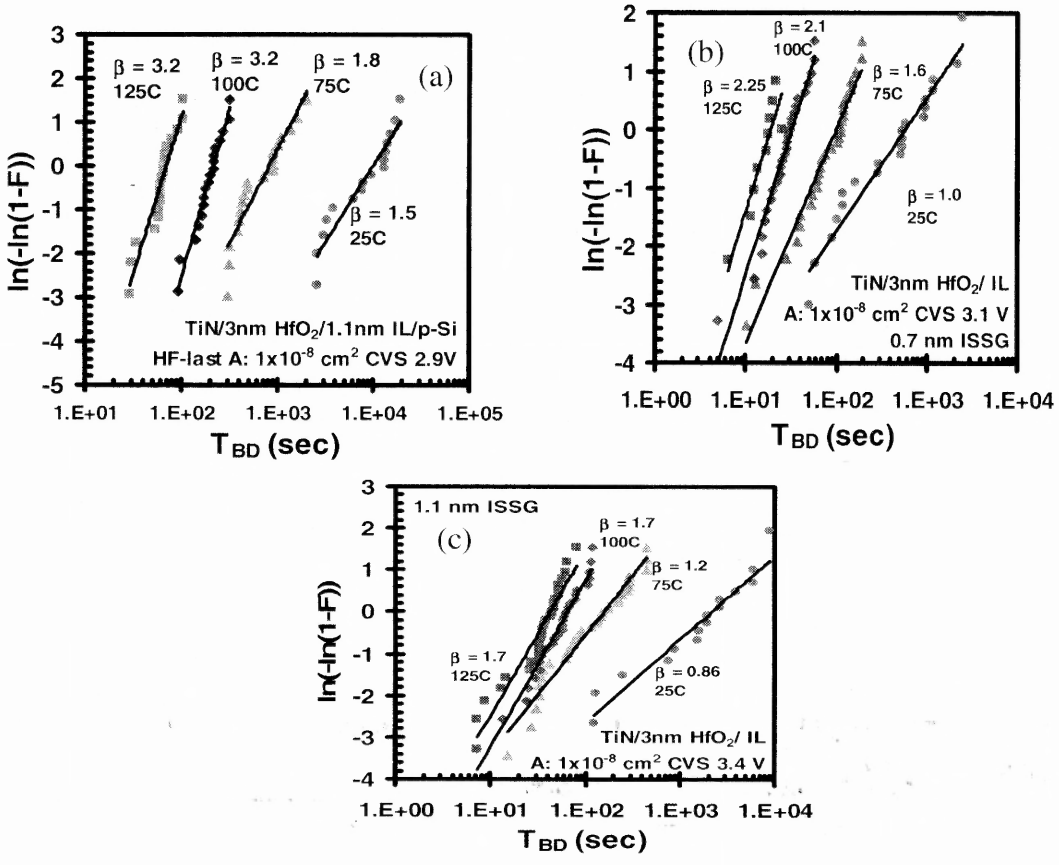


Figure 7.45 Weibull plots of T_{BD} at different temperatures for **(a)** HF-last, **(b)** 0.7 nm ISSG, and **(c)** 1.1 nm ISSG IL growth conditions.

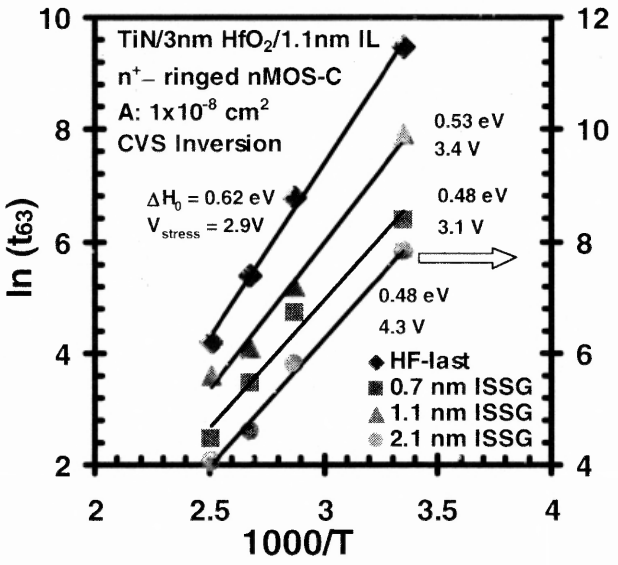


Figure 7.46 Arrhenius plot of t_{63} for different IL growth conditions.

Here, ε_0 is the free-space permittivity, ε_{ins} is the relative permittivity of the insulating material, N_t is trapped charge density, x_t is the distance of charge centroid from cathode, t_{ins} is insulator thickness, $C`_{ox}$ is oxide capacitance density.

Table 7.2 Corrected ΔH_0^* for Different IL Conditions

IL condition	V_{stress} (V)	E_{IL} (MV/cm)	ΔV_T (V)	ΔE_{IL} (MV/cm)	κ	$p_0(2+\kappa)/3$ (eA)	ΔH_0 (eV)	ΔH_0^* (eV)
HF-last	2.9	7.8	0.087	0.48333	8.5	0.23136	0.62	2.31
0.7 nm ISSG	3.1	10	0.224	1.01818	7.5	0.20932	0.53	2.41
1.1 nm ISSG	3.4	14.09	0.119	0.49583	6.1	0.17848	0.48	2.91
2.1 nm ISSG	4.3	15.24	0.382	0.764	3.9	0.13	0.48	2.36

Corrected ΔH_0^* for different IL conditions are depicted in Table 7.2 by assuming $\Delta E_{ox} \approx \Delta E_{IL}$. The values of κ and E_{ox} are corrected for different IL and stress bias conditions. The values of EOT are found from Figure 7.1 for different IL conditions. It is observed that $\Delta H_0^* \approx 2 - 3$ eV, which is within the activation energy range reported for the field-driven TDDB of SiO_2 [89]. For the fluence-driven TDDB of SiO_2, $\Delta H_0^* \approx 0.3$ eV, since it is not associated with the bond breakage [89]. Therefore, under inversion regime, IL degradation triggers the entire gate stacks breakdown and the wear-out during TDDB is mostly field-driven.

7.11 Summary

TZBD and TDDB characteristics of TiN/HfO_2 based gate stacks with varying IL and high-κ layer thickness conditions were studied in this work. IL quality was also varied to study its effect on the breakdown characteristics. It is shown that for the thin high-κ layer, TZBD is triggered by IL, whereas, for thick high-κ layer, it itself initiates the gate stacks breakdown under RVS. Four regimes of degradation can be observed during TDDB: charge trapping/defect generation, SBD, PBD and HBD. The duration of each regime, specifically charge trapping/defect generation and PBD, depends on the relative combination of IL and high-κ layer thickness. Strong correlation between SILC and defects generated within IL implies that IL breakdown triggers TDDB of the gate stack. Statistical studies of T_{BD} and Q_{BD} suggest the influence of both the field and fluence in TDDB. It is experimentally found the quality of IL, specifically for thin high-κ layer, not only affects its breakdown field

but also plays the dominant role in determining T_{BD} of the gate stack. Temperature dependent T_{BD} shows that IL degradation triggers the entire gate stacks breakdown and the wear-out during TDDB is mostly field-driven.

CHAPTER 8

CONCLUSIONS

Different reliability issues of Hf-based high-κ gate stacks are addressed in this research work. To this end mostly MOCVD TiN/Hf-silicate and ALD TiN/HfO2 based gate stacks are used. High-κ and interfacial layer thickness, and pre deposition anneal, post deposition anneals and IL growth conditions are varied to comprehensively analyze the reliability of the gate stacks.

Formation of electrically active ionic defects like charged bulk ($V^{++}/V^{+}/V^{0}/V^{-}/V^{--}$) and 'arm' (Hf-$V^{++}$-Si/ Hf-$V^{0}$-Si) O vacancies is energetically favorable in Hf-based oxides due to its predominantly ionic bondings. The defect levels have been experimentally observed for the first time in the gate stacks from low temperature, leakage, and time and temperature dependent characteristics of de-trapping from stress-induced defects.

Excellent match between experimental and calculated defect levels provide information about their physical origins. Substrate hot electron (SHE) stress with incident carrier energy, E_{inc} above the bulk charged O vacancy formation threshold results in a strong correlation between slow transient trapping and trap assisted tunneling, which is characteristic of negative-U transition of V^{++} levels. Moreover, SHH stress with E_{inc} above 'arm' O vacancy formation threshold results in stress-induced deep hole level lying within Si band-gap range, which is characteristic of Hf-V^{++}-Si level. Thus, the presence of O vacancies in these films is considered to be

confirmed. Their roles in transport mechanisms under different polarity and band bending conditions have been determined. For gate injection, transport through mid-gap states dominates. Under substrate injection, conduction through mid-gap states for low gate bias (V_g~0.5V), trap-assisted tunneling via negative-U transitions for moderate V_g(~2V), and transport through shallow traps for high V_g(~2V) dominate.

Based on transport mechanisms and defect levels, effective physical models have been formulated to explain trapping characteristics under different stress conditions. Under gate injection, trapping at deep electron and hole levels, reasonably speculated to be V^0 and Hf-V^{++}-Si, leads to slow transient trapping and causes a turn-around effect for a given gate bias condition. Under substrate injection, lateral distribution of deep trapping causes turn-around effect as far as stress levels are concerned.

Negative bias temperature instability, NBTI effects under different bias and temperature conditions were studied for TiN/Hf-silicate based pMOSFETs. For low bias conditions, mixed degradation due to both electron and hole trapping within the bulk high-κ mostly dominates ΔV_T. Interface state generation, observed from change in sub-threshold slope, $\Delta S/S_0$, was found to be negligible. For moderately high to high stress levels, initially Si-H bond breaking induced interface sates and diffused H-species induced bulk trap generation dominates. Initial temperature, time and oxide electric field dependence shows excellent match with that of R-D based NBTI model. Carrier separation technique shows that impact ionization induced hot hole generation, signature being the reversal of the polarity of source/drain current during

stress, was not observed. This possibly results in higher bond-annealing/bond-breaking ratio as, with the progress of the stress, less number of bonds are available to be broken at the presence of low energy holes. This may be responsible for the observed saturation of interface state generation and ΔV_T under high bias temperature stress conditions.

Time-zero breakdown, TZBD characteristics of ALD TiN/HfO_2 based gate stacks are comprehensively analyzed in this paper. Effects of IL and high-κ thickness, IL growth, PreDA and PDA conditions on TZBD are analyzed in this work. Cumulative failure distribution of V_{BD}, observed by applying RVS on n^+-ringed nMOS-C devices from all the splits of different lots under both inversion and accumulation regimes, suggests intrinsic BD. Breakdown fields, observed from SiO_2 and HfO_2 based MOS and MIM structures, respectively, show good match with theoretical values. E_{BD}^{IL} and $E_{BD}^{H\text{-}K}$, calculated by considering the effects of the IL quality on its EOT, are found to be within the theoretical and experimentally observed limits. Under inversion condition, for thin high-κ layers (< 3.5 nm), IL triggers BD; otherwise, high-κ layer initiates it. As far as the dependence of E_{BD}^{IL} on growth and thickness conditions related IL quality is concerned, 2.1 nm ISSG is found to be the best. For the equivalent high-κ layer, it is followed by 1.1 nm ISSG, 0.7 nm getterred, 1.1 nm chemical SiO_x, 0.7 nm ISSG and HF-last. For the same IL and thick high-κ layers, both $E_{BD}^{H\text{-}K}$ and E_{BD}^{IL} decrease as high-κ thickness increases. PreDA does not change the quality of IL. Difference in V_{BD} under inversion and

accumulation, being a signature of the quality of the gate stack, depends on PDA. For equivalent gate stacks, it is higher for PDA in N_2 at 600°C compared to NH_3 at 700°C.

Four regimes of degradation can be observed during TDDB: charge trapping/defect generation, SBD, PBD and HBD. The duration of each regime, specifically charge trapping/defect generation and PBD, depends on the relative combination of IL and high-κ layer thickness. Strong correlation between SILC and defects generated within IL suggests that IL breakdown triggers TDDB of the gate stack. Stress-time evolution of the differential resistance and its slope, calculated from SILC data, is found to correlate strongly with the gate leakage current features, in particular SBD and HBD, and to identify progressive BD. It is experimentally found the quality of IL, specifically for thin high-κ layer, not only affects its breakdown field but also plays the dominant role in determining T_{BD} of the gate stack. Arrhenius plots of temperature dependent T_{BD} for different IL growth conditions shows that activation energy of bond breakage shows an excellent match with that for SiO_2 based oxides. This further suggests that IL degradation triggers the entire gate stacks breakdown under inversion, and the wear-out during TDDB is mostly field-driven.

8.1 Impact and Limitations

Future of high-κ implementation in CMOS technology depends on further optimizing the processing conditions to reduce charge trapping in the gate stack with a view to enhancing reliability. In this research work, the defect energy levels within Hf-based high-κ have been determined, and their roles in NBTI/PBTI and transport have been investigated. This will help to decide on the correct biasing conditions of high-κ based CMOS circuits. Experimental results, gleaned from TZBD and TDDB studies, will go a long way in deciding the optimized IL thickness and processing conditions for a given Hf-based high-κ layer so that operating voltage meets 10-year life-time projections.

The impact of the reliability studies performed in this research could have been broadened further if effect of different metal gates (e.g., fully silicided) and anneal conditions (e.g. PDA in D_2 ambient) on the reliability of Hf-based high-κ gate stacks had been incorporated. Similar reliability studies of the gate stacks, which includes high-mobility channels, would have enlarged the prospects of this work further.

8.2 Future Work

Reliability studies, performed in this research, suggest that trapping at and transport through pre-existing defects are the primary issues for performance and long-term reliability of Hf-based high-κ gate stacks. Further characterization of these defects can be carried out by conducting deep level transient spectroscopy (DLTS) studies, which are essential to understand not only activation energies of defects but also capture cross section, trapping efficiency etc. of the dominant traps. This research further shows that temperature dependent wear-out is significant in metal gate/high-κ gate stacks, specifically under substrate injection. To understand effects of temperature on breakdown mechanisms, extensive temperature dependent TDDB studies need to be performed to understand how temperature affects regimes of degradation like SBD and PBD. To enhane performance further, specifically electron mobility, alternative channel materials like Si_xGe_{1-x}, GaAs are being seriously considered to replace Si in high-κ gate stacks. Reliability studies of these gate stacks appear to be a reasonable extension of this work into future.

REFERENCES

[1] A. S. Oates, " Reliability Issues for High-K Gate Dielectrics," in *IEEE* Electron Dev. Meeting, 2003, pp. 923-926.

[2] G. D. Wilk, R.M. Wallace, J. M. Anthony, "High-K gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics*, vol. 89, no. 10, pp. 5243-5253, May 2001.

[3] J. Robertson, "Interfaces and defects of high-*K* oxides on silicon, *Solid State Electronics*," vol. 49, no.1, pp. 283-293, Jan. 2005.

[4] H. F. Luan, B. Z. Wu, L. G. Kang, B. Y. Kim, R. Vrtis, D. Roberts, and D. L. Kwong, "Ultra thin high quality Ta_2O_5 gate dielectric prepared by in-situ rapid thermal processing," in *Tech. Dig. Int. Elect. Dev. Meet.*, 1998, pp. 609-613.

[5] S. A. Campbell, D. C. Gilmer, X.-C. Wang, M.-T. Hsieh; H.-S. Kim, W. L. Gladfelter, and J. Yan, "MOSFET transistors fabricated with high permitivity TiO_2 dielectrics," *IEEE Transactions on Electron Devices*, vol. 44, no.1, pp. 104-109, Jan. 1997.

[6] Z. Jin, H. S. Kwok, M. Wong," High-performance polycrystalline SiGe thin-film transistors using Al_2O_3 gate insulators Ultra thin high quality Ta_2O_5 gate dielectric," *IEEE Elect. Dev. Letts.*, vol. 19, no. 12, pp. 502-504, Dec. 1998.

[7] S. P. Muraka, and C. C. Chang," Thermal oxidation of hafnium silicide films on silicon," *Appl. Phys. Lett.*, vol. 37, no. 5, pp. 639-641, May 1980.

[8] J. A. Felix, D. M. Fleetwood, R. D. Schrimpf, J. G. Hwong, G. Lucovsky, J. R. Schwank, and M. R. Shaneyfelt, "Total Dose radiation Response of Hafnium-Silicate Capacitors," *IEEE Trans. On Nucl. Sci.*, vol. 49, no. 12, pp. 3191-3196, Dec. 2002.

[9] T. Yamaguchi, T. Ino, H. Satake and N. Fukushima, "Novel dielectric breakdown model of Hf-silicate with high temperature annealing," in *Int. Rel. Phys. Symp.*, 2003, pp. 34-37.

[10] C. D. Young, G. Bersuker, G. A. Brown, C. Lim, P. Lysaght and P. Zeitzoff, "Trapping characteristics of MOCVD hafnium based gate dielectric," in *Proceedings of Physics and Technology of High-K Gate Dielectrics II*, Electrochemical Society, 2003, pp. 347-356.

[11] C. D. Young, G. Bersuker, G. A. Brown, C. Lim, P. Lysaght and P. Zeitzoff, "Charge trapping in MOCVD hafnium based gate dielectric stack structures and its impact on device performance," in *IEEE International Reliability Workshop*, 2003, pp. 28-31.

[12] P. Punchaipetch, G. Pant, M. A. Quevedo-Lopez, C. Yao, M. El-Bouanani, M. J. Kim, R. M. Wallace, and B. E. Gnade, "Low-Temperature Deposition of Hafnium Silicate Gate Dielectrics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 10, no. 1, pp. 89- 94, Jan. 2004.

[13] R. Choi, S. J. Rhee, J. C. Lee, B. H. Lee, and G. Bersuker, "Trapping characteristics of Hf-silicate under static and dynamic trapping," *IEEE Elect. Dev. Lttrs.*, vol. 26, no. 3, pp. 197-199, Mar. 2005.

[14] G. Bersuker, J. Sim, C. Young, R. Choi, R. Harris, B. Lee, P. Zeitzoff, G. Brown, and H. Huff, "Charge Trapping Effects in High-k Transistors," in *ECS Transactions on High Dielectric Constant Gate Stacks III*, 2006, pp.246-254.

[15] H. R. Harris, R. Choi, J. H. Sim, C. D. Young , P. Majhi, B. H. Lee and G. Bersuker, "Electrical Observation of Deep Traps in High-k/Metal Gate Stack Transistors," *IEEE Elec. Dev. Lttrs.*, vol. 26, no. 12, pp. 839-841, Dec. 2005.

[16] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasaarathy, E. Vincent, and G. Ghibaudo, "Reliability of high-k oxides," *IEEE Tran. on Dev. & Mat. Rel.*, vol. 5, no. 1, pp. 5-19, Jan. 2005.

[17] S. C. Song, Z. Zhang, S. H. Bae, P. Kirsch, P. Majhi, R. Choi and B. H. Lee, "Ultra thin high-k oxides," in *Physics and Technology of High-K Dielectrics III*, 2006, pp. 231-241.

[18] B. H. Lee, Rino Choi, J. H. Sim; S. A. Krishnan, J. J. Peterson, G. A. Brown, and G. Bersuker, "Current reliability issues of high-k oxides," *IEEE Tran.on Dev. and Mat.*, vol. 5, no. 1, pp. 20-31, Jan. 2005.

[19] H. W. Lee, B. Sen, V. Filip and M. Poon, "Material properties of interfacial silicate layer and its influence on the electrical characteristics of MOS devices using hafnia as the gate dielectric," *Thin Solid Films* vol. 504, no. 1, pp.192-196, Jan. 2006.

[20] J. W. McPherson, Jinyoung Kim, Ajit Shanware, Homi Mogul, and John Rodriguez, "Trends in the Ultimate Breakdown Strength of High Dielectric-Constant Materials," *IEEE Trans. Electron Dev.*, vol. 50, no. 8, pp. 1771-1778, Aug. 2003.

[21] T. Kauerauf, R. Degaeve, E. Cartier, B. Govoreanu, P. Blomme, B. Kaczer, L. Pantisano, A. Kerbe and G. Groeseneken, "Towards understanding degradation and breakdown of SiO_2/high-k stacks," in *Int. Elect. Dev. Meet.*, 2002, pp.521 - 524.

[22] X. Garros, C. Leroux, G. Reimbold, J. Mitard, B. Guilaaumot, P. Martin, J. L. Autran, "Reliability assesssment of ultra-thin HfO_2 oxides with TiN gate and polysilicon n+ gate," *IEEE International Reliability Workshop,* 2004, pp. 176-180.

[23] E. A. Cartier, "High-k reliability models," in *SEMATECH 2nd Int. Workshop on Adv. Gate Stack Tech.*, 2005, p.83 .

[24] G. Lucovsky, C.C. Fulton, Y. Zhang, Y. Zou, J. Luning, L. Edge, J. Whitten, R.J. Nemanich, H. Ade, D.G. Schlom, V.V. Afanase'v, "Root cause of trapping in high-k oxides," in *SEMATECH International Workshop on Electrical Characterization and Reliability for High-k Devices*, 2004, p.95

[25] R. Choi, R. harris, B. H. Lee, C. D. Young, J. H. Sim, and G. Bersuker, "Charge trapping under AC stress in high-k oxides," in *SEMATECH International workshop on Electrical Characterization and Reliability for High-k Devices*, p. 153, 2004.

[26] V. V. Afanas'ev and A. Stesmans, "Evidence of E' centers in high-k oxides," *Journal of Appl. Phys.*, vol. 95, No. 5, pp. 2518-2525, May 2005.

[27] E. P. Gusev, and C. P. D'Emic, "Charge trapping in HfO_2 high-k gate dielectric stacks," *Appl. Phys. Lttrs.*, vol. 83, no. 22, pp. 5223-5226, Nov. 2003.

[28] Sufi Zafar, Alessandro Callegari, Evgeni Gusev, and Massimo V. Fischetti, "Physical model of charhe trapping in HfO_2," *Journal of Appl. Phys.,* vol. 93, no. 10, pp. 9298-9308, Oct. 2003.

[29] M. Houssa, *High-k Gate Dielectrics*. Philadelphia, PA: Institute of Physics Publishing Ltd., 2004, pp. 467-495.

[30] M. Houssa, *High-k Gate Dielectrics*. Philadelphia, PA: Institute of Physics Publishing Ltd., 2004, pp. 284-291.

[31] F. Crupi, R. Degraeve, A. Kerber, D. H. Kwak, and G. Groeseneken, "Correlation between Stress-Induced Leakage Current (SILC) and the HfO_2 bulk trap density in a SiO_2/HfO_2 stack," in *IEEE Int. Rel. Phys. Symp.*, 2004, pp. 181-184.

[32] M. Houssa, S. De Gendt, G. Groeseneken, and M. M. Heyns, "NBTI effects i In HfO_2 p-channel," *J. of Electrochem. Soc.,* vol. 151, no. 1, pp. 288-291, Jan. 2004.

[33] A. S. Foster, F. L. Gejo, A. L. Shluger and R. M. Nieminen, "Vacancy and Interstitial defects in hafnia," *Phys. Rev. B*, vol. 65, no. 17, pp. 174117:1-174117:13, Sep. 2002.

[34] J. L. Gavartin, D. Munoz-Ramo, A. L. Shluger and G. Bersuker, "Defect energy levels in HfO_2," in *SEMATECH 2nd Int. Workshop on Adv. Gate Stack Tech.*, 2005, p.56.

[35] K. Torii, K. Shirashi,,S. Miyazaki, K. Yamabe, M. Boero, T. Chikyow, K. Yamada, H. Kitajima and T. Arikado, "Physical model of BTI, TDDB, and SILC in HfO_2-based high-k gate dielectrics," in *Electron Dev. Meeting*, 2004, pp.129-132.

[36] J. Robertson and K. Xiong, "Defect levels in Hafnia," in *SEMATECH 2nd Int. Workshop on Adv. Gate Stack Tech.*, 2005, p.55.

[37] J. Robertsom, K. Xiong and B. Falabretti, "Defect levels in ZrO_2," *Transaction on Dev. & Mat. Rel.*, vol. 5, no. 1, pp. 84-90, Jan. 2005.

[38] J. L. Gavartin, L. Fonseca, G. Bersuker and A. L. Shluger, "*Ab initio* Modeling of structure and defects at the HfO_2/Si interface," *Microelectronic Eng.*, vol. 80, no. 3, pp. 412-416, Apr. 2005.

[39] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasaarathy, E. Vincent, and G. Ghibaudo, "Origin of Vt instabilities in high-k dielectrics Jahn-Teller effect or oxygen vacancies," *IEEE Tran. on Dev. & Mat. Rel.,* vol. 6, no. 2, pp. 132-135, June 2006.

[40] A. Paskaleva, A. J. Bauer, M. Lemberger, and S. Zurcher, "Different current conduction mechanisms through thin high-k $Hf_xTi_ySi_zO$ films due to the varying Hf to Ti ratio," *J of Appl Phys.*, vol. 95, no. 7, pp. 5583-5590, Jul. 2004.

[41] J. L. Gavartin, A. L. Shluger, A. S. Foster and G. I. Bersuker, "The role of nitrogen-related defects in high-k dielectric oxides: Density-functional studies," *Jnl. of Appl. Phys.*, vol. 97, no. 6, pp. 0553704: 1- 0553704: 9, June 2005.

[42] C. Leroux, J. Mitard, G. Ghibaudo, X. Garros, G. Reimbold, B. Guillaumot and F. Martin, "Characterization and modeling of hysteresis phenomena in high K dielectrics," in *IEEE Electron Dev. Meeting*, 2004, pp. 737-740.

[43] Zhen Xu, Luigi Pantisano, Andreas Kerber, Robin Degraeve, Eduard Cartier, Stefan De Gendt, Marc Heyns, and Guido Groeseneken, "A Study of Relaxation Current in High-k Dielectric Stacks," *IEEE Trans. on Elect. Dev.*, vol. 51, no. 2, pp.402-408, Feb. 2004.

[44] C. Shen, M .F. Li, H. Y. Yu, X. P. Wang, Y. –C. Yeo, D .S. H. Chan, and D. L. Kwong, "Negative-U centers in HfO_2," *Applied Physics Letters*, vol. 86, no. 2, pp. 093510:1-093510:3, March 2005.

[45] H. R. Harris, R. Choi, B. H. Leea, C. D. Young, J. H. Sim, K. Mathews, P. Zeitzoff, P. Majhi, and G. Bersuker, "NBTI effectrs in in High-k/Metal Gate Stack p-Channel Transistors," in *Int. Rel. Phys. Symp.*, 2005, pp. 80-83.

[46] E. Cartier, "O vacancies in HfO_2," in *VLSI Technology Symposium*, 2005, pp. 230-231.

[47] M. Houssa, *High-k Gate Dielectrics*. Philadelphia, PA: Institute of Physics Publishing Ltd., 2004, pp. 65-85.

[48] P. Lysaght, B. Foran, S. Stemmer, G. Bersuker, J. Bennett, R. Tichy, L. Larson, and H. R. Huff, "Thermal response of MOCVD hafnium silicate," *Microelectronic Engineering*, vol. 69, no. 1, pp. 182-189, May 2003.

[49] M. Houssa, *High-k Gate Dielectrics*. Philadelphia, PA: Institute of Physics Publishing Ltd., 2004, pp. 17-27.

[50] J. Barnett, N. Moumen, J. Gutt, M. Gardner, C. Huffman, P. Majhi, J. J. Peterson, S. Gopalan, B. Foran, H.-J. Li, B. H. Lee, G. Bersuker, P. Zeitzoff, G. A. Brown, P. Lysaght, C. D. Young, R. W. Murto, and H. R. Huff, "Physical characteristics of MOCVD Hf-silicate based n-MOSFETs," in *Spring Meeting of Mat. Res. Soc.*, 2004; p. E1.4.1.

[51] C.D. Young, N. Moumen, J. Gutt, M. Gardner, C. Huffman, P. Majhi, J. J. Peterson, S. Gopalan, B. Foran, H.-J. Li, B. H. Lee, G. Bersuker, and P. Zeitzoff, "MOCVD metal gate/Hf-silicate gate stacks," in *IEEE Int. Reliability Workshop*, 2003, pp. 41-45.

[52] P. S. Lysaght, B. Foran and G. Bersuker, "Physical and electrical properties of hafnium silicate thin films," in *Proceedings of Materials Research Society Symposium*, 2003, pp.133-139.

[53] T. Kundu, R. Garg, N. Chowdhury, and D. Misra, "Electrical characterization of high-k dielectrics," *The Electrochemical Society Interface*, pp. 23-27, Oct. 2005.

[54] M. Houssa, *High-k Gate Dielectrics*. Philadelphia, PA: Institute of Physics Publishing Ltd., 2004, pp. 151-156.

[55] D. K. Schroder, *Semiconductor Material and Device Characterization*, New York, NY: John Wiley and Sons, 1998; pp. 242-248.

[56] B. G. Streetman and S. K. Banerjee, *Solid State electronic Devices*, Saddle River, NJ: Prentice Hall 2000, pp. 255-257.

[57] D. K. Schroder, *Semiconductor Material and Device Characterization*, New York, NY: JohnWiley and Sons, 1998; pp. 386-388.

[58] J. Mitard, C. Leroux, G. Ghibaudo, G. Reimbold, X. Garros, B. Guillaumot, and F. Boulanger, "Transient trapping in HfO_2 n-MOSFEts," *Microelectronic Engineering*, vol. 80, no. 1, pp.362-366, Jan. 2005.

[59] M. V. Fischetti, R. Gastaldi, F. Maggioni, and A. Modelli, "Slow and fast states induced by hot electrons at Si-SiO_2 interface," *J. of Appl. Phys.*, vol. 53, no. 8, pp. 3136-3194, March 1982.

[60] G. Bersuker, J. Sim, C. Young, R. Choi, R. Harris, B. Lee, P. Zeitzoff, G. Brown, andH. Huff, "Charge Trapping Effects in High-k Transistors," in *ECS Transactions on High Dielectric Constant Gate Stacks III*, 2006, pp. 261-267.

[61] J. L. Gavartin, D. Munoz-Ramo, A. L. Shluger and G. Bersuker, "Shallow and deep electron traps near $HfO_2/SiO_x/Si$ interface: Ab initio modeling," in *SEMATECH 2nd Int. Workshop on Adv. Gate Stack Tech.*, 2005, p. 56.

[62] J. Robertson and K. Xiong, "Defect Energy levels in HfO_2 and ZrO_2," in *1st Int. Workshop on Adv. Gate Stack Tech.*, 2005, p.55.

[63] K. Yamabe, M. Goto, K. Higuchi, A. Uedono, K. Shiraishi and S. Miyazaki, "Charge trapping by oxygen-related defects in HfO_2-based high-k gate dielectrics," in *IEEE Int. Rel. Phys. Symp.*, 2005, pp.648-649.

[64] A. Kumar, M. V. Fischetti, T. H. Ning and E. Gusev, "Hot-carrier charge trapping and trap generation in HfO_2 and AlO_2 field-effect transistors," *J. of Appl. Phys.*, vol. 94, no. 3, pp. 1728-1738, Feb. 2003.

[65] S. C. Song, G. L. Zhang, S. H. Bae, P. Kirsch, P. Majhi, R. Choi, and B. H. Lee, "High Performance Metal Gate CMOSFETs with Aggressively Scaled Hf-Based High-k," in *ECS Trans.*, vol. 1, no. 5, pp. 609-618, Oct. 2006.

[66] N. Chowdhury, P. Srinivasan, and D. Misra, "Evidence of deep energy states from low temperature measurements and their role in charge trapping in metal gate/Hf-silicate gate stacks," in *ECS Trans.*, vol. 1, no. 5, pp. 767-775, Oct. 2006.

[67] M. Houssa, *High-k Gate Dielectrics*. Philadelphia, PA: Institute of Physics Publishing Ltd., 2004, pp. 390-392.

[68] S. Guha, E. Preisler, N. Bojarczuk, and M. Copel, "Materials Interaction at the Nanoscale in High-k Metal Gate Stacks: The Role of Oxygen," in *ECS Trans.*, vol. 1, no. 5, pp. 363-368, Oct. 2006.

[69] P. Srinivasan, N. A. Chowdhury, and D. Misra, "Charge Trapping in Ultrathin Hafnium Silicate/Metal Gate Stakcs," *IEEE Elect. Dev. Lettrs.*, vol. 26, no. 12, pp. 913-915, Dec. 2005.

[70] M. V. Fischetti, "Generation of positive charge in silicon dioxide during avalanche and tunnel electron injection," *J. Appl. Phys.*, vol. 57, no. 8, pp. 2860-2879, April 1985.

[71] O. Blank, H. Reisinger, R. Stengl, M. Gutsche, F. Wiest, V. Capodieci, J. Schulze and I. Eisele, "A model for multistep trap-assisted tunneling in thin high-k dielectrics," *J. Appl. Phys.*, vol. 97, no. 4, pp. 044107: 1-044107-7, Feb. 2005.

[72] Wei Yip Loh, Byung Jin Cho, Moon Sig Joo, M.F. Li, Daniel SH Chan, Shajan, Mathew, Dim-Lee Kwong, "Analysis of Charge Trapping and Breakdown Mechanism in High-K Dielectrics with Metal Gate Electrode using Carrier Separation," in *Int. Elect. Dev. Meet.*, 2003, pp. 927-930.

[73] D. J. DiMaria and E. Cartier, "Mechanism for stress-induced leakage currents in thin silicon dioxide films," *Journal of Applied Physics*, vol. 78, no. 8, pp. 3883-3995, May 1995.

[74] J. L. Autran, D. Munteanu, R. Dinescu, and M. Houssa, "Stretch-out of high -permittivity MOS capacitance-voltage curves resulting from a lateral non-uniform oxide charge distribution," *Journal of Non-Crystalline Solids,* vol. 322, no. 2, pp.219-225, June 2003.

[75] J. T. Watt and J. D. Plummer, "Dispersion of MOS Capacitance-Voltage Characteristics Resulting from the Random Channel Dopant Ion Distribution," *IEEE Trans. on Electron Dev.*, vol. 41, no. 11, pp. 2222-2232, Nov. 1994.

[76] C. R. Viswanathan, R. Divakaruni, and J. Kizziar, "Low-temperature CV Dispersion in MOS devices," *IEEE Elect. Dev. Lttrs.*, vol. 12, no. 9, pp. 503-505, Sep. 1994.

[77] R. Divakaruni, V. Prabhakar and C. R. Viswanathan, "Activation Energy Determination from Low-Temperature CV Dispersion," *IEEE Trans. on Elect. Dev.*, vol. 41, no. 8, pp. 1405-1413, Aug. 1994.

[78] H. Kufluoglu and M. A. Alam, "Theory of interface-trap-induced NBTI degradation for reduced cross section MOSFETs," *IEEE Trans. Elect. Dev.*, vol. 53, no. 5, pp. 1120-1130, May 2006.

[79] M. Aoulaiche, M. Houssa and R. Degraeve, "AC and DC NBTI effects in High-k p-MOSFETs," *Microelec. Engnr.*, vol. 80, no. 1, pp. 134-139, Jan. 2005.

[80] S. Fujieda, "Negative bias temperature instability in Hf-silicates," *Jap. Jnl. of Appl. Phys.*, vol. 44, no. 11, pp.2385-2392, Nov. 2005.

[81] D. Misra and N. A. Chowdhury, "Charge Trapping in High-k Gate Dielectrics: A Recent Understanding," in *ECS transactions on Dielectrics for Nanosystems II: Materials Science, Processing, Reliability, and Manufacturing*, 2006, pp. 311-321.

[82] N. A. Chowdhury, P. Srinivasan and D. Misra, "Evidence of deep energy states from low temperature measurements and their role in charge trapping in metal gate/Hf-silicate gate stacks," *ECS transactions on Physics and Technology of High-k Gate Dielectrics III*, 2005, pp. 767- 776.

[83] Y. Shi, T. P. Ma, S. Prasad and S. Dhanda, "Polarity dependent gate tunneling currents in dual-gate CMOSFETs," *IEEE Trans. Elect. Dev,*. vol. 45, no 11, pp. 2355-2360, Nov. 1998.

[84] S. Mahapatra, P. B. Kumar, and M. A. Alam, "Investigation and modeling of interface and bulk trap generation during negative bias temperature instability of p-MOSFETs," *IEEE Trans. Elect. Dev,*.vol. 51, no. 9, pp. 1371- 1379, Sep. 2004.

[86] N. A. Chowdhury, P. Srinivasan, D. Misra, R. Choi and B. H. Lee, "Observation of deep bulk defects using low temperature techniques in $TiN/HfSi_xO_y$ gate stack and their role in BTI and HCS effects," in *Proceedings of 2nd SEMATECH International Symposium on Advanced Gate Stacks Technology*, 2005, p.77.

[87] M. Houssa, G. Pourtois, M. M. Heyns, and A. Stesmans, "Modeling of NBTI induced H- diffusion in high-k oxides," *J. of Physics: Cond. Matter*, vol. 17, no. 3 , pp. S2075- S2084, March 2005.

[88] H. Wong, B. Sen, V. Filip and M. C. Poon, "Material properties of interfacial silicate layer and its influence on the electrical characteristics of MOS devices using hafnia as the gate dielectric," *Thin Solid Films*, vol. 504, no. 1, pp. 192-196, March 2006.

[89] J. W. McPherson, J. Kim, A. Shanware, H. Mogul, and J. Rodriguez, "Trends in the Ultimate Breakdown Strength of High Dielectric-Constant Materials," *IEEE Trans. Elect Dev.*, vol. 50, no. 8, pp. 1771-1778, Aug. 2003.

[90] J. McPherson, J-Y. Kim, A. Shanware, and H. Mogul, "Thermochemical description of dielectric breakdown in high dielectric constant materials," *Appl. Phys. Lttrs.*, vol. 82, no. 13, 2003, pp. 2121-2123, Sep. 2003.

[91] R. Degaeve, E. Cartier, B. Govoreanu, P. Blomme, B. Kaczer, T. Kauerauf, L. Pantisano, A. Kerber, G. Groeseneken, "Degradation and breakdown of SiO_2/high-k stacks," in *IEEE Int. Elect. Dev. Meet.*, 2002, pp.524 - 527.

[92] X. Garros, C. Leroux, G. Reimbold, J. Mitard, B. Guilaaumot, P. Martin, J. Autran, "Reliability assessment of ultra-thin HfO_2 oxides with TiN gate and polysilicon n+ gate," in *IEEE Int. Rel. Phys. Symp.*, 2004, pp. 176-180.

[93] G. Ribes, S. Bruyere, M. Denais, F. Monsier, D. Roy, E. Vincent, G. Ghibaudo, "High-k dielectrics breakdown accurate lifetime assessment methodology," in *IEEE Int. Rel. Phys. Symp*, 2005, pp. 61-66.

[94] F. Palumbo, R. Pagano, S. Lombardo,S.A. Krishnan, C. Young, R. Choi, G. Bersuker, P. Kirsch, and J. H. Stathis, "Evidence of progressive breakdown in high-k metal gate nFETs," in *SEMATECH Int. Symp. on Advanced Gate Stacks Technology*, 2006, p. 54.

[95] C. D. Young, D. Heh, S. V. Nadkarni, R. Choi, J. J. Peterson, J. Barnett, B. H. Lee, and G. Bersuker, "Electron Trap Generation in High-κ Gate Stacks by Constant Voltage Stress," *IEEE Tran. Elect. Dev. Meet.*, vol. 6, no. 2, pp. 123-131, June 2006.

[96] S. A. Krishnan, J. J. Peterson, C. D. Young, G. Brown, R. Choi, R. Harris, B. H. Lee, and G. Bersuker, "Dominant SILC mechanisms in HfO2/TiN Gate NMOS and PMOS Transistors," in *IEEE Int. Rel. Phys. Symp.*, 2005, pp. 642-643.

[97] G. Bersuker, C. S. Park, J. Barnett, P. S. Lysaght, P. D. Kirsch, C. D. Young, R. Choi, B. H. Lee, B. Foran, K. van Benthem, S. J. Pennycook, P. M. Lenahan and J. T. Ryan, "The effect of interfacial layer properties on the performance of Hf-based gate stack devices," *Jnl. Appl. Phys.*, vol. 100, no. 9, pp: 094108:1 – 094108:6, April 2006.

[98] D. Heh, C. D. Young, G. A. Brown, P. Y. Hung, G. Bersuker, E. M. Vogel, and J. B. Bernstein, "Spatial distributions of trapping centers in HfO_2/SiO_2 gate stacks," *Appl. Phys. Lttrs.* vol. 88, no. 15, pp. 152907:1 – 152907:3, Aug. 2006.