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ABSTRACT

CHARACTERIZATION AND MODELING OF LOW-FREQUENCY NOISE IN Hf-BASED HIGH- κ DIELECTRICS FOR FUTURE CMOS APPLICATIONS

by

Purushothaman Srinivasan

The International Technology Roadmap for Semiconductors outlines the need for high- κ dielectric based gate-oxide Metal Oxide Semiconductor Field Effect Transistors for sub-45 nm technology nodes. Gate oxides of hafnium seem to be the nearest and best alternative for silicon dioxide, when material, thermal and structural properties are considered. Usage of poly-Si as a gate electrode material degrades the performance of the device and hence gate stacks based on metal gate electrodes are gaining high interest. Though a substantial improvement in the performance has been achieved with these changes, reliability issues are a cause of concern. For analog and mixed-signal applications, low-frequency ($1/f$) noise is a major reliability factor. Also in recent years, low frequency noise diagnostics has become a powerful tool for device performance and reliability characterization.

This dissertation work demonstrates the necessity of gate stack engineering for achieving a low $1/f$ noise performance. Changes in the material and process parameters of the devices, impact the $1/f$ noise behavior. The impact of $1/f$ noise on gate technology and processing parameters were identified and investigated. The thickness and the quality of the interfacial oxide, the nitridation effects of the layers, high- κ oxide, bulk properties of the high- κ layer, percentage of hafnium content in the high- κ , post deposition anneal (PDA) treatments, effects of gate electrode material (poly-silicon, fully silicided or metal),

gate electrode processing are investigated in detail. The role of additional interfaces and bulk layers of the gate stack is understood. The dependence of low-frequency noise on high and low temperatures was also investigated. A systematic and a deeper understanding of these parameters on $1/f$ noise behavior are deduced which also forms the basis for improved physics-based $1/f$ noise modeling. The model considers the effect of the interfacial layer and also temperature, based on tunneling based thermally activated model. The simulation results of improved drain-current noise model agree well with the experimentally calculated values.

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HF-BASED HIGH- κ DIELECTRICS FOR FUTURE CMOS APPLICATIONS**

by

Purushothaman Srinivasan

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LIST OF SYMBOLS

- c – Capture coefficient[no unit]
 $c_{p_{HK,IL}}$ – capture probability of traps in IL,HK[no unit]
 $c_{n,p}$ – capture probability of electron, hole[no unit]
 C_{inv} - Inversion layer capacitance [μF]
 D_{it}, D_{IT} – Interface Trap Density [cm^{-2}]
 EOT – Equivalent oxide thickness[nm]
 $e_{n,p}$ – emission probability of electron, hole[no unit]
 $e_{p_{IL, HK}}$ – emission probability of (hole) traps in IL,HK[no unit]
 $E_{IL, HK}$ – Trap energy level in the IL,HK[eV]
 f_p – fraction of empty SRH centers[no unit]
 f_i – fraction of SRH centers occupied by electrons[no unit]
 g_m, g_M, G_m, G_M – Transconductance[A/V]
 I_{cp}, I_{CP} – Charge Pumping Current [A]
 I_d, I_D – Drain Current[A]
 I_g, I_G – Gate Current[A]
 $m_e^{(*)}$ _{HfO_2, SiO_2} – (Effective) mass of electron at IL,HK[g]
 $m_h^{(*)}$ _{HfO_2, SiO_2} – (Effective) mass of hole at IL,HK[g]
 m_0 – mass of electron[g]
 n_i – Intrinsic carrier density[cm^{-3}]
 $n_{0,1,2}$ – Number of carriers per unit volume total,IL,HK[$\#/cm^3$]
 $N_{0,1,2}$ – Trap densities at total,IL,HK[cm^{-3}]
 N_T, N_i – Volume Trap Density[$1/cm^3$]
 N_T, D_i – Surface Trap Density[$1/cm^2$]
 $p_{1,2}$ - Density of holes at the Si/IL,IL/HK interface[cm^{-3}]
 $p_{IL, HK}$ – Density of holes at a given distance y[cm^{-3}]
 $S_I, S_{id}, S_{iD}, S_{ID}$ – Drain Current Noise Spectral Density [A^2/Hz]

LIST OF SYMBOLS

(continued)

$$S_I / I_D^2, S_{id} / I_d^2, S_{iD} / I_D^2, S_{ID} / I_D^2$$

– Normalized Drain Current Noise Spectral Density [1/Hz]

$$S_{V_G}, S_{V_g} \text{ – Input Referred Noise Spectral Density [V}^2\text{/Hz]}$$

$t_{IL, HK}$ – Thickness of the interfacial layer, high-k layer [nm]

t_{ox} – Thickness of gate oxide [nm]

V_g, V_G, V_{GS}, V_{gs} – Gate to Source Voltage [V]

$V_{gs} - V_t, V_g - V_t, V_{GS} - V_T$ – Gate Voltage Overdrive [V]

V_t, V_T – Threshold Voltage [V]

V_{ds}, V_{DS} – Drain to Source Voltage [V]

α_H – Hooge's parameter [no unit]

$\alpha_{IL, HK}$ – Tunneling coefficients at the IL, HK [cm^{-1}]

$\delta n_{0,1,2}$ – Charge fluctuations in the carrier density total, IL, HK [no unit]

$\phi_{IL, HK}$ – Potential barrier height at the IL, HK [eV]

τ_{GM} – Geometric mean of all the trap time constant [μsecs]

τ_{net} – Net trap time constant [μsecs]

$\tau_{0, IL}$ – Initial trap time constant at the IL layer [μsecs]

$\tau_{0, HK}$ – Initial trap time constant at the HK layer [μsecs]

$\tau_{IL, HK}$ – Trap time constants of the IL, HK [μsecs]

CHAPTER 1

INTRODUCTION

Over the last 30 years CMOS (Complementary Metal Oxide Semiconductor) technology has been improving at a very high rate. Improving the technology was meant to increase the device speed, reduce the costs, and decrease the transistor sizes. In the 1970's scaling of the device dimensions was introduced to increase the device density and reduce the transistor costs. The key concept in scaling, introduced by Dennard at IBM [1], is that the various structural parameters of the MOSFET should be scaled appropriately, if the device is to keep functioning properly. If the lateral dimensions (channel length and width) are reduced by a factor of α , so should be the vertical dimensions such as source/drain junction depths and gate dielectric thickness.

The microelectronics industry managed to increase the device density per chip and decrease the feature size continuously for more than three decades. From the early 70's until mid 90's the industry followed the so-called constant voltage scaling. In this constant voltage scaling mode, the gate voltage is kept constant whereas oxide thickness and device dimensions are reduced by a factor of $1/\alpha$. This degraded the oxide integrity due to increasing the oxide field and hence process improvements were required. In addition, this scaling resulted in other undesirable effects such as hot electron injection [2] and charge trapping in the oxides. Substantial improvements in the hot carrier charge trapping were made by introducing the lightly-doped drain device (LDD) structure [3].

Due to power consumption, leakage currents represent an important issue for further scaling of CMOS devices. There are three dominant sources of leakage: junction

leakage, gate leakage, and offstage leakage. These three sources of leakage increase as transistors are scaled down. With respect to other sources of leakage, gate-oxide scaling has long been considered an eventual limiter [4] for gate oxides below $\sim 2\text{nm}$ gate dielectric thickness. With the oxides reaching the thickness of several atoms, gate leakage would rival and would surpass the transistor off-current leakage. Figure 1.1 shows the gate current versus gate bias for the 0.8nm oxides. The measurement results show [5] that at 0.85V and 100°C , the gate leakage value is in the mid- $10^{-8}\text{A}/\mu\text{m}^2$, approaching the off-state leakage level of the 30nm L_g transistor as shown in Figure 1.2 [6].

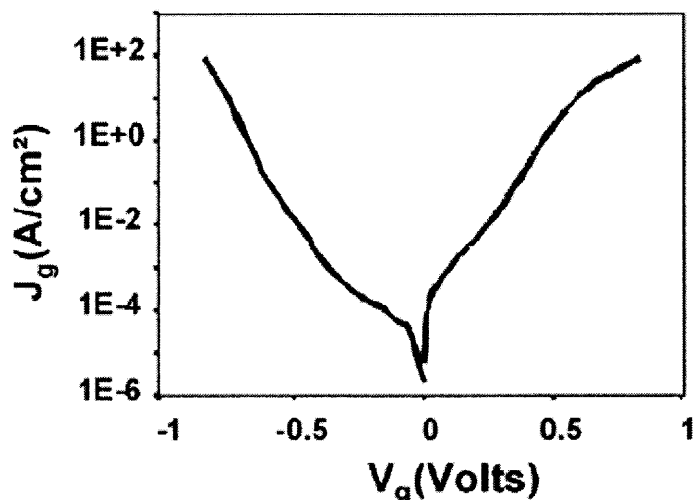


Figure 1.1 Gate current leakage for a 0.8nm oxide for the 30nm transistor. source:[5].

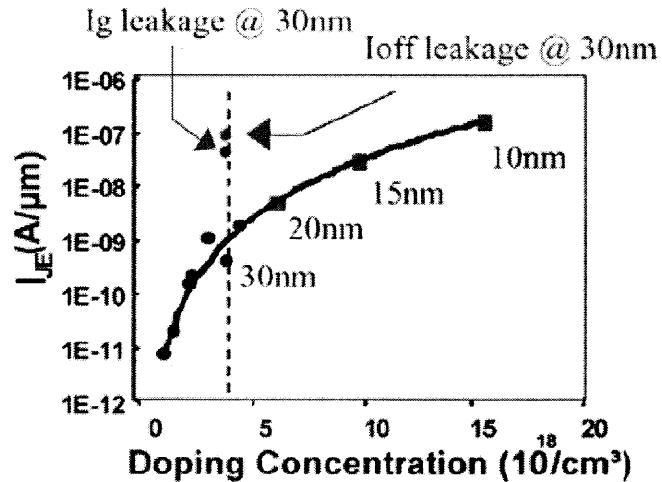


Figure 1.2 Junction leakage vs doping concentration of the substrate. Circles represent data points. Squares represent extrapolated points for future technology nodes. source:[6]

To limit the gate leakage current, alternate gate oxide materials with high dielectric constant are explored. These high dielectric constant materials help to achieve higher physical oxide thickness, thereby reducing the gate leakage current considerably.

Based on High-Performance (HP) or Low-Stand by Power (LSTP) technology consideration, an Equivalent Oxide Thickness (EOT) of 1 nm or less will be required. EOT is generally calculated as

$$\text{EOT} = (\epsilon_{\text{OX}}/\epsilon_{\text{IL}}) * t_{\text{IL}} + (\epsilon_{\text{OX}}/\epsilon_{\text{HK}})t_{\text{HK}} \quad (1.1)$$

where t represents the thickness, ϵ represents permittivity constant, the subscript OX in Equation 1.1 refers to SiO_2 layer, IL refers to interfacial layer and HK refers to high- κ layer. In order to achieve an EOT of less than 1nm, the formation of an interfacial layer, prior and after deposition should be minimized.

1.1 Requirements for alternative high- κ gate dielectric

The scaling requirements for future CMOS technologies is generally guided by International Technology Roadmap for Semiconductors (ITRS) [7], where the introduction of alternative gate high- κ dielectrics is predicted for 2005 to 2007, depending on the technology application as shown in Figures 1.3 and 1.4. For the high-performance (HP) technologies dielectric scaling is more aggressive and will reach the sub-1 nm regime. On the other hand, the leakage current requirements are more relaxed and the introduction of high- κ dielectrics is not expected before 2007. It is likely that high- κ dielectrics are first introduced in low-standby power (LSTP) technologies, due to the fact that the leakage current specifications cannot be met with conventional gate dielectrics in the sub 1.5 nm regime.

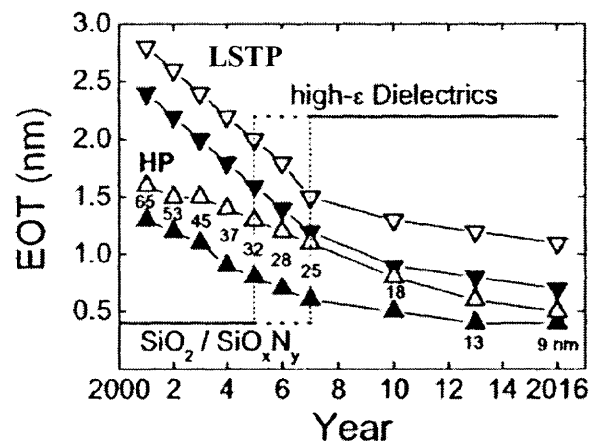


Figure 1.3 Equivalent Oxide Thickness (EOT) versus year of introduction for both High-Performance (HP) and Low Standby-Power (LSTP) technologies. For comparison the minimum (solid symbols) and maximum (open symbols) EOT is shown for each technology generation. The year of introduction for high- κ dielectrics is indicated between 2005 and 2007 as per ITRS 2005 specifications. source:[7].

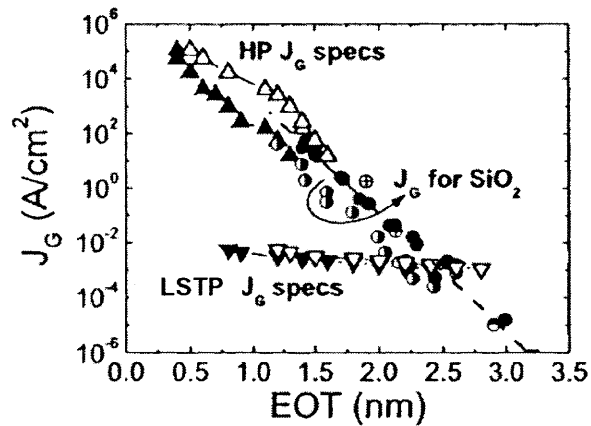


Figure 1.4 Gate leakage current specification versus EOT for High Performance and Low-Standby-Power technologies as per ITRS 2005 specifications. The same symbols for the minimum and maximum EOT are used as in Figure 1.3. Experimental data for SiO_2 from different companies are included to demonstrate the necessity for high- κ dielectrics for LSTP technologies in the near future. source:[7].

To successfully replace SiO_2 material with a high- κ dielectric, a set of material properties should be considered. Table 1.1 shows a list of such material properties for high- κ integration.

A material which satisfies all of these considerations is yet to be identified, but several promising candidates which possess the majority of these material properties have been proposed and investigated [8].

Table 1.1 Material Properties to be Considered as an Alternative to the Present Gate Dielectric SiO₂

No	Property	Desirable requirement
1	Permittivity and Barrier height	Should have higher permittivity balanced against barrier height (band gap)
2	Thermodynamic stability on Si-substrate	Stable interface with Si-substrate upto the temperatures required for CMOS integration, which is typically 1000 C
3	Interface quality	High-quality interface with Si-channel with a midgap interface density of 2×10^{10} states/cm ²
4	Film morphology	Material to remain in amorphous state throughout CMOS processing
5	Gate electrode compatibility	Compatible with poly-Si or metal gate electrodes
6	Process compatibility	Compatible with current CMOS device processing with lesser cost and higher throughput
7	Reliability	Meets the electrical reliability criteria for application in CMOS technology

1.1.1 Electrical Requirements for Alternative Gate Dielectrics in Future CMOS Technologies

Apart from material properties considerations, there are certain electrical requirements that have to be met by future CMOS devices. The primary aim of introducing high- κ gate dielectrics is to reduce the gate leakage current. The main factors determining the gate leakage current are barrier height and physical thickness of the gate dielectric. Theoretical calculations predict that significant benefit in gate leakage can be expected for Al₂O₃, ZrO₂ and HfO₂.

Fixed charge and threshold voltage control are other important aspects when considering high- κ dielectrics. For a standard CMOS process, n- and p- degenerated poly-Si gate electrodes with work functions of 4 eV and 5 eV are used to control the threshold voltage V_T . A significant shift in V_T is often observed with high- κ dielectrics and poly-Si electrodes. This observed shift is commonly attributed to fixed charge in the dielectric layer that could be piled up either at the substrate/high- κ interface or distributed throughout the film. In order to control V_T a low fixed charge is necessary.

Charge trapping and threshold voltage instabilities are other points of attention for high- κ gate dielectrics. Investigations indicate that Negative Bias Temperature Instability and charge trapping due to gate stress is of concern for most of these materials. A significant understanding of charge trapping in high- κ dielectrics is made in Section 1.1.3.1.

Achieving high carrier mobility is considered to be essential for integration in SiO₂ based devices. A wide range of literature suggests that most high- κ devices suffer from severe mobility degradation. Scattering due to fixed charge or remote phonon scattering are proposed as origin for the mobility reduction. A detailed understanding of fixed charges and role of remote phonons is studied and explored in Section 1.1.3.2 for improving the carrier mobility in high- κ devices.

The above electrical properties are important when high- κ devices are considered for digital applications. However for mixed signal and analog applications, another essential parameter that needs to be considered is noise, and noise minimization is a key issue and often defines the sensitivity or detection limit in electronic circuits. Table 1.2 gives shows ITRS mixed-signal technology requirements of a MOSFET device.

Table 1.2 Mixed-Signal Technology Requirements of a MOSFET Device [7]

Year of Production	Physical Gate Length (nm)	NMOS RF Device		NMOS Analog Device	
		T_{ox} (nm)	$1/f$ noise* ($\mu V^2 \mu m^2 / Hz$)	T_{ox} (nm)	$1/f$ noise* ($\mu V^2 \mu m^2 / Hz$)
2001	65	1.3 - 1.6	500	2.5 - 7.0	1000
2002	53	1.2 - 1.5	500	2.5 - 7.0	500
2003	45	1.1 - 1.6	300	2.5 - 5.0	500
2004	37	0.9 - 1.4	300	2.5 - 5.0	500
2005	32	0.8 - 1.3	300	2.5 - 5.0	300
2006	28	0.7 - 1.2	200	2.5 - 5.0	300
2007	25	0.6 - 1.1	200	2.5 - 5.0	300
2010	18	0.5 - 0.8	150	1.3 - 3.0	150
2013	13	0.4 - 0.6	100	1.3 - 3.0	100
2016	9	0.4 - 0.5	75	1.3 - 2.5	100

Presently, LF noise receives a growing interest from the microwave community as well. The reason is that the LF noise has a major impact on the phase noise of nonlinear circuits and devices in the GHz region. Secondly, a $1/f$ noise spectrum is up-converted to high frequencies giving rise to a $1/f^3$ sideband around the carrier frequency. A third motivation for the study of noise is that it is a strongly technology sensitive parameter [9], which in some cases can also be used as a predictive or diagnostic tool for device lifetime and reliability. This work focuses on low-frequency noise in high- κ gate dielectrics. In particular, the low frequency noise is investigated in detail as a function of technological and processing parameters.

1.1.2 Hf-Based Dielectrics

Various high- κ gate dielectrics have been proposed as an alternative to SiO_2 in recent years, and the range of the dielectric constant (k) is scattered from 5~8 for Si_3N_4 to > 100 for ferroelectrics. To make it simpler, the dielectrics can be categorized into three groups [10] – ultra high- κ ($k > 100$), moderate high- κ ($4 < k < 10$) and mid-range high- κ ($10 < k < 100$).

The ultra high- κ materials such as BST ((Ba, Sr) TiO_3 , $\kappa \sim 300$), are the most advantageous in achieving thinner equivalent oxide thickness (EOT), but they suffer from so-called Field Induced Barrier Lowering (FIBL) effect problem. The physical thickness of these materials will be so thick that the cross-section will be rectangular with a high H/L (height/length) ratio. The channel potentials will be controlled by not only the gate electrode but also the source and drain and the MOSFETs will be difficult to turn-off. Though this problem can be relieved by introducing a low- κ interfacial layer, this will cancel out the advantages of the ultra high- κ dielectric.

Si_3N_4 and Al_2O_3 are well-known candidates for the moderate high- κ materials. These are common materials in the CMOS industry, but the main issue is that the dielectric constant of Si_3N_4 is not high enough to achieve the advantage of suppressing the gate leakage current significantly. Charge traps due to high nitrogen concentration are also a concern. For Al_2O_3 , mobility degradation due to Coulomb scattering from the fixed charges in the high- κ dielectric, limits the drive current of MOSFETs.

Considering the disadvantages of ultra- and moderate high- κ materials, it was found that mid-range high- κ materials were preferable for the gate dielectric application. A variety of high- κ materials have been reported as possible candidates.

ZrO₂ and HfO₂ emerged as promising high- κ dielectrics for ultra-thin gate dielectric application. Their dielectric characteristics were well behaved and similar to each other. However, it was found that ZrO₂ was not compatible [11] with the polysilicon gate electrode, unlike HfO₂, which exhibited excellent MOSFET characteristics. Introduction of nitrogen in Zirconium solved the issue to some extent but it was found that ZrON still reacted with polysilicon [12] and the gate leakage current increased with polysilicon gate compared to those with metal gate electrodes. HfO₂ is expected to be more thermally stable because of its chemical and bonding similarities with Si.

Other important materials that were considered for possible high- κ candidates were Ta₂O₅ [13] and TiO₂. However, these materials were not stable in contact with Si substrate and formed low- κ interfacial layers, which cancelled out the advantage of high- κ value.

1.1.3 Reliability Considerations for Hf-Based Dielectrics

As HfO₂ emerged as a strong contender based on the above thermodynamic and material property considerations, various device reliability issues need to be addressed, before its implementation. HfO₂ presents various reliability issues such as boron penetration, low crystallization temperature, positive and negative bias temperature instabilities, charge trapping and low channel mobility [8]. It has been recently found out that these high- κ dielectrics were susceptible to oxygen diffusion related issues [14]. A considerable progress has been achieved in all these areas through various gate stack engineering methods which are extensively described in literature. Some of the significant gate stack engineering processes are the introduction of SiO₂ interfacial layer, mixing of Hf/Si in

right proportion for the required performance consideration and the introduction of metal gates. The introduction of metal gates is an important milestone in the engineering process, and nevertheless this should be considered as a major area of scientific study. This dissertation investigates the influence of some of the major gate technological and processing issues in relationship with $1/f$ noise, which is described in detail in Section 1.2. This is especially significant if the high- κ dielectrics are considered for analog or mixed-signal applications.

Alloys and mixtures of hafnium with silicon called as hafnium silicates have also been considered as an alternate dielectric. The dielectric constants of these silicates depend on the Hf/Si mixture percentage. They offer better leakage characteristics, improved ΔV_t , lower mobility degradation and allow larger thermal budgets during processing than HfO_2 [4]. The next two subsections deal with two important issues of Hf-based high-k devices on reliability to be considered for digital applications:

- (i) Charge Trapping and
- (ii) Mobility.

Various researchers have investigated the effects of charge trapping in Hf-based devices with poly-Si based gate electrodes [16, 18, 19]. The following sub-section investigates the charge trapping characteristics of MOCVD HfSi_xO_y (20% SiO_2) gate stack with TiN gate by applying constant voltage stress (CVS) and constant current stress (CCS) on n-MOSFETS, in substrate injection mode.

1.1.3.1 Charge Trapping in Hf-based High- κ Dielectrics. This section deals with charge trapping characteristics of Metal Organic Chemical Vapor Deposition (MOCVD) HfSi_xO_y (20% SiO_2) gate stack with TiN gate. Constant Voltage Stress (CVS) and

Constant Current Stress (CCS) on n-MOSFETS, in substrate injection mode were applied in order to understand the effects of charge trapping. Transistors used here were fabricated at SEMATECH, Austin by standard CMOS process flow where MOCVD was used to deposit the gate dielectric. The stack was formed with a thin interfacial layer of 1.0 nm SiO₂ followed by 3.5nm thick 20% SiO₂ - Hafnium Silicate layer with physical thickness of $t_{ox}=4.5$ nm (EOT = 2 +/- 0.03 nm). These devices were subjected to NH₃ Post Deposition Anneal (PDA) at 700 C for 60s, to improve the leakage performance. Physical characterization details of these structures can be found elsewhere [15].

n-MOSFETs with W/L = 10/0.25 were used for stress test, which were performed on fresh devices with uniform threshold voltages. CVS was applied with gate bias $V_g = 1, 1.5, 2$ and 3 V while CCS [16] with current densities of 2, 4, 10 and 20 A/cm² ($I_g = 50$ nA, 100nA, 250nA, 500nA) were applied at the gate using a semi-automated test measurement set up with HP4156 semiconductor parameter analyzer controlled by a LabVIEW program. Threshold voltage (V_t) and transconductance (g_m) were measured at regular stress intervals during 5 s, 10 s, 100 s, 400 s of stress. The substrate current was measured manually (within 1-2 minutes) using Fixed Amplitude Charge Pumping method (FACP) with amplitude of 1.0V. The de-trapping time was also found to be longer (~hrs) on similar MOS capacitor devices measured in the same die of the wafer [17]. The base voltage of the pulse applied at the gate was swept from 0 to 1.2 V, while the source and the drain were reverse biased by a small voltage of 50mV. Constant rise and fall times $t_r = t_f = 100$ ns, were maintained when a rectangular pulse of frequency $f=1$ MHz at the gate were applied during the measurement. The interface trap density was calculated from the charge pumping current (I_{cp}) measured before and after the stress [18] using the formula

$N_{it} = I_{cp} / qAf \text{ \#/cm}^2$, where q is the electronic charge, A is the area and f is the frequency of pulse applied.

From Figure 1.5, a positive shift in threshold voltage (ΔV_t) is observed as the stress time increases, suggesting that electron trapping is dominant in CVS (Figure 1.5a) and CCS (Figure 1.5b). The electron trapping rate increases as the slope of the threshold voltage shift (ΔV_t) also increases with the applied stress time [16]. Curve fit of the data was done using the equation [19] $\Delta V_t(N_{inj}) = \Delta V_{max} \times (1 - \exp(-\sigma_0 \times N_{inj}))^\beta$ where ΔV_{max} is proportional to total trap density ($qN/C = V_{max}$), σ_0 and β are model parameters [19]. A value of $1 \times 10^{12} \text{ \#/cm}^2$ was taken [19] based on experimentally calculated values, and σ_0 and β were fitted for the values of $1 \times 10^{-14} \text{ cm}^2$ and 0.37~0.45 respectively. As $N_{inj} < 1/\sigma_0$, it confirms that ΔV_t follows the power law.

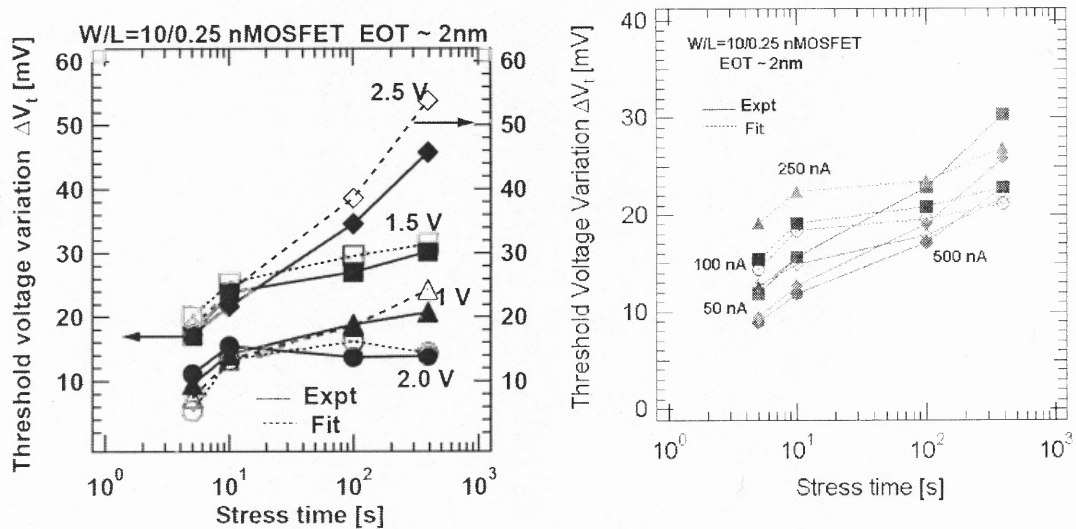


Figure 1.5 (a) Change in threshold voltage (ΔV_t) vs. Stress time during CVS. (b) Change in threshold voltage (ΔV_t) vs. Stress time during CCS. Thick lines are experimental data and dotted lines indicate model fit. Filled symbols indicate the data obtained from the experiment while the open symbols were obtained from the equation. source:[20]

During CVS and CCS, as the injected charge in the oxide increases, increased threshold voltage variation is observed as shown in Figure 1.6a of ΔV_t vs Q_{inj} plot. It is seen that the slope $\delta V_t / \delta Q_{inj}$ increases as the applied stress voltage (1.5, 2 and 2.5V) and stress current (Figure 1.6 b) increase. The slope variation is higher for 2.5V compared to that of 2 or 1.5V. Similar case is observed for CCS, where stress current of 10 A/cm² induces greater change compared to 2 A/cm². This suggests that electron trapping rate increases with the stress voltage and current levels.

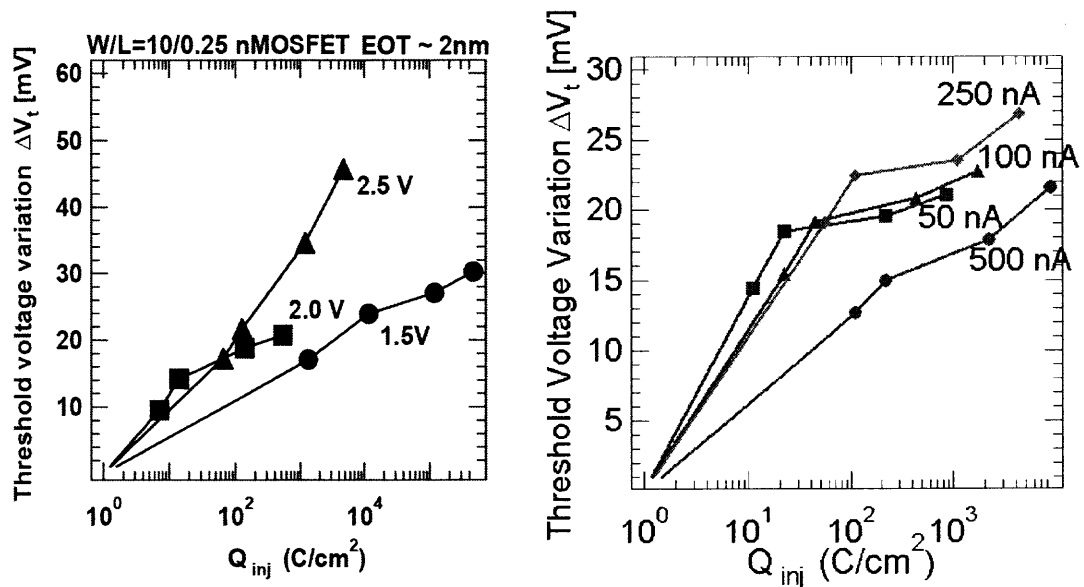


Figure 1.6 (a) Injected charge Q_{inj} Vs Change in threshold voltage (ΔV_t) for applied CVS. (b) Injected charge Q_{inj} Vs Change in threshold voltage (ΔV_t) for applied CCS. source:[20]

Gate current and gate voltage measured during CVS and CCS showed that neutral bulk trap generation might be ruled out as gate current shows negligible change during CVS. Moreover, significant electron trapping might have occurred near substrate as gate current shows slight decrease for high stress voltages, which possibly induced significant positive shift of ΔV_t (Figure 1.5). The transconductance (g_m) and sub threshold slope was

seen to degrade over the stress time, suggesting the possibility of interface trap generation.

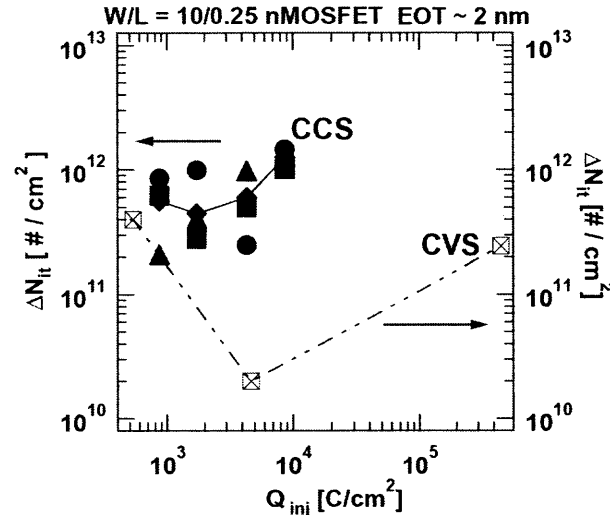


Figure 1.7 Change in interface trap density ΔN_{it} calculated using FACP during CCS (1^o Y-axis) and CVS (2^o-axis) before and after CVS. source:[20]

The charge pumping current, measured before and after CVS and CCS, is found to increase with stress voltage (not shown) and current. A shift in the base voltage level of the curve was observed for both the cases. A greater change in oxide trap densities (ΔQ_{ot}) near the IL/high- κ and substrate/IL interface (or bulk traps) than a smaller change in interface traps (ΔQ_{it}) was observed [21, 22]. An increase in I_{cp} after the applied stress also suggests a possible increase in interface traps.

Figure 1.7 shows the change in interface trap densities ΔN_{it} , calculated before and after the stress of 400 secs. A little increase in ΔN_{it} with Q_{inj} during CCS is noticed, suggesting insignificant interface trap generation. ΔN_{it} is almost constant during CVS, except for a decrease around 2V for $Q_{inj} \sim 4 \times 10^3$ C/cm², showing insignificant trap generation for the applied stress voltages. From the conductance measurements on capacitors with identical gate stack [22] the interface state generation is comparatively

insignificant even for higher CVS. Therefore, variation of positive ΔV_t for different stress levels is mostly due to electron trapping at bulk hafnium silicate, which also supports the earlier assertion.

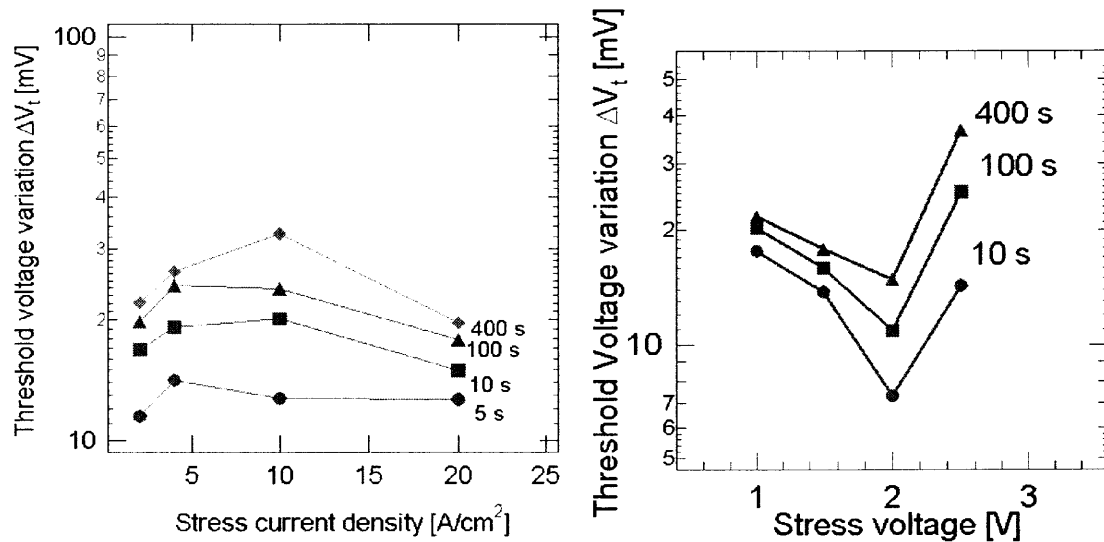


Figure 1.8 (a) Change in threshold voltage (ΔV_t) Vs stress current density for constant stress times during CCS. (b) Change in threshold voltage (ΔV_t) versus stress voltage for constant stress times during CVS. A turn-around effect is noticed at higher values in both cases. source:[20]

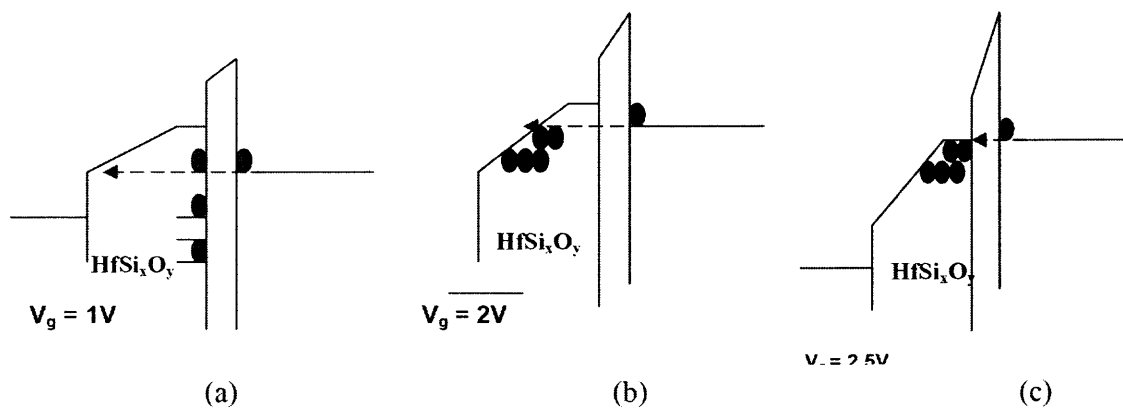


Figure 1.9 Band bending induces interface traps at $\text{HfSi}_x\text{O}_y/\text{SiO}_2$ interface to be filled. (b). Shallow traps towards $\text{TiN}/\text{HfSi}_x\text{O}_y$ interface are filled due to band alignment. (c). Shallow traps near $\text{HfSi}_x\text{O}_y/\text{SiO}_2$ interface are filled during stress. source:[20]

The threshold variation is also plotted with applied stress voltage and current densities as shown in Figure 1.8. At $V_g = 1V$, the electrons tunneling through the IL from the substrate, cannot fill shallow traps due to band alignment [23], but the high- κ /IL states at different energy levels [23] are filled (Figure 1.9a). This induces a change in V_t , as the charge centroid resides near the substrate. But at $V_g = 2V$, electrons fill shallow traps from the high- κ /IL interface (Figure 1.9b), which induces comparatively lower ΔV_t , as trapped charge centroid moves away from substrate. However, at $V_g = 2.5V$, electrons fill shallow traps near the high- κ /IL states (Figure 1.9c), and moves the charge centroid back to near high- κ /IL interface, which induces significant change in V_t . Such shift in charge centroid was earlier observed in silicon dioxide based devices at low temperatures [24].

At lower current stress ($I_g = 50$ nA), the gate voltage may induce charge trapping phenomenon as shown in Figure 1.9b. As the stress level is increased ($I_g = 100$ nA), the gate voltage increases and induces higher ΔV_t , which may be due to higher charge trapping near high- κ /IL interface (Figure 1.9c). But at stress levels of $I_g = 500$ nA, charge centroid moves towards the gate as trapped charge re-distribution [25] may occur during stress under high electric field, which induces low ΔV_t .

It is therefore concluded that electron trapping is observed from the positive shift of the threshold voltage (ΔV_t) during CVS and CCS. Curve fit of the data confirmed the power law dependence of stress-induced threshold voltage shift. Charge pumping measurements for both cases further supported significant electron trapping at bulk Hf-silicate while interface trap generation was comparatively insignificant. The turn-around effect, noticed for ΔV_t as the stress current density increases during CCS, shows

dependence of spatial distribution of charge trapping at shallow traps in bulk Hf-silicate film on band bending at different gate voltages. Redistribution of trapped charges during and after removal of stress may be additionally responsible for such turn-around effect.

1.1.3.2 Mobility in Hf-Based High- κ Dielectrics. One of the other major reliability challenge is the degraded channel mobility in these devices. Also, mobility properties of the dielectric affect low-frequency noise performance. While the study of interfacial layer (IL) dependence on mobility has been proven to be quite consistent, the high- κ thickness dependence is found to vary among the researchers. While the study at SEMATECH [26] and IMEC [27] showed a dependence of mobility on high- κ thickness, studies at STMicro [29] showed that it is independent of high- κ thickness. The role of soft optical phonons of the high- κ layer is also studied here by understanding the impact of mobility due to varying HfO₂ and interfacial thickness (IL) in highly optimized and aggressively scaled high- κ /metal gate devices, fabricated using conventional CMOS process flow. The temperature effects on mobility is also studied in detail. The temperature acceleration and mobility loss factor was estimated and correlated with the interfacial layer and HfO₂ thicknesses. Finally, the temperature sensitivity factor, a figure of merit was calculated so as to determine the predominant mechanism which limits the mobility in these high- κ /metal gate devices.

The samples used here were fabricated by IBM high-k process group at Yorktown Heights, USA. The mobilities were investigated in n-MOSFETs (doping concentration $N_{\text{sub}} \sim 1 \times 10^{17} \text{ cm}^{-3}$) with gate width $W=20\mu\text{m}$ and length $L=10\mu\text{m}$, with HfO₂ thicknesses ranging from 1.5 nm to 3.0nm [28], while the interfacial layer thickness was 0.8nm. Two different IL thicknesses – 0.8 nm and 1.5 nm SiO₂ on top of which a 2.5nm

deposited HfO₂ was also used for this study. EOT of the studied devices ranged from ~0.9 nm for the lowest HfO₂ thickness (1.5nm) and ~1.4 nm for the highest HfO₂ thickness (3.0nm). Also used in this study are i) a 0.8nm/2.5nm IL/Hf device where the Hf-content is found to be ~20% and b) SiO₂ control device. Deposition of the high- κ oxides was achieved by Metal Organic Chemical Vapor Deposition (MOCVD). Physical Vapor Deposited (PVD) TiN was employed as metal gate, while poly-Si acts as a capping layer.

Inversion split C-V was used to measure the electron mobility for the range of temperatures from 233K to 473K. A TP03000 setup was used for this purpose. The inversion C-V's were found to be independent of frequency and 100 KHz was chosen for this study. The charge trapping in these devices were negligible (hysteresis < 12 mV) then DC I_D-V_G method were used. All the devices showed the interface state density D_{it} to be $\leq 5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$, which allowed an error-free mobility extraction of these devices. The pad and series resistance effects in the devices were minimal to be ignored. However, the gate leakage current density was found to be higher in thinner devices (1.5nm and 1.7nm HfO₂) and hence appropriate corrections were made during the extraction of mobility using the standard gate current partition model.

Figure 1.10 shows the mobility curves measured by the split-CV technique and are compared for various HfO₂ thickness values from 1.5 to 3 nm. All samples had a constant IL thickness of nominally 0.8 nm. As can be seen, the mobility is found to be essentially independent of the HfO₂ thickness, as most of the small mobility variations can be shown to be caused by measurement limitations due to charge trapping in thicker layers and gate leakage through thinner HfO₂ layers at high fields.

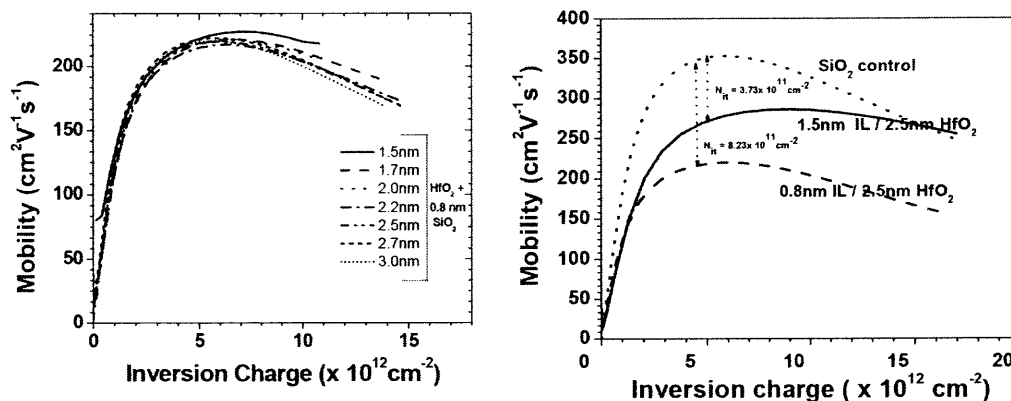


Figure 1.10 (a) Mobility Vs Inversion Charge for different HfO_2 thickness studied for $10 \times 10 \mu\text{m}^2$ TiN/ HfO_2 /n-MOSFETs. (b) Mobility Vs Inversion Charge for different interfacial thickness studied for $10 \times 10 \mu\text{m}^2$ TiN/ HfO_2 /n-MOSFETs. source:[28]

This thickness independence is in contrast to the known, strong IL thickness dependence of the mobility, which is also observed in the high mobility samples, as illustrated with Figure 1.10 (b). The strong mobility increase with increasing IL thickness has been explained by the screening of HfO_2 related charges [29] or by the screening of the soft-optical HfO_2 phonons [30,31] – Remote Charge Scattering (RCS) and Remote Phonon Scattering (RPS). As seen in Figure 1.10 (b), the required interface charges for the different interfacial layered devices were found to be very low ($< 10^{11} \text{cm}^{-2}$), which points out towards remote phonon activity as the cause.

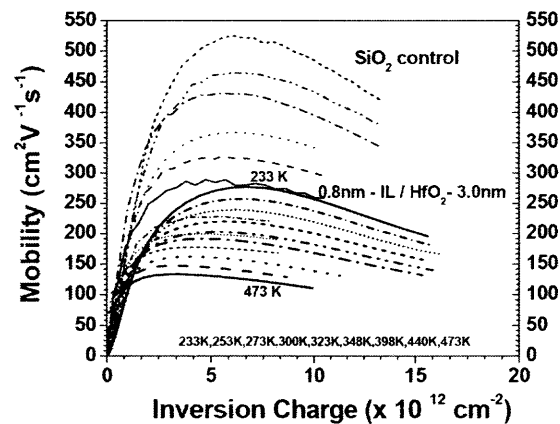


Figure 1.11 Mobility Vs Inversion Charge at different temperatures for 0.8nm IL/3.0 nm HfO₂ 10 x 10 μm² TiN/HfO₂/n-MOSFETs. SiO₂ control device is plotted as a reference in all these cases. source:[28]

To investigate it further, the temperature dependence of the mobility was measured and a comparison with SiO₂ was made. Typical T-dependent mobility data (0.8nm IL/3.0 nm HfO₂ split) is shown in Figure 1.11, and compared to mobility data for SiO₂. As expected, the mobility increases with decreasing temperature, however, the peak mobility (μ_{peak}) of the HfO₂ is found to be lower than the control device (SiO₂) for any given temperature. The mobility curves are almost parallel to each other even at higher inversion charges for HfO₂ devices, indicating negligible effect of surface roughness (μ_{SR}) component.

The measured temperature dependence on the mobility is summarized in Figures 1.12 and 1.13. In Figure 1.13, the T-dependence of the mobility at an inversion charge density of $N_{\text{inv}} = 1 \times 10^{13} \text{ cm}^{-2}$ for two different IL thicknesses is compared to the theoretical result for zero IL thickness [30] and to the control device. As can be seen, the temperature dependence can be described by a power law, $\mu \sim T^{\alpha}$, and the exponent systematically varies from $\alpha = -0.87$ (IL = 0 nm, theory) to $\alpha = -1.5$ (IL = ∞, SiO₂) with

increasing SiO₂ (IL) thickness. In contrast, α is found to be independent of the HfO₂ thickness, as summarized in Figure 1.12.

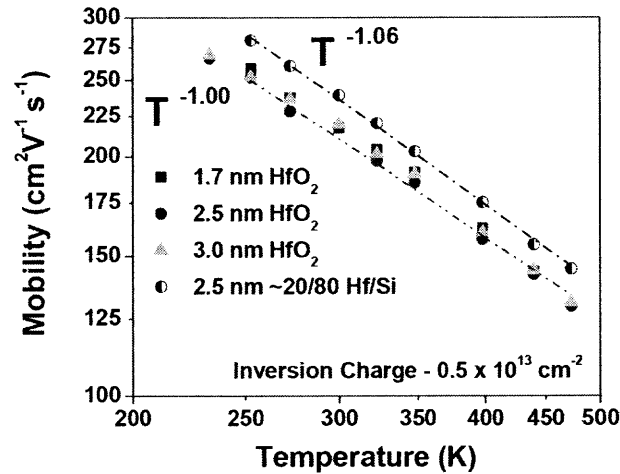


Figure 1.12 Temperature acceleration factor – Mobility Vs Temperature for (a) different HfO₂ thickness studied for $10 \times 10 \mu\text{m}^2$ TiN/HfO₂/n-MOSFETs. A 20/80 – Hf/Si is also used for comparison purpose. source:[28]

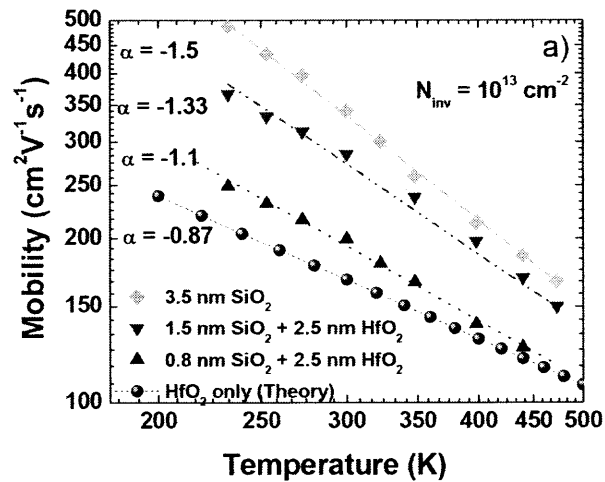


Figure 1.13 Temperature acceleration factor – Mobility Vs Temperature for different IL thickness studied for $10 \times 10 \mu\text{m}^2$ TiN/HfO₂/n-MOSFETs. A 20/80 – Hf/Si is also used for comparison purpose. source:[28]

The silicate data only shows a slight enhancement of α , not unexpected for low Si content ($\sim 20\%$). Comparing the data sets for 2.5 nm HfO_2 from Figures 1.12 and 1.13 also shows that α depends weakly on N_{inv} , except at low $N_{\text{inv}} < 1 \times 10^{12} \text{ cm}^{-2}$ where ionized impurity scattering dominates and the mobility actually increases with increasing temperature.

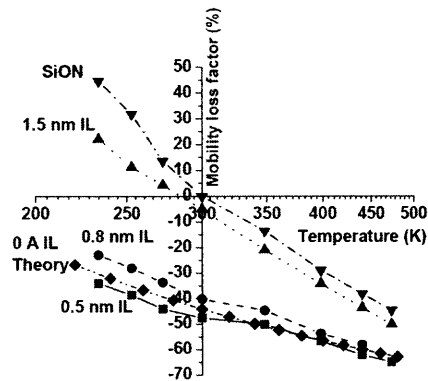


Figure 1.14 Mobility loss factor Vs Temperature for different interfacial layer thickness studied for $\text{TiN}/\text{HfO}_2/\text{n-MOSFETs}$. source:[28]

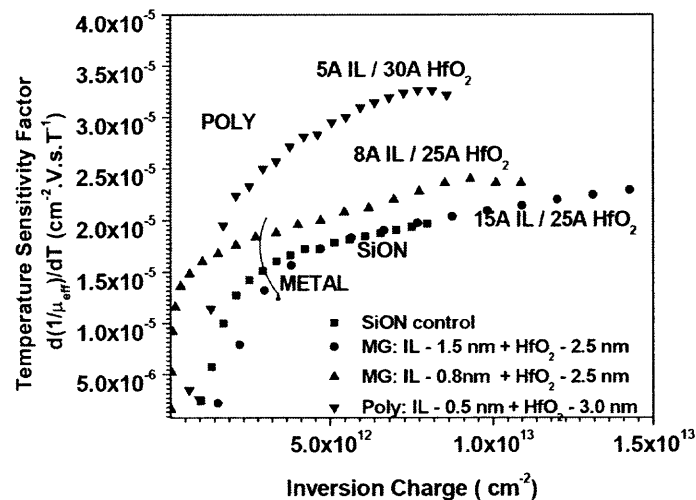


Figure 1.15 Temperature sensitivity factor Vs Inversion charge for different interfacial layer thickness studied for $\text{TiN}/\text{HfO}_2/\text{n-MOSFETs}$. source:[28]

The mobility loss factor for SiO₂ and HfO₂ devices for all measured temperatures was estimated using the reference SiO₂ value at room temperature using the formula

$$\left(\frac{\mu_{\text{SiO}_2(\text{or})\text{HfO}_2, \text{XK}} - \mu_{\text{SiO}_2, 300\text{K}}}{\mu_{\text{SiO}_2, 300\text{K}}} \right) \times 100 \% \quad (1.2)$$

where $200 < X < 500$ K. As seen in Figure 1.14, heavy mobility loss for thinner IL devices (~ 0.5 nm IL) occurs when compared to SiON devices at lower temperatures. However, the loss factor reduces as the temperature increases and the values of thinner IL devices are comparable to typical SiON devices at 473 K.

To emphasize the dominance of phonon scattering mechanism due to high- κ , the temperature sensitivity factor $d(1/\mu)/dT$ [25][32][33], is also studied here as a figure of merit, where

$$\frac{d(1/\mu)}{dT} = 1.75xT^{0.75} - \frac{y}{T^2} + z\alpha T^{\alpha-1} \quad (1.3)$$

where x,y,z are coefficients independent of temperature. The first term corresponds to impact of acoustical phonons (μ_{ph}), while the second and third terms show the effect of coulomb scattering (μ_{c}) and additional high- κ phonon scattering ($\mu_{\text{ph-HK}}$) respectively. Figure 1.15 shows the plot of the temperature sensitivity factor for different IL thickness. The temperature sensitivity is clearly enhanced for the devices with the thinner IL of 0.8nm. The results are consistent with the prediction that the electron mobility in nMOSFETs with HfO₂ containing gate stacks will be reduced due to soft-optical phonon scattering and the observed thickness dependence in Figure 1.10 suggests that the high

mobility stacks measured here yield mobility values close to the theoretically predicted limit. Evidently, with continued EOT scaling, a substantial performance penalty has to be accepted. However, it is believed that this will not prevent the use of HfO₂/metal gate stacks in future CMOS technologies, as the room and high temperature mobility values reported for long channel nMOSFETs with aggressively scaled SiON gate dielectrics are surprisingly similar [34] to the values reported here for nMOSFETs with high- κ stacks. This happens because the mobility reduction due to soft-optical phonons can be traded off for the mobility reduction due to the high nitrogen content in advanced SiON gate stacks.

In summary, the dependence of high- κ and interfacial layer thickness and its effects at different temperatures on mobility was studied in aggressively scaled, process-optimized high- κ /metal gate devices. While a strong dependence due to interfacial layer is observed, the HfO₂ layer does not influence mobility. For any given HfO₂ thickness, the mobility increases with decrease in temperature at higher inversion charges ($10^{12} \sim 10^{13} \text{ cm}^{-2}$). The temperature acceleration factor ($\mu \sim \mu_0 T^a$) was found to be dependent on interfacial layer thickness than HfO₂ thickness. The mobility loss factor was found to be lower in HfO₂ devices at higher temperatures. The temperature sensitivity factor, as a figure of merit, shows the role of high- κ soft optical phonons which reduces the mobility in nMOSFETs with HfO₂ containing gate stacks.

1.2 Motivation and Objective

The objective of this dissertation is to characterize and model the low-frequency noise in Hf-based high- κ dielectrics for sub-45 nm node analog and mixed signal applications. It

is, therefore, imperative that such devices are characterized to a great extent in order to understand various electrical parameters. State-of-the-art transistors fabricated by IMEC high- κ process group at Belgium were used to characterize the low-frequency ($1/f$) noise and various gate stack processing and technological parameters that influence the low-frequency noise in Hf-based devices were identified. The temperature dependencies were also studied using the measurement setup at IMEC, Belgium and ENSICAEN, France. The differences observed with the conventional oxides are explained. The limitations of present modeling approaches are underlined and a possible model is formulated.

1.3 Dissertation Organization

Chapter 2 gives an overview of noise and noise sources in MOS devices. The major types of noise, noise sources and their background are discussed followed by a review of low-frequency noise, which is the topic of this research. The low-frequency noise parameters are then introduced which help in the understanding process of $1/f$ noise performance in various high- κ devices. The noise origin and noise mechanisms are also underlined.

Chapter 3 discusses the recent understanding of low-frequency noise performance in high- κ dielectric based semiconductor MOSFET devices. A literature study of low-frequency noise in high- κ noise by other researchers is performed followed by understanding the interfacial layer thickness effects on $1/f$ noise. The temperature dependence of low-frequency noise is outlined briefly and an overview of $1/f$ noise performance in other high- κ dielectrics other than Hf-based devices is also discussed.

Chapter 4 considers the technological and the experimental aspects of this dissertation. The room and high temperature noise characterization setup is discussed first

followed by low temperature noise measurement setup. The high- κ gate dielectric deposition technique is outlined followed by introduction to various gate electrode deposition techniques that are relevant to this study. The various interfacial layer options are also studied and explained. Finally, the extraction of basic parameters which are required for estimation of certain parameters using low-frequency noise is discussed.

Chapter 5 describes the gate stack parameters and their influence on $1/f$ noise. The influence of thickness and the quality of the interfacial layer on $1/f$ noise is discussed first followed by the interfacial nitridation effects on $1/f$ noise. Comparison is made between non-nitrided and nitrided interface anneals on $1/f$ noise in n- and p-MOSFETs and its relationship with nitrogen induced oxygen-defect centers. The influence of gate electrodes viz. poly-Si/Metal/FUSI on low-frequency noise is then discussed followed by the effect of gate electrode processing effects on $1/f$ noise. This is followed by noise mechanism study in the literature for Hf-based MOSFETs either with poly-Si gate electrodes or metal gate electrodes. The effect of high- κ layer thickness, the k -value and the deposition technique on $1/f$ noise is understood. The impact of gate/high- κ interface and its relationship with Fermi-level pinning are then studied. The effect of substrate is outlined by using Si and GeOI for $1/f$ noise. It also describes the low temperature and high temperature dependence of low-frequency noise in Hf-based high- κ devices. The effect of high temperature is studied by comparing SiON, HfO₂ and Hf-silicate based devices followed by the impact of low temperature in SiON and Hf-silicate n- and p-MOSFETs. The anomalous noise behavior under such temperatures is analyzed.

Chapter 6 discusses the modeling aspects of noise in high- κ based devices. The implementation of current limits due to scaling is outlined followed by some basic

calculations used in estimating the tunneling parameter. The ideas for drain current modeling are also discussed.

Chapter 7 summarizes this dissertation drawn from the already completed work and provides the outline for future work.

CHAPTER 2

OVERVIEW OF NOISE

This chapter introduces the concept of noise, different types of noise and various noise sources in a MOSFET. Although, noise is a universal phenomenon, the scope of this dissertation is limited to noise in semiconductor devices, more specifically in MOSFETs. This chapter provides an overview and background information on noise sources and its possible origin in a MOSFET.

2.1 Noise and Noise Sources

Four important kinds of noise sources in MOSFETs are thermal noise, shot noise, generation-recombination (G-R) noise and low-frequency ($1/f$) noise. The illustration in Figure 2.1 shows the possible G-R and $1/f$ noise sources and its possible origin in a MOSFET.

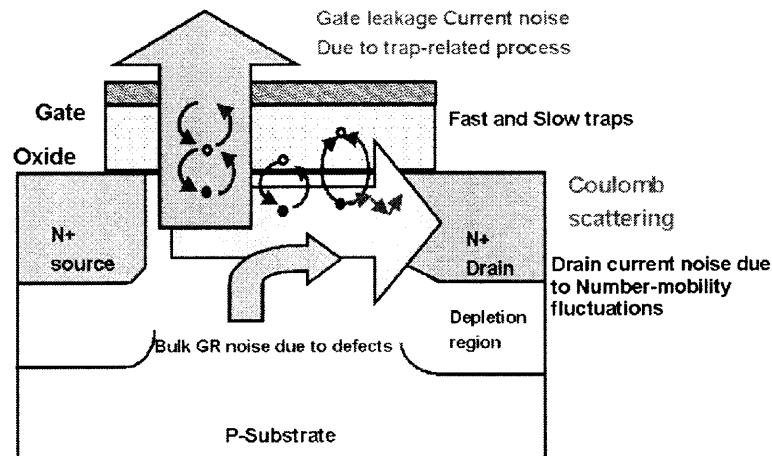


Figure 2.1 Noise sources in a MOSFET.

From the figure, it is inferred that G-R noise is caused mainly due to the defects present in the substrate. There are two kinds of 1/f noise in the MOSFET – i) Noise due to the current flowing from source to drain called as Drain Current Noise and ii) Noise due to the leakage current flowing through the gate called as Gate Leakage Current Noise. While the possible origin for drain current noise may be due to the carriers in the channel and scattering effects, the gate current noise is more due to trap related processes. This dissertation focuses on drain current noise and its possible origin in MOSFETs.

2.1.1. Thermal Noise

Thermal Noise, Nyquist noise or Johnson noise of MOSFETs is due to the random thermal motion of the charge carriers in the channel. Thermal noise dominates at high frequencies and is associated with the diffusive Brownian motion of the free carriers, driven by the thermal energy $\frac{3kT}{2}$, in a three-dimensional (3D) structure. From the drift or diffusion transport mechanisms, the thermal noise can be obtained. The double-sided power spectral density of thermal noise S_{TH} is [35] given by:

$$S_{TH} = \frac{2 R h \nu}{e^{h\nu/kT} - 1} \quad (2.1)$$

where ν is the frequency.

For $\nu \ll \frac{kT}{h}$, this simplifies to

$$S_{TH} = 2 R kT \quad (2.2)$$

For single sided spectra, this value multiplies by a factor 2. The MOSFET thermal noise expression for the drain current I_D which is widely used is

$$S_{ID} = \gamma 4 kT g_{channel} \quad (2.3)$$

where S_{ID} is the drain current noise spectral density, k is the Boltzmann's constant, T is the absolute temperature, g_{channel} is the channel conductance with zero drain-to-source voltage, with $2/3 < \gamma < 1$ in the linear region and $\gamma = 2/3$ in the saturation region for long channel device. Thermal noise is called as white noise at low frequencies, because its power spectral density is flat upto extremely high frequencies of over 10^{12} Hz.

Considering for a linear regime where $\gamma = 1$, this leads to

Drain Current Noise Spectral Density

$$S_{ID} = \frac{4 kT I_D}{V_{DS}} \quad (2.4)$$

and

Input-referred Gate Voltage Noise Spectral Density

$$S_{VG} = \frac{4 kT I_D}{g_m^2 V_{DS}} \quad (2.5)$$

$$S_{VG} = \frac{4 kT L^2 I_D}{\mu^2 C_{ox}^2 W^2 V_{DS}^2} \quad (2.6a)$$

$$= \frac{4 kT L V_T}{C_{ox} W V_{DS}^2} \quad (2.6b)$$

In saturation, the value becomes,

$$S_{VG} = 4kT \frac{\gamma}{2} \frac{L}{W \mu C_{ox} V_T} \quad (2.7)$$

The above equation is derived for g_{channel} approximated to I_D/V_{DS} in linear regime and I_D/V_T in saturation.

It can be seen from figure 2.2 that gate-referred thermal noise in a MOSFET is proportional to the absolute temperature T , lateral dimensions L, W and inversely proportional to C_{ox} .

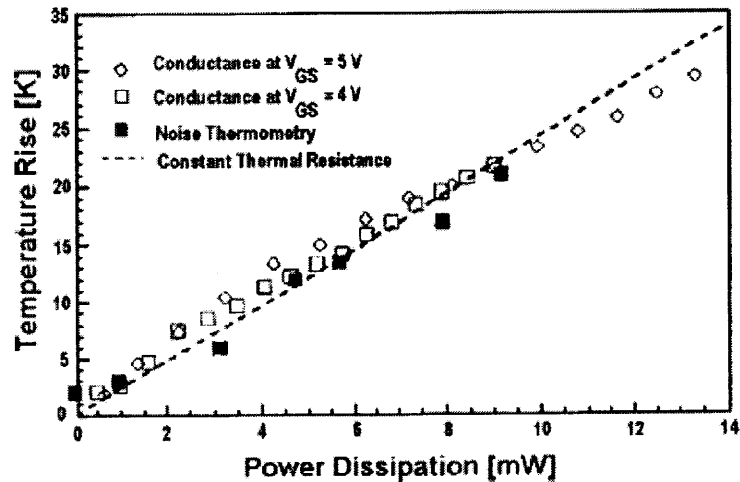


Figure 2.2 Extracted parameters from small signal conductance measurements at different bias points, plotted as local device temperature rise vs. power dissipation. source [36].

The thermal noise can be used for thermometry purposes, provided that the resistance R is accurately known. For the usual low-power dissipation case, the device or lattice temperature equals the ambient temperature T , so that the thermal noise can be used for internal calibration. When there is significant self-heating, caused by Joule heating in the device, the local temperature becomes significantly higher than T . Self-heating problems are particularly pronounced for silicon-on-insulator SOI MOSFETs. The assessment of self-heating is anticipated to become increasingly important for future scaled complementary metal-oxide semiconductors CMOS, so that noise thermometry may receive increasing interest.

In addition to thermal noise due to the channel, there exist two other additional noise sources in MOS devices. They are the thermal noise due to the gate poly resistance and bulk resistance.

2.1.2. Shot Noise

Shot noise is generated when charge carriers encounter a potential barrier (like in a p-n junction or a Schottky contact) independently in a random fashion. These discrete charge carriers carry electric current and random changes in their number result in fluctuations of the electric current. The power spectral density for the gate leakage current I_G in ultrathin oxide MOSFETs is given by

$$S_{I_G} = F 2 q I_G \quad (2.8)$$

where F is the Fano factor, a constant.

Theoretically, there is a non-fundamental extrinsic source of shot noise, which is associated with the midgap level-related SRH (Shockley-Read-Hall) GR (Generation-Recombination) mechanism in the depletion region of a junction. The SRH GR mechanism is mainly responsible for the recombination or generation of non-equilibrium carriers, defining the recombination or generation lifetime and the non-ideal drift current components. It is to be noted that the fundamental source of shot noise which is under discussion is purely intrinsic in nature.

The noise observed in floating-body operated SOI MOSFETs for a reverse biased drain-body junction is a good example [37] for shot noise. It is also seen that the shot noise spectral density S_{I_G} is independent of frequency.

Both thermal noise and shot noise are white noise and are classified under intrinsic noise sources. The name white noise is because all different frequency components are present with the same signal strength.

2.1.3. Generation Recombination Noise

Generation-Recombination noise is due to fluctuations in the number N of electrons in conduction band and holes in valence band. In its most simple form, the current through a device switches randomly between two discrete states, as represented in figure 2.3. These fluctuations in the number of free carriers are caused by trapping-detrapping of carriers of either bulk or surface defect centers.

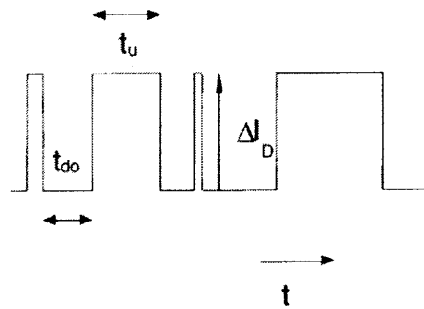


Figure 2.3 Definition of the RTS parameters in the time domain.

A single trapping-detrapping event leads to a Random Telegraph Signal [38] (RTS). The power spectral density of an RTS is a Lorentzian and is given by

$$S_{ID}(f) = \frac{4(\Delta I)^2 \tau^2}{(\tau_c + \tau_e)[1 + (2\pi f \tau)^2]} \quad (2.9)$$

Where ΔI is the switching current amplitude and the characteristic time constant τ is determined by the average up τ_u and down τ_{do} time constants respectively given by

$$\frac{1}{\tau} = \frac{1}{\tau_c} + \frac{1}{\tau_e} \quad (2.10)$$

The average up and down time constants can be identified with an average capture (τ_c) and emission time constant (τ_e). It has been found that the up and down times of an RTS usually follow a Poisson distribution.

The characteristic frequency f_c defined in Figure 2.4 can be most easily derived by plotting the function $f \times S_I$, which yields a maximum at $f = f_c$. This forms the basis of GR noise spectroscopy.

For larger MOSFETs containing many defects the analysis can be generalized. If there exists an ensemble of the defect centers of same energy level, a Lorentzian noise spectrum can be obtained, which is given by

$$S_{ID} = \frac{C_0 I^2 \tau}{1 + (\omega \tau)^2} \quad (2.11)$$

In Equation 2.11, τ is the characteristic time of the GR center, and C_0 is a constant proportional to the trap concentration. The transitions to and from the nearest band is considered for deeper lying defects. In this case, the characteristic time is again defined by the capture and emission time. An Arrhenius plot can be constructed using the sensitive nature of τ with temperature T . This is very similar deep-level transient spectroscopy DLTS, where the noise frequency f_w takes over the role of the emission rate window. The main difference between the two techniques is that the noise spectroscopy is based on a steady state between random emission and subsequent capture for a trap level where DLTS follows the transient emission of trapped charges with time, after a filling pulse.

The main advantage of using a noise-based technique is that it can be applied even to very small area devices, which is not possible for the standard capacitance based

DLTS. However, recent developments in constant-resistance DLTS on deep sub micrometer MOSFETs have demonstrated its feasibility for the analysis of deep levels.

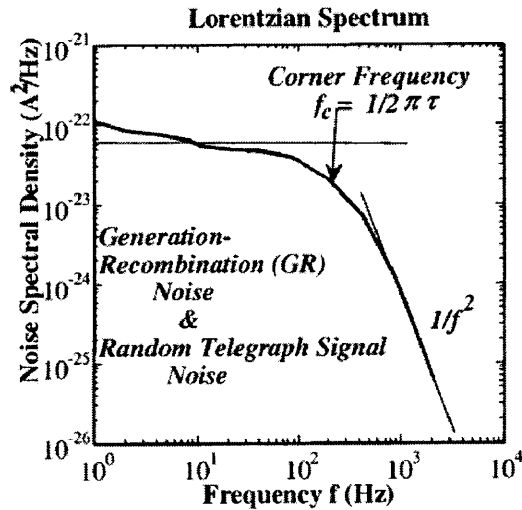


Figure 2.4 Illustration of a Lorentzian spectrum corresponding to a G-R noise.

RTS can also be used as an analytical tool where it can be used to probe the quantum effects dealing with the detection of inversion-layer quantization effects, in scaled MOSFETs.

2.1.4 Flicker or 1/f Noise

Flicker noise is found in all active devices as well as passive elements. It owes its name to its spectral density as it is approximately proportional to inverse of low frequency as

$$S_{ID}(f) = K * F (1/f^\gamma) \quad (2.12)$$

where γ is the frequency exponent whose value lies in the interval between 0.7 and 1.3. Both Generation-Recombination and flicker noise are classified as extrinsic noise sources. Additional description on this topic is given in section 2.2.

In addition to the above mentioned noise sources, there is another type of low-frequency noise found in integrated circuits and discrete transistors called ‘burst noise’. The origin of this noise has been shown to be related to the presence of heavy-metal ion contamination in the devices. Another form of noise, produced by zener or avalanche breakdown in p-n junctions, is called ‘avalanche noise’. This noise is caused by the cumulative process when high energy electron-hole pairs created in the depletion region of a reverse biased p-n junction collide with silicon atoms, generating large random noise spikes.

2.2 Low Frequency Noise

Low frequency noise (LF) noise may be examined both in frequency domain and in time domain. These two are fundamentally related and give insights to noise behavior. This section discusses briefly the low-frequency noise in both the domains and their relationship. Some of the data shown here are from the preliminary results of low-frequency measurements made at IMEC, Belgium using the setup described in Chapter 4. These data are mainly used to explain the concept of flicker noise, which is one of the fundamental extrinsic noise sources in MOSFETs.

2.2.1 LF Noise in Frequency Domain

Low-frequency noise is characterized by a plot of power spectral density (PSD) with the measured frequency f . An example of a typical plot is shown in figure 2.5. The power spectral density gives the noise power per unit of bandwidth as a function of frequency, with the units of W/Hz . Often, noise voltage or noise current is measured rather than

noise power and hence it is simply expressed as A^2/Hz or V^2/Hz . Sometimes decibels are used leading to dBV^2/Hz or dBA^2/Hz . In a semiconductor MOSFET, noise current or voltage is generally characterized either at the drain terminal or gate terminal, keeping the substrate and the source terminals at a minimum potential. Accordingly, they are defined as drain current (voltage) power spectral density and gate current (voltage) power spectral density. The power spectrum of such a noise signal is mathematically defined by Wiener-Khintchine theorem as the Fourier transform of the autocorrelation sequence of the random noise signal. An equivalent definition of PSD is the squared modulus of the Fourier transform of the time series, scaled by a proper constant term.

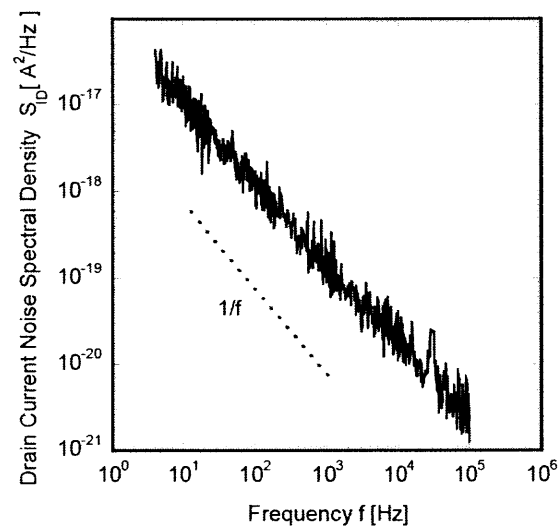


Figure 2.5 A typical noise power spectrum.

Sometimes a more complex spectrum with the frequency exponent varying between 0 and 2 is observed. This type of spectrum is considered to consist of so-called “Lorentzian spectra”.

The low frequency noise in n-MOSFETs can be under either steady-state or under periodic large-signal excitation.

2.2.2 LF Noise in Time Domain

In the time domain, the general way to characterize a noise signal is by autocorrelation function or more specifically stationarized autocorrelation function. The noise of the transistor at a particular period is important and hence averaging the statistical parameters over the whole period is not appropriate. In such cases, a bias transient will be defined and called as time dependent noise.

The scope of the present dissertation is limited to study the low-frequency noise only in the frequency domain under steady-state condition in semiconductor devices which are considered for future CMOS technologies.

2.3 Low-Frequency Noise Parameters

There are other noise parameters used to define the noise characteristics in FET-based devices. Some of the parameters that are used in this work are explained with an example and a possible definition is outlined here.

2.3.1 Drain Current Spectral Density S_{ID} (A^2/Hz) / Normalised S_{ID} (1/Hz)

As explained earlier in 2.2.1, drain current spectral density S_{ID} gives the power spectral density of the drain current I_D and is plotted for frequency f or measured drain current I_D . Sometimes the drain current noise spectral density values are normalized with the square of the drain current as S_{ID}/I_D^2 and plotted along with the measured drain current I_D or gate voltage overdrive $V_G - V_T$. A typical plot of normalized S_{ID} with drain current for an observed noise mechanism is shown in figure 2.6.

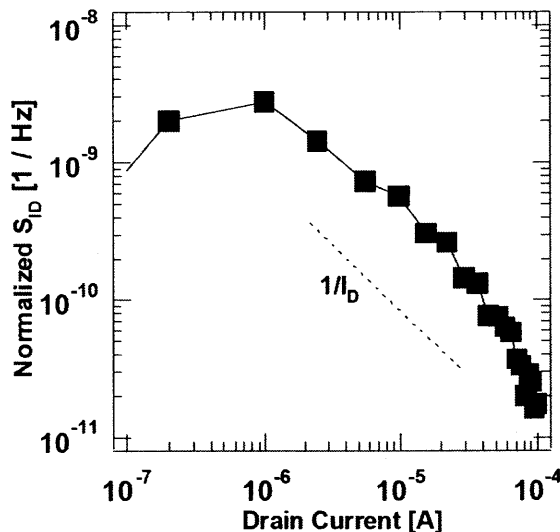


Figure 2.6 Normalized drain current spectral density S_{ID}/I_D^2 [1/Hz] Vs Drain Current I_D [A] for a typical n-MOSFET.

The basic idea of plotting S_{ID} with frequency f is to understand whether low-frequency noise ($1/f$) or a G-R noise ($1/f^2$) is present. Strictly speaking, S_{ID} is never equal to $1/f^1$ for a low-frequency noise case, but a value near 1. This value termed as frequency exponent γ and represented as $1/f^\gamma$, is a very important factor as it can explain the nature of traps and gives an idea about energy level distribution profile across the Si-band-gap. For a trap distribution that is skewed toward the interface [39], there are a greater number of high-frequency traps leading to $\gamma < 1$. Similarly for a trap distribution that is skewed away from the interface, there are a greater number of low-frequency traps leading to $\gamma > 1$. Figure 2.7 shows an example of frequency exponent variation with the applied gate voltage V_{GS} .

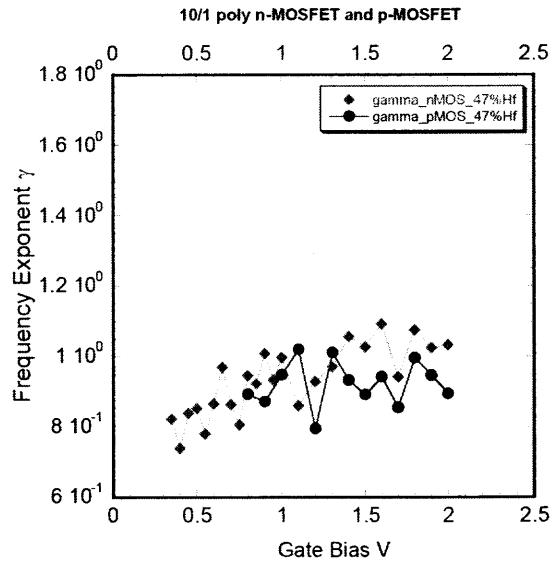


Figure 2.7 Frequency Exponent γ variation with applied gate bias.

The plot of S_{ID} or normalized S_{ID} with drain current I_D is equally important as this provides the indication of noise mechanism. Yet another characteristic study, which is equally applicable, is the plot of normalized noise with the gate voltage overdrive $V_{GS} - V_T$. Both these plots either identify or confirm the noise behavior in the studied devices. The various noise mechanisms and the method of identification on the noise behavior along with device parameter $(g_M/I_D)^2$ are discussed in detail in the next section.

Some authors also plot noise voltage spectral densities S_{VD} [40, 41] instead of S_{ID} and in either case, the plots yield identical information. Only noise current spectral densities are used, in all the devices.

2.3.2 Input referred noise S_{VG} (V^2/Hz)/ Normalized S_{VG}

On a broader approach, this parameter is very significant while analyzing the performance of systems at a circuit level. The output-referred noise does not allow a fair

comparison of circuits as the noise gets multiplied [42] by the gain of the output state of the amplifier. The idea is to represent the effect of all the noise sources in the circuit and this is illustrated in the figure 2.8.

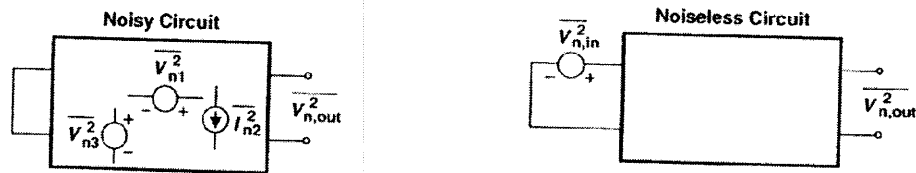


Figure 2.8 Determination of input-referred noise voltage at circuit level. source:[42]

When this parameter is studied at device level, the input-referred noise is simply referred as S_{II}/g_M^2 , where g_M represents transconductance of the device. When S_{VG} is normalized to the transistor area and frequency, this would be represented as $S_{VG} @ 1 \mu\text{m}^2 @ 1 \text{Hz}$, which is the figure of merit followed by ITRS committee [7]. The dependence of input-referred noise on gate voltage overdrive is again important as it may yield valuable information on the noise mechanism of the device. It also gives an indication of second order effects such as quantization of the conduction band energy levels near the substrate/dielectric interface, possible correlation of drain current noise with the gate current noise and also identifies where series resistance [43] is present in the device or not. A typical S_{VG} plot showing the dependence on gate voltage overdrive is shown in figure 2.9.

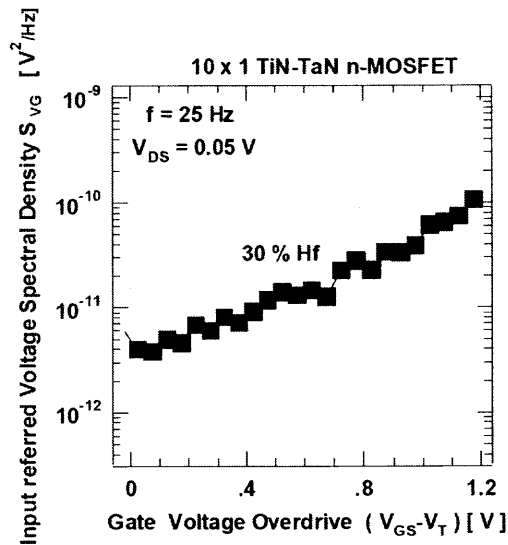


Figure 2.9 A typical input referred noise plot for a given noise mechanism.

Together with the information obtained from normalized noise, this can almost identify most of the important aspects of the device with respect to noise.

Following these two important noise parameters, one can estimate the other parameters, depending on the noise mechanism in the device. In general, if the device noise has a dependence on number fluctuation theory [44], then the volume and surface trap densities extracted from input-referred noise assume significance, while mobility scattering coefficient (α_{sc}) and Hooge's parameter (α_H) [45, 46] needs to be studied if the device noise has the dependence on mobility theory. These parameters are discussed in the next chapter which focuses on major $1/f$ noise mechanisms and its physical origin in MOSFET devices followed by the noise mechanism study in Hf-based dielectrics.

2.4 1/f Noise Mechanisms in MOSFETs

The drain current I_D in a MOSFET is proportional to the product of the mobility μ and the density (or number) of charge carriers N . The low-frequency fluctuations in the charge transport are caused by stochastic changes that can be independent (uncorrelated) or dependent (correlated) of these parameters. The product of $\mu \times N$ is monitored (which is the I_D), which does not allow the separation of mobility from number of carriers and therefore the identification of the dominant 1/f noise source becomes difficult and obscure. This duality also explains the two schools of thought which have emerged since the fifties. In many cases, theories have been discussed for a MOSFET in linear operation, though from a practical viewpoint, the saturation region is also relevant.

The physical origin of 1/f noise of drain current is explained by two major models - the number fluctuation model (ΔN) and mobility fluctuation model ($\Delta\mu$). The number fluctuation model attributes 1/f noise to random trapping and detrapping process of charge carriers in the oxide traps near the Si-SiO₂ interface. This is discussed first followed by mobility fluctuation model which attributes that 1/f noise is due to phonon-assisted lattice scattering in the channel. A unified model is also proposed in the literature which explains that 1/f noise is due to both random trapping and lattice-phonon scattering in the channel.

2.4.1 Number Fluctuation Theory - ΔN Model

The number fluctuation theory on 1/f noise was first proposed by A.L. McWhorter [44] in 1960's while working on the germanium based vacuum tube devices at MIT. The McWhorter model assumes that the origin of the fluctuations is the tunneling

of charge carriers at the semiconductor surface to and from traps which are located in the oxide close to the interface [47, 48]. As indicated in Equation (2.13), the noise power spectral density S_N due to number fluctuations is given by

$$S_N(f) = 4 \int_0^{x_1} dx N_{or}(E) f_T (1 - f_T) \Delta E \Delta y \Delta z \frac{\tau_t}{1 + (2\pi f \tau_t)^2} \quad (2.13)$$

where $N_{or}(E)$ - Oxide trap Density across the energy band gap cm^{-3}eV

$f_T(1 - f_T)$ - quasi peaked Fermi Energy function in eV

ΔE - Elemental change in energy in eV

τ_t - Total tunneling time constant in μs

f - frequency in Hz

$\Delta y, \Delta z$ - Elemental change in dimension of the device in μm

in which it is assumed that the free carriers tunnel to the traps at equal energy E and with a tunneling time constant τ_t , which varies with distance x from the interface.

$$\tau_t = \tau_0 e^{(\alpha_t x)} \quad (2.14)$$

The tunneling parameter α_t is of the order of 10^8 cm^{-1} and the attempt time τ_0 is approximately 10^{-10} s for the Si/SiO₂ interface.

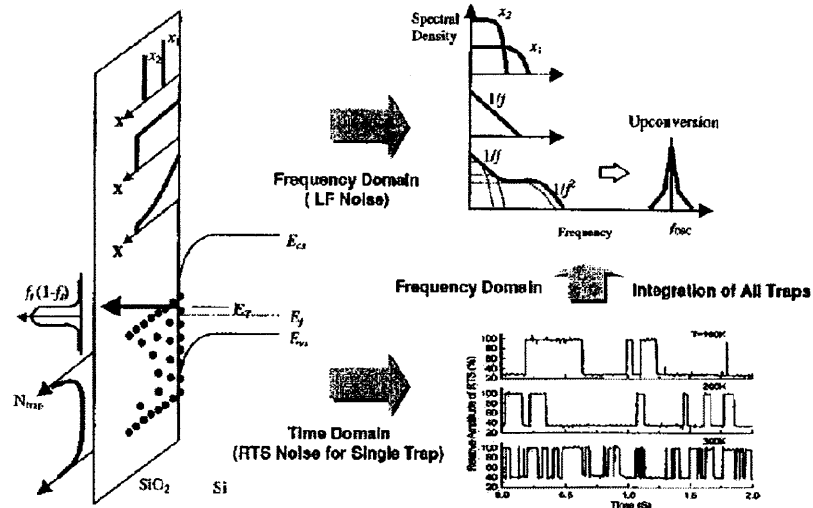


Figure 2.11 Noise spectrum and trap distribution in MOS structure in time and frequency domain based on number fluctuation theory. source: [48].

The Fermi Dirac function $f_T(E)$ gives the electron occupation probability of the trap with energy position E . Due to the sharply peaked behavior with energy of the product $f_T(1 - f_T)$, as shown in Figure 2.10, only trap levels within a few kT of the surface Fermi level E_F will contribute to the noise, which simplifies equation (2.13). For a sufficient spread in the tunneling time constant τ_t , the integral in equation (2.13) will reduce to a $1/f$ like spectrum. The longer tunneling times τ_t will correspond to deeper traps, while the higher fluctuation rates will be typical of shallower ('fast') oxide traps.

For the frequency range of <1 kHz, only traps within a distance x from the interface will contribute. For silicon, practical trap depths are expected to be < 2 nm from the Si-SiO₂ interface. Usually, a uniform oxide trap density $N_{oi}(E)$ with depth is assumed in the modeling, although depth dependent trap profiles will lead to a $1/f^{\gamma}$ like spectrum,

with $\gamma \sim 1$. For, $\gamma < 1$, the trap density is shown to increase towards the interface [39], while the opposite is true for $\gamma > 1$. In other words, for a trap distribution with more traps towards the interface, the tunneling time will be smaller so that the high frequency transitions will be emphasized.

Based on the above picture, a number of models for the $1/f$ noise of MOSFETs in linear operation have been established. To explain the $1/f$ noise in the sub threshold regime a variant of the original McWhorter picture was proposed by Fu and Sah [49] where it was assumed that the free carriers interact with a fast interface trap, through thermal capture and emission shown by the path a \rightarrow e \rightarrow f \rightarrow b in Figure 2.10. These processes are fast where a carrier trapped at the interface will be able to tunnel at constant energy to a near interface oxide trap and subsequently tunnel back, which again results in transport fluctuations at low frequencies.

An alternative picture is, when a carrier interacts with an oxide trap through thermal, phonon-assisted transitions. In many cases, thermally activated capture and emission processes play a significant role, so that the relaxation time becomes τ_{th} dependent on temperature based on the equation.

$$\tau_{th} = \tau_0 e^{(E/kT)} \quad (2.16)$$

τ_0 - Attempt time in secs

E - Activation Energy in eV

If it is assumed that the density of traps shows a distribution $D(E)$ as a function of the activation energy E of the oxide trap, the corresponding spectrum becomes

$$S_N(f) \propto \int_{E_0}^{E_1} \frac{D(E)\tau_{th}}{1+(2\pi f\tau_{th})^2} dE \quad (2.17)$$

Following the Dutta-Horn theory [50-52], summarized by equations (2.17), (2.18) and (2.19), a distribution of activation energies E in the interval E_0, E_1 equally leads to a $1/f^\gamma$ noise spectrum.

$$\gamma(\omega, T) = 1 - \frac{1}{\ln(\omega\tau_0)} \left[\frac{\partial \ln S_{VG}(\omega, T)}{\partial \ln T} - 1 \right] \quad (2.18)$$

$$E \approx -kT \ln(\omega\tau_0) \quad (2.19)$$

In this case, the frequency exponent becomes larger than 1 if the oxide trap density increases with energy; and the opposite is true for $\gamma < 1$. No trap profile with depth is necessary to explain the gate voltage dependence of γ and of the flicker noise magnitude. In fact, a specific relationship between $\gamma(\omega, T)$ and the voltage noise spectral density $S_V(\omega, T)$ can be derived from this theory, with ω the radial frequency ($2\pi f$) and to a characteristic attempt time for the random process, with a value of about 1 ps. This attempt time is related to the activation energy of the fluctuation process, according to equation (2.19). This is discussed more in detail in the temperature dependencies on $1/f$ noise, section 3.4. The thermally activated nature of the capture and the emission time constants, observed typically for random telegraph signals (RTSs) in small-area MOSFETs, has lent credence to the Dutta-Horn type of approach for $1/f$ noise, which was originally developed for metals.

Assuming that the fluctuations are in the number (ΔN) or charge density in the homogeneous channel at small V_{DS} , one can express the drain current fluctuations in an elementary area $\Delta y \Delta z$ as

$$\Delta I_D = \frac{W \mu V_{DS} q \partial N \Delta y \Delta z}{LWL} \quad (2.20)$$

In writing Equation (2.20), a linear MOSFET model is assumed, for a device with area $W \times L$ and mobility μ . In this model, fluctuations in mobility are neglected, while ΔN is the number fluctuation in the elementary surface $\Delta y \Delta z$ and q is the elementary charge. The corresponding drain current noise power spectral density is then S_{ID} .

$$S_{ID} = \frac{I_D^2}{W^2 L^2 Q_N^2} q^2 S_N \quad (2.21)$$

with

$$Q_N = C_{ox} (V_{GS} - V_T) \quad (2.22)$$

C_{ox} is the gate oxide capacitance per cm^2 , V_{GS} the gate voltage, V_T the threshold voltage, and I_D is the drain current. The corresponding input (or gate) referred noise spectral density follows from S_{VG} .

$$S_{VG} = \frac{S_{ID}}{g_M^2} = \frac{q^2 S_N}{W^2 L^2 C_{ox}^2} \quad (2.23)$$

where g_m is the transconductance.

Combining with equation (2.13) and assuming that the trap density is uniform in energy and depth finally results in the well-known expression [39]

$$S_{VG} = \frac{kTq^2}{8WLC_{ox}^2 \alpha_t} \frac{N_{ot}(E_F)}{f} \quad (2.24)$$

where the function $f_T(E)$ [$1 - f_T(E)$] is sharply peaked around the surface Fermi level E_F . In this way, only oxide traps in an energy interval of $2kT$ around E_F contribute to the $1/f$ noise.

2.4.2 Mobility Fluctuation Theory - $\Delta\mu$ Model

The $\Delta\mu$ model is purely empirical in nature and has first been proposed to explain the 1/f noise in resistors [45, 53]. It was observed by Hooge [45] and the normalized current noise spectral density for a wide range of materials could be represented by the empirical relationship

$$\frac{S_{ID}}{I_D^2} = \frac{\alpha_H}{Nf} \quad (2.25)$$

In writing equation (2.25) it is assumed that the device shows an ohmic I-V characteristic so that the spectral density scales with I^2 . N is the total number of carriers in the conductor, or more generally the total number of fluctuators. Originally, it was thought that α_H was a fundamental constant for all materials, approximately 10^{-3} . α_H is a dimensionless quantity for a frequency exponent $\gamma = 1$. However α_H is considered a figure of merit parameter, which can vary over many decades, depending on the number of defects present in the device.

Devices with reduced α_H value correspond to a low 1/f noise and vice versa. For Si-SiO₂ interface, values have been found to be in the range 5×10^{-6} to 2×10^{-3} [45, 53]. As such, the α -parameter and 1/f noise in general can thus be used to investigate the quality and processing induced defects in semiconductor technology. The major problem with noise studies is to identify the responsible source, since there are many different fluctuation processes to be considered.

Strictly speaking, α_H is not a constant but depends on the crystalline quality has led to the following [46, 54]

$$\alpha_H = \alpha_{latt} \left(\frac{\mu}{\mu_{latt}} \right)^2 \quad (2.26)$$

with α_{latt} a constant $\sim 2 \times 10^{-3}$, μ the carrier mobility and μ_{latt} the mobility due to lattice scattering only. The different scattering mechanisms are parallelly active, resulting in a total mobility which follows Matthiesen's rule and is smaller than μ . From equation (2.26), it is inferred that the lattice phonon scattering is the dominant $1/f$ noise generating process, while other types of scattering, related to defects (Coulombic, surface roughness scattering) suppress the $1/f$ noise, at low frequencies.

Adapting Hooge's law to the case of a standard MOSFET in linear operation results in

$$S_{V_G}(f) = \frac{q\alpha_H}{C_{ox}WLf} (V_{GS} - V_T) \quad (2.27)$$

which is valid above threshold and predicts a linear dependence on the gate overdrive voltage. Experimentally, p-channel devices are better described by equation (2.27) and thus experience mobility fluctuations. This is explained physically by the fact that short length p-channel devices fabricated in standard technologies, with a single n^+ polysilicon gate material, show a buried channel behavior and thus can be considered as a 'bulk' device compared with an n-MOSFET, which has a more 'surface-like' nature. The larger separation of the inversion layer from the interface and the oxide traps explains the lower $1/f$ noise which is generally found for p-MOSFETs in the same CMOS technology.

The mobility theory in the weak inversion behavior, should be according to equation 2.27 and follow a $1/N$, or a $1/I_D$ law. This means that the normalized drain current noise should increase exponentially in the sub threshold regime. However for

most of the p-channel devices, some increase is also observed below the sub threshold regime [55], which is less than predicted by equation (2.27).

Another unsolved question is the theoretical explanation of the α_H . Although several theories have been advanced, none are generally accepted, so that the Hooge parameter is considered as purely empirical.

2.4.3 Number-Mobility Correlated Theory - ΔN - $\Delta\mu$ Model

While the previously described models can be categorized as pure number or pure mobility theories, recent modeling efforts try to combine the two effects in order to come to what can be viewed as a universal $1/f$ noise theory for MOSFETs. One of the first attempts was made by Mikoshiba *et al.* [56, 57] the sum of a ΔN and a $\Delta\mu$ term was considered and it was experimentally found that the two terms were in fact correlated. The systematic study of RTS in small area MOSFET has helped in understanding this effect and resulted finally in the development by some research groups of what could be considered as a correlated mobility fluctuation theory. The variation of the RTS amplitude at high drain currents has been explained by considering interface and bulk oxide trap scattering and the resulting amplitude is given with α_{sc} a scattering parameter which is in the range of 2×10^{-15} Vs [58].

The basic concept of the correlated mobility fluctuations model is that it takes into account that the oxide/interface traps not only interact with the channel through carrier capture and generation, but also indirectly through a change in scattering rate, when the trap becomes occupied or emptied. This is generally accompanied by a change in the charge state of the scattering centre, which strongly affects the impact on the mobility;

through a change in the scattering cross section from a charged centre to a neutral one or vice versa. The drain current noise spectral density takes the form [59, 60].

$$S_{ID} = \frac{kTI_D^2}{\alpha_i fWL} \left(\frac{1}{N} \pm \alpha_{sc} \mu \right)^2 N_{ot}(E_F) \quad (2.28)$$

and yields a satisfactory fit for both n- and p-MOSFETs in a broad temperature range. Based on equation (2.28), a quadratic dependence on $(V_{GS}-V_T)$ is expected [59]. The resulting input-referred noise spectral density becomes

$$S_{VG} = S_{VFB} \left[1 \pm \alpha_{sc} \mu C_{ox} (V_{GS} - V_T) / q \right]^2 \quad (2.29)$$

where S_{VFB} the flat-band voltage noise spectral density, where

$$S_{VFB} = g_m^{-2} S_{ID} \quad (2.30)$$

If the scattering parameter α_{sc} is small, then ΔN theory is considered. Note that if different types of oxide trap, i.e. donor- and acceptor-like, are present; equations (2.28) and (2.29) can produce a local minimum in the noise for a certain drain current or gate overdrive voltage in linear operation. This is related to the + or - sign in the equations, or in other words, whether the trap induced mobility change assists or opposes the number reduction.

In order to discriminate between the different $1/f$ noise sources, the following procedure is adopted in this dissertation. The normalized drain current noise (S_{ID}/I_D^2) in linear operation is plotted versus the drain current in a log-log plot and compared with the $(g_m/I_D)^2$ ratio. If both curves run parallel, the number fluctuations dominate the overall $1/f$ noise behavior. Additionally, correlated mobility fluctuations will be present when the S_{VG} shows a quadratic increase with the gate overdrive voltage. Mobility fluctuations could be the origin of the $1/f$ noise if the normalized drain current noise varies according

to $1/I_D$, especially in weak inversion. Additionally, the S_{VG} will diverge in that case below threshold and follows a $1/I_D$ law.

CHAPTER 3

NOISE IN HF-BASED MOSFETS

This section deals with a literature review of the low-frequency noise mechanism in Hf-based MOSFETs. A brief consideration on noise in other high- κ dielectrics devices is also presented. Finally, the temperature dependence on $1/f$ noise is outlined.

3.1 Noise in High- κ Dielectrics

3.1.1. Introduction

This section deals about the low-frequency noise performance based on the work done by some of the researchers at IMEC, University of Texas at Arlington, University of Calabria, NEC laboratories of Japan, KTH institute of Sweden.

3.1.2. Literature Study and Review

The technology shift due to the replacement of the SiO_xN_y gate dielectrics with materials having a higher dielectric constant κ leads to orders of magnitude (1-3) higher $1/f$ noise compared to CMOS devices with thermal SiO_2 . The higher $1/f$ noise is in most cases ascribed to a high density of traps in the high- κ gate dielectrics. Hooge mobility fluctuation noise is also important, especially in p-channel MOSFETs. Traps in the high- κ material, located from near the channel interface to several nm inside the bulk of the material, can contribute to the $1/f$ noise. Earlier Simoen *et al.* [61] showed that electrons tunneling to and from traps in an HfO_2 layer deposited on 2.1-nm SiO_2 are the origin of the $1/f'$ noise in the devices, which illustrates the McWorter type noise

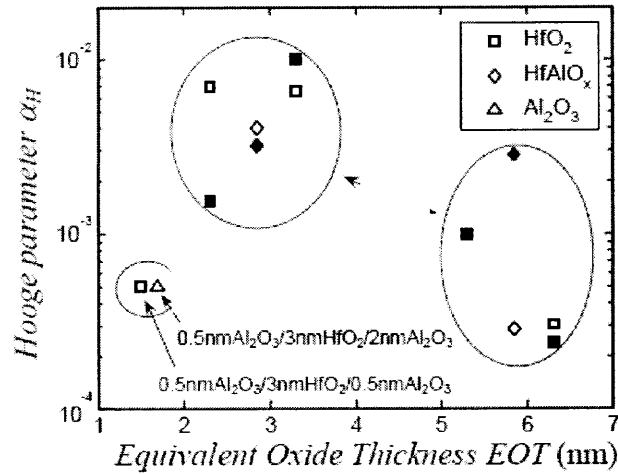


Figure 3.2 A summary of reported values of α_H plotted versus EOT. Filled symbols denote n-MOSFET and open symbols p-MOSFET, respectively. source:[62]

Giusi *et al.* [63] studied low-frequency noise in strained p-MOSFETs, with four different gate stacks as SiO_2 , SiON , HfO_2 and HfSiON of thickness nominally equivalent to 1.5 nm. The results are summarized in the following figures.

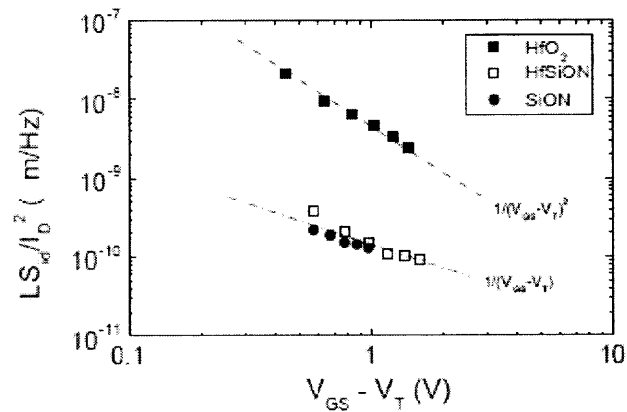


Figure 3.3 Normalized noise data with HfO_2 $L = 0.25 \mu\text{m}$, HfSiON $L = 0.25 \mu\text{m}$ and SiO_2 $L = 0.20 \mu\text{m}$. source:[63]

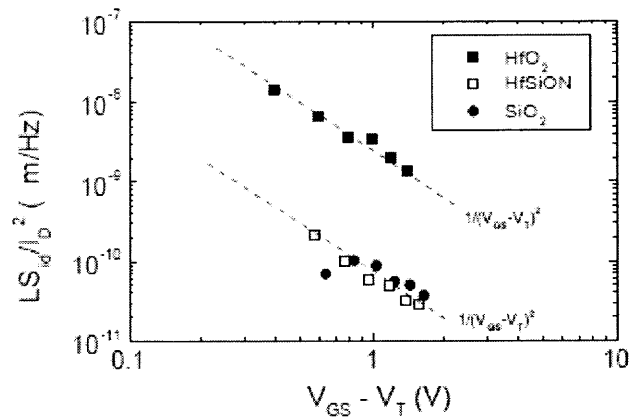


Figure 3.4 Normalized noise data with HfO₂ L = 1 μm, HfSiON L = 1 μm and SiON L = 1 μm. source:[63]

Invariably, the noise is found to be higher at least by an order of magnitude for HfO₂ devices while HfSiON results comparable to that of SiON layers. The results support the unified model of correlated number and mobility fluctuations ($\Delta N - \Delta \mu$) as the dominant noise mechanism in >1.5nm thick HfO₂ devices, while the thinner devices follow the $\Delta \mu$ theory.

3.1.3. Interfacial Layer Thickness Effects in nMOSFETs

The interfacial layer effect in nMOSFETs has been studied in detail by Simoen *et al.* [61]. A summary of the results is presented here as prelude to the observations that has been carried out in aggressively scaled metal gate n-MOSFET and p-MOSFET devices. They have assumed that if the dominant mechanism in high- κ stacks is number fluctuations, the current spectral density (S_{ID}) at a frequency of 1 Hz will be sensitive to traps within a distance of 2.5nm from the Si-SiO₂ (IL) interface. This would imply that

S_{ID} will strongly depend on the features of the interfacial layer that is present between the Si-substrate and the high- κ material.

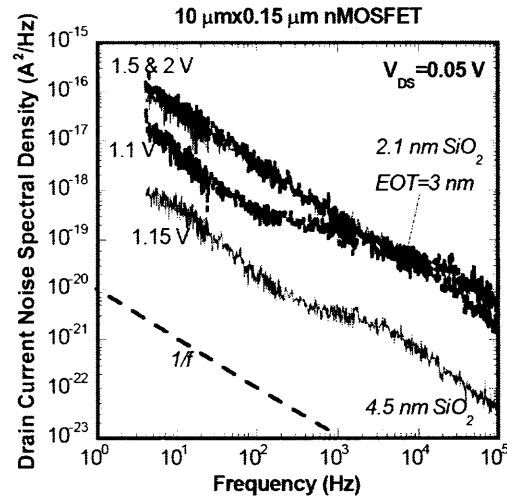


Figure 3.5 Low frequency drain current noise spectra at $V_{DS} = 0.05$ V for two different interfacial layer thicknesses studied. source:[61]

The influence of low-frequency noise was studied for three processing splits each with different interfacial layer thickness. The interfacial layer thicknesses were varied as i. 0.8 nm ii. 2.1 nm and iii. 4.5 nm on the top of which MOCVD processed HfO₂ was deposited in such a way that the EOT of all the devices were close to 2 nm. From Figure 3.5 it is seen that the intermediate case of 2.1 nm showed a mixed S_{ID} Vs f behaviour where at low gate voltages, the S_{ID} spectra appeared to be typical for thermal SiO₂, while at higher gate voltages, trapping in HfO₂ enhanced the noise spectral density. From the normalized noise spectral density and drain current graph as shown in Figure 3.6, a clear trend was observed where the curve for intermediate interfacial thickness n-MOSFET came close to thick SiO₂ case at low drain currents and overlaps with 0.8nm interfacial layer data at higher gate bias.

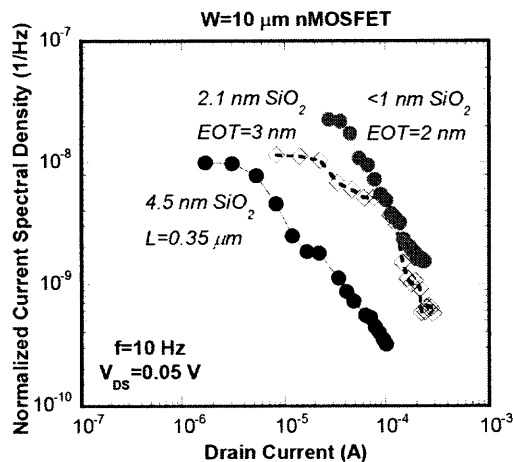


Figure 3.6 Normalized current spectral density versus I_D for an n-MOSFET with 5 nm ALD HfO_2 and of three different interface layer thickness, at $f=10$ Hz and $V_{DS}=0.05$ V. source:[61]

It was concluded that the dominant noise mechanism was indeed number fluctuations, as per their initial assumption, from the observed parallelism between normalized noise (S_{ID}/I_D^2) and $(g_m/I_D)^2$ ratio as per the graph shown in Figure 3.7.

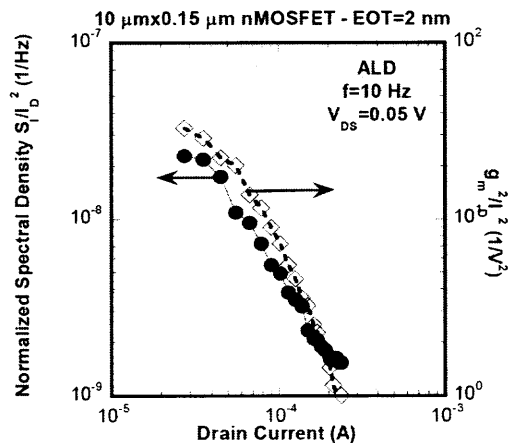


Figure 3.7 S_I/I_D^2 vs I_D for an $L=150$ nm n-MOSFET with an $EOT=2$ nm (HfO_2 by ALD). source:[61]

The input referred voltage spectral density multiplied by L was represented as a function of gate voltage overdrive $|V_{GS} - V_T|$ as shown in Figure 3.8. Significant higher noise in thinner SiO_2 compared with the thicker SiO_2 was observed which was related to the high defectiveness of the HfO_2 layer.

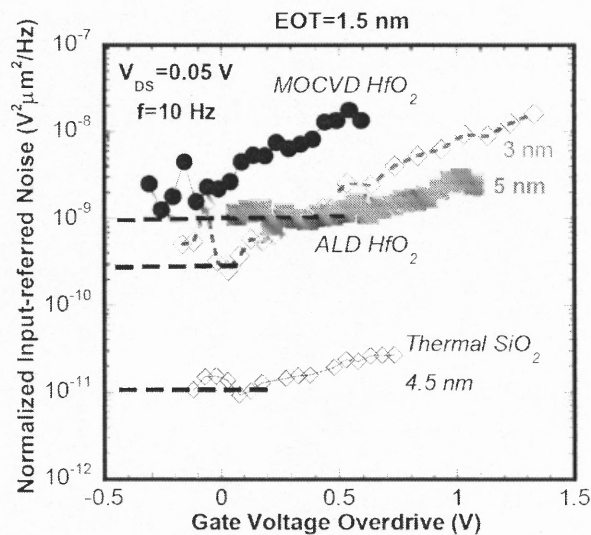


Figure 3.8 Normalized input-referred voltage noise spectral density versus gate voltage overdrive for ALD n-MOSFETs with two different interfacial layer thickness in comparison with 4.5 nm SiO_2 device. $f=10 \text{ Hz}$ and $V_{DS}=0.05 \text{ V}$. source:[61]

The observation agreed with the proposed model for the threshold voltage V_T instability, based on the defect band below the conduction band of HfO_2 . Section 5.1 deals with the interfacial layer effects and also the quality of interfacial layer on $1/f$ noise in TiN-TaN n- and p-MOSFETs in detail.

3.2 1/f Noise in La₂O₃ Based Systems

This section briefly discusses low-frequency noise and its behavior in La₂O₃ based system.

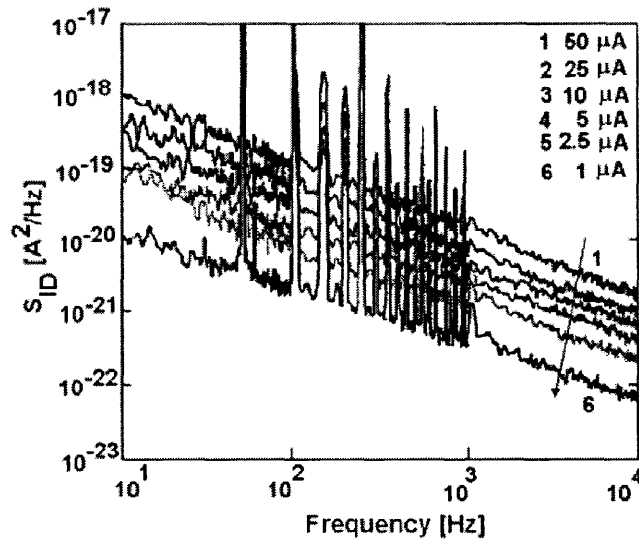


Figure 3.9 Low frequency noise performance of a 27 $\mu\text{m}/2.5 \mu\text{m}$ n-MOSFET La₂O₃ device. source: [64].

Saaddin *et al.* [64] have studied the noise behavior and mechanism in La₂O₃ gate dielectrics. Al was used as metal gate and equivalent oxide thickness (EOT) was evaluated to be 3 nm. 1/f noise was measured in linear and saturation region of operation and found that the noise is higher by two orders of magnitude when compared to Si-SiO₂ based devices. A high value of oxide trap density ($1.2 \times 10^{19} \text{ eV}^{-1} \text{ cm}^{-3}$) has been estimated. From their normalized noise and $(g_m/I_d)^2$ curves, it can be deduced that the noise mechanism is mainly due to number fluctuations in their case.

3.3 1/f Noise in Al₂O₃ and HfO₂/Al₂O₃ Systems

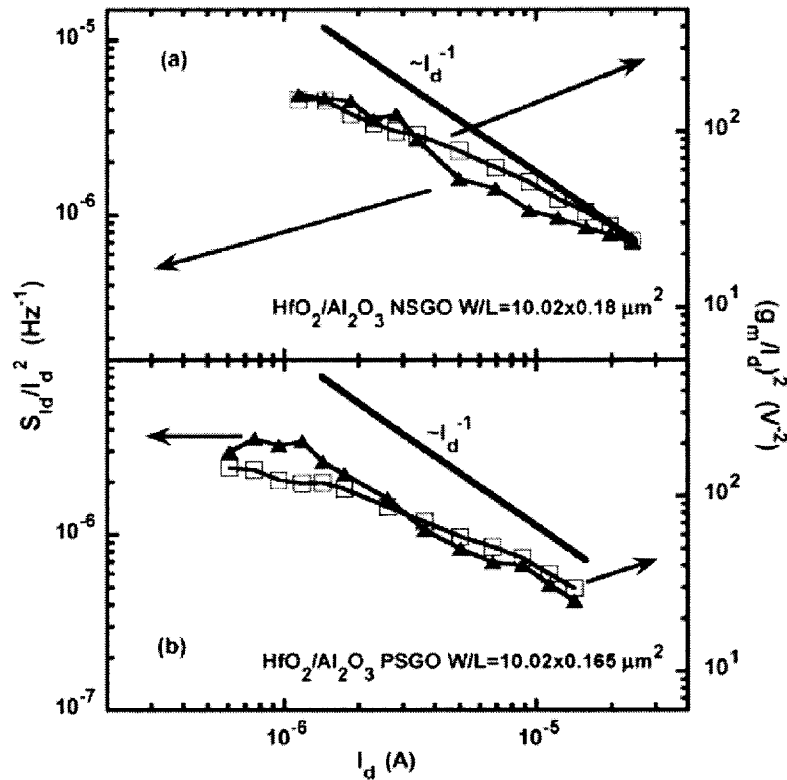


Figure 3.10 Comparison of drain current and normalized drain current noise spectral density at 1 Hz and transconductance. The solid straight line depicts I_D^{-1} dependence for each case. $V = 40$ mV. source:[65].

Min *et al.* [65] have studied various types of high- κ devices including Al₂O₃ based gate stacks. They have also analyzed in a similar way to understand the noise mechanism in these gate dielectrics and found that if bulk mobility fluctuations were the main cause of 1/f noise, then, S_{ID}/I_D^2 should be proportional to I_D since channel carrier concentration N is proportional to I_D . From the above Figure 3.10 they concluded that origin of 1/f noise is the interface (number fluctuations) and not bulk (mobility) in these devices.

Haartmann *et al.* [62] Studied the low-frequency noise Si and SiGe surface channel p-MOSFETs with various types of high- κ gate dielectrics (Al_2O_3 , $\text{Al}_2\text{O}_3/\text{HfAlO}_x/\text{Al}_2\text{O}_3$ and $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3$) as shown in Figure 3.11. The $1/f$ noise was explained by the unified number fluctuation model correlated to mobility ($\Delta N - \Delta \mu$) for n-MOSFETS, while p-MOSFETS follow Hooge's mobility model. It was found that the density of traps in the gate dielectrics was found to be in the range of $1 \times 10^{18} - 4 \times 10^{19} \text{ cm}^{-3} \text{ eV}^{-1}$, with the Al_2O_3 device showing higher values than the tri-layer stack devices, which roughly scaled with the thickness of the Al_2O_3 in the gate dielectrics. Thus, the main source of the $1/f$ noise is attributed to traps in the Al_2O_3 . The channel composition, Si vs. SiGe, plays a negligible role for the $1/f$ noise, although the density of interface states differs by a factor of six (higher in the SiGe devices).

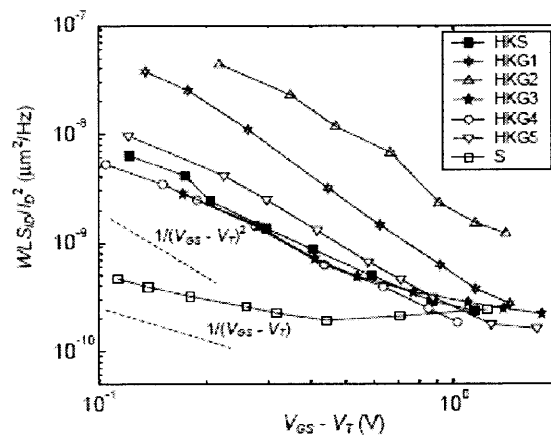


Figure 3.11 Normalized drain current noise at 10 Hz vs. gate voltage overdrive. $V_{DS} = -50 \text{ mV}$. $W \times L = 10 \mu\text{m} \times 0.8 \mu\text{m}$. HKS refers to $\text{Al}_2\text{O}_3/\text{HfAlO}_x/\text{Al}_2\text{O}_3$ (0.5/4/0.5 nm), HKG1 refers to Al_2O_3 (5 nm) $\text{Si}_{0.8}\text{Ge}_{0.2}$ (10 nm) 3.2 nm, HKG2 Al_2O_3 (5 nm) $\text{Si}_{0.7}\text{Ge}_{0.3}$ (10 nm) 3.4 nm, HKG3 refers to $\text{Al}_2\text{O}_3/\text{HfAlO}_x/\text{Al}_2\text{O}_3$ (0.5/4/0.5 nm) $\text{Si}_{0.8}\text{Ge}_{0.2}$ (10 nm) 2.4 nm, HKG4 $\text{Al}_2\text{O}_3/\text{HfAlO}_x/\text{Al}_2\text{O}_3$ (0.5/4/0.5 nm) $\text{Si}_{0.7}\text{Ge}_{0.3}$ (10 nm) 2.7 nm, HKG5 refers to $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3$ (0.5/4/0.5 nm) $\text{Si}_{0.7}\text{Ge}_{0.3}$ (10 nm) 2.2 nm, while S refers to SiO_2 (3 nm) Si 3 nm. source: [62].

3.4 Temperature Dependence of 1/f Noise

It has been earlier discussed in 2.4.1 that 1/f noise is a thermally activated process having a broad distribution of energies relative to kT since the capture and emission times of traps are strongly temperature dependent [50-52]. The frequency and the temperature are related via

$$\gamma(\omega, T) = 1 - \frac{1}{\ln(\omega\tau_0)} \left[\frac{\partial \ln S_{VG}(\omega, T)}{\partial \ln T} - 1 \right] \quad (3.1)$$

where τ_0 is the “attempt to escape frequency” for the defect. In that case, the shape of defect-energy distribution can be inferred from the noise measurements via

$$S(\omega) \propto \int \frac{\tau}{1 + \tau^2 \omega^2} D(\tau) d\tau \quad (3.2)$$

If the noise process involves a distribution of characteristic times $D(\tau) \propto \tau^{-1}$ for $\tau_1 \leq \tau \leq \tau_2$, then the defect energy is related to the temperature and frequency through the expression

$$E_0 = -kT \ln(\omega\tau_0) \quad (3.3)$$

Hence, 1/f noise cannot be easily be described or modeled as simple capture or emission of charge by defects with single energy levels as they are strongly correlated with activation energy levels of these defects. Evidence of thermally activated charge exchange between the Si channel and defects in the near interfacial SiO_2 has been already shown in SiO_2 based devices by Fleetwood *et al.* [66].

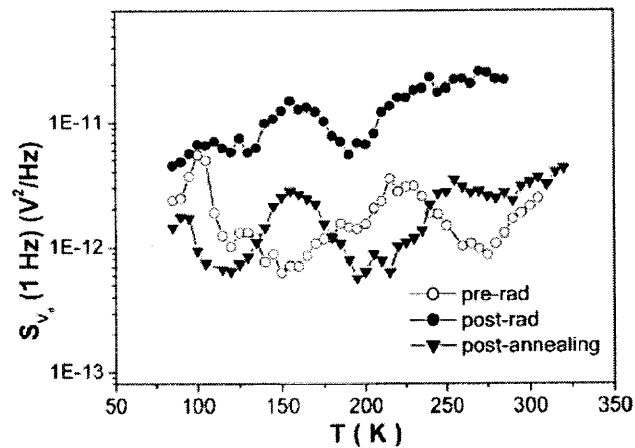


Figure 3.12 The noise magnitude at 1 Hz versus temperature for SiO₂ before irradiation (open circles), after 10-keV X-ray irradiation to 500 krad (SiO₂) (solid circles), and after a 24 h anneal at 477 K at 0 V (solid triangles). source: [66].

The typical trap densities in high- κ devices are ~ 50 times higher than a reasonable quality SiO₂, while the noise spectral densities are at least higher by an order of magnitude. Also the interfacial SiO₂ layer is seen to have a strong impact on LF noise spectra [67]. Though it is predicted that similar effects with high- κ , it is important to study the effects arising due to the presence of high- κ layers due to its inherent nature of high defect densities when compared to SiO₂ dielectrics.

Hence the temperature dependence study of $1/f$ noise in high- κ based dielectrics becomes inevitable, to have a complete understanding on the trap profile distribution and subsequent modeling in high- κ based dielectrics. This is the main topic of discussion in Chapter 5 and Chapter 6 of the dissertation.

CHAPTER 4
TECHNOLOGICAL AND EXPERIMENTAL ASPECTS

4.1 Noise Characterization and Setup

This section deals with the measurement setup that was used to characterize the devices for low-frequency (1/f) noise. A near-common setup was used to characterize at room and high temperatures, while a different setup was used to characterize at low temperatures.

4.1.1 Noise Characterization Setup at High and Room Temperatures

Figure 4.1 shows the noise characterization setup used for the study at room temperatures

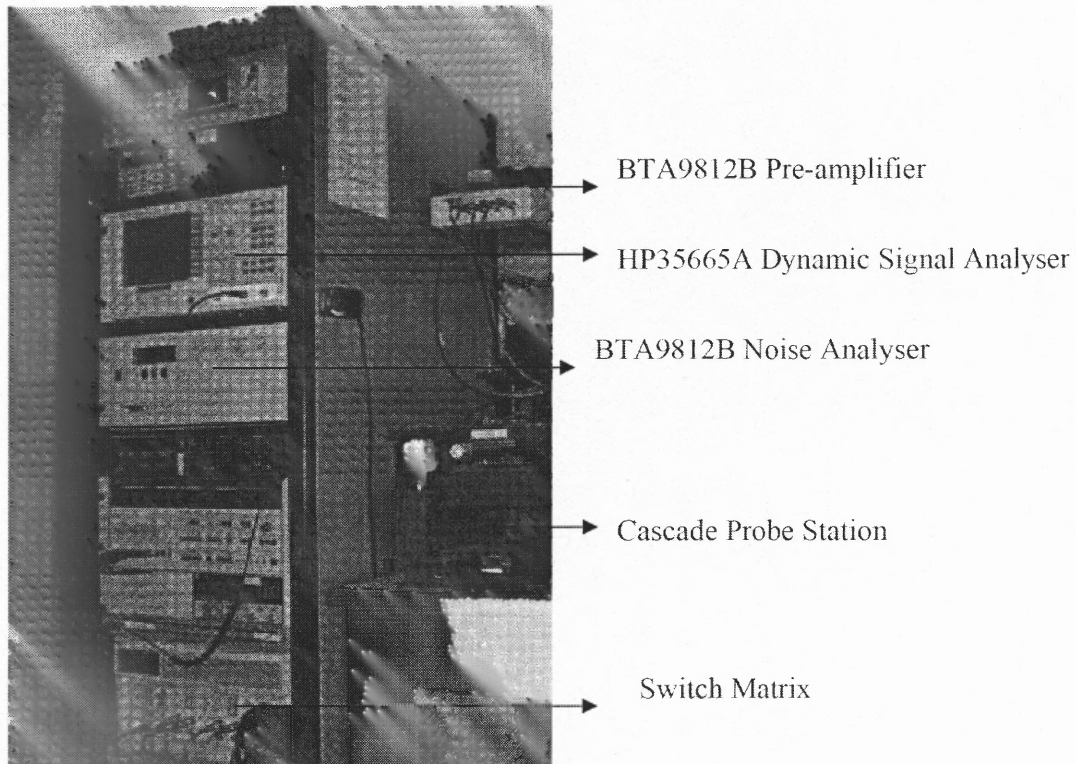


Figure 4.1 Wafer-level low-frequency noise characterization system.

Wafer-level devices fabricated using CMOS process flow was used for the investigation of low-frequency noise in high- κ dielectrics. The fabricated devices were mounted on the cascade probe station which was controlled manually. The terminal output of transistors was then directly connected to Berkeley Technology Associates BTA9812B Noise pre-amplifier. It is to be noted in the setup that the cables leading to the pre-amplifier is very short since the length of the cable should be minimum as possible. This would help in reducing the noise pick-up from the external environment and also avoid RC impedance effects of the cable to interfere with the low-frequency noise level in the devices. Once the noise gets amplified by the pre-amplifier, the output is then connected to the BTA9812B noise analyzer, through the switch matrix. Switch matrix here is mainly to shift the two types of setup seen above – i. Device $1/f$ noise setup and ii. Device stress setup. This noise pre-amplifier and analyzer has the capability to amplify either voltage noise or current noise. It is ideal to use current amplifier at lower voltages and voltage amplifier at higher voltages. However, in most of the cases, the voltage amplification has been used. The output of the noise analyzer is then connected to dynamic signal analyzer HP35665A. Dynamic signal analyzer is essentially a spectrum analyzer which provides the basic information on the voltage or current spectral density of the measured $1/f$ noise.

The whole setup is controlled automatically via GP-IB cables and a special software by Celestry Technologies – NOISEPRO™ [68] is used to analyze and record the measured data. Figure 4.2 shows the typical screen for bias measurement setup for MOSFETs.

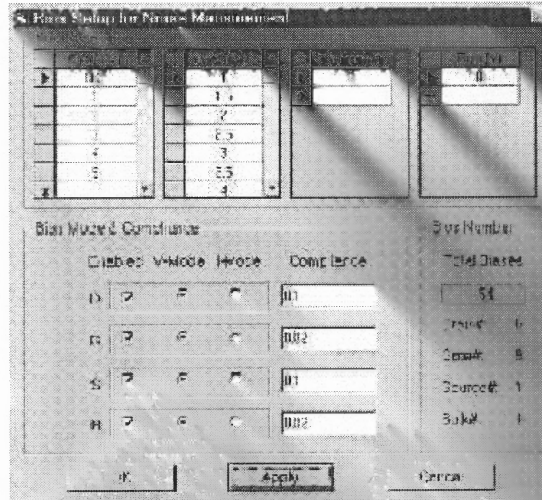


Figure 4.2 Voltage bias setup screen using NoisePro software.

The same setup has been used to measure low-frequency noise at high temperatures except that the adjacent cascade probe station was used along with the above the setup. The main reason was employing adjacent probe station is to have access to the temperature system which can heat the wafer to the required temperature. This setup is presently located in AMSIMEC labs of InterUniversity MicroElectronics (IMEC) Center, Leuven, Belgium.

4.1.2 Low-Frequency Noise Measurement Setup at Low Temperatures

Figure 4.3 and 4.4 shows the low-frequency noise characterization system used for low-temperature measurements. The cryo-setup is shown in Figure 4.3. The samples were mounted on a four terminal low-temperature device chamber. To operate the device at low-temperatures, the pressure in the chamber needs to be reduced to reach ultra-low vacuum level in the order of $10^{-7} \sim 10^{-8}$ Torr. A portable two-level high speed cryo-pump system is used for the same. The first-level pump reduces the atmospheric pressure in the device chamber to moderate pressure to the order to $10^{-3} \sim 10^{-4}$ Torr.

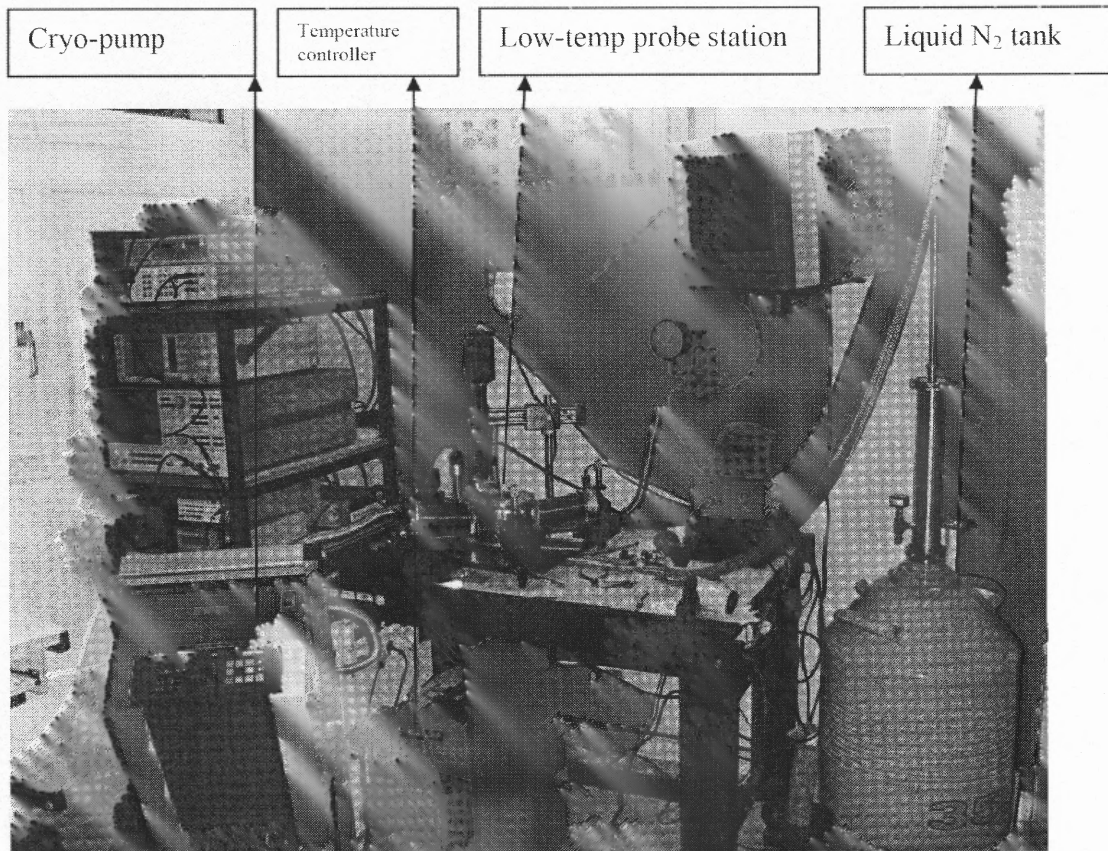


Figure 4.3 Low-temperature low-frequency noise characterization system showing the cryo-setup.

The system automatically switches to cryo-pump when the above pressure is sensed using the built-in pressure sensors. A 8-16 hour wait is required to achieve such low-vacuum levels. The cryo-pump is stopped and disconnected from the chamber once the required pressure is obtained. This is mainly to avoid the interference from the inductive-motors which is very sensitive on the noise measurement system. The pressure level in the chamber is also continuously monitored using a pressure monitor already connected to the device chamber.

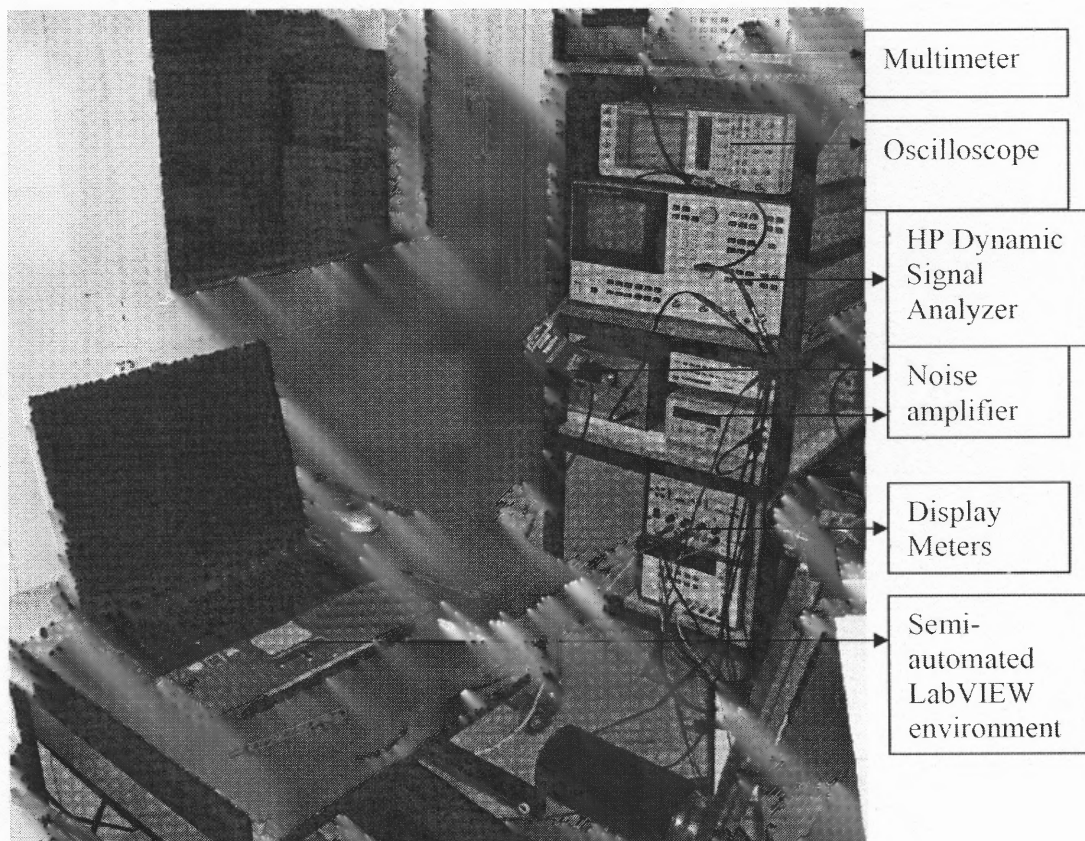


Figure 4.4 Low-temperature low-frequency noise characterization system.

Once the pressure reaches ultra-low vacuum levels, the low-temperature system is activated by adjusting the pressure levels in the liquid nitrogen tank connected to the low-temperature chamber. The temperature of the device chamber is controlled using temperature controller as shown in Figure 4.3. The sensitivity of the controller is high enough to maintain the set temperature at $< 1\%$ error.

Figure 4.4 shows the electrical side of the low-temperature measurement system in detail. The system essentially performs the same function as explained for room temperature measurement setup except that the method in which the spectrum is different. The total system is differentiated into two main parts – i. setup to measure noise voltage spectral density from 1 Hz to 10 Hz and ii. Setup to measure noise voltage

spectral density from 10 Hz to 10^5 Hz. Typically, for measuring 10Hz to 10^5 Hz the noise is amplified and then a noise analyzer is used and the equipment used is depicted in Figure 4.4. HP based dynamic signal analyzer is also used here for output spectral density display. Multimeters are employed to set and monitor the voltage bias levels applied at the gate and drain terminals of the transistors. An oscilloscope is also used to monitor possible interferences from the power line sources and external environment. The whole setup is semi-automated and is operated under LabView™ environment where the spectral density outputs can be stored in the personal computer directly. These measurements were performed in Noise instrumentation Laboratory at GREYC-ENSICAEN, CEDEX, France

For both room temperature and low-temperature setups used, a 16-level sampling was performed to obtain the noise spectrum. The drain-to-source resistance was also monitored appropriately and necessary modifications to the spectra are performed to obtain the results for the measured devices.

One other issue during low-frequency noise measurements on transistors with high- κ gate dielectrics is the threshold voltage instability. A low-frequency noise measurement from 1 Hz to 10^5 Hz takes several minutes. During this time period, the threshold voltage can shift a few tenths of volts, in the worst case. As the threshold voltage is not fixed, care must be taken when studying the noise variation with the gate voltage overdrive for example. In these measurements, the devices were given some time to settle after each bias point adjustment. The drain current was measured before and after the noise measurements at each bias point and the average current was used in the calculations. The variations in the average drain current and transconductance were found

to be acceptably low ($< 1\%$) in most cases, except at low currents in the subthreshold region.

4.2 Gate Dielectric and Gate Electrode Deposition Techniques

The main aim of this section is to provide a broad idea of the process technologies involved in the fabrication of the devices employed in the study of $1/f$ noise. The devices that were used to characterize $1/f$ noise involved different IMEC-related process steps. Due to the limited access to IMEC-specific process steps, only a basic understanding about the different deposition methods are presented here. The deposition techniques are broadly classified into two main categories:

1. Deposition of high- κ gate dielectric material
2. Deposition of metal gate electrode material.

4.2.1 Deposition of High- κ Gate Dielectric

Two types of process are mainly employed in the deposition of high- κ dielectric:

1. Atomic layer Deposition process (ALD)
2. Metal Organic Chemical Vapor Deposition process (MOCVD).

4.2.1.1 Atomic Layer Deposition. There are some special considerations for the deposition of high- κ gate oxides by atomic layer deposition process [10]:

1. The deposition process should help in reducing the equivalent oxide thickness (EOT) by protecting the permittivity of the deposited high- κ dielectric. In other words, there should be less formation or intermixing of layers which can reduce the value of k .
2. The starting layer of this deposition is typically Si or SiO_2 . The precursors should be selected in such a way that it will not react with silicon during the deposition or the annealing treatments.

3. The film growth and coverage should be comparable or better than that of deposition of SiO_2 . In other words, it should provide a good uniform film surface.
4. The last consideration is how oxidative the ALD process is towards silicon. The different oxygen sources are arranged in increasing order of oxidation power: oxygen radical \rightarrow ozone \rightarrow hydrogen peroxide \rightarrow water \rightarrow alkoxides of metals with highly stable oxides.

The first ALD processes for HfO_2 were based on HfCl_4 and water. There are two main concerns related to HfCl_4 based processes. Since these solids consist of very fine particles, the particle transportation from the source to the film becomes difficult. The second is poor nucleation on hydrogen terminated silicon. Generally this problem is highly reduced if the starting layer is thin silicon oxide, since the nucleation highly improves. Sometimes, the chlorine residues left from the precursors are also considered as a potential problem but post-deposition annealing has been found to decrease the chlorine residue content, present, if any. As far as the deposition rate is concerned, it is found to decrease with increasing temperature and typical values of 0.5-1.0 Å/cycle have been reported at 500 C.

HfO_2 films deposited by this process have a film structure that develops from an amorphous phase through the metastable tetragonal or cubic phase to the stable monoclinic phase as the deposition temperature and film thickness increase. If HfO_2 crystallizes, they become monoclinic but sometimes the tetragonal phase is also present. In general, the films $< 5\text{nm}$ are amorphous as deposited but crystallize during annealing. Quite wide range of permittivities of 12-22 [69-72] have been reported for ALD deposited HfO_2 . When HfO_2 is deposited on SiO_2 it is found to provide four to five

orders of magnitude reduction in leakage current [71] while poor dielectric characteristics have been obtained on hydrogen-terminated silicon mainly because of poor nucleation.

Studies have also been performed on possible alternative hafnium precursors to overcome the above addressed issue of particle size and nucleation. HfI_4 is one such potential precursor [72]. Although it reduces or eliminates the above issues, it results in unwanted formation of interfacial layer. Alkoxides of hafnium provide poorer thermal stability. 1-methoxy-2-methyl-2-propanolate complex of hafnium and metal alkylamide hafnium tetrakis (ethylmethylamide) [73] are also considered potential hafnium precursors. Finally, hafnium nitrate [74] has been used as a precursor in ALD of HfO_2 films, since easy decomposition of this compound has made it attractive, but found to be sensitive to the external environment such as the condition of the deposition chamber.

4.2.1.2 Metal Organic Chemical Vapor Deposition. Chemical Vapor Deposition is a process by which gaseous molecular precursors are converted to solid-state materials on a heated surface. CVD is always performed in a vacuum or inert atmosphere to prevent incorporation of unwanted matter during deposition. For CVD of high- κ materials the metal-containing precursors with or without the oxidizing agents are directed to a heated surface leading to their decomposition and the deposition of high- κ dielectric materials. Precursors for CVD of metal oxides generally fall into one of three classifications – organometallic, metalorganic or inorganic compounds. Basically all the chemicals used in ALD can be used for CVD processing. However, metal halides are normally avoided in CVD because of their higher decomposition temperature and O_2 is normally used as the oxidant. Metal alkoxides, β -diketonates, metal alkyl amides and metal nitrates are common precursors for CVD of high- κ materials.

One of the issues in the CVD of metal oxides from MO sources is the inclusion of impurities such as carbon and hydrogen in the films. These arise due to incomplete scission of one of the organic ligands. Metal nitrate is a promising new precursor as it could lead to hydrocarbon free deposition of high- κ dielectric materials due to absence of hydrogen or carbon atoms.

The composition and microstructure of the CVD deposited films depend largely on the deposition conditions and the purity of the precursors. The films typically incorporate carbon impurities which can be increased by increasing the oxygen flow rate. Generally, the deposited films are likely to be polycrystalline with an interfacial layer on silicon.

4.2.1.2 Deposition of Interfacial Oxide. In most of the devices studied, the interfacial layer used here is silicon dioxide (SiO_2). The interfacial oxide used here is chemically grown oxide using dry oxidation process. The surface chemistry is ozone based and is termed as IMEC clean process. One of the studies described in Chapter 5 involved the nitridation on the interfacial layer. This was performed using Decoupled Plasma Nitridation (DPN). DPN of interfacial oxide is a new technology using inductive coupling to generate nitrogen plasma thereby high level of nitrogen is incorporated uniformly onto the top surface layer which is the Si substrate in this case.

4.2.2 Deposition of gate electrode material

Two types of gate electrodes were predominantly studied i. poly-Si ii. TiN-TaN metal gate. In either case, two types of process technologies in the deposition of the gate electrode were used:

- i. Physical Vapor Deposition (PVD).
- ii. Atomic Layer Deposition (ALD).

Atomic Layer Deposition process for high- κ dielectric has already been discussed earlier in section 4.2.1.1. For gate electrode materials, the process essentially remains the same, except that the precursors change for gate electrode materials.

4.2.2.1 Physical Vapor Deposition. In physical vapor deposition, vacuum evaporation, sputtering deposition, oxidation of metals and laser-assisted deposition have all been used to deposit the gate electrode material. They found to have some unique aspects with respect to other processing with regard to gate electrode deposition [75].

- i. A versatile and robust family of techniques is available.
- ii. Deposition of gate electrode material is not limited to the synthesis of volatile and stable gas-phase metal-containing precursors.
- iii. A broad range from near room temperature to very high temperatures is available.

4.3 Gate Capacitance and EOT determination

Typically, the gate capacitance and the equivalent oxide thickness of the gate dielectrics studied are extracted using capacitance-voltage (C-V) characteristics. If poly-Si is used as a gate electrode material, the poly-depletion effect due to the formation of depletion layer between the poly-Si and gate oxide and also the inversion-layer width add series capacitances to the oxide capacitance, degrading the total gate capacitance to less than C_{ox} which is shown in Figure 4.5.

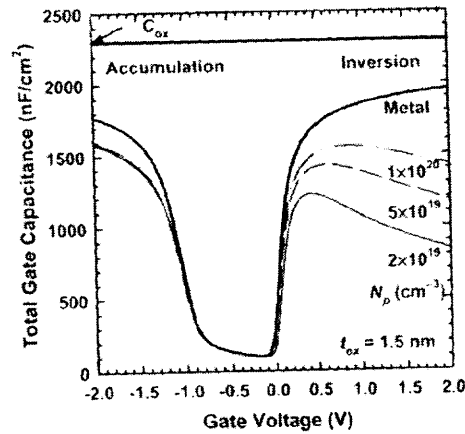


Figure 4.5 Low-frequency C-V plots to extract gate capacitance and EOT [9].

On the positive gate voltage side, otherwise termed as inversion region of the capacitor, one can define capacitance equivalent thickness (CET), in terms of measured capacitance C_{inv} as,

$$CET = \frac{A\epsilon_{ox}}{C_{inv}} \quad (4.1)$$

This CET is dependent on the gate voltage applied since poly-depletion effect worsens at higher gate voltages.

On the negative voltage side, otherwise termed as accumulation, the gate is also accumulated if one uses n+ as polysilicon gate. There is no poly-depletion region and hence the capacitance is insensitive to the poly doping [76]. Generally, the capacitance of the poly-gate for all dopings is slightly lower than metal gate because of the finite width of the accumulation layer on the poly-Si side. Since the accumulation capacitance is insensitive to poly-Si doping as well as to substrate doping, it is used to extract EOT of the MOS device. In other words, EOT is defined as the physical thickness of an oxide film that would reproduce the measured C-V characteristics in accumulation, when

incorporated in the correct model. The capacitance oxide thickness, calculated from the measured accumulation capacitance, allows the determination of EOT from the measured C-V data of a capacitor with known area. It should also be noted that it is very difficult to accurately extract the physical thickness of the gate oxide using the high-resolution transmission electron microscope (HRTEM) cross-sectioning technique. The manipulation of TEM image contrast can easily result in several angstroms of variation. Several novel capacitance and current techniques have also been developed to allow accurate capacitance measurement and thickness determination in 2.0-1.0 nm regimes which by itself is a good research topic for study.

CHAPTER 5

1/F NOISE PERFORMANCE OF ADVANCED HIGH-K GATE STACKS

This chapter discusses about various gate technological and processing parameters that could influence 1/f noise in Hf-based dielectrics. Some of the gate processing and technological parameters that could possibly influence 1/f noise are:

- (1) Interfacial layer (SiO_2) oxide - t_{IL}
 - i) Interfacial oxide thickness
 - ii) Interfacial layer oxide quality
 - iii) Special treatments – Post Deposition Anneal and Nitridation effects.
- (2) High- κ gate dielectric - $t_{\text{high-}\kappa}$
 - i) High- κ oxide thickness
 - ii) κ -value of the layer
- (3) Gate electrode effects
 - i) Poly-Si Vs Fully-Silicided (FUSI) Vs. Metal
 - ii) Metal Gate Electrode processing – ALD Vs PVD processed gates
- (4) Gate Electrode/High- κ interface
- (5) Nature of the channel – Si or Ge

The effects of 1/f noise on these gate technological and processing parameters are discussed in detail in various sections of this Chapter. Apart from these parameters, it is seen that Si-SiO₂ interface is shown to have an effect from earlier studied SiO₂ devices [77] while the influence of interfacial layer/high- κ interface is unknown and considered as a future work.

5.1 Interfacial layer effect

5.1.1. Interfacial layer thickness effects in HfO₂/TaN n-MOSFETs

The 1/f noise performance was investigated in n-MOSFETs with gate width $W=10\mu\text{m}$ and gate length $L=1\mu\text{m}$, with two different IL thicknesses – 0.4 nm and 0.8 nm nitrided SiO₂ IL on top of which HfO₂ was deposited. The EOT of the studied n MOSFETs is 0.92 nm (0.4nm IL and 2.5 nm HfO₂) and 1.44nm (0.8nm IL) respectively. The EOT of the studied p-MOSFETs is 1.31nm (0.4nm IL) and 1.35nm (0.8nm IL) respectively. Deposition of the high- κ oxides was achieved either by Atomic Layer Deposition (ALD) or Metal Organic Chemical Vapor Deposition (MOCVD). Physical Vapor Deposited (PVD) TiN/TaN was employed as metal gate. These devices were annealed in ammonia at 800°C for 60 s. The 1/f noise has been evaluated in MOSFETs biased in linear operation with a drain voltage $|V_{DS}| \leq 50\text{mV}$. The gate leakage was at least one decade lower with respect to the channel current.

Figure 5.1 shows the I_D - V_G and G_M - V_G characteristics of n-MOSFETs. For n-MOSFETs, a higher value of I_D and G_M is observed for lower IL thickness, mainly due to lower EOT values.

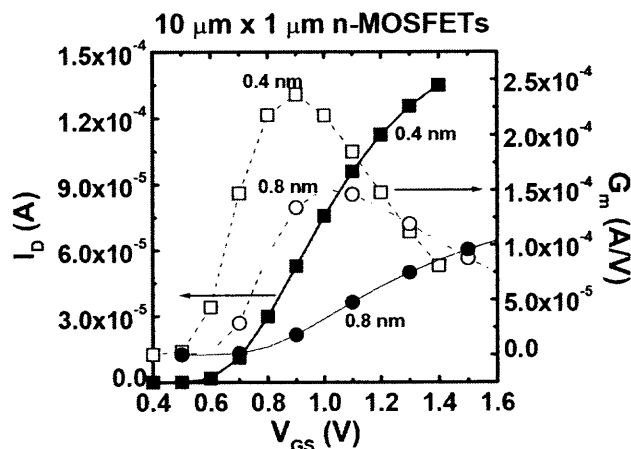


Figure 5.1 Drain current and transconductance vs gate voltage for different IL thickness of n-MOSFET.

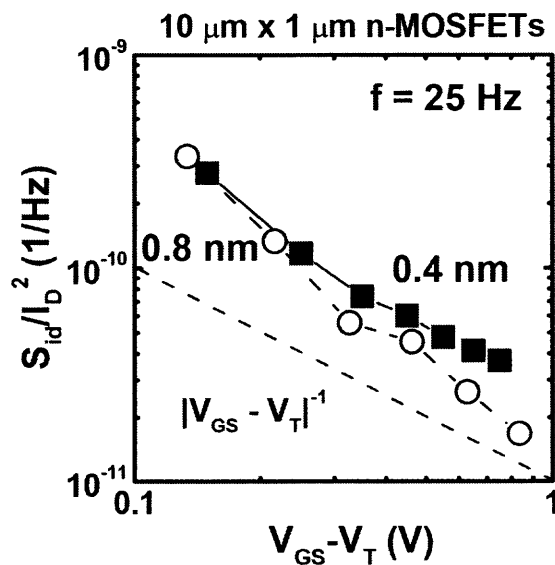


Figure 5.2 Normalized drain current noise spectral density vs gate voltage overdrive for two different IL thicknesses for n-MOSFET.

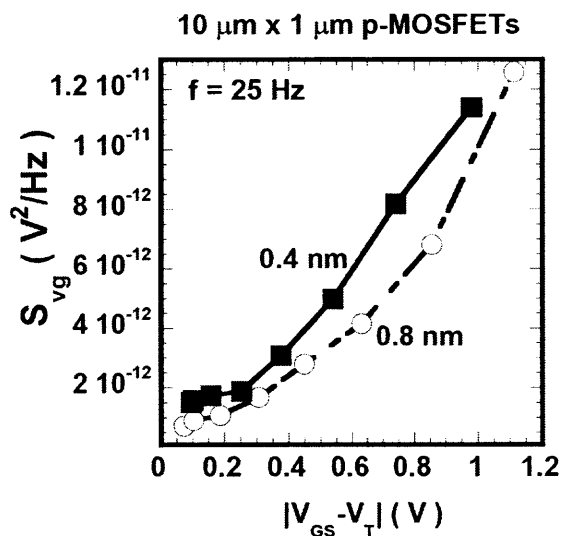


Figure 5.3 Input-referred noise vs gate voltage overdrive for two different IL thicknesses for n-MOSFET.

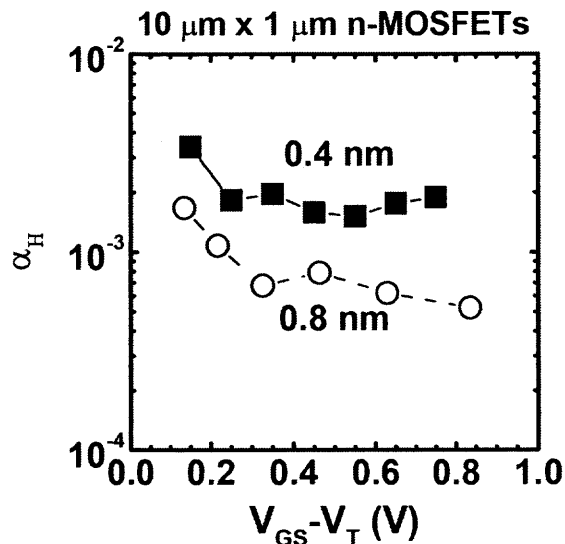


Figure 5.4 Hooge's parameter vs gate voltage overdrive for two different IL thicknesses for n-MOSFET.

Figure 5.2 shows the normalized noise current spectral density S_{iD}/I_D^2 dependence over the gate voltage overdrive $|V_{GS}-V_T|$ at $f=25\text{Hz}$. For n-MOSFETs, the normalized S_{id} varies as $(V_{GS}-V_T)^{-m}$ with $m\sim 1.5$ for the 0.8 nm IL thickness, which highlights that noise is due to correlated number mobility fluctuations, and $m\sim 1$ for 0.4 nm, which points out that noise is mainly due to mobility fluctuations. As shown in Figure 5.3, the input-referred voltage spectral density $S_{vg}=S_{id}/G_M^2$ at $f=25\text{Hz}$ exhibits a pronounced dependence on the gate voltage overdrive for all devices. Higher S_{vg} values are noticed for n-MOSFETs with 0.4 nm IL compared to 0.8 nm. Hooge's parameter as a figure of merit is plotted in Figure 5.4 as a function of gate voltage overdrive.

The higher Hooge's parameter in lower IL thickness devices can be attributed to two different causes: higher C_{ox} values or lower channel mobility. The first cause can be disregarded since the observed α_H increase is significantly higher compared to the

corresponding C_{ox} increase. Thus it is concluded that channel mobility is the cause. The enhanced mobility fluctuations are mainly due to lower mobility values in high- κ gate stacks with lower IL thickness, as reported by other researchers. Increased mobility fluctuations for lower IL thickness can be ascribed to increased Coulomb scattering from charges in the high- κ layer closer to the Si-SiO₂ interface.

5.1.2. Interfacial Layer Thickness Effects in p-MOSFETs

Figure 5.5 shows the I_D - V_G and G_M - V_G characteristics of p-MOSFETs. A slightly higher value of I_D and G_M is observed for higher interfacial thickness, mainly due to lesser differences observed in EOT values. The EOT of 0.8 nm device was 1.35 nm while for 0.4 nm, the value was 1.31 nm.

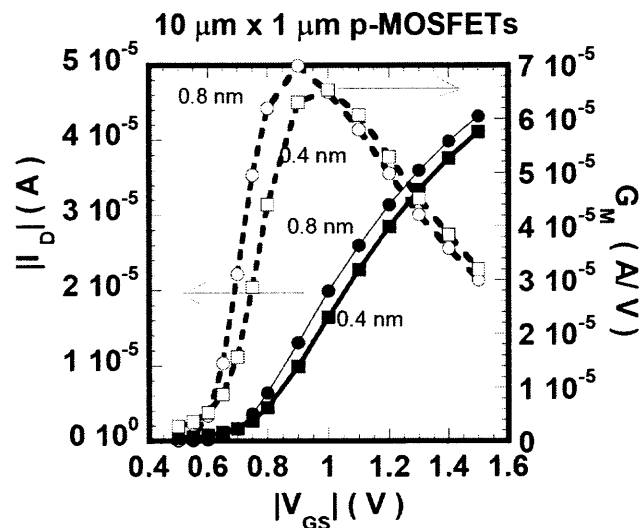


Figure 5.5 Device characteristics of 0.4 nm and 0.8 nm interfacial layer and 2 nm of HfO₂ dielectric oxides at $|V_{DS}| = 0.05$ V.

As seen from Figure 5.6, the normalized LF noise spectra of p-MOSFETs for a $|V_{GS}-V_T|$ of 0.1 V are predominantly of $1/f^\gamma$ type, with $\gamma \sim 1$. Change in S_{ID} is minimal

between 0.4nm and 0.8nm as observed from the noise spectra of p-devices for the same gate voltage overdrive. This is mainly due to the observed similar values of EOT between the devices. For p-MOSFETs, the normalized S_{ID} varies as $|V_G - V_T|^{-1.5}$, which highlights that it is more or less correlated number-mobility model [39, 59], but from normalized noise values with I_D (not shown), the noise mechanism points to Hooge's mobility model [46]. But no significant variation in noise power is noticed among the two different IL devices.

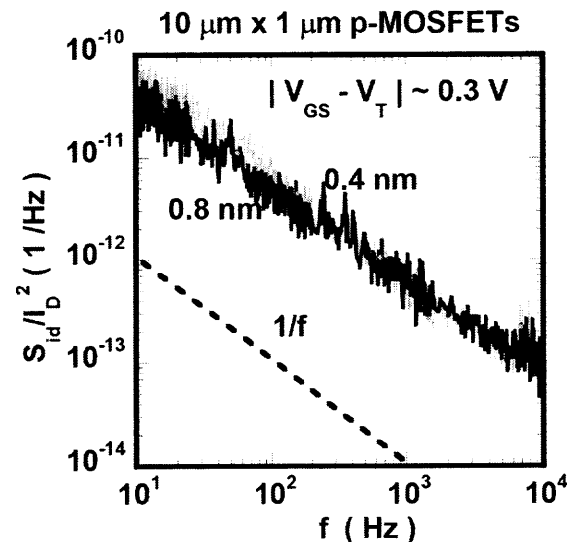


Figure 5.6 Normalized drain current noise spectral density S_{ID}/I_D^2 Vs Frequency f [Hz] for 0.4nm and 0.8nm IL oxides.

As shown in Figure 5.7, the input-referred gate voltage spectral density S_{VG} at $f=25\text{Hz}$ shows a pronounced dependence on the gate voltage overdrive ($V_{GS} - V_T$) for p-MOSFETs. Higher S_{VG} values are noticed for HfO_2 p-channel transistors with 0.4 nm interfacial layer compared to 0.8nm. The contribution is due to both increased S_{ID} and lower G_M as earlier observed. For p-MOSFETs, clearly, S_{VG} dependence on gate voltage

overdrive is observed, further confirming that mobility fluctuations dominate over number fluctuations.

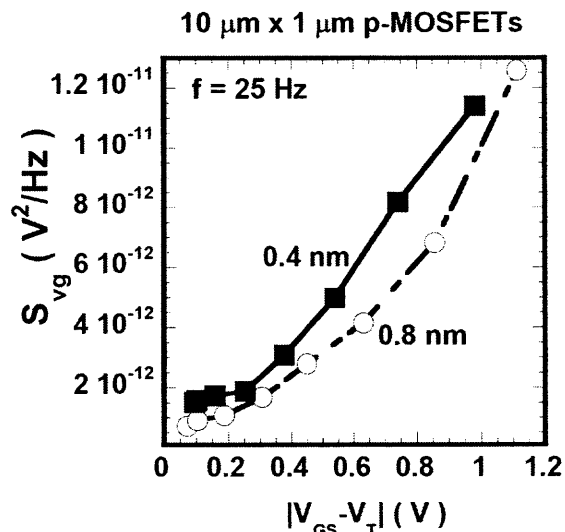


Figure 5.7 Input referred noise spectral density S_{VG} [V^2/Hz] Vs gate voltage overdrive ($V_{GS}-V_T$) [V] for two different IL thicknesses for p-MOSFETs.

Hooge parameter is considered as a figure of merit where the resulting values are plotted in Figure 5.8 as a function of gate voltage overdrive $|V_{GS}-V_T|$. Here, the Hooge's parameter [46] is evaluated using the formula fNS_{ID}/I_D^2 , where N is the number of carriers in the channel approximated by $WLC_{OX}(V_{GS}-V_T)$. A strong dependence is observed with regard to interfacial thickness in p-MOSFETs, where the values are significantly higher for 0.4 nm interfacial layer thickness for $|V_{GS}-V_T| > 0.25V$. The higher Hooge's parameter in lower IL thickness devices can be attributed to two different causes: higher C_{ox} values or lower channel mobility. The first cause can be disregarded since the observed α_H increase is significantly higher compared to the corresponding C_{ox} increase. Thus we conclude that channel mobility is the cause. The enhanced mobility fluctuations are mainly due to lower mobility values in high- κ gate stacks with lower IL

thickness, as reported by other researchers [105]. Increased mobility fluctuations for lower IL thickness can be ascribed to increased Coulomb scattering from charges in the high- κ layer closer to the Si-SiO₂ interface.

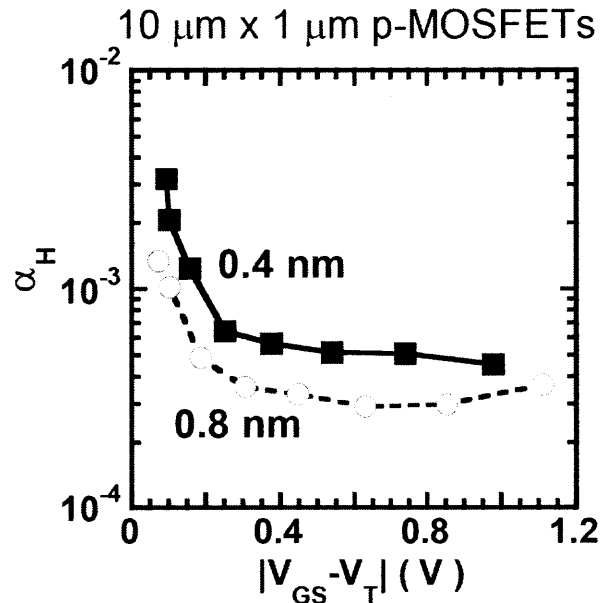


Figure 5.8 Hooge's parameter Vs. Gate Voltage Overdrive ($V_{GS} - V_T$) [V] for two different IL thicknesses for p-MOSFETs.

5.1.3. Interfacial Layer Quality Effects in p-MOSFETs

It is shown here that not only the thickness of the interfacial layer but also the quality of interfacial layers has an influence on 1/f noise. Three different oxides are studied in p-MOSFETs by keeping the interfacial thickness constant as shown in Figure 5.9 (i) First, with an interfacial layer of 0.8nm SiO₂ grown thermally (ii) Second, with an interfacial layer of same thickness whose quality is varied by nitriding the oxide i.e. N₂O (iii) Third, with an interfacial layer of 0.4nm SiO₂ grown by thermal oxidation. The last sample used here is mainly for comparison purposes, though this was discussed in earlier part of the text.

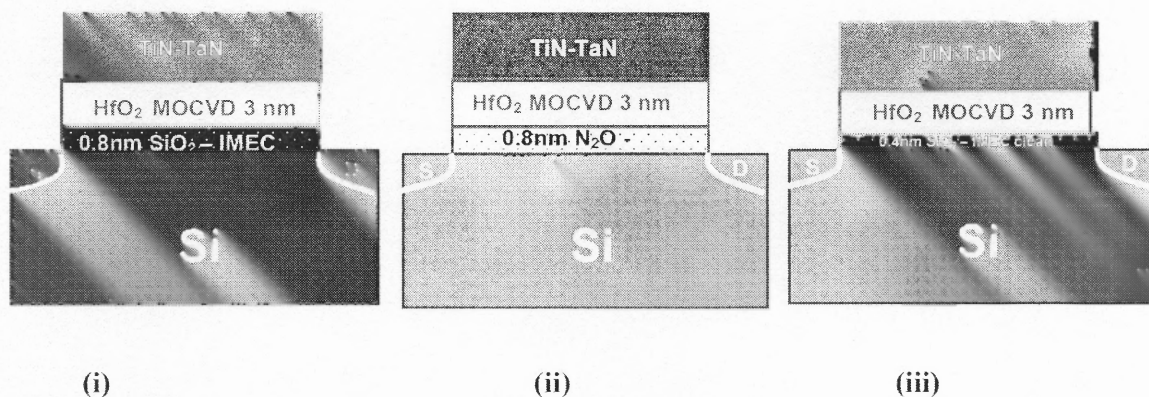


Figure 5.9 Three different interfacial layers studied – 0.8nm thermal SiO₂, 0.8 nm N₂O and 0.4 nm SiO₂.

After observing the drain current spectra to have a $1/f^\gamma$ fit, where $\gamma \sim 1$, the normalized noise and the input referred noise were plotted as a function of gate voltage overdrive as plotted as shown in Figure 5.10 and Figure 5.11, respectively.

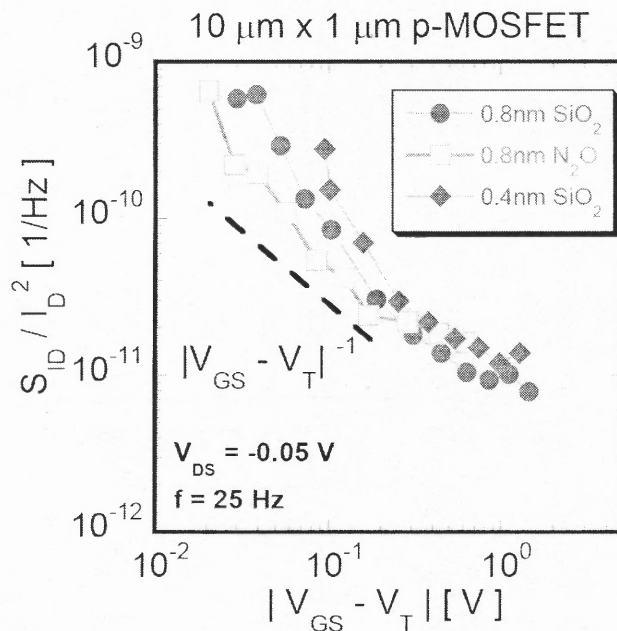


Figure 5.10 Normalized current spectral density versus I_D for a p-MOSFET with 5 nm ALD HfO₂ and of three different interface layers, at $f = 25$ Hz and $|V_{DS}| = 0.05$ V.

Figure 5.10 shows that the device with 0.8nm N_2O as interfacial layer, behaves differently as compared to 0.8nm interfacial layer of thermal SiO_2 . While it is seen that the devices, have a mobility-based behavior on $1/f$ noise, a cross-over type of behavior is observed where the normalized noise power shows lowest noise at lower gate voltages, while it is higher at higher gate voltage overdrives. The trend is confirmed in Figure 5.11 from the input-referred noise values, where the cross-over occurs around 0.2~0.3 V. This cross-over kind of behavior was also earlier observed in pure N_2O stacks [78] as compared to SiO_2 gate stacks. This cross-over behavior is mainly attributed to the increase of bulk traps due to nitridation effects. The nitridation effects of the interfacial layer are further discussed in detail in the forthcoming chapter. The cross-over voltages in such devices were in the range of 2~3 volts while, in this case, it is found to be less than 1 V. Higher noise is also observed for 0.4 nm interfacial layer devices, confirming the earlier observation on interfacial thickness effects on $1/f$ noise.

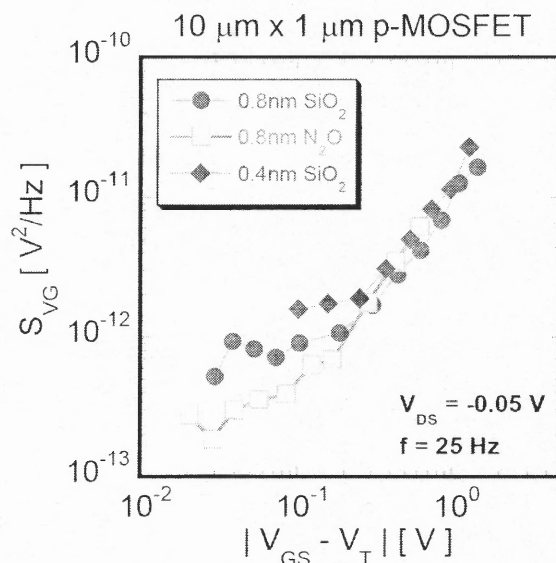


Figure 5.11 Input referred noise spectral density S_{VG} [V²/Hz] Vs gate voltage overdrive $|V_{GS} - V_T|$ [V] for three different IL for p-MOSFETs.

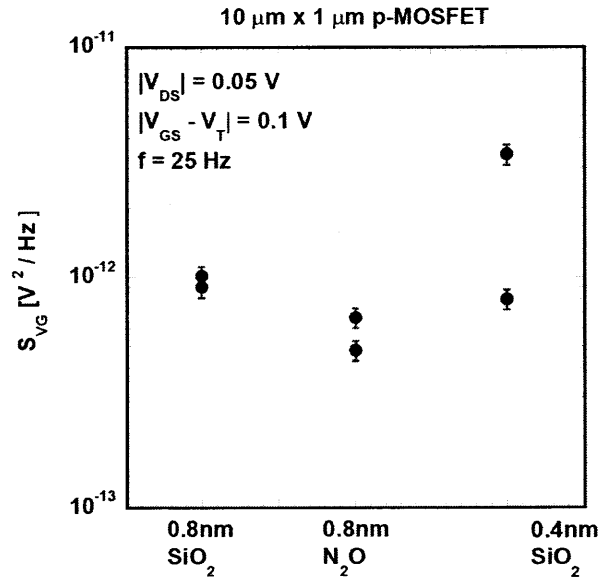


Figure 5.12 Input referred noise spectral density S_{VG} [V^2/Hz] Vs three different IL for p-MOSFETs at $|V_{GS}-V_T| \sim 0.1$ V and $|V_{DS}| \sim 0.05$ V and $f = 25$ Hz.

Figure 5.12 summarizes the results obtained from all the devices by including the device-to-device variation also, where the input-referred noise is found to be 5x less at $|V_{GS}-V_T| \sim 0.1$ V for N_2O devices when compared to thermal SiO_2 for the same interfacial thickness, but apparently increases by at least 2x when $|V_{GS} - V_T| > 0.5$ V due to cross-over behavior.

5.2 Interfacial Layer Treatment – Nitridation Effects

5.2.1 Pre-and Post-deposition Conditions

N- and p-channel MOSFETs of dimensions $W/L=10/1$ (μm) with pure HfO_2 as gate dielectric were fabricated using a CMOS process flow. The main process steps for nitrated and non-nitrated interface are indicated in Table 5.1. On top of a 0.8 nm thin

interfacial chemical oxide (SiO_2), resulting from the use of ozone chemistry, HfO_2 was deposited by MOCVD. Physical Vapor Deposited TiN/TaN metal gate was employed as the gate material. The estimated Equivalent Oxide Thicknesses (EOT) of the studied devices is listed in Table 5.2.

Two types of interfaces are investigated for n-MOSFETs – I) non-nitrided and II) nitrided. For the latter, decoupled plasma nitridation (DPN) was employed. “Soft” nitridation of the interface was done with plasma energy (PE) close to 25 kJ. Following the DPN of the devices, a post nitridation anneal (PNA) was carried out in an O_2 ambient at 800°C for $\sim 15\text{s}$. In this case, the percentage nitrogen involved is $\sim 7\text{-}9\%$, estimated from the XPS measurements [79].

Nitrided-interface n-MOSFETs involved NH_3 , O_2 and no anneal conditions, while non-nitrided-interface devices had no anneal, N_2 and NH_3 anneals. The non-nitrided-interface p-MOSFET devices involved four different post deposition anneals – O_2 , N_2 and NH_3 and a no-anneal condition. All the anneals were performed at 800°C for 60s before the metal gate formation. In the case of no-anneal condition, the metallization process was carried out after gate dielectric deposition. After gate electrode metallization, the wafers were subjected to forming gas anneal (FGA) at 520°C for 20 min.

Table 5.1 CMOS Fabrication Flow Showing Important Process Steps Required for Nitrided and Non-nitrided Interface n-MOSFETs



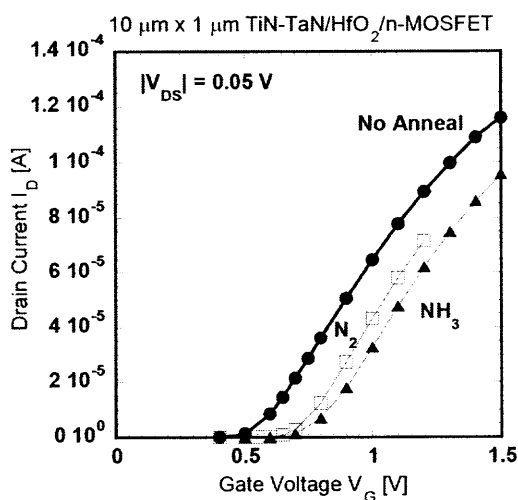
NON-NITRIDED INTERFACE	NITRIDED INTERFACE
 <p>● Chemical oxide growth (0.8nm interfacial layer SiO₂)</p> <p>● HfO₂ Deposition (MOCVD)</p> <p>● PDA 800° C (NH₃ or N₂)</p> <p>● Metallization (PVD – TiN/TaN)</p> <p>● Gate electrode FGA anneal (520°C - H₂ + N₂ ambient – 30 min)</p>	 <p>● Chemical oxide growth (0.8nm interfacial layer SiO₂)</p> <p>● Decoupled Plasma Nitridation (7-9% N₂ incorporated)</p> <p>● Post-nitridation anneal (800° C) in oxygen ambient</p> <p>● HfO₂ Deposition (MOCVD)</p> <p>● PDA 800° C (NH₃, O₂ or N₂)</p> <p>● Metallization (PVD – TiN/TaN)</p> <p>● Gate electrode FGA anneal (520°C - H₂ + N₂ ambient – 30 min)</p>

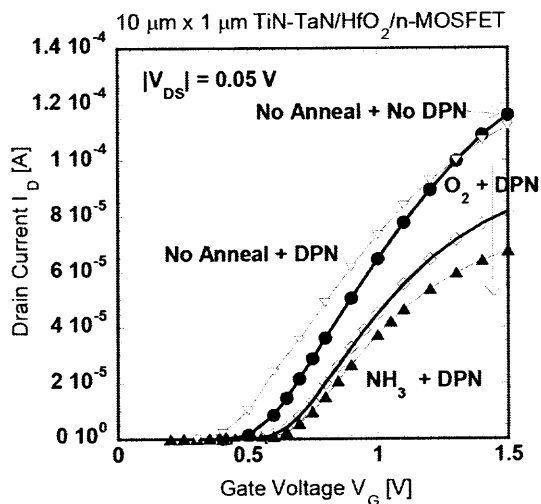
Table 5.2 Device and Noise Parameter Values for the Different Nitrided and Non-nitrided Interface n-MOSFET and p-MOSFET Devices Studied

Sl. No		Anneal Condition	Silicate thickness (nm)	EOT (nm)	S_{ID} f= 25 Hz [A ² /Hz]	$\sqrt{S_{V_{GS}-V_T}}$ ~0.1 V [V/ $\sqrt{\text{Hz}}$]	$WLS_{V_{GS}-V_T}$ ~0.1 V [V ² $\mu\text{m}^2/\text{Hz}$]	Normalized $S_{V_{GS}-V_T}$ ~0.1 V [V ² $\mu\text{m}^2/\text{Hz}$]	N_T [1/cm ³ eV]	D_T [1/cm ²]
1	nMOSFET	No Anneal	2	1.50	1.5e-20	8.5e-07	7.3e-12	125~175	7.3e+18	3.9e+12
2		N ₂	2	1.42	1.4e-20	7.2e-07	5.3e-12	100~150	5.2e+18	2.2e+12
3		NH ₃	2	1.44	1.1e-19	2.4e-06	5.9e-11	900~1500	5.9e+19	7.0e+11
4		DPN NH ₃	2	1.21	6.2e-20	1.9e-06	3.6e-11	850~900	3.6e+19	1.5e+12
5		DPN O ₂	2	1.24	3.8e-20	1.6e-06	2.6e-11	850~900	2.6e+19	1.1e+12
6		DPN No Anneal	2	1.25	8.8e-20	2.3e-06	5.4e-11	950~1050	5.5e+19	2.3e+12
7	pMOSFET	No Anneal	2	1.34	2.14e-21	6.42e-07	4.12e-12	95~105	-	-
8		NH ₃	2	1.34	4.38e-21	9.31e-07	8.66e-12	200~225	-	-
9		O ₂	2	1.39	3.25e-21	8.13e-07	6.61e-12	150~175	-	-
10		N ₂	2	1.39	3.00e-21	9.20e-07	8.47e-12	200~225	-	-

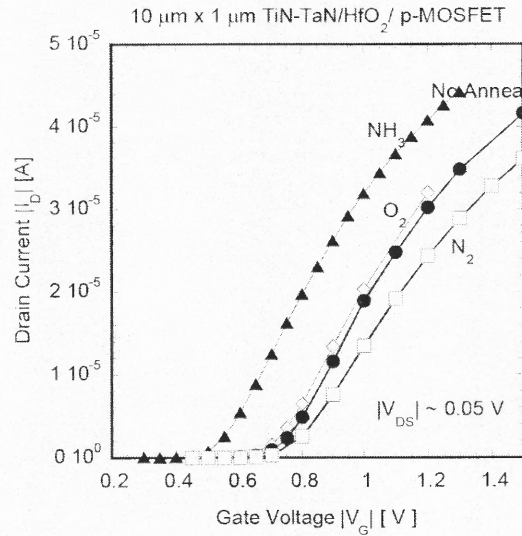
Figure 5.13(a),(b),(c) shows the device characteristics of non-nitrided and nitrided interface n-MOSFETs and non-nitrided interface p-MOSFETs respectively for various post-deposition anneals studied. Devices with no-anneal condition have the highest drive current with lower threshold voltage V_T shifts compared to other PDA conditions for n-MOSFETs while NH_3 has the highest drive current for p-MOSFETs. Also inferred from Figure 5.13(b) that post-deposition anneals (O_2 , NH_3) in devices with nitrided interface reduces the saturation drive current I_D .



(a)



(b)



(c)

Figure 5.13 Device transfer characteristics I_D - V_G for (a) non-nitrided interface and (b) for nitrided interface devices, with different post deposition anneals for n-MOSFETs (c) for non-nitrided interface devices, with different post deposition anneals for p-MOSFETs.

5.2.2 Non-nitrided Interface and Post-deposition Anneals in n-MOSFETs

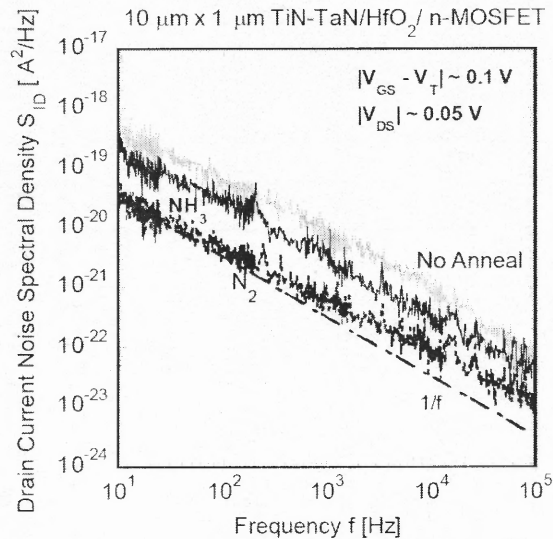


Figure 5.14 Drain Current Noise Spectral Density S_{ID} [A^2/Hz] Vs Frequency f [Hz] for HfO_2 devices with different (PDA) post deposition anneals for n-MOSFETs.

Figure 5.14 shows the low frequency noise spectra at $|V_{DS}|$ of 0.05V and a gate voltage overdrive of $|V_G - V_T|$ of ~ 0.1 V for various post-deposition anneals of the HfO_2 gate dielectric. Predominantly $1/f$ like spectra are obtained with the frequency exponent γ in the range $0.9 \sim 1.05$. Differences exist in the drain current spectra where N_2 anneals have the lowest noise spectral densities. Devices annealed with NH_3 show higher noise values, which are comparable with no anneal spectra.

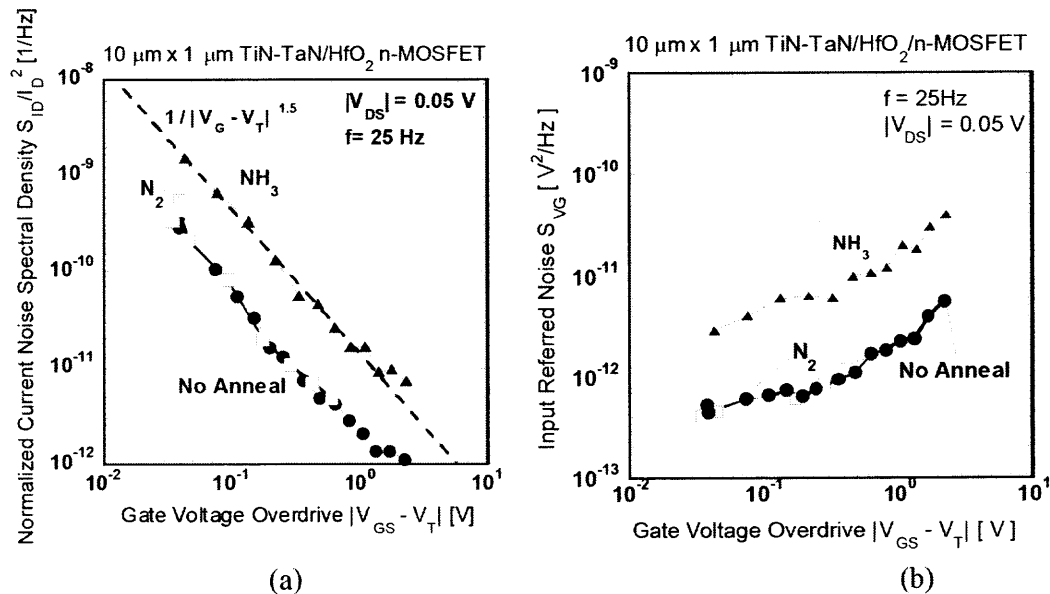


Figure 5.15 (a) Normalized Drain Current Noise Spectral Density S_{ID}/I_D^2 [1/Hz] Vs Gate Voltage Overdrive $|V_{GS} - V_T|$ [V] for non-nitrided interface devices with different post deposition anneals for n-MOSFETs. Figure 5.15(b) Input-referred noise S_{VG} [V^2/Hz] Vs Gate Voltage Overdrive $|V_{GS} - V_T|$ [V] for non-nitrided interface devices with different post deposition anneals for n-MOSFETs.

The corresponding normalized noise current spectral density S_{ID}/I_D^2 is represented in Figure 5.15a versus the gate voltage overdrive $|V_{GS} - V_T|$ for $f = 25$ Hz and $|V_{DS}| = 0.05$ V. Clearly, for all anneal conditions the normalized noise reduces as the gate voltage

overdrive increases. For any given $|V_{GS}-V_T|$, NH_3 annealed devices show the highest values, which are typically one order of magnitude higher when compared with N_2 or no anneal devices. Irrespective of the anneal conditions, the S_{ID}/I_D^2 dependence on $|V_{GS}-V_T|$ is found to be approximately 1.5. This suggests that the $1/f$ noise in these devices can be described in the frame of the theory of correlated number fluctuations [39, 59], based on carrier trapping/detrapping and scattering in the dielectric.

As shown in Figure 5.15(b), the input gate-referred voltage spectral density ($S_{VG} = S_{ID}/g_m^2$) at $f = 25\text{Hz}$ versus the gate voltage overdrive $|V_{GS}-V_T|$ is seen to be dependent on the type of post-deposition anneal. As can be observed for all $|V_{GS}-V_T|$, lower values of S_{VG} are noted for N_2 and no anneal conditions while higher values up to an order of magnitude are noticed for NH_3 anneal conditions, in conformity to the results observed in Figure 5.15(a).

5.2.3 Nitrided Interface and Post-deposition Anneals in n-MOSFETs

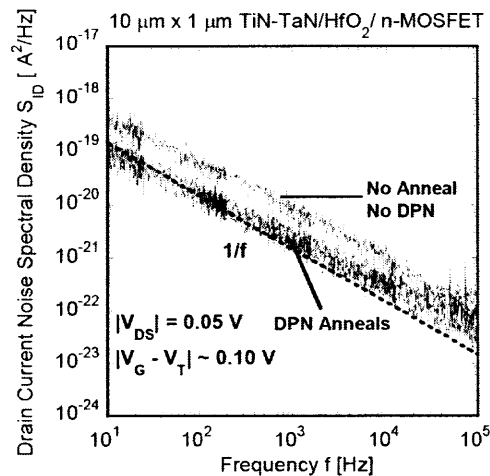


Figure 5.16 Drain Current Noise Spectral Density S_{ID} [A²/Hz] Vs Frequency f [Hz] for nitrided interface devices with different post deposition anneals for n-MOSFETs.

Figure 5.16 shows the low frequency noise spectra at $|V_{DS}|$ of 0.05V and a gate voltage overdrive of $|V_{GS} - V_T|$ of 0.1V for various post-deposition anneals of an HfO_2 gate dielectric on a nitrated interfacial layer. Unlike for the non-nitrated interface case shown in Figure 5.14, no differences were observed in the drain spectra where N_2 and NH_3 post-deposition anneals have almost similar noise spectral densities. Even devices with no post deposition annealing and nitrated interface have similar values as compared to various post-anneals, while the no anneal and no DPN condition has higher drain current noise values.

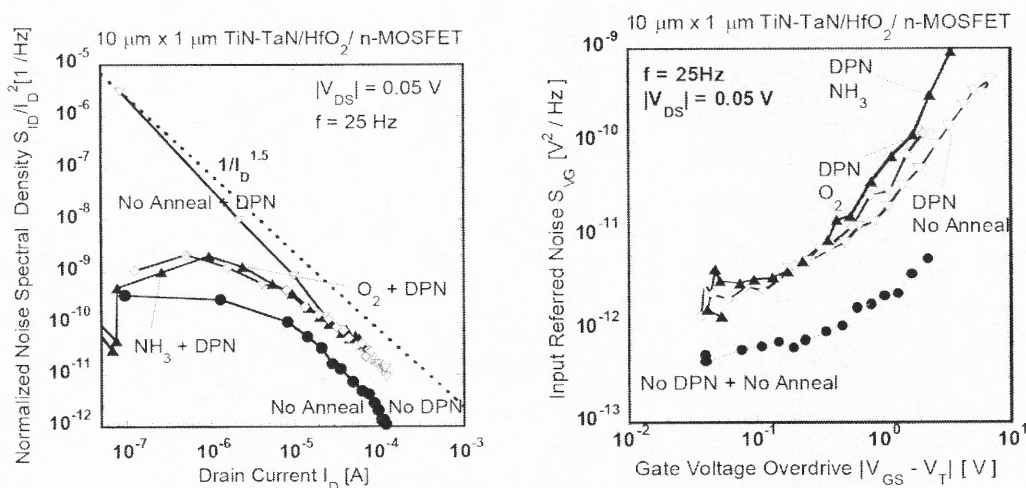


Figure 5.17 (a) Normalized Drain Current Noise Spectral Density S_{ID}/I_D^2 [1/Hz] Vs Drain Current I_D [A] for nitrated interface devices with different post deposition anneals for n-MOSFETs. Figure 5.17(b) Input-referred noise S_{VG} [V^2/Hz] Vs Gate Voltage Overdrive $|V_{GS} - V_T|$ [V] for non-nitrated interface devices with different post deposition anneals for n-MOSFETs.

Figure 5.17a shows the corresponding normalized noise current spectral density S_{ID}/I_D^2 against the drain current I_D for $f = 25\text{Hz}$ and $|V_{DS}| = 0.05\text{V}$. Except for nitrated interface and no anneal case, a clear plateau of normalized noise at lower drain currents and a roll-off at higher frequencies is observed, suggesting that the noise mechanism is

due to number fluctuations. But for only nitrated interface and no post-deposition anneal, the noise mechanism follows $1/I_D^{1.5}$ suggesting that the noise mechanism involves additional scattering-related effects [39, 59] also.

Figure 5.17b shows the input-referred noise S_{VG} plotted against the gate voltage overdrive $|V_G - V_T|$ for various interface-nitrated and post-deposition anneal conditions.

While similar S_{VG} values and similar profiles are noticed for various post-anneal conditions, an order of magnitude difference exists for the non-nitrated and no-anneal condition.

From the above results, it is clear that I) Nitridation of the interfacial oxide has an impact both on the noise spectra and the noise mechanism in these devices II) Nitridation of the interface suppresses the effect of the post-deposition anneal III) Interface nitridation with no anneal has a different noise behavior when compared to nitrated interface and post-deposition anneal conditions.

5.2.4 Non-nitrated Interface and Post-deposition Anneals on p-MOSFETs

Figure 5.18 shows the low frequency noise spectra at $|V_{DS}|$ of 0.05V and a gate voltage overdrive of $|V_G - V_T|$ of $\sim 0.1V$ for various post-deposition anneals of the HfO_2 gate dielectric in p-MOSFETs. Unlike n-MOSFETs, drain current spectra values are found to be similar for all post-deposition anneals. The corresponding normalized noise current spectral density S_{ID}/I_D^2 is represented in Figure 5.19a versus the gate voltage overdrive $|V_{GS} - V_T|$ for $f = 25$ Hz and $|V_{DS}| = 0.05$ V.

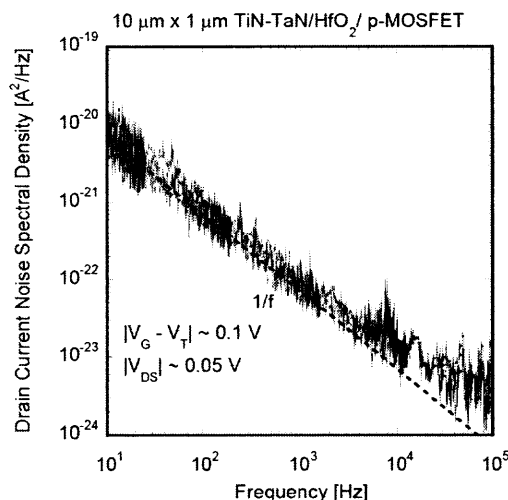


Figure 5.18 Drain Current Noise Spectral Density S_{ID} [A^2/Hz] Vs Frequency f [Hz] for non-nitrided interface devices with different post deposition anneals for p-MOSFETs.

Except for a no-anneal condition, the normalized noise S_{ID}/I_D^2 is inversely proportional to $|V_G - V_T|$ and hence these devices are explained in the frame of mobility fluctuation theory, which confirm the earlier observation on p-MOSFET devices with metal gates. As shown in Figure 5.19b, the input gate-referred voltage spectral density ($S_{VG} = S_{ID}/g_m^2$) at $f = 25\text{Hz}$ versus the gate voltage overdrive $|V_{GS} - V_T|$ is seen to have a similar profile for all the PDA conditions. The values are found to be higher for a NH_3 anneal condition while it is lower for a no-anneal condition similar to an n-MOSFET case. The S_{VG} variation with gate voltage overdrive is also seen to be different than any of the n-MOSFET cases studied, where lower dependency on $|V_{GS} - V_T|$ is noted.

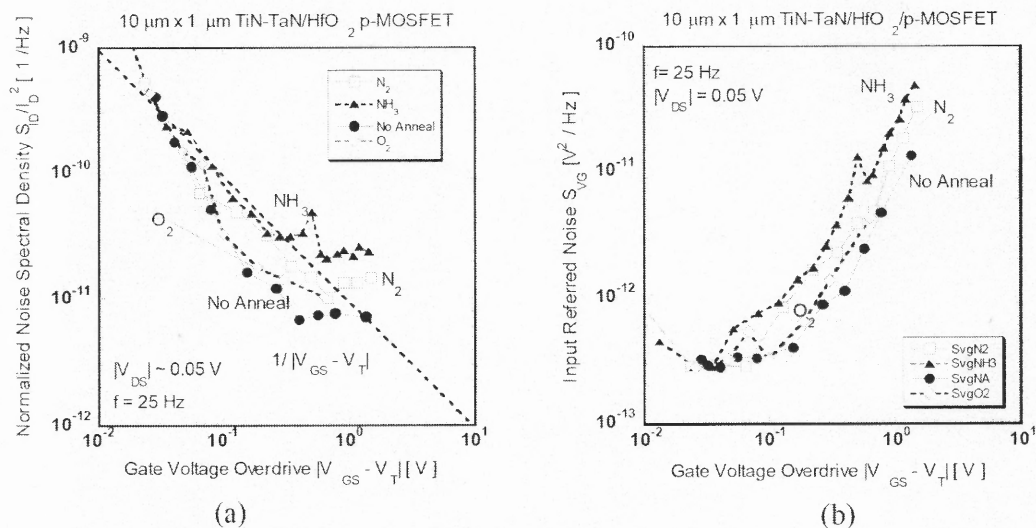


Figure 5.19 (a) Normalized Drain Current Noise Spectral Density S_{ID}/I_D^2 [1/Hz] Vs Gate Voltage Overdrive $|V_{GS} - V_T|$ [V] for non-nitrided interface devices with different post deposition anneals for p-MOSFETs. Figure 5.19b: Input-referred noise S_{VG} [V²/Hz] Vs Gate Voltage Overdrive $|V_{GS} - V_T|$ [V] for non-nitrided interface devices with different post deposition anneals for p-MOSFETs.

5.2.5 Trap Profile Behavior of Nitrided and Non-nitrided Interface n-MOSFETs

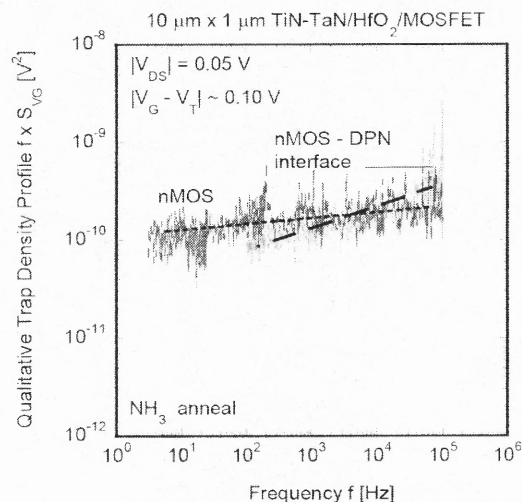


Figure 5.20 $f \times$ Input-referred noise S_{VG} [V²/Hz] Vs Frequency f [Hz] for devices with (a) non-nitrided interface n-MOSFET and (b) nitrided interface n-MOSFET for NH₃ case.

Figure 5.20 compares the qualitative trap density profiles obtained by plotting the product of frequency f and input-referred gate noise spectra ($f \times S_{VG}$) versus the frequency for a non-nitrided and a nitrided-interface n-MOSFET and a NH_3 anneal condition. The frequency axis can also be interpreted in terms of the tunneling depth from the Si substrate based on the equation [80]

$$\frac{1}{2\pi f} = \tau_0 e^{\alpha_t z} \quad (5.1)$$

with τ_0 the time constant at the interface (10^{-10} s) and α_t is the attenuation coefficient, z is the tunneling depth .

Based on this interpretation, trap density profile differences between nitrided-interface and non-nitrided-interface devices are observed for n-type high- κ MOSFETs with NH_3 post-deposition annealing. It is almost constant with depth throughout the high- κ and the interfacial layer for non-nitrided-interface devices, while for a nitrided-interface, an increasing trap density profile is observed around the interfacial layer, at high frequencies. This shows that the nitridation of the interface may have an additional impact on the stoichiometry of interfacial layer by creating a high density of N-related noisy traps close to the Si-SiO₂ interface [81-83].

5.2.6 Nitrogen Induced Oxygen Defect Centers

Depending on the ambient during PDA and the use of DPN, it is clear that different amounts (and profiles) of nitrogen will be introduced in the gate stack, which may influence the density and profiles of the N- and oxygen-vacancy-related traps. These concentration profiles are also quite important to determine the impact on 1/f noise. It has been recently established that the nitrogen related defects have a strong correlation with

the oxygen vacancies and interstitials induced in high- κ devices [14],[84-93]. In the case of nitrided-interface and non-nitrided-interface conditions, involving N_2 and NH_3 , different nitrogen-defect mechanisms seem to exist.

It is widely believed that ‘molecular’ N_2 is involved in the case of N_2 anneal condition in n-MOSFETs [93], which is observed to have a minimal effect on the oxygen vacancies. This would mean that N_2 is ineffective in inhibiting the oxygen transport into the oxide. It is always possible that the mobile oxygen can diffuse in the interfacial layer (SiO_2), since oxygen has a higher affinity for Si than Hf, as the Gibbs free energy for the chemical reaction with SiO_2 is lower [94].

In the case of interfaces involving plasma nitridation (DPN), ‘atomic’ N is involved in n-MOSFETs [93] where atomic nitrogen can react with oxygen unlike the earlier case. Due to this reaction, the total number of oxygen vacancies would be lower. In that case, lesser mobile oxygen is involved in transport. The role of this atomic nitrogen is also believed to passivate the Si- SiO_2 (substrate-interfacial layer) interface. It is possible that this interface passivation can suppress the effect of post deposition anneals, which may explain similar values of $1/f$ noise observed in plasma nitrided interface devices.

Since the mobile oxygen involved is higher in non-nitrided-interfaces, it is possible that this oxygen can diffuse in the SiO_2 interfacial region, which increases the possibility of regrowth of the interfacial layer. Due to this regrowth, the thickness of the interfacial layer may increase, as is confirmed by the corresponding higher EOT values in Table 5.2. The increase in interfacial layer thickness yields a reduced $1/f$ noise [1], which is in line with the observation of a lower $1/f$ noise in the case of non-nitrided N_2 anneal

when compared to nitrided anneal conditions where nitrogen (DPN) is involved as shown in Table 5.2.

But in the case of NH_3 anneal condition, two different species are believed to be involved [93] - $\text{NH}_2^{+/}$ and a proton (H^+). The likelihood that the proton (H^+) can bond to O is seen to be lower and hence there is charge build up due to the generation of protons and, hence, more electron trapping related events can occur. As additional trapping may be involved, higher $1/f$ noise is observed in these devices.

Relating the above discussions of (I) trap profiles and (II) nitrogen-defect induced oxygen transport, it looks like that the binding configuration between various atoms seem to play an important role, which can explain further the differences observed between plasma nitrided and non-plasma nitrided devices and its relationship to the observed differences in the trap density profile behavior. In the case of decoupled plasma nitrided (DPN) devices, it is possible that Si is mostly bonded to O and Hf has a preferential bonding to O, while few Hf-N bonds may exist at the high- κ /IL interface, leaving a lower number of oxygen vacancies. Hence more Si-O-N and Hf-O bonds exist at the high- κ /IL interface, giving rise to an increasing trap concentration in the vicinity of the interfacial layer of the gate stack.

With respect to the results for the p-MOSFETs, no conclusions can be drawn on a possible effect of N on the local trap density profile from the $1/f$ noise results. This is due to the fact that the fluctuation mechanism is related to scattering and not to trapping. Apparently, a PDA has a small effect (if any) on the scattering centers in the gate dielectric of p-channel devices, which may be different than the trapping centers responsible for the $1/f$ noise in n-MOSFETs.

5.2.7 Trap Density Estimation

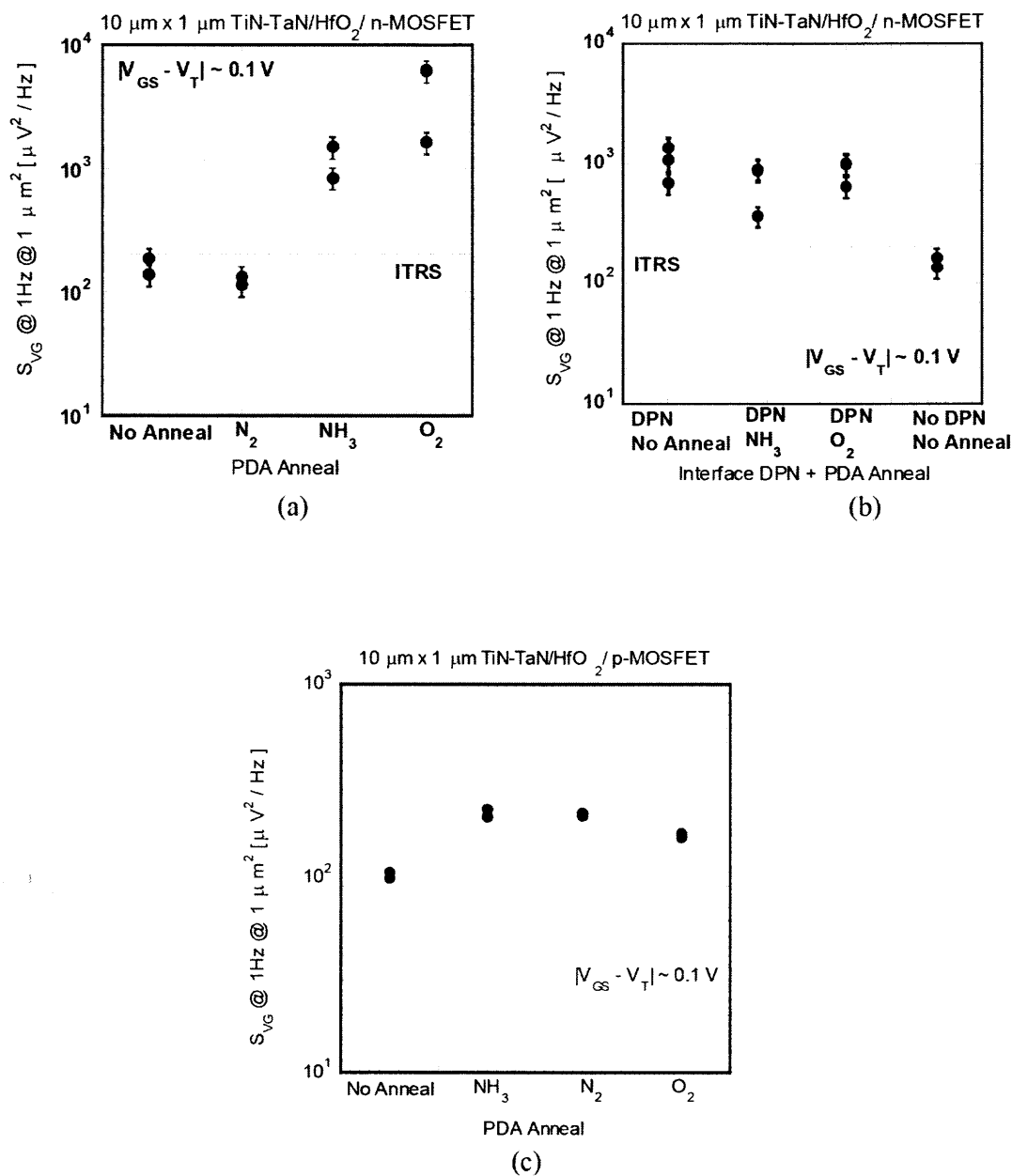


Figure 5.21 Input-referred noise S_{VG} [V^2/Hz] at $|V_{GS} - V_T| \sim 0.1\ \text{V}$ and $V_{DS} \sim 0.05\ \text{V}$ Vs various PDA anneals for (a) non-nitrided interface n-MOSFET (b) interface nitrided n-MOSFET devices (c) non-nitrided interface p-MOSFET with different post deposition anneals.

Figure 5.21 a, b, c show normalized input referred noise S_{VG} for $|V_{GS} - V_T| \sim 0.1$ V and $V_{DS} \sim 0.05$ V for different non-nitrided interface post deposition anneals for n-MOSFET and p-MOSFETs and for various interface nitrided devices with different post deposition anneals for n-MOSFET. The ITRS [7] specification of $200 \mu V^2/Hz$ for a MOSFET RF device is also shown as a dotted line in the figures. While the no anneal condition has a lower value (~ 150) close to ITRS specs, differences due to post-deposition anneals are noticed when the interface is non-nitrided. NH_3 (~ 1150) and O_2 (~ 3000) anneal show noise values higher by an order of magnitude when compared to other PDA conditions. In the case of nitrided interface devices, the effect of post-deposition anneal is suppressed as explained earlier due to which a similar value of S_{VG} is noticed for all the PDA conditions (~ 900). In p-MOSFET case, the effect of PDA anneal is not seen as the values are found to be more or less similar (~ 200).

From the values of S_{VG} , an effective volume trap density N_T can be estimated for n-MOSFETs using the formula [55],

$$S_{VFB} = q^2 k T N_T / (W L C_{EOT}^2 \alpha_t f) \quad (5.2)$$

where kT is the thermal energy, q is the electron charge and the oxide capacitance density $C_{EOT} = \epsilon_{ox} / EOT$ with ϵ_{ox} the permittivity of SiO_2 . The tunneling parameter α_t is estimated semi-empirically from the expected values of the effective tunneling mass of the electron (m_e^*) in the dielectric and the potential barrier for electron emission at the silicon-oxide interface (ϕ_b) using the formula [80]

$$\alpha_t = \text{sqrt} \left((2m_e^* \phi_b) / \hbar^2 \right) \quad (5.3)$$

where \hbar is Planck's constant divided by 2π .

The surface trap density, calculated from N_T , is estimated using the formula $4kTzN_T$, where z is the tunneling distance of the electron from the Si/high- κ interface at $f = 25\text{Hz}$. The traps may be considered as border traps [95] located near the substrate-dielectric interface.

For non-nitrided n-MOSFETs, N_2 PDA shows the lowest volume (N_T) and surface trap densities (D_T) indicating its beneficial effect, while NH_3 PDA has the highest trap values. On the other hand the nitrided interface devices, the trap values are found to be almost similar in the range of $3\sim 5 \times 10^{19} \text{ 1/cm}^3\text{eV}$ for N_T and $1\sim 2 \times 10^{12} \text{ 1/cm}^2$ for D_T .

5.3 High- κ Layer Effects

5.3.1 High- κ Oxide Thickness

Figure 5.22 shows the drain current spectra S_{id} for a high- κ layer thickness of 1, 2 and 3 nm respectively. The high- κ layer is a 70% Hf-silicate gate dielectric. The interfacial layer is $\sim 0.8\text{nm}$ for all the cases. The increase in $1/f$ noise with decrease in high- κ dielectric layer thickness is found to be marginal as the variations in CET due to studied high- κ layers are negligible. Figure 5.23 shows the normalized noise spectral density S_{ID}/I_D^2 for various gate voltage overdrives ($V_{GS} - V_T$) for metal gate n-MOSFETs. The normalized noise should be either proportional to $|V_{GS}-V_T|^2$ if number fluctuations are the dominant mechanism [96], or $|V_{GS}-V_T|$ if mobility fluctuations exist [96]. But, clearly in this case, it is seen that the normalized noise is proportional to a factor of 1.5, which is in between these two values. This shows that the dominant mechanism may be closely related to the correlated number and mobility fluctuations ($\Delta N-\Delta\mu$) theory.

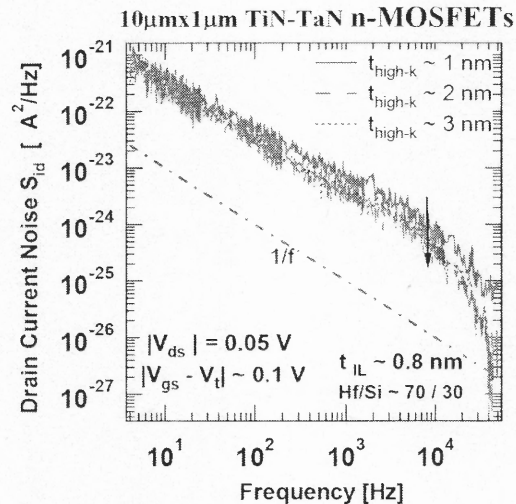


Figure 5.22 Drain current spectral density S_{id} versus Frequency f for n-channel devices with various high- κ layer thicknesses. The interfacial layer (IL) oxide is SiO_2 and has a thickness of ~ 0.8 nm.

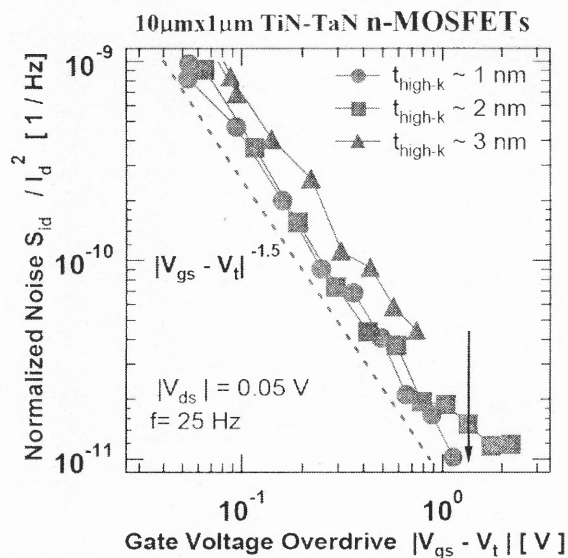


Figure 5.23 Normalized noise spectral density S_{ID} versus gate voltage overdrive ($V_{GS} - V_T$) for n-channel devices with various high- κ layer thickness. The interfacial layer (IL) oxide is SiO_2 and has a thickness of ~ 0.8 nm.

The normalized noise values increase as the high- κ dielectric thickness reduces for all studied gate voltage overdrives, but this variation is only found to be marginal and does not exactly support the theory [96]. A similar behavior was found in p-MOSFETs.

5.3.2 κ Value Effects

Figure 5.24a and b shows the plot of normalized input referred gate voltage noise S_{VG} versus % κ -value of dielectric for poly-Si n- and p-MOSFET devices at $|V_{DS}|$ of 0.05 V and $|V_{GS}-V_T|$ of 0.1 V, and 0.5 V. It is seen that n-MOSFETs have on the average lower S_{VG} values than p-MOSFETs, for Hf-silicate devices where the κ -value varies from 4 to 22. Both 0% Hf where the κ -value is 4~5 and HfO₂ where the κ -value is 20~22 provide an interesting case, where these values possibly show that p-MOSFET devices have higher noise for $|V_{GS}-V_T|$ of 0.1 V but lower noise at $|V_{GS}-V_T|$ of 0.5 V. The device-to-device variation is also seen to be higher in devices with κ -value of 20~22 [HfO₂-100% Hf] and this makes the interpretation difficult to make any conclusion. This device-to-device variation observed for HfO₂ may possibly correlate to material quality of dielectric, where HfO₂ is considered to be inferior when compared to Hf-silicates or SiON devices.

From the overall observation after considering the device-to-device variation and various bias points, it is possible to infer that a weaker to no-dependence of S_{VG} may be observed for κ -values from ~6 to ~18 for both n- and p-MOSFETs. This is seen to be much weaker than reported in literature [97]. As reported previously, it is concluded here that the κ -value has weak to no impact on the noise, for the type of processing used here.

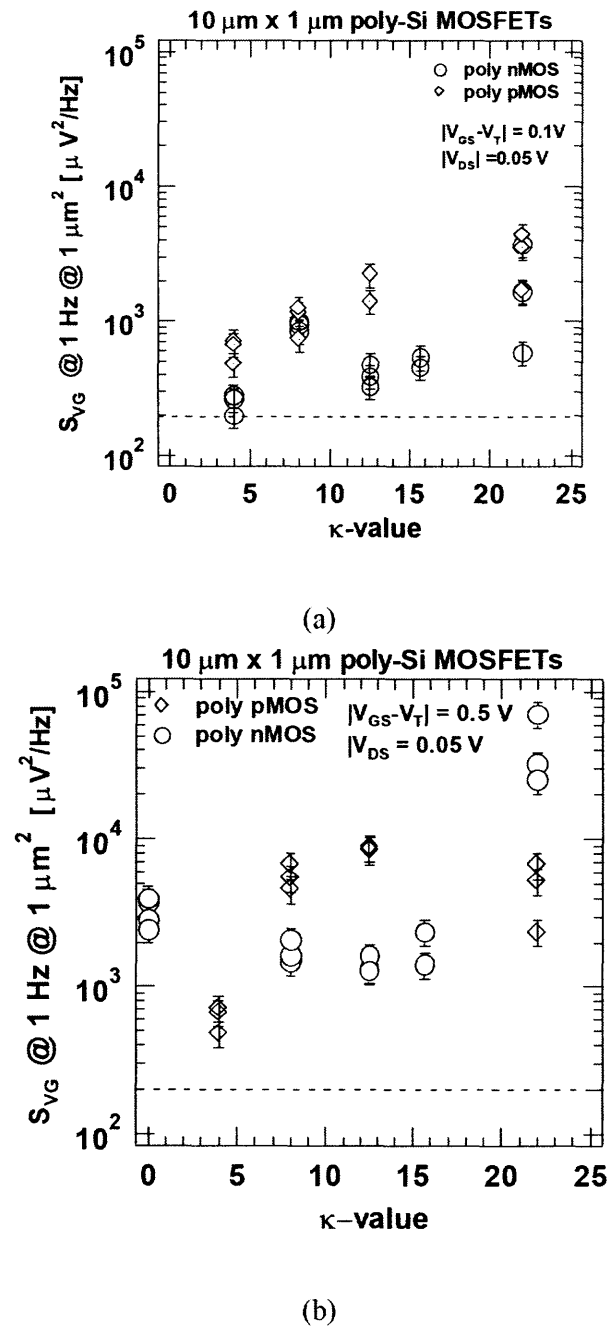


Figure 5.24 Normalized input referred gate voltage noise S_{VG} vs κ -value of dielectric for poly-Si n- and p-MOSFET devices at $|V_{DS}|$ of 0.05V and $|V_{GS}-V_T|$ of a) 0.1V and b) 0.5V.

5.4 Gate Electrode Effects

5.4.1 Gate Electrode Material in p-MOSFETs – Poly-Si/FUSI/TiN-TaN

The noise investigations are performed for devices with three different gate electrode materials: poly-Si, metal (TiN-TaN) and Fully Ni Silicide (FUSI). These electrode materials enable a tuning of the work function, while the poly-Si allows taking into consideration the Fermi-level pinning [98] at the gate electrode-dielectric interface.

P-channel MOSFETs fabricated using a conventional CMOS process flow, with SiON (2.0 nm), pure HfO₂ and with various SiO₂/HfO₂ ratios classified as I) Silicon-rich (higher percentage of SiO₂), II) Hafnium-rich (higher percentage of HfO₂) and III) Equal amount of hafnium-silicon were considered as gate dielectric to study the trap profiles in W/L=10/1 (μm) devices. A Metal Organic Chemical Vapor Deposition (MOCVD) process was used to deposit the gate dielectrics. A 0.8 nm thin interfacial chemical oxide layer (IMEC clean) based on ozone chemistry was employed in all these devices prior to the high-κ gate dielectric deposition.

Three different gate electrode materials were considered to study the effects related to the gate electrode-dielectric interface: N-doped polysilicon (poly-Si) using phosphorus as the dopant material, TiN-TaN (metal) and Fully NiSi (FUSI) gates. In the case of metal gates, TaN was the metal gate electrode while TiN acts as the capping layer – both deposited by Physical Vapor Deposition (PVD). To study the effects of the composition of the underlying high-κ dielectric layer on the gate dielectric-electrode interface, the percentage of Hf was varied from 0% to 53% and 65% in the FUSI gate devices.

The physical thicknesses of the various high- κ dielectrics for p-MOSFETs and the estimated EOT of all devices studied are given in Table 5.4. They all received a post-deposition anneal in NH_3 at 800°C for 60 s before gate electrode deposition. A Forming Gas Anneal (FGA) at 520°C for 20 min was employed once the gate electrodes were formed. Dopant activation anneal was performed at 1000°C and < 1 sec.

Table 5.4 Estimated EOT Values, Physical Thickness and Tunneling Depths of the Devices Studied for Comparison of Gate Electrodes with Dielectrics of Various Composition

SI	Gate	Gate Dielectric	Physical Thickness (+/- 0.1 nm)	EOT (+/- 0.1 nm)	Estimated Tunneling depths z (nm)
1	Poly	SiON	1.5	~1.60	2.01
		23% Hf	2.8	1.75	2.10
		47% Hf	2.8	1.47	2.35
		HfO_2	~ 2.8	1.90	2.60
2	Metal (TiN-TaN)	30% Hf	2.8	1.39	2.15
		55% Hf	2.8	1.46	2.34
		70% Hf	2.8	1.65	2.45
		HfO_2	2.8	1.39	2.60
3	FUSI (NiSi)	SiON	2.2	1.80	2.01
		53% Hf	3	1.35	2.30
		65% Hf	3	1.18	2.43

Figure 5.25 shows the I_D - V_G and G_M - V_G characteristics of TiN-TaN (metal), poly-Si, NiSi (FUSI) gate electrodes of ~55% Hf-silicate gate dielectric oxides. A higher V_T shift and lower G_M is observed for poly-Si MOSFETs while metal and FUSI performances are quite comparable, which is mainly attributed to a work-function shift of the gate electrode material.

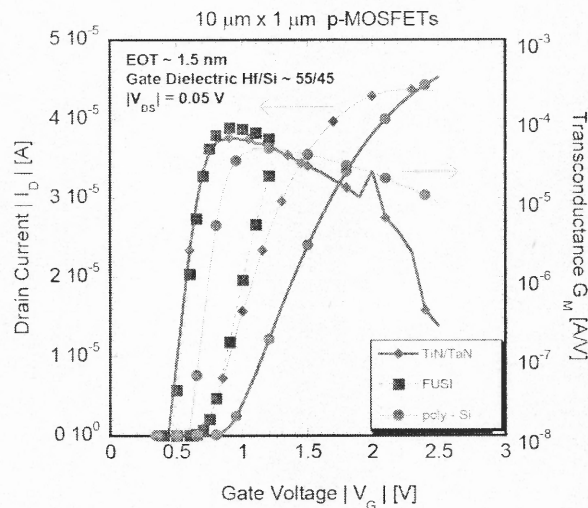


Figure 5.25 Drain Current $|I_D|$ [A] Vs Gate Voltage $|V_G|$ [V] and transconductance G_M Vs gate voltage $|V_G|$ [V] characteristics of TiN-TaN, FUSI and poly-Si gate p-MOSFETs for 55% Hf-silicate gate oxides.

Figures 5.26, 5.27 and 5.28 represent the $f \times S_I$ Vs frequency f at $|V_G - V_T| = 0.1$ to 0.2 V and $|V_{DS}| \sim 0.05$ V, for p-MOSFETs with different gate electrode materials studied, with every plot showing the performance for various Hf %.

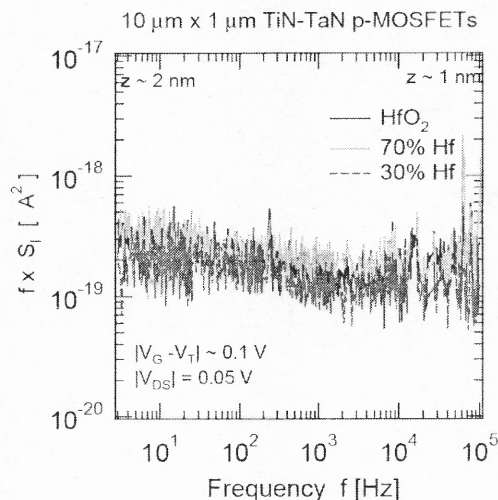


Figure 5.26 Qualitative trap profile $f \times S_I$ [A^2] Vs frequency f [Hz] at $|V_G - V_T| \sim 0.1$ V of metal gate p-MOSFETs for various Hf-silicate gate oxides.

For the $f \times S_I$ spectra the translation of the frequency axis into a tunneling distance z is also indicated along a second x-axis, for some average composition x . Assuming a pure tunneling model for the trapping and neglecting the interfacial layer, the tunneling depth z can be calculated from Equation (5.1) and α_t the tunneling parameter, given by

$$\alpha_t = \sqrt{[(2m_h^* \phi_b) / h^2]} \quad (5.4)$$

where h is Planck's constant divided by 2π .

The tunneling parameter α_t is estimated semi-empirically from the expected values of the effective tunneling hole mass (m_h^*) in the dielectric and the potential barrier for hole emission at the silicon-oxide interface (ϕ_b), which varies with composition x .

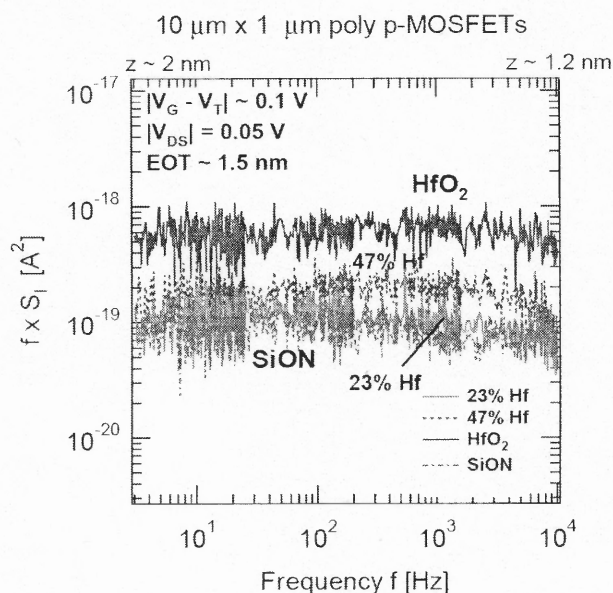


Figure 5.27 Qualitative trap profile $f \times S_I$ [A^2] Vs frequency f [Hz] at $|V_{GS} - V_T| \sim 0.1$ V of poly gate p-MOSFETs for various Hf-silicate gate oxides.

Assuming a Si/HfO₂ interface, the barrier height for the holes is taken as 3.4 eV for HfO₂ while the effective hole mass in Si is taken as $0.15m_0$, with m_0 the rest mass of the electron. The tunneling coefficient for holes is then estimated to be roughly 0.72×10^8

1/cm for the Si/HfO₂ system while it is $\sim 0.86 \times 10^8$ 1/cm for the Si/SiO₂ system. For an intermediate Hf composition, α_t is interpolated by assuming a linear variation with x in barrier height from 3.4 eV to 4.4 eV for the HfO₂ and the SiO₂ system, respectively.

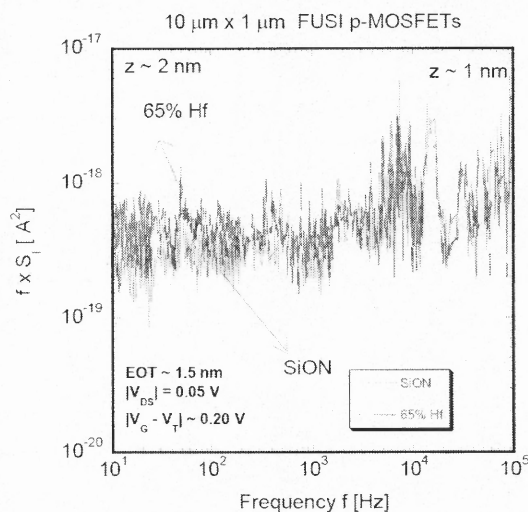


Figure 5.28 Qualitative trap profile $f \times S_1$ [A²] Vs frequency f [Hz] Vs f at $|V_G - V_T| \sim 0.2$ V of FUSI gate p-MOSFETs for various Hf-silicate gate oxides.

It is also noted that these spectra roughly correlate with trap density profiles in the oxide, though accurate Capacitance Equivalent Thickness (CET) values need to be considered. The impact due to the gate electrode material is clearly seen when Figures 5.26, 5.27 and 5.28 are compared.

The SiON devices are probed very close to the gate-dielectric interface as the physical thickness of the devices are ~ 2.0 nm, while for Hf-oxide devices, the tunnel depths at low frequencies indicate that one is probing the bulk of the high- κ layer close to the gate electrode-dielectric interface.

The three sets of devices with different gate electrodes (Figure 5.26, Figure 5.27 and Figure 5.28) show different qualitative trap profiles with tunneling depth. While the

metal gate devices (Figure 5.27) give higher values in the high- κ layer (lower frequency values) and at the interfacial layer of the device, a constant value is observed throughout the oxide and at the interface in the case of poly-Si electrodes (Figure 5.26). FUSI gates behave differently, where the lowest values were seen to be in the bulk high- κ layer and an increasing trend is observed towards the substrate-dielectric interface.

The frequency exponent γ of the observed $1/f^\gamma$ behavior was also studied and was observed to change as $\gamma \sim 1$ for poly-Si, $\gamma > 1$ for TiN-TaN while for FUSI it is $\gamma < 1$. Christensson [80] and C. Surya [51-52] have already shown in SiO₂ devices that the deviation in γ relates to the distribution of traps across the bandgap. If $\gamma < 1$, there is a greater number of high-frequency traps and the trap distribution is skewed towards the IL-Si interface, while for $\gamma > 1$, there is a greater number of low-frequency traps where the trap distribution is skewed away from the interface [39]. In our case on high- κ devices, FUSI gates ($\gamma < 1$) and TiN-TaN metal gates ($\gamma > 1$) emulate the behavior respectively. Alternatively, the behavior of the frequency exponent in these devices can also be regarded as a confirmation to the profile distribution observed from the $f \times S_I$ spectra as in Figures 5.26, 5.27 and 5.28.

The possible influence of gate electrode material on the properties of the high- κ layer near the gate electrode/high- κ interface and, therefore, on the $1/f$ noise parameters is also studied. Figure 5.29 shows the Drain Current Noise S_I Vs Drain Current $|I_D|$ of the three types of gate electrodes for a high- κ gate oxide of $\sim 55\%$ Hf. The fit shows that for all the cases S_I are proportional to I_D^2 , indicating that the noise mechanism could be related to trapping effects in the oxide following the number fluctuation (ΔN) theory. The drain current noise S_I is found to be lower for FUSI and metal gates when compared to

poly-Si, which correlates with the transconductance G_M and threshold voltage V_T in these devices (Figure 5.25).

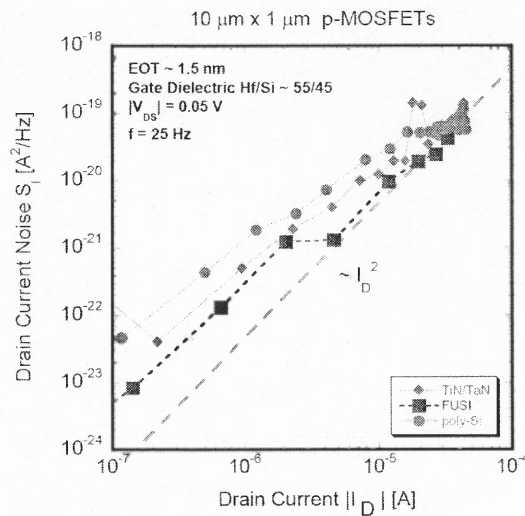


Figure 5.29 Drain Current Noise Spectral Density S_I [A²/Hz] Vs Drain Current $|I_D|$ [A] characteristics of TiN-TaN, FUSI and poly-Si gate p-MOSFETs for 55% Hf-silicate gate oxides.

It is inferred that the gate electrode material has a significant impact on $1/f$ noise and on the behavior of trap profiles when considering equivalent energy levels. For poly-Si (Figure 5.26), it is seen that HfO_2 has comparatively higher values in the $f \times S_I$ spectra while Hf-silicates have values in between SiON and HfO_2 . This difference is not noticeable in the case of metal gates (Figure 5.27), while the differences are found to be smaller in the case of FUSI gate devices (Figure 5.28).

For the poly p-MOSFET case, Figure 5.26 - which show the $f \times S_I$ spectra for different compositions of x , it may be possible that the defect centers related to oxygen vacancies may have different concentrations depending on the Hf composition. Fleetwood *et al.*[99] have shown that these E' defect centers have an impact on $1/f$ noise in SiO_2 . Although it has been recently reported that these defect centers have higher

concentration in Hf-based oxides, their complete role is currently still under further investigation. It is quite well known that the high- κ layer, which is generally considered more defective than SiO_2 , has a lower affinity towards oxygen and the Gibbs free energy for $\text{HfO}_2 + \text{Si}$ is smaller [94]. Hence it may be possible that during gate electrode processing a higher oxygen out-diffusion to the interfaces occur leading to a high vacancy concentration and, therefore, resulting in more oxygen related defects in the HfO_2 case. The oxygen vacancy concentration is expected to be higher in HfO_2 than Hf-silicates because of the higher Hf concentration in the bulk high- κ layers. The fact that no pronounced differences are observed in the case of FUSI or metal gates may be due to the possible impact of the gate electrode material on the oxygen related defects, as explained below.

Considering the HfO_2 (or a 55%Hf) case for the three gate electrodes, a higher O_2 transport (out-diffusion) is possible in the case of poly-Si gate electrodes due to a greater probability of a $\text{HfO}_2 + \text{Si}$ reaction, whereas this may be less applicable for FUSI gate devices due to the lower Si content in the gate electrode and not applicable at all in the case of a metal gate. Hence oxygen transport may be retarded or inhibited during the metal gate deposition process in the case of metal and FUSI gates leading to a lower concentration of oxygen related defect centers in the high- κ oxide. Due to these lower densities one observes a lower $1/f$ noise compared to poly-Si as seen in Figure 5.29.

This behavior is found to be quite consistent with a similar study conducted by Yu *et al.* [100], where they observed the influence of two types of FUSI gate electrodes (NiSi and NiSiGe) on the oxygen transport in HfSiON based high- κ devices.

It has to be mentioned that although we observed [101] in the past more scattering related effects in the case of metal gate p-MOSFETs, the assumption of a tunneling model for metal gate electrode p-MOSFETs is here taken into consideration only to enable a comparison between the three gate electrode materials. Recently, a similar study by [102] another group attributes $1/f$ noise in metal gate p-MOSFETs to number fluctuation theory, in which case, the tunneling model is applicable. The present data does not allow making a conclusive decision.

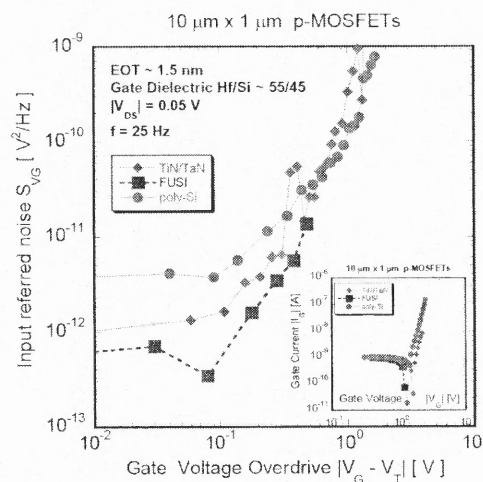


Figure 5.30 Input Referred Noise S_{V_G} [V^2/Hz] Vs Gate Voltage Overdrive $|V_{G_S} - V_T|$ [V] characteristics of TiN-TaN, FUSI and poly-Si gate p-MOSFETs for $\sim 55\%$ Hf-silicate gate oxides. (Inset) Gate leakage $|I_G|$ [A] – Gate Voltage $|V_G|$ [V] characteristics of TiN-TaN, FUSI and poly-Si gate p-MOSFETs for 55% Hf-silicate gate oxides.

Figure 5.30 shows the log-log plot of the input-referred noise S_{V_G} vs the gate voltage overdrive $|V_G - V_T|$ of poly-Si, metal and FUSI gates for oxides with $\sim 55\%$ Hf. The S_{V_G} 's have a parabolic nature with an increasing trend in all the three cases at higher gate voltages. This is believed to be partly due to an increased gate leakage current at higher gate voltage overdrives as shown in the inset of Figure 5.30. The input-referred

noise is seen to be the lowest in the case of FUSI gate devices while poly-Si gate p-MOSFETs have the highest input referred noise values. This is attributed to both higher G_M and lower S_I values of FUSI devices.

In order to investigate the possible influence of the composition of the underlying high- κ dielectric layer on the $1/f$ noise, various percentages of Hf in the high- κ dielectric layer were studied for FUSI gates. From the S_I - I_D characteristics in Figure 5.31, it looks like that this parameter has little or no effect on the $1/f$ noise. This is confirmed by the input referred noise of Figure 5.32 showing a very weak or no dependence on Hf content while the reference SiON transistors have somewhat lower values. These results are found to be quite consistent with the explanation given above relating to oxygen-vacancy-related defects and their effect on the high- κ gate stack composition.

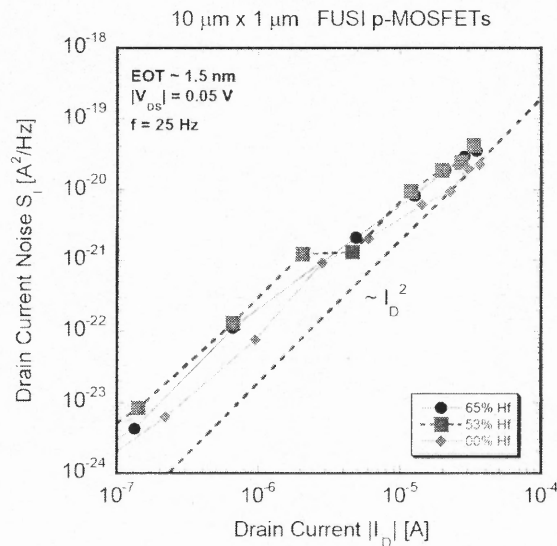


Figure 5.31 Drain Current Noise Spectral Density S_I [A²/Hz] Vs Drain Current $|I_D|$ [A] characteristics of FUSI gate p-MOSFETs for various Hf-silicate gate oxides.

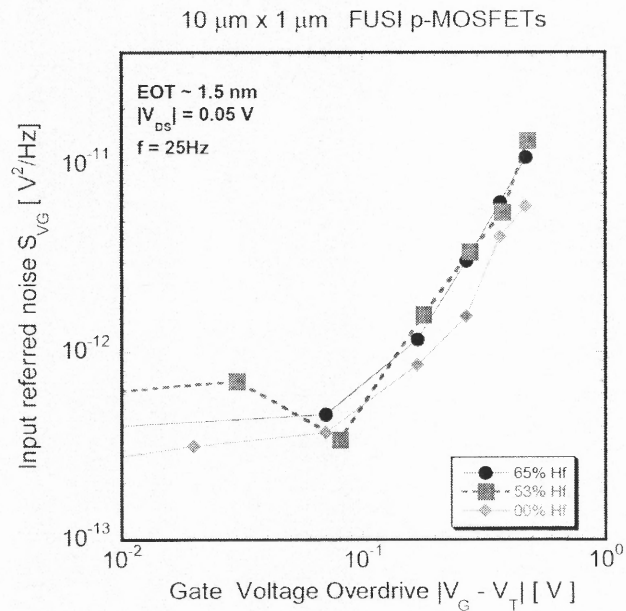


Figure 5.32 Input referred noise S_{V_G} [V^2/Hz] Vs Gate Voltage Overdrive $|V_G - V_T|$ [V] characteristics of FUSI gate p-MOSFETs for various Hf-silicate gate oxides.

Combining the results of all the samples in the S_{V_G} Vs % Hf plot at $|V_G - V_T| \sim 0.15$ of Figure 5.33, the values are seen to be more or less comparable among various Hf content devices, while for SiON, a slightly lower value is noticed. The latter meets the ITRS [7] specification of $200 \mu\text{V}^2/\text{Hz}$. From these results, it is seen that there is a weak or no correlation between the Hf-content and the $1/f$ noise magnitude in FUSI gate p-MOSFETs.

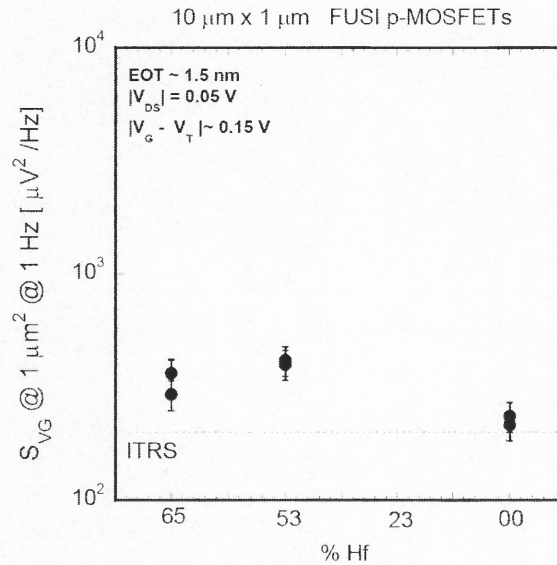


Figure 5.33 Input referred noise S_{VG} [V^2/Hz] Vs %HfO₂ of FUSI gate p-MOSFETs at $|V_G - V_T| \sim 0.15 \text{ V}$.

Assuming a trapping origin of the $1/f$ noise, an effective volume trap density N_T can be estimated from the values of S_{VG} , using the Equation (5.2). Table IV shows for the FUSI devices the volume N_T and surface trap densities D_T , and the S_I and S_{VG} values along with the tunneling depth z . The surface trap densities, calculated from N_T , are estimated using the formula $4kTzN_T$, where z is the tunneling distance of the carrier from the Si/high- κ interface at $f = 25 \text{ Hz}$. From Table 5.5, it can be inferred that the surface trap densities are higher for high- κ based devices when compared to SiON based FUSI gate devices.

Table 5.5 Noise Parameters and Estimated Trap Densities for FUSI Gate Devices with Different Hf-percentages of High- κ Dielectric.

Hafnium content in the high- κ dielectric	Values at $ V_{GS}-V_T = 0.10$ to 0.20 V, $ V_{DS} = 0.05$ V, $f = 25$ Hz						
	S_I [A ² /Hz]	S_{VG} [V ² /Hz]	$\sqrt{S_{VG}}$ [V/ $\sqrt{\text{Hz}}$]	z [nm]	α_1 [1/cm]	N_T [1/cm ³ eV]	D_T [1/cm ²]
00% Hf	6.12E-21	9.00E-13	9.48E-07	2.01	0.86E08	2.30E+18	4.81E+10
53% Hf	9.58E-21	1.62E-12	1.27E-06	2.30	0.78E08	2.76E+18	6.60E+10
65% Hf	8.18E-21	1.31E-12	1.14E-06	2.43	0.74E08	1.95E+18	4.92E+10

The possible influence of composition of the underlying high- κ dielectric layer on the $1/f$ noise, were also studied for poly-Si and TiN-TaN (metal) gate devices for various percentage of Hf-silicate devices.

5.4.2 Comparison in n- and p-MOSFETs – Poly-Si Vs TiN-TaN

To investigate more in detail the impact of the gate electrode material [poly-Si versus metal] on the noise performance, by considering the device-to-device variation, Figure 5.34a and 5.35a is plotted with data obtained from poly-Si and metal gate devices for n-MOSFETs and p-MOSFETs.

To achieve this, a 0.8 nm thin interfacial chemical oxide layer [IMEC clean] was employed on top of which either HfO₂ or Hf_xSi_{1-x}ON with various Hf-contents ranging from 25 \pm 5%, 50 \pm 5% and 70 \pm 5% were deposited. 0% Hf refers here a SiON gate dielectric case, whereas 100% Hf refers to HfO₂ gate dielectric. Deposition of the high- κ oxides was achieved by MOCVD. Both standard polysilicon and TiN/TaN was employed

as a gate electrode material. These devices were post-deposition annealed in NH_3 at 800°C for 60 s, followed by a forming gas anneal at 520°C for 20 min.

Figures 5.34b and 5.35b show the values for $|V_{\text{GS}}-V_{\text{T}}|$ of 0.5 V for the same set of devices compared. For n-MOSFETs, the impact of the gate material is noticed for pure HfO_2 gate stacks [100% Hf], whereby the metal electrode devices perform on the average better - close to an order of magnitude for HfO_2 - when compared to poly-Si electrode MOSFETs. This can be observed quite clearly for $|V_{\text{GS}}-V_{\text{T}}|$ of 0.5 V case, though $|V_{\text{GS}}-V_{\text{T}}| \sim 0.1$ V data have results towards this observed trend.

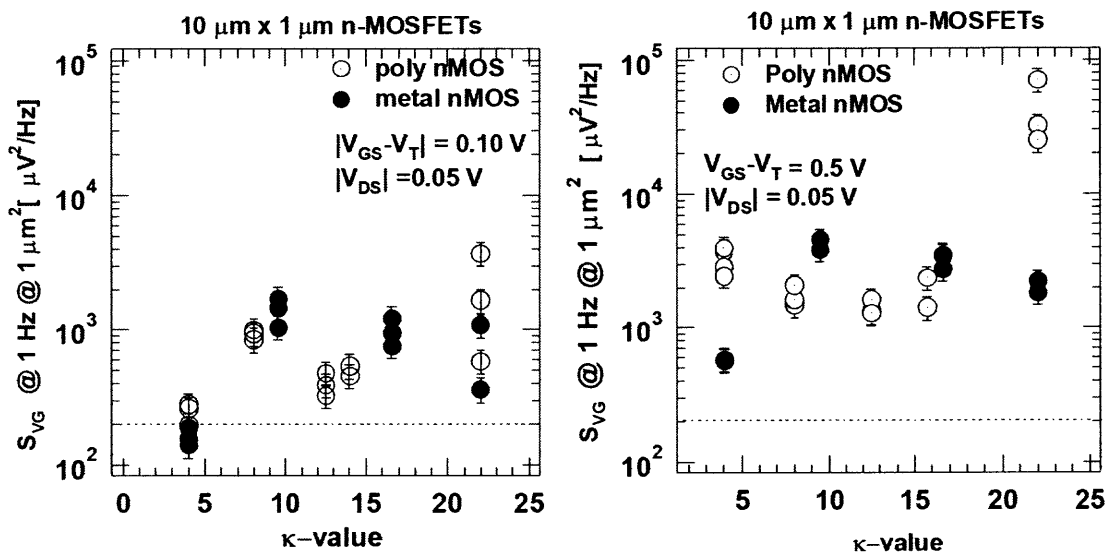


Figure 5.34 (a) Impact of gate electrode material on $1/f$ noise for n-MOSFET poly-Si and metal gate devices. The comparisons are made using the normalized S_{VG} values at $|V_{\text{DS}}|=0.05\text{V}$ and $|V_{\text{GS}}-V_{\text{T}}| = 0.1\text{V}$ and (b) $|V_{\text{DS}}|=0.05\text{V}$ and $|V_{\text{GS}}-V_{\text{T}}| = 0.5\text{V}$. Dotted line on the figure indicates the ITRS requirement.

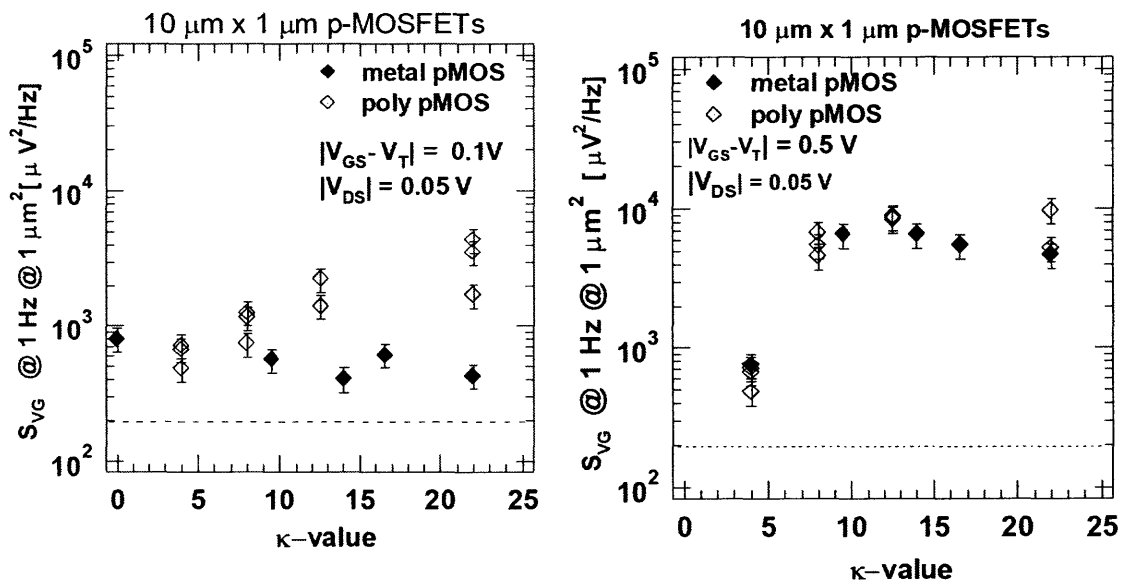


Figure 5.35 (a) Impact of gate electrode material on 1/f noise for p-MOSFET poly-Si and metal gate devices. The comparisons are made using the normalized S_{VG} values at (a) $|V_{DS}|=0.05\text{V}$ and $|V_{GS}-V_T| = 0.1\text{V}$ and (b) $|V_{DS}|=0.05\text{V}$ and $|V_{GS}-V_T| = 0.5\text{V}$. Dotted line on the figure indicates the ITRS requirement.

It will be discussed in the next chapter that the presence of fixed oxide charges Q_{fc} at the poly-Si/high- κ interface, could account for a higher noise in poly-Si/HfO₂ devices. The impact of the gate electrode material is found to be weak for other Hf-silicate percentages MOSFETs in Figure 5.34. For p-MOSFET devices, the metal gate devices behave significantly better in Figure 5.35. The input referred noise is somewhat higher for p-MOSFETs than for n-MOSFET, for Hf-silicates, and significantly higher with respect to the ITRS requirement. This may be due to observed differences in noise behavior between n-MOSFET and p-MOSFET devices. While n-MOSFETs tend to follow the theory on number fluctuations in general, p-MOSFETs follow mobility fluctuations. Recently it has been observed that the correlation between 1/f noise and low-field mobility is higher in such devices, which could be the possible reason for higher 1/f noise

in p-MOSFETs. Recently Lu *et al.* [103] have observed that hole trapping is an important issue to be considered in HfO₂ based devices. Hence it is possible the higher 1/f noise exists in p-MOSFETs if one argues that trapping is the origin of 1/f noise is p-MOSFETs also. From all these discussions, it is clear that in these devices noise is one of the critical factors for 45 nm analog applications.

5.4.3 Gate Electrode Processing Effects – ALD Vs PVD

In the above experimental condition, the TaN bottom electrode was either deposited by Physical Vapor Deposition (PVD) or Atomic Layer Deposition (ALD) as metal gate, while TiN (PVD) was used as a capping layer. Figure 5.36 shows the comparison of normalized S_{VG} 's for ALD and PVD deposited TaN gate electrodes for n-MOSFET devices at $|V_{GS} - V_T| = 0.1$ V and $|V_{DS}| = 0.6$ V, while the inset shows the values at $|V_{DS}| = 0.05$ V.

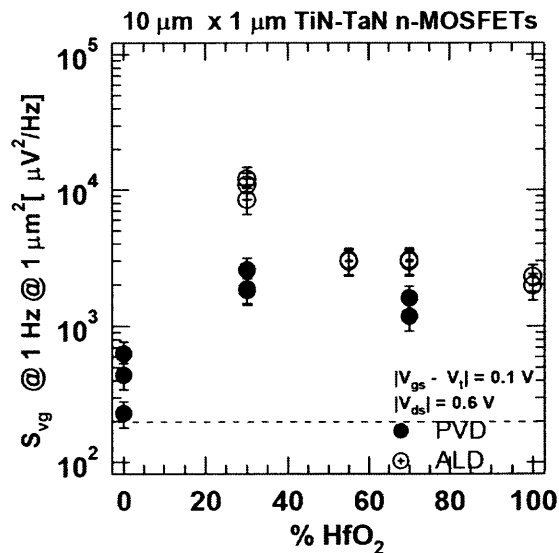


Figure 5.36 Impact of gate stack processing – ALD Vs PVD on 1/f noise. Comparisons are made using the normalized S_{VG} values at $|V_{DS}|=0.6$ V and $|V_{GS}-V_T| = 0.1$ V. Dotted line on the figure indicates the ITRS requirement.

The gate oxide deposited is still MOCVD in both the cases. The noise performance of PVD deposited gate electrodes is better when compared to ALD deposited gate electrodes. This trend is more evident for $|V_{DS}|$ of 0.05 V case. ALD processed TaN gate electrodes are also found to be nitrogen rich and more resistive than PVD processed gate electrodes. Hooker *et al.* [104], observed that the impact of nitrogen could significantly influence the charge trapping in similar devices. It has been quite well proven that $1/f$ noise is due to traps, in n-MOSFET devices. In our earlier observation as described in Section 5.2, it is seen that the nitrogen content in the gate dielectric quite strongly influences the $1/f$ noise. From these two observations, it may be possible that the nitrogen content in the processed gate electrodes could influence the noise behavior. In contrast to the previous sections which reported the impact of the nature of gate oxide or gate electrode (poly-Si versus metal), the effect due to the deposition technique used for the metal gate electrode is observed across all studied Hf-concentrations. While the reference SiON devices came close to the ITRS noise requirement [7], one can notice that the noise factor for the silicates is still higher by at least an order of magnitude.

In general, lower noise is observed for SiON for n- and p-MOSFETs, though one can observe higher values for poly n-MOSFET $|V_{GS}-V_T| \sim 0.5$ V case. The difference observed at $|V_{GS}-V_T| \sim 0.5$ V may be due to increased correlation between gate and drain current noise at higher gate voltages for poly n-MOSFETs, which we have observed earlier. In comparison with $1/f$ noise ITRS requirement of $200 \mu V^2/Hz$ [7] for CMOS device for 45 nm node, between half to one decade higher noise is observed in these devices.

Table 5.6 Comparison of Volume (N_T) and Surface Trap Densities (D_T) as Figure of Merit for Various Gate Stack Compositions for n-channel poly-Si and Metal gate (PVD and ALD gate electrode) Si-substrate n-MOSFET Devices.

GATE ELECTRODE	GATE STACK COMPOSITION $ V_{GS}-V_T = 0.1 \text{ V}, V_{DS} = 0.05 \text{ V}$									
	HfO ₂		Hf-rich		Hf-Si		Si-rich		SiON	
	N_t (1/cm ³ eV) 10 ¹⁸	D_t (1/cm ²) 10 ¹²	N_t (1/cm ³ eV) 10 ¹⁸	D_t (1/cm ²) 10 ¹²	N_t (1/cm ³ eV) 10 ¹⁸	D_t (1/cm ²) 10 ¹²	N_t (1/cm ³ eV) 10 ¹⁸	D_t (1/cm ²) 10 ¹²	N_t (1/cm ³ eV) 10 ¹⁸	D_t (1/cm ²) 10 ¹²
Poly	370	10.7	24.3	7.2	0.9	0.3	1.2	0.8	0.7	0.2
Metal (PVD)	1.1	0.35	1.9	0.6	NA	NA	3.2	1.0	0.5	0.15
Metal (ALD)	17.7	5.1	16.5	4.9	21.4	6.4	8.7	2.7	NA	NA

In the case of metal gate electrodes, also only a weak dependence of the input-referred noise on Hf-content in the silicates has been observed, reported previously. We have considered all the available Hf-silicate percentage for the remaining discussion to study the impact of gate electrode and its' processing, along with reference SiON and HfO₂ devices.

5.5 Noise Mechanism study in Hf-based MOSFETs

5.5.1 Poly-Si Gate Electrodes

This section describes the low frequency noise mechanism observed in devices with Hf-silicate as gate dielectric and poly-Si as gate electrode. N-channel MOSFETs of dimensions $W/L=10/1$ (μm), with SiON (1.5 nm), pure HfO₂ and with various SiO₂/HfO₂ ratios [three different values of x/y of Hf_xSiO_yN, as 23/77, 47/53 and 65/35] were fabricated using conventional CMOS process flow. A 0.8 nm thin interfacial chemical oxide layer was employed on top of which either HfO₂ or HfSiON with various Hf-

contents, ranging from 30%, 55% to 70% were deposited. Deposition of the high- κ oxides was achieved by MOCVD. Polysilicon was employed as gate electrode material. These devices were post-deposition annealed in NH_3 at 800°C for 60 s, followed by a FGA @ 520°C for 20 min.

The normalized current noise spectral density S_{ID}/I_D^2 against the drain current I_D is represented in Figure 5.37 and Figure 5.38 for n and p-MOSFETs, respectively. The normalized values are \sim two orders of magnitude higher for the HfO_2 devices as shown in Figure 5.37, when compared with their SiON and $\text{Hf}_x\text{Si}_{1-x}\text{ON}$ counterparts, while the difference is comparatively lower for p-MOSFETs. For the various silicate ratios, similar S_{ID}/I_D^2 values are observed for both n and p-MOSFETs. As can be noted in Figure 5.37, a leveling off in weak inversion and a roll-off with $1/I_D^k$, where $k \sim 1$, occurs in strong inversion.

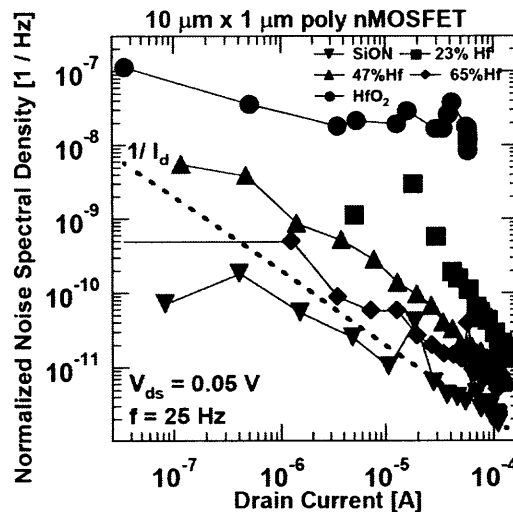


Figure 5.37 Normalized drain current spectral density S_{ID}/I_D^2 Vs Drain current I_D for $10\ \mu\text{m} \times 1\ \mu\text{m}$ poly-Si n-MOSFETs for various Hf-silicates at $V_{DS}=0.05\text{V}$ and $f=25\text{Hz}$.

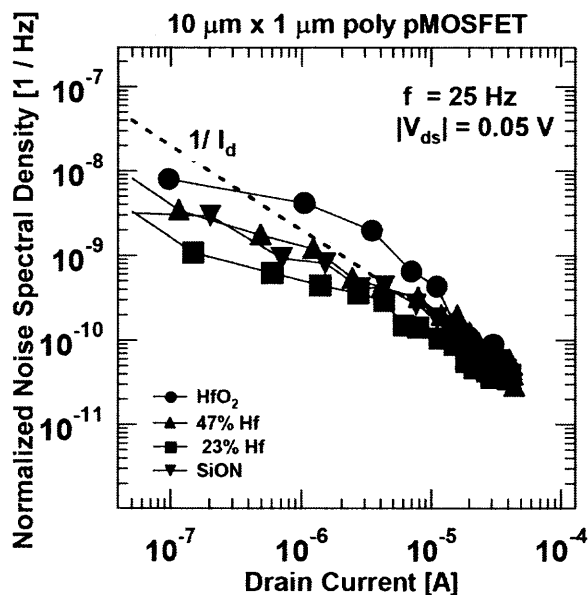


Figure 5.38 Normalized drain current spectral density S_{ID}/I_D^2 Vs Drain current I_D for 10 μm x 1 μm poly-Si p-MOSFETs for various Hf-silicates at $|V_{DS}|=0.05\text{V}$ and $f=25\text{Hz}$.

It was also observed that S_{ID} at $f = 25\text{Hz}$ and for all Hf/Si ratios varies according to I_D^x for $1 < x < 2$, whereby x lowers for increasing I_D . An I_D^2 dependence was noticed at low drain currents, suggesting a $1/f$ noise origin related to trapping/de-trapping of charges near the interface (number fluctuations).

From the variation in the normalized drain current noise spectral density S_{ID}/I_D^2 with drain current, represented in Figure 5.38 and 5.39 for n and p-MOSFETs. It can be deduced that there is an agreement with the g_M^2/I_D^2 ratio. This again suggests that the $1/f$ noise in the studied transistors can be described in the frame of the correlated number fluctuations theory [39], based on carrier trapping/detrapping in the gate dielectric.

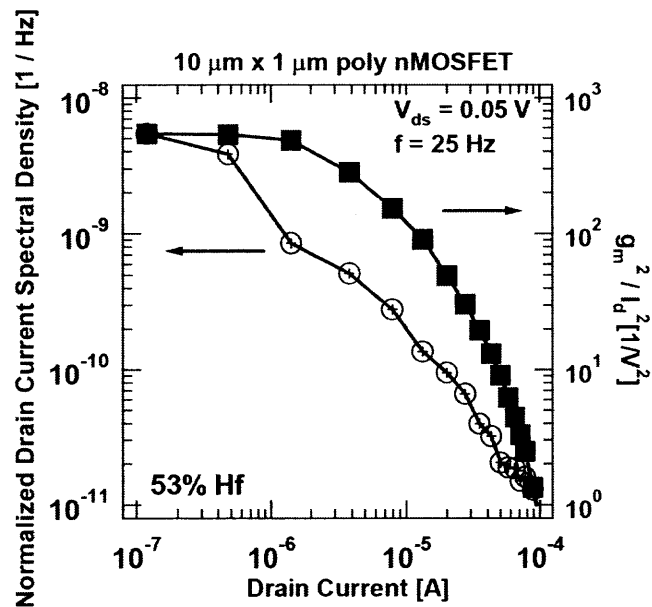


Figure 5.39 Normalized drain current spectral density S_{ID}/I_D^2 and g_m^2/I_D^2 Vs drain current I_D for $10\ \mu\text{m} \times 1\ \mu\text{m}$ n-MOSFETs for 53% Hf dielectric at $V_{DS}=0.05\text{V}$ and $f=25\text{Hz}$.

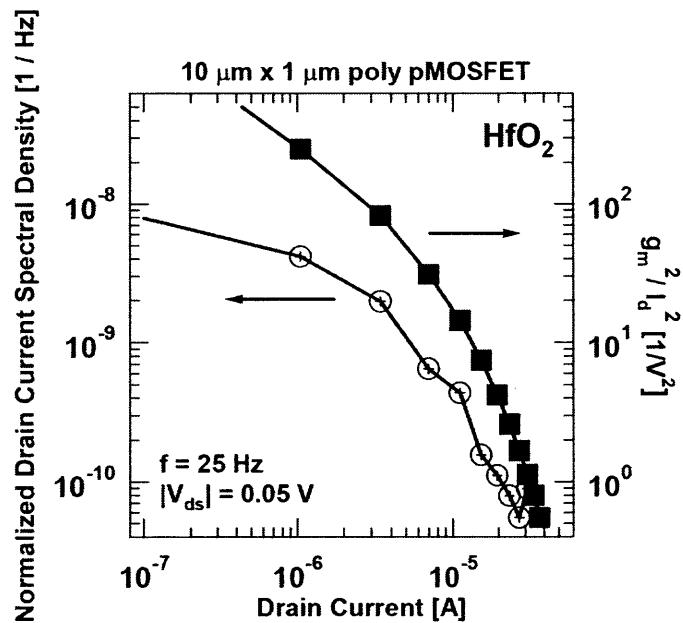


Figure 5.40 Normalized drain current spectral density S_{ID}/I_D^2 and g_m^2/I_D^2 Vs drain current I_D for $10\ \mu\text{m} \times 1\ \mu\text{m}$ n-MOSFETs for 53% Hf dielectric at $V_{DS}=0.05\text{V}$ and $f=25\text{Hz}$.

5.5.2 Metal (TiN-TaN) Gate Electrodes

N- and p-MOSFETs of W/L=10/1, with a 0.8 nm thin interfacial SiO₂ layer on top of which silicates with various compositions equal to 30%, 55%, 70% and 100% HfO₂ were deposited. PVD TiN/TaN was employed as metal gate. Deposition of the high- κ oxides was achieved by MOCVD. These devices were annealed in ammonia at 800°C for 60 s. EOT of the devices were found to be 1.5 +/- 0.2 nm.

To investigate the origin of the 1/f noise, the normalized noise spectral density S_{ID}/I_D^2 dependence versus the drain current $|I_D|$ at a constant frequency $f=25\text{Hz}$ is reported as in Figure 5.41. In case number (Δ) fluctuations dominate, a leveling off in weak inversion will be noticed and a roll-off with $1/I_D^k$ in strong inversion ($k\sim 1$). This is clearly seen in Figure 5.41 for the n-MOSFETs.

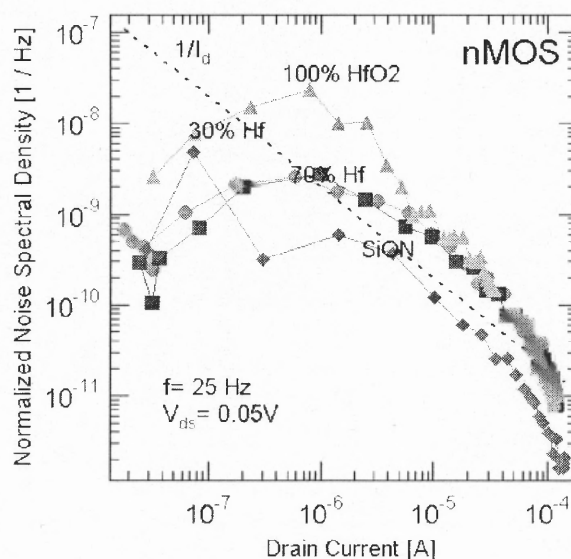


Figure 5.41 Normalized drain current noise spectral density S_{ID}/I_D^2 at $|V_{DS}|=0.05\text{V}$ for metal gate n-MOSFETs for various gate stack composition with SiON as reference gate oxide.

The p-channel devices, on the other hand, show an S_{ID} that varies with $1/I_D$ in Figure 5.42, over the whole current range studied. This points to a mobility fluctuations ($\Delta\mu$) dominance for p-MOSFET devices [46]. Moreover, no strong dependence on the Hf-content was found for the normalized noise of p-MOSFETs in Figure 5.42.

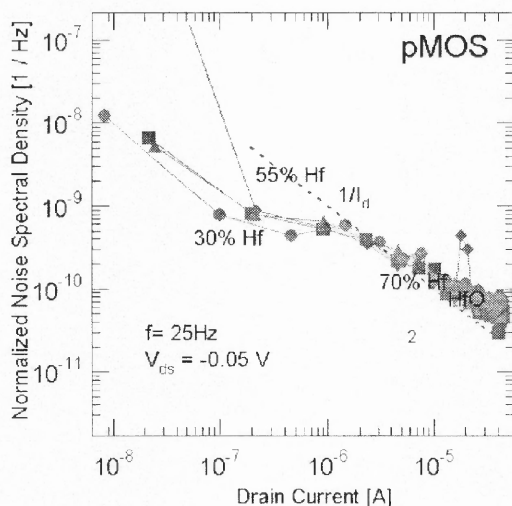


Figure 5.42 Normalized drain current noise spectral density S_{ID}/I_D^2 at $|V_{DS}|=0.05V$ for metal gate p-MOSFETs for various Hf-based gate stack composition.

For n-MOSFETs at $f = 25$ Hz, Figure 5.43 shows a good agreement between these two functions, supporting the number fluctuation theory for these devices. However, as illustrated in Figure 5.44 for p-MOSFETs, no clear correlation is noticed, so that in this case, bulk mobility fluctuations are the possible origin of the noise.

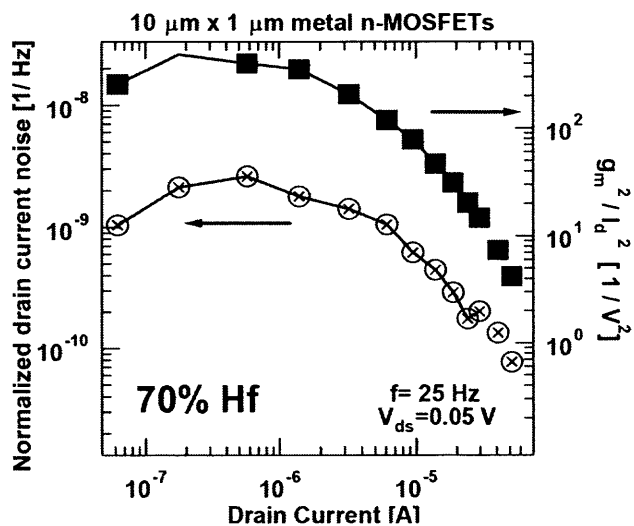


Figure 5.43 Normalized drain current spectral density S_{ID}/I_D^2 (1° Axis; circles) and g_m^2/I_D^2 (2° Axis; squares) versus drain current I_D for 53%Hf n-MOSFETs.

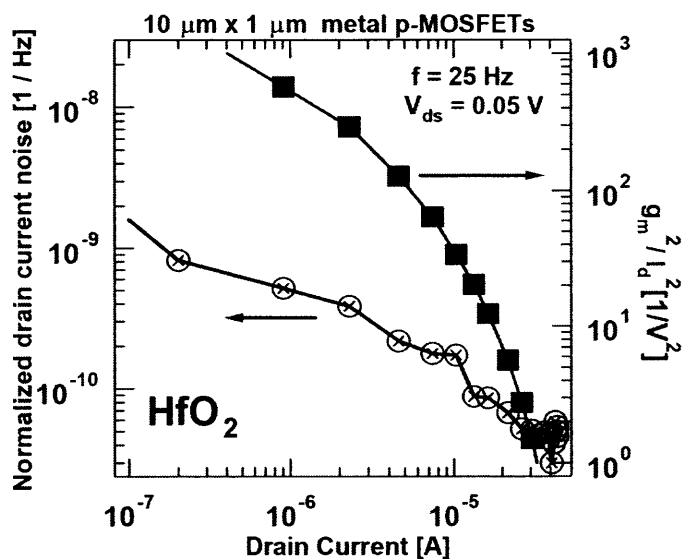


Figure 5.44 Normalized drain current spectral density S_{ID}/I_D^2 (1° Axis; circles) and g_m^2/I_D^2 (2° Axis; squares) versus drain current I_D for HfO₂ p-MOSFETs.

5.6 Gate/High- κ Interface

5.6.1 Gate/High- κ Interface Treatment

To investigate the influence of gate/high- κ interface, two different types of devices were considered. The starting gate dielectric is a 1.5 nm thick SiON layer and ALCVD was used to deposit 5, 10, and 20 cycles of HfO₂ on the top of the SiON as shown in Figure 5.45. More information on the volume of deposited Hf can be found from the Rutherford Backscattering Studies (RBS) from L. A. Ragnarsson *et al.* [105]. The equivalent Oxide Thickness (EOT) was 1.5 nm +/- 0.2 nm for all studied devices. It is to be noted that 10 cycles corresponds to an oxide thickness of ~ 1 nm. The samples were subjected to a Forming Gas Anneal (FGA) at 520°C for 20 min. To understand and verify the Fermi-pinning effect on 1/f noise at the gate-SiON interface, two types of gate material are being used: n-type polysilicon (poly Si) or Fully nickel Silicided (FUSI) (undoped).

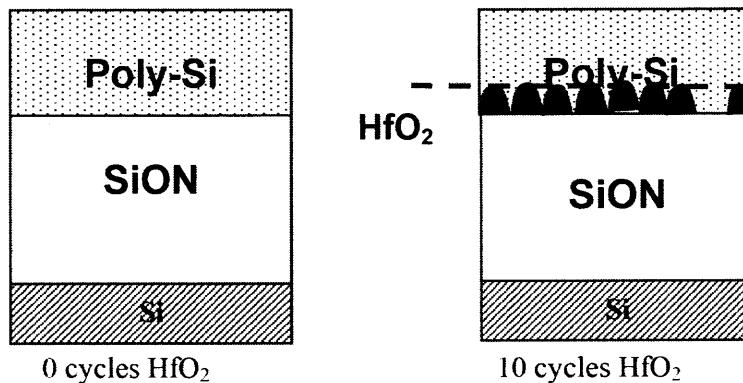


Figure 5.45 Schematic of gate stack with and without the growth cycles of HfO₂.

The noise has been measured on 10 μm x 1 μm and 10 μm x 0.25 μm poly-Si devices, while only 10 μm x 0.25 μm n-MOSFETs were used for FUSI gates. On-wafer

noise measurements were performed in linear operation at a constant drain voltage $|V_{DS}|=0.05$ V for gate voltages $|V_{GS}|$ between 0.3 – 1.2 V, in steps of 50mV using BTA9812 hardware and NoisePro software from Cadence.

5.6.2 Fermi Level Pinning Effects – Poly-Si Vs FUSI

Figure 5.46a and 5.46b shows the transconductance characteristics of, poly and FUSI gates with and without HfO_2 cycles respectively. A 10 ~ 15% reduction in mobility is observed when a few cycles of HfO_2 are present at the gate-SiON interface in these devices. The ~ 0.6 V increase in the threshold voltage for SiON in Figure 5.46b compared to Figure 5.46a is related to the 0.6 eV lower work function of the FUSI gate. For the FUSI gates, a significant increase of the inversion capacitance density (C_{eff}) and reduced poly-depletion effects were observed.

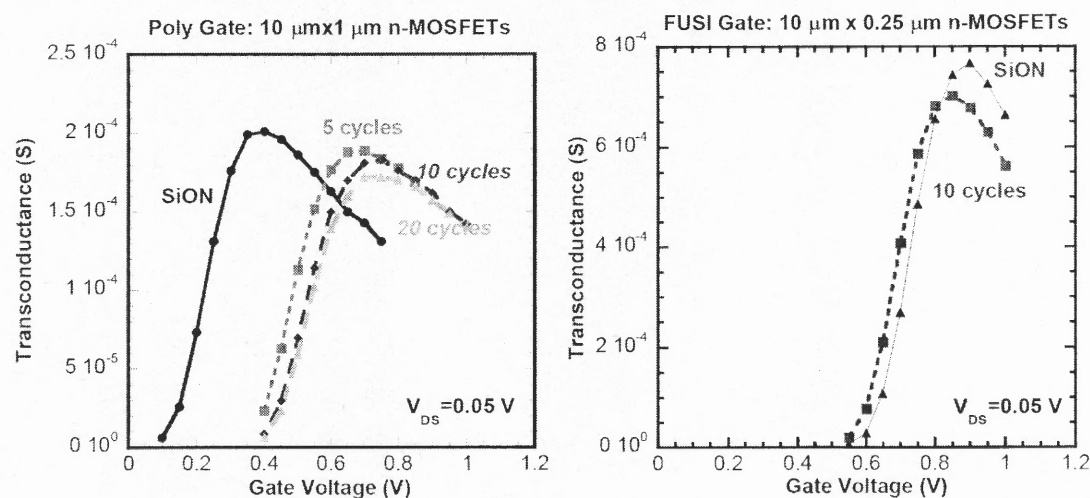


Figure 5.46 Input characteristics in linear operation ($V_{DS}=0.05$ V) for (a) 10 $\mu\text{m} \times 1.0 \mu\text{m}$ poly-silicon gate and 10 $\mu\text{m} \times 0.25 \mu\text{m}$ FUSI gate (b) n-MOSFETs with and without a few cycles of HfO_2 on top of a 1.5 nm SiON gate dielectric.

Figure 5.47 shows the noise spectra of pure SiON and devices with 5, 10 and 20 cycles of HfO₂ for $|V_{DS}| = 0.05$ V and $|V_{GS} - V_T| = 0.10$ V for poly-Si gates. The noise spectra S_{ID} obtained on SiON devices with few cycles of HfO₂ showed a similar $1/f^\gamma$ behavior across all the frequencies with a frequency exponent $\gamma \sim 1$. A mixed behavior was noticed for 1.5 nm EOT SiON devices whereby the device exhibits two different slopes – a higher value of γ ($\gamma \sim 1.2$) for the low frequency part $f < 100$ Hz, and a lower value ($\gamma \leq 1$) at higher frequencies. A similar nature was also observed in FUSI gate devices with SiON and 10 cycles of HfO₂. Assuming that the current fluctuations are due to trapping, this indicates a higher trap density close to both interfaces.

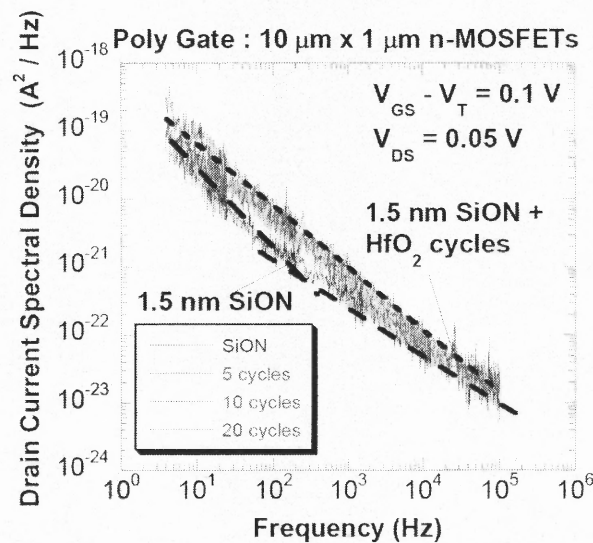


Figure 5.47 Drain current spectra S_I Vs frequency f of devices with SiON and 5, 10 and 20 cycles of HfO₂. Two different slopes are observed for pure SiON devices.

The values of the frequency exponent γ were also plotted for various gate voltage overdrives as shown in Figure 5.48. In the case of SiON with few cycles, γ is found to be constant ($\gamma \sim 1$) over the measured gate voltage overdrives, while for SiON, γ varies significantly from 0.9 to as high as 1.8. Excess noise peaks are observed as indicated in

Figure 5.48 by numbers. These peaks have a frequency exponent $\gamma > 1$, which would mean that a greater number of low-frequency traps are away from the substrate-dielectric interface [39]. In the case of a few cycle devices, the frequency exponent γ is less than 1 for $V_{GS} > V_T$ indicating that the trap distribution is increasing towards the substrate-dielectric interface.

As the normalized spectral density (S_I/I_D^2) and the $(g_M/I_D)^2$ ratio are found to be parallel to each other, the McWhorter [44] theory related to carrier trapping can be used to analyze the noise origin. Though this emphasizes that carrier number fluctuations due to tunneling to and from the traps are the cause for the observed $1/f$ noise, it is probable that scattering-related events could also contribute to the source of $1/f$ noise. Both approaches are further used to get a better insight into the underlying fundamental differences in these devices.

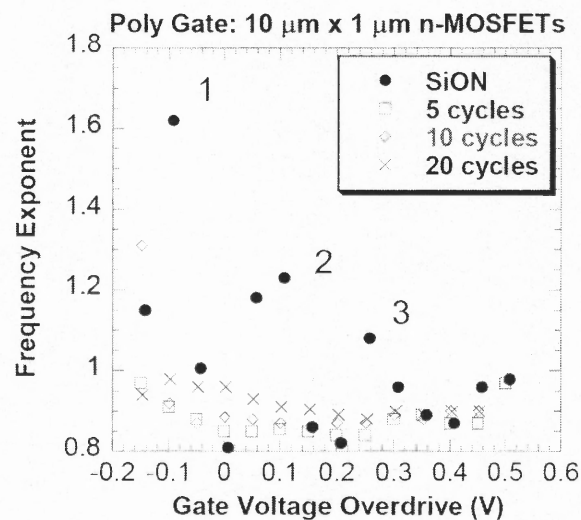


Figure 5.48 Frequency exponent γ Vs gate voltage overdrive for poly-Si devices with pure SiON and with a few cycles of HfO₂ on top of SiON. Numbers indicate excess noise peaks in SiON.

The above differences observed are explained using two possible fluctuation mechanisms related to trapping and scattering – number fluctuation theory and correlated mobility fluctuation theory. The first theory assumes that channel carriers are the origin of $1/f$ noise while the second theory takes into account the scattering related events also.

5.6.2.1 Number fluctuation theory based approach. The low-frequency contribution generated by deeper lying traps can be studied by plotting the trap density values with depth as shown in Figures 5.49a and 5.49b, based on the simplest approximation, where the tunneling distance z is related to the noise frequency f by Equation (5.1).

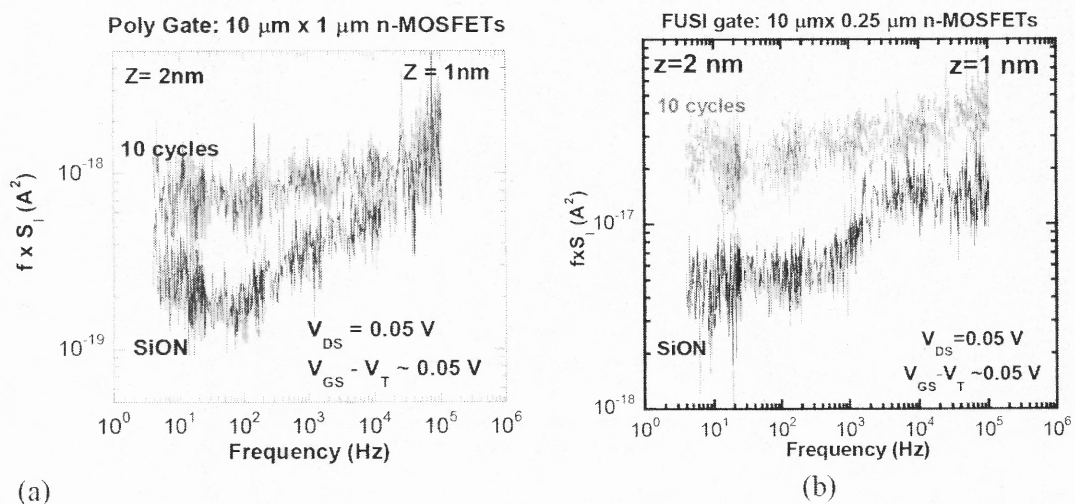


Figure 5.49 Normalized low-frequency noise spectrum $f \times S_I$ versus frequency f in linear operation ($V_{DS}=0.05$ V) and at $V_{GS} - V_T \sim 0.05$ V, for (a) $10 \mu\text{m} \times 1 \mu\text{m}$ poly-Si n-MOSFETs and (b) $10 \mu\text{m} \times 0.25 \mu\text{m}$ n-MOSFETs, with SiON and SiON plus 10 cycles HfO_2 , respectively.

In Figures 5.49a and 5.49b, the current noise spectral density S_I multiplied by the frequency f is represented versus f for poly and FUSI gate devices with and without 10 cycles of HfO_2 at $V_{GS} - V_T \sim 0.05$ V. By representing the spectra in this way, a few features become more obvious. First, it is clear that the highest noise is found in case of

10 cycles for both FUSI and poly gates. Next, it is also obvious that the frequency exponent (γ) changes with f ; in the case that $\gamma=1$, one would expect a horizontal curve, which confirms the results obtained in Figure 5.48. In the context of the McWhorter model, one can say that the variation of γ is due to a non-uniform density of oxide traps (N_{ot}). As shown in Figure 5.49a, the trap density is lower approaching the gate-dielectric interface, compared with the Si/SiON interface. Putting this in perspective, the tunneling depth at the lowest (~ 4 Hz) and highest (100 kHz) frequency, calculated from Eq. (1) is indicated in Figure 5.49a and 5.49b. It is clear that the low-frequency part of the spectra corresponds to a depth that is larger than the physical oxide thickness, but in the same range of the electrical or effective thickness.

The trap density calculations are based on the relationship with S_{VG} as per the Equation (5.2). A decaying profile is noticed near the interfacial layer as shown in Figure 5.49a, which is in agreement with the well-established fact that there exists a highly defective transition layer close to the Si/SiO₂ interface. The spectra of Figure 5.49a suggest an increased trap density in the SiON layer when approaching the silicon interface. There are two possible reasons for that: it is known that the presence of nitrogen introduces additional noise centers, so that Figure 5.49a would indicate an increasing nitrogen profile towards the silicon interface. Alternatively, it is known that the transition layer of 0.6 nm between the silicon substrate and the bulk oxide is highly defective and consists of suboxides. This again could be the origin of a higher $1/f$ noise at higher frequencies in the case of the poly or FUSI gate transistors.

Around 1.7 nm, the volume trap density of the SiON device increases to as high as 10^{17} $1/\text{cm}^3$. This is close to the gate-SiON interface and suggests that there is an

increasing trap density probed in the transition layer of the poly-Si/SiON interface. Unlike the SiON case, the trap values are higher and are found to be constant throughout the oxide depth, in devices with few cycles HfO_2 as shown in Figure 5.50a.

Due to Fermi-level pinning at the HfO_2 /poly-Si interface, oxide charges present at this interface could translate into a more or less constant trap density in the oxide as seen in Figure 5.50a. These additional charges are not present in the pure SiON layer and therefore one sees lower trap density values for pure SiON device. Further confirmation can be seen from the static DC characteristics where a shift in threshold voltage $V_T \sim 0.2$ V is observed in Figure 5.50b.

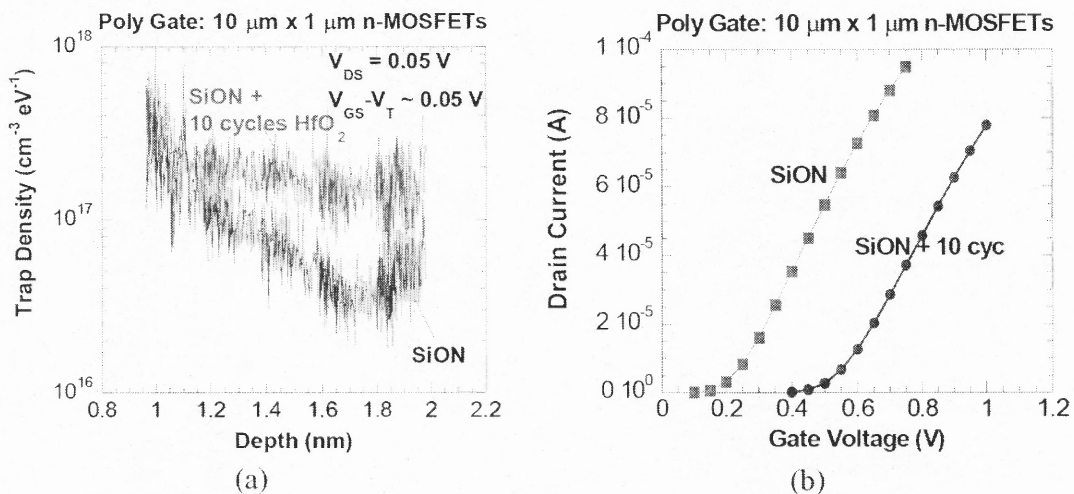


Figure 5.50 (a) Trap density versus depth in linear operation ($V_{DS}=0.05 \text{ V}$) and at $V_{GS} - V_T \sim 0.05 \text{ V}$, for a $10 \mu\text{m} \times 1 \mu\text{m}$ poly-Si n-MOSFET with and without 10 cycles HfO_2 on top of a 1.5 nm SiON gate dielectric. (b) Threshold Voltage V_T shifts observed between SiON and SiON with 10 cycles of HfO_2 .

When regarding the low-frequency part, corresponding with the layer near/at the gate-oxide interface, it is clear that the density of fluctuation sources is a strong function of the gate material used, with the lowest value for the FUSI pure SiON devices. Translated to a density of traps, it means that there exist about three times more traps

close to the gate-oxide interface for the FUSI + 10 cycles HfO₂ transistor, compared with its FUSI pure SiON counterpart. Moreover, a Fermi-level pinning effect has, for example, also been reported for the PtSi/HfO₂ gate stack [106], whereby it is shown that the presence of Si atoms at the interface causes the pinning effect, i.e., by creating a high density of interface traps. From Figure 5.51, it is seen that the trap density increases based on number of cycles deposited, confirming higher Fermi-level pinning effect at the interface. A similar trap density increase at $f=10$ Hz, i.e., close to the gate-dielectric interface was obtained for a FUSI gate with 10 cycles of HfO₂.

In the literature, different types of traps have been proposed to explain the Fermi-level pinning [98]. They all rely on an oxygen deficit, leading either to the formation of Si-Hf bonds at the interface or to V-O centers. Although 1/f noise cannot identify the defects sites responsible for the increased trap density, the fact that there appears to be a continuous increase of N_{ot} into the bulk of the SiON layer supports the second hypothesis. Alternatively, one could suppose that the traps at the gate-oxide interface correspond to Si-Hf bonds while deeper in the material additional V-O centers are being created during the HfO₂ deposition, possibly by an out-diffusion of oxygen to the surface.

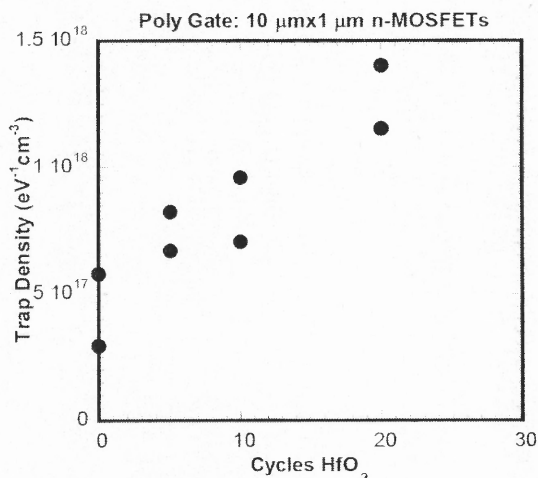


Figure 5.51 Trap Density Vs cycles HfO₂ for poly-gate 10 μm x 1 μm n-MOSFETs.

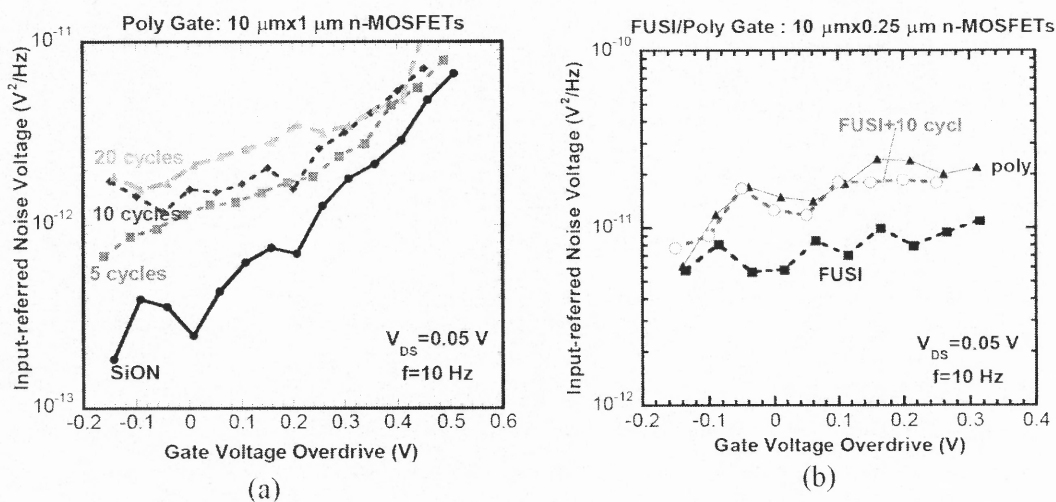


Figure 5.52 Input-referred noise spectral density S_{VG} at 10 Hz versus gate voltage overdrive $V_{GS} - V_T$ in linear operation ($V_{DS}=0.05$ V) for n-MOSFETs corresponding with (a) a poly silicon gate and SiON or SiON plus a few cycles HfO₂, and (b) a poly-Si gate with SiON and a poly-Si or FUSI gate with SiON plus a few cycles of HfO₂.

Similar values of input-referred noise S_{VG} were observed for FUSI and poly-Si gate in Figure 5.52b, when account is made of the polysilicon depletion effect on the effective capacitance. Comparable trap densities were found for FUSI and poly-Si gate devices, close to the gate and near the silicon interface.

5.6.2.2 Correlated mobility fluctuation theory based approach. For larger gate voltage overdrives, the input-referred noise spectral density of the studied devices can be described by the correlated-mobility fluctuations model [39], described by Equation (5.3). The effective mobility was calculated from the channel transconductance values measured during noise and is plotted along the electric field and the injected charge Q_{inj} on the 1^o and 2^o X-axes respectively as shown in Figure 5.53a. It is seen that the peak mobility μ_{peak} for devices with few cycles reduced to $\sim 80\%$ of the pure SiON value. In that case, the noise increase for a few cycles has to be related with the mobility degradation, which was evaluated by estimating $q\alpha_{sc}N_{ot}$ as a figure of merit, where α_{sc} is the scattering coefficient and N_{ot} the oxide trap density.

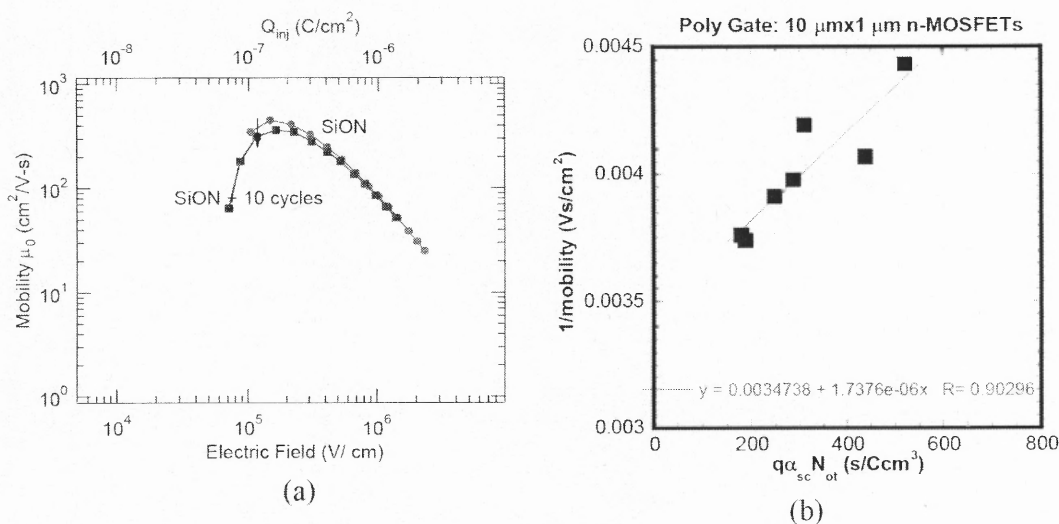


Figure 5.53 (a) Mobility Vs Electric Field (1 X-axis), Injected Charge (2 X-axis) for poly-Si devices with pure SiON and SiON with 10 cycles of HfO₂ (b) 1/mobility versus $q\alpha_{sc}N_{ot}$ – A figure of merit parameter.

Figure 5.53b shows the correlation between 1/mobility and the figure of parameter - $q\alpha_{sc}N_{ot}$ for poly-Si gate devices. For n-MOSFET, it is seen that $q\alpha_{sc}N_{ot}$ increases from its original value corresponding with pure SiON due to the addition of few cycles of

HfO₂. Koga *et al.* [107] assumed that the mobility is limited by the coulomb scattering of channel carriers by the trapped charge at the interface and in the dielectric (μ_{cit}) with $\mu_{cit} = 1 / \alpha_{sc} N_{IT} = \mu_{c0} \sqrt{N} / N_{IT}$, where N_{IT} is the number of occupied traps per unit area and μ_{c0} is a fitting parameter.

The effect of the gate-dielectric interface on 1/f noise using few cycles of HfO₂ has been studied. The presence of a small amount of HfO₂ at the top interface, thought responsible for the Fermi-level pinning, gives rise to a strong increase in the 1/f noise. Based on the experimental behavior reported here, the most straightforward explanation is that the existence of a high density of gate interface traps is causing a higher 1/f noise.

5.7 Substrate Effects – Si Vs GeOI

To determine the effects of substrate influence on 1/f noise, two different types of substrates were considered – Si and Ge. Processing was performed on 200 mm diameter GeOI substrates fabricated by the smart-cut process, as described elsewhere [108]. The gate dielectric stack process consists of several steps [108]. The wafers were first dipped in an HF-2% solution followed by a pre-bake step in H₂ to remove the native oxide from the Ge surface. A thin layer (~ 0.46 nm) of epitaxial Si was grown on the surface and was partially oxidized in N₂O plasma at room temperature to form a thin interfacial SiO₂ layer (IL). Next, 10 nm HfO₂ was deposited on top of the interfacial SiO₂ layer by Atomic Layer Deposition at 300°C. A TaN metal gate was made by Physical Vapor Deposition (PVD), on top of which a PVD TiN capping layer was deposited. Post-deposition annealing (PDA) was carried out in an O₂ environment at 400°C for 1 min. The thickness and doping density of the Ge layers were such that the fabricated transistors are partially

depleted. XPS measurements showed that the equivalent oxide thickness (EOT) of the formed interfacial SiO_2 layer was 0.65 nm. The total EOT of the gate stack was 2.7 nm based on standard C-V measurements. Figure 5.54 shows a TEM picture of the device without the metal gate formation.

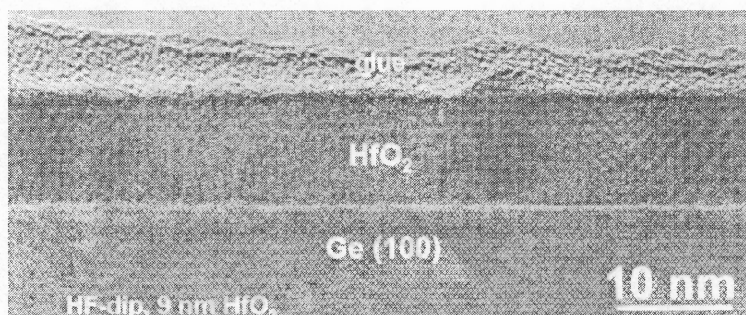


Figure 5.54 TEM photograph of a HfO_2 dielectric on a GeOI substrate, without the metal gate formation.

W/L = 10/1 μm n- and p-channel Si/ HfO_2 /TaN-TiN devices were also fabricated using a conventional CMOS process flow. In this case, a 0.8 nm thin interfacial layer obtained by an ozone treatment was first formed on top of which HfO_2 was deposited by a Metal Organic Chemical Vapor Deposition (MOCVD) process. The devices underwent decoupled plasma nitridation (DPN), similar to the N_2O treatment received by the Ge devices before the deposition of the metal electrode. The same TiN-TaN metal gate was deposited by PVD. These devices were post-deposition annealed in NH_3 at 800°C for 60s, followed by annealing in forming gas (FGA) at 520°C for 20 min. The equivalent oxide thickness of the device was estimated to be 2 nm.

The treatment of the interfacial layer of the Ge devices is certainly different when compared to the Si devices, mainly due to the lower stability of GeO_2 compared with SiO_2 . It has been shown earlier that for the same conventional silicon-like CMOS process

flow, the formation of an interfacial layer by an ozone-based process on GeOI substrates resulted in higher interface trap densities, which for sure will lead to much higher noise. For Si devices, it has also been demonstrated that the deposition technique (ALD Vs MOCVD) has no strong impact on the interface state densities in the high- κ layer; though a variation in noise mechanism is observed. However, Guo *et al.*, have recently reported results on improved processing on Ge-O-I based state-of-the transistors.

Figure 5.55 shows the transfer characteristics of both p-MOSFET and n-MOSFET for $|V_{ds}|$ of 1 V. The corresponding threshold voltage V_t is ~ 1.5 V (n-MOSFET) and ~ -0.5 V (p-MOSFET). A high off-state leakage current is observed for n-MOSFET, which is attributed to non-optimized dopant activation conditions, resulting in residual ion implantation damage in the depletion region of the substrate-drain area [110].

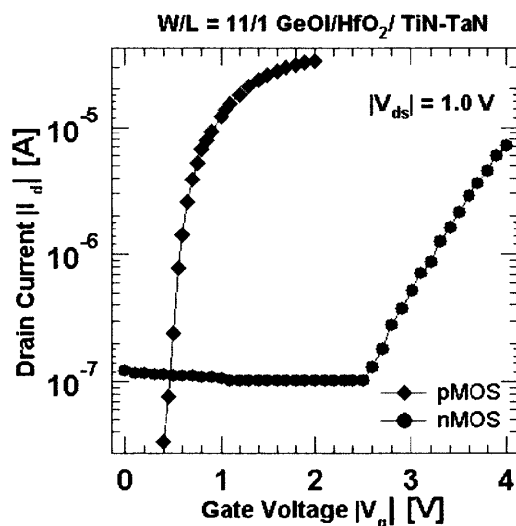


Figure 5.55 Transfer characteristics ($I_d - V_{gs}$) of $11 \mu\text{m} \times 1 \mu\text{m}$ n-MOSFET and p-MOSFET transistor on a GeOI substrate with a TiN-TaN/HfO₂ gate stack and fabricated by a conventional CMOS process flow.

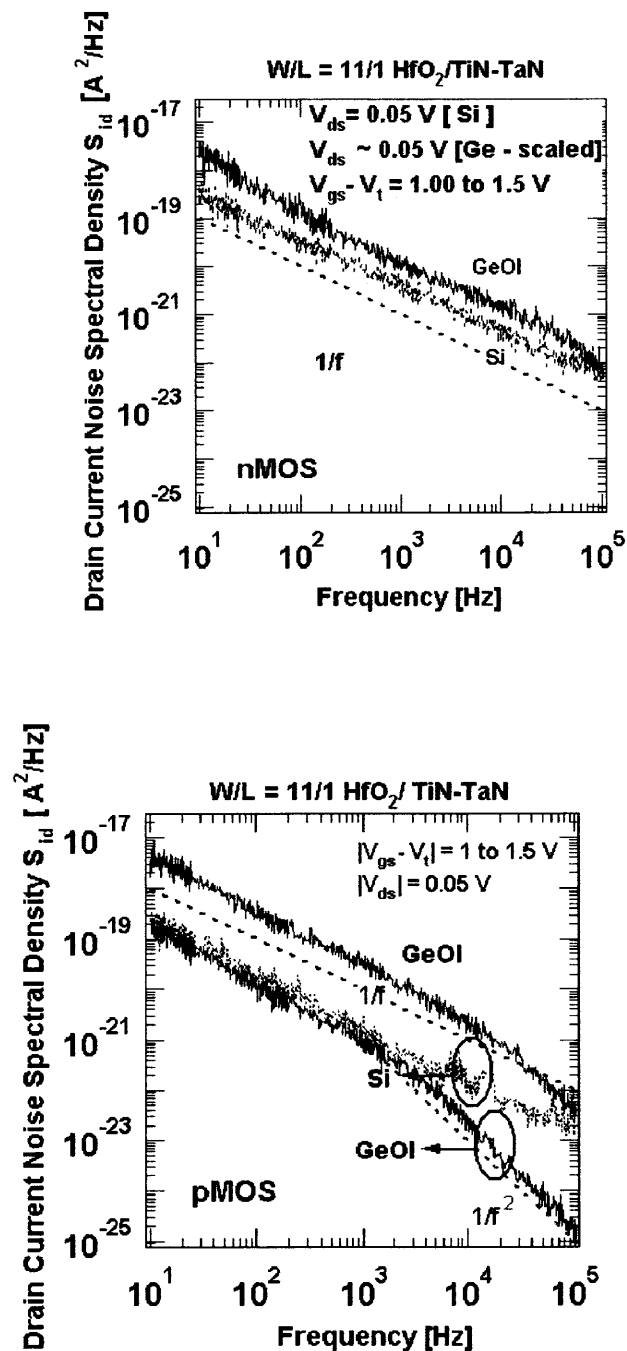


Figure 5.56 (a) Comparison of LF noise spectra at $|V_{ds}|=0.05$ V and $|V_{gs}-V_t| = 1.0$ to 1.5 V for HfO₂/TiN-TaN n-MOSFET (a) and p-MOSFET (b) devices on GeOI and Si substrates. To guide the eye, dotted lines are drawn according to $1/f$ or $1/f^2$.

Figure 5.56a shows LF noise spectra of n-MOSFETs processed on both Si and Ge substrates. A scaling of the V_{ds} has been taken into account, and the gate voltage overdrives of $|V_{GS} - V_T| = 1$ to 1.5 V. The noise performance of the p-MOSFETs is shown in Figure 5.56b.

It is seen that the LF noise spectra for n-MOSFET are of the $1/f^\gamma$ type, with a frequency exponent γ in the range 1.0 ~ 1.15. The p-MOSFET devices exhibit in addition, a Generation-Recombination (GR) component at higher frequencies, apart from $1/f^\gamma$. The occurrence of the GR component depends on the applied V_{DS} and is not seen in all p-MOSFET devices.

Comparing the GeOI and the silicon devices, two striking conclusions can be drawn: first, the current spectral density S_{id} is typically one order of magnitude higher for Ge substrates when compared to Si, for the same bias condition, second: no GR noise has been found in Si MOSFETs. This could point to the GeOI substrate as responsible for the GR noise: it has recently been reported [111] that Ge diffusion into SiO_2 gives rise to additional GR noise, like found in the p-MOSFETs shown in Figure 5.56b. The white noise of the devices is beyond the frequency range of the measurements. We also exclude an RC filtered junction shot noise as the origin of the Lorentzian spectrum as the device is operated in the linear regime for sufficiently low gate bias (~ 1.5 to 2 V).

An increase in $1/f$ noise in strained silicon n-MOSFETs was also ascribed to in-diffusion of Ge [112]. Ge in-diffusion has been observed in HfO_2 as well, when deposited by MOCVD [113]. However, for the case of ALD HfO_2 on germanium used in the studied devices, no in-diffusion is observed [114].

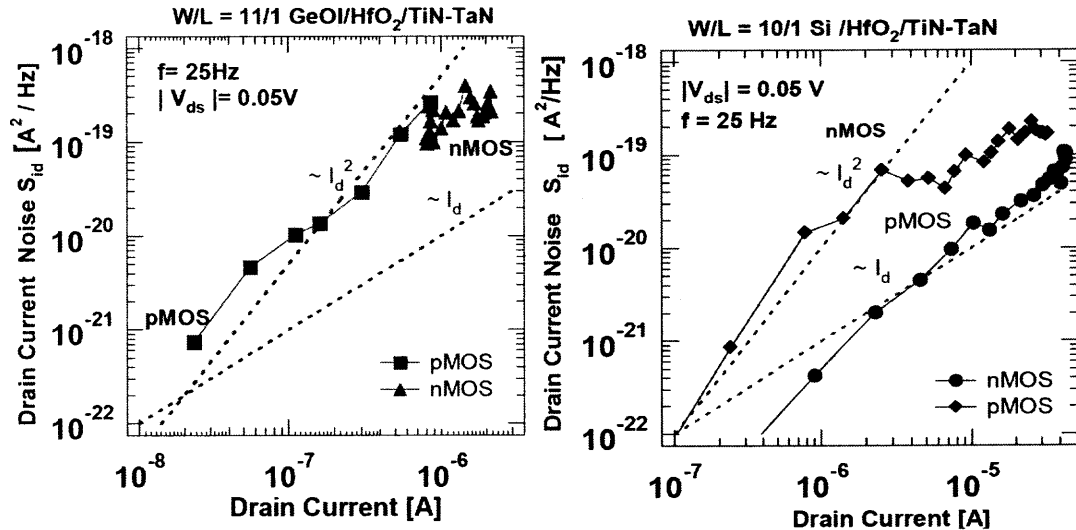


Figure 5.57 (a) Drain current spectral density (S_{id}) at $f=25$ Hz versus drain current $|I_d|$ for (a) $W/L = 11/1$ (μm) GeOI/HfO₂/TiN-TaN n- and p-MOSFETs, and (b) $W/L = 10/1$ (μm) Si/HfO₂/TiN-TaN n- and p-MOSFETs.

We conclude, therefore, that Ge traps in the gate oxide are an unlikely cause of the observed higher $1/f$ and GR noise in the devices studied here. The origin of the observed GR noise could be due to non-optimized dopant activation, leaving unannealed implantation damage in the drain depletion region. To investigate the origin of the $1/f$ noise, the S_{ID} dependence on the drain current $|I_D|$ at constant frequency ($f = 10$ Hz) is studied as shown in Figure 5.57a and is compared with Si devices ($f = 25$ Hz) in Figure 5.57b. For n- and p-MOSFETs Si devices, S_{ID} is found to be proportional to $|I_D|^2$ for low drain currents, while for high drain currents it is proportional to $|I_D|$. The same trend is also found for the n- and p-MOSFET GeOI devices. Further confirmation about the noise mechanism involved can be obtained from the normalized noise spectral density S_{id}/I_d^2 in Figure 5.58 which follows $[g_m/I_D]^2$. This points to a number-fluctuations origin. It is well known that number fluctuations in a device are caused due to carrier exchange with traps in the dielectric layer (border traps). Moreover, the input-referred noise spectral density

$S_{VG}=S_{ID}/g_m^2$ is constant with gate voltage overdrive in support of this interpretation. The peaks in Figure 5.58 are real and are caused due to variation in the frequency exponent γ at the given values of V_{gs} .

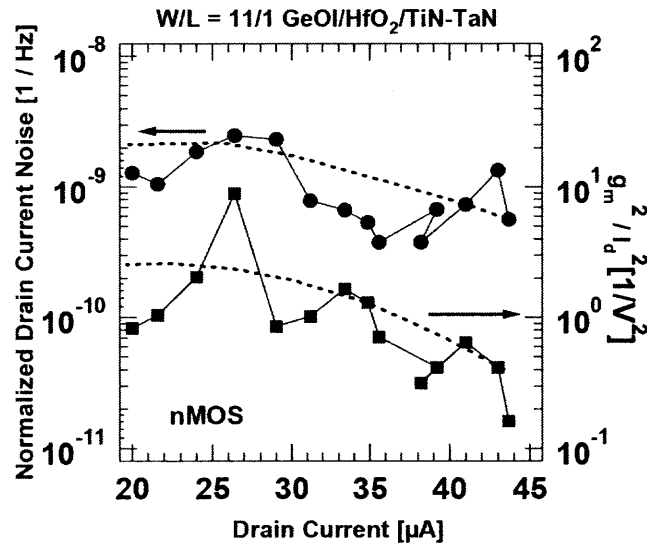


Figure 5.58 Normalized drain current spectral density S_{id}/I_d^2 (1° Axis; circles) and g_m^2/I_d^2 (2° Axis; squares) versus drain current I_d for a $W/L = 11/1$ (μm) GeOI/HfO₂/TiN-TaN n-MOSFET.

As the $1/f$ noise in GeOI MOSFETs is mainly due to trapping in the gate dielectric, an effective volume trap density N_T can be calculated from S_{VG} , based on Equation (5.2) where the oxide capacitance density $C_{EOT}=\epsilon_{ox}/EOT=1.29\times 10^{-6}$ F/cm², with ϵ_{ox} the permittivity of SiO₂, kT the thermal energy and f the frequency. The tunneling parameter α for the Ge substrate is calculated using the formula in Equation (5.3), where m^* is the effective mass in the HfO₂ dielectric ($=0.18m_0$ for HfO₂), h is Planck's constant, and ϕ_b is the Ge-HfO₂ barrier height, equal to 3.0 eV for electrons. The tunneling parameter is calculated to be $\sim 6.5\cdot 10^7$ cm⁻¹ and is smaller than for the Si/HfO₂ system. A

more correct calculation for α also considers the details of the IL, but the above value can be used in first approximation.

It is seen that the surface trap values (D_t) estimated using the formula ($4kTzN_t$), where z is the tunneling distance of an electron from the Ge/HfO₂ interface at $f=1\text{Hz}$, is found to be a few 10^{12} cm^{-2} for both n- and p-type devices, in the same range as the charge pumping values on similar devices as in Table VI. The values are approximately a factor 2 (p-) to 10 (n-MOSFET) higher than for Si/HfO₂/TiN-TaN devices.

The question at hand is why the $1/f$ noise in MOSFETs on a GeOI substrate is higher than on silicon material, for a similar gate stack processing. It is well known that $1/f$ noise is sensitive to traps in the gate dielectric at a few nm from the interface, so that the higher interface trap density observed in Ge MOSFETs is not responsible, when looking at the first instance. However, as shown before in, the $1/f$ noise of a HfO₂ transistor on silicon is a strong function of the IL thickness and the chemical composition of the high- κ layer. For the same high- κ layer thickness and chemical composition and a thinner IL, the $1/f$ noise increases significantly. The noise is also seen to vary with chemical composition of the high- κ layer. In our case, a comparison has been done for the same chemical composition (HfO₂). Simoen *et al.* [61] showed that higher noise is observed in devices with lower SiO₂ interfacial oxide thickness. In this case, higher noise ($\sqrt{S_{VG}}$) is observed for GeOI devices whose IL thickness (SiO₂) is 0.65 nm while for the Si devices, $\sqrt{S_{VG}}$ is approximately 1.5 times lower than GeOI as the IL thickness (SiO₂) is 0.8 nm. It has furthermore been established that for the same deposition conditions, a thinner IL results on a Ge substrate compared with silicon, given that there is an impact of metallic Hf layer in our devices during deposition.

Table 5.7 Comparison of Interfacial Layer Thickness (IL), Input Referred Noise PSD (S_{VG}), Volume (N_T) and Surface Trap (D_T) Densities for n- and p-MOSFET devices on GeOI and Si substrates. Comparison of Results Obtained from Charge Pumping (CP) and Noise Measurements are Also Shown for n- and p-MOSFET GeOI

Substrate	Channel	Interfacial layer thickness (nm)	$\sqrt{S_{VG}}_{ V_{GS}-V_{T1}=0.5}$ [V/ $\sqrt{\text{Hz}}$]	$WLS_{Vg}_{ V_{GS}-V_{T1}=0.5}$ ($V^2\mu\text{m}^2/\text{Hz}$)	N_T Volume Trap Density ($1/\text{cm}^3\text{eV}$)	D_T Surface Trap Density ($1/\text{cm}^2$)
Ge	p-MOSFET	0.65	3.0×10^{-5}	9.0×10^{-9}	1.4×10^{20}	5.5×10^{12}
						1.2×10^{12} (From CP)
	n-MOSFET	0.65	1.7×10^{-5}	2.8×10^{-9}	1.1×10^{20}	4.3×10^{12}
						3.1×10^{12} (From CP)
Si	p-MOSFET	0.80	7.2×10^{-6}	5.2×10^{-10}	6.0×10^{19}	3.1×10^{12}
	n-MOSFET	0.80	3.7×10^{-6}	1.4×10^{-10}	6.5×10^{18}	3.2×10^{11}

Combining these two facts, may explain the observed higher $1/f$ noise. In addition, considering the higher N_{it} , the quality of the IL on GeOI will be inferior compared with silicon, which may have an additional impact on the defectiveness of the HfO_2 layer deposited on it.

In conclusion, the LF noise of n- and p-MOSFETs with metal gate and HfO_2 on GeOI has a $1/f$ noise spectrum, dominated by carrier trapping in the gate dielectric. The noise power is 1~2 orders higher when compared to Si substrates. S_{VG} results show trap densities at least an order of magnitude higher when compared to Si-based devices. It is probable that the quality and thickness of the Ge/IL could be the major reason for higher values of the interface trap density and noise observed in both p- and n-MOSFET devices.

5.8 Temperature Effects

It has been earlier discussed in Chapter 2 and 3 that $1/f$ noise depends on temperature due to its relationship with energy. This chapter discusses about the effects of temperature on low-frequency noise in Hf-based MOSFETs. High temperature effects on low-frequency noise in HfO₂-based devices are discussed first followed by discussion on the effect of low-temperatures on Hf-silicate devices. SiON dielectric based devices are also compared for their $1/f$ noise performance at low temperatures. The outcome of these results is then used in Chapter 6 for modeling of drain current noise in Hf-based dielectrics.

5.8.1 Effect of High Temperature on $1/f$ Noise

This section deals with the effect of high temperature on $1/f$ noise in HfO₂ devices. The temperature of the device was increased from 25° C to 125° C as per the experimental described in earlier section 4.2.2. 10 μm x 1 μm HfO₂ devices were employed prepared by conventional CMOS process flow. A 0.8nm thin interfacial layer of SiO₂ following ozone chemistry was employed on the top of which HfO₂ was deposited by MOCVD process such that EOT of the devices were estimated to be approximately ~ 1.5 nm. TaN was used as the gate electrode while TiN was used as a capping layer. Post-deposition anneal were carried out at 800° C using NH₃ anneal while the post-metallization anneal was done in Forming Gas Anneal (FGA) environment at 520° C for 30 min.

5.8.2 Effect of High Temperature in HfO₂ n-MOSFETs

Figure 5.59 shows I_D - V_G and G_M - V_G characteristics of TiN-TaN/HfO₂ n-MOSFETs at 298K and 398K. The threshold voltage is seen to shift by 0.30 V towards left and the peak transconductance degrades by $\sim 30\%$. This gate voltage shift is also seen in the G_M - V_G characteristics. It has been investigated earlier that the transconductance degradation in HfO₂ devices are mainly due to larger lattice vibrations interfering with the channel carriers during current transport [115].

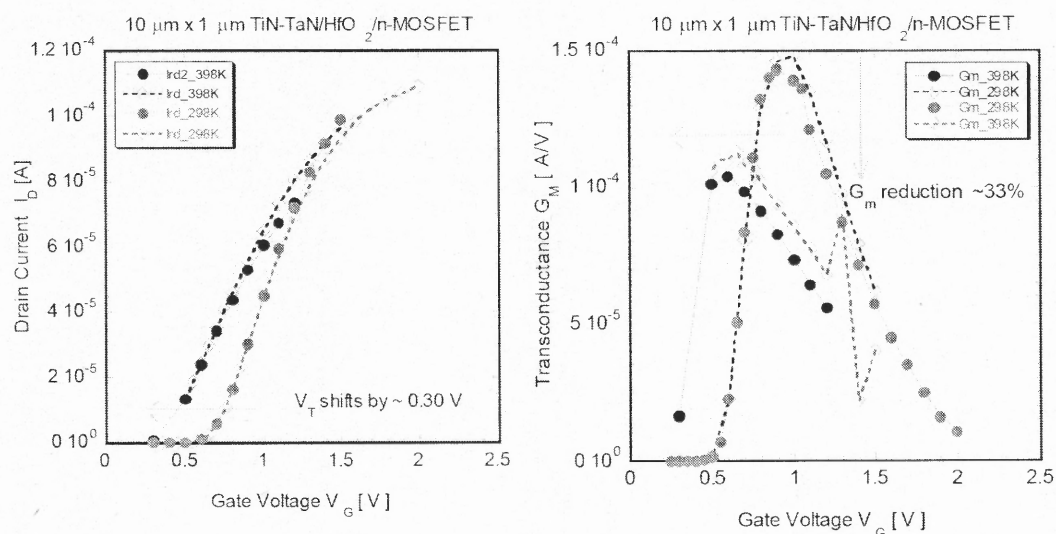


Figure 5.59 I_D - V_G and G_M - V_G characteristics of HfO₂ devices at 298K and 398 K.

Figure 5.60 shows the I_G - V_G characteristics of the device. The gate current increases by a magnitude of half-order, indicating the possibility of Poole-Frenkel [116] conduction mechanism being dominant.

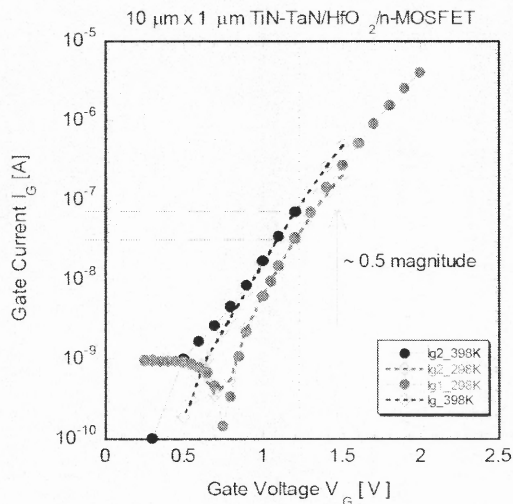


Figure 5.60 I_G - V_G characteristics of TiN-TaN/HfO₂ devices at 298K and 398 K.

Figure 5.61 shows the Drain Current Noise Spectral Density S_{ID} Vs Frequency f for HfO₂ devices at 298K and 398K. Typically $1/f$ nature is observed for both temperature conditions and is seen that the S_{ID} decreases near to an order of magnitude as the temperature increases for a given $|V_{GS} - V_T| \sim 0.12$ V and $|V_{DS}| \sim 0.05$ V value.

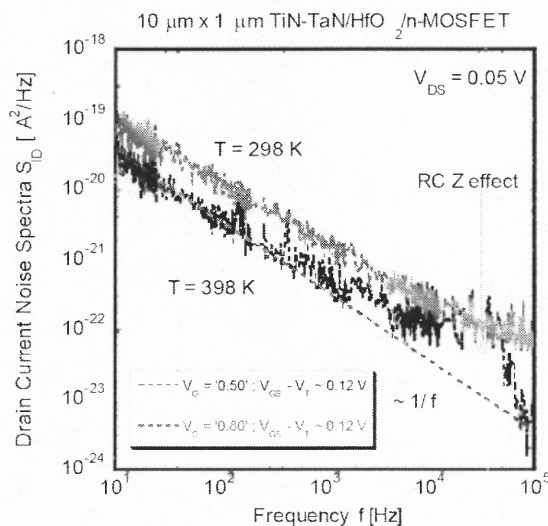


Figure 5.61 Drain Current Noise Spectral Density Vs Frequency for TiN-TaN/HfO₂ devices at 298K and 398 K.

The RC effects are noticed for S_{ID} spectra at 398K, mainly due to the usage of longer cables as the access to temperature system was limited.

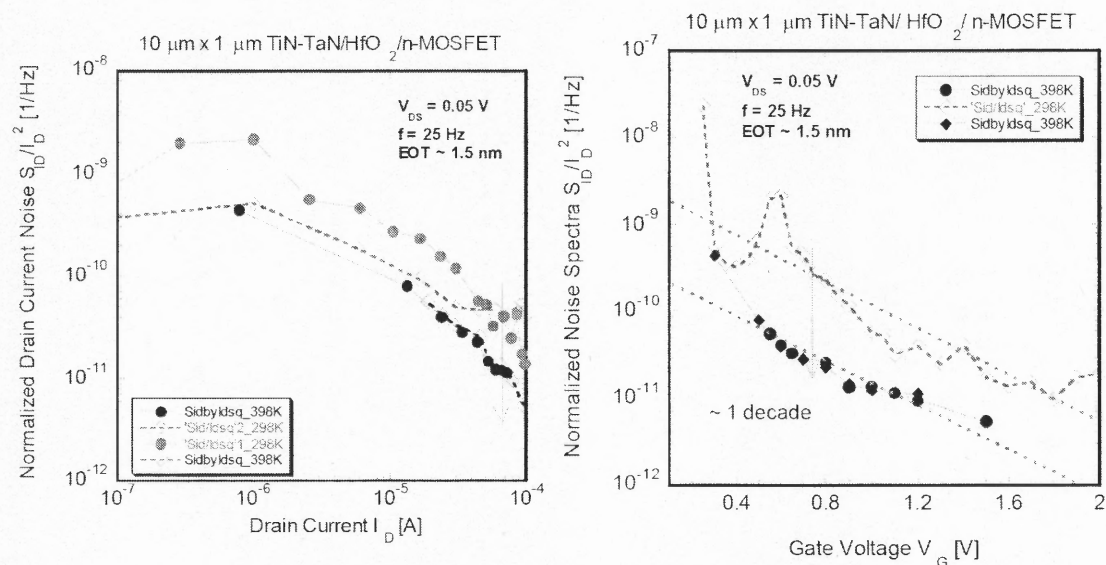


Figure 5.62 Normalized Drain Current Noise Spectral Density Vs Drain Current for TiN-TaN/HfO₂ devices at 298K and 398 K.

Figure 5.62 shows the noise spectral density normalized with the square of the drain current plotted against the measured drain current values. Two main observations were noticed – (i) the normalized noise show lower values at higher temperatures by $\sim 8\text{X}$ close to an order of magnitude (ii) a weak plateau is observed at lower drain currents followed by roll-off at higher drain currents which is a signature of number fluctuation theory. Moreover the curves for both the temperatures are seen to be almost parallel indicating no variation in the noise mechanism. The normalized noise behavior with gate voltage variation as seen in Figure 5.62 confirms the same.

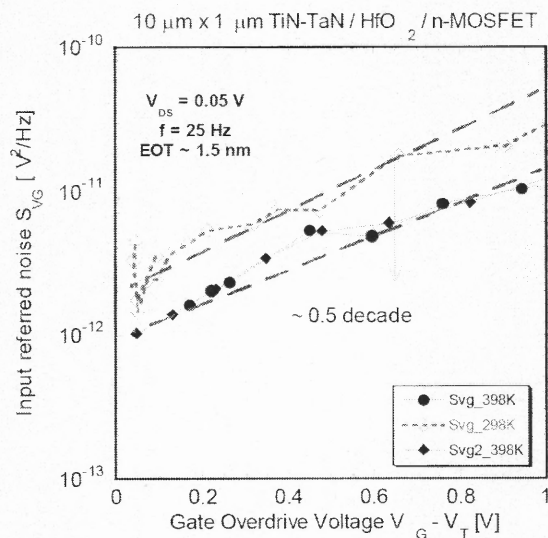


Figure 5.63 Input Referred Noise Vs Gate Voltage Overdrive for TiN-TaN/HfO₂ devices at 298K and 398 K.

Figure 5.63 shows input referred noise S_{V_G} for variation in gate voltage overdrive $V_G - V_T$. While the S_{V_G} values lower by half-a decade for a Δ change of 100 C, the noise dependencies on gate voltage overdrive clearly points out that trapping is the origin of noise at high temperatures in metal gate hafnium oxide based n-MOSFET devices.

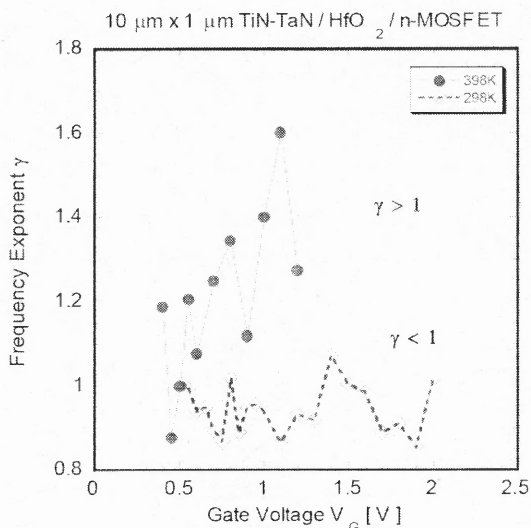


Figure 5.64 Frequency exponent γ Vs Gate Voltage V_G at 298K and 398K for TiN-TaN/HfO₂/n-MOSFETs.

Figure 5.64 shows the frequency exponent variation with gate voltage for the HfO_2 MOSFETs at both the temperatures. The variation in frequency exponent is related to temperature via Equation (3.1). Significant observations are made from Figure 5.64 – (i) the frequency exponent variation at room temperature is almost independent of gate voltage and the values are found to be lower than 1 (ii) the frequency exponent variation is quite strongly dependent on applied gate voltage and tends to show an increasing value as the gate voltage increases. Moreover the values are found to be greater than 1. This could possibly imply a variation in both trap distribution profile and energy level of the defects involved in $1/f$ noise. This is mainly due to the observed differences in frequency exponent and the gate voltage dependence respectively as possibly shown in Figure 5.65.

At room temperature, the trap distribution can be such that a greater number of high-frequency traps may be present near the IL-substrate interface, while the trap distribution at 398K may be such that a greater number of low-frequency traps are present in the HfO_2 layer away from the IL-substrate interface.

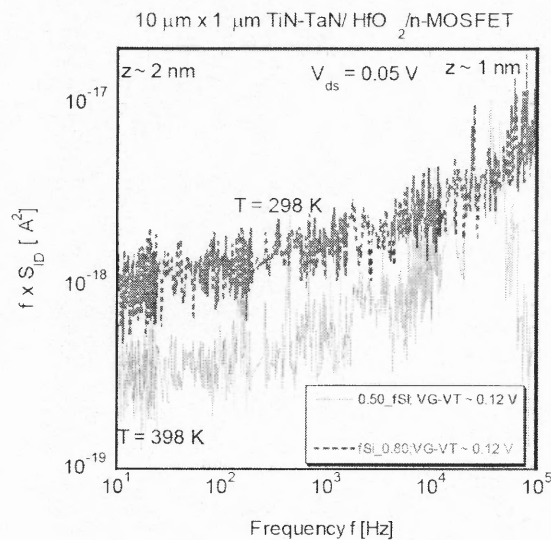


Figure 5.65 $f \times S_{ID}$ Vs frequency at 298K and 398K for TiN-TaN/ HfO_2 /n-MOSFETs.

5.8.3 Effect of Low Temperature 1/f Noise

This section deals with the effects on 1/f noise at low temperatures down to liquid nitrogen temperatures. Four sets of devices were used to understand the temperature dependency on low-frequency noise, the details of which are tabulated below:

Type 10 μm x 1 μm	Gate Dielectric	EOT	Processing condition
n-MOSFETs	Hf/Si ~ 55/45	~ 1.4 nm	NH ₃ 800°C anneal PVD TiN/TaN metal gate electrode
	SiON	~ 1.6 nm	NH ₃ 800°C anneal PVD TaN metal gate electrode with poly-Si gate over top.
p-MOSFETs	Hf/Si ~ 55/45	~ 1.4 nm	NH ₃ 800°C anneal PVD TiN/TaN metal gate electrode
	SiON	~1.7nm	NH ₃ 800°C anneal ALD TiN/TaN metal gate electrode

The measurement setup and the conditions were explained in detail earlier in Chapter 4, Section 3.

5.8.4 Low Temperature 1/f Noise in SiON and Hf-silicate n- MOSFETs

The first half deals the low temperature effects on Hf-silicate n-MOSFETs. Figure 5.66 shows the drain current spectra of both SiON and HfSiON devices for temperatures from 77K to 300K for a given $|V_{GS}-V_T| \sim 0.1$ V and $|V_{DS}| \sim 0.05$ V.

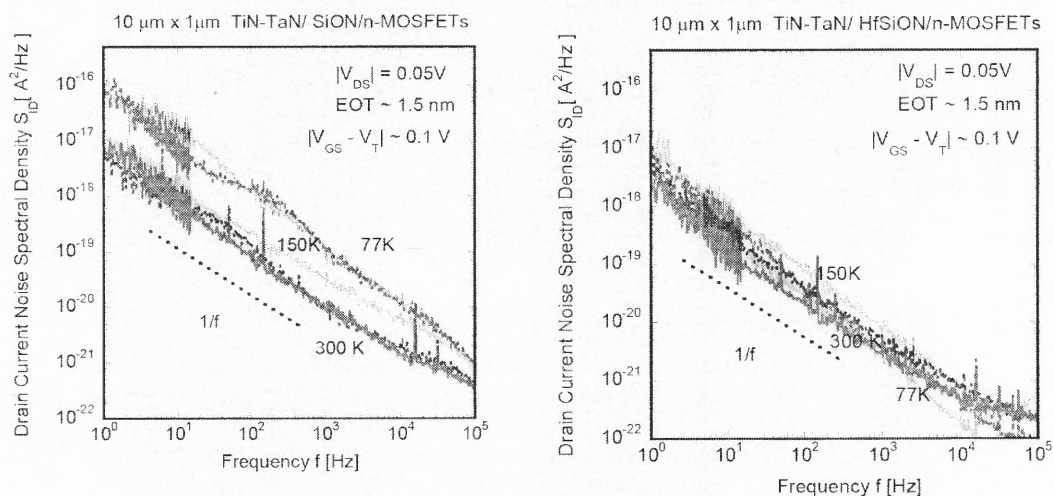


Figure 5.66 Drain Current Noise Spectral Density Vs Frequency for SiON and Hf-silicate n-MOSFETs for temperatures from 77K to 300K.

For SiON devices, the temperature dependence is clearly seen where 1/f noise increases by more than a decade when temperature reduces from 300K to 77K. But in the case of Hf-silicate devices, no such clear increase is noticed, where S_{ID} spectra have similar values for different temperatures. This is clearly evident in Figure 5.66 where the increase in 1/f noise is evident for SiON devices when the temperature decreases from 300K to 77K. Moreover, it is also seen that 1/f noise in HfSiON has comparatively lower values than SiON MOSFETs. This is due to the fact that these devices are found to suffer from leakage currents higher than expected for a typical SiON device.

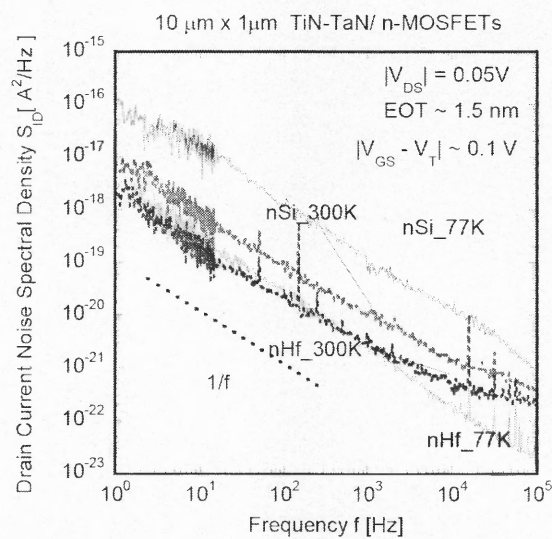


Figure 5.67 Drain Current Noise Spectral Density Vs Frequency for SiON and Hf-silicate n-MOSFETs for temperatures from 77K to 300K.

For a right comparison, the spectral values are normalized with square of the drain current and plotted for drain current as shown in the Figure 5.67 for both SiON and HfSiON devices. For both the cases, S_{ID}/I_D^2 increase as the temperature reduces from 300K to 77K. For a given drain current ($10^{-4} A$), the difference in normalized noise S_{ID}/I_D^2 is two orders of magnitude higher at 77K when compared to 300K, while for HfSiON devices the differences are reduced. Moreover, for SiON devices, the normalized values are proportional to $\sim 1/I_D^2$ for all the temperature values studied. The curves for all the temperatures run almost parallel indicating that trapping could be the origin of $1/f$ noise, independent of temperature. But this is not the case for HfSiON devices, where the normalized values are proportional to $\sim 1/I_D$ for temperatures below 150 K, indicating that the noise mechanism is related to scattering effects rather than trapping. As the temperature increases, the behavior gradually shifts from mobility fluctuations to correlated number fluctuations, since the S_{ID}/I_D^2 dependency shift from $1/I_D$ to $1/I_D^{1.5}$.

This is quite clearly evident when both SiON and HfSiON devices are plotted together as shown in Figure 5.67. This behavior also means that the noise mechanism in metal-gate/Hf-based devices is a function of temperature in n-MOSFETs.

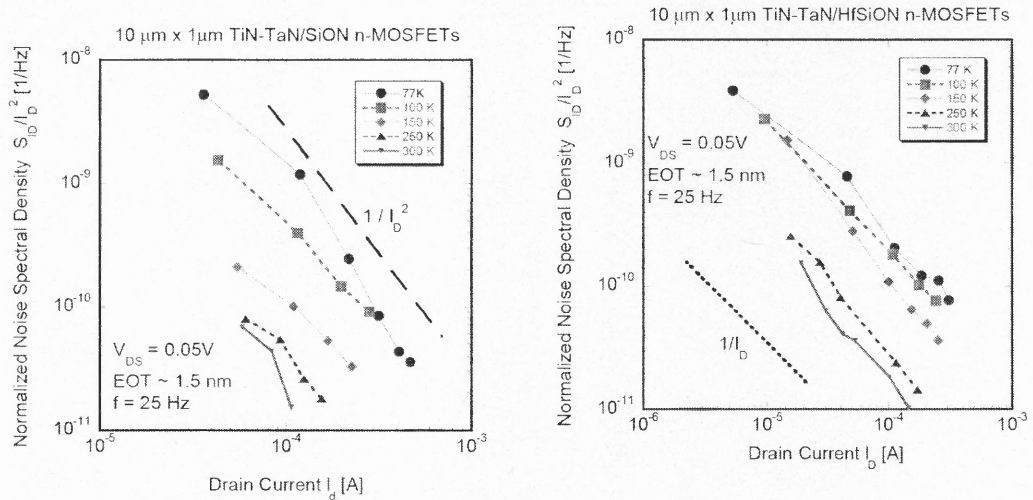


Figure 5.68 Normalized Noise spectral density S_{ID}/I_D^2 Vs Drain Current I_D for SiON and HfSiON n-MOSFETs for temperatures from 300K to 77K.

It is also observed from Figure 5.68 that the normalized noise values are more or less comparable between SiON and HfSiON devices even at 77K as earlier observed in 300K also.

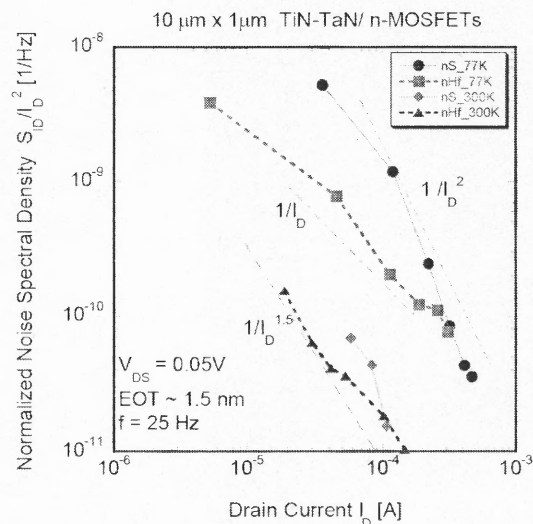


Figure 5.69 Normalized Noise spectral density S_{ID}/I_D^2 Vs Drain Current I_D for SiON and HfSiON n-MOSFETs for temperatures 77K and 300K.

Figure 5.70 shows the input referred noise variation S_{VG} with respect to gate voltage overdrive $|V_{GS} - V_T|$ for SiON and HfSiON devices. In the case of SiON devices, the S_{VG} values increase by one order of magnitude as the temperature reduces from 300K to 77K. Moreover, the values are seen to be almost independent of gate voltage overdrive, which is a signature of number fluctuation theory supporting the earlier conclusion based on the normalized noise values. In the case of HfSiON, the S_{VG} values also increase as the temperature reduces. However this increase comes in a non-linear fashion, where the increase in S_{VG} for decrease in temperature is not the same. Similar values are noticed for lower temperatures (between 77K to 150K), while lower values were noticed for 250K and 300K. The S_{VG} values also show a strong dependence on $|V_{GS} - V_T|$, an indication on the theory of mobility fluctuations [46].

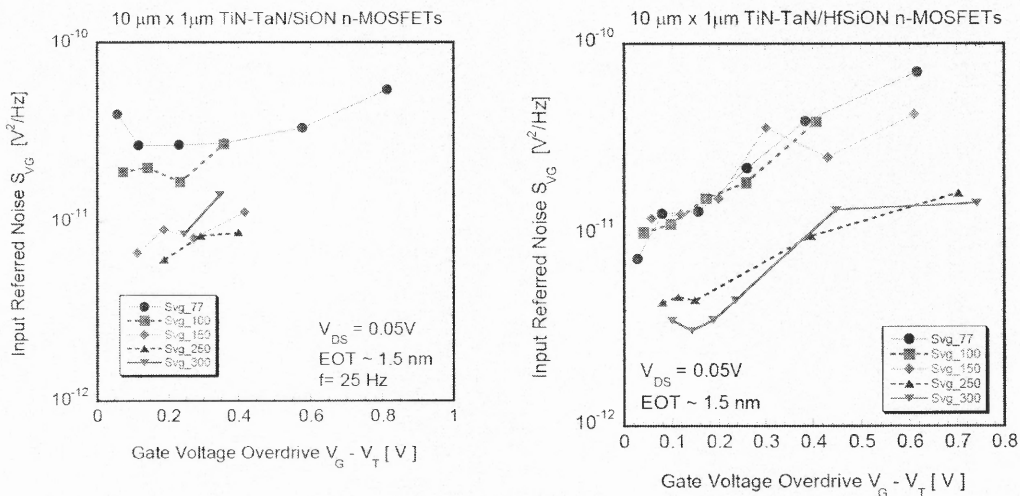


Figure 5.70 Input referred noise Vs Gate voltage overdrive for SiON and HfSiON n-MOSFETs for temperatures from 300K to 77K.

Figure 5.71 shows the comparison graph for input referred noise with gate voltage overdrive at 77K and 300K for SiON and HfSiON devices.

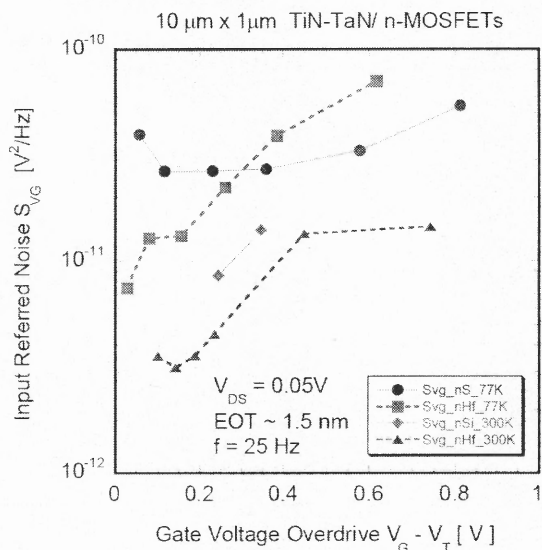


Figure 5.71 Input referred noise S_{VG} Vs Drain Current I_D for SiON and HfSiON n-MOSFETs for temperatures 77K and 300K.

The S_{VG} dependence on gate voltage overdrive $|V_G - V_T|$ is quite evident for Hf-silicate devices whereas it is almost independent for SiON devices at 77K, confirming that mobility fluctuations are dominant over number fluctuations in HfSiON devices at lower temperatures, whereas at room temperatures, the dependency shifts for both the devices and is found to support the theory on correlated mobility-number fluctuations [39], which is in accordance to earlier obtained results at room temperatures.

5.8.5 Low temperature 1/f noise in SiON and Hf-silicate p-MOSFETs

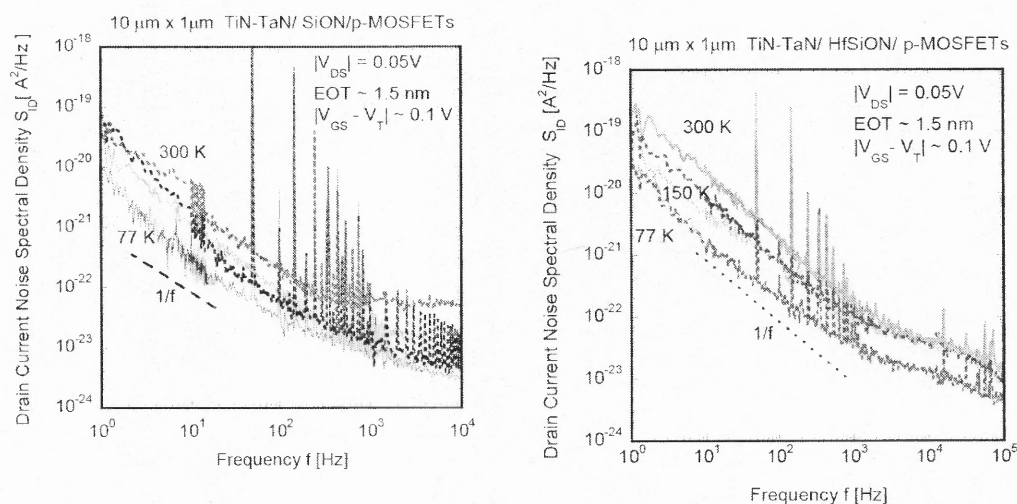


Figure 5.72 Drain Current Noise Spectral Density Vs Frequency for SiON and Hf-silicate p-MOSFETs for temperatures from 77K to 300K.

Figure 5.72 shows the drain current noise spectral density Vs frequency for SiON and HfSiON n-MOSFETs for temperatures from 77K to 300K for $|V_{GS} - V_T|$ of 0.1 V. 1/f type spectra are observed for frequencies lower than 1 KHz for both the cases. The spikes observed here are due to the interference from the power lines and hence we obtain them as harmonics of 60Hz. In the case of SiON devices, the variation in 1/f noise is minimal for variation in temperature. In the case of HfSiON devices, a clear dependence is noticed

where $1/f$ noise decreases with increase in temperature. These differences are quite visible if the plot of SiON and HfSiON devices are compared in the same graph for the temperatures 77K and 300K as shown in the Figure 5.73.

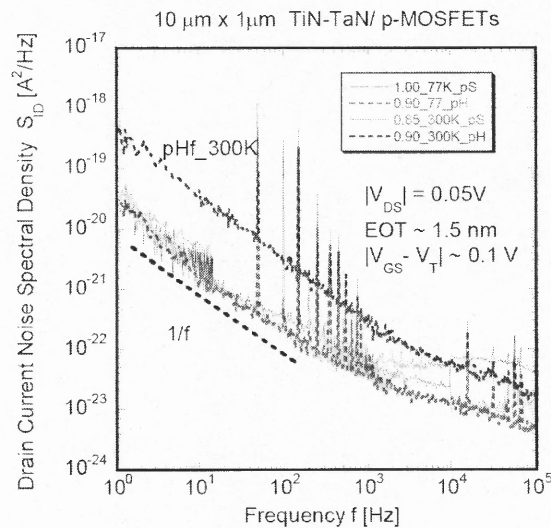


Figure 5.73 Drain Current Noise Spectral Density Vs Frequency for SiON and Hf-silicate p-MOSFETs for temperatures from 77K to 300K.

To understand the noise mechanism in these devices, the normalized noise spectral density is plotted for variation in drain current for both SiON and HfSiON p-MOSFETs as shown in Figure 5.74. In the case of SiON devices, S_{ID}/I_D^2 is proportional to $\sim 1 / I_D$ for all the temperatures studied, indicating that mobility fluctuations could be the possible origin. It has been earlier proved in SiON p-MOSFETs that mobility fluctuations are the possible origin of $1/f$ noise at room temperature which confirms the general observation. In this case, no variation in noise mechanism is observed as the temperature varies. Moreover, the variation in normalized noise is found to be minimal where the values are almost comparable for 77K and 300K at higher drain currents.

HfSiON devices show a different case, where the noise mechanism is found to be dependent on the temperature. At room temperature the normalized noise is seen to be proportional to $\sim 1 / I_D$, indicating that mobility fluctuations could be the origin of noise. This also confirms to our earlier observation in metal gate devices that mobility fluctuations could be the origin of $1/f$ noise in p-MOSFETs.

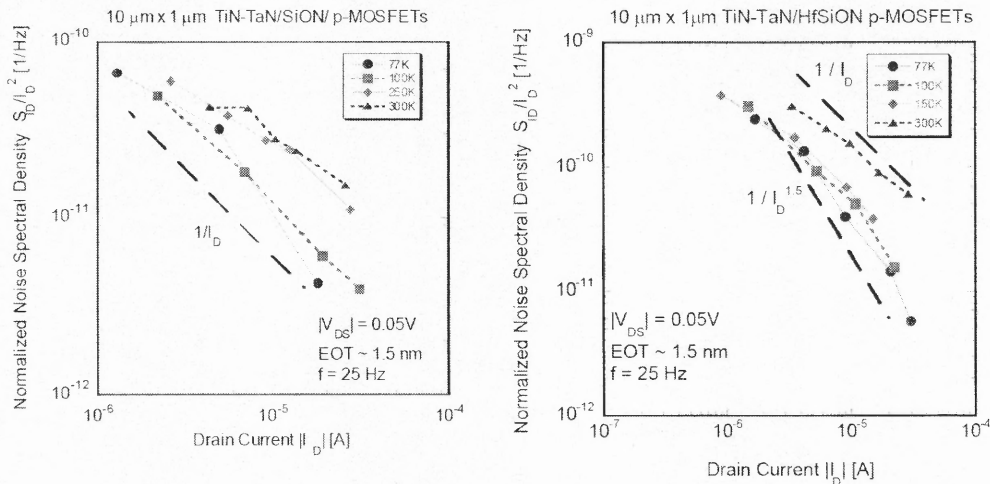


Figure 5.74 Normalized Drain Current Noise Spectral Density Vs Drain Current for SiON and Hf-silicate p-MOSFETs for temperatures from 77K to 300K.

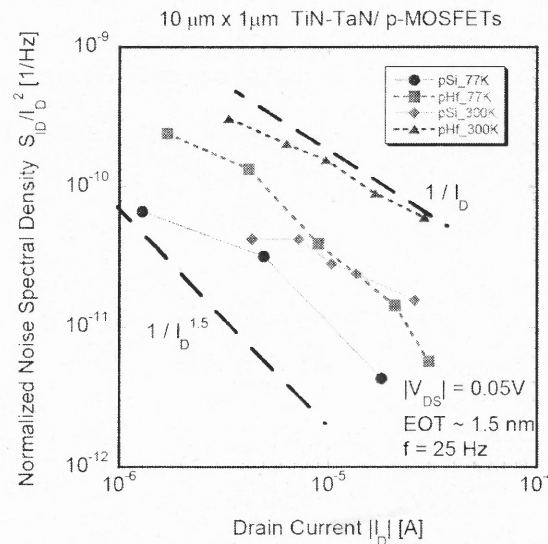


Figure 5.75 Normalized Drain Current Noise Spectral Density Vs Drain Current for SiON and Hf-silicate p-MOSFETs for temperatures for 77K and 300K.

As temperature reduces, the noise dependency is seen to shift from $\sim 1/I_D$ to $1/I_D^{1.5}$ indicating a possible change in noise mechanism from pure mobility fluctuations to correlated theory on number fluctuations.

This is more evident when the S_{ID}/I_D^2 is plotted for I_D for SiON and HfSiON devices in the same graph as shown in Figure 5.76 for 77K and 300K. Another observation from the figure is that the normalized noise is significantly higher in Hf-silicate p-MOSFET devices than SiON devices for both 77K and 300K. Moreover, unlike SiON devices, the variation in normalized noise values may be significant between 77K and 300K in HfSiON devices.

To confirm the noise mechanism and its origin observed from normalized noise values, the input referred noise is plotted as a function of gate voltage overdrive as shown in the Figure 5.76.

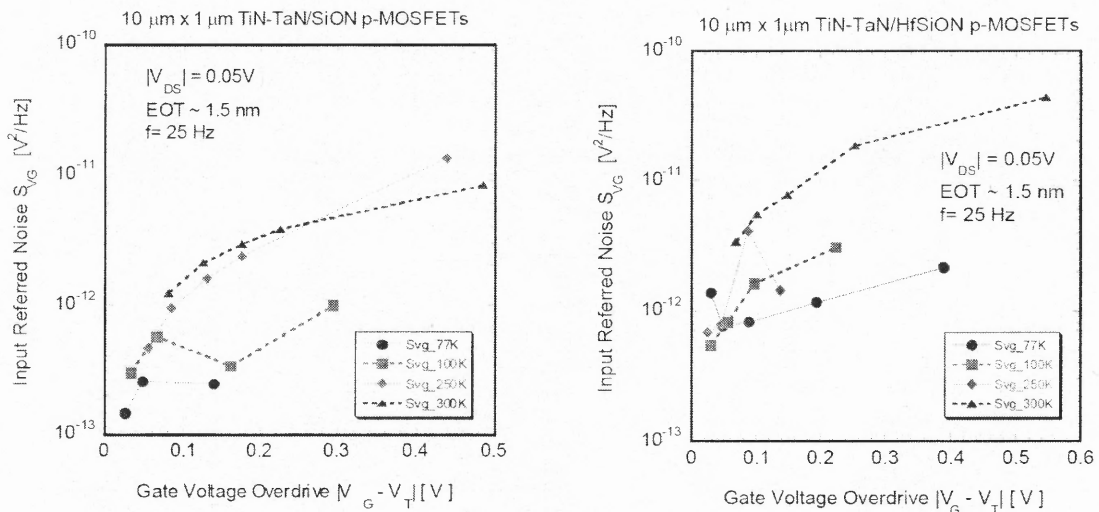


Figure 5.76 Input referred noise Vs gate voltage overdrive for SiON and Hf-silicate p-MOSFETs for temperatures from 77K to 300K.

In the case of SiON devices, the input referred noise values are found to be dependent on $|V_G - V_T|$ for 250 K and 300 K, a signature of mobility fluctuation theory [46] whereas the dependence on gate voltage overdrive is not clearly seen at lower temperatures. But in general an increasing trend may be predicted, which may indicate that scattering effects are more dominant than trapping in these devices. For HfSiON devices, this may not be the case, where $|V_{GS} - V_T|$ dependence is pre-dominantly noticed at 300K whereas it is more or less constant at 77K. This is more evident in the Figure 5.77, where at 300K, S_{VG} increases with gate voltage overdrive whereas the increase is minimal at 77K. Moreover one can also observe that the S_{VG} differs almost by an order of magnitude between 77K and 300K for SiON and HfSiON devices, unlike normalized noise values. This may be due to higher G_M variation in SiON devices between the observed temperatures.

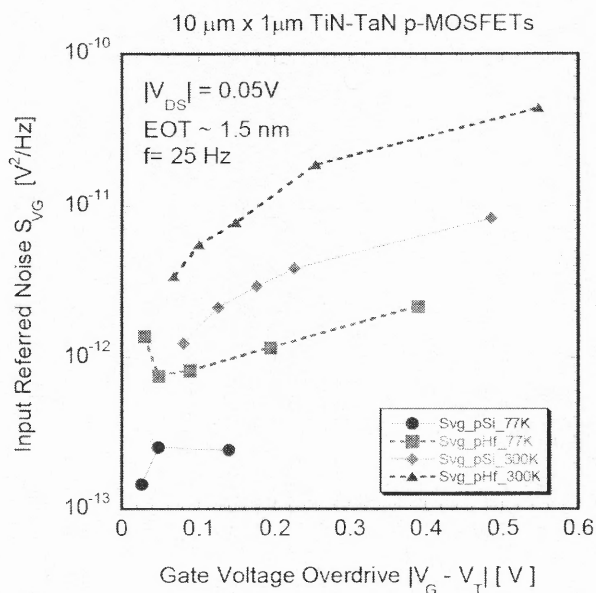


Figure 5.77 Input referred noise Vs Gate voltage overdrive for SiON and Hf-silicate p-MOSFETs for temperatures for 77K and 300K.

From these results it is seen that the noise behavior and mechanism is completely different for HfSiON devices for both n- and p-MOSFETs at low and high temperatures when compared to SiON devices. The results indicate that these devices are more sensitive to temperature resulting in $1/f$ noise being a strong function of temperature. This would mean that the activation energy levels [67] would vary when compared to SiON devices. It becomes necessary then to estimate these energy levels to identify the exact values involved in $1/f$ noise. More detailed analysis and the estimates of the energy levels involved in $1/f$ noise mechanism in the devices are needed which could be considered as a future work.

5.8.6 Guidelines for reduced $1/f$ noise in future CMOS devices

As a guideline for consideration of Hf-based CMOS devices for future technology nodes (45nm and beyond), the following gate technological and processing parameters are recommended for both n-and p-MOSFETs reduced $1/f$ noise in mixed-signal and analog applications:

- (1) Optimal thickness of the interfacial layer – 0.8nm
- (2) Thickness of the high-k layer – 1.5nm to 3.0nm
- (3) Type of anneal – Interface-Nitridation Anneal followed
by any type of Post-Deposition Anneal
- (4) Gate Electrode – Fully Silicided (NiSi)
- (5) Gate Oxide Material – HfO_2
- (6) Substrate – Si

If a metal gate electrode need to be used, TaN-the mid gap metal show lower noise compared to other types of electrodes, while TiN acts as a capping layer. The type of gate processing would be a Physical Vapor Deposition process.

CHAPTER 6

NOISE MECHANISMS AND MODELING

Based on the observations in Chapter 4 and Chapter 5, the low-frequency noise in Hf-based high- κ gate stacks is modeled. The limitations imposed by the present noise mechanisms are discussed first; following with some of the basic parameters for high- κ gate stacks are re-estimated. The drain current noise model is then formulated based on the above re-estimated parameters for high- κ gate stacks.

6.1 Limits of Noise Mechanism in Thin Gate SiON MOSFETs

The drain current noise spectral density S_{ID} in most cases follows I_D^2 dependence for lower currents for n-MOSFETs, as found in Figures 6.1 and 6.2. The metal or NiSi gate nMOSFETs exhibit similar S_{ID} values in Figures 6.1 and 6.2, compared with poly-gate. The normalized current spectral density is compared with $(g_m/I_D)^2$ as shown in Figure 6.3 and exhibit two cases: for the NiSi gate device, both characteristics are parallel for most of the drain current range, while for poly gate, there is a strong difference between the two curves. In the NiSi case, the $1/f$ noise behavior is likely due to trapping, while for poly-Si, $1/f$ noise behavior may not be completely due to trapping, particularly in strong inversion.

For the n-MOSFET transistors studied, the foundations of the number fluctuations theory have to be reconsidered, since the physical gate oxide thickness of 1.5 nm corresponds to a frequency of ~ 1 kHz. Moreover, the plot of $(LS_{VG})^{0.5}$ versus the gate voltage overdrive ($V_{GS}-V_T$) in Figure 6.4, show a discernible difference between the three

cases studied. The NiSi transistor exhibits a flat behavior at lower $|V_{GS}-V_T|$ values, indicating negligible correlated mobility fluctuations, while a pronounced $V_{GS}-V_T$ dependence is noticed for the poly-gate transistors. This suggests that the gate electrode has a strong impact on the $1/f$ noise characteristics of 1.5 nm SiON devices, both in weak and in strong inversion, which cannot be explained in the frame of the available classical models. For deep submicron devices, the mobility fluctuations due to remote charge and phonon scattering [62] should be considered in the model for adequately explaining the $1/f$ noise behavior. The difference in screening of the fluctuating charges at the gate interface may explain the strong impact of the gate material reported here.

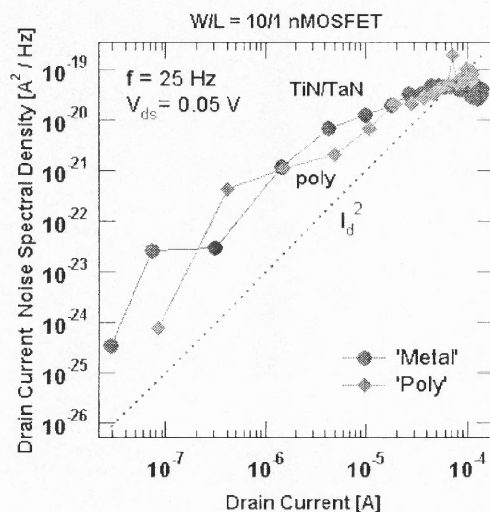


Figure 6.1 Drain current noise spectral density S_{ID} versus I_D for the same transistors, for $f=25$ Hz and $V_{DS}=0.05$ V.

The question that remains to be answered is the origin of the LF fluctuations at the gate-oxide interface charges. One possible explanation is the image charge that is induced at the gate/SiON interface by a charge trapped in the oxide.

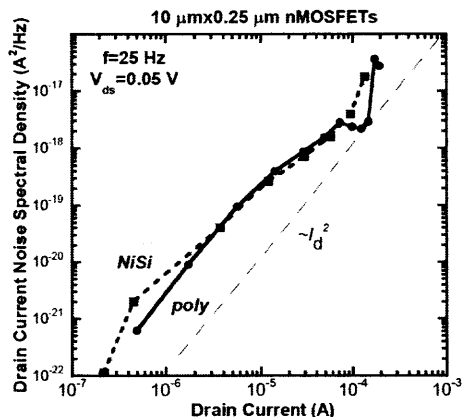


Figure 6.2 S_{ID} versus I_D for a $10\ \mu\text{m} \times 0.25\ \mu\text{m}$ n-MOSFET with fully-silicided (NiSi) and poly gate for 1.5 nm SiON n-MOSFET.

If this is not screened properly, it will induce additional shifts in the threshold (or flat-band) voltage and, hence, number fluctuations and in addition, can cause extra remote scattering (mobility fluctuations). The results on the poly-gates seem to pinpoint the latter mechanism as responsible for the higher noise.

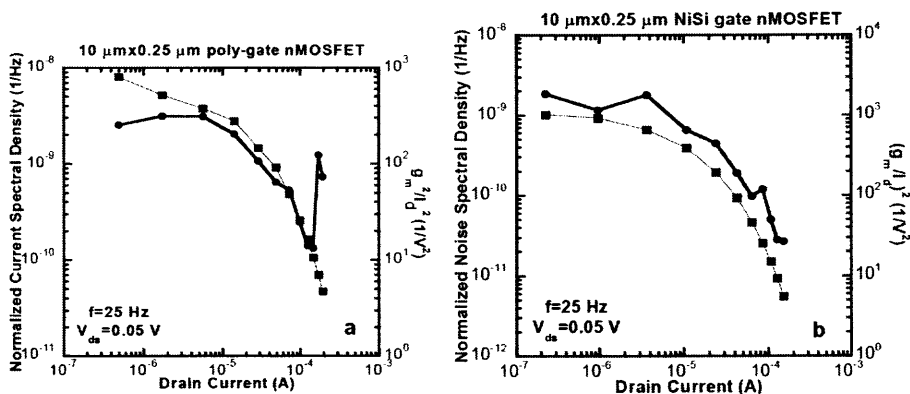


Figure 6.3(a) Normalized current noise spectral density ($f=25\ \text{Hz}$) and $(g_m/I_D)^2$ at $V_{DS}=0.05\ \text{V}$ for a $10\ \mu\text{m} \times 0.25\ \mu\text{m}$ poly gate n-MOSFET. **(b)** Normalized current noise spectral density ($f=25\ \text{Hz}$) and $(g_m/I_D)^2$ at $V_{DS}=0.05\ \text{V}$ for a $10\ \mu\text{m} \times 0.25\ \mu\text{m}$ NiSi gate n-MOSFET.

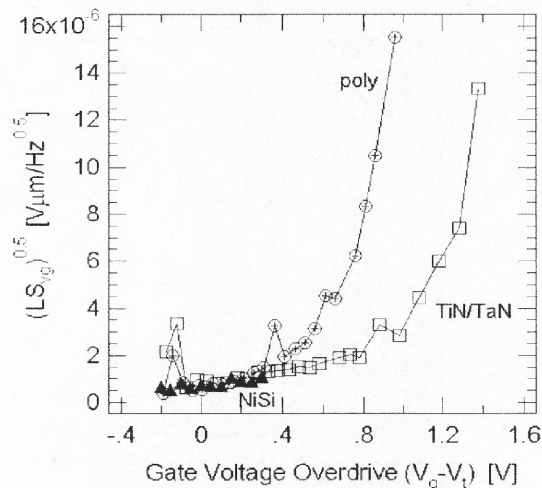


Figure 6.4 Square root of the normalized input-referred noise spectral density versus gate voltage overdrive for different gate materials for 1.5 nm SiON n-MOSFET.

6.2 Scaling Effects on 1/f Noise

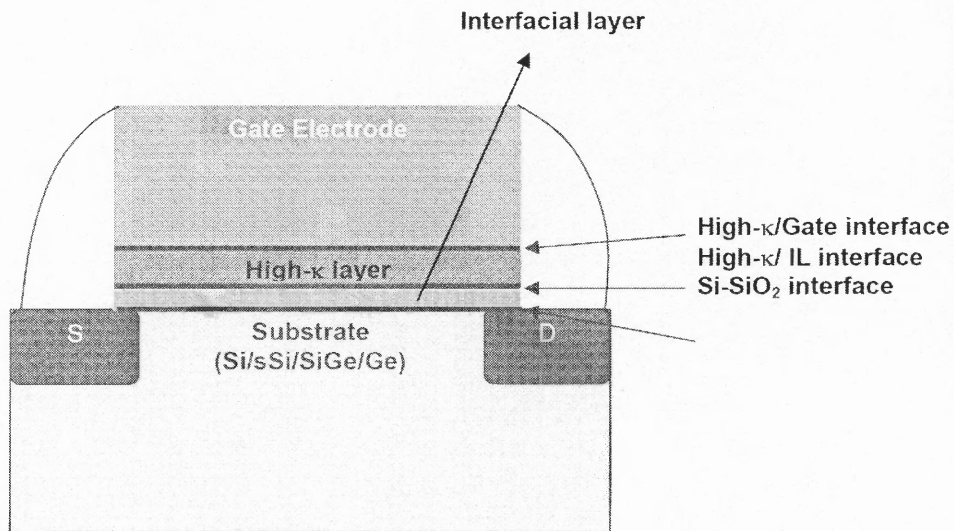


Figure 6.5 A typical high- κ MOSFET structure showing the influence of various scaling elements affecting the 1/f noise performance. Eight major technological parameters are identified which can have a significant impact on 1/f noise.

Figure 6.5 shows the typical scaling elements that may affect the 1/f noise. These factors are

- (1) Si-SiO₂ interface
- (2) Interfacial layer (SiO₂) oxide thickness - t_{IL}
- (3) High- κ gate dielectric thickness - $t_{high-\kappa}$
- (4) Overall Equivalent Oxide Thickness (EOT)
- (5) Gate Electrode
- (6) Gate Electrode/High- κ interface
- (7) κ -value of the high- κ oxide layer, and
- (8) Nature of Substrate.

The noise parameter dependences for n- and p-MOSFETs in the linear region have been studied in detail by Vandamme *et al.* [96] and summarized in Table 6.1. Table 6.1 shows the dependence of various parameters viz. gate length (L), width (W), oxide thickness (t_{ox}), gate voltage overdrive ($V_{GS} - V_T$) on the noise parameters namely normalized drain current noise spectra (S_{ID}/I_D^2), drain current noise (S_{ID}) and input-referred noise (S_{VG}).

Table 6.1 Low-frequency Noise Dependence on Device Parameters

	ΔN $\alpha \sim t_{ox}/[V_{GS} - V_T]$	$\Delta\mu$ $\alpha = \text{constant}$
S_{ID}/I_D^2	$[t_{ox}]^2 [V_{GS} - V_T]^2 [1/WL]$	$[t_{ox}] [V_{GS} - V_T] [1/WL]$
$S_{ID,sat}$	$[V_{GS} - V_T]^2 [W/L^3]$	$[V_{GS} - V_T]^3 [1/t_{ox}] [W/L^3]$
S_{VG}	$[t_{ox}]^2 [1/WL]$	$[t_{ox}]^2 [V_{GS} - V_T] [1/WL]$

These dependences vary based on the involved noise mechanism – ΔN number fluctuations theory [44] when the channel carriers are the origin of noise, and the $\Delta\mu$ mobility theory [46] claiming that scattering effects as the source of noise. In reality, it is often observed that a correlated function of these two noise mechanisms – correlated mobility-number fluctuation [39] (ΔN - $\Delta\mu$ theory exists in most devices). These

expressions are also applicable for devices with high- κ dielectric oxides, except that CET values would be more appropriate than C_{ox} values.

It should also be noted that scaling the gate length not only increases the normalized noise magnitude but also gives rise to two other phenomena. One is that it enhances the device-to-device spread among the devices [117] and second is that the noise spectrum changes its character from $1/f$ -like into a Lorentzian ($1/f^2$) one [58], typical for a Generation-Recombination (GR) type of spectrum.

6.2.1 Oxide Thickness Dependence

The expected proportionalities of $1/f$ noise on oxide thickness depend on the noise mechanism that the devices support. It has been shown earlier that n-MOSFETs support the theory on number fluctuations [44], while p-MOSFETs support mobility fluctuations. It has also been reported that in dealing with silicon dioxide thickness scaling, a number of phenomena occur in parallel other than the noise magnitude increase, in particular for n-MOSFETs. The first one is the gate voltage dependence of the LF noise. For thicker oxides [118] the input-referred noise is independent on the gate voltage, while it becomes quadratically dependent on the gate voltage for thinner oxides.

Earlier, Figure 5.22 showed the drain current spectra S_{ID} for a high- κ layer thickness of 1, 2 and 3 nm respectively. The high- κ layer is a 70% Hf-silicate gate dielectric. The interfacial layer is ~ 0.8 nm for all the cases. The increase in $1/f$ noise with decrease in high- κ dielectric layer thickness is found to be marginal as the variations in CET due to studied high- κ layers are negligible. From Table 6.1, it can be inferred that the normalized noise should be either proportional to $|V_{GS}-V_T|^2$ if number fluctuations is

the dominant mechanism, or $|V_{GS}-V_T|$ if mobility fluctuations exist. The normalized noise values increase as the high- κ dielectric thickness reduces for all studied gate voltage overdrives, but this variation is only found to be marginal and does not exactly support the theory. A similar behavior was found in p-MOSFETs.

Figures 6.6 and 6.7 show the normalized noise values S_{ID}/I_D^2 and the input referred noise S_{VG} as a function of the high- κ dielectric layer thickness $t_{high-\kappa}$ for n- and p-MOSFETs at $|V_{DS}| \sim 0.05V$ and $|V_{GS}-V_T| \sim 0.1V$, with the same 0.8 nm interfacial layer. The noise values are seen to be lower for p- than for n-MOSFETs, which confirm the earlier observations.

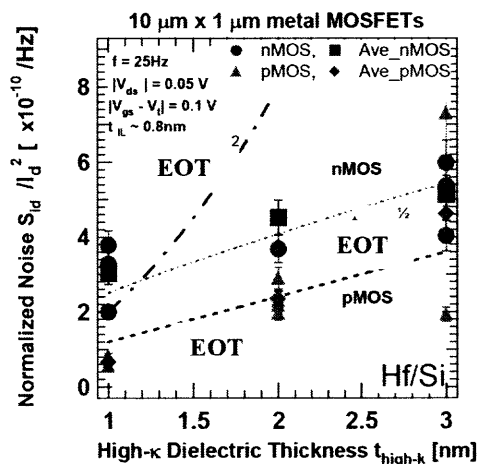


Figure 6.6 Normalized drain current spectral density S_{ID}/I_D^2 versus Hafnium silicate thickness for n- and p-channel devices.

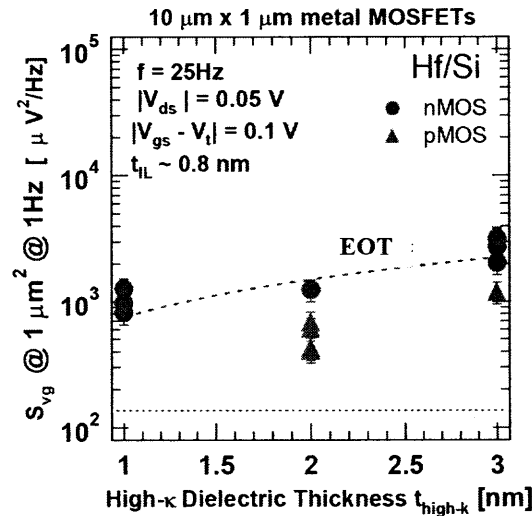


Figure 6.7 Normalized S_{v_g} values versus Hafnium silicate layer thickness for n- and p-channel devices.

Also from Fig 6.7, it can be seen that the values are higher by more than a decade compared to the ITRS [7] requirement of $200 \mu\text{V}^2/\text{Hz}$, shown by the dotted line. From earlier observations, it has been quite established that n-MOSFETs follow correlated number fluctuations while p-MOSFETs follow the theory on mobility fluctuations. Hence for n-MOSFETs, the values of normalized noise S_{ID}/I_D^2 and the input referred noise S_{VG} should be squarely proportional to EOT, while for p-MOSFETs, S_{VG} should vary linearly with EOT, according to Table 6.1.

In our case, for p-MOSFETs, the $t_{\text{high-}\kappa}$ dependence of S_{ID}/I_D^2 and S_{VG} are clearly visible and seem to follow the theory. But deviations are noticed for n-MOSFETs, where the dependency changes and is found to be between $\text{EOT}^{1/2}$ and EOT.

It was earlier investigated the effect of the interfacial layer on $1/f$ noise, and a strong dependence on the interfacial layer thickness was reported, from section 5.1 and 5.3.

Figure 5.3 showed the input referred noise values S_{V_G} for a gate voltage overdrive $|V_{GS} - V_T| \sim 0.1\text{V}$ and $|V_{DSs}| \sim 0.05\text{ V}$ for two different interfacial layers. It was seen that the devices with the lowest interfacial layer thickness t_{IL} (and in-turn higher EOT), show the highest 1/f noise, while a highest IL thickness results in a lower 1/f noise. When HfO_2 is used as a high- κ dielectric, the noise values increase almost by an order of magnitude when the 0.8 nm interfacial oxides is replaced by a 0.4 nm oxide layer.

In a similar experiment conducted by Kojima *et al.* [120], a strong EOT dependence was observed and they attribute the increase in 1/f noise to both the interfacial layer oxide and the high- κ layer of varying thicknesses. They observed a higher increase in S_{V_g} values for an increase in high- κ layer thickness than for an increase in the interfacial layer thickness. Min *et al.* [40] have reported similar observations on interfacial layer dependences in other Hf-based gate stacks.

Another observation is the proximity effect of the gate-dielectric interface on the 1/f noise. It has been reported that the gate-dielectric interface has an additional impact on the 1/f performance of the devices. Though the effect is very pronounced for a poly/high- κ interfacial layer, this effect in metal/high- κ is not observed.

6.2.2 Area Dependence $W \times L$

Figure 6.8 shows the drain current spectra S_{ID} for $W=10\ \mu\text{m}$ TiN-TaN/p-MOSFETs with a 3 nm high- κ dielectric as function of the channel length for $|V_{GS}-V_T| \sim 0.1\text{ V}$ and $|V_{DS}| = 50\text{ mV}$. The L values compared here are 1.0, 0.8, 0.5 and 0.25 μm . It is seen that the 1/f noise decreases as the channel length increases.

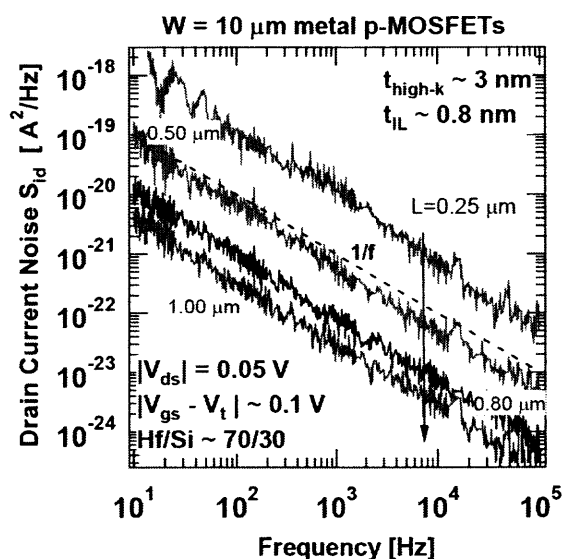


Figure 6.8 Drain current spectral density S_{ID} versus Frequency f for p-channel Hf-silicate devices with a high- κ thickness of 3 nm. The interfacial layer thickness was 0.8 nm for all the devices studied.

The increase in S_{ID} values is not linear as shorter channel lengths have comparatively a higher increase in noise. This non-linear increase in noise is mainly due to short channel effects, where these effects play a very significant role at lower mask lengths. The effect of width- W also has a significant impact on the $1/f$ noise, where a similar behavior can be expected for p-MOSFET devices. The gate length and the oxide thickness dependences are also studied for normalized noise $S_{\text{ID}} / I_{\text{D}}^2$ values. Figure 6.9 shows the normalized noise spectral density $S_{\text{ID}} / I_{\text{D}}^2$ Vs gate voltage overdrive $|V_{\text{GS}} - V_{\text{T}}|$ for the studied channel lengths in p-MOSFETs with 70% Hf-silicates. Clearly, the normalized noise decreases with increase in channel length. On accurate terms, the comparison should be performed for effective channel lengths $(L - \Delta L)$ [second order effects]. The curves run almost parallel to each other, indicating a similar decrease for the

whole gate voltage overdrive range. A similar trend can be expected for n-MOSFETs devices also, as per the scaling law of devices.

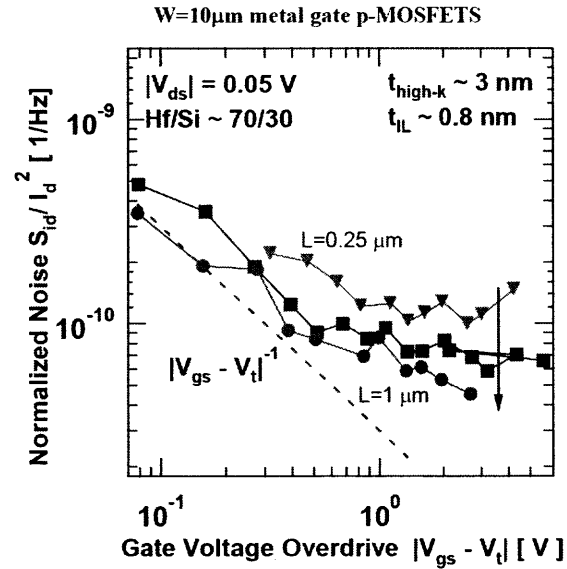


Figure 6.9 Normalized noise spectral density S_{ID} versus gate voltage overdrive ($V_{GS} - V_T$) for p-channel devices with various channel length L .

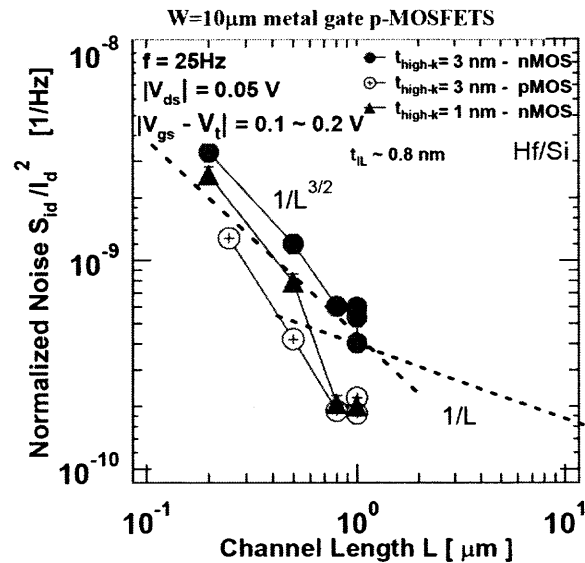


Figure 6.10 Normalized drain current spectral density S_{ID}/I_D^2 versus channel length L for n- and p-MOSFETs with different Hafnium silicate thicknesses.

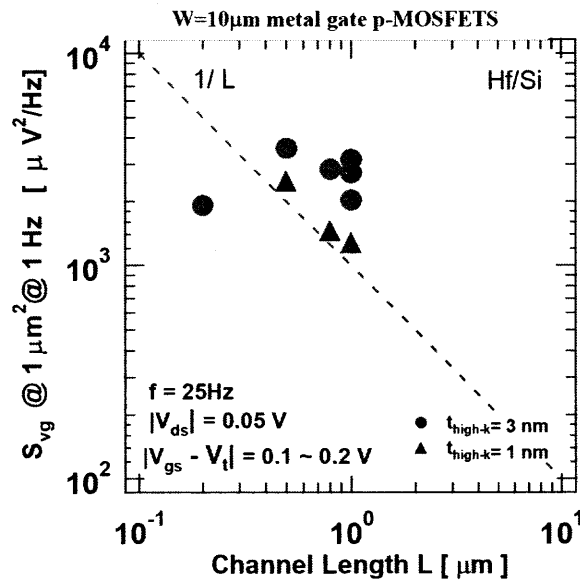


Figure 6.11 Normalized drain current spectral density S_{ID}/I_D^2 versus channel length L for n- and p-MOSFETs with different Hafnium silicate thicknesses.

The input-referred noise for all n- and p-MOSFETs were estimated based on the formula $S_{VG} = S_{ID}/g_m^2$, where g_m is the transconductance of the device. Figures 6.10 and 6.11 shows the normalized noise values and input referred noise as a function of channel length L for both n- and p-MOSFETs for different t_{high-k} thickness, with the same 0.8 nm interfacial layer.

The data for n- and p-MOSFETs clearly shows a deviation from $1/L$ for both S_{VG} and S_{ID}/I_D^2 values, where a stronger dependence on the channel length is observed ($1/L^{3/2}$) at lower L values. Since the measurements and the analyses are limited to the linear region, the series resistance in all these devices is low enough to be neglected in this analysis. In addition, it should be remarked that instead of the mask length the effective channel length should be used.

Such a deviation from a $1/L$ behavior for lower L was also observed in SiO_2 based devices and was earlier reported by the group of Celik-Butler *et al.*[121].

Based on the gate stack engineering using high- κ dielectrics, a possible drain current model is formulated which takes into consideration the following

- i. A thin interfacial layer of SiO_2 is present between the substrate and the high- κ dielectric. The presence of interfacial layer has a stronger impact on $1/f$ noise than the high- κ layer which was earlier discussed in section 5.1.
- ii. $1/f$ noise is different from that of a typical SiO_2 behavior with respect to temperature as earlier investigated in Chapter 5. In other words, the anomalous temperature dependence on $1/f$ noise is considered.
- iii. Direct tunneling occurs in the interfacial layer region and trap assisted tunneling occurs in the high- κ layer.
- iv. Bias dependencies are considered when estimating the tunneling trap time constants and attenuation factor.
- v. Section 5.4 discussed the gate electrode effects and the impact of image charges on $1/f$ noise associated with them. In this model, gate electrodes considered are metal gates and poly-depletion effects are ignored.

Some of the established factors that are taken into consideration are:

1. Large number of traps is present in the high- κ layer defect band-gap which are shallow [16].
2. Scattering effects are also considered [46,62].
3. Asymmetry between gate and substrate injection due to the presence of high- κ layers and interfacial layer [10].

Based on the above criterion, the band-gap model for high- κ is formulated as shown in Figure 6.12. Before applying the power spectral density equation for $1/f$ noise, certain factors needs to be re-estimated based on the above model.

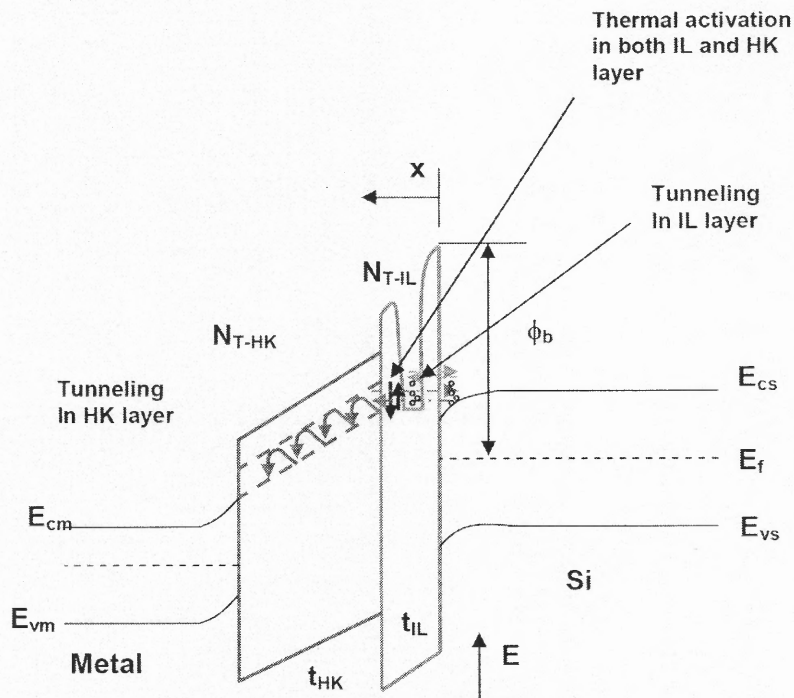


Figure 6.12 Tunneling model with energy dependence for a dual-layer gate stack.

6.3 Drain Current Low-Frequency Noise (1/f) Model For Dual Layer High- κ Gate Stacks

6.3.1 Trap Density Profiles for Hf-based Dielectrics

Based on the earlier discussions, the 3-D trap distribution of gate stacks for a typical SiO_2 case was also studied and extended to a dual-layer case.

6.3.1.1 Trap Density Distribution in Si- SiO_2 System. The trap charge distribution is expressed over energy E and distance x in the oxide [122] as:

$$N_T(E, x) = N_{T0} e^{(\xi_1 |E - E_f| + \left(\xi_2 \frac{V_{gs} - V_{T0}}{t_{ox}} x + \xi_3 \right) x)} \quad (6.1)$$

where

N_{T0} = Volume trap density at the Si-SiO₂ int interface

ξ_1, ξ_2, ξ_3 = Exponential factors characterizing the distribution of traps in the oxide

E_i = Intrinsic Fermi level

V_{gs} = Applied gate bias, V_{T0} = Threshold voltage

t_{ox} = oxide thickness x = distance of oxide trap located at Si-SiO₂ interface

Equation 6.1 probes the trap distribution over energy and distance, but a more realistic model can be provided by making the conduction and valence band tails to be a sum of two exponentials as given by:

$$N_T(E, x) = N_{T0} \left[\begin{aligned} & (1 - \xi_c) e^{\left(\frac{E_c - E}{kT_c} + \xi_2 \frac{V_{gs} - V_{T0}}{t_{ox}} x + \xi_3 x \right)} + \\ & (1 - \xi_v) e^{\left(\frac{E - E_v}{kT_v} + \xi_2 \frac{V_{gs} - V_{T0}}{t_{ox}} x + \xi_3 x \right)} + \frac{1}{2} (\xi_c + \xi_v) \end{aligned} \right] \quad (6.2)$$

Where ξ_c, T_c – Trap parameters characterizing the Conduction Band and ξ_v, T_v – Trap parameters characterizing the Valence Band

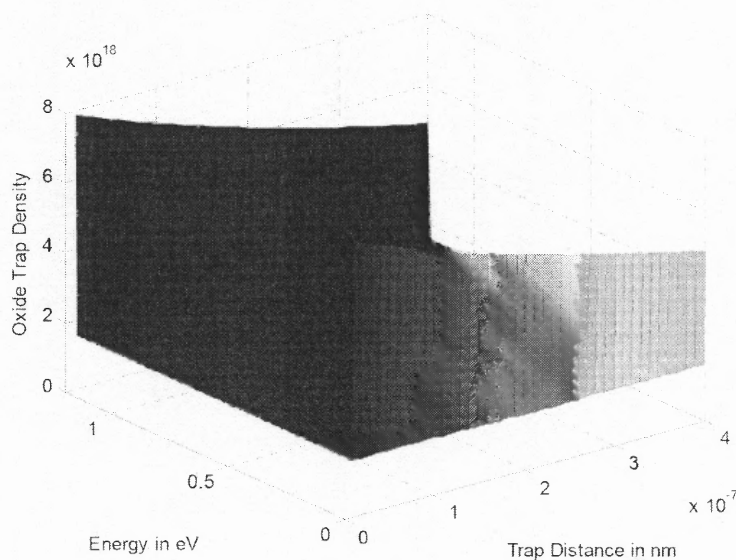


Figure 6.13 3-D Trap Distribution of the Si-SiO₂ system.

This model was already proposed by J. Lee *et al.* [122]. This is now being extended to the case of a dual-layer gate stack.

6.3.1.2 Trap Distribution in High- κ Dielectrics. The voltage across the interfacial layer and high- κ dielectric is given by:

$$\begin{aligned} V_{ox} &= E_{HK} t_{HK} \left(1 + \frac{EOT_{IL}}{EOT_{HK}} \right) \\ V_{ox} &= E_{IL} t_{IL} \left(1 + \frac{EOT_{HK}}{EOT_{IL}} \right) \end{aligned} \quad (6.3)$$

where V_{ox} – voltage across the oxide
 E_{HK}, E_{IL} – Electric Field across high-k and IL
 t_{HK}, t_{IL} – Thickness of high-k and interfacial layer
 EOT_{IL}, EOT_{HK} – Equivalent oxide thickness of IL and high-k

Hence, the net field across the high- κ can be modified to

$$\frac{V_{gs} - V_{T0}}{t_{ox}} x = \frac{(V_{gs} - V_{T0})x_{HK}}{t_{HK} \left(1 + \frac{EOT_{IL}}{EOT_{HK}} \right)} + \frac{(V_{gs} - V_{T0})x_{IL}}{t_{IL} \left(1 + \frac{EOT_{HK}}{EOT_{IL}} \right)} \quad (6.4)$$

Equation 6.4 has now two components: (i) the first component which indicates the field across the high- κ layer while the (ii) second component shows the field across the interfacial layer.

Substituting equation 6.4 in 6.1 will split the equation containing four major components.

- (i) conduction band tail component of high- κ layer
- (ii) valence band tail component of the high- κ layer
- (iii) conduction band tail component of interfacial layer
- (iv) valence band tail component of the interfacial layer

The overall equation describing the trap density of a dual layer high- κ gate stack would be then given by:

$$N_T(E, x) = N_{T0} \left[\begin{array}{l} (1 - \xi_c) e^{\left(-\frac{E_c - E}{kT_c} + \xi_2 \frac{(V_{gs} - V_{T0})x_{HK}}{t_{HK} \left(1 + \frac{EOT_{IL}}{EOT_{HK}}\right)} x_{HK} + \xi_3 x_{HK} \right)} + \\ (1 - \xi_v) e^{\left(-\frac{E - E_v}{kT_v} + \xi_2 \frac{(V_{gs} - V_{T0})x_{HK}}{t_{HK} \left(1 + \frac{EOT_{IL}}{EOT_{HK}}\right)} x_{HK} + \xi_3 x_{HK} \right)} + \\ (1 - \xi_c) e^{\left(-\frac{E_c - E}{kT_c} + \xi_2 \frac{(V_{gs} - V_{T0})x_{IL}}{t_{IL} \left(1 + \frac{EOT_{HK}}{EOT_{IL}}\right)} + \xi_3 x_{IL} \right)} + \\ (1 - \xi_v) e^{\left(-\frac{E - E_v}{kT_v} + \xi_2 \frac{(V_{gs} - V_{T0})x_{IL}}{t_{IL} \left(1 + \frac{EOT_{HK}}{EOT_{IL}}\right)} + \xi_3 x_{IL} \right)} + \frac{1}{2} (\xi_c + \xi_v) \end{array} \right] \quad (6.5)$$

It is to be noted that no additional exponential factors (fitting parameters) other than $\xi_c, \xi_v, \xi_2, \xi_3$ which characterizes the distribution of traps in the oxide is used. Of course, accurate and precise results can be obtained if the individual fitting parameters are represented for interfacial and high- κ layer.

Figure 6.14 shows the 3D model of the high- κ trap distribution for a system with HfO_2 thickness of 5 nm for a metal gate. A dielectric constant value of 20 has been used in this case. The decreasing trap profile is noticed in the interfacial layer much like the Si-SiO₂ system as seen in Figure 6.13. However, the profile of the trap density is different in the high- κ area, where the trap density either remains constant or increases at higher thickness. The result however does not come as a surprise as it has been quite proven that the traps in the bulk of HfO_2 are high when compared to a SiO₂ bulk.

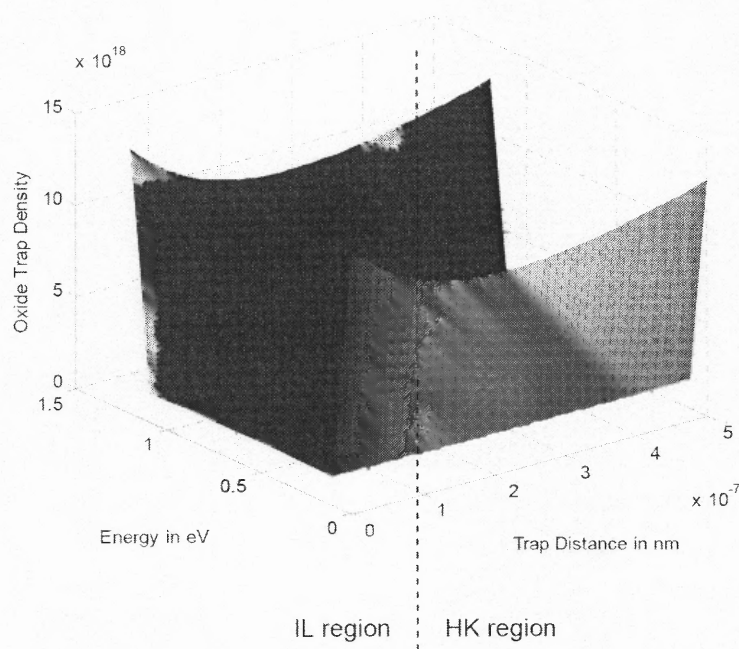


Figure 6.14 3-D Trap Distribution of the Si-SiO₂/HfO₂ system.

A 2D graph of the above result with oxide trap density and trap distance is shown below:

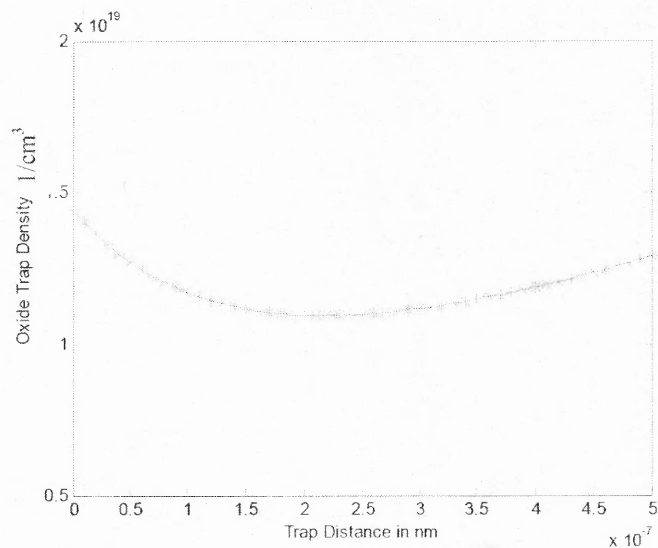


Figure 6.15 Oxide trap density (1/cm³) Vs trap distance (nm) of a SiO₂/HfO₂ system.

6.3.1.3 Experimental Results on the Trap Distribution. Recall the results obtained for a metal gate based on $1/f$ noise characterization as

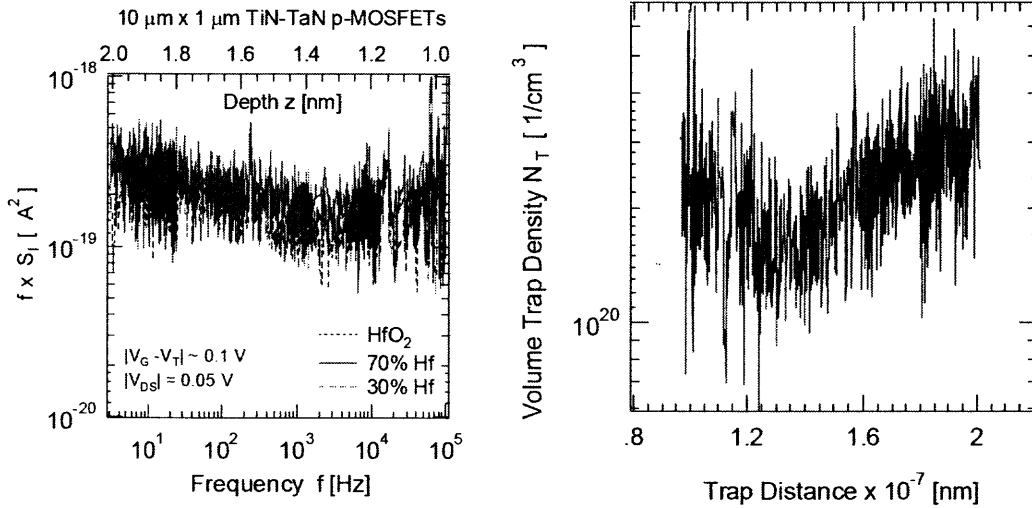


Figure 6.16 (a) $f \times S_I$ Vs frequency/Depth of a metal gate/high- κ system (b) Volume trap density Vs trap distance for the same metal gate/high- κ system.

It is to be noted that $f \times S_I$ has a direct relationship with the trap density volume while the frequency is proportional to tunneling depth based on the formula:

$$\frac{1}{2\pi f} = \tau_0 e^{(\alpha_t z)} \quad (6.6)$$

Where f is the frequency, z is the tunneling depth, α_t is the tunneling parameter, τ_0 is the tunneling time constant. In this case, a 2D model is considered, and is assumed that $E=0$.

Based on the experimental and simulation results the trap distribution is shown below:

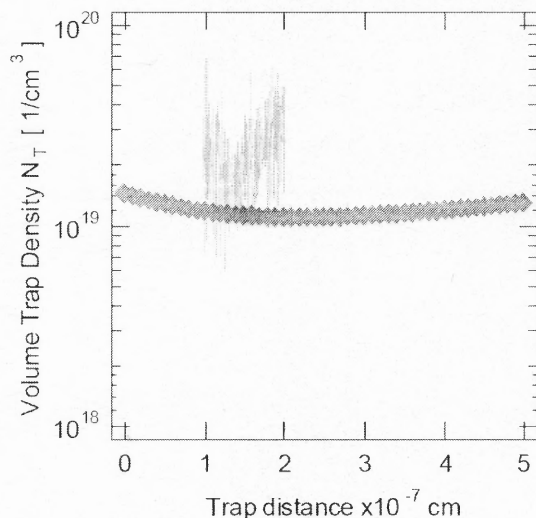


Figure 6.17 Volume Trap density Vs trap distance of a high- κ system – experimental and simulated.

It is seen that the simulated trap density values match with the experimental trap density values in the order of 10^{19} – 10^{20} cm^{-3} . As regards to the trap profile a similar behavior (increasing trap distribution) in the high- κ region is noticed in both experimental and simulated results. It is also to be noted that $1/f$ noise characterization probes traps close to the interface and hence no traps representing the experimental part at the Si-SiO₂ interface is noticed. However, a higher trap density values with decreasing trap profile near the Si-SiO₂ interface is seen experimentally which confirms the simulated results. A 2D model is considered here, which assumes that there is no contribution from energy part of the low-frequency noise model as proposed earlier. These difference is theoretical estimation could explain the difference in the values observed between experimental and simulation results.

This chapter models the low-frequency ($1/f$) noise for drain current in a dual gate stack containing SiO₂ as the interfacial layer and HfO₂ as the gate insulator. Higher $1/f$

noise is trapping and de-trapping of carriers [19] due to the traps in the high- κ layer [20] due to which the

- (i) Tunneling distance (ii) Trapping time constant, and (iii) Trap density should be different [21].

The proposed modeling takes into account, all these three important parameters and modeled here. When a typical SiO₂ device is compared with a dual layer gate stack, the traps may reside in either layer. In that case, the proposed physics-based tunneling model is based on direct tunneling in the interfacial layer (IL) combined with trap-assisted tunneling in the high- κ layer.

Based on SRH characteristics, the tunneling trap time constants were estimated for a dual-layer gate stack as shown in the Appendix. But in theory, the trap occupancy in the high- κ should depend on the occupancy of the traps in the interfacial layer, since the trapped charge in the interfacial layer might screen the effect of the charges in the dielectric. Another argument would also be that the occupancy of one trap in the interfacial layer might affect the energy level of the trap in the high- κ layer or vice versa. In that case, the correlation properties between the interfacial layer and high- κ dielectric needs to be studied which would be difficult and cumbersome and hence it is assumed that these fluctuations to be independent of each other.

However, if low-frequency noise needs to be modeled one has to account for the fact, the energy dependence of these traps in the interfacial layer and high- κ layer are different. In that case, the tunneling of electrons to and from these traps is no more elastic in energy. Hence one would consider tunneling of these carriers, which is inelastic in nature both in interfacial and the high- κ layer, which are assisted by traps present in both

these layers. In other words, the model would consider not only the location of the traps in the oxide but also the energy level of these traps in the oxide. Hence it becomes more important to understand the trap distribution in the gate stack across the energy band gap. An attempt has been made to provide a 3-D trap distribution of the gate stack in the next section. The results are then compared with experimental values and a conclusion is made.

Considering the energy distribution of traps, it is important to understand the energy distribution of traps in HfO_2 in a dual-layer gate stack, due to various reasons. This importance has been discussed extensively and has also been verified and modeled by several authors studying the energy distribution of the traps. The energy levels in the high- κ layer have a strong influence (mainly due to O related vacancies) on the device characteristics were verified independently by researchers at IMEC/IBM (A. Kerber *et al.*) [16], Robertson *et al.* [123] and more recently by N. Chowdhury *et al.* [124]. Moreover, Z. Celik *et al.* [77], Reibold *et al.* [125],C. Surya *et al.* [52], Dutta *et al.* [50] and more recently by J. Lee *et al.* [122,126], outlined the importance of this distribution for a SiO_2 or thin SiON case in a $1/f$ noise context. In a more recent paper by B. Min and Z. Celik-Butler [127], a unified model for a dual-layer was proposed which includes the interlayer dielectric. However they considered that the energy distribution of traps in both IL and high- κ are not affected by the low-frequency noise.

This is important and should be considered when the unified model of $1/f$ noise for a dual-layer gate stack is considered. Moreover, the trap profiles are also completely different in the high- κ gate stack, which influence the energy distribution strongly in these layers. This document attempts to model the low-frequency noise for drain current

by combining the tunneling time constant with energy dependence of the traps. Hence the device is modeled based on the above characteristics:

The energy dependence of traps is considered in the following way for this gate stack.

- (i) In the case of interfacial layer, direct tunneling occurs with the energy distribution equivalent that of a thin SiON case.
- (ii) In the case of a high- κ dielectric, it is known that the majority of the defect levels are shallow; even though it has been proved that the deep defect levels do exist. The conduction mechanism mostly is of Poole-Frenkel hopping type in these shallow defect layers, which are strongly trap assisted. However, this makes the analysis and modeling very complicated if all the factors are taken into account. In this case, it is simply considered that the low-frequency noise is affected by the energy distribution of the traps in the high- κ layer (not exactly considering the exact values of energy), equivalent that of a SiON case.

6.3.2 Formulation of 1/f Drain Current Noise Model for High- κ Dielectrics

The low-frequency model is derived as follows: First the model is derived for a single layer gate stack and then the formulation is extended to the dual layer gate stack.

For a single layer gate stack, the thermally activated time constant τ given by:

$$\tau = \tau_{th} e^{(\beta E)} \quad (6.7)$$

Where β is the exponential factor of the thermal activation process, involving the thermal energy equivalent to kT.

The effective trap time constants (based on the derivation in appendix) in that case would be then modified to

$$\tau_{eff} = \tau_0 [e^{(\alpha z + \beta E)}] \quad (6.8)$$

It is to be noted that the equation is also closely related to the proposed Trap assisted Tunneling model (TATA) proposed in the paper by J. Lee *et al.* [122,126],

$$\tau_{eff} \sim \tau_{eff0} e^{[\lambda_{th} E + q \lambda_{tm} \left(1 - \frac{V_{gs} - V_{T0}}{4\phi_b / q}\right) x]} \quad (6.9)$$

Considering the noise power spectral density due to all the traps in the interfacial and high- κ layer within the elemental volume of $\Delta x \Delta y \Delta z$,

$$S_{\Delta N_T} = \int_0^W \int_{E_v}^{E_c} \int_0^{t_{ox}} 4N_T(E, x) f_i (1 - f_i) dx \frac{\tau_{eff}(E, x)}{1 + \omega^2 \tau_{eff}^2(E, x)} dy dz dE \quad (6.10)$$

Integrating the volume part and retaining the energy and thickness;

$$S_{\Delta N_T} = 4N_T(E, x) kTW \Delta x \underbrace{\int_0^{t_{ox}} \frac{\tau_{eff}(E, x)}{1 + \omega^2 \tau_{eff}^2(E, x)} dz}_{S_{\Delta N_T}} dE \quad (6.11)$$

The integral contains the effective trap time constant dependent on energy and location of the traps. Hence, if this double integral is evaluated, one can derive the power spectral density of the drain current S_{Id} .

Substituting for $\tau_{eff} = \tau_0 [e^{(\alpha z + \beta E)}]$ in eqn. 6.11;

$$S_{\Delta N_T} = \frac{1}{\omega^2 \tau_0} \int_{E_v}^{E_c} \int_0^{t_{ox}} \frac{e^{(\alpha z + \beta E)}}{\left(\frac{1}{\omega^2 \tau_0^2} + e^{2(\alpha z + \beta E)}\right)} dz dE \quad (6.12)$$

Integrating the oxide part reduces the equation to

$$= \frac{1}{\omega^2 \tau_0} \int_0^E \left(\frac{\tau_0 \omega \left[\tan^{-1}(\tau_0 \omega e^{(\beta E)}) \right] - \left[\tan^{-1}(\tau_0 \omega e^{(\alpha t_{ox} + \beta E)}) \right]}{\alpha} \right) dE \quad (6.13)$$

$$= \frac{1}{\alpha \omega^2 \tau_0} \left[\int_0^E \left[\tan^{-1}(\tau_0 \omega e^{(\alpha t_{ox} + \beta E)}) \right] dE - \tau_0 \omega \int_0^E \left(\tau_0 \omega \left[\tan^{-1}(\tau_0 \omega e^{(\beta E)}) \right] \right) dE \right]$$

Integrating the \tan^{-1} term with e^x term inside yields a complex term with real and imaginary part. To further simplify the process, revisit the part using Taylor's series approximation as:

$$e^x \sim 1 + x + \frac{x^2}{2!} + \dots$$

$$e^x \sim 1 + x$$

Hence

(6.14)

$$e^{(\beta E)} \sim 1 + \beta E$$

$$e^{(\alpha t_{ox} + \beta E)} \sim e^{\alpha t_{ox}} + e^{\alpha t_{ox}} \beta E$$

$$e^{(\alpha t_{ox} + \beta E)} \sim (1 + \alpha t_{ox}) + (1 + \alpha t_{ox})(\beta E)$$

Subs eqns. 6.14 in 6.13 will yield the result as:

$$S_{\Delta N_{Ty}} = \frac{1}{\alpha \omega^2 \tau_0} \left[\underbrace{\int_0^E \tan^{-1}(\tau_0 \omega [(1 + \beta E)(1 + \alpha t_{ox})]) dE}_I - \overbrace{\int_0^E \left(\tau_0 \omega \left[\tan^{-1}(\tau_0 \omega (1 + \beta E)) \right] \right) dE}^{II} \right] \quad (6.15)$$

Term I is of the form: $\int \tan^{-1}[(a + bx)(c + d)] dx$ and integrating this equation will give:

$$-\frac{1}{2b(c+d)} [2(c+d)(a+bx) \tan^{-1}[a(1+bx)] - \frac{\log(a^2(c+d)^2 + b^2x^2(c+d)^2 + 2abx(c+d)^2 + 1)}{2ab}]$$

Term II is of the form: $\int \tan^{-1}[a(1+bx)] dx$ and integrating this part will yield:

$$\frac{\tan^{-1}[a(1+bx)]}{b} + x \tan^{-1}[a(1+bx)] - \frac{\log(b^2x^2a + 2bxa^2 + a^2 + 1)}{2ab}$$

Including these terms will make the eqn 6.15 will make it more complex as it would contain 6 different terms. The log terms for both cases is ignored, the implications of which will be discussed at the end of the derivation:

Hence term I reduces to,

$$\int_0^E \tan^{-1}[\tau_0 \omega(1 + \beta E)] dE = \frac{\tan^{-1}[\tau_0 \omega(1 + \beta E)]}{\beta} + E \tan^{-1}[\tau_0 \omega(1 + \beta E)] \quad (6.16)$$

And term II reduces to

$$\int_0^E \left(\tau_0 \omega \left[\tan^{-1} \left[(1 + \beta E)(1 + \alpha t_{ox}) \right] \right] \right) dE = \left(E + \frac{\tau_0 \omega}{\beta} \right) \tan^{-1}(\tau_0 \omega [(1 + \beta E)(1 + \alpha t_{ox})]) \quad (6.17)$$

Subs. Eqns. 6.16 and 6.17 in 6.15 will give

$$S_{\Delta N_T} = \frac{1}{\alpha \omega^2 \tau_0} \left[\left(E + \frac{\tau_0 \omega}{\beta} \right) \tan^{-1}(\tau_0 \omega [(1 + \beta E)(1 + \alpha t_{ox})]) - \tau_0 \omega \left[\frac{\tan^{-1}[\tau_0 \omega(1 + \beta E)]}{\beta} + E \tan^{-1}[\tau_0 \omega(1 + \beta E)] \right] \right] \quad (6.18)$$

Subs. Eqn 6.18 into 6.11 will yield:

$$S_{\Delta N_T} = \frac{4N_T(E, x)kTW\Delta x}{\alpha \omega^2 \tau_0} \left[\left(E + \frac{\tau_0 \omega}{\beta} \right) \tan^{-1}(\tau_0 \omega [(1 + \beta E)(1 + \alpha t_{ox})]) - \tau_0 \omega \left[\frac{\tan^{-1}[\tau_0 \omega(1 + \beta E)]}{\beta} + E \tan^{-1}[\tau_0 \omega(1 + \beta E)] \right] \right] \quad (6.19)$$

Eqn. 6.19 is a complex term containing both energy and tunneling distance de-convoluted (or made independent). To check the validity of the equation, put E=0 in eqn. 6.19. The equation will then reduce to:

$$S_{\Delta N_T} = \frac{1}{\alpha \omega^2 \tau_0} \left[\frac{\tau_0 \omega}{\beta} \tan^{-1}(\tau_0 \omega [1 + \alpha t_{ox}]) - \tau_0 \omega \left(\frac{\tan^{-1}[\tau_0 \omega]}{\beta} \right) \right]$$

Solving further, it is seen that,

$$S_{\Delta N_T} = \frac{1}{\omega(\alpha\beta)} \left[\tan^{-1}(\tau_0\omega[1 + \alpha t_{ox}]) - \tau_0\omega(\tan^{-1}[\tau_0\omega]) \right] \quad (6.20)$$

Equation 6.20 is the term neglecting the energy term and it is seen that it is very similar to the eqn. 4 proposed by Z. Celik-Butler [126] in their recent paper.

However there are two differences noticed when compared to their proposed eqn.

- (i) The term $[1 + \alpha t_{ox}]$ is present instead of $e^{\alpha t_{ox}}$. This can be explained and this arises due to earlier Taylor's series approximation as per the equation 6.14. Hence, one can consider this factor to be $e^{\alpha t_{ox}}$ and for $1 + \beta E$, it would then be $e^{\beta E}$
- (ii) Also it is seen that tunneling constant has both the factors α and β . This is expected as this would mean the geometric mean of the time constant involving the trap distance and trap energy.

This confirms the validity of the equation with the energy term included.

Based on the above argument and reversing back the Taylor series approximation, it is seen that;

$$S_{\Delta N_T} = \frac{4N_T(E, x)kTW\Delta x}{\alpha\omega^2\tau_0} \left[\left(E + \frac{\tau_0\omega}{\beta} \right) \tan^{-1}(\tau_0\omega[e^{\alpha t_{ox} + \beta E}]) - \tau_0\omega \left[\frac{\tan^{-1}[\tau_0\omega e^{\beta E}]}{\beta} + E \tan^{-1}[\tau_0\omega e^{\beta E}] \right] \right] \quad (6.21)$$

This term requires a further explanation, before proceeding for a dual layer stack. Earlier, J. Lee *et al.* [122] for the same condition as:

$$S_{\Delta N_T} = \frac{\Delta y W k T N_{T0} e^{\xi_1 | E_{fn} - E_i |}}{q \lambda_{tun,eff} \left(1 - \frac{V_{gs} - V_{T0}}{4\phi_b / q} \right) [2\pi\tau_{eff0} e^{(\lambda_{th,eff} E_{fn})}]^{\gamma-1} f^\gamma \cos\left[\frac{\pi}{2}(\gamma-1)\right]} \quad (6.22)$$

However, in 6.22, for a thin SiON case, $S_{\Delta N}$ does not have a thickness dependency (or in other words, no t_{ox} term), but γ dependency. In this case, when one substitutes the value $\gamma \sim 1$, then one would get back the original equation of $S_{\Delta N}$.

In the proposed equation 6.22, the t_{ox} dependency is noticed along with energy level of the traps. Hence this would be more appropriate if one considers the case of a dual-layer gate stack.

The log term in the earlier part of the derivation (before substituting in eqn. 9) is ignored due to the following reasons:

1. The term would contain the square of the energy and t_{ox} term, the product of which would have a lower numerical value, when compared to the \tan^{-1} term.
2. There would be two log terms one each for \tan^{-1} term. If these two log terms are then considered together, then the overall value of this difference becomes totally insignificant.

Hence for the same above, the log term is ignored. Assuming the fluctuations in the interfacial layer and high- κ layer are independent of each other, even though it is understood that the occupancy of one trap might affect the energy level of the other, then:

$$S_{\Delta N_T} = \int_0^W \int_{E_v}^{E_c} \int_0^{t_{IL}} 4N_T(E, x) f_i(1-f_i) dx \frac{\tau_{IL}(E, x)}{1 + \omega^2 \tau_{IL}^2(E, x)} dy dz dE + \int_0^W \int_{E_v}^{E_c} \int_{t_{IL}}^{t_{IL}+t_{HK}} 4N_T(E, x) f_i(1-f_i) dx \frac{\tau_{HK}(E, x)}{1 + \omega^2 \tau_{HK}^2(E, x)} dy dz dE \quad (6.23)$$

$$S_{\Delta N_T} = \frac{4N_{T,IL}(E, x)kTW\Delta x}{\alpha_{IL}\omega^2\tau_0} \left[\left(E_{IL} + \frac{\tau_0\omega}{\beta_{IL}} \right) \tan^{-1}(\tau_0\omega [e^{\alpha_{IL}t_{IL} + \beta_{IL}E_{IL}}]) - \tau_0\omega \left[\frac{\tan^{-1}[\tau_0\omega e^{\beta_{IL}E_{IL}}]}{\beta_{IL}} + E_{IL} \tan^{-1}[\tau_0\omega e^{\beta_{IL}E_{IL}}] \right] \right] + \frac{4N_{T,HK}(E, x)kTW\Delta x}{\alpha_{HK}\omega^2\tau_0} \left[\left(E_{HK} + \frac{\tau_0\omega}{\beta_{HK}} \right) \tan^{-1}(\tau_0\omega [e^{\alpha_{HK}(t_{HK}+t_{IL}) + \beta_{HK}E_{HK}}]) - \tau_0\omega \left[\frac{\tan^{-1}[\tau_0\omega e^{(\alpha_{HK}t_{HK} + \beta_{HK}E_{HK})}]}{\beta_{HK}} + E_{HK} \tan^{-1}[\tau_0\omega e^{(\alpha_{HK}t_{HK} + \beta_{HK}E_{HK})}] \right] \right] \quad (6.24)$$

Considering the oxide thickness that if $t_{IL} > t_{HK}$, it is obvious that the t_{HK} would vanish and the equation would reduce to:

$$S_{\Delta N_T} = \frac{4N_{T,IL}(E, x)kTW\Delta x}{\alpha_{IL}\omega^2\tau_0} \left[\left(E_{IL} + \frac{\tau_0\omega}{\beta_{IL}} \right) \tan^{-1}(\tau_0\omega [e^{\alpha_{IL}t_{IL} + \beta_{IL}E_{IL}}]) - \tau_0\omega \left[\frac{\tan^{-1}[\tau_0\omega e^{\beta_{IL}E_{IL}}]}{\beta_{IL}} + E_{IL} \tan^{-1}[\tau_0\omega e^{\beta_{IL}E_{IL}}] \right] \right] \quad (6.25)$$

and for a case where $t_{HK} > t_{IL}$, t_{HK} would then be,

$$S_{\Delta N_T} = \frac{4N_{T,HK}(E, x)kTW\Delta x}{\alpha_{HK}\omega^2\tau_0} \left[\left(E_{HK} + \frac{\tau_0\omega}{\beta_{HK}} \right) \tan^{-1}(\tau_0\omega [e^{\alpha_{HK}t_{HK} + \beta_{HK}E_{HK}}]) - \tau_0\omega \left[\frac{\tan^{-1}[\tau_0\omega e^{\beta_{HK}E_{HK}}]}{\beta_{HK}} + E_{HK} \tan^{-1}[\tau_0\omega e^{\beta_{HK}E_{HK}}] \right] \right] \quad (6.26)$$

Nominally the threshold thickness has seen to be ~ 2.5 nm.

Based on the above equation for $S_{\Delta NT}$ one can arrive the equation of the S_{Id} , based on the unified model [39, 59, 128].

$$S_{\Delta Id} = \left[\frac{I_d}{\Delta N} (1 + \alpha_{sc}\mu_{eff}N_{inv}) \right]^2 S_{\Delta N_T} \quad (6.27)$$

And

$$S_{Id} = \frac{1}{L^2} \int_0^L S_{\Delta Id} \Delta x dx \quad (6.28)$$

Hence eqn. 6.23, would then be

$$S_{I_D} = \left[\frac{kTI_d^2}{WL} \left(\frac{1}{N_{inv}} + \alpha_{sc}\mu_{eff} \right) \right]^2 x \left[\frac{4N_{T,IL}}{\alpha_{IL}\omega^2\tau_0} \left[\left(E_{IL} + \frac{\tau_0\omega}{\beta_{IL}} \right) \tan^{-1}(\tau_0\omega [e^{\alpha_{IL}t_{IL} + \beta_{IL}E_{IL}}]) - \tau_0\omega \left[\frac{\tan^{-1}[\tau_0\omega e^{\beta_{IL}E_{IL}}]}{\beta_{IL}} + E_{IL} \tan^{-1}[\tau_0\omega e^{\beta_{IL}E_{IL}}] \right] \right] + \frac{4N_{T,HK}}{\alpha_{HK}\omega^2\tau_0} \left[\left(E_{HK} + \frac{\tau_0\omega}{\beta_{HK}} \right) \tan^{-1}(\tau_0\omega [e^{\alpha_{HK}(t_{HK} + t_{IL}) + \beta_{HK}E_{HK}}]) - \tau_0\omega \left[\frac{\tan^{-1}[\tau_0\omega e^{\beta_{HK}E_{HK}}]}{\beta_{HK}} + E_{HK} \tan^{-1}[\tau_0\omega e^{\beta_{HK}E_{HK}}] \right] \right] \right] \quad (6.29)$$

Equation 6.29 can be simplified to

$$S_{I_D} = \left[\frac{kTI_d^2}{WL} \left(\frac{1}{N_{inv}} + \alpha_{sc}\mu_{eff} \right) \right]^2 \left[\frac{2}{(\pi f)^2\tau_0} \right] \left[\frac{N_{T,IL}}{\alpha_{IL}} Y + \frac{N_{T,HK}}{\alpha_{HK}} Z \right] \quad (6.30)$$

where

$$Y = \left[\left(E_{IL} + \frac{\tau_0 \omega}{\beta_{IL}} \right) \tan^{-1} \left(\tau_0 \omega \left[e^{\alpha_{IL} t_{IL} + \beta_{IL} E_{IL}} \right] \right) - \tau_0 \omega \left[\frac{\tan^{-1} \left[\tau_0 \omega e^{\beta_{IL} E_{IL}} \right]}{\beta_{IL}} + E_{IL} \tan^{-1} \left[\tau_0 \omega e^{\beta_{IL} E_{IL}} \right] \right] \right] \quad (6.31)$$

And

$$Z = \left[\left(E_{HK} + \frac{\tau_0 \omega}{\beta_{HK}} \right) \tan^{-1} \left(\tau_0 \omega \left[e^{\alpha_{HK} (t_{HK} + t_{IL}) + \beta_{HK} E_{HK}} \right] \right) - \tau_0 \omega \left[\frac{\tan^{-1} \left[\tau_0 \omega e^{(\alpha_{HK} t_{HK} + \beta_{HK} E_{HK})}}{\beta_{HK}} \right] + E_{HK} \tan^{-1} \left[\tau_0 \omega e^{(\alpha_{HK} t_{HK} + \beta_{HK} E_{HK})} \right] \right] \right] \quad (6.32)$$

Equation 6.30 gives the power spectral density of low-frequency noise for drain current for a dual layer gate stack.

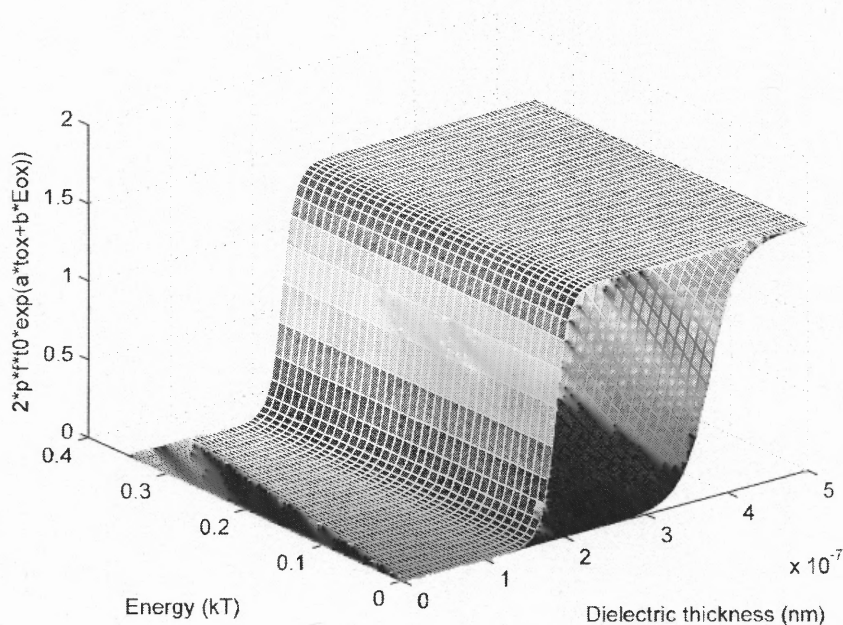


Figure 6.18 Calculation of \tan^{-1} factor for SiO_2 (white lines) and HfO_2 layers (black lines) as a function of energy and oxide thickness for $f = 1 \text{ Hz}$ and $\tau = 1 \times 10^{-10} \text{ s}$. The β component of energy is taken as 0.02 /eV , while corresponding values for SiO_2 and HfO_2 have been taken.

6.3.3 Approximation of Noise Model for Number Theory

The earlier derivation is based on correlated number-mobility fluctuation theory. However, if number fluctuations are the dominant mechanism over mobility fluctuations, then the equation would then gets modified.

Based on equation 6.25 and 6.26, equation 6.18 can be rewritten as:

$$S_{\Delta N_T} = \frac{4kTW\Delta x}{\omega^2\tau_0} \left[\frac{N_{T,IL}(E,x)}{\alpha_{IL}} Y + \frac{N_{T,HK}(E,x)}{\alpha_{HK}} Z \right] \quad (6.33)$$

Earlier Simoen *et al.* [129], showed in simplest terms, that for a SiO₂ system,

$$S_{ID} = \frac{I_D^2}{W^2 L^2 Q_N^2} q^2 S_{N_T} \quad (6.34)$$

and

$$S_{VG} = \frac{q^2}{W^2 L^2 C_{OX}^2} S_{N_T} \quad (6.35)$$

One can substitute eqn. 6.33, 6.35 in equation 6.27 and integrating Δx over L will yield:

$$S_{VG} = \frac{4kTq^2}{WL\omega^2\tau_0 C_{OX}^2} \left[\frac{N_{T,IL}(E,x)}{\alpha_{IL}} Y + \frac{N_{T,HK}(E,x)}{\alpha_{HK}} Z \right] \quad (6.36)$$

and

$$S_{ID} = \frac{4kTq^2}{WL\omega^2\tau_0 Q_N^2} \left[\frac{N_{T,IL}(E,x)}{\alpha_{IL}} Y + \frac{N_{T,HK}(E,x)}{\alpha_{HK}} Z \right] \quad (6.37)$$

Equations 6.36 and 6.37 gives the drain current noise and input referred noise in simplest terms, if number fluctuations are assumed the dominant mechanism. If one goes out further to solve 6.36 and 6.37, with some basic assumptions on the term E and neglecting the β term, the S_{VG} term would further reduce to:

$$S_{VG} = \frac{kTq^2}{8WLfC_{OX}^2} \left[\frac{N_{T,IL}(E, x)}{\alpha_{IL}} + \frac{N_{T,HK}(E, x)}{\alpha_{HK}} \right] \quad (6.38)$$

For all practical and calculation purposes, equation 6.38 can be considered as the input-referred noise term for a dual-layer gate stack.

6.3.4 Validation of 1/f Drain Current Noise Model for High- κ Dielectrics

Based on the above equations, the simulated results of the equation are correlated with the measured results.

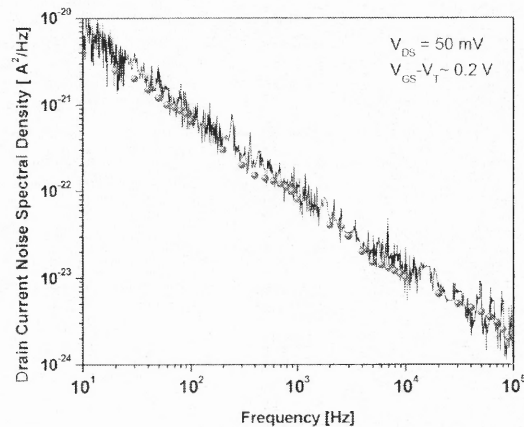


Figure 6.19 Measured and simulated results of drain Current noise Vs frequency of a typical n-MOSFET metal gate device.

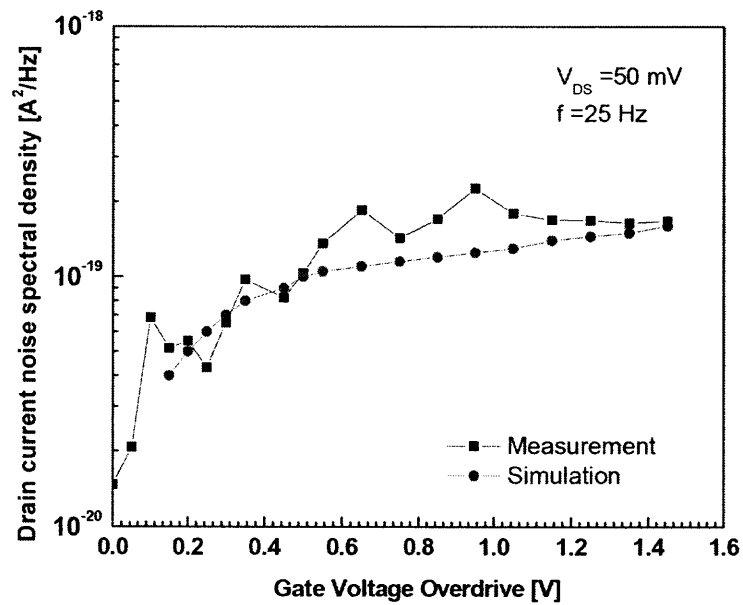


Figure 6.20 Simulated and measured results for drain current noise vs gate voltage of a typical metal gate n-MOSFET device.

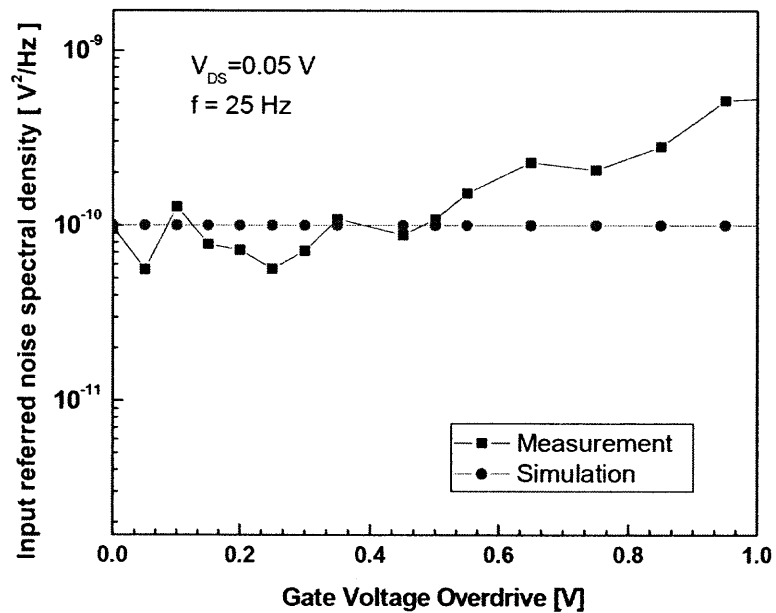


Figure 6.21 Simulated and measured results for input referred noise vs gate voltage of a typical metal gate n-MOSFET device.

Figure 6.19 shows the comparison between simulated and measured results of drain current noise spectral density in linear region for a metal gate HfO₂ n-MOSFET. The results are based on assumption that the devices follow number fluctuation theory as explained in Sec 6.3.3. Table 6.2 shows the values used for trap densities and the tunneling parameters for the high-k oxide and the interfacial layer to estimate the drain current noise.

Table 6.2 Fitting Parameters for Tunneling Constant and Trap Densities Used for High- κ and Interfacial Layer at Various Trap Locations

SL. No	Trap Distance (nm)	$N_T(\text{IL}) \text{ cm}^{-3}$	$\alpha_{\text{IL}} \text{ cm}^{-1}$	$N_T(\text{HK}) \text{ cm}^{-3}$	$\alpha_{\text{HK}} \text{ cm}^{-1}$
1	0	1.5×10^{17}	1.2×10^8	-	0.5×10^8
2	<0.8	0.8×10^{16}	1.2×10^8	-	0.5×10^8
3	>0.8	-	1.2×10^8	3.5×10^{19}	0.5×10^8
4	1	-	1.2×10^8	3.75×10^{19}	0.5×10^8
5	1.5	-	1.2×10^8	4.0×10^{19}	0.5×10^8
6	2.0	-	1.2×10^8	5.0×10^{19}	0.5×10^8

The simulation results agree well with the experimental results, within an acceptable error. Figure 6.20 explains the simulated drain current noise values under different gate bias conditions in linear region of operation. The measured results are seen to have some spikes between 0.2 V to 1.0 V, in comparison with simulation. The error between simulated and measured results is less than a factor of 2X. These spikes are mainly attributed to the sensitivity of the 1/f noise test and characterization system to external disturbances. Figure 6.21 shows the compared results of gate input referred noise

spectral density in comparison with gate voltage overdrive for a typical metal gate / HfO₂ device. While the simulation results show that S_{VG} is in the order of 10^{-10} V²/Hz, S_{VG} tends to increase at higher gate voltage overdrive. This is mainly attributed to the contribution of gate leakage current, as it becomes significantly higher at higher overdrive voltages.

CHAPTER 7

SUMMARY AND FUTURE OUTLOOK

7.1 Summary

The research presented in this dissertation explored the performance of low-frequency noise of Hf-based MOSFETs. $1/f$ type noise was found to be predominant source of low-frequency noise in these advanced gate stacks. Various gate technological and processing parameters that could influence $1/f$ noise were identified and the role of each parameter was investigated in detail in Chapter 5. The effects of $1/f$ noise on high and low temperature was also investigated briefly. Overall:

- (i) The $1/f$ noise is greatly influenced by interfacial layer. The thickness, quality and the annealing effects of interfacial layer have a significant on $1/f$ noise. Proper engineering of this interfacial layer is necessary to keep the flicker noise at a reduced level. However, the effect of high- k layer thickness is minimal $1/f$ noise when a optimal value ($\sim 0.8\text{nm}$) of interfacial layer is used.
- (ii) Profound effect of gate electrodes and gate electrode/high- k interface is noticed. Comparison studies between the poly-Si, Fully silicided and metal gate electrodes showed that the distribution of oxide traps are different, leading to difference in $1/f$ noise. Fermi-level pinning at the interface translates to oxide traps due to which changes in noise behavior is noticed.
- (iii) The other effects such as Hf-content, gate processing, substrate all have the influence on $1/f$ noise and their role was investigated in detail. The physical origin and noise mechanisms in the high- κ devices were studied in detail. The

role of temperature plays a major role since the trap energy levels are shallow in HfO₂ gate dielectric.

- (iv) Based on the above observations, a new flicker noise model for n-MOSFETs was deduced in Chapter 6, since the existing models could not explain some of the noise behavior in high-k gate stacks completely. The effects of interfacial layer, high-k oxide and the temperature were considered for modeling the drain current noise in n-MOSFETs. A thermally activated tunneling based model was proposed, where both location and energy distribution of traps in both high-k and interfacial oxide has been considered and modeled.

7.2 Recommendations for Future Work

The performance of advanced high-k gate stacks was investigated for 1/f noise. The work was limited to characterization of devices for drain current 1/f noise. Input-referred gate current noise was used for this study for gate related noise values. However, a direct measurement of gate current noise would prove be to more useful. Although it is predicted, that the gate current: drain current ratio would be very small, correlation of the noise currents would become significant for aggressively scaled high-k gate stacks.

The effect of high-k/interfacial layer interface has not been well understood with respect to 1/f noise. One can investigate by accurate conversion of frequency to tunneling depth axis and study the distribution of traps in the region. More detailed investigation is needed to understand the effects of 1/f noise on this interface.

Chapter 5 discussed about the effect of 1/f noise at high and low temperature. The effects were found to be significantly different from that of typical SiO₂, mainly due to the different energy levels of the traps in the high-k layer. More insights and detailed

investigation on understanding the activation energy levels of traps and its effects on $1/f$ noise is needed, for accurate modeling of $1/f$ noise for these devices.

Chapter 6 considered the effects of interfacial layer, high- k layer and the temperature for $1/f$ drain current noise modeling in high- k based n-MOSFETs. The study needs to be extended for p-MOSFET devices, where the noise origin follows the theory on mobility fluctuations. Detailed understanding and $1/f$ noise modeling for p-MOSFETs is required.

APPENDIX

ESTIMATION OF TRAP TIME CONSTANTS

A.1 Basic Trapping Process in the Dual Layer Gate Stack

Consider a basic trapping process in a dual-layer gate stack, where a trap in the interfacial layer or the high- κ layer follows the Shockley-Read-Hall (SRH) characteristics, called as SRH center. A SRH acceptor center is in the negatively charged state if it is filled with one electron or in the neutral state when it is empty, while the donor center is in a positively charged state when it is empty or neutral when it is filled [80].

The fluctuation of the number of trapped electrons comes from the four electron and hole emission and capture processes by the centers as indicated in Figure A.1.

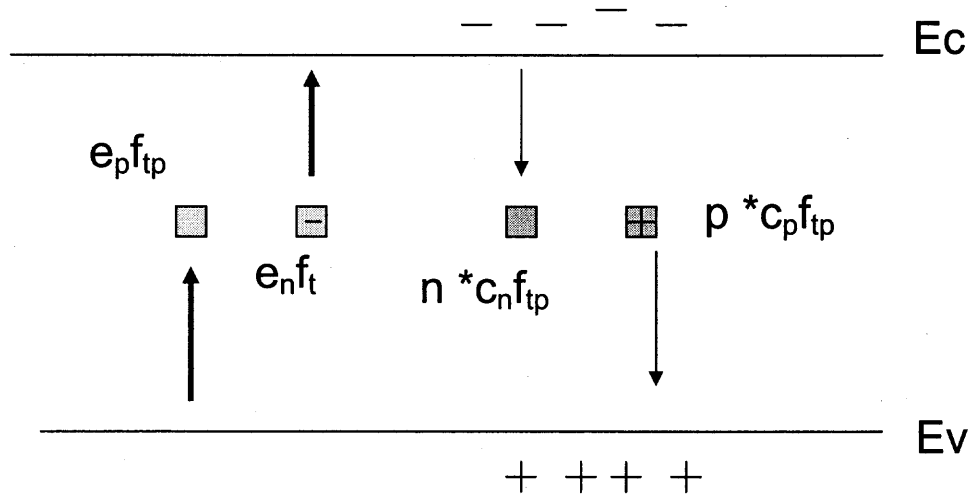


Figure A.1 Basic trapping process (capture and emission) across the Si-bandgap for a dual-layer gate stack.

Then the rate of change of the trapped electron concentration is the difference between the rate of filling and emptying of the centers due to the four processes as indicated in Figure A.1.

Rate of change of carrier concentration (both electrons and holes):

$$\frac{\partial n_t}{\partial t} = N_t [(c_n f_{tp} n - e_n f_t) - (c_p f_{tp} p - e_p f_t)] \quad (6.39)$$

Using the above equation one can deduce the trap time constant of electrons and holes.

A.2 Fluctuation of Charge States in the Interfacial Layer and High- κ Dielectric

Now consider a dual layer high- κ dielectric stack, with two different concentration of trap densities in the interfacial layer and high- κ layer as shown in Figure 8.

Four different types of processes could possibly occur:

- (i) tunneling to traps at the distance y from the Si/IL interface (in the interfacial layer), where $0 < y < y_1$
- (ii) Capture and emission process in the interfacial layer
- (iii) tunneling to traps at the distance y from the Si/IL interface (in the high- κ layer), where $y_1 < y < y_2$
- (iv) Capture and emission process in the high- κ layer

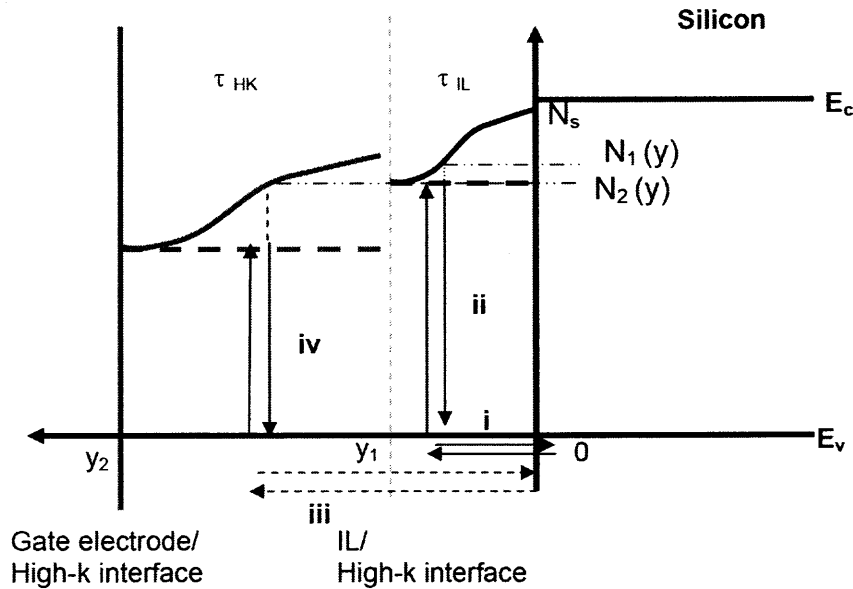


Figure A.2 Schematic picture of the capture and emission processes in dual layer high- κ gate stack. N_s is the trap density at the interface, while $N_1(y)$ and $N_2(y)$ are the density of empty traps in the interfacial and the high- κ layer.

The rate of capture and emission process would be different between the high- κ layer and the interfacial layer, due to the physical and material properties of these layers, and hence the trap time constant is expected to be different in these layers. But it has been well established experimentally that the interfacial layer has a strong influence on $1/f$ noise properties. Hence it is possible that the effect of high- κ layer is screened by the traps in the interfacial layer, or in other words these two processes are strongly correlated.

A.3 Estimation of Tunneling Time Constant based on Charge Fluctuations in the Interfacial Layer and High- κ Dielectric

The time constant in the interfacial and the high- κ layer is estimated by assuming either the change in the number of electrons or number of holes in their respective bandgaps:

The change in the number of holes per unit volume trapped at y is then given by:

$$\frac{\partial n_0}{\partial t} = \frac{\partial n_{IL}}{\partial t} + \frac{\partial n_{HK}}{\partial t} \quad (6.39)$$

where

$$\begin{aligned} \frac{\partial n_{IL}}{\partial t} &= N_1(y) f_p e_{p_{IL}}(y) - N_1(y) f_t c_{p_{IL}}(y) p_1 \\ \frac{\partial n_{HK}}{\partial t} &= N_2(y) f_p e_{p_{HK}}(y) - N_2(y) f_t c_{p_{HK}}(y) p_2 \end{aligned} \quad (6.40)$$

Where p_1 and p_2 are the density of holes at the IL/Si and IL/high- κ interfaces. At equilibrium,

$$\begin{aligned} N_1(y) f_p e_{p_{IL}}(y) &= N_1(y) f_t c_{p_{IL}}(y) p_1 \\ N_2(y) f_p e_{p_{HK}}(y) &= N_2(y) f_t c_{p_{HK}}(y) p_2 \end{aligned} \quad (6.41)$$

$$\begin{aligned} \frac{e_{p_{IL}}}{c_{p_{IL}}} &= \frac{p_1 f_t}{f_p} = p_{IL} \\ \frac{e_{p_{HK}}}{c_{p_{HK}}} &= \frac{p_2 f_t}{f_p} = p_{HK} \end{aligned} \quad (6.42)$$

Where

$$\begin{aligned} p_{IL} &= n_i e^{\frac{(E_i - E_{IL})}{kT}} \\ p_{HK} &= n_i e^{\frac{(E_i - E_{HK})}{kT}} \end{aligned} \quad (6.43)$$

Using (1.36) in equation (1.34)

$$\frac{\partial n_0}{\partial t} = (N_1(y) f_p e_{p_{IL}} - N_1(y) f_t c_{p_{IL}} p_1) + (N_2(y) f_p e_{p_{HK}} - N_2(y) f_t c_{p_{HK}} p_2) \quad (6.44)$$

Equation 1.39 may be written as:

$$\frac{\partial n_0}{\partial t} = e_{p_{IL}} [N_1(y) - n_1(y)] - c_{p_{IL}} p_1 n_1(y) + e_{p_{HK}} [N_2(y) - n_2(y)] - c_{p_{IL}} p_2 n_2(y) \quad (6.45)$$

Neglecting the variation due $N(y)*e_p$ it is seen that,

$$\frac{\partial n_0}{\partial t} = -[e_{p_{IL}} n_1(y) + c_{p_{IL}} p_1 n_1(y)] - [e_{p_{HK}} n_2(y) + c_{p_{IL}} p_2 n_2(y)] \quad (6.46)$$

Obtaining the fluctuation δn_0 from n_0 ,

$$\frac{\partial[\delta n_0(y)]}{\partial t} = -[e_{p_{IL}} + c_{p_{IL}} p_1] \partial[\delta n_1(y)] - [e_{p_{HK}} + c_{p_{HK}} p_2] \partial[\delta n_2(y)] \quad (6.47)$$

$$\frac{\partial[\delta n_0(y)]}{\partial t} = -[c_{p_{IL}} (p_{IL} + p_1)] \partial[\delta n_1(y)] - [c_{p_{HK}} (p_{HK} + p_2)] \partial[\delta n_2(y)] \quad (6.48)$$

With decay time constants,

For Interfacial Layer $\tau_{IL} = \frac{1}{[c_{p_{IL}} (p_{IL} + p_1)]} \quad (6.49)$

For high- κ Layer

$$\tau_{HK} = \frac{1}{[c_{p_{HK}} (p_{HK} + p_2)]} \quad (6.50)$$

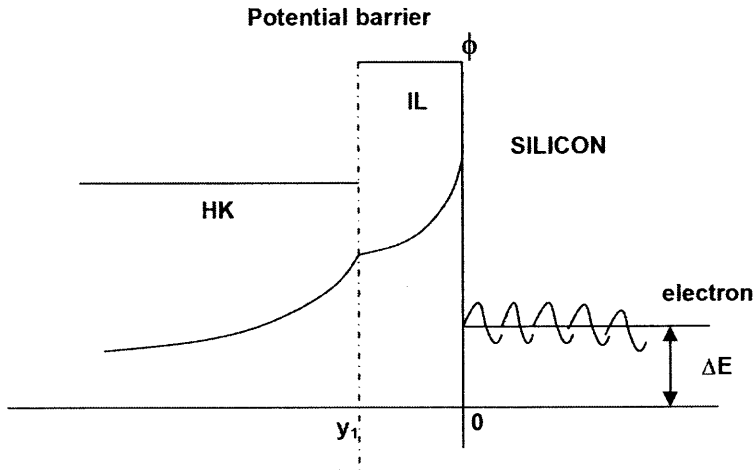


Figure A.3 Potential barrier to calculate the probability of finding an electron in the interfacial layer and the high- κ layer from the interface.

If it is now assumed that all traps have the same capture coefficient c , independent of y and assume the probabilities of finding an electron between $0 < y < y_1$ and $y_1 < y < y_2$ are $P_1(y)$ and $P_2(y)$, then the probability that a hole at the interfaces (Si/IL and IL/high- κ interface) will be captured by a trap from the interface is then given by:

$$\begin{aligned} c_{p_{IL}} &= cP_{IL}(y) \\ c_{p_{HK}} &= cP_{HK}(y) \end{aligned} \quad (6.51)$$

With a simple potential barrier shown in Figure 9 and neglecting the energy ΔE of the impinging electron,

$$\begin{aligned} P_{IL}(y) &= e^{-\alpha_{IL}y} \\ P_{HK}(y) &= e^{-\alpha_{HK}y} \end{aligned} \quad (6.52)$$

Then equation 1.44 and 1.45 becomes

$$\tau_{IL} = \frac{1}{c(p_{IL} + p_1)} e^{\alpha_{IL}y} \quad (6.53)$$

And

$$\tau_{HK} = \frac{1}{c(p_{HK} + p_2)} e^{\alpha_{HK}y} \quad (6.54)$$

where

$$\alpha_{IL} = \frac{2}{\hbar} \sqrt{2m_{IL}^* \phi_{IL}} \quad (6.55)$$

and

$$\alpha_{HK} = \frac{2}{\hbar} \sqrt{2m_{HK}^* \phi_{HK}} \quad (6.56)$$

$$\text{and } m_{IL} = m_{SiO_2}^* m_0 \text{ and } m_{HK} = m_{HfO_2}^* m_0$$

and numerically it is found to be

$$m_{HfO_2} < m_{SiO_2} \text{ and } \phi_{HK} < \phi_{IL}$$

The values of m_{HfO_2} and m_{SiO_2} are found to be $0.18m_0$ and $\sim 0.35m_0$ for electrons.

One way of estimating the total decay constant involving the two layers, is to assume that the density of empty traps in the high- κ and IL are the same as $n1 \sim n2 = n_0$, then equation, 1.43 would mean

$$\frac{\partial[\delta n_0(y)]}{\partial t} = [\tau_{IL} + \tau_{HK}] \partial[\delta n_0(y)] \quad (6.57)$$

and,

$$\tau_{net} = \tau_{0,IL} e^{\alpha_{IL}y} + \tau_{0,HK} e^{\alpha_{HK}y} \quad (6.58)$$

Simplifying further,

$$\tau_{net} = \tau_{GM} [e^{\alpha_{IL}y} + e^{\alpha_{HK}y}] \quad (6.59)$$

where

$$\tau_{GM} = G.M. [\tau_{0,IL}, \tau_{0,HK}] \quad (6.60)$$

A.4 Simulation Results

Based on the above derived results, numerical values were fitted based on the assumed values of capture probabilities and hole concentration in the interfacial and the high- κ layer. The results are summarized below:

(a) Estimation of trap time constant in the interfacial layer and high- κ dielectric:

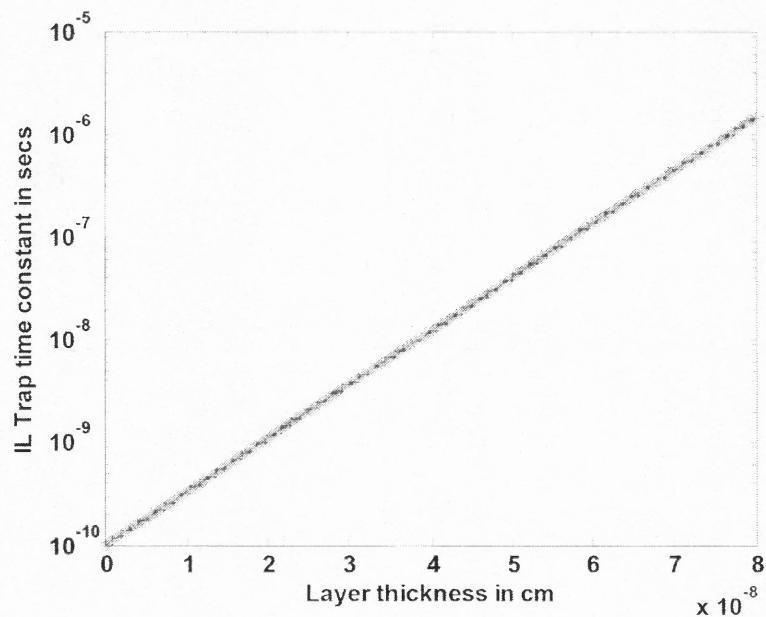


Figure A.4. Estimation of trap time constant at the interfacial layer. The initial value of $\tau_{0,IL}$ is estimated to be 1×10^{-10} secs.

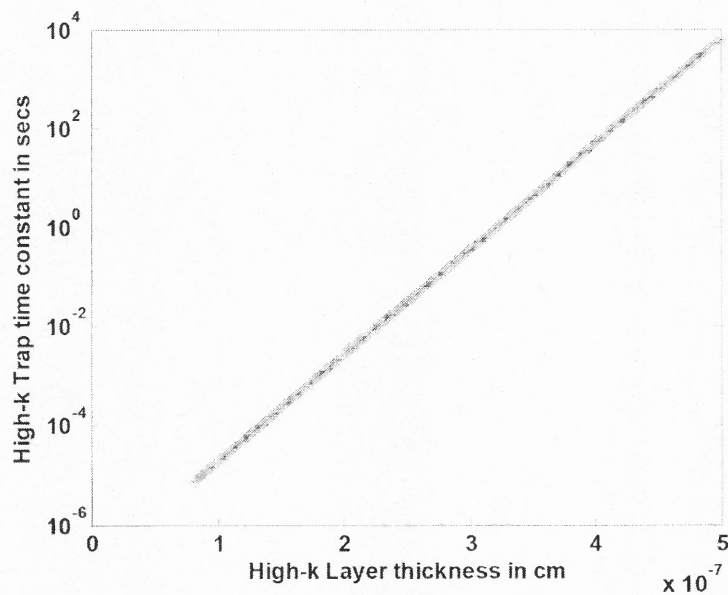


Figure A.5 Estimation of trap time constant at the interfacial layer. The initial value of $\tau_{0,IL}$ is estimated to be 1.5×10^{-7} secs.

(b) Estimation of total trap time constant:

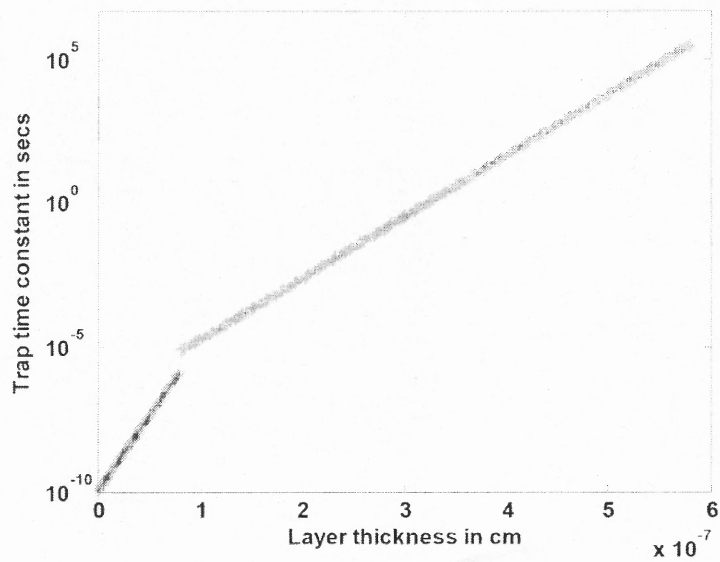


Figure A.6 Estimation of total trap time constant including the interfacial layer (Blue) and high- κ layer (Red).

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