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ABSTRACT

PLASMA INDUCED DAMAGE TO Si AND SiGe DEVICES AND MATERIALS

by
Wei Zhong

This thesis studied the plasma-induced damage to Si and strained $Si_{1-x}Ge_x$, and the resulting change in device characteristics. The energetic particles (ions, electrons and photons) in plasma reactor present a potentially hostile environment for processing VLSI devices. An inductively coupled plasma (ICP) reactor was used to study its damage effects to thin gate oxides. Electrical characterizations by C-V, ramped voltage breakdown (RVB) and deep-level transient spectroscopy (DLTS) measurement, and x-ray photoelectron spectroscopy (XPS) analysis were employed to investigate the damages to thin gate oxides and Si/SiO_2 interface. The shift of flat band voltage, the reduction of breakdown voltage and the creation of high interface trap density were found to be in good agreement with the creation of suboxidation states at Si/SiO_2 interface. It is observed that device damage is well associated with the reactor operating conditions. The major mechanism responsible for damage appeared to be high-energy electron charging which occurred when only the ICP power was activated, without any rf bias to the wafer-carrying electrode. Energetic particle bombardment damage was dominant when the wafer-carrying electrode was biased and the damage was considerably higher for rf bias power grater than 35W.

The effect of plasma processing to the strained $Si_{1-x}Ge_x$ layer of p^+- n diode has been investigated. The effect of SF_6 plasma, used to etch an overlying Si film stopping at the strained $Si_{1-x}Ge_x$ film, on the electrical properties of an underlying $Si_{1-x}Ge_x/Si$ heterojunction device was studied. The changes of C-V and I-V characteristics, such as

higher depletion capacitance and lower diffusion current were attributed to ion bombardment and radiation-induced bonding change, such as creation of interface charges and recombination centers. The TEM analysis revealed the dislocation loops in Si/$Si_{1-x}Ge_x$ /Si outside the aluminum contact region due to the ion bombardment stress. The O_2 plasma ashing has moderate effect to $Si_{1-x}Ge_x$ device when the device was protected by aluminum contact layer.

The C-V profiling techniques on SiGe MOS structures were used to investigate the change of valence band discontinuity (ΔE_V) at the Si/SiGe interface before and after plasma exposure and high temperature annealing. Wet and plasma etched samples were annealed at 500, 600, 700 and 800 °C for 60 seconds. It was observed that the accuracy of extracting the changes of ΔE_V using the C-V profiling was strongly influenced by the release of electrons from the traps at SiO_2/Si interface, which were created during the low-pressure CVD SiO_2 deposition. The device simulations have been used to confirm this finding. By carefully analyzing the C-V profile at slight depletion region the band gap modifications at back Si/SiGe interface due to process-induced damage could be evaluated. The dry etched sample was partially relaxed after 700 °C annealing while wet etched sample was partially relaxed after 800 °C annealing. Dry etched sample demonstrated a faster relaxation mechanism as compared to its wet etched counterpart due to the creation of dislocation loops by dry etching process. The C-V method is a simple, fast and efficient approach to estimate any band-gap modification in SiGe due to process-induced damage, but the measurements and simulations in slight depletion region should be carried out with special care and high resolution.

PLASMA INDUCED DAMAGE TO Si AND SiGe DEVICES AND MATERIALS

by
Wei Zhong

A Dissertation
Submitted to the Faculty of
New Jersey Institute of Technology
In Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy in Electrical Engineering

Department of Electrical & Computer Engineering

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APPROVAL PAGE

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TABLE OF CONTENTS

Chapter **Page**

1 INTRODUCTION 1

1.1 Motivation 1

1.2 Objectives of the Research 3

1.3 Thesis Organization 5

2 PLASMA ETCHING PROCESS AND PLASMA DAMAGE 7

2.1 Basic Physical Phenomena in RF Discharges 7

2.2 General Description of Plasma Etch Tools 12

2.3 Plasma Induced Damage to Silicon Devices 17

2.3.1 Plasma Damage to Si/SiO_2 System 17

2.4 Plasma Damage to $Si/Si_{1-x}Ge_x$ Heterojunction Systems 20

2.4.1 $Si_{1-x}Ge_x$ Material and Devices 20

2.4.2 Physical and Electrical Damage to Strained $Si_{1-x}Ge_x$ Devices.. 26

3 EXPERIMENTAL TECHNIQUES 27

3.1 Electrical Characterization 27

3.1.1 I-V & C-V Measurements to Evaluate MOS System 27

3.2 Deep Level Transient Spectroscopy (DLTS) Techniques 33

3.3 Physical Characterization 41

3.3.1 Secondary Ion Mass Spectroscopy (SIMS) 41

3.3.2 X-Ray Photoelectron Spectroscopy (XPS) 42

3.3.3 Transmission Electron Microscopy (TEM) 44

3.4 Simulation of $Si_{1-x}Ge_x$ Device for Damage Estimation 46

3.4.1 Overview of Device Simulator 46

TABLE OF CONTENTS
(Continued)

Chapter | Page

3.4.2 Important Physics and Equations in SiGe MOS Simulation .. 47

3.4.3 Simulation of $Si_{1-x}Ge_x$ MOS Capacitor ... 50

4 ETCH-INDUCED DAMAGE TO MOS DEVICE IN HIGH-DENSITY ICP ETCHING REACTOR ... 55

4.1 Introduction ... 55

4.2 Experimental Details ... 56

4.3 Measurement Results ... 60

4.3.1 C-V Measurements ... 60

4.3.2 Breakdown Measurements ... 64

4.3.3 DLTS Analysis ... 65

4.3.4 XPS Characterization ... 67

4.4 Discussion of Results ... 70

4.5 Summary ... 71

5 PLASMA INDUCED DAMAGE TO STRAINED $Si_{1-x}Ge_x$ ... 72

5.1 Electrical Studies on SF6 and O2 Plasma Etched $Si_{1-x}Ge_x$ p^+-n Heterojunction ... 72

5.1.1 Sample Preparation ... 73

5.1.2 Current-Voltage Measurements ... 76

5.1.3 C-V Measurements ... 77

5.1.4 TEM Analysis ... 77

5.1.5 Effects of O_2 Plasma Ash Process ... 78

TABLE OF CONTENTS
(Continued)

Chapter **Page**

5.1.6 Summary 79

5.2 Evaluation of Plasma Process-Induced Bandgap Modification of Strained $Si_{1-x}Ge_x$ Heterojunction Using MOS Capacitor 80

5.1.1 Sample Preparation 80

5.1.2 C-V Measurements 82

5.1.3 Device Simulation 84

5.1.4 Discussion of Results 95

5.1.5 Summary 97

6 CONCLUSIONS 98

6.1 Suggestions for Future Work 100

APPENDIX EXAMPLE OF ATLAS INPUT FILE 101

REFERENCES 103

LIST OF TABLES

Table **Page**

4.1 A list of the various processing conditions 57

5.1 List of simulated SiGe MOS structures 85

LIST OF FIGURES

Figure		Page
2.1	Schematic view of a dc glow discharge showing the most prominent regions of the discharge	8
2.2	Schematic view of rf discharge	10
2.3	Schematic diagram of (a) diode and (b) triode reactor configurations	13
2.4	Basic steps in a dry-etching processing	15
2.5	Illustration of an inductively coupled plasma reactor	16
2.6	Energy band diagram for thermal SiO_2 layer on an underlying Si substrate exposed to low-energy ions and photos which are present in an RIE	18
2.7	Idealized model for the space-charge build-up as a function of time during Irradiation of a MOS structure under a positive gate bias	19
2.8	Energy bandgap versus lattice constant	20
2.9	Strained and unstrained SiGe layer	21
2.10	Critical thickness versus Ge content	22
2.11	Energy band diagram of graded-base SiGe HBT compared to a Si BJT	24
2.12	(a) A fully pseudomorphic pMOS layer configuration with typical design parameter. (b) The quantum well for holes and inversion of the n- SiGe layer under a sufficiently high negative gate voltage	24
3.1	To illustrate the operation of an MOS capacitor, capacitance as a function of bias, and the corresponding energy-band diagrams are shown in accumulation, depletion, inversion, and at flatband	29
3.2	Normalized high frequency and low frequency capacitance as a function of gate bias calculated for and acceptor concentration of 2×10^{16} cm^{-3}, oxide thickness 100nm, and T=300 K	30
3.3	(a) Low frequency equivalent circuit of MOS, (b) high frequency equivalent circuit of MOS	31
3.4	Combined (a) high frequency (1MHz) and (b) low frequency C-V curves for a MOS capacitor	32

LIST OF FIGURES
(Continued)

Figure **Page**

3.5 Typical time dependence involved in pulsed bias capacitance transients for majority- and minority carrier traps 35

3.6 Injection pulse sequence which is used to produce a capacitance transient for a minority-carrier trap 36

3.7 Majority-carrier pulse sequence which is used to produce a capacitance transient for a majority-carrier traps 36

3.8 Illustration of how a double boxcar is used to define the rate window........ 38

3.9 Thermal emission rates vs *1000/T* determined from the DLTS spectra 39

3.10 Schematic diagram of a secondary ion mass spectrometer 41

3.11 SiGe MOS capacitor structure used for simulation 51

3.12 Simulated device structure with mesh 51

3.13 Atlas command group with primary statements in each group 52

3.14 Use Tonyplot to display the C-V plot 53

3.15 Use Tonyplot to display the energy diagram cross the MOS capacitor under certain bias condition 54

4.1 A schematic diagram of the ICP reactor 57

4.2 Normalized C-V characteristics of various samples: (a) immediately after metal deposition; (b) after a 10 minutes annealing at 280°C in N_2 ambient 62

4.3 Quasi-static C-V curves for MOS capacitors after plasma etching in an ICP reactor with different process conditions 63

4.4 The breakdown distribution of various samples 64

4.5 DLTS spectra for the control sample #1 and the plasma etched sample #4........ 66

4.6 Interface traps density N_{ss} in the plasma etched sample (#4) as a function of energy 66

4.7 XPS spectra of various samples 68

LIST OF FIGURES
(Continued)

Figure		Page
4.8	XPS counts for various suboxide states	69
5.1	Scanning electron microgragh of the RTCVD wafer	72
5.2	SIMS profiles for as-grown RTCVD sample	74
5.3	Wet etching results	74
5.4	Device structures were used for study and comparison	75
5.5	The I-V characteristics of wet etched sample #1 and SF6 plasma etched sample #2	76
5.6	The C-V characteristics of wet etched sample and SF_6 plasma etched sample	77
5.7	(a) High resolution TEM of Si/ $Si_{1-x}Ge_x$ /Si interface after plasma (b) Weak beam dark field TEM microgragh showing the dislocation loops	78
5.8	The I-V characteristics of unetched sample#3 and O_2 plasma ashed sample#4.	79
5.9	Typical structure of MOS capacitor used in this study	80
5.10	Schematic band diagram under the slight depletion condition (a) and the accumulation condition (b)	81
5.11	Typical C-V profiles obtained for the wet etched samples	83
5.12	Typical C-V profiles obtained for the dry etched samples	84
5.13	Simulated C-V plots of SiGe MOS capacitors with different energy bandgap values	87
5.14	Energy band diagram in G1 and G2 under –0.5V bias	88
5.15	Hole concentration in G1 and G2 under –0.5V bias	89
5.16	Energy band diagram in G1 and G2 under –1.25V bias	89
5.17	Hole concentration in G1 and G2 under –0.5V bias	90

LIST OF FIGURES
(Continued)

Figure **Page**

5.18 Simulated C-V plots of SiGe MOS capacitor with SiO_2 fixed positive charges 91

5.19 Simulated C-V plots of SiGe MOS capacitor with SiO_2 interface traps (with different trap densities and different trap energy levels)..................... 93

5.20 Simulated C-V plots of SiGe MOS capacitor with SiO_2 fixed positive charges and interface traps to match Figure 5.11... 94

5.21 Simulated C-V plots of $Si_{1-x}Ge_x$ MOS capacitor with additional relaxed structures (G9', G10', G11' and G12') for comparison............................ 94

5.22 Zoomed plot of Figure 2.1 at slight depletion region............................... 96

CHAPTER 1

INTRODUCTION

1.1 Motivation

This is a silicon world. Greater than 95% of today's $200 billion plus global semiconductor market uses the semiconductor silicon (Si) to realize a host of integrated circuits (IC) ranging from 1 GHz microprocessors to 64 Mb dynamic random-access memory (DRAM) chips. Si has a number of practical advantages over the other numerous semiconductors, including: 1) an extremely high-quality dielectric (SiO_2) can be easily grown on Si and used for isolation, passivation, or as an active layer (e.g., gate oxide); 2) Si can be grown in very large, virtually defect-free single crystal (200 mm in production today, rapidly moving to 300 mm), yielding many (low-cost) IC's per wafer; 3) Si has excellent thermal properties allowing for the efficient removal of dissipated heat; 4) Si can be controllably doped with both n- and p-type impurities with extremely high dynamic range (10^{12}-10^{22} cm^{-3}); 5) Si has excellent mechanical strength, facilitating ease of handling and fabrication; 6) it is easy to make very low-resistance ohmic contacts to Si, thus minimizing device parasitics; and 7) Si is extremely abundant and easily purified. Thus, from IC manufacturing standpoint, Si is a dream come true.

Introducing Ge into Si has a number of consequences. First and most importantly, because Ge has a larger lattice constant than Si, the energy bandgap of Ge is smaller than that of Si (0.66 eV versus 1.12 eV), thus $Si_{1-x}Ge_x$ has a bandgap smaller than that of Si, making it a suitable candidate for bandgap engineering in Si. In addition, the compressive strain lifts the conduction and valence band degeneracies at the band extremes, effectively reducing the density of states and improving the carrier mobility with respect

to pure Si (the latter due to a reduction in carrier scattering). The $Si_{1-x}Ge_x$ heterojunction combines heterojunction device performance with silicon manufacturability. It has been the subject of many investigations in recent years.

A series of Si-compatible hetero-structure devices, based on epitaxial growth in the $Si/Si_{1-x}Ge_x$ system, has stirred a strong interest for high-speed devices. The narrow band gap of strained $Si_{1-x}Ge_x$ has been used to fabricate heterojunction bipolar transistors (HBT's) [1, 2], modulation-doped field effect transistors (MODFET's) [3], long wavelength optoelectronics devices [4, 5], and tunneling and superlattice devices. Due to the lattice mismatch between silicon and germanium, the $Si_{1-x}Ge_x$ film gown on silicon is strained up to a critical thickness. It is very important to preserve the quality of these heterojunctions throughout the fabrication process.

Dry etching techniques such as reactive ion etching (RIE), magnetron reactive ion etching (MRIE), plasma etching (PE), ion beam etching (IBE), electron cyclotron resonance (ECR) etching, reactive ion beam etching (RIBE) and inductively coupled plasma (ICP) etching can cause damage and contamination effects in exposed materials [6-18]. In fact, damage is often inherent in these processes due to the presence of ion bombardment, which can create bonding damage in semiconductors and insulators [6-14, 16, 18], as well as due to the presence of UV radiation, which can create bonding damage in insulators [15]. Contamination is also often inherent in these processes due to the presence of residue layers made up of reactant species and reaction products and due to the presence of impurities which may permeate the etched material during the dry etching exposure [8, 9, 16-22]. Inductively coupled plasma sources have emerged as the most used in plasma etchers. They are capable of uniform etching of anisotropic features over

large area wafers at etch rates comparable to conventional high-pressure capacitively coupled reactive ion etching tools. The ion energies incident on the wafers can be effectively decoupled from plasma generation by independently applying rf power to the wafer chuck.

The reliability and electrical performance of these Si devices and strained $Si/Si_{1-x}Ge_x$ hetero-structure devices may be significantly affected by plasma processing during device manufacturing. Creation of strain-relieving misfit dislocation and/or threading dislocations [23] may be possible when strained $Si_{1-x}Ge_x$ films are processed using reactive ion etching. Though reactive ion etching of Si has been studied the impact of inductively coupled plasma on Si device are still unfolding. Besides not much is known about the modifications to electrical characteristics of strained $Si_{1-x}Ge_x$. It is very important to show that how the plasma process affects the strained $Si_{1-x}Ge_x$ hetero-structure material and devices.

1.2 Objectives of the Research

The overall goal of the research carried out for this thesis has been to obtain a basic understanding of plasma induced electrical and physical damages to Si and SiGe devices leading to the optimization of plasma etch process and development of next generation plasma etch tools suitable for sub-micro heterojunction devices. The investigation has been focused on studying the issues related to device physics with the objective of gaining a fundamental understanding of the damage mechanisms of the associated plasma etching.

This broad objective of this program has been achieved by carrying out research in two key areas. Firstly, by using well known Si MOS device to evaluate the plasma induced damage in advanced ICP reactor; and secondly by applying the similar testing techniques and the device simulations to SiGe p^+-n diode and SiGe MOS devices.

Electrical and physical characterizations, such as I-V, C-V, Deep Level Transient Spectroscopy (DLTS), Transmission Electron Microscopy (TEM), X-Ray Photoelectron Spectroscopy (XPS), were used to study the plasma induced damages in ICP reactor. These studies were aimed at establishing the correlation between and electrical and physical damage, and developing basic understanding of damage mechanisms.

C-V profiling on $Si_{1-x}Ge_x$ MOS capacitor is potentially powerful method to estimate plasma process-induced band-gap modifications. The presence of interface trap has significantly influenced the measurement result. In this thesis, the utility of device simulator is demonstrated by the insights gained into the underlying mechanisms of space charge and surface-state charge between heterojunction semiconductor and insulator. The finding of the influence of interface traps has been simulated and it correlates with the measurement result well.

The results of this work have significant technological consequences and applications. For example, the fundamental understanding of etch induced damage to thin gate oxide in ICP reactors will enable their widespread usage by integrated circuit manufactures. In addition, the testing and simulation results of $Si_{1-x}Ge_x$ device in this thesis will help to develop new methods of detection and approaches of damage control of plasma induced damage in $Si_{1-x}Ge_x$ materials and devices.

1.3 Thesis Organization

Chapter 2 reviews basic physic phenomena in RF glow discharges, plasma etching tools, and the fundamental understanding of plasma induced damage to Si and SiGe devices. The background of SiGe technology is also described in that chapter.

Chapter 3 describes electrical and physical measurement techniques that have been used for this research. That includes I-V, C-V, DLTS developed as a part of this thesis work, SIMS, XPS and TEM. The knowledge of these techniques will lead to understand and interpret the research results in this thesis. In addition an overview of device simulation relevant to this work is presented in that chapter.

The research results of etch induced damage to thin oxide in ICP reactor have been described in Chapter 4. This work was done as part of project funded by SEMATECH Center of Excellence in New Jersey. It is observed that device damages are well associated with the operating conditions of the reactor.

Chapter 5 outlines the research results of process induced damage to strained $Si_{1-x}Ge_x$ material and devices. This work was done as part of project funded by the National Science Foundation (grant No. ECS-9207665). It is found that SF_6 plasma used to etch an overlying Si film stopping at the SiGe strained film can cause electrical damage to Si/SiGe heterojunction device. The O_2 photo-resistor strip process has no strong effect on the SiGe device due to the protection from its aluminum contact layer. The presence of interface trap at SiO_2 deposited by low-pressure CVD process creates big kink at C-V profile at accumulation region of SiGe MOS capacitor. The C-V curves were affected by the reduction of trap densities as well as the reduction of ΔE_v due to relaxation after

annealing. Dry etched sample demonstrates a faster relaxation mechanism as compared to its wet etched counterpart due to the creation of dislocation loops by dry etching process.

Chapter 6 is the conclusions of this research and the suggestions for future works. An example of Atlas input file of an ideal SiGe MOS capacitor is presented in Appendix. For the purpose of clarity, Chapters 5 and 6 have their own introduction and summary sections.

CHAPTER 2

PLASMA ETCHING PROCESS AND PLASMA DAMAGE

A plasma is defined as a partially ionized gas composed of ions, electrons and a variety of neutral species. It contains approximately equal concentrations of positively charged particles (positive ions) and negatively charged particles (electrons and negative ions). The plasma useful to ULSI processing is a weakly ionized plasma, called a "glow discharge", containing a significant density of neutral particle - more than 90% in most etchers.

2.1 Basic Physical Phenomena in RF Discharges

When an electric field of sufficient magnitude is applied to a gas, the dissociation of gas occurs. The process begins with release of an electron by some means such as photo-ionization or field emission. The released electron is accelerated by applied field and gains kinetic energy, but in the course of its travel through the gas, it loses energy in collision with gas molecules. There are two types of collisions, elastic and inelastic. Elastic collisions deplete very little of electron's energy, because of the great mass difference between electrons and molecules. Ultimately the electron energy becomes high enough to excite or ionize a molecule by inelastic collisions. In ionizing collisions the electrons loses essentially all of its energy. Ionization frees another electron, which is accelerated by the field, and so the process continues. If the applied voltage exceeds the breakdown potential, the gas rapidly becomes ionized through its volume.

Electrons released in ionizing collisions and by secondary processes are lost from the plasma by drift and diffusion to the boundaries, by recombination with positive ions,

and, in certain electronegative gases, by attachment to neutral molecules to form negative ions. The discharge reaches a self-sustained steady state when electron generation and loss processes balance each other. Non-ionizing, inelastic collisions between electrons and gas molecules or atoms also occur. Two important types of nonionizing collision are electronic excitation of molecules (or atoms) and molecular fragmentation. Electronically excited molecules and atoms account for much of the luminous glow of the plasma by emitting photons as they relax to lower-lying electronic states. Molecular fragments are often highly reactive atoms and free radicals. A free radical is a molecular fragment having an unpaired electron.

The simplest discharge to produce is the glow discharge, in which a dc potential is applied between two metal electrodes in a partially evacuated enclosure. The discharge is visibly non-uniform between the electrodes and is composed of a series of luminous light and dark zones, shown in Figure 2.1.

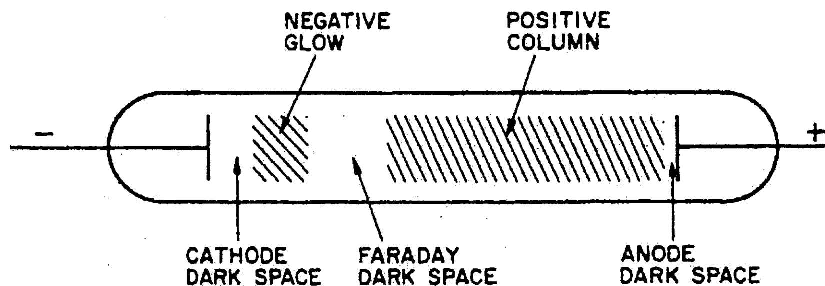


Figure 2.1 Schematic view of a dc glow discharge showing the most prominent regions of the discharge (after S. M. Sze, Ref. 24).

If a low-frequency alternating field is applied across the electrodes in Figure 2.1 their polarity changes every half-cycle so that each electrode alternates as cathode. The ions and electrons can both follow the filed and establish a glow discharge identical to

that of dc discharge, except for periodic polarity reversal. As the frequency of the applied field is increased, the ions created during breakdown cannot be fully extracted from the gap prior to field reversal. As the frequency is increased further, a large fraction of the electrons have insufficient time to drift to the positive electrode during a half-cycle. These electrons then oscillate in the inter-electrode gap and undergo collision with gas molecules. The lower limit of frequency for oscillation depends on the electron mobility, the electrode spacing, and the amplitude of the applied field. The frequency limit is typically the rf range.

Three advantages are realized with rf discharges, which make their use widespread. First, electrons can pick up sufficient energy during their oscillation in the gap to cause ionization. The discharge can thus be sustained independent of the yield of secondary electrons form the walls and electrodes, Second, the probability of ionizing collisions is enhanced by electrons allowing operation at pressures as low as ~10^{-3} Torr. The third advantage is that electrodes within the discharge can be covered with insulating material. This permits sputter etching and reactive sputter etching of insulators, and also eliminates problems due to the build-up of insulating material on metal electrodes that can occur when reactive gases are employed in plasma etching.

The potentials that develop at various points in the rf discharge are important in determining the energies of ions incident on surface in the plasma. Three potentials pertinent to various etching techniques are labeled in Figure 2.2. V_t is the potential at the surface of the rf-powered electrode measured with respect to ground. V_p is the plasma potential with respect to ground, V_f is the potential (relative to ground) of an electrically floating surface, such as an insulating wall or a substrate isolated form ground by an

insulating film. The potential of the surface with respect to the plasma determines the maximum possible energy of ions bombarding that surface. To a first approximation, the rf coupling across the ion sheaths is capacitive, with the area and thickness of a sheath determining the capacitance. For this reason, the ratio R of the area of the rf-powered electrode to the area of all ground surfaces in contact with the plasma is a key parameter in determining how the applied voltage is distributed among the ion sheaths. The potential V_p-V_t increases as R decreases. As a practical consequence, this relationship means that sputter etching which requires relatively large V_p-V_t, is most efficient when R is small and the substrate forms or is attached to the rf-powered electrode (the target).

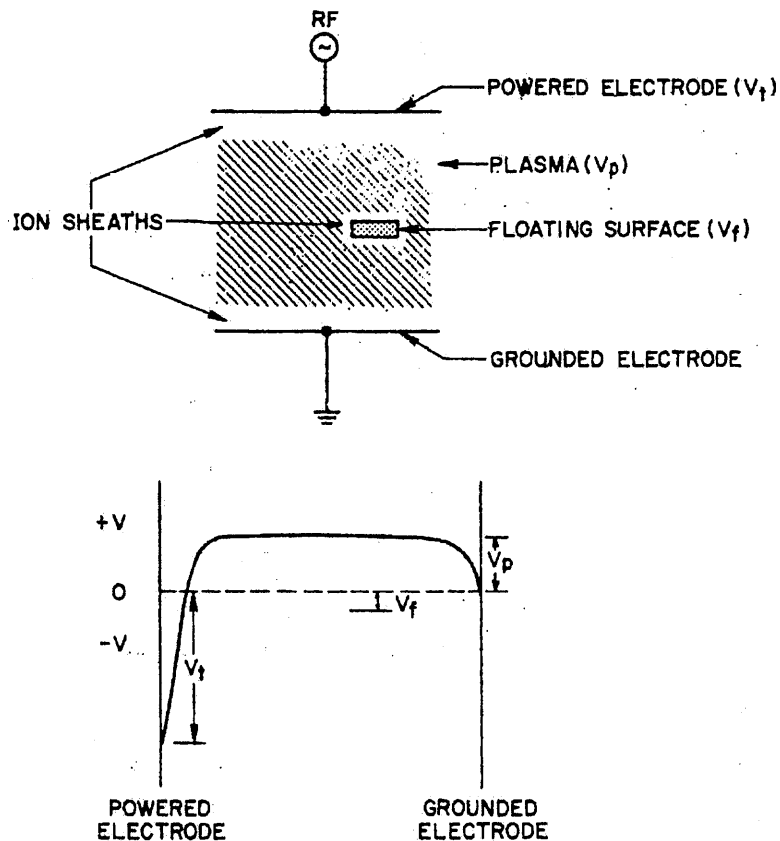


Figure 2.2 Schematic view of rf discharge (after S. M. Sze, Ref. 24).

Under the same conditions the ground-electrode ion sheath has a comparatively small potential drop V_p across it. Therefore very little or no sputtering occurs there. Plasma-etching system tend to be more symmetric (R ~0.5) and operated at higher pressure (usually in the 0.1- to 1.0-torr range). Hence the potential across the ion sheaths, including the powered electrode, are on the order of V_p (less than 100 V). The floating potential, V_f is usually only a few volts below ground. Therefore, ions bombarding on a floating surface do not usually have energies much greater than V_p.

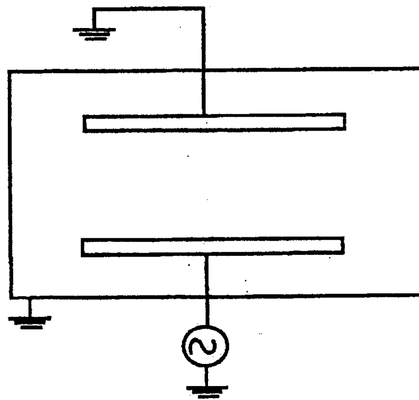
2.2 General Description of Plasma Etch Tools

In the plasma etching literature, various terms such as plasma etching (referred to etching wafer placed on ground electrode in a relative high pressure plasma) and reactive ion etching or reactive sputter etching (referred to etching wafer placed on powered electrode in a relatively low pressure plasma) are used extensively to describe various process conditions. However, plasma etching term is widely used today to describe all process conditions because it is a well accepted fact now that ions are rarely the etchant and neutrals are responsible for almost all reactive etching [25]. In this thesis, the term plasma etching is used instead of reactive ion etching to describe low pressure etching processes.

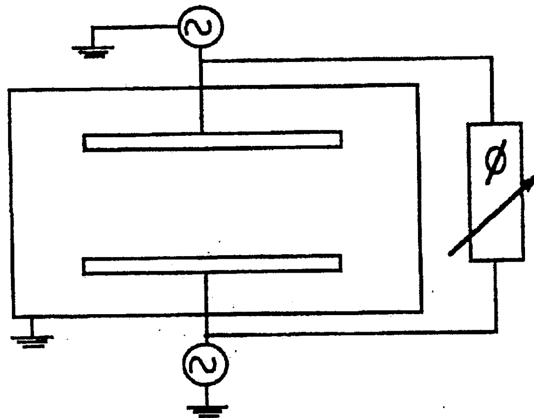
Parallel-plate configurations are widely used in a single wafer etcher due to their simplicity and ability to direct energetic ions normal to the surface being etched. Production etching systems can have a variety of configurations depending on the parameters of a process needed to be controlled as well as the specific applications of the system. The most common, commercially used, single wafer etching tool configuration today is the parallel-plate planer diode (Figure 2.3 (a)). One of the two electrodes of the diode configuration is capacitively coupled to the rf power supply through an impedance matching network and the other electrode is grounded. The frequency of the rf power supply can range from several kHz to several MHz [26]. However, the most common commercially used frequency is 13.56 MHz (an industry standard reflecting FCC regulations) and discussion in this thesis is limited only to the plasma process occurring in a 13.56 MHz discharge. The major limitation of the diode configuration is the strong coupling between the plasma generation and the induced bias. As the power is increased

to enhance ionization in plasma, the induced bias also increases and can cause substantial substrate damage.

Triodes, as their name implies, are tri-electrode discharge systems. In triodes (see Figure 2.3b), two of the three electrodes are powered while the third electrode is normally at the ground potential. The plasma parameters (ion energy, electron temperature and charged particle concentrations) can be somewhat independently varied in a triode relative to an equivalent diode system [27].



(a) Diode



(b) Triode

Figure 2.3 Schematic diagram of (a) diode and (b) triode reactor configurations (after V. Patel, Ref. 28).

The extensive use of plasmas to active etch processes derives from two major features of low-temperature non-equilibrium discharge. The first of these is the existence of energetic electrons with average energies in the range of 2 to 10 eV in the plasma volume. These electrons break bonds to form chemically active etchant species or their precursors. The electrons are also responsible for ionization, which sustains the discharge and creates ions. These ions are often essential to the etch process. The second important feature of plasmas for etching applications is the acceleration of ions at the plasma boundary. In many configurations, the ions are accelerated by the electric field in the sheath region between the plasma boundary and wafer. This field can accelerate ions, normal to the wafer surface, with typical energies in the range of 50 to 1000 eV. The ion bombardment often results in mechanisms that allow lithographic patterns to be etched anisotropically with little or no lateral removal of materials. This feature is essential to realization of increasing device density in modern integrated circuits, and is perhaps, the major reason why plasma activated etching is used so extensively.

The plasma etching process proceeds in five steps as illustrated in Figure 2.4 (1). The process begins with generation of the etchant species in the plasma. (2) The reactant is then transported by diffusion through a stagnant gas layer to the surface. (3) The reactant is adsorbed on the surface. (4) This is followed by chemical reaction (along with physical effects such as ion bombardment) to form volatile compounds. (5) These compounds are desorbed from the surface, diffused into the bulk gas, and pumped out by the vacuum system.

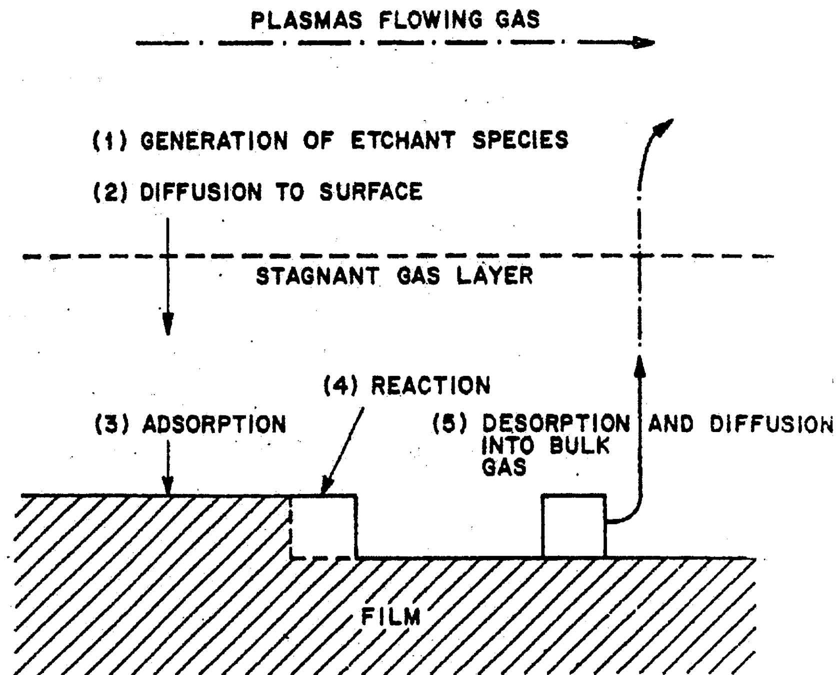


Figure 2.4 Basic steps in a dry-etching processing (after S. M. Sze, Ref. 29).

As the features for ULSI continue to decrease, the limits of the conventional rf capacitive-coupled parallel system are being approached. Other types of high-density plasma sources, such as inductively coupled plasma (ICP) sources or helicon plasma sources, may become the main plasma sources for future ULSI processing. An inductively coupled plasma source, shown in Figure 2.5, generates high-density, low-pressure plasma that is decoupled for the wafer, and it allows independent control of ion flux and ion energy [73]. Plasma is generated by a flat spiral coil that is separated from the plasma by a dielectric plate on the top of the reactor. The wafer is located several skin depths away from the coil, so it is not affected by the electromagnetic field generated by the coil. There is little density loss because plasma is generated only a few mean free paths away from the wafer surface. Therefore, a high-density plasma and high etch rates

are achieved. The ion potential in ICP is more than 20 eV while the average electron temperature is about 3-6 eV [74].

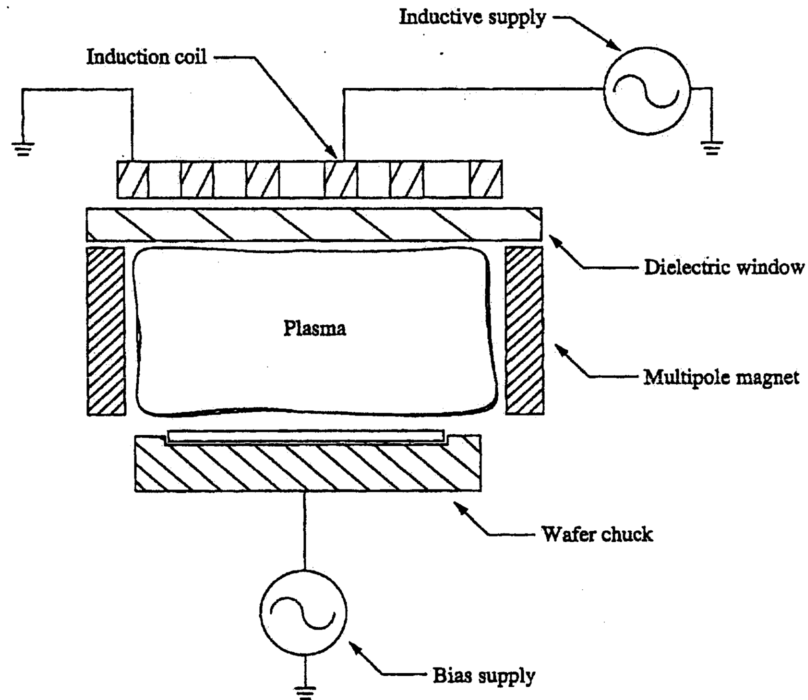


Figure 2.5 Illustration of an inductively coupled plasma reactor (after Keller, Forster, and Barnes, Ref. 73).

2.3 Plasma Induced Damage to Silicon Devices

Due to its advantages mentioned in previous chapter, plasma etching is a key process in VLSI circuit fabrication. Unfortunately plasma exposure also deleteriously affects semiconductors and insulators since it can result in (1) intrinsic bonding damage, (2) etching species and impurity permeation, and (3) residue or surface film formation. These damages and contamination effects lead to anomalous electrical behavior for metal/silicon contacts to etched Si surface and increased neutral trap density, increased positive charge, and increased interface state density for SiO_2. This section will mainly focus on the plasma induced damages to SiO_2 and Si/SiO_2 interface, while the damages induced in Si by dry etching can be found in Ref. 30 and its references.

2.3.1 Plasma Damage to Si/SiO_2 System

The variety of energetic particles (ions, electrons, and photons) present in a plasma creates a potentially hostile environment for processing VLSI devices. The gate oxide and the SiO_2-Si interface are particularly susceptible to damage by irradiation with these particles [31,32].

The damage can take several forms (as shown in Figure 2.6): (1) atomic displacement resulting from energetic ion impact; for reactive etching this usually limited to a region no more than 10 nm below the exposed surface; (2) primary ionization where Si-O bonds are broken and electron-hole pairs formed; this process is caused mainly by deep UV photons and soft x-rays, and (3) secondary ionization where electrons created by atoms displacement or primary ionization interact with defects in the Si-O network. Each of these forms of damage produces similar electronic defects-trapped positive charge and

neutral traps [33]. These damages will be fatal in long terms to thin insulators such as MOSFETs gate dielectrics and capacitor insulators.

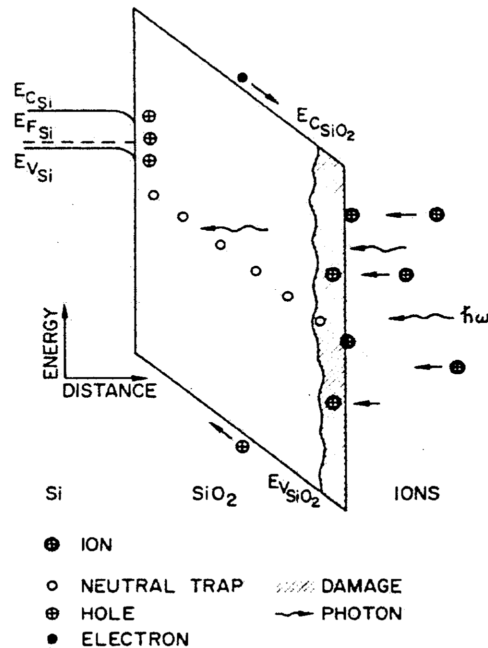
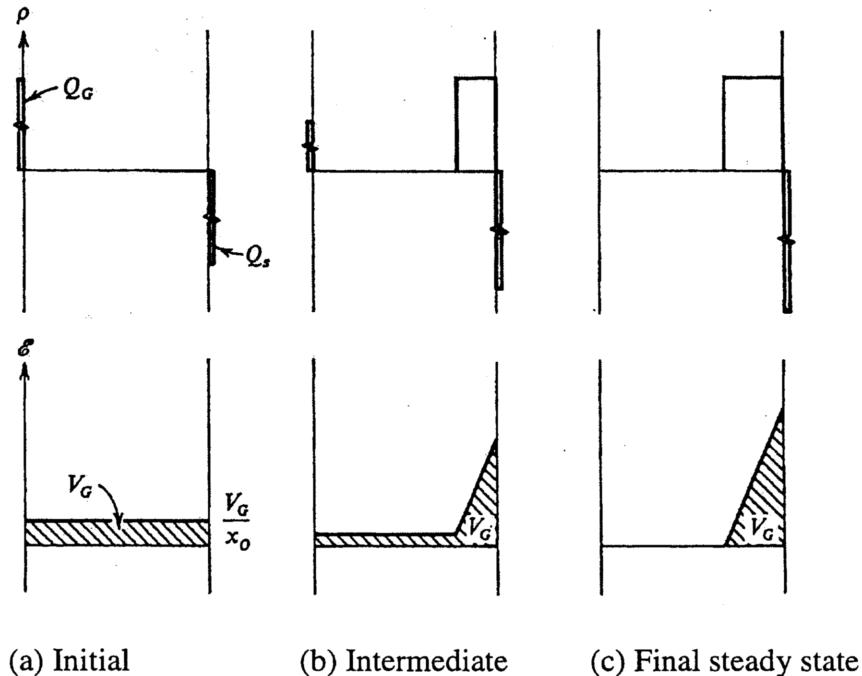


Figure 2.6 Energy band diagram for thermal SiO_2 layer on an underlying Si substrate exposed to low-energy ions and photos which are present in an RIE (Ref. 33).

An idealized model for the build-up of such positive space charge in the oxide under ionizing radiation exposure is as follows in Figure 2.7 [35]. During irradiation, electron-hole pairs will be generated in the oxide. If there is no electric field present in the oxide, the electrons and holes will recombine, resulting in no net charge building up in the oxide. However, if there is an electric field present in the oxide, this field will tend to separate the electrons and holes. In particular, a field corresponding to a positive gate voltage will tend to pull electrons toward the gate electrode, where most flow out into the external circuit. Very few electrons become trapped in the oxide. Holes drift much more slowly toward the negative electrode. If no electron can enter interface from the silicon into the oxide, trapping of the holes near the oxide-silicon interface will result in a

gradual build-up of a space charge. Due to the increased electric field, an increasing fraction of the total applied voltage will be dropped across this space-charge region. Thus as the space charge grows, eventually the field in the rest of the oxide layer is brought to zero.



(a) Initial (b) Intermediate (c) Final steady state

Figure 2.7 Idealized model for the space-charge build-up as a function of time during irradiation of a MOS structure under a positive gate bias. [Ref. 35]

High-temperature annealing (1000 °C in N_2) removes the atomic displacement damage, but trapping sites related to the implanted ions are still present [34]. Photo damage is manifested as trapped holes and neutral traps. The trapped holes can be removed by annealing at 400 °C, whereas removal of the neutral traps requires annealing at 600 °C or more. Therefore they can not be removed when Al electrodes or contacts are already in place. It has also been demonstrated that the latent damage will reappear easily by hot carriers and the device performance will be degraded soon [36].

2.4 Plasma Damage to Si/$Si_{1-x}Ge_x$ Heterojunction Systems

2.4.1 $Si_{1-x}Ge_x$ Material and Devices

Figure 2.8 shows the energy bandgap as a function of lattice constant for several elemental and compound semiconductors. Since AlAs and GaAs have similar lattice constant, the ternary alloy AlGaAs has essentially the same lattice constant over the entire range of compositions from AlAs to GaAs. As a result, one can choose the composition x of the ternary compound $Al_xGa_{1-x}As$ to fit the particular device requirement and grow this composition on a GaAs wafer. The resulting epitaxial layer will be lattice matched to the GaAs substrate.

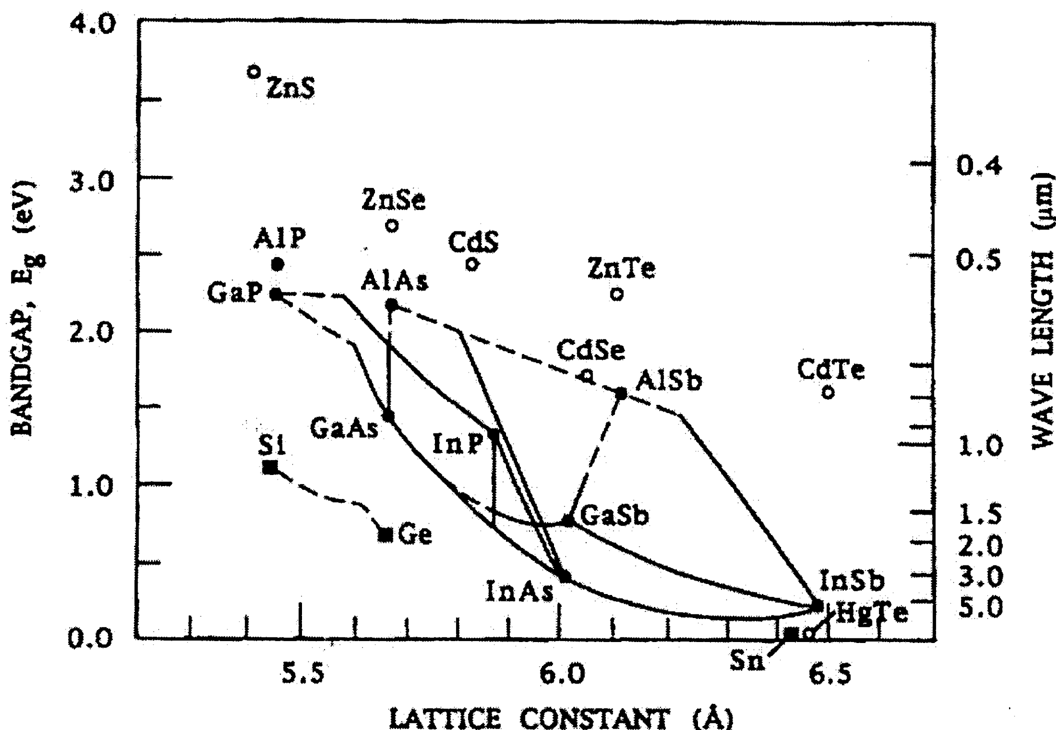


Figure 2.8 Energy bandgap versus lattice constant (after Jalali and Pearton, Ref. 37).

In addition to the widespread use of lattice-matched epitaxial layer, the advanced epitaxial growth techniques allow for the growth of very thick layer of lattice-mismatched crystal. If the mismatch is only a few percent and the layer is thin, the epitaxial layer grows with a lattice constant in compliance with that of the seed crystal. The resulting layer is in compression or tension along the surface plane as its lattice constant adapts to the substrate crystal. Such a layer is called *psedomorphic* because it is not lattice matched to the substrate without strain. An unstrained SiGe layer is compared with a strained SiGe layer on the Si substrate shown in Figure 2.9. For the relaxed layer there will be many dislocations at the interface.

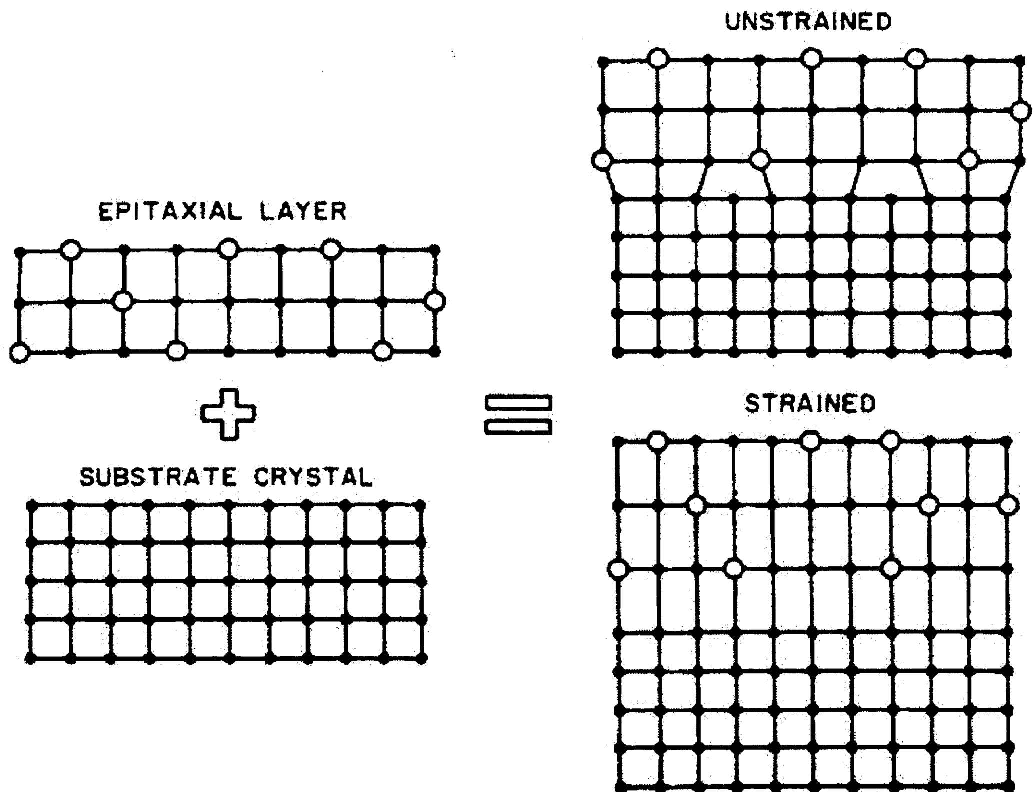


Figure 2.9 Strained and unstrained SiGe layer (Ref. 38).

The thickness of the $Si_{1-x}Ge_x$ layer is important device design consideration. The maximum thickness for psedomorphic growth (the critical thickness) of $Si_{1-x}Ge_x$ alloys is an important property of the system. Van der Merwe [39] introduced the concept of critical thickness based on equilibrium theory. He defined critical thickness as the film thickness below which it was energetically favorable to contain the misfit by elastic energy stored in the distorted crystal and above which it was favorable to store part of energy in misfit dislocation at the heteroepitaxial interface. Figure 2.10 shows the critical thickness versus Ge content.

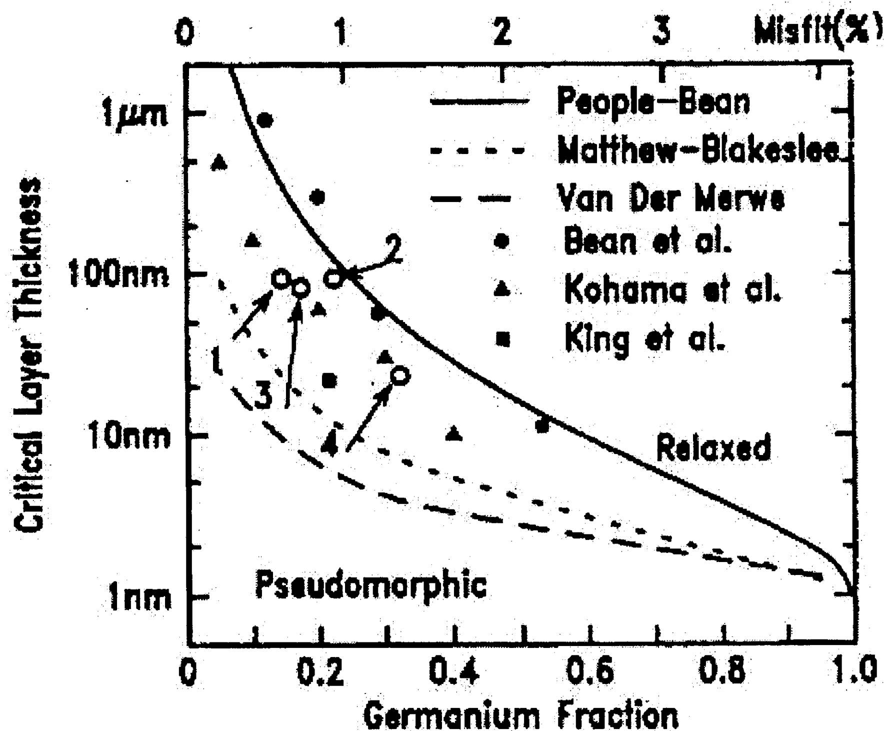


Figure 2.10 Critical thickness versus Ge content (after Iyer et al., Ref. 40).

The experimental observation of the onset of strain relaxation is limited by the experimental techniques used. Conventional x-ray diffraction and transmission electron

microscopy (TEM) can detect relaxation only when it exceeds 0.1%. Refinements of these techniques, such as triple-crystal x-ray diffraction, may be enable resolution of strain below 0.01%. Electron-induced-current (EBIC) can be used to image dislocations because of the increased carrier recombination in the vicinity of dislocation. Other electrical evaluation methods for the quality of heterojunction include measurement of the reverse leakage current across p-n junction, the ideality factor of the forward injection, and measurement of band discontinuities.

In the SiGe HBT, most of the bandgap reduction results from shift in valence-band edge. The conduction-band discontinuity is usually a small fraction of the total bandgap difference. The experimental data indicate that valence-band discontinuity between Si and $Si_{1-x}Ge_x$ can be approximated by ΔE_V=6.4x meV for 0<x<17.5%. The essential differences between the SiGe HBT and the Si Bipolar Transistor are best illustrated by considering a schematic energy band diagram. Observe in Figure 2.11 [41] that Ge-induced reduction in base bandgap that occurs at EB edge of the quasi-neutral base induces a quasi-drift field in the neutral base. Figure 2.12 shows a suitable layer configuration for a fully pseudomorphic Si/ $Si_{1-x}Ge_x$ pMOS [42].

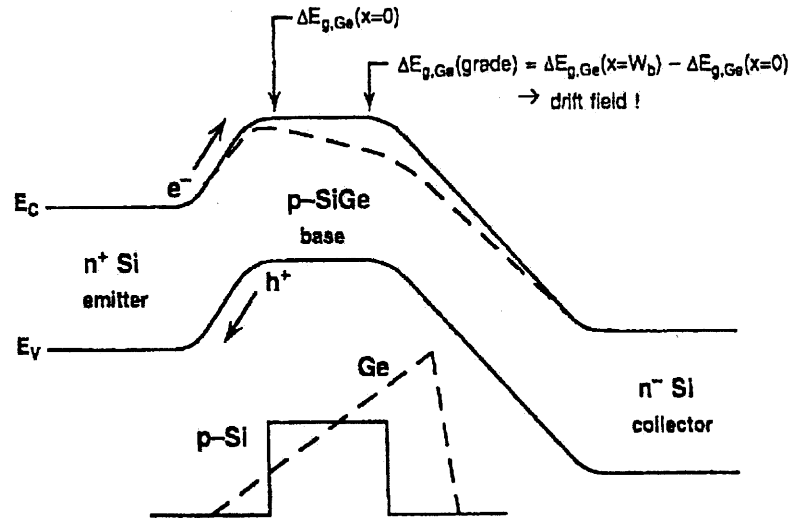


Figure 2.11 Energy band diagram of graded-base SiGe HBT compared to a Si BJT (after J. D. Cressler, Ref. 41).

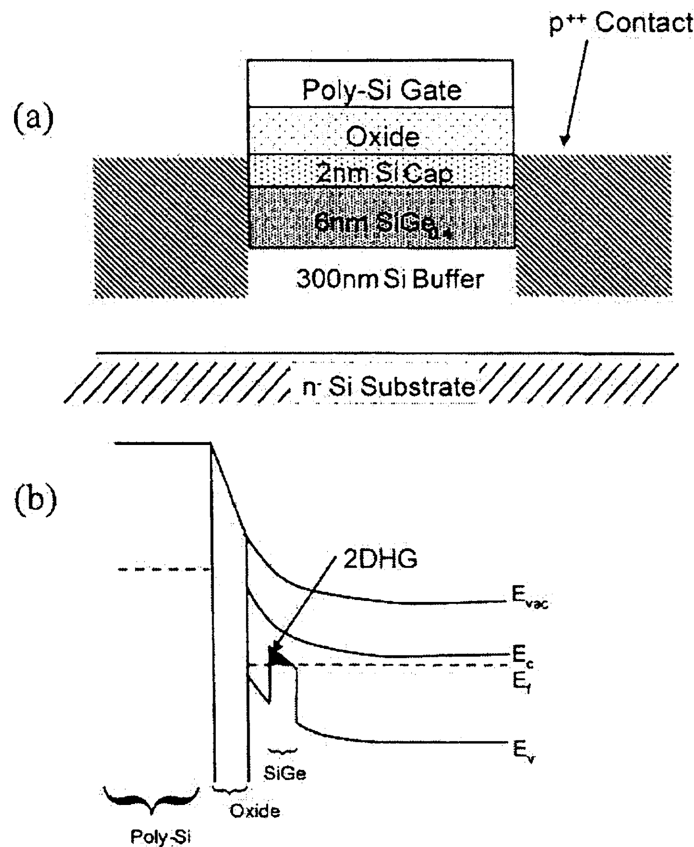


Figure 2.12 (a) A fully pseudomorphic pMOS layer configuration with typical design parameters. (b) The quantum well for holes and inversion of the n- SiGe layer under a sufficiently high negative gate voltage (after T. E. Whall, Ref. 42).

Because of the mismatch between the pseudomorphically grown SiGe layer and the underlying silicon substrate, strained SiGe alloy changes carrier mobility due to the strain-induced energy shifts and dislocation in the energy-band spectrum. The effective drift mobility of holes in a strained MOS gate SiGe/Si heterostructure inversion layer shows 50% enhancement in mobility over that of silicon at room temperature. Results calculated for the lattice drift mobility of strained SiGe also show increase in the mobility relative to that of silicon.

Vapor-phase epitaxy and molecular beam epitaxy technologies are capable of growing epitaxial layer with high crystalline perfection and purity. Highly controlled doping level up to 10^{19} cm^{-3} or more can be achieved, and highly controlled changes in the doping level are possible during growth with minor adjustment in growth parameters. With MOCVD, layer thickness below 5 nm has been achieved. With MBE, thickness below 1 nm has been reached.

2.4.2 Physical and Electrical Damage to Strained $Si_{1-x}Ge_x$ Devices

The fabrication of heterojunction structures often requires to make contact to a buried SiGe or Si layer, e.g. in Si/SiGe/Si heterostructures used to form Si-Based HBT where the base region consists of the SiGe alloy whereas the emitter and collector region are made of Si. Making contact to the SiGe base region requires etching Si and stopping on the SiGe base. In other application etching SiGe and stopping on a Si underlayer is required. The dry etching characteristics of strained SiGe in terms of etch rates, etch profiles and surface-chemical aspects have been studied [43, 44], but the research on plasma induced damage to the SiGe underlayer after etching the Si is very limited. In this

study, the electrical measurements I-V & C-V characteristics of wet etched, SF_6 plasma etched, un-etched and O_2 ashed samples of $Si_{1-x}Ge_x$ p^+-n heterojunction were presented. These electrical evaluation methods can serve as very sensitive qualitative measurements of heterojunction quality. In addition, the material characterizations of these samples by SIMS and TEM have been performed. It has been reported that plasma etching may create strain-relieving misfit dislocation and/or threading dislocation to strained SiGe material and can relax the strain of coherently strained SiGe after subsequent annealing [23, 45]. This thesis explores this area further, using the device simulation to verify these findings and show the limitation of C-V profiling as a detection method.

CHARPTER 3

EXPERIMENTAL TECHNIQUES

3.1 Electrical Characterization

3.1.1 I-V & C-V Measurements to Evaluate MOS System

There are several different ways of investigating semiconductor surfaces and oxide-semiconductor interfaces. The MOS capacitor is the most powerful for investigating nearly all the electrical properties of the MOS system [46]. The superiority of the MOS capacitor rests on its simplicity of analysis results because thermal equilibrium conditions are obtained and because a one-dimensional treatment is accurate. Using the MOS capacitor, nearly all of the properties of interest in the SiO_2, at the Si-SiO_2 interface, and in the silicon can be measured. The MOS capacitor is simpler to use for these studies than actual devices used in integrated circuits. Any change in process that improves the electrical properties of the MOS capacitor makes the same improvement on the actual device.

Using MOS capacitor for measuring properties of the MOS system, the following properties can be obtained:

1 Doping profile in the silicon

2 Conductivity type of the silicon

3 Dielectric constant of SiO_2

4 Work function differences between silicon and gate

5 Oxide breakdown field

6 Interface trap level density (Q_{it}) as a function of the energy in the bandgap

7 Charge configurations in the oxide such as oxide fixed charge (Q_f) and the charge at the interface between SiO_2 and another insulator deposited on top of it.

8 Mobile ionic charge Q_m and oxide-trapped charge Q_{ot} in SiO_2

9 Interface trap capture probability for both electrons and holes as a function of energy in the bandgap

10 Surface recombination velocity

I-V Measurement

Ramped voltage breakdown (RVBD) and time dependent breakdown (TDBD) are the most important gate oxide integrity (GOI) tests. A good number is a breakdown field of 12 MV/cm or more. The I-V characteristics of Schottky barriers (leakage) are sensitive to lifetime and interface states i.e. sensitive to surface damage. The I-V test is not as straightforward in interpretation as GOI and C-V but is a "best" electrical method for detecting lattice damage.

C-V Measurement

C-V tests are necessary to determine mobile and trap concentrations. The MOS capacitor is at thermal equilibrium at all values of gate bias below the oxide breakdown field. That is, no dc current flows when gate bias is applied. Thus the Fermi level in the silicon always is flat all the way to the Si-SiO_2 interface as shown Figure 3.1. Energy values E_c and E_v are the conduction and valence band edges, respectively; E_i is the intrinsic Fermi level; E_{FS} is the Fermi level in the silicon; E_{FM} is the Fermi level in the metal; and W is depletion layer width. At low frequencies the MOS capacitor also is in

thermal equilibrium under small-signal excitation, provided that minority carriers can respond to variation in the ac field.

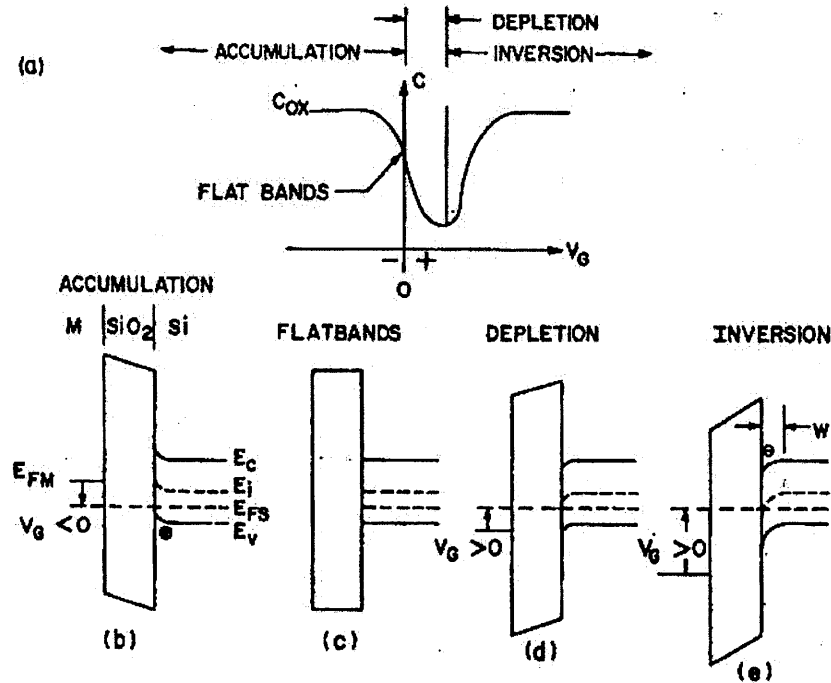


Figure 3.1 To illustrate the operation of an MOS capacitor, capacitance as a function of bias, and the corresponding energy-band diagrams are shown in accumulation, depletion, inversion, and at flatbands (after E. H. Nicollian and J. R. Brews, Ref. 46, p. 82).

Minority carriers follow an applied gate voltage as long as the period of the applied ac voltage is much longer than the minority carrier response time τ_R. Response time for minority carriers in silicon at room temperature is typical 0.01-1sec in strong inversion. Because this response time is very long, inversion layer capacitance will be frequency dependent, except at very low frequencies. This frequency dependence is illustrated in Figure 3.2 which shows capacitance measured as function of gate bias at 27°C with frequency of the ac gate voltage as parameter. At high frequencies, where $\omega^{-1} >> \tau_R$, minority carries do not follow the ac gate voltage but do follow gate bias changes. The low and high frequency C-V curves are practically identical in accumulation,

depletion, and most of weak inversion because in these regions, minority carrier concentration in the depletion layer is negligibly small compared to majority carrier concentrate. Therefore, it does not matter whether minority carriers respond to the ac voltage. The major difference between low and high frequency C-V curves occurs in weak to strong inversion where minority carrier concentration in the depletion layer becomes comparable to and exceeds majority carrier concentration. Minority carrier effects cannot be neglected in these regions.

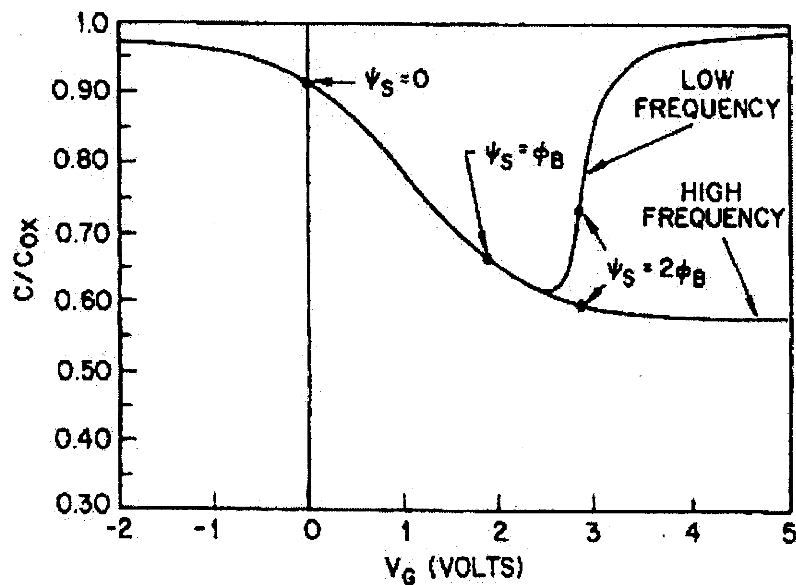
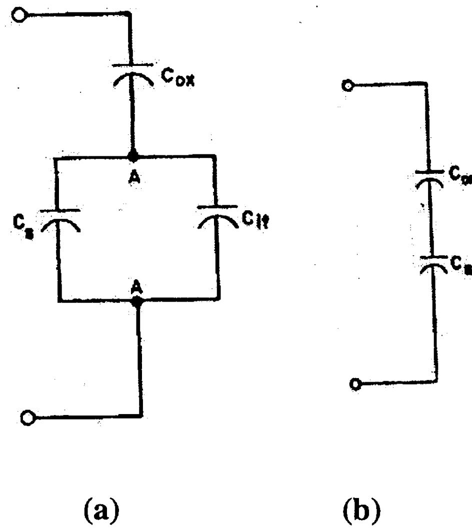


Figure 3.2 Normalized high frequency and low frequency capacitance as a function of gate bias calculated for and acceptor concentration of 2×10^{16} cm^{-3}, oxide thickness 100 nm, and T=300 K (after E. H. Nicollian and J. R. Brews, Ref. 46, p. 156).



(a) (b)

Figure 3.3 (a) Low frequency equivalent circuit of MOS, (b) high frequency equivalent circuit of MOS.

Castange and Vapaille [47] were the first to combine high and low frequency C-V curves to obtain a measured *Cs*. The step eliminates the need for a theoretical computation of C_s and for measurement of the doping profile of the device. From figure 3.3 it can yield

$$C_{LF} = (C_s + C_{it})\frac{C_{ox}}{C_{ox} + C_s + C_{it}} \tag{3.1}$$

$$C_{HF} = \frac{C_{ox} C_s}{C_s + C_{ox}} \tag{3.2}$$

Therefore

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \tag{3.3}$$

where C_{ox} is the oxide capacitor per unit area, C_s is the silicon surface capacitor per unit area and C_{it} is interface trap capacitor per unit area. In this way C_{it} is obtained directly from the measured C-V curves, without the uncertainty introduced by a theoretical C_s and without uncertainty as to whether C_s has been calculated for the correct band bending.

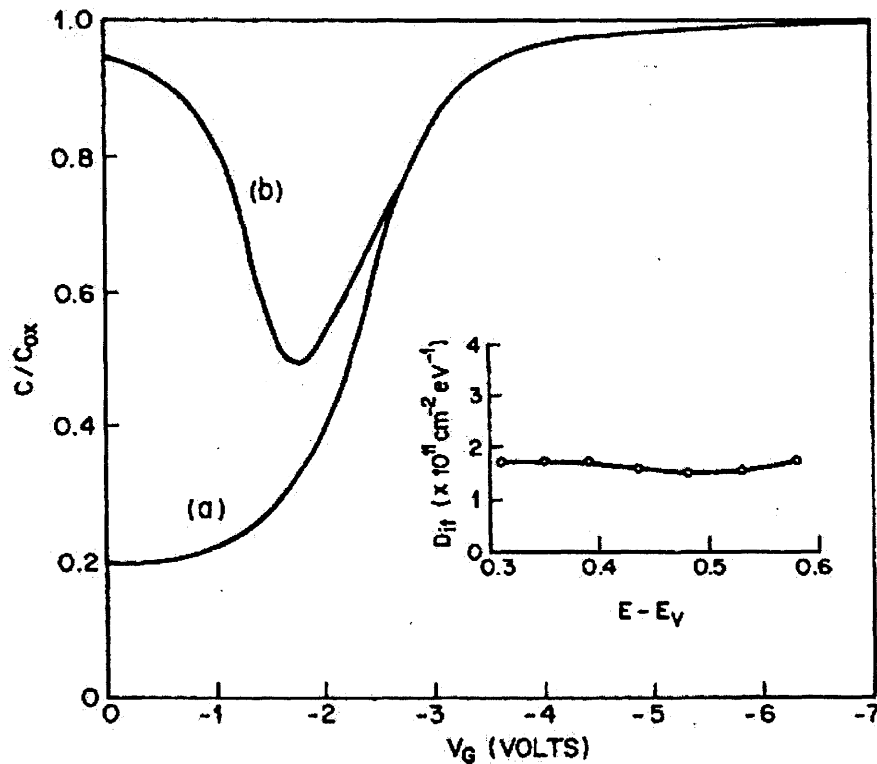


Figure 3.4 Combined (a) high frequency (1MHz) and (b) low frequency C-V curves for a MOS capacitor (after E. H. Nicollian and J. R. Brews, Ref. 46, p. 331).

In this thesis, MOS capacitors using Si as well as SiGe were fabricated for studying the plasma induced damage to Si/SiO_2 interface in Si and misfit dislocations strained SiGe material. The high frequency and quasi-static C-V measurements were performed. The plasma induced damages and the interface state densities were derived from C-V measurement results.

3.2 Deep Level Transient Spectroscopy (DLTS) Techniques

Luminescence has been widely used with great success in the study of shallow centers. But it misses the deeper non-radiative centers. The deep-level transient spectroscopy (DLTS) is a high-frequency capacitance transient thermal scanning method useful for observing a wide variety of traps in semiconductors. It is sensitive, rapid, and easy to analyze [48]. The DLTS measurement system consists of a sensitive capacitance measurement apparatus with good transient response, one or two pulse generators to make rapid changes in the diode bias, a dual-gated signal integrator, and x-y recorder, and a variable temperature cryostat. The presence of each trap is indicated by a positive or negative peak on a flat baseline plotted as a function of temperature. The heights of these peaks are proportional to their respective trap concentrations. The sign of each peak indicates whether it is due to a majority- or minority-carrier trap, and the positions of the peaks are simply and uniquely determined by the integrator gate setting and the thermal emission properties of the respective traps. By the proper choice of the experimental parameters it is possible to measure the thermal emission rate, activation energy, concentration profile, and capture rate of each trap.

For simplicity, only the situation in *p*-type material and in an asymmetric n^+-p diode will be described here. In the quiescent state of the system the diode is reverse biased and observable traps are within the depletion region. Thus the capture rates are zero and the occupation of the level is determined by the thermal emission rates e_1 and e_2 of minority and majority carriers respectively. The steady electron occupation of a level is

$$\overline{n_1} = [e_1 /(e_1 + e_2)]N \tag{3.4}$$

where N is the concentration of the trap. The capture and thermal emission rates for minority carriers (electrons in this example) are c_1 and e_1 respectively. The capture and thermal emission rates for majority carriers (holes in this example) are c_2 and e_2 respectively. An electron trap has to have $e_1 >> e_2$ and a hole trap $e_2 >> e_1$. The emission rates are proportional to a Boltzman factor and thus depend exponentially on the energy difference between the trap level and the conduction band (electron emission) and the trap level and the valence band (hole emission). Because of this, electron traps tend to be in the upper half of the gap and the hole traps in the lower half.

There are two main types of bias pulses (see Figure 3.5), namely, an injection pulse which momentarily drives the diode into forward bias and injects minority carriers into the region of observation shown in Figure 3.6, and a majority-carrier pulse which momentarily reduces the diode bias and introduces only majority carriers into the region of observation shown in Figure 3.7.

The steady-state electron occupation during a bias pulse is

$$\overline{n_1} = [c_1 /(c_1 + c_2)]N \tag{3.5}$$

where c_1 is the minority-carrier (electron) capture rate proportional to the concentration of injected minority carriers and c_2 is the majority-carrier (hole) recombination rate proportional to the majority-carrier concentration. In all the situations considered, the capture rates are much larger than the emission rates, which can be neglected during the

bias pulse. An injection pulse which introduces a large enough number of electrons so as to make $c_1 >> c_2$ and overwhelm the trap emptying process will completely fill the trap with electrons; such a pulse is called a saturation injection pulse. A majority-carrier pulse, on the other hand, introduces only holes, and thus tends to empty all traps of electrons, i.e., fill them with holes.

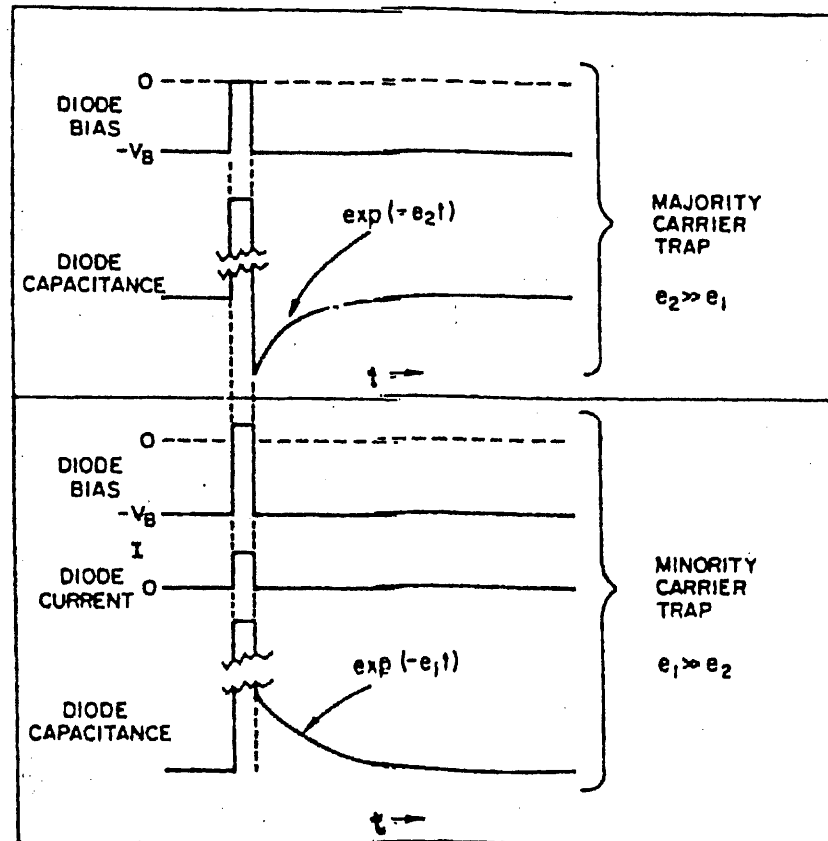


Figure 3.5 Typical time dependence involved in pulsed bias capacitance transients for majority- and minority carrier traps. The upper half is a majority-carrier pulse sequence while the lower half is an injection-pulse sequence (after D. V. Lang, Ref. 48).

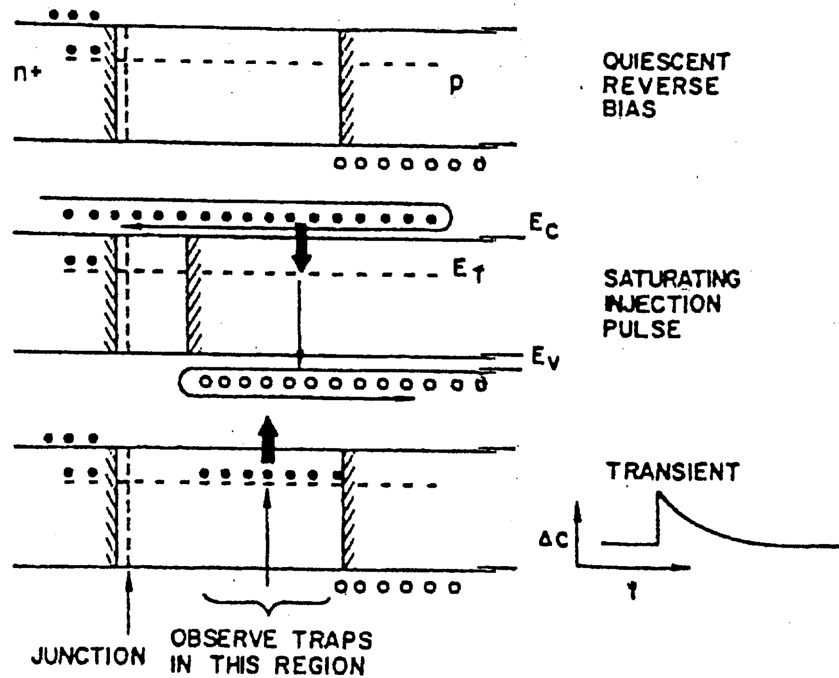


Figure 3.6 Injection pulse sequence which is used to produce a capacitance transient for a minority-carrier trap (after D. V. Lang, Ref. 48).

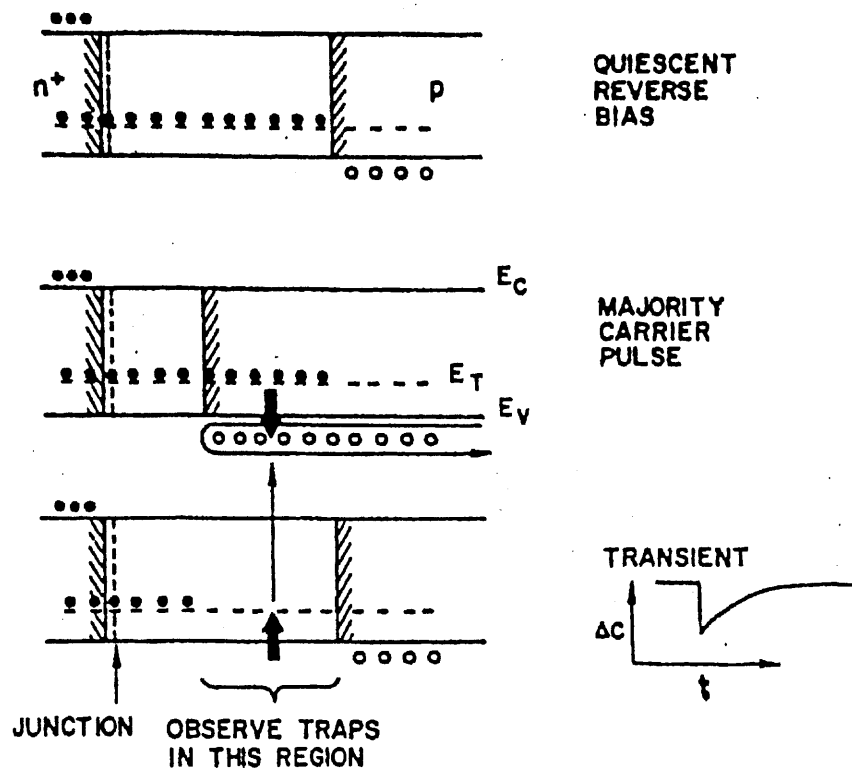


Figure 3.7 Majority-carrier pulse sequence which is used to produce a capacitance transient for a majority-carrier traps (after D. V. Lang, Ref. 48).

The concentration of a trap can be obtained directly from the capacitance change corresponding to completely filling the trap with a saturating injection pulse (in the case of minority-carrier trap) or the largest possible majority-carrier pulse (in the case of a majority-carrier trap). The relationship for an electron trap in a n^+-p step junction is simply

$$N = 2(\Delta C / C)(N_A - N_D) \tag{3.6}$$

where N is the trap concentration, ΔC is the capacitance change at $t=0$ due to a saturating injection pulse, C is the capacitance of the diode under quiescent reverse-biased condition, and N_A-N_D is the net acceptor concentration on the p side of the junction where the trap is observed.

The essential feature of DLTS is the ability to set an emission rate window such that the measurement apparatus only responds when it sees a transient with a rate within this window. Thus if the emission rate of a trap is varied by varying the sample temperatures, the instrument will show a response peak at the temperature where the trap emission rate is within the window. The emission rates are thermally activated and by the principle of detailed balance can be given as

$$e_1 = (\sigma_1 \langle v_1 \rangle N_{D1} / g_1) \exp(-\Delta E / kT) \tag{3.7}$$

where σ_l is the minority-carrier cross section, $<v_l>$ is the mean thermal velocity of minority carriers, N_{Dl} is the effective density of states in the minority-carrier band, g_l is

the degeneracy of the trap level, and ΔE is the energy separation between the trap level and the minority-carrier band. An exactly similar equation holds for e_2 with subscripts changed from 1 to 2 and with all quantities referring to majority carriers. A standard means of characterizing the depth of a trap is to construct a plot of $\log e_1$ or $\log e_2$ vs. $1000/T$ and to report the slope of the resulting straight line as the activation energy of the trap.

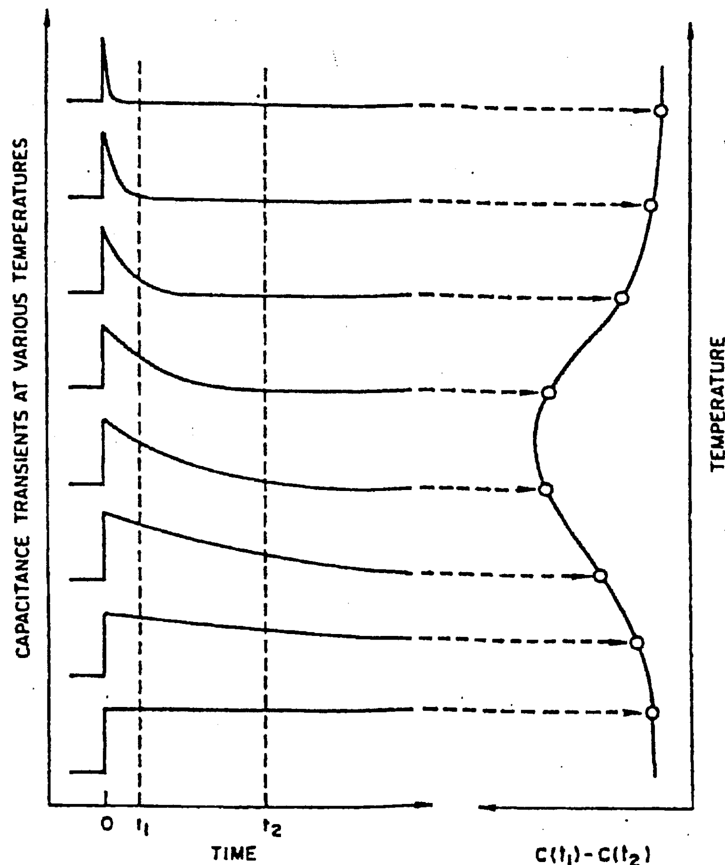


Figure 3.8 Illustration of how a double boxcar is used to define the rate window. The left-hand side shows capacitance transient at various temperatures, while the right-hand side shows the corresponding DLTS signal resulting from using the double boxcar to display the difference between the capacitance at time t_1 and the capacitance at time t_2 as a function of temperature (after D. V. Lang, Ref. 48).

The emission rate corresponding to the maximum of a trap peak observed in a DLTS thermal scan is

$$\tau_{max} = (t_1 - t_2)[\ln(t_1 / t_2)]^{-1} \tag{3.8}$$

This can generate one point of $\log e_1$- or $\log e_2$- vs $-1000/T$ plot. Other points can simply be obtained from other scans made with different gate settings and thus different values of τ_{max} and different trap peak positions.

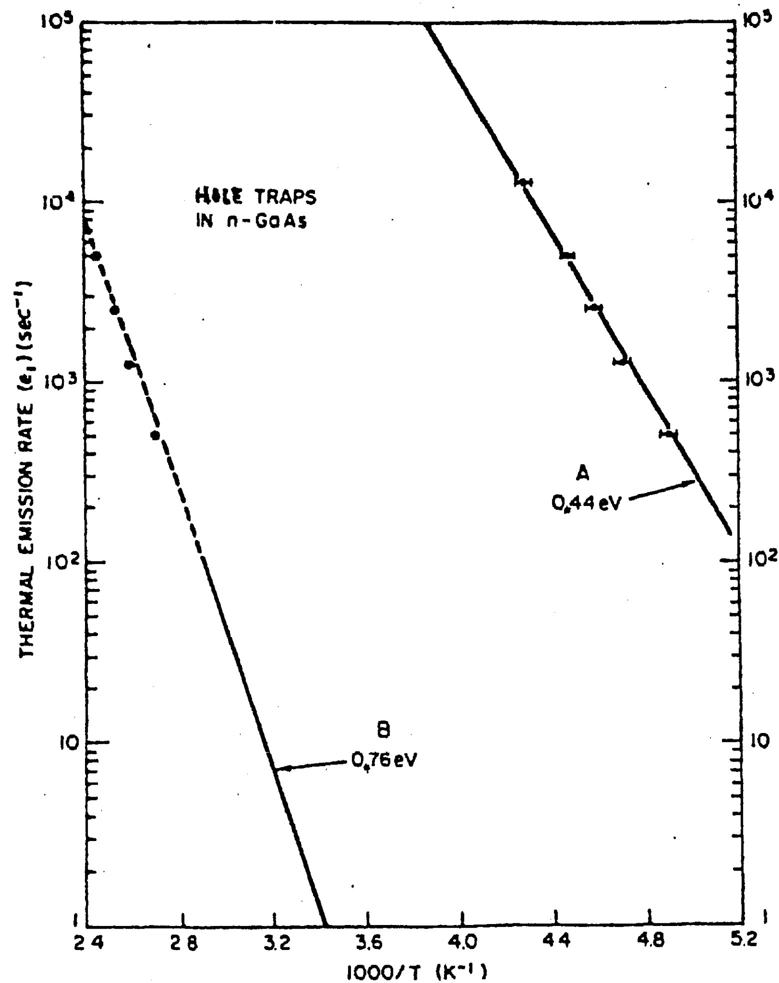


Figure 3.9 Thermal emission rates vs *1000/T* determined from the DLTS spectra (after D. V. Lang, Ref. 48).

The DLTS technique has been used in this research for Si MOS capacitor and SiGe/Si p^+-n diode. It provides the information about process induced electrical defects at the silicon and silicon dioxide interface and detects any process induced defects and misfit dislocations at the Si/SiGe interface. The equations described here have been applied to calculate the trap concentrations and the energy level of these traps.

3.3 Physical Characterization

3.3.1 Secondary Ion Mass Spectroscopy (SIMS)

In the SIMS method, an ion beam sputters material off the surface of a sample, and the ionic component is mass analyzed and detected (Figure 3.10). Sputtered ions are extracted and mass analyzed with a magnetic prism or quadrupole analyzer. In a system that uses a magnetic prism, a two-dimensional image of the distribution of an ionic species across the surface can be obtained by directing the secondary ion beam onto a channel plate. In quadrupole instruments the image is formed by recording the changing secondary ion-beam current as primary beam is rastered across the sample surface. The intensity of the detected signal is related to the mass concentration. The mass spectrum can be displayed as a function of time, giving a depth profile of the chemical species.

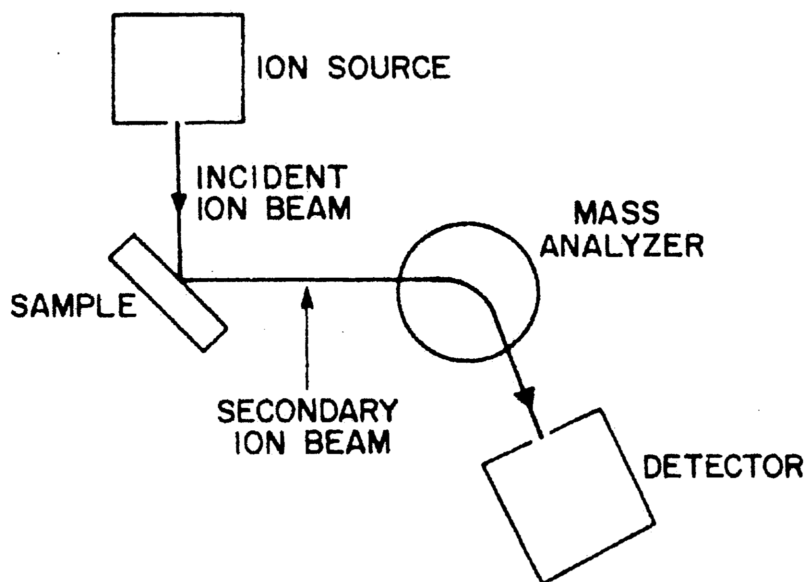


Figure 3.10 Schematic diagram of a secondary ion mass spectrometer. (After S. M. Sze. Ref . 24, p. 527).

Both positive and negative incident ions are used with a beam energy typically between 5 and 15 keV. Since only the ionic fraction of sputtered material produces a SIMS signal, ion beams are chosen that produce the highest ion yields of the species under study. Positive cesium ion beams are generally useful for producing high negative ion yields of electronegative species from a target, and O2+ ion beams are usually used for generating high positive ion yields from electropositive species.

The incident beam is rastered across a small area of the surface to create a crater with a nearly flat bottom. Mass analysis is performed on the ionic fraction of sputtered material only from a central portion of crater. When very low primary ion currents are used, sputtering rate are lowered to the point where data can be collected from a few monolayers, and surface analysis can be performed. Depth profiles are obtained by using higher primary ion currents. Lateral spatial resolution depends on the type of ion optics used in the instrument. Increased resolution must be traded off with sensitivity. SIMS achieves lateral resolution of about 0.5 μm which is useful for the analysis of some patterned VLSI chips. Vertical (depth) resolution is controlled by many factors, such as texture at the bottom of a crater, the contribution of signals from the crater wall, and impurity redistribution during ion milling.

3.3.2 X-Ray Photoelectron Spectroscopy (XPS)

X-ray bombardment of a sample can stimulate the emission of core-level electrons if the incident x-ray energy is sufficiently high. Letting E_o be the energy of the incident x-radiation, E_b the binding energy of the emitted electrons, $\Delta\phi$ the work function difference

between the samples and spectrometer surface, and E_{xp} the energy of the emitted electron (photoelectron kinetic energy),

With constant $\Delta\phi$ and E_o in a given experiment, electrons of different binding energies give rise to separate peaks in the photoelectron spectrum. The application of this phenomenon to chemical analysis of the bombard surface is called x-ray photoelectron spectroscopy (XPS); this procedure is also called electron spectroscopy for chemical analysis (ESCA).

The incident x-ray beam is usually generated by low-energy electron bombardment of an aluminum or magnesium anode. K_α radiation from magnesium has an energy of 1253.9 eV and a linewidth of 0.7 eV, and K_α radiation from aluminum has an energy of 1487.0 eV and linewidth of 0.85 eV. Since $\Delta\phi$ is about 1 eV, photoelectron energies from aluminum or magnesium sources are sufficiently low so that escape depth are less than 50A. XPS therefore provides chemical information from a region within a few monolayers of the surface.

XPS is often used as a complement or back-up to AES, because of the following three advantages. First, radiation sensitive material can be nondestructively studied, because the scattering cross section for x-ray induced desorption and dissociation are significantly lower than the corresponding cross sections for electron bombardment. Second, insulators can be studied with less surface charging, since a neutral incident beam is used. The energy levels of core electrons are affected by valence state and type of chemical bonding. The energy resolution of XPS peaks is typically about 0.5 eV, and since different chemical bonds often produce shifts in the binding energy by larger amounts, these shift can be detested and bond identified [49].

3.3.3 Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM) is a useful tool for solving problems in VLSI technology that require high spatial resolution. TEM offers a resolution of about 2A. In a transmission electron microscope an electron beam passes through the thin-film sample, and forms an image that displays morphological and crystallographic features of the film components. Commercial TEM instruments use electron beams with energy between 60 and 350 keV. Higher beam energy permits greater sample penetration; the maximum thickness of silicon which permits TEM image formation is 1.5 μm for 200 keV beam, but only 0.5 μm for an 80 keV beam.

Contrast in a TEM image can be described for two situations. One is TEM study of crystalline materials (such as silicon, aluminum, polysilicon, and various silicides), and the other is the study of amorphous materials. In crystalline materials, the incident electron beam is diffracted by the material and local variations in diffraction intensity produce contrast in an image from the undiffracted beam (bright field image) or from one or more diffracted beam (dark field image). The intensity of the emergent beam is periodic with sample thickness. The sample thickness corresponding to one period or more in silicon is 60.2 nm for a (111) reflection and 75.7 nm for a (220) reflection [50]. Thus, a thicker region of the sample does not necessarily look lighter in the negative; wedge-shaped crystalline sample produces a TEM image that has alternate light and dark bands called thickness extinction contours. Dark bands are also caused by a bent sample and are then called bend extinction contours. Abrupt changes in thickness, phase structure, or crystallographic orientation cause corresponding abrupt changes in contrast, and these crystallographic features can be easily imaged at high resolution.

In the case of nearly amorphous material, contrast is determined by local changes in electron scattering which result from differences in sample thickness or from differences in chemical or phase composition. A sample region whose thickness varies continuously produces a corresponding continuous variation in image intensity, unlike the case of diffraction contrast. TEM images obtained from oxides, nitrides, and other amorphous materials are therefore somewhat easier to interpret intuitively than images obtained from crystalline samples.

3.4 Simulation of $Si_{1-x}Ge_x$ Device for Damage Estimation

3.4.1 Overview of Device Simulator

Atlas is a physical-based device simulator. Physical-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto two or three-dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, onto this grid it is possible to simulate the transport of carriers through a structure. This means that the electrical performance of a device can be modeled in DC, AC or transient modes of operation.

Physical-based simulation provides three major advantages: it is predictive, it provides insight, and it captures theoretical knowledge in a way that makes this knowledge available to non-experts. Physical-based simulation is different from empirical modeling. The goal of empirical modeling is to obtain analytic formulae that approximate existing data with good accuracy and minimum complexity. Empirical models provide efficient approximation and interpolation. They do not provide insight, or predictive capabilities, or encapsulation of theoretical knowledge. Physical-based simulation is an alternative to experiments as a source of data.

Physical-based simulation has become very important for two reasons. First, it is almost always much quicker and cheaper than performing experiments. Second, it provides information that is difficult or impossible to measure. The drawbacks of simulation are that all the relevant physics must be incorporated into a simulator, and numerical procedures must be implemented to solve the associated equations.

The steps of using the physical-based simulation include defining the physical structure, defining the physical models to be used and defining the bias conditions for which electrical characteristics are to be simulated.

3.4.2 Important Physics and Equations in SiGe MOS Simulation

Many years of research into device physics has resulted in a mathematical model of the operation of any semiconductor device. This model consists of a set of fundamental equations which link together the electrostatic potential and the carrier densities, within some simulation domain. These equations, which are solved inside any general purpose device simulator, have been derived from Maxwell's laws and consist of Poisson's equation, the continuity equations and the transport equations. Poisson's equation relates variations in electrostatic potential to local charge densities. The continuity equations describe the way that the electron and hole densities evolve as a result of transport processes, generation processes, and recombination processes.

Traps and Defects

Semiconductor materials exhibit crystal flaws which can be caused by dangling bonds at interface or by the presence of impurities in the substrate. The presence of these defect centers, or traps, in semiconductor substrates may significantly influence the electrical characteristics of the device. Trap centers, whose associated energy lies in a forbidden gap, exchange charge with the conduction and valence bands through the emission and recombination of electrons. The trap centers change the density of space charge in semiconductor bulk and influence the recombination statistics.

Device physics has established the existence of three different mechanisms which add to the space charge term in Poisson's equation, in addition to the ionized donor and acceptor impurities. These are interface trapped charges, interface trap states and bulk trap states. Interface trapped charge is modeled as a sheet of charge at the interface and therefore is controlled by the interface boundary condition. Interface traps and bulk traps will add space charge directly into the right hand side of Poisson's equation.

Two basic types of trap have been found to exist; donor-like (electron traps) and acceptor-like traps (hole traps). A donor-like trap, similar to ionized donor impurities N_D^+, is positively charge and therefore can only capture an electron. This means that donor-like traps are *positive* when *empty* of an electron but are *neutral* when *filled.* An acceptor-like trap, similar to ionized acceptor impurities N_A^-, is *negative* when *filled* but are *neutral* when *empty.* In a semiconductor there is a position of the Fermi level corresponding to neutrality. At this condition, those traps above the Fermi level are defined as acceptor-like and those below the Femi level are donor-like. The position of the trap is defined relative to the conduction or valence bands using *E.LEVEL* in ATLAS.

Poisson's Equation

Poisson's equation including the carrier concentrations, the ionized donor and acceptor impurity concentrations N_D^+ and N_A^-, charge due to traps and defects, Q_T has the form:

$$Div(\varepsilon \nabla \psi) = q(n-p-N_D^+ + N_A^-) + Q_T \qquad (3.9)$$

$$Q_T = q\,(p_t - n_t) \qquad (3.10)$$

where n_t and p_t are the density of trapped charge for donor-like and acceptor traps respectively. The trapped charge depends upon the trap DENSITY and its probability of occupation, $F_{n,p}$. for donor-like and acceptor-like, respectively, the trapped charge is calculated by the equations:

$$n_t = DENSITY \times F_n \tag{3.11}$$

$$p_t = DENSITY \times F_p \tag{3.12}$$

$$F_n = \frac{v_n SIGNn + e_p}{v_n(SIGNn + SIGPp) + (e_n + e_p)} \tag{3.13}$$

$$F_p = \frac{v_p SIGNn + e_n}{v_p(SIGNn + SIGPp) + (e_n + e_p)} \tag{3.14}$$

where SIGN and SIGP are the carrier capture cross section for electrons and holes respectively, v_n and v_p are the thermal velocities for electrons and holes and the electron and hole emission rates, e_n and e_p are defined by:

$$e_n = DEGEN.FACv_n SIGNn_i \exp\frac{E.LEVEL - E_i}{kT_L} \tag{3.15}$$

$$e_n = \frac{1}{DEGEN.FAC} v_p SIGN n_i \exp \frac{E_i - E.LEVEL}{kT_L} \quad (3.16)$$

where E_i is the intrinsic Fermi level position, E.LEVEL is the energy level in the bandgap of each discrete trap center and DEGEN.FAC is the degeneracy factor of the trap center. The latter term takes into account that spin degeneracy will exist, that is the "empty" and "full" conditions of a flaw will normally have different spin and orbital degeneracy choices.

The electric field is obtained from the gradient of the potential.

$$\vec{E} = \nabla\psi \quad (3.17)$$

3.4.3 Simulation of $Si_{1-x}Ge_x$ MOS Capacitor Using Silvaco Device Simulator

Firstly, use Silvaco's DevEdit to create the 2D MOS device structures (as shown is Figure 3.11), generate the mesh (Figure 3.12) and save it as a structure file. This structure file, which contains device dimension and defined material, will be loaded into Atlas for simulation. The structure used in simulation is similar to that of a conventional MOS capacitor, except for the present of the $Si_{1-x}Ge_x$ channel, separated from the Si/SiO_2 interface by a Si cap layer.

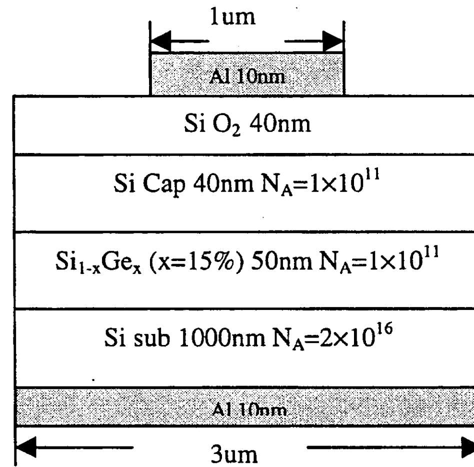


Figure 3.11 SiGe MOS capacitor structure used for simulation.

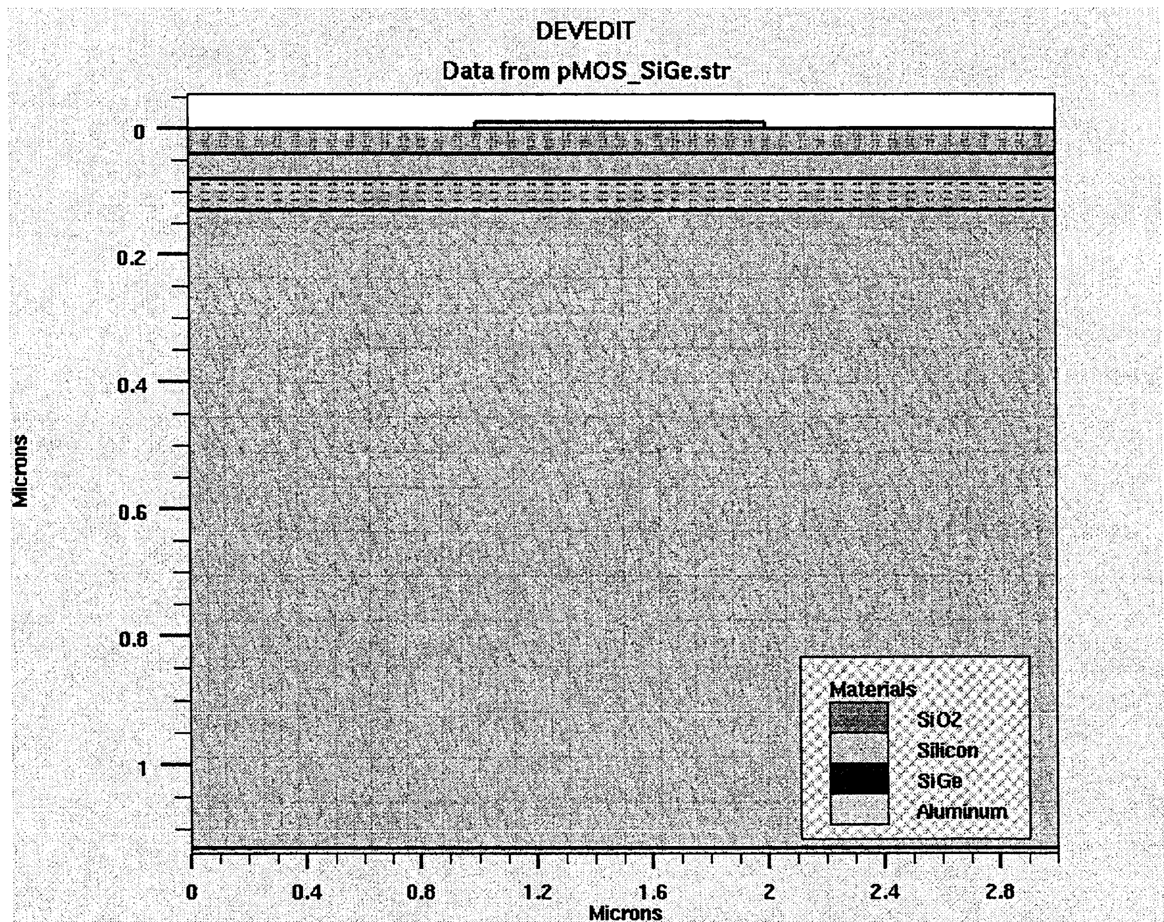


Figure 3.12 Simulated device structure with mesh.

Secondly, use Silvaco's Deckbuilder to create an Atlas input file. There are five groups of statement in this file, and these must occur in the correct order. These groups are indicated in Figure 3.13. The input file for this example is shown in Appendix.

Group	*Statement*
1. Structure Specification	Mesh Region Electrode Doping
2. Material Models Specification	Material Models Contact Interface
3. Numerical Method Select	Method
4. Solution Specification	Log Solve Load Save
5. Results Analysis	Extract Tonyplot

Figure 3.13 Atlas command group with primary statements in each group [Ref. 51].

Finally, run the simulation and use the Tonyplot to interpret the results. Figure 3.14 shows the simulated C-V plot. Figure 3.15 shows the energy diagram cross the MOS capacitor.

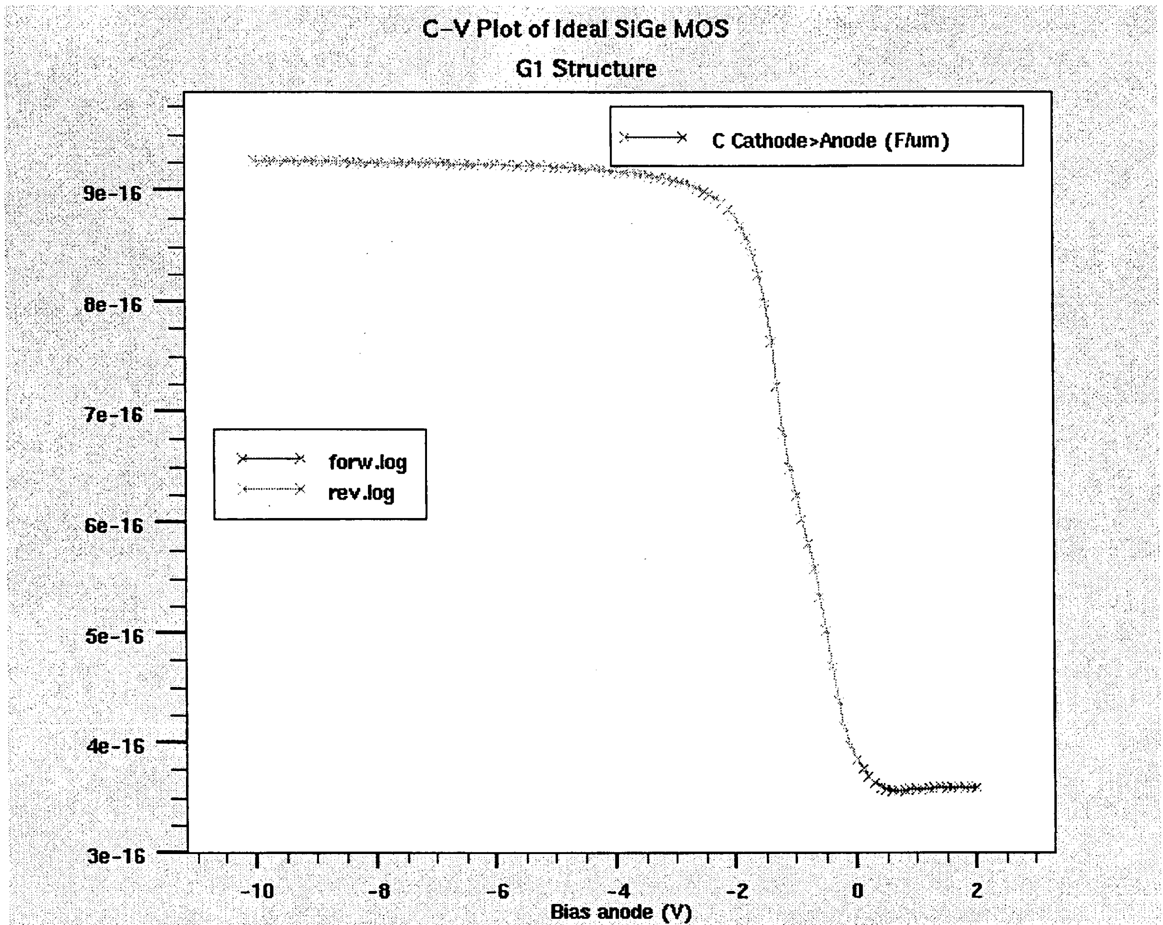


Figure 3.14 Use Tonyplot to display the C-V plot.

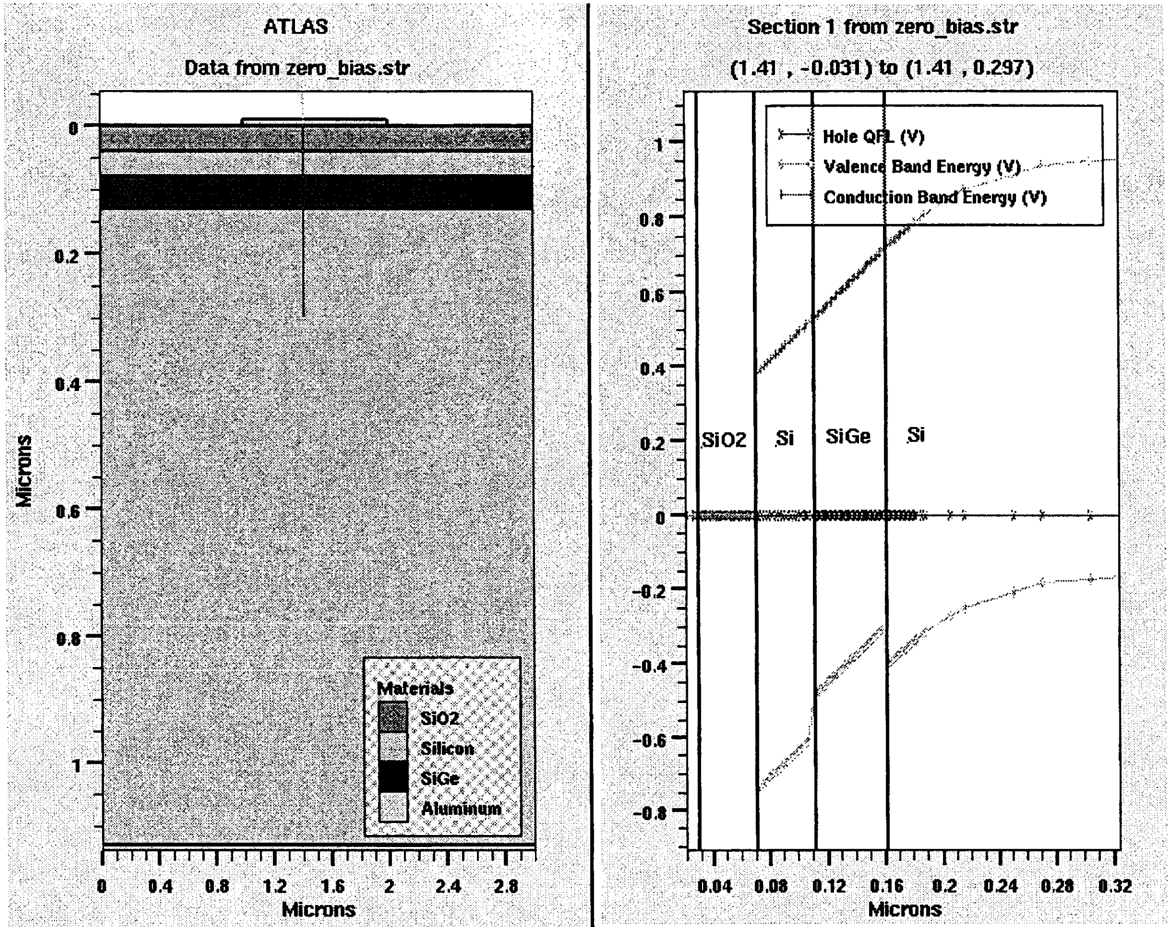


Figure 3.15 Use Tonyplot to display the energy diagram cross the MOS capacitor under certain bias condition.

CHARPTER 4

ETCH-INDUCED DAMAGE TO MOS DEVICE IN HIGH-DENSITY ICP ETCHING REACTOR

4.1 Introduction

Inductively coupled plasma (ICP) sources are able to operate at lower pressures (1-20 mTorr) and can produce plasma densities in the 1×10^{11} - 1×10^{12} ions cm^{-3} range [52, 53]. They are capable of uniform etching of anisotropic features over large area wafers at etch rates comparable to conventional high-pressure capacitively coupled reactive ion etching (RIE) tools. The ion energies incident on the wafers can be effectively decoupled from plasma generation by independently applying RF power to the wafer chuck. However, a fundamental understanding of the etch induced damage to thin gate oxide in these types of etching source is required to enable their widespread acceptance by integrated circuit manufactures.

Plasma etching can cause oxide charging where charges are trapped in the oxide and surface state are created at the Si-SiO_2 interface, thereby deforming the C-V characteristics of the gate oxide. However, the physical nature of those charge traps is not well understood. By identifying the type of defect created in the oxide by the etching process, one can more easily investigate ways to make gate oxides more resistant to such damage. This research correlates plasma induced electrical damage to thin gate oxide with that of the physical damage during polysilicon etching in an ICP etcher leading to the development of a basic understanding of damage. The electrical measurements were carried out using high frequency, quasi-static C-V and DLTS measurements (see Chapter 3 for more details) whereas physical damage was investigated using x-ray photoelectron spectroscopy.

4.2 Experimental Details

Figure 4.1 shows the high-density ICP reactor configuration used in this work. A patented RF coil used in this source has flat and solenoidal excitation section and produces remarkably uniform plasma with uniformity better than ±5% over 200 mm. Due to unique coil geometry, this source appears to have a greater B field or inductive coupling and lower E field or capacitive coupling than conventional flat (pancake type) sources. The RF coil design contributed to the uniformity due to higher degree of inductive coupling over a large power and pressure range. The uniformity was measured using a Langmuir probe.

In this reactor the gap between the ICP and RF electrodes was 4 in (10.16 cm) and ICP coil was water-cooled. Under the condition used for etching in this reactor, the phase difference between the inductive source and RF source has minimal effect. The change in induced bias on the RF electrode was less than 2% when the phase was varied between 0 and 360°. The etch selectivity of polysilicon on oxide in this reactor with the etching condition (power, pressure, gas and distance) is in the range of 15:1 to 20:1.

Wafers with 500 nm thick n-doped polysilicon on 15nm thick oxide were etched in this reactor at various wafer biasing conditions (as listed in table 4.1) in SF_6/O_2 plasma.

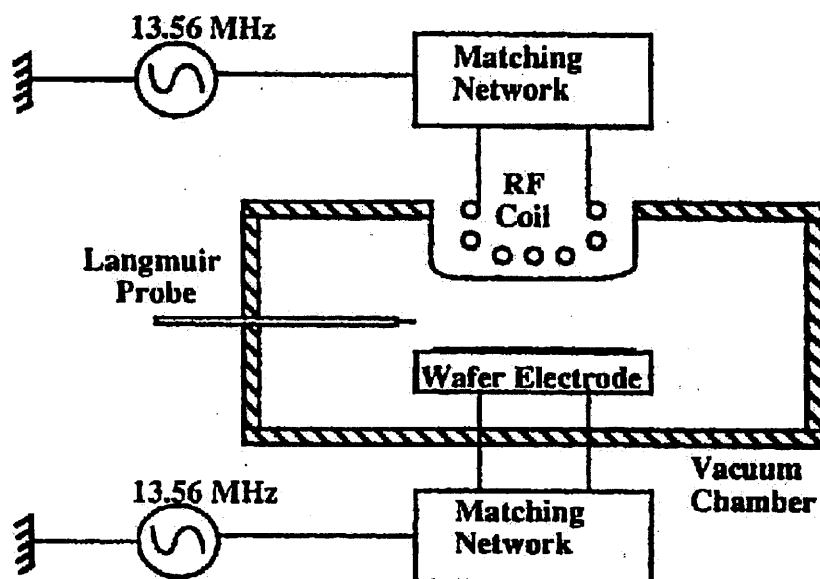


Figure 4.1 A schematic diagram of the ICP reactor.

Table 4.1 A list of the various processing conditions.

	Sample #2	Sample #3	Sample #4	Sample #5
ICP power (W)	800	800	800	800
Wafer bias power (W)	0	10	15	35
Induced bias (V)	+16	-70	-132	-203
Gas flow: SF_6 (sccm)	30	30	30	30
O_2 (sccm)	7	7	7	7
Poly-Si etch rate (nm min^{-1})	425	450	470	480

At low pressure (1-5 mTorr) the electronegativity of SF_6 is not a problem for polysilicon etching. The wafer electrode was floating when ICP power was activated alone. The dc bias was +16 V for this condition (sample#2) whereas when the wafer electrode was powered the dc bias was negative (Table 4.1). The induced dc bias was measured with a RF choke, a capacitor filter and a resistive voltage divider. The +16 V

on the floating electrode (dc or time averaged floating potential) is with respect to earth and not with respect to the plasma potential. It is expected that the plasma potential is more positive with respect to this floating potential. When the wafer electrode is not powered (the substrate is at floating potential) the electron flux to the substrate is much greater as compared with RF bias etching. This is because for a floating electrode the electrons arriving at the electrode are given by [54]

$$n'_{e\,floating} = n_e \exp(-\frac{e(V_p - V_f)}{KT_e}) \tag{4.1}$$

whereas for a biased electrode

$$n'_{e\,biased} = n_e \exp(-\frac{e(V_p - V_{dc})}{KT_e}) \tag{4.2}$$

where n_e is the electron density in the plasma, e is the electronic charge, k is the Boltzman constant, T_e is the electron temperature and V_p, V_f and V_{dc} are the absolute value of the plasma potential and the bias electrode potential respectively. Since V_p-V_f<< V_p-V_{dc} and the mean free speeds are nearly equal ($\overline{C_e'^2} = \overline{C_e^2}$) to maintain the charge flux balance at the electrode [54, 55],

$$n'_{e\,floating} \rangle\rangle n'_{e\,biased} \tag{4.3}$$

Thus, the number of electrons arriving at the floating electrode is much higher as compared to the biased electrode. The number of ions arriving at the sheath edge n_i stays nearly the same due to space charge limited ion current. Though the above analysis is for dc plasma, for rf plasma the same analysis holds true. In addition, the electrons that reach the floating electrode suffer an $e(V_p-V_f)$ loss of kinetic energy in crossing the sheath, which is much smaller compared to the biased case. Therefore, the electrons in the biased case have energies greater than the electrons in the biased case when they arrive at the electrode surface. Because of the large electrons flux the measured dc bias was positive whereas during rf bias conditions dominant ion flux to the surface developed a negative dc bias.

Wet oxidation was used to grow the thin oxide (15nm) at 900°C on cleaned silicon wafers. Doped polysilicon was then deposited by LPCVD. The end-point of polysilicon etching was determined using a He-Ne laser interferometer with 10% over-etch. A control wafer (sample #1) was prepared by wet etching polysilicon in KOH at 75°C. MOS capacitor structures were formed by evaporating Al dots (300 μm and 600 μm in diameter) in a resistive heating vacuum evaporator using a shadow mask on one half of the area of the wafer for electrical characterization. The 300 μm diameter capacitors were used for high frequency, quasi-static C-V and DLTS measurements and 600μm diameter dots were used for oxide breakdown measurements.

The other half of the area of the wafers was used for physical characterization using XPS. Each wafer was cleaved into several samples and separately analyzed to verify the uniformity of etch results. Spectra typical for each etching condition are reported. The samples were transferred in air from etching facility to the XPS instrument.

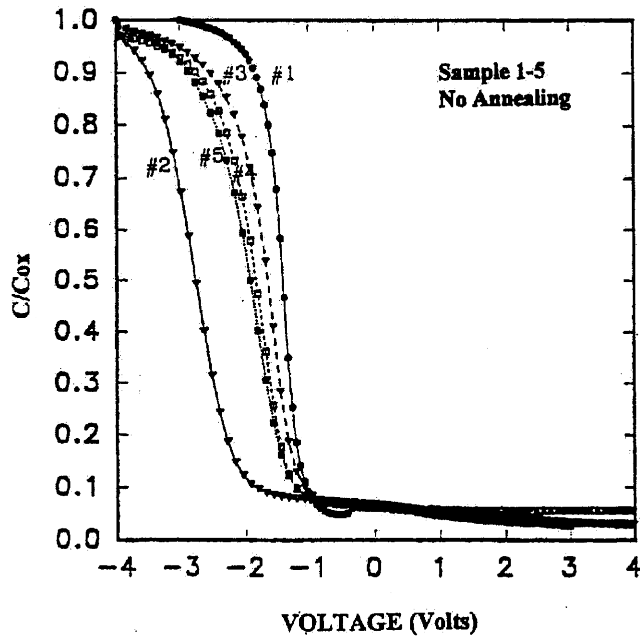
All spectra were obtained using unmonochromatized Al K_α radiation. XPS was performed both before and after annealing to 250°C in UHV and no significant changes were observed.

4.3 Measurement Results

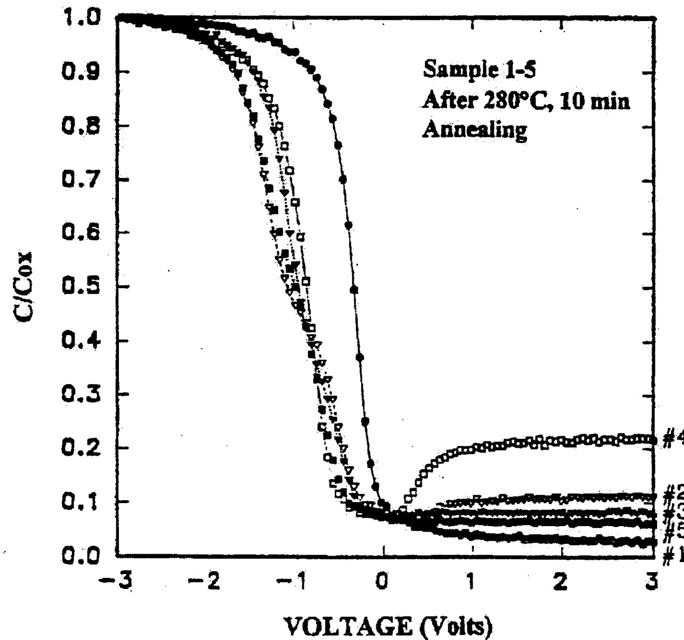
4.3.1 C-V Measurements

Normalized high-frequency C-V curves for various MOS samples immediately after aluminum deposition (before any metal annealing) are shown in Figure 4.2(a) where the flat band voltages were measured. The corresponding positive charge densities in the oxide for samples 1-5 are measured and compared. Highest charging effects were observed for the sample without any wafer bias (sample #2) and an increase in charging effect was also observed for increase in wafer bias (sample #3 being the lowest and sample #5 being the highest). These samples were then annealed at 280°C for 10 min in N_2 ambient [56] to eliminate any charging effects that was created at the metal-oxide interface during metal evaporation. Figure 4.2(b) shows the high-frequency C-V characteristics of samples annealed after metal deposition. A recovery in flat-band voltage was noticed for all samples. Taking the control sample (sample #1) as reference flat-band voltage shifts (δV_f) of –0.905, -0.67, -0.57 and –0.857 V were observed for samples 2-5 respectively. The shift pattern of the flat-band voltage in both unannealed and annealed samples remained the same, which indicates the presence of a considerable amount of oxide charge due to plasma etching, though the interface stated between the metal and the oxide annealed out during metal annealing. A strong presence of fast interface states was also observed in the C-V curves for sample #2 compared with other

samples. In high-frequency C-V measurements the effects of the interface states are neglected as the interface trapped charge varies with gate bias whereas the fixed oxide charge (r_f) is independent of gate bias. The modification to the fixed oxide charge can mainly due to the carrier trapping during etching. Besides, a small component of mobile ionic charge (Q_m) might have been added due to sputtering of the sidewalls of the reactor.



(a)



(b)

Figure 4.2 Normalized C-V characteristics of various samples: (a) immediately after metal deposition; (b) after a 10 minutes annealing at 280°C in N_2 ambient.

The quasi-static C-V measurement for annealed MOS capacitor including the control sample (sample #1) are shown in figure 4.3. A strong deformation of C-V curves is observed in sample #2, indicating generation of interface traps during etching. The damage to the interface in the above sample is possibly due to plasma induced electrical charging effects produced mainly because of non-uniformity current stressing during the over-etch process [57]. Though the current stressing due to plasma nonunifomity is very small in the ICP reactor etch damage has occurred for minimal local nonuniformity. The density of interface traps generated during plasma etching, when extracted from the combination of high-frequency and quasi-static C-V curves, indicated plasma

nonuniformity in the case of sample #2 where a positive dc potential was induced (Table 3.1) at the floating rf electrode. The positive dc potential increased the electron flux towards the wafer, producing lager damage to the oxide. An increase in the interface state density D_{it} is noticed for the plasma etched samples. D_{it} of the control sample (wet etched) in negligible whereas D_{it} values for samples 2 - 5 were 8.9×10^{11} cm^{-2}, 4.4×10^{11} cm^{-2}, 2.4×10^{11} cm^{-2} and 8.1×10^{11} cm^{-2} respectively. In addition, when the wafer bias was increased (sample #5) the density of the interface traps increased as compared to sample #3 and #4 as damage due to ion bombardment because dominant at higher rf power. No increase in nonuniformity is noticed at higher biased in this reactor. Therefore, at a constant ICP power the wafer bias should be minimum to reduce plasma etching induced electrical damage to thin gate oxide in an ICP reactor.

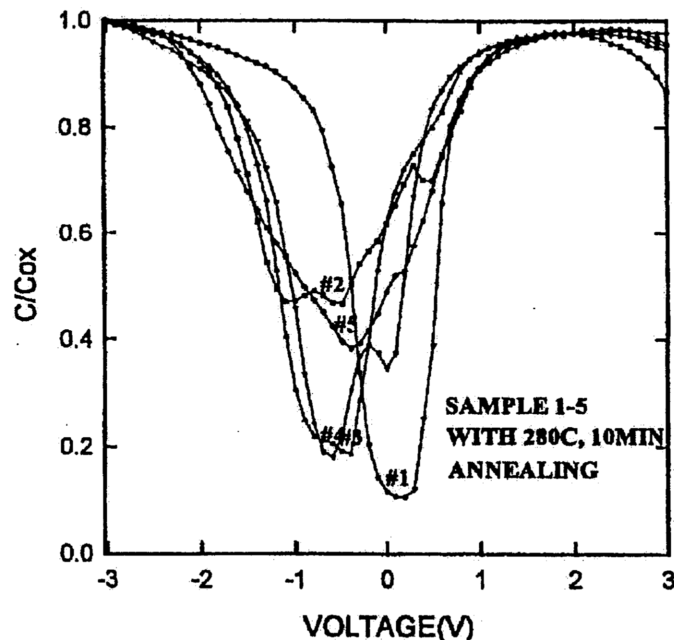


Figure 4.3 Quasi-static C-V curves for MOS capacitors after plasma etching in an ICP reactor with different process conditions.

4.3.2 Breakdown Measurements

Figure 4.4 shows the breakdown distribution on samples immediately after aluminum deposition. During the ramped voltage breakdown (RVBD) measurements, the Al gate electrodes were biased negatively with respect to the substrate. The applied stress field was increased by 0.5 MV/cm (200 ms/step) until the current exceeded 1.0 μA. It can be noticed that samples with higher oxide charge density in Figure 4.4 show a lower breakdown field. The wet etched wafer (sample #1) exhibited the highest breakdown field while the wafer with zero rf bias (sample #2) exhibited the lowest breakdown field. For wafers etched under various biasing conditions (sample #3-5) the values of breakdown fields were higher than sample #2 and were found to decrease with increasing substrate bias power. The correlation between breakdown and positive charge trapping can be explained by breakdown model that assumes that breakdown results from enhancement of the electrical field at the interface due to the oxide charging.

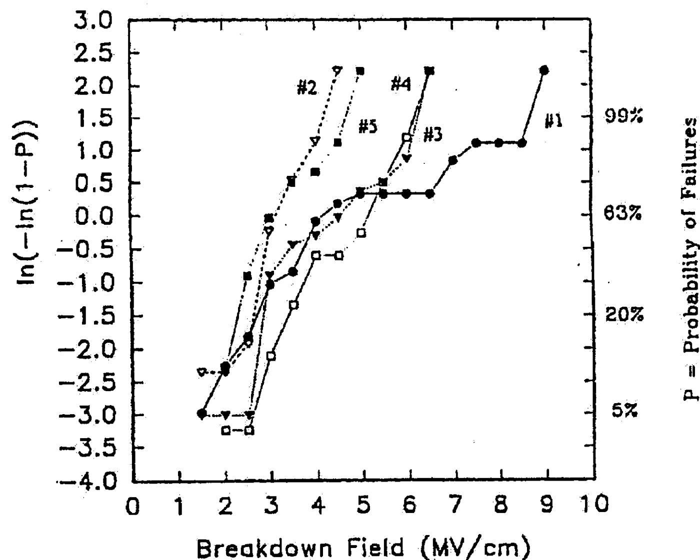


Figure 4.4 The breakdown distribution of various samples.

4.3.3 DLTS Analysis

Representative DLTS spectra observed in the control sample (#1) and the plasma etched sample (#4) are presented in figure 4.5. The quiescent voltage V_a and pulse voltage V_b were 0.5 and –1.5V respectively. The spectra show a peak around 370 K for both sample #1 and sample #4, which is attributed to minority carrier generation, since the peak height increased with increasing quiescent bias voltage V_a [58]. Comparing the two curves it can clearly seen that interface traps have been created in sample #4 and no interface traps were observed in the control sample (wet etched) at the same sensitivity.

The interface trap density N_{ss} for sample #4 was calculated using the following equations [58]:

$$N_{ss}(E_t) = [C(t_2) - C(t_1)]\frac{C_{ox}\varepsilon_s N_A}{C^3(t_1)kT\ln(t_1/t_2)} \tag{3.4}$$

$$E_t = E_v + \frac{kT}{q}\ln\left(\sigma_p v_{th} N_v \frac{t_2 - t_1}{\ln(t_2/t_1)}\right) \tag{3.5}$$

where $C(t_1)$ and $C(t_2)$ are the capacitance transient values at times t_1 and t_2 respectively, C_{ox} is the oxide capacitance per unit area, ε_s is the dielectric constant of silicon, N_A is the substrate doping, σ_p is the capture cross section of the traps, E_t and E_v are trap energy level and top of the valence band respectively, v_{th} is the thermal velocity of carriers, k is Boltzmann's constant, T is the absolute temperature and N_v is the effective density of states in the valence band.

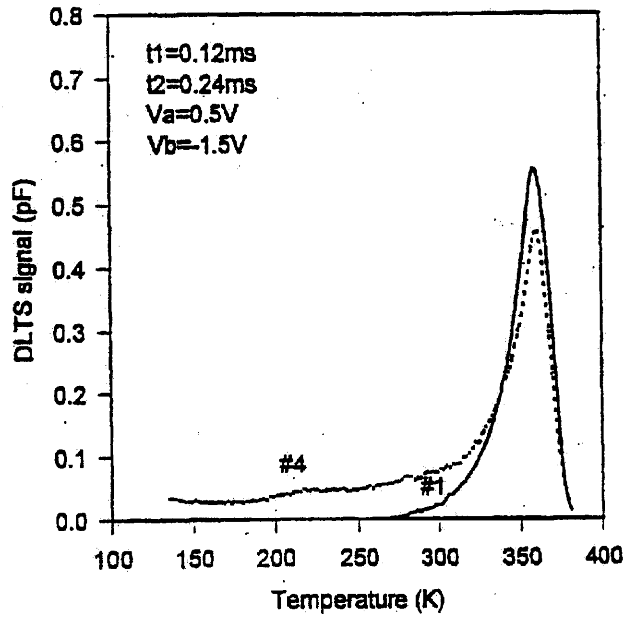


Figure 4.5 DLTS spectra for the control sample (#1) and the plasma etched sample (#4)

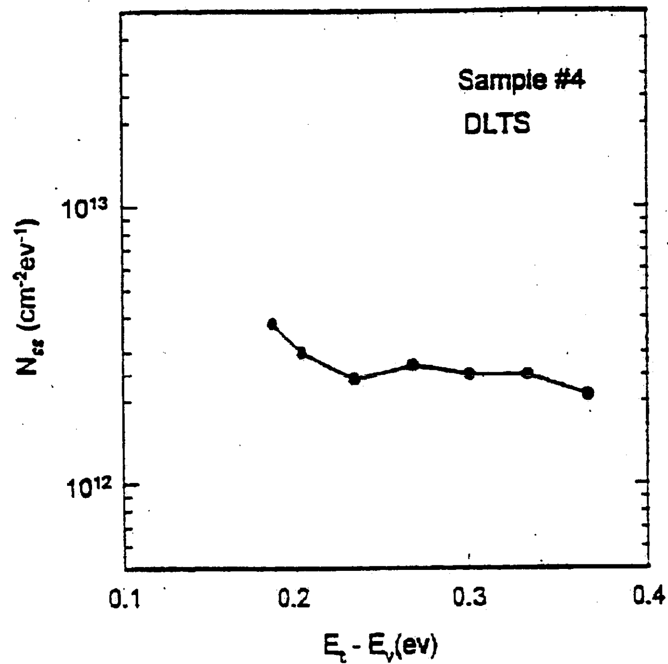


Figure 4.6 Interface traps density N_{ss} in the plasma etched sample (#4) as a function of energy.

DLTS measurements of the majority carrier band edge are limited by the response time of the capacitance meter and by the lowest temperature the DLTS system can reach. Also they are limited toward midgap by the minority carrier generation peak [59]. The interface traps density (N_{ss}) can be measured for energy values 0.19 eV < $E_t - E_v$ <0.37 eV. N_{ss} for the plasma etched sample (#4) as a function of energy is shown in 4.6. The trap density was obtained after taking a capture cross-section value of $\sigma_p = 10^{-5}$ cm^{-2}. The N_{ss} value obtained using DLTS technique is higher than the N_{ss} value obtained using quasi-static technique. This could be attributed to the fact that DLTS can be influenced by energy and temperature dependence of the capture cross-section [60] or by the error of combined high- and low- frequency technique. No bulk trap has been detected by DLTS.

4.3.4 XPS Characterizations

Figure 4.7 shows XPS spectra obtained from these samples. The peak near 104 eV corresponds to stoichiometric SiO_2 with silicon in the 4+ oxidation state [Si(4+)]. The feature near 99 eV is from the Si substrate [Si(0)] under the oxide. The intensity between 100 and 103 eV corresponds to Si in oxidation states Si(n+) (n=1, 2, 3). These intermediate oxidation states are typically associated with defective SiO_2 where the bonds between Si and (4-n) of its O neighbors in the SiO_4 tetrahedral unit have been broken and replaced by Si or some similar bonding. As can be seen from this figure 4.7 the density of intermediate oxidation states is very similar for each process except for etching with zero-bias power condition (sample #2).

To see whether all suboxides are produced uniformly, or whether some states are preferred, the area under each peak is plotted in figure 4.8. To obtain the data, each Si 2p spectrum was fitted to the sum of five Gaussian pairs, a pair representing the 2p1/2 and 2p3/2 spin orbit split components at an intensity ratio of 1:2 for each oxidation state. For each spectrum, the same chemical shift, ΔE_n, and peak width for the Si(n+) oxidation state was assumed* and fits were determined by minimizing χ^2 while varying the intensity of each pair. A comparison of the percentage of total Si 2p intensity attributed to each oxidation state yield essentially the same plot.

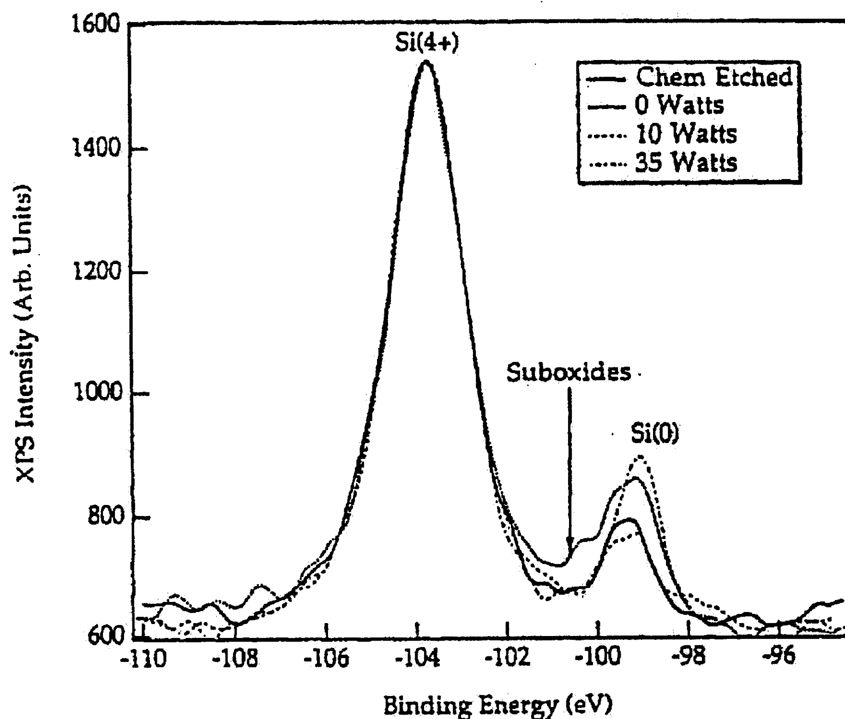


Figure 4.7 XPS spectra of various samples.

* Peak shift for the oxidation states Si(n+) (n=1, 2, 3, 4) relative to the Si(0) line were 1.1, 2.0, 2.8 and 3.25 eV to higher binding energy, respectively. Peak widths were taken as a resolution-limited 0.75 eV except for Si(4+) which, owing to an intrinsic width of 1.15 eV, was taken as 1.35 eV. These values are consistent within our resolution with those determined for the thin oxide by synchroton radiation techniques (cf[62])

Although a quantitative comparison of the density of different oxidation states cannot be made without correcting the cross section variation [61], the relative concentration of a given oxidation state for each sample can be concluded directly. Figure 4.8 clearly shows that the sample with zero bias (sample #2) has a significantly higher density of Si (1+) states as compared to the other samples. This configuration is either an Si bonded to a single O whose three other bonds are terminated by residual H incorporated in the oxide during the wet oxidation process, or it represents the braking of the bonding of a substrate Si to a bridging O at the Si-SiO_2 interface.

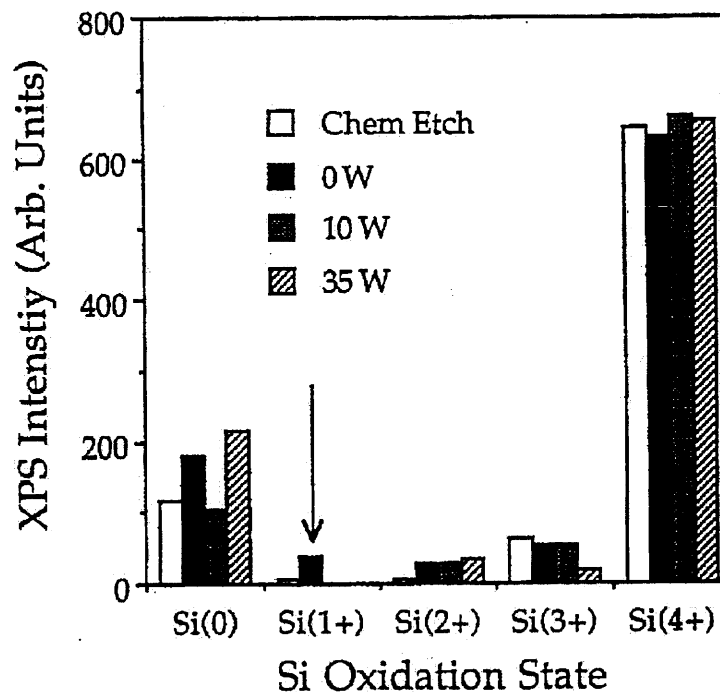


Figure 4.8 XPS counts for various suboxide states.

4.4.1 Discussion of Results

In this study, damage to the thin oxide due to surface charging is noticed, even a device does not have floating conductive gates, to concentrate the tunneling current at weak region in the oxide during the overetch period [62-64]. A very uniform plasma obtained in this reactor when the inductive power and rf power exist together, minimizes the probability of surface charging. During the zero-bias condition, the substate is floating and electron flux to the substrate is much greater as compared with rf biased etching. In addition, even though a Langmuir probe was employed to study the nonuniformity, any spatial resolution very close to the wafer surface could not be obtained and finer scale nonuniformities beyond the sensitivity of the probe were also undetected. Therefore, it is believe that either the damage is caused by the high-energy electron impact or due to the existence of localized plasma nonuniformity when only rf coil was powered. The nonuniform plasma could stimulate the accumulation of charges on gate electrode. These stored charges can cause an electric breakdown of the thin gate oxide [72]

A possible mechanism is that the high electron flux causes tunneling current to flow through the thin oxide. This tunneling current can induce surface states at Si-SiO_2 interface and trap charge in oxide [62, 64]. It is interesting to note that previous attempts to study radiation damage with low-energy electron beams have found [65] enhancement of the Si(3+) oxidation state as opposed to the Si(1+) as observed here. This may be due to energy of the bombarding electrons generated in the plasma, or it may be the results of a cooperative effect from simultaneous electron and ion bombardment.

4.5 Summary

Electrical damage to the thin oxide during etching was found in good agreement with the physical damage. From the XPS study, it can be concluded that degradation of the thin oxide is associated with creation of suboxidation state. Besides, the major possible mechanisms responsible for damage in this study appear to be high-energy electron charging when only the ICP power is activated without any bias power applied to the wafer carrying electrode. Energetic ion bombardment damage is dominant when the wafer-carrying electrode is biased and in the condition the damage increases with increases in power rf bias.

CHAPTER 5

PLASMA INDUCED DAMAGE TO STRAINED $Si_{1-x}Ge_x$

5.1.1 Electrical Studies on SF_6 and O_2 Plasma Etched $Si_{1-x}Ge_x$ p^+-n Heterojunction

In this study, the electrical measurements I-V & C-V characteristics of wet etched, SF_6 plasma etched, un-etched and O_2 ashed samples of $Si_{1-x}Ge_x$ p^+-n heterojunction were presented. These electrical evaluation methods can serve as very sensitive qualitative measurements of heterojunction quality. In addition, material characterizations of these samples by SIMS and TEM have been performed.

The $Si_{1-x}Ge_x$ wafers used for this experiment were grown by RTCVD techniques. An n-type (As doped) silicon (1×10^{16} cm^{-3}) layer (500nm) was first grown on a n^+-Si substrate. Then a p-type (1×10^{19} cm^{-3}) strained $Si_{0.86}Ge_{0.14}$ epitaxial layer (40 nm) was grown on it at 900°C for 20 seconds. Finally, a 120nm p-silicon (1×10^{16} cm^{-3}) cap was deposited (Figure 5.1 and Figure 5.2). The wafer was cut into several pieces. Then went through different processes to study the plasma etching damage and contamination effects.

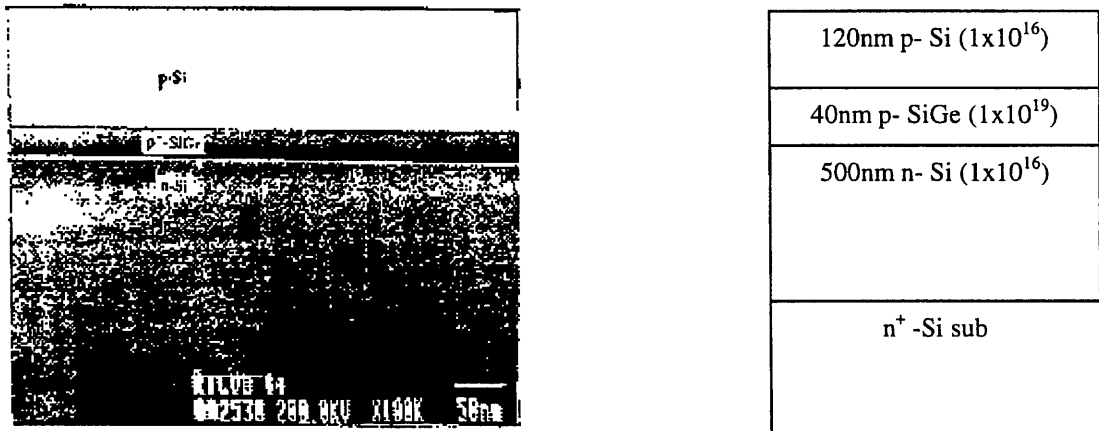


Figure 5.1 Scanning electron microgragh of the RTCVD wafer.

5.1.1 Sample Preparations

The fabrication of heterojunction structures often requires making contact to buried SiGe layer. Making contact to the $Si_{1-x}Ge_x$ region requires etching overlying Si and stopping at the $Si_{1-x}Ge_x$ layer. This process has been simulated in this study by producing sample #1 and sample #2. The p-silicon cap layer in sample #1 was removed using strain sensitive etchant composed of 100g KOH, 4g $K_2Cr_2O_7$, and 100mL propanol in 400 mL of water at 26°C [2]. The wet etching rate of Si is 16 nm/min (Figure 5.3), that is 20 times higher than etching rate of strained $Si_{1-x}Ge_x$. The p-silicon cap of sample #2 was removed using plasma etch in a DRYTECH 100 plasma reactor under the pressure of 150 mTorr, a RF power of 400 W (0.3 W/cm^2), 50 sccm SF_6 and 50 sccm Freon 115, for 30 seconds. The etching rate of Si is 240nm/min. The SIMS analysis showed that Si cap had been completely removed and the etching just stopped at the $Si_{1-x}Ge_x$ interface. It was also found that for SF_6 plasma the $Si_{1-x}Ge_x$ surface is Ge rich. This has already been reported by G. S. Oehrlein et al. [43]. In sample #3 and sample #4 the p-silicon cap layers were not removed. The contacts (300 μm diameter) of samples 1-4 were formed by depositing aluminum dots on the front of these samples through a shadow mask whereas blanket depositions were made on the backside of these samples (Figure 5.4). A post-metal annealing was done in nitrogen ambient at 300°C for sample #3 and sample #4 to form the heterojunction diodes. To study the effect of oxygen plasma ashing, sample #4 was exposed to O_2 plasma for 5 minutes under the pressure of 150 mTorr, the RF power of 600 watts (0.44 W/cm^2) and gas flow of 20 sccm. This process is equivalent to the standard O_2 plasma process used to remove the photoresist and clean the wafer after defining the metal pattern.

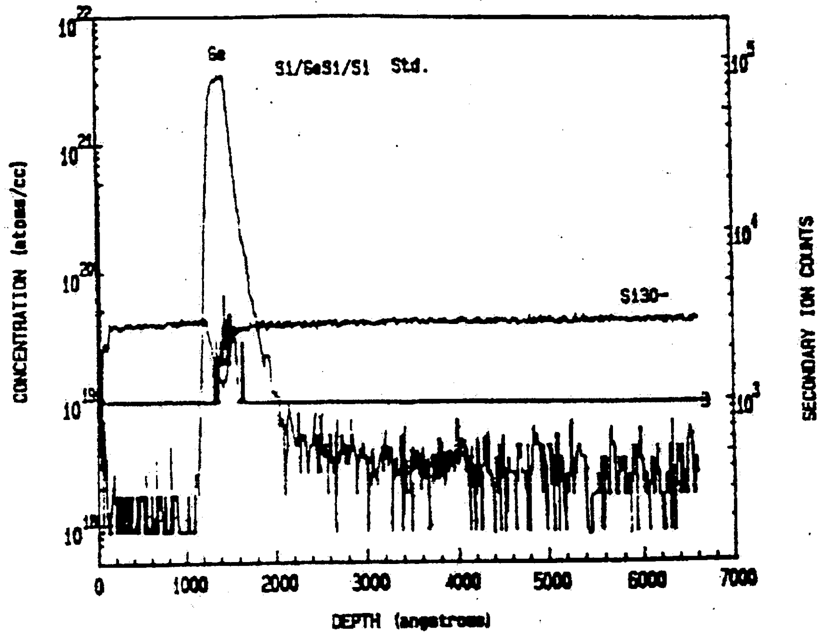


Figure 5.2 SIMS profiles for as-grown RTCVD sample.

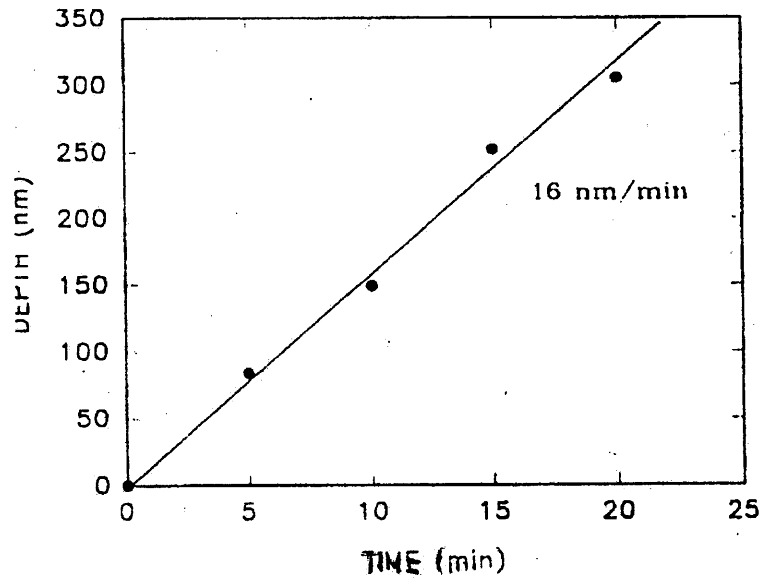


Figure 5.3 Wet etching results.

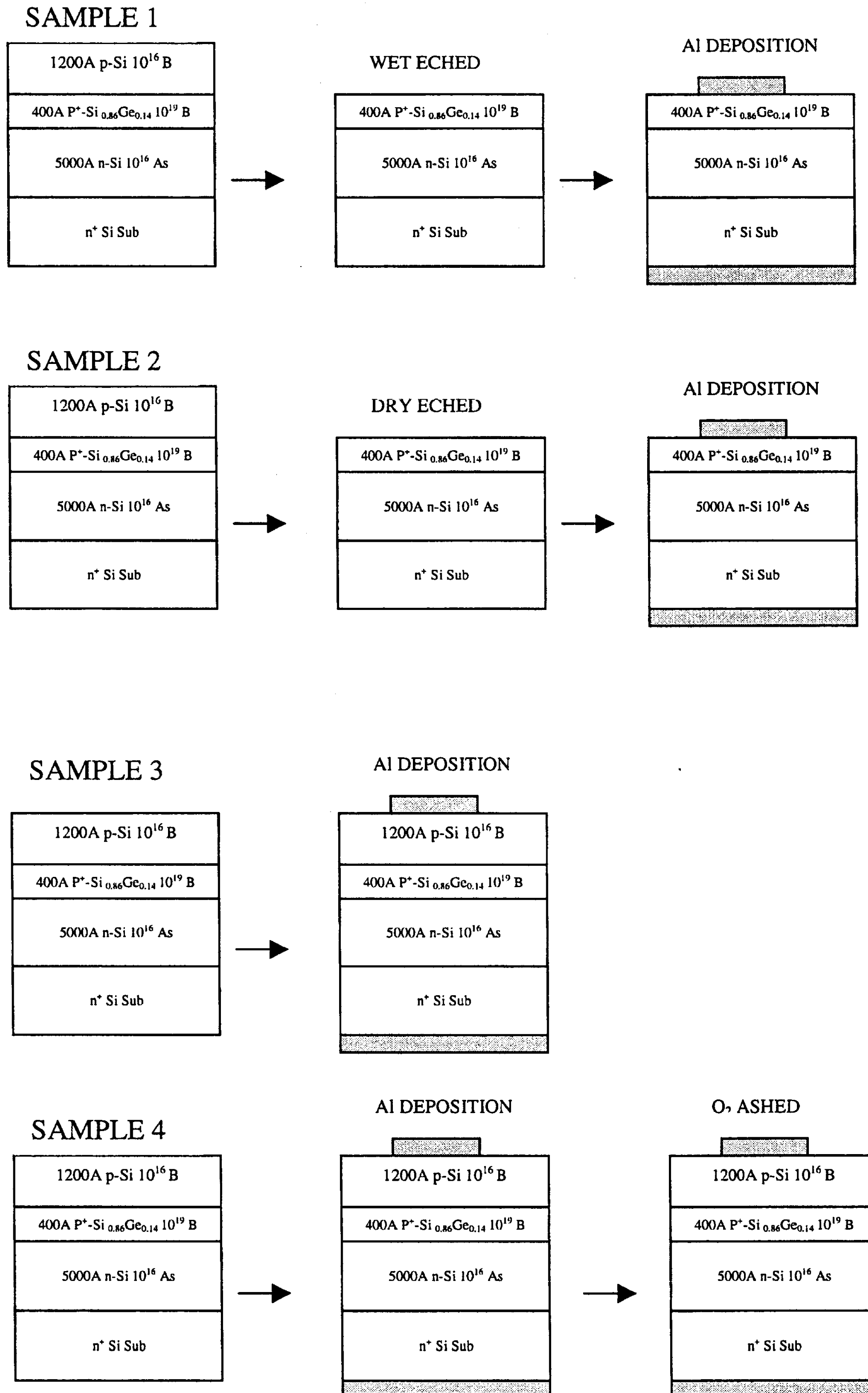


Figure 5.4 Device structures were used for study and comparison.

5.1.2 Current-Voltage Measurements

I-V characteristics of the wet etched sample #1 and plasma-etched sample #2 are shown in the Figure 5.5. The I-V degradation has the following features: 1) in the initial region, the current level of the plasma etched sample is higher than the wet etched sample for a given voltage. This indicates that higher recombination current has been generated. 2) at higher biases where the diffusion component is stronger, the current level of the plasma etched sample drops below that of wet etched sample. During the plasma etch, the $Si_{1-x}Ge_x$ might have been partially relaxed by forming misfit dislocations. Therefore, the band gap of the $Si_{1-x}Ge_x$ layer would increase which would reduce the current level [66]. 3) a degradation in the non-ideality factor in noticed (from 1.4 to 2.2) after etching indicating a recombination dominance in the forward characteristics because of generation of more recombination sites caused by stress during plasma etching.

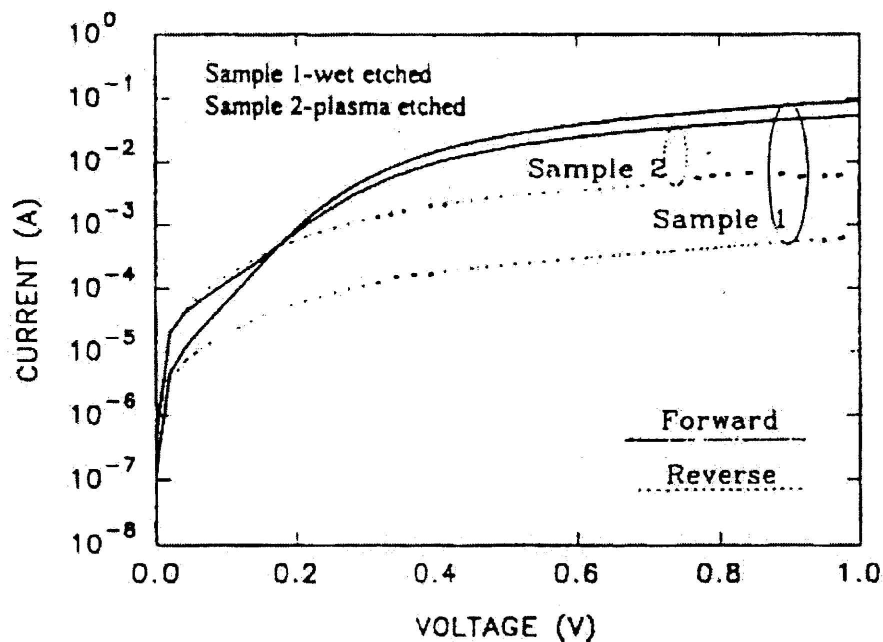


Figure 5.5 The I-V characteristics of wet etched sample #1 and SF_6 plasma etched sample #2.

5.1.3 C-V Measurements

C-V measurement of the wet etched sample #1 and SF6 plasma etched sample #2 are shown in the Figure 5.6. This also confirms that the SF_6 etching has negative effect. The capacitance is higher than the wet etched samples. This is because dry etching damages the sample and creates electrically active states in the depletion region. Interface charges in the electrically active stated can contribute to a parasitic capacitance (C_s) which acts in parallel to the depletion capacitance (C_d) [67-69]. Therefore, the overall capacitance is higher than the wet etched samples.

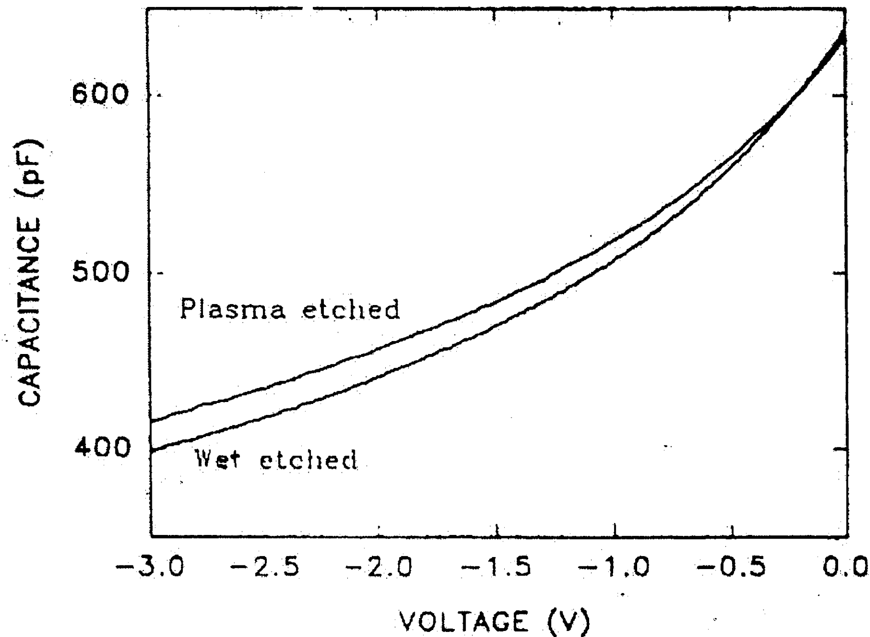


Figure 5.6 The C-V characteristics of wet etched sample and SF_6 plasma etched sample.

5.1.4 TEM Analysis

Through the use of TEM, it was found that dislocation loops were formed in $Si/Si_{1-x}Ge_x$ /Si outside the aluminum region due to the ion bombardment stress. The density of the

dislocation loops is low ~1.9×10^{10} cm^{-2}. The loops are between 1-1.4 nm in size, and extend 238 nm deep (Figure 5.7(b)).

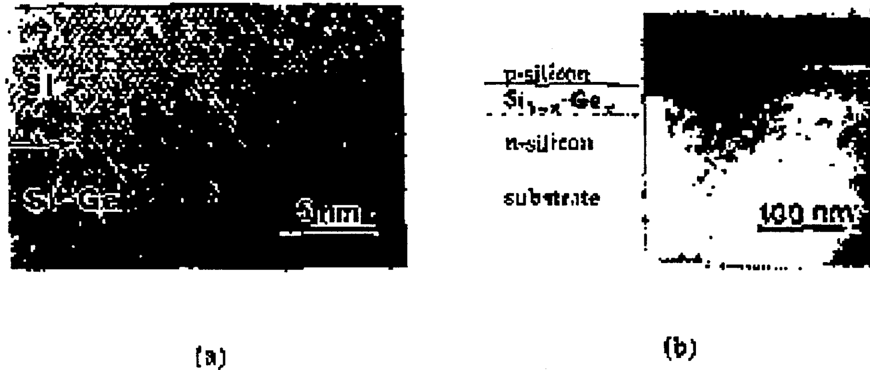


Figure 5.7 (a) High resolution TEM of Si/ $Si_{1-x}Ge_x$ /Si interface after plasma ashing.
(b) Weak beam dark field TEM micrograph showing the dislocation loops.

5.1.5 Effects of O_2 Plasma Ash Process

I-V characteristics of the un-etched sample #3 and O_2 plasma ashed sample #4 are shown in Figure 5.8. The difference in the I-V characteristics between two samples was not at all substantial. This is because of the Si/$Si_{1-x}Ge_x$ /Si was not directly exposed to the plasma. Si/$Si_{1-x}Ge_x$/Si had been shield by aluminum layer. The forward current of O_2 ashed sample is slightly lower than that of the un-etched sample. This is might be due to an increase in the series resistance of the ohmic contact caused by plasma electrical stress. C-V profiles for sample #3 and #4 are almost identical.

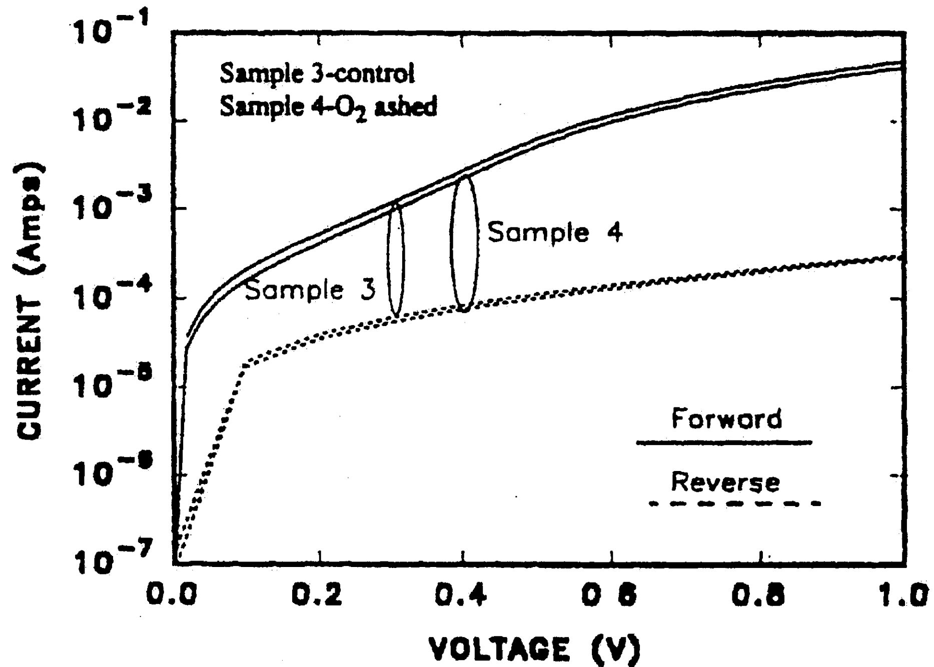


Figure 5.8 The I-V characteristics of un-etched sample #3 and O_2 plasma ashed sample #4.

5.1.6 Summary

SF_6 plasma was used to etch an overlying Si film stopping at the $Si_{1-x}Ge_x$ strained film. This can cause electrical damage to $Si_{1-x}Ge_x$/Si heterojunction device. The damage is mainly because of ion bombardment and radiation-induced bonding changes. Plasma etching creates interface charges and more recombination centers that can give higher depletion capacitance, and decrease the diffusion current. The O_2 plasma has no strong effect on the $Si_{1-x}Ge_x$ device when the device is protected by its aluminum contact layer. That is good for $Si_{1-x}Ge_x$ device process.

5.2 Evaluation of Plasma Process-Induced Bandgap Modification of a Strained $Si_{1-x}Ge_x$ Heterostructure Using MOS Capacitor

In this study, a capacitance-voltage (C-V) profiling technique on $Si_{1-x}Ge_x$ MOS capacitor to estimate the change of band gap of $Si_{1-x}Ge_x$ film (grown on p-type substrate) exposed to plasma etching and subsequent annealing process has been employed. C-V profiling is a fast and efficient approach to estimate plasma process-induced band-gap modifications, since measurement techniques such as photoemission measurement, x-ray photoelectron spectroscopy, or photoreflectance measurement can be time consuming.

5.2.1 Sample Preparations

The typical structure of the MOS capacitor used in this study is schematically shown in Figure 5.9. One characteristics of this structure is that the $Si_{1-x}Ge_x$ quantum well layer is located within the depletion layer formed by gate bias. Thus, this device structure allows the Fermi level at each hetero-interface to be varied by changing the gate voltage and, as a result, allows the position where holes are accumulated to be controlled, as described below.

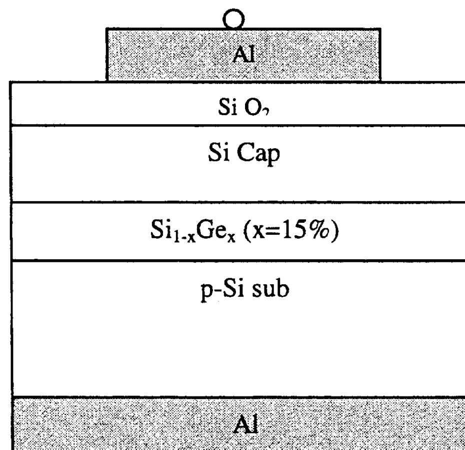


Figure 5.9 Typical structure of $Si_{1-x}Ge_x$ MOS capacitor used in this study.

Under the slight depletion condition, as shown in Figure 5.10 (a), the surface of the top Si is depleted and holes are accumulated only in the $Si_{1-x}Ge_x$ well. Under the strong accumulation condition (Figure 5.10 (b), holes are accumulated both in the top Si surface layer and in the $Si_{1-x}Ge_x$ well region. When the magnitude of the negative gate is sufficiently large, the incremental charges associated with ac gate voltage are formed only into the accumulation layer of the Si top surface.

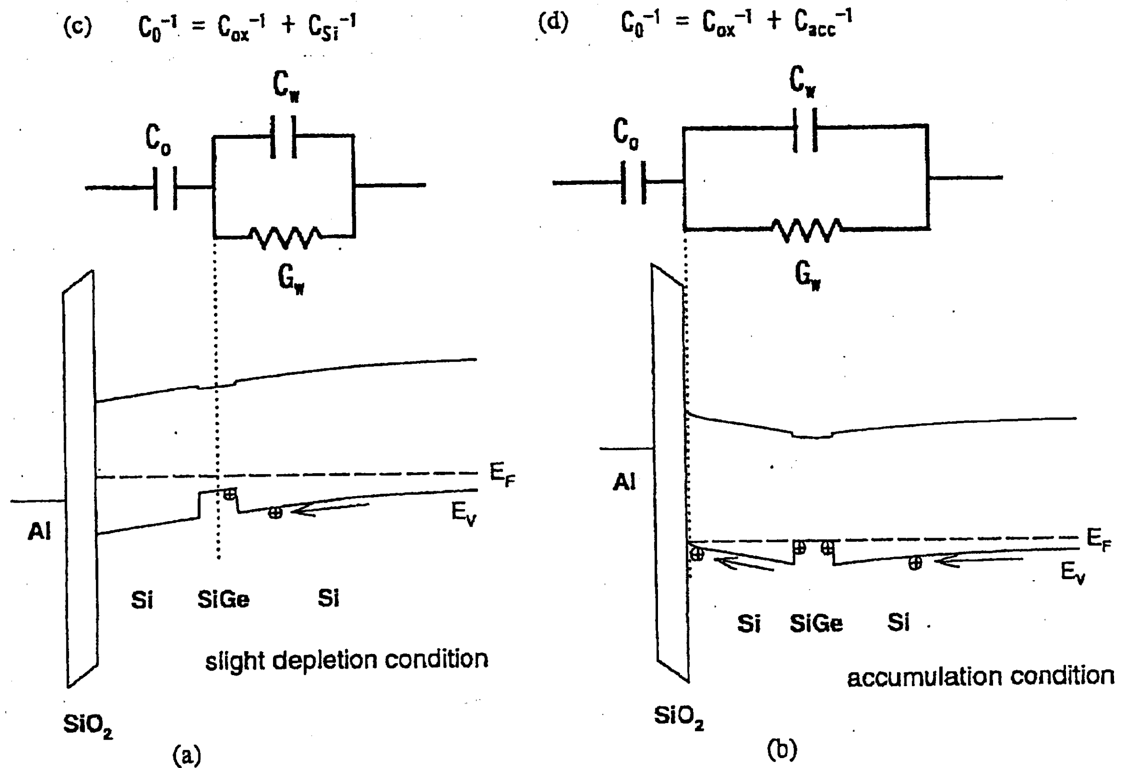


Figure 5.10 Schematic band diagram under the slight depletion condition (a) and the accumulation condition (b).

15% of Ge is used to grow strained $Si_{1-x}Ge_x$ film for high-mobility advantage. Undoped 50 nm thick $Si_{1-x}Ge_x$ (x=0.15) was grown on a p-Si (2×10^{16} cm^{-3}) substrate by conventional chemical-vapor deposition (CVD) at 700°C at atmospheric pressure. A 150 nm thick Si cap layer was deposited on the $Si_{1-x}Ge_x$ layer. Plasma etching was performed

in a DRYTECH 100 plasma reactor at a chamber pressure of 150 mTorr with flow rate of 50 sccm SF6 and 50 sccm Freon 115. The RF power was 400 W. The etch rate was 4nm/s and etch was continued for 28s for partial removal of the Si cap layer (approximately 110 nm). On the other hand, wet etching was carried out in a solution of 25 mg KOH, 1mg $K_2Cr_2O_7$, 25 ml propanol in 100 ml of water at 26°C. The etch rate was 16nm/min and etching was continued for 7 min. Both the dry and wet etched samples were annealed at temperatures of 500, 600, 700 and 800°C for 60 s in a rapid thermal process (RTP) reactor under vacuum. SiO_2 was then deposited by low-pressure CVD at 450°C, so as to minimize the thermal budget, which could cause the relaxation of strain in the $Si_{1-x}Ge_x$ layer. The thickness of SiO_2 was 40 nm. Aluminum dots were then evaporated through a metal mask by thermal evaporation to make metal-oxide-semiconductor (MOS) capacitors. Back contact was made with Aluminum deposition on the Si substrate. A postmetal annealing was carried out at 350°C in N_2 ambient.

5.2.2 High Frequency C-V Measurements

High frequency C-V measurements were performed using Boonton 71BD capacitance meter. Figure 5.11 shows a typical C-V profile obtained for wet etched samples. There is a distinct kink in the un-annealed sample and the nature of the kink changed as the annealing was performed at temperature of 500, 600, and 700°C. No such kink was observed for samples annealed at 800°C. The kinks of dry etched samples, as shown from the C-V plots (Figure 5.12), have similar trends as wet etched samples as the annealing temperature increased. The kinks for wet etched samples are more pronounced than dry

etched samples under same annealing condition. These C-V plots had flat band corrections.

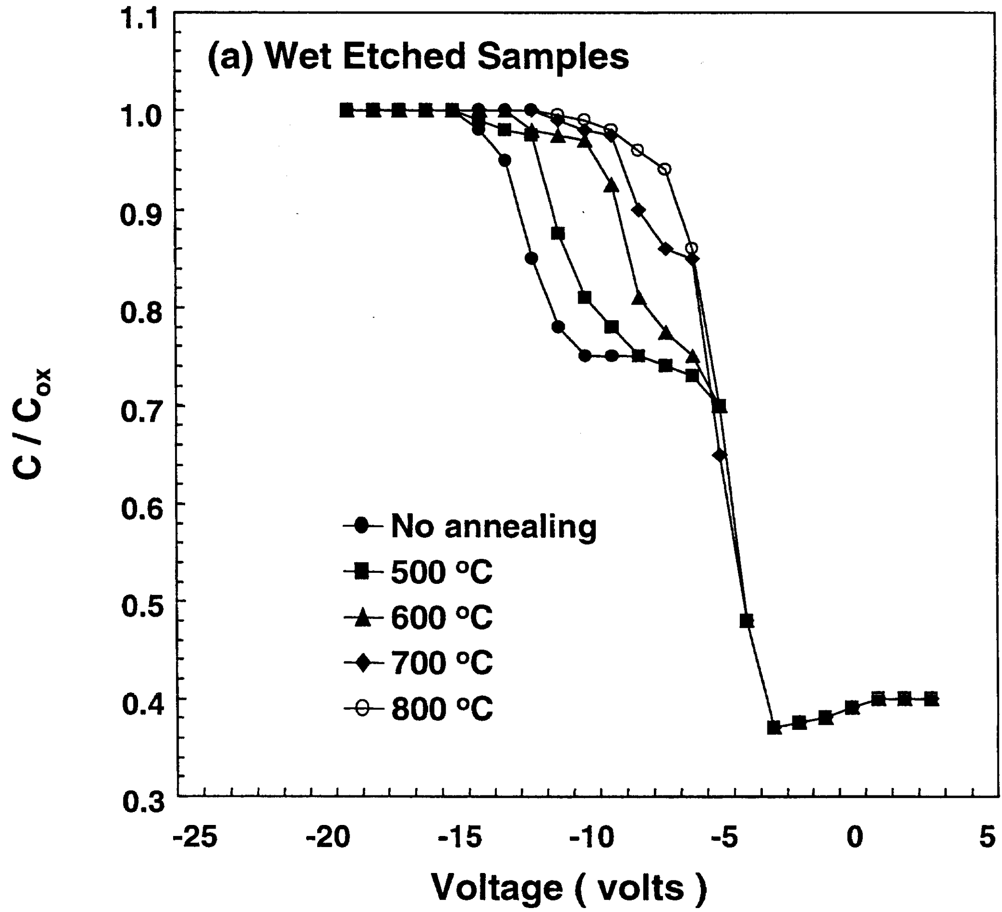


Figure 5.11 Typical C-V profiles obtained for the wet etched samples.

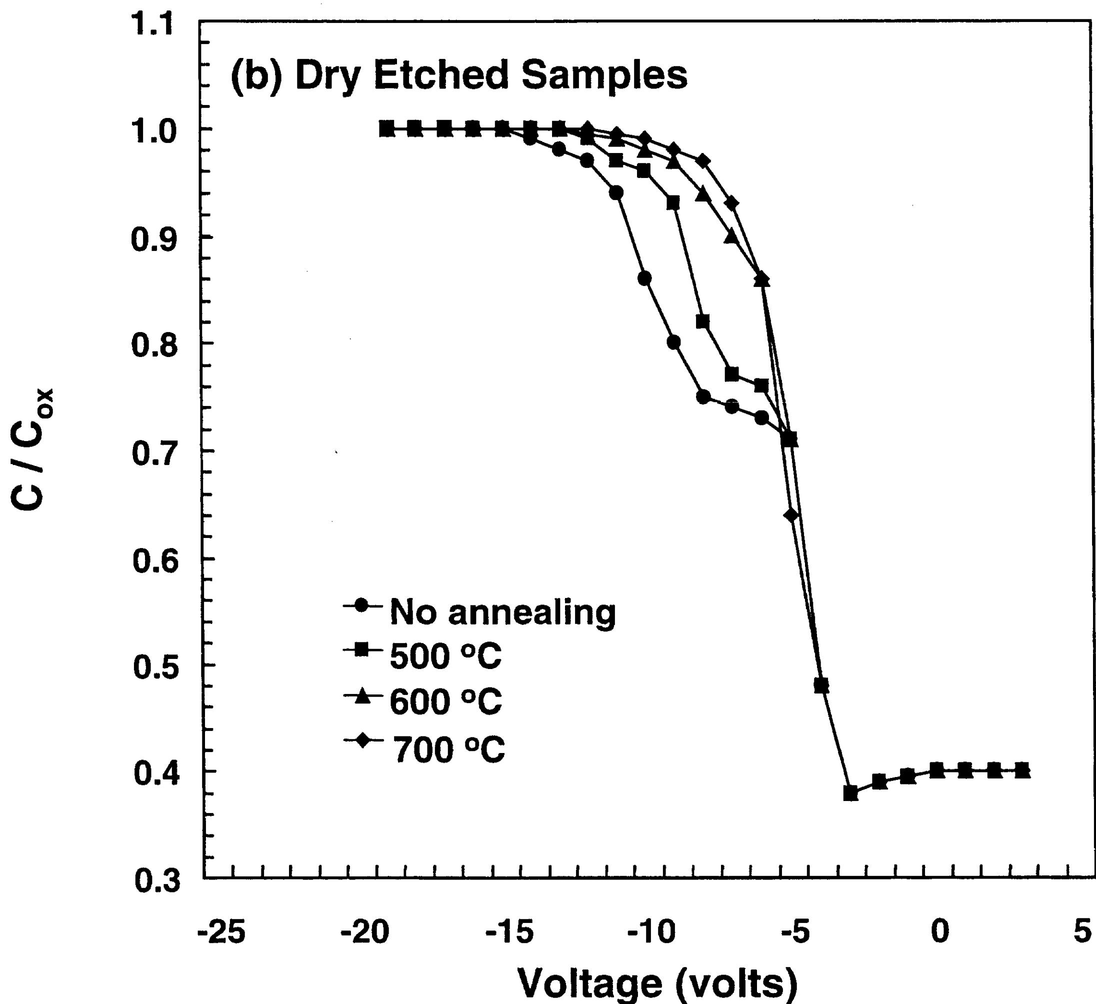


Figure 5.12 Typical C-V profiles obtained for the dry etched samples.

5.2.3 Device Simulation

It has been reported that the kinks are due to the present of strained $Si_{1-x}Ge_x$ layer [45]. When the $Si_{1-x}Ge_x$ /Si MOS is driven form slight depletion to accumulation mode (Figure 5.10), holes are accumulated only in the $Si_{1-x}Ge_x$ quantum well region. Since the total capacitor equals the series combination of C_{ox} and $C_{SiGe\ well}$, the total capacitance will be smaller than the MOS capacitance without $Si_{1-x}Ge_x$ well. When applied voltage becomes

more negative, more holes will be accumulated into the accumulation layer at the Si O_2/Si interface instead of the $Si_{1-x}Ge_x$ well. The total capacitor will finally equal to C_{ox}. If the bandgap of strained $Si_{1-x}Ge_x$ layer has been increased due to the relaxation after high temperature annealing or plasma etching, the kink will be relatively smaller. When the $Si_{1-x}Ge_x$ layer is completely relaxed, the E_g of $Si_{1-x}Ge_x$ will be as same as Si, no more kinks will be observed. To verify this finding, several device simulations (using Silvaco's Atlas) have been carried out. Table 5.1 summarized the structures simulated in this section. Figure 3.11 shows the dimension of these structures.

Table 5.1 List of simulated $Si_{1-x}Ge_x$ MOS structures

Structure name	**Description**
G1	Ideal SiGe MOS capacitor
G2	SiGe capacitor with Eg=1.12 eV for SiGe*
G3	SiGe capacitor with fixed charge (Q_f = 2e11 cm^{-2}) in SiO_2
G4	SiGe capacitor with interface donor-like traps at SiO_2/Si interface (Density=2e12, e.level=0.4eV**)
G5	SiGe capacitor with interface donor-like traps at SiO_2/Si interface (Density=2e12, e.level=0.3eV)
G6	SiGe capacitor with interface donor-like traps at SiO_2/Si interface (Density=5e11, e.level=0.4eV)
G8	SiGe capacitor with fixed charge (Qf=2.5e12) and interface donor-like traps at SiO_2/Si interface (Density=3.5e12, e.level=0.23eV)
G9	SiGe capacitor with fixed charge (Qf=2.5e12) and interface donor-like traps at SiO_2/Si interface (Density=2e12, e.level=0.23eV)
G10	SiGe capacitor with fixed charge (Qf=2.5e12) and interface donor-like traps at SiO_2/Si interface (Density=1e12, e.level=0.23eV)
G11	SiGe capacitor with fixed charge (Qf=2.5e12) and interface donor-like traps at SiO_2/Si interface (Density=0.5e12, e.level=0.15eV)
G12	SiGe capacitor with fixed charge (Qf=2.5e12) only
G9'	SiGe capacitor with fixed charge (Qf=2.5e12) and interface donor-like traps at SiO_2/Si interface (Density=2e12, e.level=0.23eV), SiGe: Eg=1.12eV
G10'	SiGe capacitor with fixed charge (Qf=2.5e12) and interface donor-like traps at SiO_2/Si interface (Density=1e12, e.level=0.23eV), SiGe: Eg=1.12eV
G11'	SiGe capacitor with fixed charge (Qf=2.5e12) and interface donor-like traps at SiO_2/Si interface (Density=0.5e12, e.level=0.15eV), SiGe: Eg=1.12eV
G12'	SiGe capacitor with fixed charge (Qf=2.5e12) only, SiGe: Eg=1.12eV

* *Eg*=1.01 eV has been used for all strained $Si_{1-x}Ge_x$ in structures G1 and G3-G12.

** *e.level*=E_t-E_v, where E_t is the trap energy level and E_v is the valence band energy level.

Firstly, G1 and G2 structures have been simulated to see the effect of bandgap increase due to plasma induced $Si_{1-x}Ge_x$ relaxation. From Figure 5.13 it can be observed that the kink from strained $Si_{1-x}Ge_x$ is smaller than the observed data shown in Figure 5.11. That is because the valence band difference (ΔE_v=0.11 eV) is not significant enough to create a large kink during accumulation. In simulations, E_g=1.12 eV (same as Si) was used for completely relaxed SiGe, while ΔE_v=7.4x=111 meV [70] and E_g=1.01 eV were used for strained $Si_{1-x}Ge_x$ (x=15).

The value of C_{ox}, calculated using equation 5.2.1,

$$C_{ox} = \varepsilon_o \varepsilon_r \frac{A}{d} \qquad (5.2.1)$$

where ε_r=3.9, ε_o=8.854x10^{-14} F/cm, A=1 μm, d=40 nm. The calculated value 8.6x10^{-16} F/μm is smaller than value of 9.2x10^{-16} F/μm as shown in Figure 5.13. This is because the top and bottom electrodes are not symmetrical in our simulation. If the top and bottom electrodes have identical areas the calculated value matches the simulation result. The fringing field effect normally neglected during the calculation of experimental samples due to their large aspect ratio of A/d, but for these simulated structures it has to be accounted for. The effective area A_{eff}=9.2/8.6=1.07 μm.

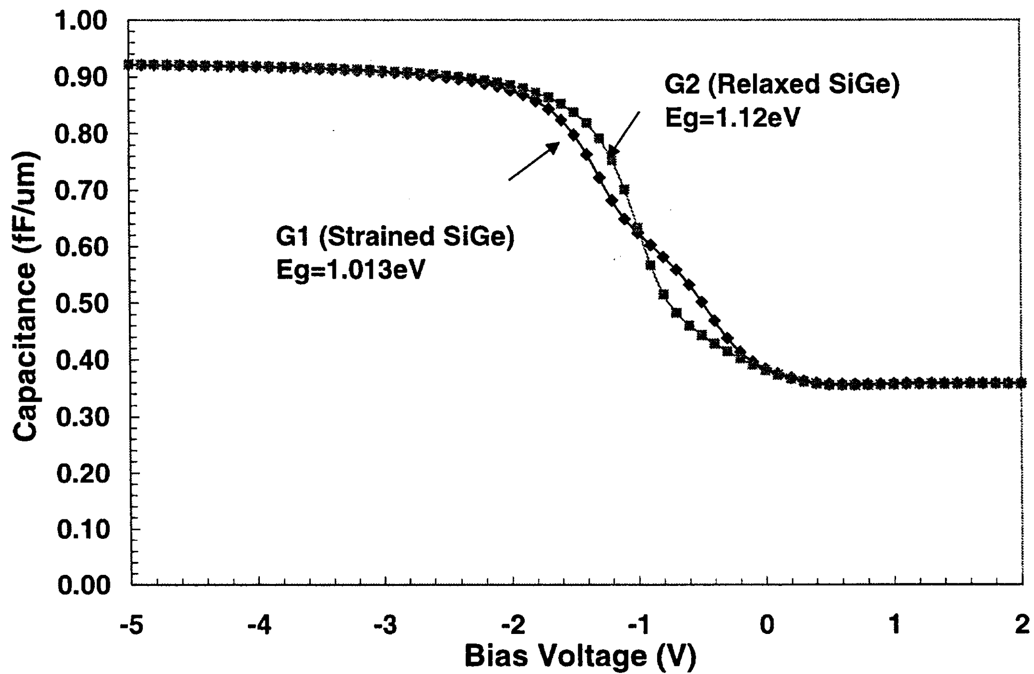


Figure 5.13 Simulated C-V plots of $Si_{1-x}Ge_x$ MOS capacitors with different energy bandgap values.

Figures 5.14 and 5.15 can be used to explain the higher capacitance of strained SiGe (G1) compared to that of relaxed SiGe (G2) when the bias is from 0 to –1V (under slight depletion region). Even though the Silicon buffer layer is still depleted, because the energy difference (*Ef-Ev*) at back strained SiGe/Si interface is less compared to the energy difference (*Ef-Ev*) in silicon buffer region (Figure 5.14), some holes start to be accumulated in SiGe quantum well (Figure 5.15). The incremental charges associated with ac gate voltage are formed only in the SiGe quantum well. Since the effective depletion depth is reduced to the thickness of silicon cap layer, the total capacitance with quantum well is higher compared to completely relaxed film without quantum well.

Figures 5.16 and 5.17 can be used to explain the lower capacitance of strained SiGe (G1) compared to that of relaxed SiGe (G2) when the bias is from –1 to –1.25 V (under slight accumulation region). That is because holes are still accumulated in SiGe well instead of at SiO_2/Si interface. The total capacitor, which equals to the combination of C_{ox} and $C_{SiGe\ well}$ in series, becomes smaller compared to relaxed SiGe film without quantum well.

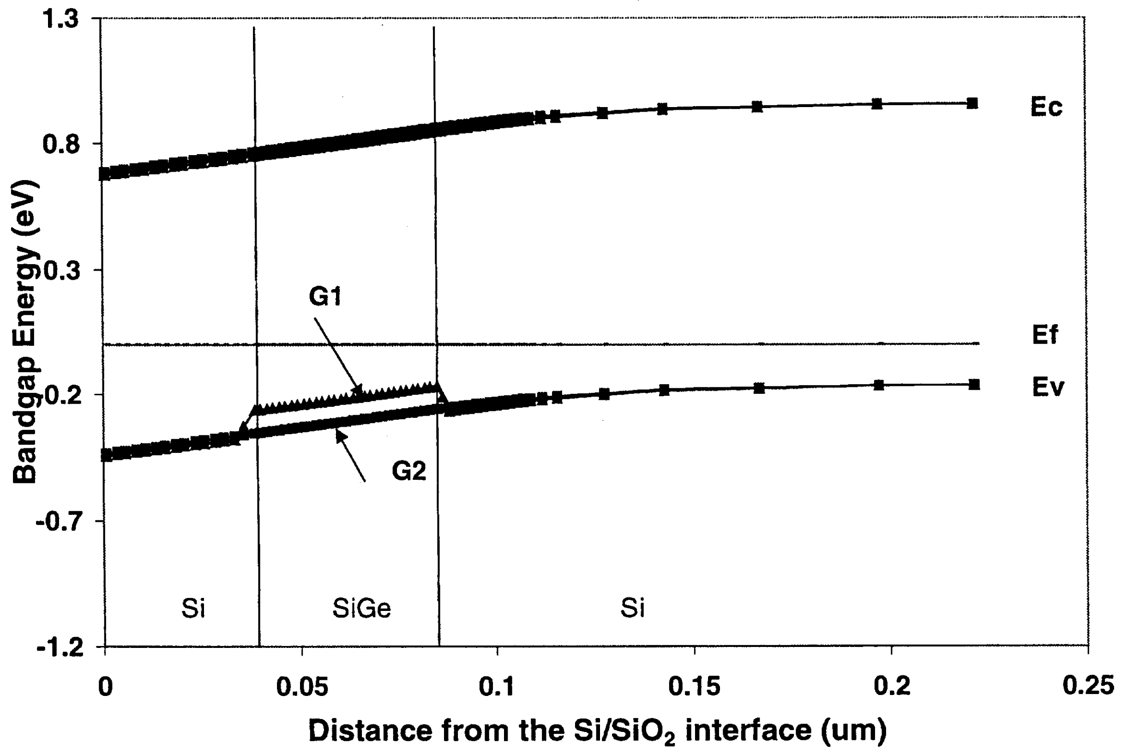


Figure 5.14 Energy band diagram in G1 and G2 under –0.5V bias.

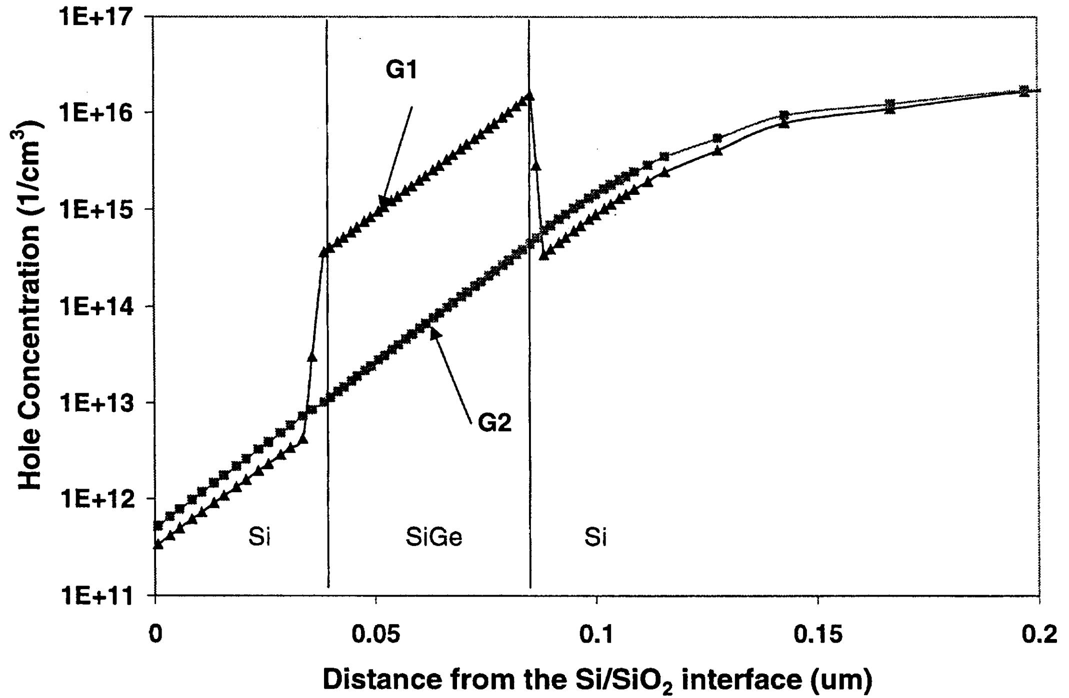


Figure 5.15 Hole concentration in G1 and G2 under –0.5 V bias.

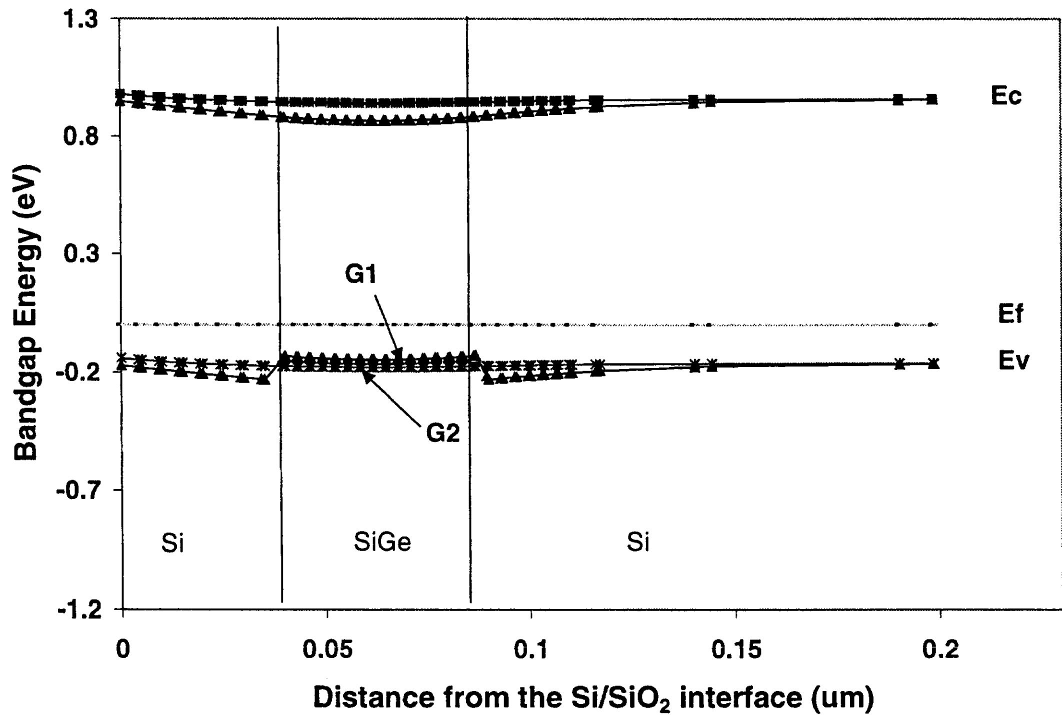


Figure 5.16 Energy band diagram in G1 and G2 under –1.25 V bias.

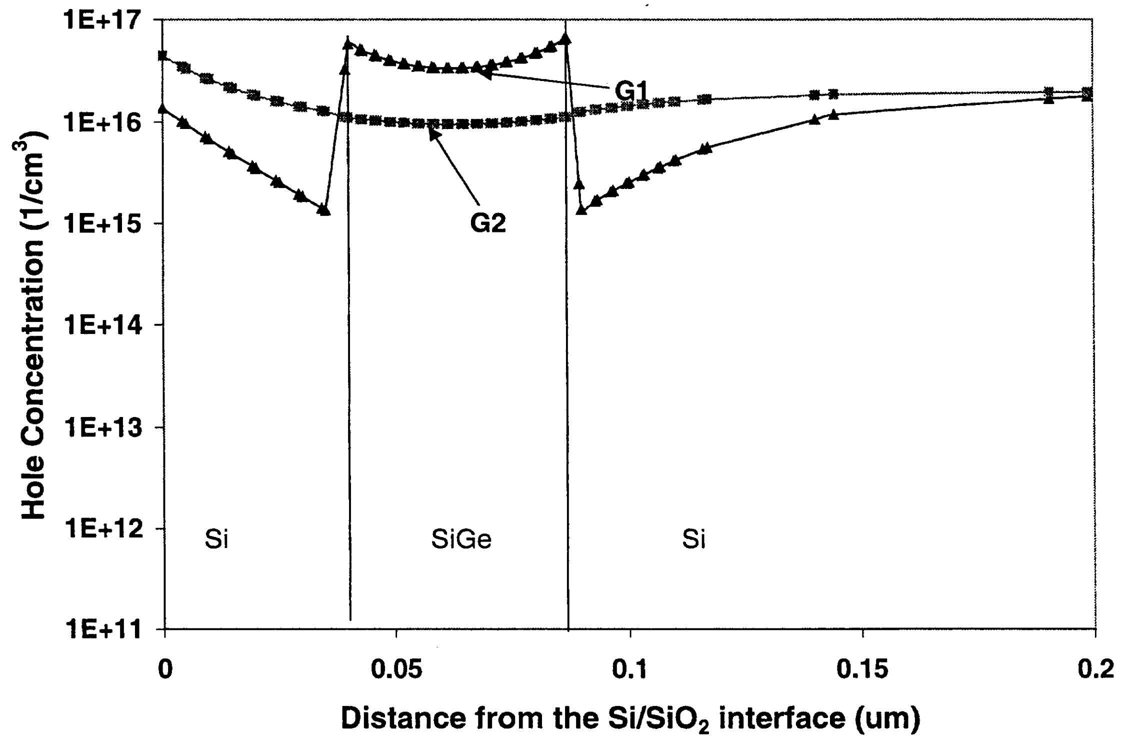


Figure 5.17 Hole concentration in G1 and G2 under –1.25V bias.

Secondly, effects of SiO_2 fixed positive charges have been simulated with structure G3, strained SiGe capacitor with fixed oxide charge of $2x10^{11}$ cm^{-2}. If the energy level of donor trap is well above the Fermi level even at the large reverse bias then the charge state of this trap is bias independent and it is referred to as "fixed charge trap". The fixed positive charge produces a parallel shift of the C-V curve to the left (see Figure 5.18) by ΔV_{FB} of 0.37 V which is in agreement with calculated result (Eq. 5.2.3).

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_o} \qquad (5.2.2)$$

where Q_f, Q_m and Q_{ot} are fixed-oxide charges, mobile ionic charges and oxide-trapped charges respectively. If use equation 5.2.3 to calculate the effect of fixed charge ($2x10^{11}$ cm^{-2}) on flat band voltage, the ΔV_{FB} will be:

$$\Delta V_{FB} = -\frac{\Delta Q_f}{C_o} = -\frac{1.6\times10^{-19}\times2\times10^{11}\times1.07\times10^{-8}}{9.2\times10^{-16}} = -0.37V \qquad (5.2.3)$$

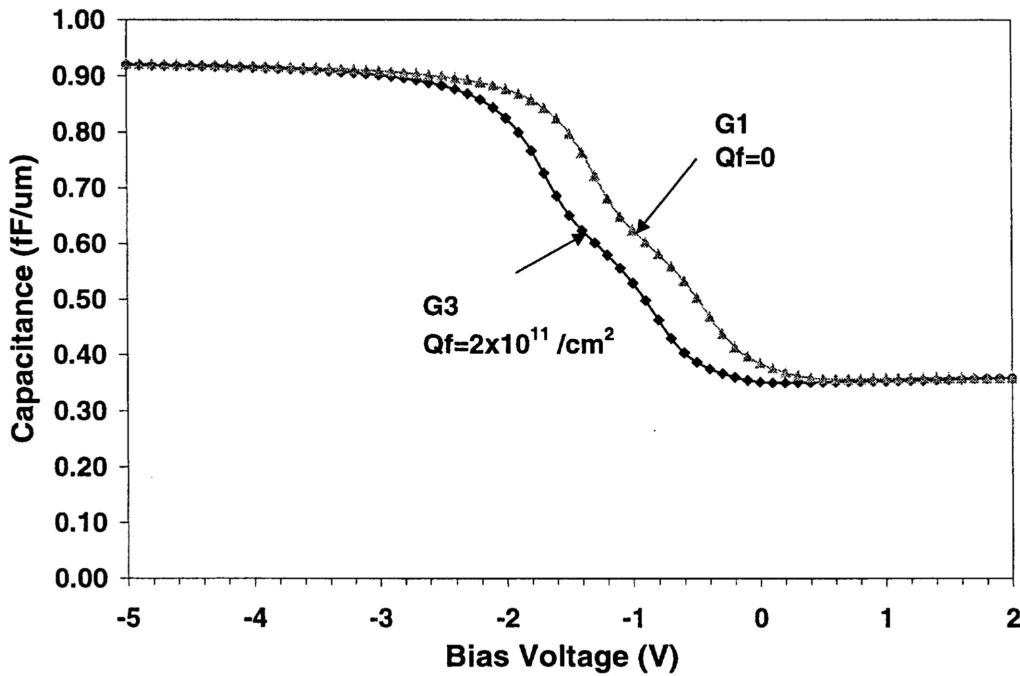


Figure 5.18 Simulated C-V plots of $Si_{1-x}Ge_x$ MOS capacitor with SiO_2 fixed positive charges.

Thirdly, structures G4-G6 have been simulated to see the effects of interface trap densities and their positions in the bandgap (Figure 5.19). The simulations have used the single-level surface states. The device simulations show that the big steps or kinks from measured C-V plots are mainly due to the present of donor-like interface traps at the low temperature silicon oxide (LTO). The trap has been predicted theoretically, by Tamm and

by Shockley [71], that because of disruption of the periodicity of the lattice at a surface, a high density of state will be introduced into the forbidden gap near a semiconductor surface. Such states have traditionally been called *fast surface states*. The charge in the fast surface states will vary with the band bending or surface potential. At reverse bias condition the quasi-Fermi level at top of cap Si is higher than the trap energy level, these donor-like traps filled with electron and become neutral. When the quasi-Fermi level moves lower than the trap energy level, these traps start to release the electrons and become positive charges. Thus the increase of capacitor becomes slower and the step or kink is created. After the interface traps released all trapped electrons, the depletion decreases quickly when the reverse bias becomes more negative. The Capacitance increases and finally equals C_{ox}. The C-V curve after kink has the same shape as G1 (ideal $Si_{1-x}Ge_x$ MOS capacitor) and only shifts to left due to these fixed charges and positive charge from interface traps.

The step in the C-V curve moves up when the trap energy level moves closer to valence band with constant trap density (G4 vs. G5). The C-V curve shifts to the right side when the trap density reduces with constant trap energy level (G4 vs. G6). The flat band voltage (V_{FB}) of G4 and G6 are shifted by -0.93 V and -3.7 V respectively from G1 due to the total interface trap density of $5x10^{-11}$ cm^{-2} and 2 $x10^{-12}$ cm^{-2}.

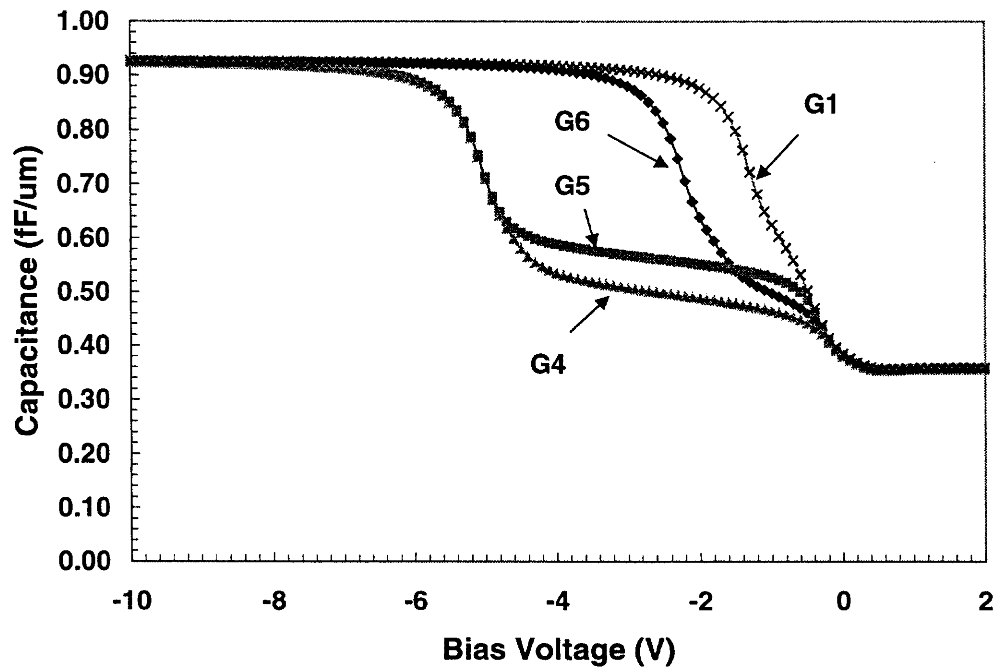


Figure 5.19 Simulated C-V plots of $Si_{1-x}Ge_x$ MOS capacitor with SiO_2 interface traps (with different trap densities and different trap energy levels).

Finally, various interface trap densities, trap energy levels and fixed charges are used to replicate the observed experimental results. Structures G8-G12 have been simulated (Figure 5.20) to match the C-V plot in Figure 5.11. Structures G9'-G12' which have energy bandgap (E_g) of 1.12 eV for SiGe layer to match the condition of relaxed SiGe film have been added for comparison in Figure 5.21. Figure 5.21 shows that the change in the shape of kink is caused by the interface charge reduction as well as relaxation in SiGe film.

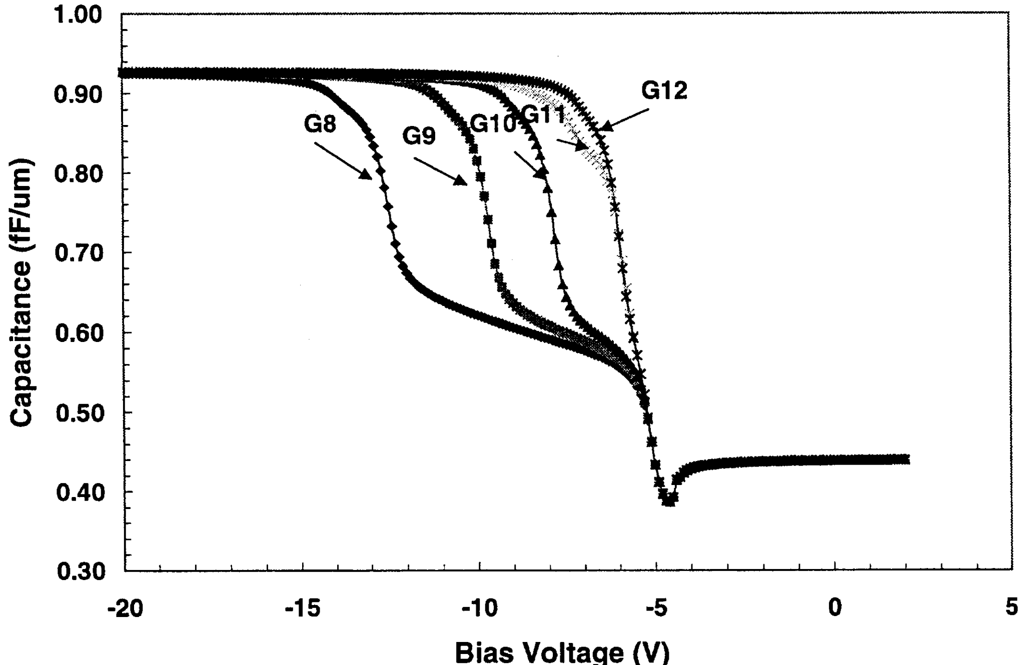


Figure 5.20 Simulated C-V plots of $Si_{1-x}Ge_x$ MOS capacitor with SiO_2 fixed positive charges and interface traps to match Figure 5.11.

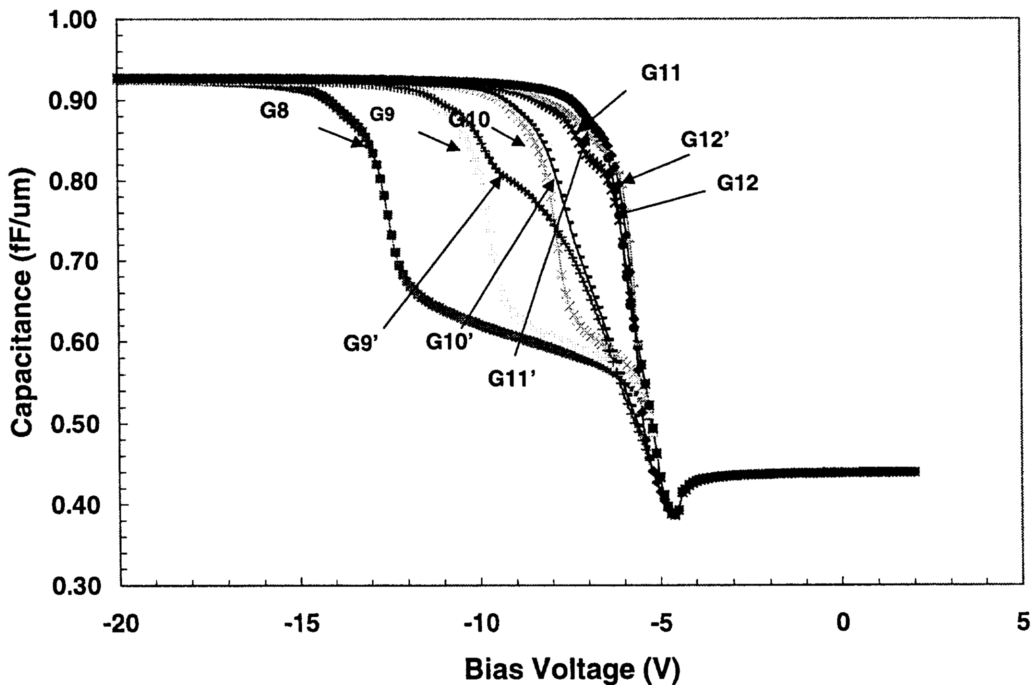


Figure 5.21 Simulated C-V plots of $Si_{1-x}Ge_x$ MOS capacitor with additional relaxed structures (G9', G10', G11' and G12') for comparison.

5.2.4 Discussion of Results

The presence of interface traps at poorly formed Si/SiO_2 interface heavily influences the C-V characteristics as evident from the simulation. Because the oxide was deposited at low temperature the built-in fixed oxide charges are also higher. The effect of the fixed charge can be determined by the flat band correction since the shift of the C-V curve is parallel.

Figure 5.11 shows that the high temperature annealing (at 500 °C and 600 °C) reduces the total interface trap density at SiO_2/Si interface, while 700 °C annealing might also reduce the energy level. The kink disappeared after the 800 °C annealing due to complete removal of interface trap. This explanation has been simulated in Figure 5.20 using structure G8-G12 to replicate the measured plots in Figure 5.11.

High quality SiO_2 is necessary for using C-V profiling to detect the plasma induced damages to $Si_{1-x}Ge_x$ MOS capacitor. The simulations show that the interface trap densities should be less than 10^{11} cm^{-2}. This would result in minimal distortion needed to determine the valence band offset between the strained SiGe and Si. Thermally oxidized silicon surfaces have relatively low density of fast surface states, but the process normally requires high temperature (700-1200 °C), which could cause the relaxation of strain in SiGe layer. If one tries to use LTO in the test structures, as done in this work, additional Si control capacitors with no SiGe well need to be included to eliminate the effect of interface effects in C-V measurement for extraction of integrity of strained SiGe film.

For SiGe MOS with moderate interface trap density, it may still use the C-V profiling by expanding the coordinate of C-V curves at a slight depletion region where the holes start to be accumulated in SiGe well due to the valence band offset at back

Si/SiGe interface. Because under this condition the Fermi level at Si/SiO_2 interface is not low enough to let interface traps to release trapped electrons, the change of C-V curve is only caused by ΔE_v change and is not due to the change of interface trap charge. Using this method to examine Figures 5.11 and 5.12, it can be concluded that wet etched sample after 800°C annealing and dry etched sample after 700 °C annealing are partially relaxed. Dry etched sample demonstrates a faster relaxation mechanism as compared to its wet etched counterpart. The C-V plot should be taken with fine steps at this region in order to distinguish the difference between strained and partially relaxed film. The slopes of C-V plot at slight accumulation region for dry etched samples are also smaller than for the wet etched samples. That indicates that the dry etching changes the properties of Si surface or SiGe layer.

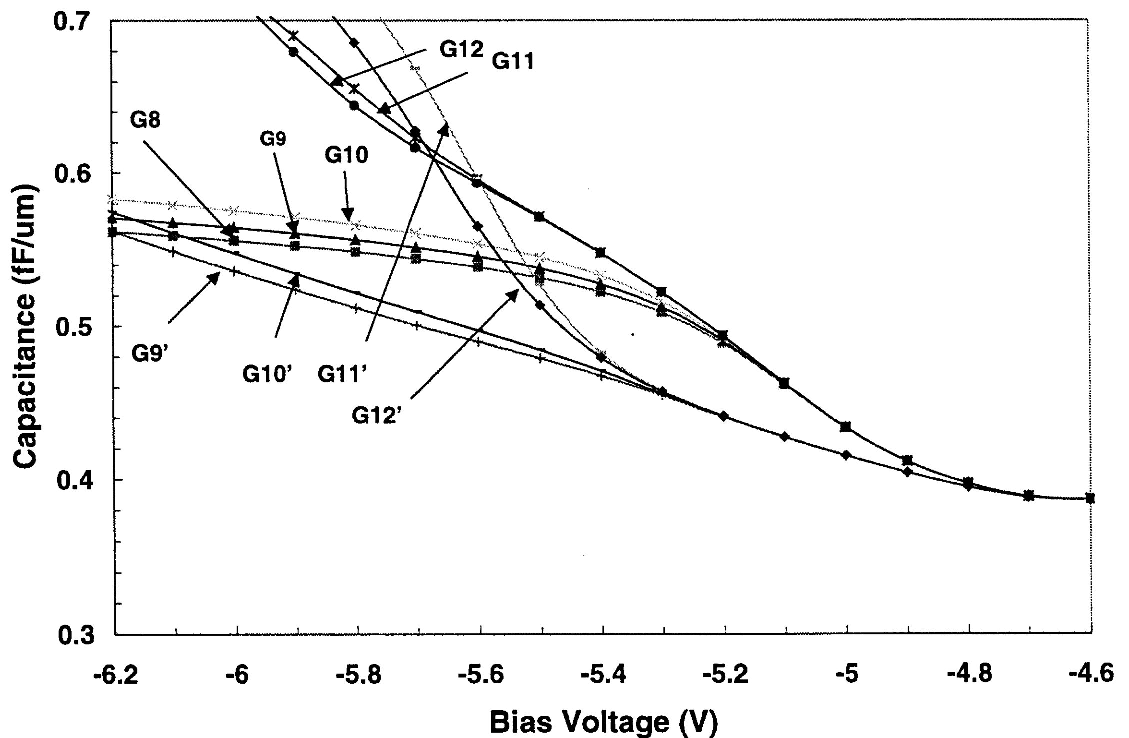


Figure 5.22 Zoomed plot of Figure 5.21 at slight depletion region.

5.2.5 Summary

C-V profiling has been applied to study the effect of plasma etching and subsequent annealing on the valence-band discontinuity E_v at the Si/SiGe interface. The presence of interface trap at SiO_2 deposited by low-pressure CVD process influences heavily to the C-V profile at slight accumulation region. Both the reduction of trap densities and the reduction of ΔE_v, due to relaxation after annealing, affect the C-V profile at that region. This makes the extraction of ΔE_v very difficult. The device simulations have been used to confirm the findings and to provide the insights on the device operation. It indicates that the interface trap has to be below 10^{11} cm^{-2} in order to use C-V profiling at slight accumulation region to detect the E_v change after the plasma etching or high temperature annealing. With moderate level of interface states ($>10^{11}$ cm^{-2}), the relaxation mechanism can be probed using C-V measurement at slight depletion region (as shown in Figure 5.22). Dry etched sample demonstrates a faster relaxation mechanism as compared to its wet etched counterpart due to the creation of dislocation loops by dry etching.

CHAPTER 6

CONCLUSIONS

This research has made two significant contributions in the area of evaluating plasma induced damage: 1) application-oriented measurement of Si MOS capacitor for evaluating the plasma induced damage processed by an advanced inductively coupled plasma (ICP) reactor; 2) research-oriented measurements and simulations of strained SiGe devices for gaining a fundamental understanding of plasma induced electrical and physical damages to heterojunction material, and for developing a fast detection technique.

Electrical characterizations such as C-V, RVB and DLTS measurements, and physical analysis such as XPS were employed to investigate the plasma induced damage to thin oxide processed by ICP reactor under different operating conditions. The shift of flat band voltage, the reduction of breakdown voltage and the creation of high interface trap density were found to be in good agreement with the creation of suboxidation states at Si/SiO_2 interface. The major mechanism responsible for damage appeared to be high-energy electron charging when only the ICP power was activated without any bias to the wafer-carrying electrode. Energetic particle bombardment damage was dominant when the wafer-carrying electrode was biased and the damage was considerable for rf bias power greater than 35 W. A statistical distribution of breakdown voltage was used to investigate the plasma induced damage in thin oxide.

The SF_6 plasma used to etch an overlying Si film stopping at the $Si_{1-x}Ge_x$ strained film caused electrical damage to an underlying $Si_{1-x}Ge_x/Si$ heterojunction device. The changes of C-V and I-V characteristics, such as higher depletion capacitance and lower

diffusion current were attributed to ion bombardment and radiation-induced bonding change, such as creation of interface charges and recombination centers. The TEM analysis revealed the dislocation loops in Si/$Si_{1-x}Ge_x$ /Si outside the aluminum region due to the ion bombardment stress. The O_2 plasma ashing has no strong effect to $Si_{1-x}Ge_x$ device when the device was protected by aluminum contact layer.

C-V profiling has been applied to study the effect of plasma etching and subsequent annealing on the valence-band discontinuity ΔE_v at the Si/SiGe interface of SiGe MOS capacitor. The presence of interface trap at SiO_2 deposited by low-pressure CVD process created big kink at C-V profile at accumulation region. The change of C-V profile was caused by the reduction of trap densities as well as the reduction of ΔE_v due to relaxation after high temperature annealing. The interference from these traps made the extraction of ΔE_v very difficult. The device simulations have been used to confirm the findings and to provide the insights on device operation. By carefully evaluating the C-V profile at slight depletion region the band gap modifications due to process-induced damage could be distinguished. When compared with experimental results it was found that the dry etched sample was partially relaxed after 700°C annealing and wet etched sample was partially relaxed after 800°C annealing. Dry etched sample demonstrated a faster relaxation mechanism as compared to its wet etched counterpart due to the creation of dislocation loops in strained SiGe layer by dry etching process.

A PC based DLTS system has been developed to carry out this research. This DLTS system is consists of MMR Technologies Cryogenic Cooling System, MMR Technologies K-20 temperature controller and a vacuum pump, Boonton 7200 Capacitance Meter and a computer. A BASIC program was written to control the

temperature and to do the data acquisition through GPIB card and data acquisition card. This extremely efficient transient data acquisition system allows a single transient to be sampled up to 11 (or more) different sample rates without changing the hardware configuration as compared using a conventional dual-gated signal averager (double boxcar). This system is very useful for observing a wide variety of traps in semiconductors.

6.1 Suggestions for Future Work

Several continuations and new directions are suggested by the present thesis.

The Atlas Device Simulator has demonstrated its effectiveness to explain and predict the experimental results. It should be used extensively for future device design and experiment design.

C-V profiling technique has potential application for estimating the change of band gap of $Si_{1-x}Ge_x$ exposed to plasma etching and subsequent annealing process. This application should be investigated with low trap density SiO_2 as discussed in Chapter 5. In addition to reducing the SiO_2 interface trap density, the Si control capacitors without $Si_{1-x}Ge_x$ well can be used as control samples. These control samples should go through the same process steps as the SiGe MOS capacitors. The difference of C-V profile between the SiGe and its Si counterpart will provide useful information for extracting the ΔEv after each process step. The measurements and simulations in appropriate regions should be carried out with care and high resolution as shown in Figure 5.22.

APPENDIX A

EXAMPLE OF ATLAS INPUT FILE

This is the input file used for simulation of structure G1 in Chapter 5.

```
# SiGe pMOS simulation: High Frequency C-V Curve
# Wei Zhong
# 2/23/2001, for Ph. D dissertation
# SiGe energy bandgap Eg=1.013 eV
# Disable Qf=5e11 cm^-2 at SiO2/Si
# Disable Qt=3.5 cm^-2 at Si/SiGe

go atlas
```

 # Structure specification

```
mesh infile=pMOS_SiGe.str master.in
save outfile=temp.str master.out
```

 # Material Models Specification

```
material material=Si eg300=1.12 align=0.
material material=SiGe eg300=1.013
material region=1 eg300=7

contact name=anode workfunction=4.1
contact name=cathode con.resistance=1e-7

# Non ideal case
# Unmark following line if want to add fixed charge to SiO2/Si interface
# interface qf=5e11 x.min=0 x.max=3 y.min=0.035 y.max=0.045
# Unmark following line if want to add interface trap to SiO2/Si interface
# inttrap region=1 donor density=3.5e12 e.level=0.3 degen=1 sign=1e-16 sigp=1e-17

model srh auger conmob fldmob evsatmod=1 print

output charge e.field con.band val.band qfn qfp qss ox.charge band.param traps u.srh \
    u.radiative u.auger e.velocity e.mobility h.velocity h.mobility
```

 # Numerical Method Selection

```
method newton itlimit=12 dvmax=1 maxtrap=10 carr=2 vsatmod.inc=0.0075
```

 # Solution Specification

```
solve init
solve outf=zero_bias.str master
tonyplot zero_bias.str
solve vanode=0 outf=zero
load infile=zero
solve vanode=0 vstep=0.1 vfinal=1.9 name=anode
solve vanode=2 outf=2v_bias.str master
load infile=zero
solve vanode=0 vstep=-0.1 vfinal=-1.9 name=anode
solve vanode=-2 outf=m2v_bias.str master
tonyplot 2v_bias.str
tonyplot m2v_bias.str

# Ramp up frequency to 1 MHz
solve previous ac freq=1 direct
solve ac freq=10 fstep=10 mult.f nfstep=5 direct
solve ac freq=1e6 outf=nill

#Reverse Hi C-V
log outf=rev.log master s.param inport=anode outport=cathode width=1
solve ac vanode=0 vstep=-0.1 name=anode vfinal=-10 freq=1e6 direct
log off
#Forward Hi C-V
load infile=nill
log outf=forw.log master s.param inport=anode outport=cathode width=1
solve ac vanode=0 vstep=0.1 name=anode vfinal=2 freq=1e6 direct

# Results Analysis

# Display C-V curve
tonyplot -overlay rev.log forw.log

quit
```

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